

Section 1 Overview

1.1 Features

This LSI includes 1.8 GHz Quad Arm® Cortex®-A55 on-chip FPU, Neon™, L1-caches and L3-cache, 800 MHz Dual Arm® Cortex®-R8 on-chip FPU, TCM, and L1-cache, 200MHz Arm® Cortex®-M33 on-chip FPU and DSP-extension, DRP-AI, Mali™-G31 (GE3D), Mali™-C55 (ISP), 6 MB of on-chip SRAM, 2ch GbEthernet MAC, USB2.0, USB3.2 Gen 2x1, 4-MIPI® CSI-2® camera input interface, 1-MIPI® DSI® video output interface, PCIe® Gen3 4Lane or 2-2Lane (EP/RC), various communication interfaces such as xSPI, eMMC™, I2S (TDM), I3C®, PDM, and security functions.

■ CPU

- On-chip Quad 64-bit Arm® Cortex®-A55 Core processors
Application processing (up to 1.8 GHz)
- On-chip Dual 32-bit Arm® Cortex®-R8 (MPCore™) processors
Real-time processing (up to 800 MHz)
- 32-bit Arm® Cortex®-M33 processor
System management (up to 200 MHz)

■ Accelerator engines

- AI accelerator (dynamically reconfigurable processor for AI (DRP-AI))
- Dynamically reconfigurable processor (DRP)
- 3D graphics engine (GE3D) (option)
- Image signal processor (ISP) (option)
- Image scaling unit (ISU)
- Video codec unit (VCD)

■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (6-Mbyte on-chip SRAM with ECC)
- External DDR memory interface
2-channel memory controller for LPDDR4-3200 or LPDDR4X-3200 with a 32-bit bus width
- xSPI interface
- SDHI (eMMC/SD (1-, 4-, 8-bit bus width) supported)

■ Boot

- Selectable boot CPU from Cortex®-M33 or Cortex®-A55

■ Extended-function timers

- 32-bit general-purpose timer (16 ch.)
- 32-bit CMTW (8 ch.)

■ Various communication/storage/network interfaces

- Ethernet (2 ch.: 10/100/1000 BASE)
- USB2.0 (1 ch.: Host/Function, 1 ch.: Host-only)
- USB3.2 Gen2 × 1 (2 ch.: Host-only)
- PCIe Gen3 (1, 2, or 4 lanes × 1 pair or 1 or 2 lanes × 2 pairs)
- MIPI CSI-2 (4 ch.: 1, 2, or 4 lanes)
- MIPI DSI (1 ch.: 1, 2, or 4 lanes)
- CAN/CANFD (compliant with ISO11898-1) (6 ch.)
- SCI (10 ch.: UART/SPI/I2C-host)
- SPI (3 ch.)
- I2C (9 ch.)
- I3C (1 ch.)

■ Audio

- Asynchronous sampling rate converter unit (SCU) (up to 192 kHz)
- DMAC for Audio (ADMAC) is available to transfer audio formats of I2S with SCU.
- Flexible audio clock generator (ADG) for audio functions.
- I2S (TDM) input/output interfaces (half-duplex 10 ch.; full-duplex 5 ch.)
- SPDIF input/output interfaces (3 ch.)
- Pulse density modulation (PDM) input interfaces (6 ch.)

■ Analog/Digital converter (ADC) and sensors

- 2.5 Msps 12-bit ADC (8 ch.)
- Internal temperature sensors (2 ch.)

■ Security

- Hardware cryptographic engine (option)

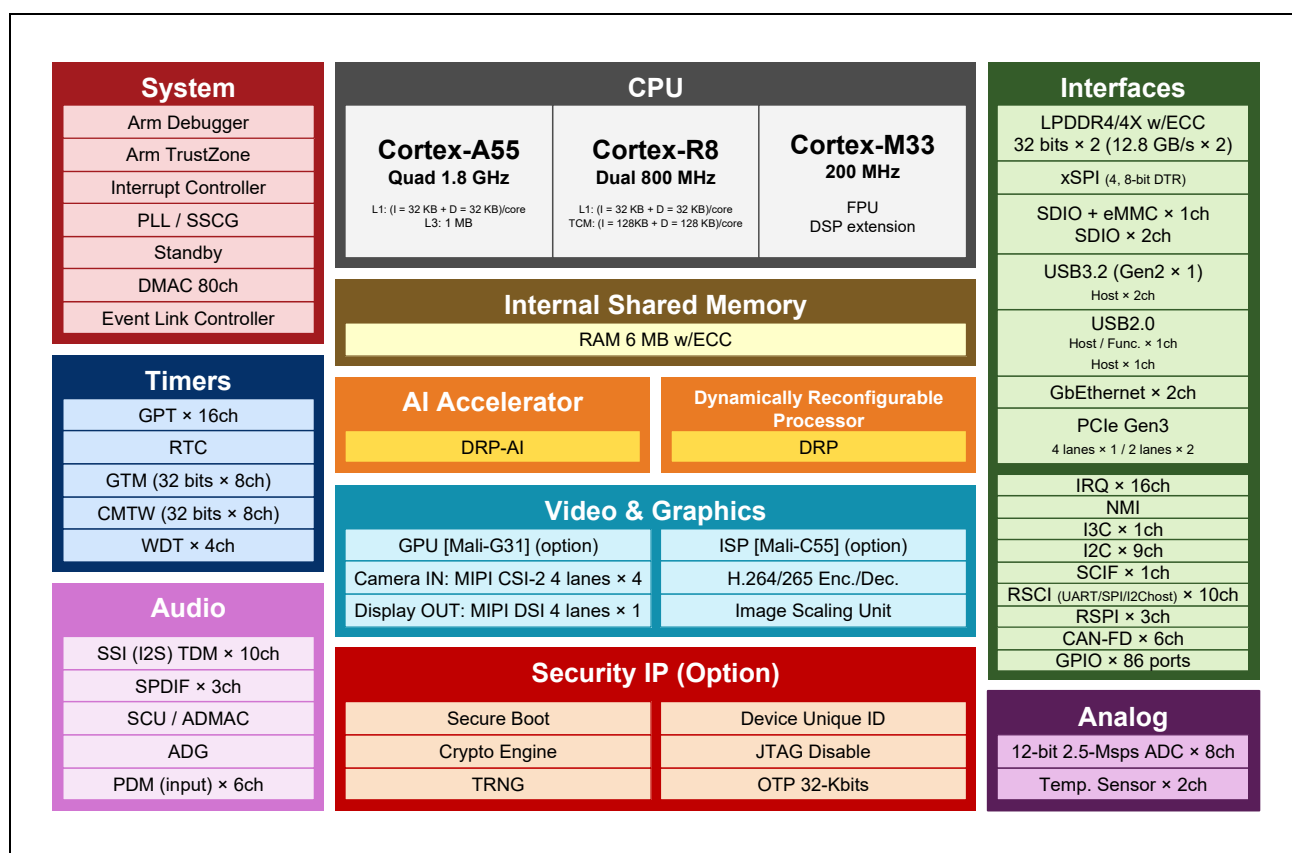


Figure 1.1-1 Diagram of Functional Overview

1.2 Product Lineup

Table 1.2-1 Product Lineup

Group	Name	Part Number	GE3D	Security	ISP
RZ/V2H	RZ/V2H	R9A09G057H41GBG	N/A	N/A	N/A
		R9A09G057H42GBG	Available (Mali-G31)		
		R9A09G057H45GBG	N/A	Available	
		R9A09G057H46GBG	Available (Mali-G31)		
	RZ/V2HP	R9A09G057H44GBG	Available (Mali-G31)	N/A	Available (Mali-C55)
		R9A09G057H48GBG	Available (Mali-G31)	Available	

Note: “#ACx” or “#BCx” is added to the end of part numbers. “#ACx” is packaged in the individual tray, and “#BCx” is packaged in the full carton.

1.3 Functions

The following tables list the functions of this LSI.

Table 1.3-1 CPU

Item	Description
Application Processor Cortex-A55 (CA55)	• Arm Cortex-A55 Quad Core 1.8 GHz with 0.9 V, 1.1 GHz with 0.8 V • L1 I-cache 32 Kbytes (with parity) and D-cache 32 Kbytes (with ECC) per core • L2 cache: 0 Kbyte • L3 cache: 1 Mbyte (with ECC)*1 • MMU supported • Neon™ and FPU supported • Cryptographic extension supported (for security-supported products only) • Armv8-A architecture
Realtime Processor Cortex-R8 (CR8)	• Arm Cortex-R8 Dual MPCore 800 MHz • L1 I-cache 32 Kbytes (with ECC) and D-cache 32 Kbytes (with ECC) per core • I-TCM 128 Kbytes (with ECC) and D-TCM 128 Kbytes (with ECC) per core • VFPv3, double precision • Armv7-R architecture • No support for dual-link lock-step technology
System Manager Cortex-M33 (CM33)	• Arm Cortex-M33 processor 200 MHz • FPU supported • DSP extension supported • Security extension supported • Armv8-M architecture
Debug Interface	• Arm® CoreSight® architecture • JTAG and SWD interfaces supported • ETF: Total of 60 Kbytes for program flow tracing • JTAG disabling supported (option)
Boundary Scan	• Boundary scan based on IEEE 1149.1 via the JTAG interface is supported. • Note that some module pins are not available on this boundary scan.

Note 1. The maximum operating frequency of the L3 cache is 1.26 GHz.

Table 1.3-2 Accelerator Engines

Item	Description
Dynamically reconfigurable processor (DRP)	• DRP (DRP1)
AI accelerator (DRP-AI)	• DRP-AI (AI-MAC + DRP0) • Up to 8 dense TOPS • Up to 80 sparse TOPS
3D Graphics Engine (GE3D) (option)	• Arm Mali-G31 • One single-pixel shader core • 8-Kbyte L2 cache • OpenGL ES™ 1.1, 2.0, and 3.2 supported • OpenCL 2.0 full profile supported
Image Signal Processor Unit (ISP) (option*) *RZ/V2HP only	• Arm Mali-C55 • 1 unit, supporting 4K • Maximum pixel rate: 630 Mpixels/s • Supports the functions below: – Black level correction – WB gain – Defect pixel correction – Color correction – Gamma correction – Edge enhancement and sharpness filter – Down-scaling and cropping – Dynamic range correction – 2-exposure HDR – Shading correction • Supports input formats: RAW8, 10, 12, 14, 16, 20 • Supports output formats: YUV422, YUV420, RGB
Image Scaling Unit (ISU)	• Scaling down function with bilinear interpolation • Input image size (max): 4096 × 4096 • Output image size (max): 4096 × 4096 • Supports color format: RGB/ARGB, YCbCr/YUV, RAW (Grayscale)
Video Codec Unit (VCD)	• H.264/H.265 codec module • Support for encoding and decoding – H.264/AVC (High Profile, level 4.2; Main Profile, level 4.2; Baseline Profile, level 4.2) – H.265/HEVC (Main Profile, level 5) • Maximum size – (H.264) 1920 × 1080 × 60 fps*1 – (H.265) 3840 × 2160p × 30 fps*1 • I-/P-slice supported for H.264/H.265 encoding • I-/P-/B-slice supported for H.264/H.265 decoding

Note 1. Maximum frame rate for this size. The number of streams can be defined within this specification by software.

Table 1.3-3 On-chip SRAM and External Memory Interfaces

Item	Description
System RAM	• 6 Mbytes (with ECC)
External Bus Controller for LPDDR4/4X SDRAM (DDR)	• 2 channels • Support for LPDDR4-3200 and LPDDR4X-3200 • Bus width: 32-bits • In line ECC (16 ECC regions) supported (support for error detection interrupts)*¹ • Memory size: Up to 16 Gbytes (8 Gbytes per channel) • Auto-refresh, self-refresh, and IO retention supported • Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported)
xSPI Controller (xSPI)	• 1 channel (2 chip select signals) • Compliant with the xSPI protocol • Protocol mode 1, 4, or 8 pins with SDR or DDR (1S-1S-1S, 4S-4D-4D, 8D-8D-8D)*¹ 2 or 4 pins with SDR (1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S) • Support for XiP mode • Support for up to 256-Mbyte address space (support for up to 128M bytes per channel address space in boot sequence)
SD Card Host Interface/ Multimedia Card Interface (SD/MMC)	• 3 channels • Channel 0 supports SDHI and e-MMC. • Channels 1 and 2 support SDHI. • SD memory I/O card interface (1-bit or 4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD specification version 3.01 • Default, high-speed, UHS-I/SDR50, SDR104 and DDR50 transfer modes supported • Error check function: CRC7 (command), CRC16 (data) • Support for card detection and write protection • MMC interface (1-bit, 4-bit, or 8-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 4.51 • High-speed, HS200 and HS-DDR transfer modes supported

Note 1. This function is supported by the devices other than "#AC0" and "#BC0". "#AC0" and "#BC0" do not support it (see **Table 1.2-1**).

Table 1.3-4 Boot

Item	Description
Boot	• Boot CPU selectable as CA55 and CM33 • CM33 boot – Boot mode 2: Booting from a serial flash memory connected to the xSPI bus space – Boot mode 3: Booting from SCIF download • CA55 boot – Boot mode 0: Booting from eSD – Boot mode 1: Booting from eMMC – Boot mode 2: Booting from a serial flash memory connected to the xSPI bus space – Boot mode 3: Booting from SCIF download <i>Note:</i> 1.8 V or 3.3 V selectable for eMMC and xSPI interfaces.

Table 1.3-5 System, Data Transfer, Enhanced Interrupt Controller Unit, Clock Functions

Item	Description
Direct Memory Access Controller (DMAC)	• 80 channels • Transfer modes: Single transfer mode and block transfer mode • LINK mode (DMA transfer under descriptor control) supported • Transfer size: 1, 2, 4, 8, 16, 32, 64, or 128 bytes • Transfer request: Software trigger, external DMA requests (DREQ) and interrupt requests from peripheral functions • A specific DMA transfer interval can be specified to adjust the bus occupancy.
Clock Pulse Generator (CPG)	• Generates the clocks from an external clock or external resonator (24 MHz). – Maximum CA55 clock: 1.8 GHz (0.9 V), 1.1 GHz (0.8 V) – Maximum CR8 clock: 800 MHz – Maximum CM33 clock: 200 MHz – Maximum DDR clock: 800 MHz (LPDDR4/4X-3200) – Maximum GE3D clock: 630 MHz – Maximum ISP clock: 630 MHz – Maximum H.264/H.265 clock: 400 MHz – Maximum system bus clock: 400 MHz • SSC (spread spectrum clock) supported
Interrupt Controller (GIC)	• Arm® CoreLink® generic interrupt controller (GIC-600) for CA55 • 32 priority levels available • Nested vectored interrupt controller (NVIC) for CM33 • Integrated interrupt controller (NVIC) for CR8 • External Interrupt pins (NMI, IRQ0 to IRQ15, and TINT0 to TINT31) • On-chip peripheral Interrupts: Priority level set for each module
Event Link Controller (ELC)	• Up to 455 event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event-linked operation of signals of 16 port pins, P60 to 67 and P80 to 87, is to be possible.
Error Controller	• Error events from CPU and peripherals are captured and merged to interrupt with mask for CA55 and CM33 respectively. • System reset can be generated by error events.
Message Handling Unit (MHU)	• Message handling function between the cores of CA55, CR8 and CM33 • Assert interrupts to inform messages and responses from/to every core

Table 1.3-6 Various Communication/Storage/Network Interfaces (1/3)

Item	Description
USB3.2 Host (USB3)	• 2 channels • Compliant with USB3.2 Gen2 × 1 • Maximum rate: 10 Gbps • Support for control, bulk, interrupt, and isochronous transfer • Internal dedicated DMA
USB2.0 Host/Function (USB2)	• 2 channels (ch. 0: Host/Function; ch. 1: Host-only) • Compliant with USB2.0 • Support for On-The-Go (OTG) functionality (ch. 0 only) • Support for control, bulk, interrupt, and isochronous transfer • Internal dedicated DMA
PCI Express® 3.0 (PCIE)	• PCIe Gen3 • Root complex or Endpoint selectable • Lane configuration selectable from below: – 1, 2, or 4 lanes × 1 channel – 1 or 2 lanes × 2 channels
MIPI CSI-2 Interface with camera image processing (CRU)	• 4 channels • Number of lanes: 1, 2, or 4 lanes per channel • Maximum bandwidth: 2.1 Gbps per lane • Support for the throughput up to 4K RAW12 60 fps • Support for 4 virtual channels selected from VC0 to VC15 • Support for input data formats: – YUV422 8 bits or 10 bits – RGB444, RGB555, RGB565, RGB666, RGB888 – RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20 – YUV420 8-bits or 10-bits (image processing not supported) – Legacy YUV420 8-bits (image processing not supported) – YUV420 8-bits or 10-bits (chroma shifted pixel sampling) (image processing not supported) – User defined byte-based data • The other formats from the MIPI CSI-2 interface can also be output without image processing. • Generic long packet data types 1 to 4 • User defined 8-bit data types 1 to 8
MIPI DSI Interface with LCD controller (LCDC)	• 1 channel • Number of lanes: 1, 2, or 4 lanes • Support for the throughput up to 1920 × 1200 RGB888 60 fps • Support for the throughput up to 1280 × 1024 RGB888 120 fps • Maximum bandwidth: 1.5 Gbps per lane • Support for 2-plane blending (with the ability to blend 2 differently sized images) • Support for image processing: – Dither processing (RGB666) – Clipping – RGB gamma correction LUT • Support for input data formats: – RGB565, RGB666, RGB888 – ARGB1555, ARGB4444, ARGB8888 – YUV (YcbCr) 444 8-bits, YUV (YcbCr) 422 8-bits, YUV (YcbCr) 420 8-bits • Support for output data formats: – RGB666, RGB888

Table 1.3-6 Various Communication/Storage/Network Interfaces (2/3)

Item	Description
Gigabit Ethernet Interface (GBETH)	• 2 channels • Compliant with IEEE802.3 • Compliant with IEEE802.1Qav, IEEE802.1Qat, and IEEE802.1AS • Compliant with IEEE1588-2008 with nano second timer in ch. 0 (main) and ch. 1 (sub) • Support for 10BASE, 100BASE, and 1000BASE • Support for full duplex and half duplex • Support for RGMII and MII Interfaces
CANFD Interface (CANFD)	• 6 channels • CAN-FD ISO 11898-1 (2015) compliant • Support for up to 8 MHz with payload transfer • Message buffer – 64 transmit message buffers per channel – 256 shared buffers for RXMB and FIFO buffers per channel
I3C Bus Interface (I3C)	• 1 channel • Support for 1.2 V and 1.8 V • Master or Slave mode selectable • Support for the multi-master • Compliant with MIPI I3C v1.0 and I3C Basic v1.0 - The following functions are not supported: – Bridge device (I3C v1.0 and I3C Basic v1.0) – Asynchronous timing control async mode 2 & 3 (I3C v1.0) • Support for DMAC and event linking
I2C Bus Interface (RIIC)	• 9 channels • Master or Slave mode selectable • Support for the multi-master • Support for Standard mode (100 kHz), Fast mode (400 kHz), and Fast mode+ (1 MHz) • Support for DMAC and event linking
Renesas Serial Communication Interface (RSCI)	• 10 channels • 6 communication modes – Asynchronous interfaces – 8-bit clock synchronous interface – Simple IIC (host-only) – Simple SPI (with one chip select signal) – Smart card interface – Simple LIN (expanded SCIX mode) • 32-stage FIFO registers for transmission and reception • Clock source selectable from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and half-duplex communications • Data length: 7 to 9 bits • Bit-rate modulation • Double speed mode • Loopback function to enable self-diagnosis • Support for DMAC and event linking • Support for CRC calculation by the CRC unit

Table 1.3-6 Various Communication/Storage/Network Interfaces (3/3)

Item	Description
Renesas Serial Peripheral Interface (RSPI)	• 3 channels • SPI transfer facility The MOSI (master out slave in), MISO (master in slave out), SSL (slave select, 4 channels available), and RSPCK (SPI clock) signals enable serial transfer through SPI operation (four lines). The MOSI, MISO, and RSPCK signals enable clock-synchronous operation (three lines). Capable of handling serial transfer as a master or slave. • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. 32-bit × 16-stage buffers for transmission and reception. Up to 16 frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits). • Buffered structure Independent 16 stages and channels for MOSI and MISO Double buffers for both transmission and reception • RSPCK can be stopped automatically with the reception buffer full for master reception. • Support for DMAC and event link • Support for CRC calculation by the CRC unit
CRC Calculator (CRC)	• 1 channel • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of five generating polynomials: – $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$ (CRC-32) – $X^{32}+X^{28}+X^{27}+X^{26}+X^{25}+X^{23}+X^{22}+X^{20}+X^{19}+X^{18}+X^{14}+X^{13}+X^{11}+X^{10}+X^9+X^8+X^6+1$ (CRC-32C) – $X^{16}+X^{15}+X^2+1$ (CRC-16) – $X^{16}+X^{12}+X^5+1$ (CRC-CCITT) – X^8+X^2+X+1 (CRC-8) • Support for RSCI and RSPI interfaces
Serial Communication Interface with FIFO (SCIF)	• 1 channel • Asynchronous mode • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud-rate generator • Separate 16-byte FIFO registers for transmission and reception

Table 1.3-7 Extended-Function Timers

Item	Description
General-Purpose Timer (GPT)	• 32 bits × 16 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Enabling synchronized operation of the several counters between 2 units • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Automatic generation of three-phase PWM waveforms incorporating dead times through the combination of three counters • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter functions for signals on the input capture and external trigger pins • Event linking by the ELC • Support for phase counting mode
Port Output Enable for GPT (POEG)	• Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRQ pins • Initiation by an output disable request from GPT • Initiation by detection of oscillation stopping or by software
Compare Match Timer W (CMTW)	• 32 bits × 8 channels • Compare-match, input-capture input, and output-comparison output are available (ch. 0 to ch. 3) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events
Watchdog Timer (WDT)	• 4 channels • A counter underflow can reset the LSI.
General Timer (GTM)	• 32 bits × 8 channels • Two operating modes: – Interval timer mode – Free-running comparison mode
Real Time Clock (RTC)	• A 100-year calendar from 2000 to 2099 • BCD code display • Clock source is an oscillator dedicated to RTC (32.768-kHz) • Automatic adjustment function for leap years • Alarm function

Table 1.3-8 Audio

Item	Description
Sampling Rate Converter Unit (SCU)	• 10 channels • Sampling rate: Up to 192 kHz • Asynchronous/synchronous sampling rate conversions are available. • Support for resolutions of up to 24 bits • High-sound-quality type (THD + N*1 is -132 dB) and general-sound-quality type (THD + N*1 is -96 dB) • Automatically generates antialiasing filter coefficients • Four modules support one, two, four, six, or eight channels, and six modules support one or two channels. <i>Note 1.</i> Total harmonic distortion plus noise
Audio Clock Generator Unit (ADG)	• Supplies clock signals to the SSIU, SCU and SPDIF module.
Direct Access Memory Controller for Audio (ADMAC)	• Allows transfer of L/R data via I2S • 29 channels • Controls data transfer between the audio modules (SSIU, SCU)
Serial Sound Interface Unit (SSIU)	• 10 channels for half-duplex communication with transmit or receive function • 5 channels for full-duplex communication (full-duplex pairing: ch. 0 & 9, ch. 1 & 2, ch. 3 & 4, ch. 5 & 6, ch. 7 & 8) • Support for I2S, monaural, and TDM audio formats • Support for master and slave functions • Generation of programmable word clocks and bit clocks • Multi-channel formats • Support for 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support for WS (word select) signal continuation with which the WS signal is not stopped • Support for DMAC
SPDIF Interface (SPDIF)	• 3 channels • Support for the IEC 60958 standard (stereo and consumer use modes only) • Sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Bi-phase mark encoding • Double buffered data • Parity encoded serial data • Support for DMAC
Pulse Density Modulation (PDM)	• 6 channels • Direction: Input • Sampling rate: 8, 10, 12, 15, 16, 20, 24, 25, 30, 40, or 48 kHz • Capable of filtering 1-bit digital input data and converting them into 20-bit or 16-bit digital data • Support for the stereo microphone (L/R sampling by rising/falling clock edge) • Support for the sound activity detector to wake up CPU from WFI • Support for DMAC

Table 1.3-9 12-bit Analog to Digital Converter

Item	Description
A/D Converter (ADC0)	• 8 channels • Resolution: 12 bits • Input range: 0 V to 1.8 V • Conversion rate: 2.5 Msps, 2.0 Msps, 1.0 Msps, 0.5 Msps, 0.25 Msps • Operation mode: Single scan, continuous scan, group scan • Condition for starting A/D conversion – Software trigger – Asynchronous trigger: External ADTRG trigger supported – Synchronous trigger: ELC and GPT timers • Interrupt sources: A/D scan end, window compare match, compare match/mismatch, data register overwrite

Table 1.3-10 Internal Sensors

Item	Description
Temperature Sensor Unit (TSU)	• 2 channels for internal temperature • Includes a 12-bit A/D convertor per unit • Resolution: 0.0625°C/code • Range: -40°C to 125°C • Precision: ±5°C • Conversion rate: 14.9 ksps • Operation mode: Single scan • Condition for starting measurement – Software trigger – Synchronous trigger: ELC • Interrupt sources: Conversion end, window compare match

Table 1.3-11 Security

Item	Description
Trusted Secure IP (option)	• Security algorithm – Common key encryption: AES – Non-common key encryption: RSA, ECC • Other features – TRNG (true-random number generator) – Hash value generation: SHA-1, SHA-224, SHA-256, GHASH – Support for unique ID

Table 1.3-12 General-Purpose I/O Pins

Item	Description
General-purpose I/O ports (GPIO)	• Multiple I/O pins: 86 pins • Selectable: Pulling up or down by register settings • Selectable: N-ch. open-drain mode, Schmitt mode • 3.3-V tolerant pins available for use: 75 • Selectable IO-voltages for eight power blocks (7 blocks: 1.8 V or 3.3 V; 1 block: 1.2 V or 1.8 V)

Table 1.3-13 Power Supply Voltage

Item	Description
Power supply voltage	• VDD (core): 0.8 V • VDD (CA55): 0.8 V or 0.9 V • VDD (ADC, TSU, OTP): 1.8 V • VDD (DDR IO): 1.1 V, 0.6 V (only 0.6 V: for LPDDR4X) • VDD (MIPI DPHY): 1.2 V, 1.8 V (only 1.8 V: for MIPI CSI-2) • VDD (others): 1.8 V, 3.3 V

Table 1.3-14 Temperature Range

Item	Description
Junction temperature (Tj)	• -40°C to +125°C

Table 1.3-15 Quality Level

Item	Description
Quality level	• Industrial usage, etc.

Table 1.3-16 Package

Item	Description
Package	• 1368-pin FCBGA, 19-mm square, 0.50-mm pitch

1.4 Block Diagram

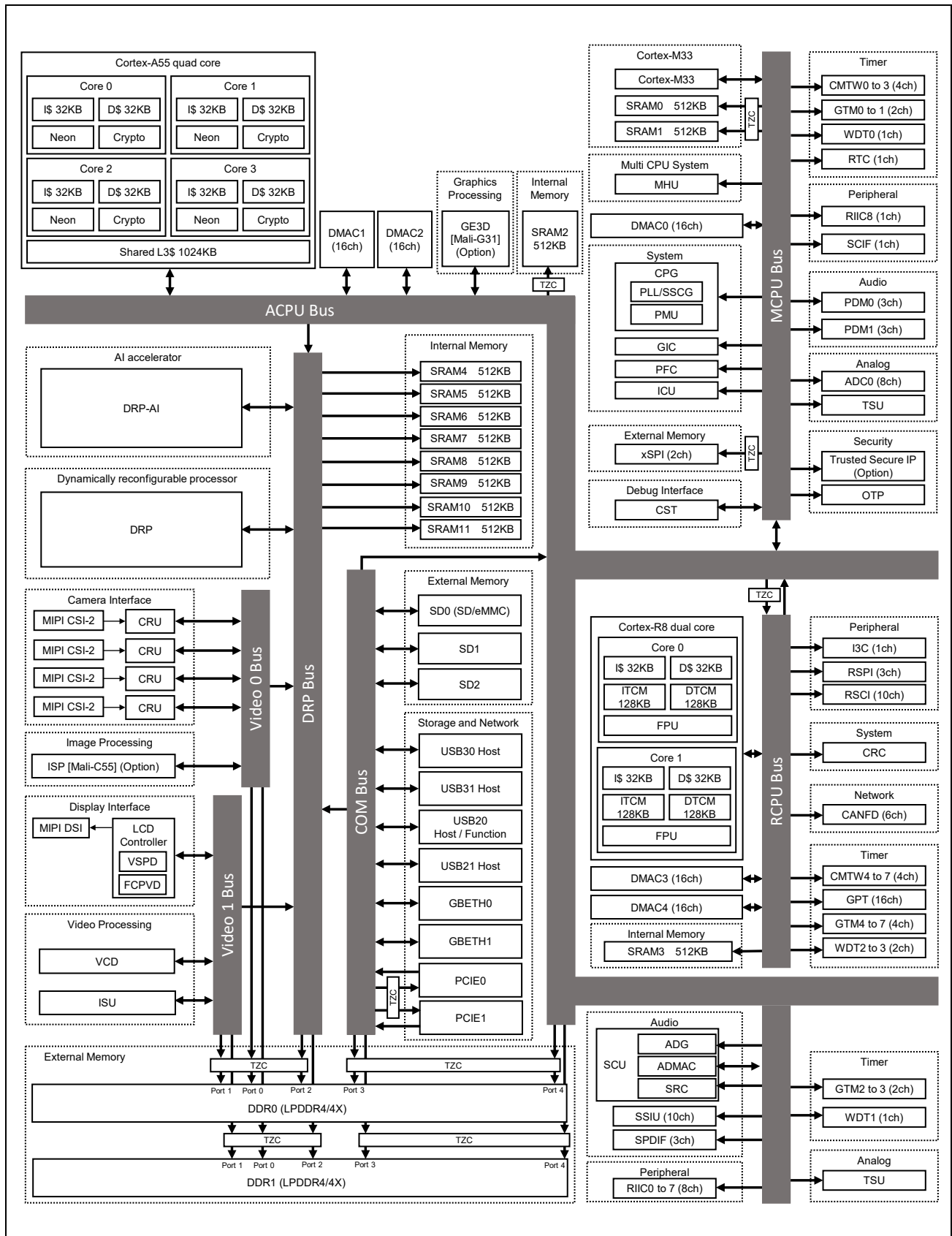


Figure 1.4-1 Block Diagram

Table 1.4-1 List of Units (1/2)

Unit Name	Unit Number	Function
ADC	ADC0	A/D converter
ADG	—	Audio clock generator
ADMAC	—	DMAC for audio
CA55	—	Arm Cortex-A55
CANFD	CANFD0	CAN-FD interface
CM33	—	Arm Cortex-M33
CMTW	CMTW0 to CMTW7	Compare match timer
CPG	—	Clock pulse generator
CR8	—	Arm Cortex-R8
CRC	—	CRC operation unit
CRU	CRU0 to CRU3	Camera data receive unit (MIPI CSI-2 interface)
CST	—	Debug interface (Arm CoreSight)
DDR	DDR0, DDR1	LPDDR4/4X controller
DMAC	DMAC0 to DMAC4 (each 16 ch.)	Direct memory access (DMA) controller
DRP	DRP1	Dynamically reconfigurable processor
DRP-AI	DRP0 and AI-MAC	AI accelerator
ELC	—	Event link controller
GBETH	GBETH0, GBETH1	Gigabit Ethernet interface
GE3D	—	3D graphics engine
GIC	—	Generic interrupt controller
GPT	GPT0, GPT1 (each 8 ch.)	General purpose timer
GTM	GTM0 to GTM7	General timer
GPV	—	Global programmers view
I3C	I3C0	I3C bus interface
ICU	—	Interrupt control unit
ISP	—	Image signal processor
ISU	—	Image scaling unit
LCDC	—	LCD controller
MHU	—	Message handling unit
OTP	—	One time programmable memory
PCIE	PCIE0, PCIE1	PCI Express 3.0 interface
PCU	—	Power control unit
PDM	PDM0, PDM1	Pulse density modulation (PDM) interface
PFC	—	Pin function controller
POEG	POEG0, POEG1	Port output enable for GPT
PMU	—	Power management unit
PWC	—	Power sequence controller
RIIC	RIIC0 to RIIC8	I2C bus interface
RSCI	RSCI0 to RSCI9	Serial communication interface
RSPI	RSPI0 to RSPI2	Serial peripheral interface
RTC	—	Real time clock
SCIF	SCIF0	Serial communication interface with FIFO
SD	SD0 to SD2	SD/MMC host interface
Secure IP	—	Trusted secure IP

Table 1.4-2 List of Units (2/2)

Unit Name	Unit Number	Functional Overview
SRAM	SRAM0 to SRAM11	SRAM
SRC	—	Sampling rate controller
SSIU	—	Serial sound interface unit
SYC	—	System counter
SYS	—	System controller
SYSTEM BUS	—	Internal bus
ACPU Bus	—	A bus connected to Cortex-A55, DDR memory controllers, SRAM, and its peripheral units
RCPU Bus	—	A bus connected to Cortex-R8, SRAM, and its peripheral units
MCPU Bus	—	A bus connected to Cortex-M33, SRAM, its peripheral units, and the system control units
DRP Bus	—	A bus connected to DRP, DRP-AI, SRAM, and DDR memory controllers
Video 0 Bus Video 1 Bus	—	A bus connected to image processing units and DDR memory controllers
COM Bus	—	A bus connected to communication interface units and DDR memory controllers
TSU	TSU0, TSU1	Temperature sensor unit
TZC	—	CoreLink™ TrustZone Address Space Controller
USB2	USB20, USB21	USB2.0 host / function interface
USB3	USB30, USB31	USB3.2 host interface
VCD	—	H.265/H.264 multi codec
WDT	WDT0 to WDT3	Watchdog timer
xSPI	xSPI0	xSPI controller

This section describes the pins of this LSI.

[illegible]

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Table 2.1-1 Ball Numbers and External Pin Names (1/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
A1	V _{SS}	B1	DDR0_DQA15	C1	DDR0_DMIA1	D1	DDR0_DQA12
A2	DDR0_DMIA0	B2	V _{SS}	C2	DDR0_DQA9	D2	DDR0_DQA13
A3	DDR0_DQA0	B3	DDR0_DQA1	C3	V _{SS}	D3	DDR0_DQA11
A4	DDR0_DTEST	B4	DDR0_DQA2	C4	DDR0_DQA5	D4	V _{SS}
A5	DDR0_ATEST	B5	V _{SS}	C5	DDR0_DQA3	D5	DDR0_DQA6
A6	DDR0_CSA0	B6	DDR0_CKEA0	C6	V _{SS}	D6	DDR0_DQA4
A7	DDR0_CSA1	B7	DDR0_CAA4	C7	DDR0_CAA2	D7	V _{SS}
A8	DDR0_VDDQ	B8	V _{SS}	C8	DDR0_CAA3	D8	DDR0_CKEA1
A9	DDR0_VDDQ	B9	DDR0_VDDQ	C9	DDR0_VDDQ	D9	V _{SS}
A10	DDR0_VDDQ	B10	DDR0_CAB4	C10	DDR0_CAB2	D10	DDR0_CKEB1
A11	DDR0_VDDQLP	B11	V _{SS}	C11	V _{SS}	D11	V _{SS}
A12	DDR0_VDDQLP	B12	DDR0_CKEB0	C12	DDR0_CAB0	D12	DDR0_CAB5
A13	DDR0_ZN	B13	DDR0_VDDQLP	C13	DDR0_VDDQLP	D13	V _{SS}
A14	DDR0_DQB1	B14	DDR0_DQB4	C14	DDR0_DQB3	D14	DDR0_DQB2
A15	DDR0_DMIB0	B15	V _{SS}	C15	V _{SS}	D15	V _{SS}
A16	DDR0_DQB7	B16	DDR0_DQB12	C16	DDR0_DQB6	D16	DDR0_DQB9
A17	DDR0_DMIB1	B17	V _{SS}	C17	V _{SS}	D17	V _{SS}
A18	DDR0_DQB11	B18	DDR0_DQB13	C18	DDR0_DQB15	D18	DDR0_DQB8
A19	V _{SS}	B19	V _{SS}	C19	V _{SS}	D19	V _{SS}
A20	DDR1_DQB11	B20	DDR1_DQB13	C20	DDR1_DQB15	D20	DDR1_DQB8
A21	DDR1_DMIB1	B21	V _{SS}	C21	V _{SS}	D21	V _{SS}
A22	DDR1_DQB7	B22	DDR1_DQB12	C22	DDR1_DQB6	D22	DDR1_DQB9
A23	DDR1_DMIB0	B23	V _{SS}	C23	V _{SS}	D23	V _{SS}
A24	DDR1_DQB1	B24	DDR1_DQB4	C24	DDR1_DQB3	D24	DDR1_DQB2
A25	DDR1_ZN	B25	DDR1_VDDQLP	C25	DDR1_VDDQLP	D25	V _{SS}
A26	DDR1_VDDQLP	B26	DDR1_CKEB0	C26	DDR1_CAB0	D26	DDR1_CAB5
A27	DDR1_VDDQLP	B27	V _{SS}	C27	V _{SS}	D27	V _{SS}
A28	DDR1_VDDQ	B28	DDR1_CAB4	C28	DDR1_CAB2	D28	DDR1_CKEB1
A29	DDR1_VDDQ	B29	DDR1_VDDQ	C29	DDR1_VDDQ	D29	V _{SS}
A30	DDR1_VDDQ	B30	V _{SS}	C30	DDR1_CAA3	D30	DDR1_CKEA1
A31	DDR1_CSA1	B31	DDR1_CAA4	C31	DDR1_CAA2	D31	V _{SS}
A32	DDR1_CSA0	B32	DDR1_CKEA0	C32	V _{SS}	D32	DDR1_DQA4
A33	DDR1_ATEST	B33	V _{SS}	C33	DDR1_DQA3	D33	DDR1_DQA6
A34	DDR1_DTEST	B34	DDR1_DQA2	C34	DDR1_DQA5	D34	V _{SS}
A35	DDR1_DQA0	B35	DDR1_DQA1	C35	V _{SS}	D35	DDR1_DQA11
A36	DDR1_DMIA0	B36	V _{SS}	C36	DDR1_DQA9	D36	DDR1_DQA13
A37	V _{SS}	B37	DDR1_DQA15	C37	DDR1_DMIA1	D37	DDR1_DQA12

Table 2.1-1 Ball Numbers and External Pin Names (2/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
E1	DDR0_DQA14	F1	V _{SS}	G1	V _{SS}	H1	DSI_DPDATA3
E2	V _{SS}	F2	DDR0_DQSAT1	G2	V _{SS}	H2	DSI_DNDATA3
E3	DDR0_DQA8	F3	DDR0_DQSAC1	G3	V _{SS}	H3	V _{SS}
E4	DDR0_DQA10	F4	V _{SS}	G4	V _{SS}	H4	V _{SS}
E5	V _{SS}	F5	DDR0_DQSAT0	G5	V _{SS}	H5	V _{SS}
E6	DDR0_DQA7	F6	DDR0_DQSAC0	G6	V _{SS}	H6	V _{SS}
E7	DDR0_CAA0	F7	V _{SS}	G7	—	H7	V _{SS}
E8	DDR0_CAA1	F8	DDR0_CKAT	G8	V _{SS}	H8	DSI_VDD18
E9	DDR0_CAA5	F9	DDR0_CKAC	G9	V _{SS}	H9	DSI_VDD18
E10	DDR0_CAB1	F10	V _{SS}	G10	V _{SS}	H10	V _{SS}
E11	DDR0_CAB3	F11	DDR0_CKBT	G11	V _{SS}	H11	DDR0_VDDQLP
E12	DDR0_CSB1	F12	DDR0_CKBC	G12	V _{SS}	H12	DDR0_VDDQLP
E13	DDR0_CSB0	F13	V _{SS}	G13	V _{SS}	H13	V _{SS}
E14	DDR0_RESETN	F14	DDR0_DQSBT0	G14	V _{SS}	H14	DDR0_VAA
E15	DDR0_DQB0	F15	DDR0_DQSBC0	G15	V _{SS}	H15	V _{SS}
E16	DDR0_DQB5	F16	V _{SS}	G16	V _{SS}	H16	DDR0_VDDQLP
E17	DDR0_DQB10	F17	DDR0_DQSBT1	G17	V _{SS}	H17	DDR0_VDDQLP
E18	DDR0_DQB14	F18	DDR0_DQSBC1	G18	V _{SS}	H18	DDR0_VDDQLP
E19	V _{SS}	F19	V _{SS}	G19	V _{SS}	H19	V _{SS}
E20	DDR1_DQB14	F20	DDR1_DQSBC1	G20	V _{SS}	H20	DDR1_VDDQLP
E21	DDR1_DQB10	F21	DDR1_DQSBT1	G21	V _{SS}	H21	DDR1_VDDQLP
E22	DDR1_DQB5	F22	V _{SS}	G22	V _{SS}	H22	DDR1_VDDQLP
E23	DDR1_DQB0	F23	DDR1_DQSBC0	G23	V _{SS}	H23	V _{SS}
E24	DDR1_RESETN	F24	DDR1_DQSBT0	G24	V _{SS}	H24	DDR1_VAA
E25	DDR1_CSB0	F25	V _{SS}	G25	V _{SS}	H25	V _{SS}
E26	DDR1_CSB1	F26	DDR1_CKBC	G26	V _{SS}	H26	DDR1_VDDQLP
E27	DDR1_CAB3	F27	DDR1_CKBT	G27	V _{SS}	H27	DDR1_VDDQLP
E28	DDR1_CAB1	F28	V _{SS}	G28	V _{SS}	H28	V _{SS}
E29	DDR1_CAA5	F29	DDR1_CKAC	G29	V _{SS}	H29	V _{SS}
E30	DDR1_CAA1	F30	DDR1_CKAT	G30	V _{SS}	H30	V _{SS}
E31	DDR1_CAA0	F31	V _{SS}	G31	V _{SS}	H31	V _{SS}
E32	DDR1_DQA7	F32	DDR1_DQSAC0	G32	V _{SS}	H32	V _{SS}
E33	V _{SS}	F33	DDR1_DQSAT0	G33	V _{SS}	H33	V _{SS}
E34	DDR1_DQA10	F34	V _{SS}	G34	V _{SS}	H34	V _{SS}
E35	DDR1_DQA8	F35	DDR1_DQSAC1	G35	V _{SS}	H35	V _{SS}
E36	V _{SS}	F36	DDR1_DQSAT1	G36	V _{SS}	H36	PCIE_TXDNL0
E37	DDR1_DQA14	F37	V _{SS}	G37	V _{SS}	H37	PCIE_TXDPL0

Table 2.1-1 Ball Numbers and External Pin Names (3/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
J1	V _{SS}	K1	DSI_DPDATA2	L1	V _{SS}	M1	DSI_DPDATA0
J2	V _{SS}	K2	DSI_DNDATA2	L2	V _{SS}	M2	DSI_DNDATA0
J3	NC	K3	V _{SS}	L3	DSI_DPCLK	M3	V _{SS}
J4	NC	K4	V _{SS}	L4	DSI_DNCLK	M4	V _{SS}
J5	V _{SS}	K5	NC	L5	V _{SS}	M5	DSI_DPDATA1
J6	V _{SS}	K6	NC	L6	V _{SS}	M6	DSI_DNDATA1
J7	DSI_VDD12	K7	V _{SS}	L7	DSI_VREG0P4V	M7	V _{SS}
J8	DSI_VDD12	K8	DSI_VDD0P8	L8	V _{SS}	M8	CSI3_MSVDD18
J9	V _{SS}	K9	DSI_VDD0P8	L9	V _{SS}	M9	CSI3_MSVDD18
J10	V _{SS}	K10	V _{SS}	L10	V _{SS}	M10	V _{SS}
J11	V _{SS}	K11	V _{SS}	L11	PLDVDD08_PLLVDO_DSI	M11	V _{SS}
J12	V _{SS}	K12	V _{SS}	L12	PLVSS_PLLVDO_DSI	M12	V _{SS}
J13	V _{SS}	K13	V _{SS}	L13	PLVDD_PLLVDO_DSI	M13	V _{SS}
J14	V _{SS}	K14	V _{SS}	L14	V _{SS}	M14	V _{SS}
J15	V _{SS}	K15	V _{SS}	L15	PLDVDD08_PLLDDR0	M15	V _{SS}
J16	V _{SS}	K16	V _{SS}	L16	PLVSS_PLLDDR0	M16	V _{SS}
J17	V _{SS}	K17	V _{SS}	L17	PLVDD_PLLDDR0	M17	V _{SS}
J18	V _{SS}	K18	V _{SS}	L18	V _{SS}	M18	V _{SS}
J19	V _{SS}	K19	V _{SS}	L19	V _{SS}	M19	V _{SS}
J20	V _{SS}	K20	V _{SS}	L20	V _{SS}	M20	V _{SS}
J21	V _{SS}	K21	V _{SS}	L21	PLDVDD08_PLLDDR1	M21	V _{SS}
J22	V _{SS}	K22	V _{SS}	L22	PLVSS_PLLDDR1	M22	V _{SS}
J23	V _{SS}	K23	V _{SS}	L23	PLVDD_PLLDDR1	M23	V _{SS}
J24	V _{SS}	K24	V _{SS}	L24	V _{SS}	M24	V _{SS}
J25	V _{SS}	K25	V _{SS}	L25	PLDVDD08_PLLETH_GPU	M25	V _{SS}
J26	V _{SS}	K26	V _{SS}	L26	PLVSS_PLLETH_GPU	M26	V _{SS}
J27	V _{SS}	K27	V _{SS}	L27	PLVDD_PLLETH_GPU	M27	V _{SS}
J28	V _{SS}	K28	V _{SS}	L28	V _{SS}	M28	V _{SS}
J29	V _{SS}	K29	PCIE_VCC18AL01	L29	PCIE_VCC18ACMN	M29	PCIE_VCC18AL23
J30	V _{SS}	K30	PCIE_VCC18AL01	L30	PCIE_VCC18ACMN	M30	PCIE_VCC18AL23
J31	V _{SS}	K31	V _{SS}	L31	V _{SS}	M31	V _{SS}
J32	V _{SS}	K32	V _{SS}	L32	V _{SS}	M32	PCIE_REFCLKP0
J33	V _{SS}	K33	V _{SS}	L33	V _{SS}	M33	PCIE_REFCLKN0
J34	PCIE_RXDNL0	K34	V _{SS}	L34	PCIE_RXDNL1	M34	V _{SS}
J35	PCIE_RXDPL0	K35	V _{SS}	L35	PCIE_RXDPL1	M35	V _{SS}
J36	V _{SS}	K36	PCIE_TXDNL1	L36	V _{SS}	M36	PCIE_TXDNL2
J37	V _{SS}	K37	PCIE_TXDPL1	L37	V _{SS}	M37	PCIE_TXDPL2

Table 2.1-1 Ball Numbers and External Pin Names (4/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
N1	V _{SS}	P1	CSI3_DATA1P	R1	V _{SS}	T1	CSI3_DATA0P
N2	V _{SS}	P2	CSI3_DATA1N	R2	V _{SS}	T2	CSI3_DATA0N
N3	CSI3_DATA2P	P3	V _{SS}	R3	CSI3_CLKP	T3	V _{SS}
N4	CSI3_DATA2N	P4	V _{SS}	R4	CSI3_CLKN	T4	V _{SS}
N5	V _{SS}	P5	CSI3_DATA3P	R5	V _{SS}	T5	V _{SS}
N6	V _{SS}	P6	CSI3_DATA3N	R6	V _{SS}	T6	V _{SS}
N7	NC	P7	V _{SS}	R7	NC	T7	V _{SS}
N8	NC	P8	CSI3_MSVD0P8	R8	V _{SS}	T8	CSI2_MSVD0P8
N9	V _{SS}	P9	CSI3_MSVD0P8	R9	V _{SS}	T9	CSI2_MSVD0P8
N10	V _{SS}	P10	V _{SS}	R10	V _{SS}	T10	V _{SS}
N11	V _{SS}	P11	V _{SS}	R11	V _{SS}	T11	V _{SS}
N12	VDD08_DDR	P12	VDD08_OTHERS	R12	V _{SS}	T12	V _{SS}
N13	V _{SS}	P13	V _{SS}	R13	VDD08_OTHERS	T13	VDD08_OTHERS
N14	VDD08_DDR	P14	VDD08_OTHERS	R14	V _{SS}	T14	V _{SS}
N15	V _{SS}	P15	V _{SS}	R15	VDD08_OTHERS	T15	VDD08_OTHERS
N16	VDD08_DDR	P16	VDD08_OTHERS	R16	V _{SS}	T16	V _{SS}
N17	V _{SS}	P17	V _{SS}	R17	VDD08_OTHERS	T17	VDD08_OTHERS
N18	VDD08_DDR	P18	VDD08_OTHERS	R18	V _{SS}	T18	V _{SS}
N19	V _{SS}	P19	V _{SS}	R19	VDD08_OTHERS	T19	VDD08_OTHERS
N20	VDD08_DDR	P20	VDD08_OTHERS	R20	V _{SS}	T20	V _{SS}
N21	V _{SS}	P21	V _{SS}	R21	VDD08_OTHERS	T21	VDD08_OTHERS
N22	VDD08_DDR	P22	VDD08_OTHERS	R22	V _{SS}	T22	V _{SS}
N23	V _{SS}	P23	V _{SS}	R23	VDD08_OTHERS	T23	VDD08_OTHERS
N24	VDD08_DDR	P24	VDD08_OTHERS	R24	V _{SS}	T24	V _{SS}
N25	V _{SS}	P25	V _{SS}	R25	VDD08_OTHERS	T25	VDD08_OTHERS
N26	VDD08_DDR	P26	VDD08_OTHERS	R26	V _{SS}	T26	V _{SS}
N27	V _{SS}	P27	V _{SS}	R27	PCIE_VCC08AL23	T27	PCIE_VCC08AL23
N28	PCIE_VCC08AL01	P28	PCIE_VCC08AL01	R28	V _{SS}	T28	V _{SS}
N29	VDD1833_ET0	P29	VDD1833_PRE18_ET0	R29	VDD1833_ET1	T29	VDD1833_PRE18_ET1
N30	VDD1833_ET0	P30	VDD1833_PRE18_ET0	R30	VDD1833_ET1	T30	VDD1833_PRE18_ET1
N31	V _{SS}	P31	V _{SS}	R31	V _{SS}	T31	V _{SS}
N32	V _{SS}	P32	PCIE_REFCLKN1	R32	V _{SS}	T32	ET0_TXCTL_TXEN
N33	V _{SS}	P33	PCIE_REFCLKP1	R33	V _{SS}	T33	ET0_RXCTL_RXDV
N34	PCIE_RXDNL2	P34	V _{SS}	R34	PCIE_RXDNL3	T34	V _{SS}
N35	PCIE_RXDPL2	P35	V _{SS}	R35	PCIE_RXDPL3	T35	V _{SS}
N36	V _{SS}	P36	PCIE_TXDNL3	R36	V _{SS}	T36	ET0_MDC
N37	V _{SS}	P37	PCIE_TXDPL3	R37	V _{SS}	T37	ET0_TXC_TXCLK

Table 2.1-1 Ball Numbers and External Pin Names (5/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
U1	V _{SS}	V1	CSI2_DATA2P	W1	V _{SS}	Y1	CSI2_DATA0P
U2	V _{SS}	V2	CSI2_DATA2N	W2	V _{SS}	Y2	CSI2_DATA0N
U3	CSI2_DATA3P	V3	V _{SS}	W3	CSI2_CLKP	Y3	V _{SS}
U4	CSI2_DATA3N	V4	V _{SS}	W4	CSI2_CLKN	Y4	V _{SS}
U5	V _{SS}	V5	CSI2_DATA1P	W5	V _{SS}	Y5	NC
U6	V _{SS}	V6	CSI2_DATA1N	W6	V _{SS}	Y6	NC
U7	NC	V7	V _{SS}	W7	NC	Y7	V _{SS}
U8	NC	V8	CSI2_MSVD0P8	W8	V _{SS}	Y8	CSI1_MSVD0P8
U9	V _{SS}	V9	CSI2_MSVD0P8	W9	V _{SS}	Y9	CSI1_MSVD0P8
U10	V _{SS}	V10	V _{SS}	W10	V _{SS}	Y10	V _{SS}
U11	V _{SS}	V11	V _{SS}	W11	V _{SS}	Y11	PLVDD_PLLCM33
U12	VDD08_OTHERS	V12	VDD08_OTHERS	W12	V _{SS}	Y12	V _{SS}
U13	V _{SS}	V13	V _{SS}	W13	VDD08_OTHERS	Y13	VDD08_OTHERS
U14	VDD08_OTHERS	V14	VDD08_OTHERS	W14	V _{SS}	Y14	V _{SS}
U15	V _{SS}	V15	V _{SS}	W15	VDD08_OTHERS	Y15	VDD08_OTHERS
U16	VDD08_OTHERS	V16	VDD08_OTHERS	W16	V _{SS}	Y16	V _{SS}
U17	V _{SS}	V17	V _{SS}	W17	VDD08_OTHERS	Y17	VDD08_OTHERS
U18	VDD08_OTHERS	V18	VDD08_OTHERS	W18	V _{SS}	Y18	V _{SS}
U19	V _{SS}	V19	V _{SS}	W19	VDD08_OTHERS	Y19	VDD08_OTHERS
U20	VDD08_OTHERS	V20	VDD08_OTHERS	W20	V _{SS}	Y20	V _{SS}
U21	V _{SS}	V21	V _{SS}	W21	VDD08_OTHERS	Y21	VDD08_OTHERS
U22	VDD08_OTHERS	V22	VDD08_OTHERS	W22	V _{SS}	Y22	V _{SS}
U23	V _{SS}	V23	V _{SS}	W23	VDD08_OTHERS	Y23	VDD08_OTHERS
U24	VDD08_OTHERS	V24	VDD08_OTHERS	W24	V _{SS}	Y24	V _{SS}
U25	V _{SS}	V25	V _{SS}	W25	VDD08_OTHERS	Y25	VDD08_OTHERS
U26	VDD08_OTHERS	V26	VDD08_OTHERS	W26	V _{SS}	Y26	V _{SS}
U27	V _{SS}	V27	V _{SS}	W27	PLVDD_PLLCA55	Y27	PLVSS_PLLCA55
U28	USB20_USDVDD	V28	USB20_USDVDD	W28	V _{SS}	Y28	PLDVDD09_PLLCA55
U29	VDD33_PRE18_OTHERS	V29	VDD33_OTHERS	W29	USB20_USVDD33	Y29	USB20_USVDD18
U30	VDD33_PRE18_OTHERS	V30	VDD33_OTHERS	W30	USB20_USVDD33	Y30	USB20_USVDD18
U31	V _{SS}	V31	ET0_COL	W31	V _{SS}	Y31	V _{SS}
U32	ET0_MDIO	V32	ET0_TXER	W32	ET1_RXCTL_RXDV	Y32	V _{SS}
U33	V _{SS}	V33	ET0_RXD0	W33	ET0_PHYINTR	Y33	ET1_RXER
U34	ET0_RXER	V34	ET0_TXD2	W34	ET0_RXD3	Y34	ET1_MDIO
U35	ET0_TXD0	V35	ET0_TXD3	W35	ET0_RXD2	Y35	ET1_MDC
U36	V _{SS}	V36	ET0_TXD1	W36	ET0_RXD1	Y36	ET1_TXCTL_TXEN
U37	ET0_RXC_RXCLK	V37	ET0_CRS	W37	V _{SS}	Y37	ET1_TXC_TXCLK

Table 2.1-1 Ball Numbers and External Pin Names (6/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
AA1	V _{SS}	AB1	CSI1_DATA3P	AC1	V _{SS}	AD1	CSI1_DATA2P
AA2	V _{SS}	AB2	CSI1_DATA3N	AC2	V _{SS}	AD2	CSI1_DATA2N
AA3	NC	AB3	V _{SS}	AC3	CSI1_CLKP	AD3	V _{SS}
AA4	NC	AB4	V _{SS}	AC4	CSI1_CLKN	AD4	V _{SS}
AA5	V _{SS}	AB5	CSI1_DATA1P	AC5	V _{SS}	AD5	CSI1_DATA0P
AA6	V _{SS}	AB6	CSI1_DATA1N	AC6	V _{SS}	AD6	CSI1_DATA0N
AA7	NC	AB7	V _{SS}	AC7	NC	AD7	V _{SS}
AA8	NC	AB8	CSI1_MSVD0P8	AC8	V _{SS}	AD8	CSI0_MSVD0P8
AA9	V _{SS}	AB9	CSI1_MSVD0P8	AC9	V _{SS}	AD9	CSI0_MSVD0P8
AA10	V _{SS}	AB10	V _{SS}	AC10	V _{SS}	AD10	V _{SS}
AA11	PLVSS_PLLCM33	AB11	PLDVDD08_PLLCM33	AC11	V _{SS}	AD11	VDD08_OTHERS
AA12	VDD08_OTHERS	AB12	VDD08_OTHERS	AC12	VDD08_OTHERS	AD12	VDD08_OTHERS
AA13	V _{SS}	AB13	V _{SS}	AC13	VDD08_OTHERS	AD13	VDD08_OTHERS
AA14	VDD08_OTHERS	AB14	VDD08_OTHERS	AC14	V _{SS}	AD14	V _{SS}
AA15	V _{SS}	AB15	V _{SS}	AC15	VDD08_OTHERS	AD15	VDD08_OTHERS
AA16	VDD08_OTHERS	AB16	VDD08_OTHERS	AC16	V _{SS}	AD16	V _{SS}
AA17	V _{SS}	AB17	V _{SS}	AC17	VDD08_OTHERS	AD17	VDD08_OTHERS
AA18	VDD08_OTHERS	AB18	VDD08_OTHERS	AC18	V _{SS}	AD18	V _{SS}
AA19	V _{SS}	AB19	V _{SS}	AC19	VDD08_OTHERS	AD19	VDD08_OTHERS
AA20	VDD08_OTHERS	AB20	VDD08_OTHERS	AC20	V _{SS}	AD20	V _{SS}
AA21	V _{SS}	AB21	V _{SS}	AC21	VDD09_CA55	AD21	VDD09_CA55
AA22	VDD08_OTHERS	AB22	VDD08_OTHERS	AC22	V _{SS}	AD22	V _{SS}
AA23	V _{SS}	AB23	V _{SS}	AC23	VDD09_CA55	AD23	VDD09_CA55
AA24	VDD09_CA55	AB24	VDD09_CA55	AC24	V _{SS}	AD24	V _{SS}
AA25	V _{SS}	AB25	V _{SS}	AC25	VDD09_CA55	AD25	VDD09_CA55
AA26	VDD09_CA55	AB26	VDD09_CA55	AC26	V _{SS}	AD26	V _{SS}
AA27	V _{SS}	AB27	V _{SS}	AC27	USB30_USDVDD	AD27	USB30_USDVDD
AA28	USB30_USVPTX	AB28	USB30_USVPTX	AC28	V _{SS}	AD28	V _{SS}
AA29	USB21_USVDD33	AB29	USB21_USVDD18	AC29	USB21_USDVDD	AD29	USB30_USVPH
AA30	USB21_USVDD33	AB30	USB21_USVDD18	AC30	USB21_USDVDD	AD30	USB30_USVPH
AA31	V _{SS}	AB31	V _{SS}	AC31	V _{SS}	AD31	USB20_TXRTUNE
AA32	V _{SS}	AB32	ET1_TXD0	AC32	ET1_TXD3	AD32	ET1_RXD3
AA33	V _{SS}	AB33	ET1_RXD2	AC33	USB20_OTGEXICEN	AD33	V _{SS}
AA34	ET1_TXD2	AB34	ET1_RXD1	AC34	V _{SS}	AD34	USB21_DM
AA35	ET1_TXD1	AB35	ET1_RXD0	AC35	V _{SS}	AD35	USB21_DP
AA36	V _{SS}	AB36	ET1_CRS	AC36	ET1_COL	AD36	V _{SS}
AA37	ET1_RXC_RXCLK	AB37	ET1_TXER	AC37	ET1_PHYINTR	AD37	V _{SS}

Table 2.1-1 Ball Numbers and External Pin Names (7/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
AE1	V _{SS}	AF1	CSI0_DATA2P	AG1	V _{SS}	AH1	CSI0_DATA1P
AE2	V _{SS}	AF2	CSI0_DATA2N	AG2	V _{SS}	AH2	CSI0_DATA1N
AE3	CSI0_DATA3P	AF3	V _{SS}	AG3	CSI0_CLKP	AH3	V _{SS}
AE4	CSI0_DATA3N	AF4	V _{SS}	AG4	CSI0_CLKN	AH4	V _{SS}
AE5	V _{SS}	AF5	NC	AG5	V _{SS}	AH5	VDD08_OTHERS
AE6	V _{SS}	AF6	CSI0_MSVDD0P8	AG6	V _{SS}	AH6	VDD08_OTHERS
AE7	NC	AF7	CSI0_MSVDD0P8	AG7	VDD08_OTHERS	AH7	VDD08_OTHERS
AE8	NC	AF8	V _{SS}	AG8	VDD08_OTHERS	AH8	VDD08_OTHERS
AE9	V _{SS}	AF9	VDD08_OTHERS	AG9	VDD08_OTHERS	AH9	VDD08_OTHERS
AE10	VDD08_OTHERS	AF10	VDD08_OTHERS	AG10	VDD08_OTHERS	AH10	V _{SS}
AE11	VDD08_OTHERS	AF11	VDD08_OTHERS	AG11	V _{SS}	AH11	V _{SS}
AE12	VDD08_OTHERS	AF12	V _{SS}	AG12	VDD1833_JTAG	AH12	VDD1833_PRE18_JTAG
AE13	V _{SS}	AF13	V _{SS}	AG13	V _{SS}	AH13	V _{SS}
AE14	VDD08_OTHERS	AF14	VDD08_OTHERS	AG14	V _{SS}	AH14	VDD1833_PRE18_OTHERS_A
AE15	V _{SS}	AF15	V _{SS}	AG15	VDD08_AWO	AH15	VDD1833_PRE18_OTHERS_A
AE16	VDD08_OTHERS	AF16	VDD08_OTHERS	AG16	VDD08_AWO	AH16	V _{SS}
AE17	V _{SS}	AF17	V _{SS}	AG17	VDD08_AWO	AH17	V _{SS}
AE18	VDD08_OTHERS	AF18	VDD08_OTHERS	AG18	VDD08_AWO	AH18	V _{SS}
AE19	V _{SS}	AF19	V _{SS}	AG19	VDD08_AWO	AH19	V _{SS}
AE20	VDD08_OTHERS	AF20	VDD08_OTHERS	AG20	TS1DVDD08A	AH20	V _{SS}
AE21	V _{SS}	AF21	V _{SS}	AG21	TS1AVDD18	AH21	V _{SS}
AE22	VDD09_CA55	AF22	VDD09_CA55	AG22	V _{SS}	AH22	PLDVDD08_PLLCLN_DTY_DRP
AE23	V _{SS}	AF23	VDD09_CA55	AG23	VDD09_CA55	AH23	PLVSS_PLLCLN_DTY_DRP
AE24	VDD09_CA55	AF24	VDD09_CA55	AG24	V _{SS}	AH24	PLVDD_PLLCLN_DTY_DRP
AE25	V _{SS}	AF25	VDD09_CA55	AG25	VDD09_CA55	AH25	V _{SS}
AE26	VDD09_CA55	AF26	VDD09_CA55	AG26	V _{SS}	AH26	V _{SS}
AE27	V _{SS}	AF27	V _{SS}	AG27	USB31_USDVDD	AH27	USB31_USDVDD
AE28	USB31_USVPTX	AF28	USB31_USVPTX	AG28	V _{SS}	AH28	V _{SS}
AE29	USB30_USVDD33	AF29	USB30_USVDD18	AG29	USB31_USVPH	AH29	USB31_USVDD33
AE30	USB30_USVDD33	AF30	USB30_USVDD18	AG30	USB31_USVPH	AH30	USB31_USVDD33
AE31	V _{SS}	AF31	V _{SS}	AG31	V _{SS}	AH31	V _{SS}
AE32	PCIE1_RSTOUTB	AF32	PCIE0_RSTOUTB	AG32	USB20_OTGID	AH32	USB21_TXRTUNE
AE33	USB20_VUBUSIN	AF33	V _{SS}	AG33	USB30_TXRTUNE	AH33	V _{SS}
AE34	V _{SS}	AF34	USB30_DM	AG34	V _{SS}	AH34	USB31_TX0M
AE35	V _{SS}	AF35	USB30_DP	AG35	V _{SS}	AH35	USB31_TX0P
AE36	USB20_DM	AF36	V _{SS}	AG36	USB30_TX0M	AH36	V _{SS}
AE37	USB20_DP	AF37	V _{SS}	AG37	USB30_TX0P	AH37	V _{SS}

Table 2.1-1 Ball Numbers and External Pin Names (8/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
AJ1	V _{SS}	AK1	CSI0_DATA0P	AL1	V _{SS}	AM1	NC
AJ2	V _{SS}	AK2	CSI0_DATA0N	AL2	V _{SS}	AM2	NC
AJ3	NC	AK3	V _{SS}	AL3	TS0AVDD18	AM3	OTPVDD18
AJ4	NC	AK4	V _{SS}	AL4	TS0DVDD08A	AM4	VDD08_AWO
AJ5	VDD08_OTHERS	AK5	V _{SS}	AL5	V _{SS}	AM5	NC
AJ6	VDD08_OTHERS	AK6	VDD18_PWC	AL6	PWEN2	AM6	PWEN0
AJ7	VDD08_OTHERS	AK7	VDD18_PWC	AL7	PWEN1	AM7	QRESNSEL
AJ8	VDD08_OTHERS	AK8	ADAVDD18	AL8	ADAVSS18	AM8	NC
AJ9	V _{SS}	AK9	ADAVDD18	AL9	ADAVSS18	AM9	P15
AJ10	V _{SS}	AK10	V _{SS}	AL10	VDD1833_PRE18_AWO	AM10	VDD1833_PRE18_AWO
AJ11	VDD1833_AWO	AK11	VDD1833_AWO	AL11	V _{SS}	AM11	V _{SS}
AJ12	V _{SS}	AK12	V _{SS}	AL12	VDD1833_PRE18_XSPI	AM12	VDD1833_PRE18_XSPI
AJ13	VDD1833_XSPI	AK13	VDD1833_XSPI	AL13	V _{SS}	AM13	V _{SS}
AJ14	VDD1833_OTHERS_A	AK14	VDD1833_OTHERS_A	AL14	VDD1218_I3C	AM14	VDD1218_I3C
AJ15	VDD1833_PRE18_OTHERS_B	AK15	VDD1833_PRE18_OTHERS_B	AL15	V _{SS}	AM15	V _{SS}
AJ16	VDD1833_OTHERS_B	AK16	VDD1833_OTHERS_B	AL16	V _{SS}	AM16	XSPIO_INT0N
AJ17	VDD1833_PRE18_OTHERS_C	AK17	VDD1833_PRE18_OTHERS_C	AL17	V _{SS}	AM17	P45
AJ18	VDD1833_OTHERS_C	AK18	VDD1833_OTHERS_C	AL18	V _{SS}	AM18	P33
AJ19	VDD1833_PRE18_OTHERS_D	AK19	VDD1833_PRE18_OTHERS_D	AL19	V _{SS}	AM19	P40
AJ20	VDD1833_OTHERS_D	AK20	VDD1833_OTHERS_D	AL20	V _{SS}	AM20	P54
AJ21	VDD1833_PRE18_SD2	AK21	VDD1833_PRE18_SD2	AL21	V _{SS}	AM21	P65
AJ22	VDD18_AWO	AK22	VDD18_AWO	AL22	V _{SS}	AM22	P62
AJ23	V _{SS}	AK23	V _{SS}	AL23	V _{SS}	AM23	P74
AJ24	VDD1833_SD2	AK24	VDD1833_SD2	AL24	V _{SS}	AM24	P77
AJ25	VDD1833_PRE18_SD1	AK25	VDD1833_PRE18_SD1	AL25	V _{SS}	AM25	P72
AJ26	VDD1833_SD1	AK26	VDD1833_SD1	AL26	V _{SS}	AM26	V _{SS}
AJ27	VDD1833_PRE18_SD0	AK27	VDD1833_PRE18_SD0	AL27	V _{SS}	AM27	PA5
AJ28	VDD1833_SD0	AK28	VDD1833_SD0	AL28	V _{SS}	AM28	PA0
AJ29	USB31_USVDD18	AK29	V _{SS}	AL29	V _{SS}	AM29	P94
AJ30	USB31_USVDD18	AK30	V _{SS}	AL30	V _{SS}	AM30	P93
AJ31	V _{SS}	AK31	V _{SS}	AL31	V _{SS}	AM31	P91
AJ32	NC	AK32	NC	AL32	V _{SS}	AM32	V _{SS}
AJ33	USB3_USRESREF	AK33	V _{SS}	AL33	USB31_TXRTUNE	AM33	V _{SS}
AJ34	V _{SS}	AK34	USB31_RX0M	AL34	V _{SS}	AM34	V _{SS}
AJ35	V _{SS}	AK35	USB31_RX0P	AL35	V _{SS}	AM35	V _{SS}
AJ36	USB30_RX0M	AK36	V _{SS}	AL36	USB31_DM	AM36	V _{SS}
AJ37	USB30_RX0P	AK37	V _{SS}	AL37	USB31_DP	AM37	V _{SS}

Table 2.1-1 Ball Numbers and External Pin Names (9/10)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
AN1	V _{SS}	AP1	ANI004	AR1	ANI002	AT1	ANI006
AN2	V _{SS}	AP2	ANI001	AR2	ADAVSS18	AT2	ANI007
AN3	V _{SS}	AP3	ADAVSS18	AR3	ANI003	AT3	ANI000
AN4	V _{SS}	AP4	BOOTPLLCA0	AR4	BOOTSELCPU	AT4	V _{SS}
AN5	V _{SS}	AP5	MD_BOOT2	AR5	MD_BOOT1	AT5	BOOTPLLCA1
AN6	V _{SS}	AP6	WDTUDFCA	AR6	WDTUDFCM	AT6	SCIF_TXD
AN7	MD_BOOT3	AP7	NMI	AR7	BSCANP	AT7	V _{SS}
AN8	QBYPASS	AP8	MD_BOOT4	AR8	NC	AT8	P01
AN9	P04	AP9	P02	AR9	P03	AT9	P13
AN10	V _{SS}	AP10	P06	AR10	P07	AT10	V _{SS}
AN11	P20	AP11	P10	AR11	P12	AT11	P14
AN12	V _{SS}	AP12	TDI	AR12	TMS_SWDIO	AT12	TDO
AN13	V _{SS}	AP13	XSPI0_CKP	AR13	XSPI0_CKN	AT13	V _{SS}
AN14	XSPI0_RST00N	AP14	XSPI0_IO0	AR14	XSPI0_IO1	AT14	XSPI0_CS0N
AN15	XSPI0_RESET0N	AP15	XSPI0_IO6	AR15	XSPI0_IO5	AT15	V _{SS}
AN16	XSPI0_ECS0N	AP16	XSPI0_IO7	AR16	XSPI0_IO4	AT16	XSPI0_IO3
AN17	P46	AP17	P43	AR17	P32	AT17	P35
AN18	P36	AP18	P41	AR18	P31	AT18	P42
AN19	V _{SS}	AP19	P34	AR19	P37	AT19	V _{SS}
AN20	P56	AP20	P60	AR20	P61	AT20	P50
AN21	P51	AP21	P66	AR21	P57	AT21	P67
AN22	V _{SS}	AP22	P52	AR22	P55	AT22	V _{SS}
AN23	P80	AP23	P81	AR23	P87	AT23	P82
AN24	P83	AP24	P85	AR24	P84	AT24	V _{SS}
AN25	V _{SS}	AP25	P73	AR25	P75	AT25	P76
AN26	V _{SS}	AP26	V _{SS}	AR26	P70	AT26	V _{SS}
AN27	VSS	AP27	PA2	AR27	V _{SS}	AT27	V _{SS}
AN28	PA4	AP28	PA1	AR28	PA6	AT28	V _{SS}
AN29	P97	AP29	PA7	AR29	PA3	AT29	V _{SS}
AN30	P92	AP30	P90	AR30	P95	AT30	V _{SS}
AN31	P96	AP31	V _{SS}	AR31	PB2	AT31	V _{SS}
AN32	V _{SS}	AP32	PB4	AR32	PB0	AT32	V _{SS}
AN33	PB1	AP33	PB3	AR33	PB5	AT33	V _{SS}
AN34	V _{SS}	AP34	SD1DAT0	AR34	SD1DAT3	AT34	SD1DAT2
AN35	SD0DAT1	AP35	SD0DAT0	AR35	SD1CMD	AT35	V _{SS}
AN36	SD0CMD	AP36	SD0DAT5	AR36	SD0DAT6	AT36	SD0RSTN
AN37	SD0CLK	AP37	SD0DAT2	AR37	SD0DAT3	AT37	SD0DAT4

Table 2.1-1 Ball Numbers and External Pin Names (10/10)

Ball Num.	External Pin Name
AU1	ADAVSS18
AU2	ANI005
AU3	ADAVSS18
AU4	MD_BOOT0
AU5	MD_CLKS
AU6	SCIF_RXD
AU7	QRESN
AU8	P00
AU9	P11
AU10	P05
AU11	P21
AU12	TRSTN
AU13	TCK_SWCLK
AU14	XSPI0_DS
AU15	XSPI0_IO2
AU16	V _{ss}
AU17	P30
AU18	P44
AU19	P47
AU20	P53
AU21	P64
AU22	P63
AU23	P86
AU24	P71
AU25	V _{ss}
AU26	EMXTAL
AU27	EMEXTAL
AU28	AUDIO_XTAL
AU29	AUDIO_EXTAL
AU30	RTXIN
AU31	RTXOUT
AU32	QEXTAL
AU33	QXTAL
AU34	SD1DAT1
AU35	SD1CLK
AU36	SD0DAT7
AU37	V _{ss}

2.2 External Pins

2.2.1 List of External Pins

Table 2.2-1 List of External Pins (1/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
QXTAL	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open for CLKIN into QEXTAL or always in use for the crystal resonator
QEXTAL	Input	1.8	VDD18_AWO	—	1.8-V OSC	Always in use
EMXTAL	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open
EMEXTAL	Input	1.8	VDD18_AWO	—	1.8-V OSC	V _{ss}
RTXOUT	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open
RTXIN	Input	1.8	VDD18_AWO	—	1.8-V OSC	V _{ss}
AUDIO_XTAL	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open
AUDIO_EXTAL	Input	1.8	VDD18_AWO	—	1.8-V OSC	V _{ss}
BOOTSELCPU	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
BOOTPLCA1	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Always in use
BOOTPLCA0	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_BOOT4	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_BOOT3	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_BOOT2	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Always in use
MD_BOOT1	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Always in use
MD_BOOT0	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_CLKS	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Open
QRESN	Input	1.8	VDD18_PWC	—	1.8-V I/O	Always in use
NMI	Input	1.8	VDD18_PWC	—	1.8-V I/O	Pull down
QBYPASS	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Open
BSCANP	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Open
QRESNSEL	Input	1.8	VDD18_PWC	—	1.8-V I/O	Pull down
PWEN0	Output	1.8	VDD18_PWC	Low	1.8-V I/O	Open
PWEN1	Output	1.8	VDD18_PWC	Low	1.8-V I/O	Open
PWEN2	Output	1.8	VDD18_PWC	Low	1.8-V I/O	Open
TMS_SWDIO	Input / Output	1.8/3.3	VDD1833_JTAG	Hi-Z	3.3/1.8-V switching I/O (type 1)	Pull up
TCK_SWCLK	Input	1.8/3.3	VDD1833_JTAG	—	3.3/1.8-V switching I/O (type 1)	Pull up or pull down
TDO	Output	1.8/3.3	VDD1833_JTAG	Hi-Z*3	3.3/1.8-V switching I/O (type 1)	Open
TDI	Input	1.8/3.3	VDD1833_JTAG	—	3.3/1.8-V switching I/O (type 1)	Pull up or pull down
TRSTN	Input	1.8/3.3	VDD1833_JTAG	—	3.3/1.8-V switching I/O (type 1)	Pull down
VDD1833_JTAG	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_JTAG	—	1.8	—	—	—	Open*6
WDTUDFCM	Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
WDTUDFCA	Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
SCIF_RXD	Input	1.8/3.3	VDD1833_AWO	—	3.3/1.8-V switching I/O (type 1)	Pull up

Table 2.2-1 List of External Pins (2/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
SCIF_TXD	Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
ANI000 to 007	Input	1.8	ADAVDD18	—	ADC I/O	Open
ADAVDD18	—	1.8	—	—	—	Always in use
ADAVSS18	—	—	—	—	—	Always in use
XSPI0_CKP	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
XSPI0_CKN	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
XSPI0_CS0N	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
XSPI0_DS	Input / Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
XSPI0_IO0 to 7	Input / Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
XSPI0_RESET0N	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
XSPI0_RST00N	Input	1.8/3.3	VDD1833_XSPI	—	3.3/1.8-V switching I/O (type 1)	Pull down
XSPI0_INT0N	Input	1.8/3.3	VDD1833_XSPI	—	3.3/1.8-V switching I/O (type 1)	Pull down
XSPI0_ECS0N	Input	1.8/3.3	VDD1833_XSPI	—	3.3/1.8-V switching I/O (type 1)	Pull down
VDD1833_XSPI	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_XSPI	—	1.8	—	—	—	Open*6
SD0CLK	Output	1.8/3.3	VDD1833_SD0	Low	3.3/1.8-V switching I/O (type 3)	Open
SD0CMD	Input / Output	1.8/3.3	VDD1833_SD0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
SD0DAT0 to 7	Input / Output	1.8/3.3	VDD1833_SD0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
SD0RSTN	Output	1.8/3.3	VDD1833_SD0	Low	3.3/1.8-V switching I/O (type 3)	Open
VDD1833_SD0	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_SD0	—	1.8	—	—	—	Open*6
SD1CLK	Output	1.8/3.3	VDD1833_SD1	Low	3.3/1.8-V switching I/O (type 3)	Open
SD1CMD	Input / Output	1.8/3.3	VDD1833_SD1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
SD1DAT0 to 3	Input / Output	1.8/3.3	VDD1833_SD1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
VDD1833_SD1	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_SD1	—	1.8	—	—	—	Open*6
VDD1833_SD2	—	1.8/3.3	—	—	—	Open
VDD1833_PRE18_SD2	—	1.8	—	—	—	Open
USB20_DP	Input / Output	3.3	USB20_USVDD33	Low	USB2 PHY	Open
USB20_DM	Input / Output	3.3	USB20_USVDD33	Low	USB2 PHY	Open

Table 2.2-1 List of External Pins (3/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
USB20_OTGID	Input	1.8	USB20_USVDD18	Hi-Z	USB2 PHY	Open
USB20_VUBUSIN*11	Input	3.3*4	USB20_USVDD33	Hi-Z	USB2 PHY	Open
USB20_OTGEXICEN	Output	3.3	VDD33_OTHERS	High	3.3-V I/O	Open
USB20_TXRTUNE	—	—	—	—	USB2 PHY	Open
USB20_USVDD33	—	3.3	—	—	—	V _{SS}
USB20_USVDD18	—	1.8	—	—	—	V _{SS}
USB20_USDVDD*10	—	0.8	—	—	—	V _{SS}
USB21_DP	Input / Output	3.3	USB21_USVDD33	Low	USB2 PHY	Open
USB21_DM	Input / Output	3.3	USB21_USVDD33	Low	USB2 PHY	Open
USB21_TXRTUNE	—	—	—	—	USB2 PHY	Open
USB21_USVDD33	—	3.3	—	—	—	V _{SS}
USB21_USVDD18	—	1.8	—	—	—	V _{SS}
USB21_USDVDD*10	—	0.8	—	—	—	V _{SS}
USB30_DP	Input / Output	3.3	USB30_USVDD33	Low	USB2 PHY	Open
USB30_DM	Input / Output	3.3	USB30_USVDD33	Low	USB2 PHY	Open
USB30_RX0M	Input	0.8	USB30_USVPTX	—	USB3 PHY	Open
USB30_RX0P	Input	0.8	USB30_USVPTX	—	USB3 PHY	Open
USB30_TX0M	Output	0.8	USB30_USVPTX	Hi-Z	USB3 PHY	Open
USB30_TX0P	Output	0.8	USB30_USVPTX	Hi-Z	USB3 PHY	Open
USB3_USRESREF	—	—	—	—	USB3 PHY	Open
USB30_TXRTUNE	—	—	—	—	USB2 PHY	Open
USB30_USVPH	—	1.8	—	—	—	V _{SS} *12
USB30_USVPTX	—	0.8	—	—	—	V _{SS} *12
USB30_USVDD33	—	3.3	—	—	—	V _{SS} *12
USB30_USVDD18	—	1.8	—	—	—	V _{SS} *12
USB30_USDVDD*10	—	0.8	—	—	—	V _{SS} *12
USB31_DP	Input / Output	3.3	USB31_USVDD33	Low	USB2 PHY	Open
USB31_DM	Input / Output	3.3	USB31_USVDD33	Low	USB2 PHY	Open
USB31_RX0M	Input	0.8	USB31_USVPTX	—	USB3 PHY	Open
USB31_RX0P	Input	0.8	USB31_USVPTX	—	USB3 PHY	Open
USB31_TX0M	Output	0.8	USB31_USVPTX	Hi-Z	USB3 PHY	Open
USB31_TX0P	Output	0.8	USB31_USVPTX	Hi-Z	USB3 PHY	Open
USB31_TXRTUNE	—	—	—	—	USB2 PHY	Open
USB31_USVPH	—	1.8	—	—	—	V _{SS} *12
USB31_USVPTX	—	0.8	—	—	—	V _{SS} *12
USB31_USVDD33	—	3.3	—	—	—	V _{SS} *12
USB31_USVDD18	—	1.8	—	—	—	V _{SS} *12
USB31_USDVDD*10	—	0.8	—	—	—	V _{SS} *12
PCIE_TXDPL0	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_TXDNL0	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_TXDPL1	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_TXDNL1	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_TXDPL2	Output	1.8	PCIE_VCC18AL23	Hi-Z	PCIE PHY	Open*9
PCIE_TXDNL2	Output	1.8	PCIE_VCC18AL23	Hi-Z	PCIE PHY	Open*9
PCIE_TXDPL3	Output	1.8	PCIE_VCC18AL23	Hi-Z	PCIE PHY	Open*9
PCIE_TXDNL3	Output	1.8	PCIE_VCC18AL23	Hi-Z	PCIE PHY	Open*9
PCIE_RXDPL0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_RXDNL0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_RXDPL1	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_RXDNL1	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_RXDPL2	Input	1.8	PCIE_VCC18AL23	—	PCIE PHY	Open
PCIE_RXDNL2	Input	1.8	PCIE_VCC18AL23	—	PCIE PHY	Open

Table 2.2-1 List of External Pins (4/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
PCIE_RXDPL3	Input	1.8	PCIE_VCC18AL23	—	PCIE PHY	Open
PCIE_RXDNL3	Input	1.8	PCIE_VCC18AL23	—	PCIE PHY	Open
PCIE_REFCLKP0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_REFCLKN0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_REFCLKP1	Input	1.8	PCIE_VCC18AL23	—	PCIE PHY	Open
PCIE_REFCLKN1	Input	1.8	PCIE_VCC18AL23	—	PCIE PHY	Open
PCIE0_RSTOUTB	Output	3.3	VDD33_OTHERS	High	3.3-V I/O	Open
PCIE1_RSTOUTB	Output	3.3	VDD33_OTHERS	High	3.3-V I/O	Open
PCIE_VCC18ACMN	—	1.8	—	—	—	V _{SS} *13
PCIE_VCC18AL01	—	1.8	—	—	—	V _{SS} *13
PCIE_VCC18AL23	—	1.8	—	—	—	V _{SS} *13
PCIE_VCC08AL01	—	0.8	—	—	—	V _{SS} *13
PCIE_VCC08AL23	—	0.8	—	—	—	V _{SS} *13
ET0_MDIO	Input / Output	1.8/3.3	VDD1833_ET0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
ET0_MDC	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_RXCTL_RXDV	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_TXCTL_TXEN	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXER	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_RXER	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_RXC_RXCLK	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_TXC_TXCLK	Input / Output	1.8/3.3	VDD1833_ET0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
ET0_CRS	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_COL	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_TXD0	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXD1	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXD2	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXD3	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_RXD0	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_RXD1	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_RXD2	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down

Table 2.2-1 List of External Pins (5/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
ET0_RXD3	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_PHYINTR	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
VDD1833_ET0	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_ET0	—	1.8	—	—	—	Open*6
ET1_MDIO	Input / Output	1.8/3.3	VDD1833_ET1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
ET1_MDC	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_RXCTL_RXDV	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_TXCTL_TXEN	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_TXER	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_RXER	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXC_RXCLK	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_TXC_TXCLK	Input / Output	1.8/3.3	VDD1833_ET1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
ET1_CRS	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_COL	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_TXD0	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_TXD1	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_TXD2	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_TXD3	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_RXD0	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXD1	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXD2	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXD3	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_PHYINTR	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
VDD1833_ET1	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_ET1	—	1.8	—	—	—	Open*6

Table 2.2-1 List of External Pins (6/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
DSI_DPCLK	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNCLK	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA0	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA0	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA1	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA1	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA2	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA2	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA3	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA3	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_VREG0P4V	—	—	—	—	—	Open
DSI_VDD0P8	—	0.8	—	—	—	Always in use
DSI_VDD18	—	1.8	—	—	—	Open
DSI_VDD12	—	1.2	—	—	—	Open
CSI0_CLKP	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_CLKN	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA0P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA0N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA1P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA1N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA2P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA2N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA3P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA3N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_MSVDD18	—	1.8	—	—	—	Open
CSI0_MSVDD0P8	—	0.8	—	—	—	Always in use
CSI1_CLKP	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_CLKN	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA0P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA0N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA1P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA1N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA2P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA2N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA3P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA3N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_MSVDD18	—	1.8	—	—	—	Open
CSI1_MSVDD0P8	—	0.8	—	—	—	Always in use
CSI2_CLKP	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_CLKN	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA0P	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA0N	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA1P	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA1N	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA2P	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA2N	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA3P	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_DATA3N	Input	1.8*1	CSI2_MSVDD18	—	CSI PHY	Open
CSI2_MSVDD18	—	1.8	—	—	—	Open
CSI2_MSVDD0P8	—	0.8	—	—	—	Always in use
CSI3_CLKP	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_CLKN	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open

Table 2.2-1 List of External Pins (7/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
CSI3_DATA0P	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_DATA0N	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_DATA1P	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_DATA1N	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_DATA2P	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_DATA2N	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_DATA3P	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_DATA3N	Input	1.8*1	CSI3_MSVDD18	—	CSI PHY	Open
CSI3_MSVDD18	—	1.8	—	—	—	Open
CSI3_MSVDD0P8	—	0.8	—	—	—	Always in use
DDR0_DQA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA2	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA3	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA4	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA5	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA6	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA7	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAT0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAC0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA8	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA9	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA10	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA11	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA12	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA13	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA14	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA15	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAT1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAC1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB2	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB3	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB4	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB5	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB6	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB7	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_QSBO0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_QSBC0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB8	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB9	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB10	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB11	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB12	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB13	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB14	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB15	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open

Table 2.2-1 List of External Pins (8/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
DDR0_DQSBT1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSBC1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_CKEA0	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CKEA1	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CAA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKAT	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKAC	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA2	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA3	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA4	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA5	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKEB0	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CKEB1	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CAB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKBT	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKBC	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB2	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB3	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB4	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB5	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_RESETN	Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_DTEST	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_ATEST	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_ZN	—	—	—	—	DDR PHY	Open
DDR0_VDDQ	—	1.1	—	—	—	V _{SS}
DDR0_VDDQLP*6	—	0.6/1.1	—	—	—	V _{SS}
DDR0_VAA	—	1.8	—	—	—	V _{SS}
DDR1_DQA0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA2	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA3	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA4	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA5	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA6	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA7	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DMIA0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSAT0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSAC0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA8	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA9	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA10	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA11	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA12	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA13	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA14	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQA15	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open

Table 2.2-1 List of External Pins (9/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
DDR1_DMIA1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSAT1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSAC1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB2	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB3	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB4	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB5	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB6	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB7	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DMIB0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSBT0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSBC0	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB8	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB9	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB10	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB11	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB12	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB13	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB14	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQB15	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DMIB1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSBT1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_DQSBC1	Input / Output	0.6/1.1	DDR1_VDDQLP	Low	DDR PHY	Open
DDR1_CKEA0	Input / Output	1.1	DDR1_VDDQ	Low	DDR PHY	Open
DDR1_CKEA1	Input / Output	1.1	DDR1_VDDQ	Low	DDR PHY	Open
DDR1_CAA0	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAA1	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CKAT	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CKAC	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CSA0	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CSA1	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAA2	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAA3	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAA4	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAA5	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CKEB0	Input / Output	1.1	DDR1_VDDQ	Low	DDR PHY	Open
DDR1_CKEB1	Input / Output	1.1	DDR1_VDDQ	Low	DDR PHY	Open
DDR1_CAB0	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAB1	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CKBT	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CKBC	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CSB0	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CSB1	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAB2	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAB3	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAB4	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_CAB5	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_RESETN	Output	1.1	DDR1_VDDQ	Low	DDR PHY	Open
DDR1_DTEST	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open
DDR1_ATEST	Input / Output	0.6/1.1	DDR1_VDDQLP	Hi-Z	DDR PHY	Open

Table 2.2-1 List of External Pins (10/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
DDR1_ZN	—	—	—	—	DDR PHY	Open
DDR1_VDDQ	—	1.1	—	—	—	V _{SS}
DDR1_VDDQLP*8	—	0.6/1.1	—	—	—	V _{SS}
DDR1_VAA	—	1.8	—	—	—	V _{SS}
P00	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P01	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P02	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P03	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P04	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P05	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P06	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P07	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P10	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P11	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P12	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P13	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P14	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P15	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P20	Input / Output	1.2/1.8	VDD1218_I3C	Hi-Z	1.8/1.2-V switching I/O	Open
P21	Input / Output	1.2/1.8	VDD1218_I3C	Hi-Z	1.8/1.2-V switching I/O	Open
P30	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P31	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P32	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P33	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P34	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open

Table 2.2-1 List of External Pins (11/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
P35	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P36	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P37	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P40	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P41	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P42	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P43	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P44	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P45	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P46	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P47	Input / Output	1.8/3.3	VDD1833_OTHER S_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P50	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P51	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P52	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P53	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P54	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P55	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P56	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P57	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P60	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P61	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P62	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P63	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open

Table 2.2-1 List of External Pins (12/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
P64	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P65	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P66	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P67	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P70	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P71	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P72	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P73	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P74	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P75	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P76	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P77	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P80	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P81	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P82	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P83	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P84	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P85	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P86	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P87	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P90	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
P91	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
P92	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open

Table 2.2-1 List of External Pins (13/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
P93	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P94	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P95	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P96	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P97	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA0	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA1	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA2	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA3	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA4	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA5	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA6	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA7	Input / Output	1.8/3.3	VDD1833_OTHER S_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PB0	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB1	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB2	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB3	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB4	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB5	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
TS0AVDD18	—	1.8	—	—	—	Always in use
TS0DVDD08A	—	0.8	—	—	—	Always in use
TS1AVDD18	—	1.8	—	—	—	Always in use
TS1DVDD08A	—	0.8	—	—	—	Always in use
OTPVDD18	—	1.8	—	—	—	Always in use
PLVDD_PLLCM33	—	1.8	—	—	—	Always in use
PLVSS_PLLCM33	—	—	—	—	—	Always in use
PLVDD_PLLCLN_DTY_DRP	—	1.8	—	—	—	Always in use
PLVSS_PLLCLN_DTY_DRP	—	—	—	—	—	Always in use

Table 2.2-1 List of External Pins (14/14)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
PLVDD_PLLCA55	—	1.8	—	—	—	Always in use
PLVSS_PLLCA55	—	—	—	—	—	Always in use
PLVDD_PLLVDO_DSI	—	1.8	—	—	—	Always in use
PLVSS_PLLVDO_DSI	—	—	—	—	—	Always in use
PLVDD_PLDDR0	—	1.8	—	—	—	Always in use
PLVSS_PLDDR0	—	—	—	—	—	Always in use
PLVDD_PLDDR1	—	1.8	—	—	—	Always in use
PLVSS_PLDDR1	—	—	—	—	—	Always in use
PLVDD_PLLETH_GPU	—	1.8	—	—	—	Always in use
PLVSS_PLLETH_GPU	—	—	—	—	—	Always in use
PLDVDD08_PLLCM33	—	0.8	—	—	—	Always in use
PLDVDD08_PLLCLN_DTY_DRP	—	0.8	—	—	—	Always in use
PLDVDD09_PLLCA55	—	0.8/0.9*5	—	—	—	Always in use
PLDVDD08_PLLVDO_DSI	—	0.8	—	—	—	Always in use
PLDVDD08_PLDDR0	—	0.8	—	—	—	Always in use
PLDVDD08_PLDDR1	—	0.8	—	—	—	Always in use
PLDVDD08_PLLETH_GPU	—	0.8	—	—	—	Always in use
VDD09_CA55	—	0.8/0.9*5	—	—	—	Always in use
VDD08_AWO	—	0.8	—	—	—	Always in use
VDD08_DDR	—	0.8	—	—	—	Always in use
VDD18_AWO	—	1.8	—	—	—	Always in use
VDD1833_AWO	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_AWO	—	1.8	—	—	—	Open*6
VDD33_OTHERS	—	3.3	—	—	—	Open*6
VDD33_PRE18_OTHERS	—	1.8	—	—	—	Open*6
VDD08_OTHERS	—	0.8	—	—	—	Always in use
VDD1833_OTHERS_A	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_OTHERS_A	—	1.8	—	—	—	Open*6
VDD1833_OTHERS_B	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_OTHERS_B	—	1.8	—	—	—	Open*6
VDD1833_OTHERS_C	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_OTHERS_C	—	1.8	—	—	—	Open*6
VDD1833_OTHERS_D	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_OTHERS_D	—	1.8	—	—	—	Open*6
VDD1218_I3C	—	1.2/1.8	—	—	—	Open*6
VDD18_PWC	—	1.8	—	—	—	Always in use
Vss	—	—	—	—	—	Always in use

Note 1. This voltage is the IO buffer voltage. The amplitude is different between LP (low power) mode and HS (high speed) mode. For details, refer to the *MIPI Alliance Specification for D-PHY Version 1.2*.

Note 2. Pull-up or pull-down resistors are integrated in the IO buffers. For the resistance values, refer to the DC characteristics in **Section 3, Electrical Characteristics**.

Note 3. This pin is compliant with the JTAG specification.

Note 4. See **Figure 2.3-1** for how to connect the USBVBUS.

Note 5. VDD09_CA55 and PLDVDD09_PLLCA55 should be at the same voltage.

Note 6. When these power supplies are open, the corresponding signal pins should be open. When supplying power, follow the instructions in the table.

Note 7. The initial value indicates the status during a reset (QRESN = 0) and immediately after release from the reset state (QRESN = 1).

Note 8. When using these pins at 1.1 V, DDRx_VDDQLP should be connected to DDRx_VDDQ. (x = 0, 1)

Note 9. All unconnected lanes must be terminated during compliance test.

Note 10. Connect an external resistor (6.2 kΩ). For details, refer to the *RZ/V2H Group PCB Design Guidelines*.

- Note 11. A load switch or similar component should be added so that voltage is applied to the USB20_VUBUSIN pin after power is supplied for USB20.
- Note 12. Connect these pins to V_{SS} only when both USB30 and USB31 are unused. If either USB30 or USB31 is used, power must be supplied to these pins.
- Note 13. Connect these pins to V_{SS} only when all PCIE lanes (Lane 0 to Lane 3) are unused. If any lane is used, power must be supplied to these pins.

2.2.2 List of Multiplexed Functional Pins

For details on pin functions, refer to the *RZ/V2H Group User's Manual: Hardware*.

Table 2.2-2 List of Multiplexed Functional Pins (1/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P00	GPIO/TINT_ GP00	—	PDMDAT00	—	—	—	—	—	—
		—	GTETRGA	GTETRGE	—	—	IRQ0	—	—
P01	GPIO/TINT_ GP01	—	PDMCLK00	—	—	—	—	—	—
		—	GTETRGA	GTETRGE	—	—	IRQ1	—	—
P02	GPIO/TINT_ GP02	—	PDMDAT01	—	—	—	—	—	—
		—	GTETRGC	GTETRGG	—	—	IRQ2	DACK0	DREQ0
P03	GPIO/TINT_ GP03	—	PDMCLK01	—	—	—	—	—	—
		—	GTETRGA	GTETRGE	—	—	IRQ3	TEND0	DREQ0
P04	GPIO/TINT_ GP04	—	PDMDAT02	SSLA0	SSLB2	ADTRG	—	—	SSI3_SDAT A
		SPDIF1_OUT	TOC20	TIC20	GTETRGE	—	IRQ8	—	XSPI0_WP0 N
P05	GPIO/TINT_ GP05	—	PDMCLK02	SSLA1	SSLC2	ADTRG	TOC31	TIC31	SSI4_SCK
		SPDIF1_IN	TOC21	TIC21	GTETRGE	—	IRQ9	DACK0	XSPI0_ECS1 N
P06	GPIO/TINT_ GP06	—	SDA8	—	—	—	—	—	—
		—	—	—	—	—	IRQ12	—	—
P07	GPIO/TINT_ GP07	—	SCL8	—	—	—	—	—	—
		—	—	—	—	—	IRQ13	—	—
P10	GPIO/TINT_ GP10	—	PDMDAT10	—	—	—	—	—	AUDIO_CLK B
		—	TOC00	TIC00	GTETRGA	—	IRQ4	DACK0	XSPI0_CS1 N
P11	GPIO/TINT_ GP11	—	PDMCLK10	—	—	—	—	—	AUDIO_CLK C
		—	TOC01	TIC01	GTETRGA	—	IRQ5	—	XSPI0_RES ET1N
P12	GPIO/TINT_ GP12	—	PDMDAT11	—	—	—	—	—	SSI3_SCK
		SPDIF0_OUT	TOC10	TIC10	GTETRGC	—	IRQ6	—	XSPI0_RST O1N
P13	GPIO/TINT_ GP13	—	PDMCLK11	—	—	—	—	—	SSI3_WS
		SPDIF0_IN	TOC11	TIC11	GTETRGA	—	IRQ7	TEND0	XSPI0_INT1 N
P14	GPIO/TINT_ GP14	—	PDMDAT12	SSLA2	SSLB3	ADTRG	TOC20	TIC20	SSI4_WS
		SPDIF2_OUT	TOC30	TIC30	GTETRGG	—	IRQ10	TEND0	XSPI0_WP1 N

Table 2.2-2 List of Multiplexed Functional Pins (2/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P15	GPIO/TINT_ GP15	—	PDMCLK12	SSLA3	SSLC3	ADTRG	—	—	SSI4_SDAT A
		SPDIF2_IN	TOC31	TIC31	GTETRGH	—	IRQ11	TEND0	DREQ0
P20	GPIO/TINT_ GP20	—	SDA30	—	—	SDA2	—	—	—
		—	GTETRGC	GTETRGG	—	—	IRQ14	DACK3	DREQ1
P21	GPIO/TINT_ GP21	—	SCL30	—	—	SCL2	—	—	—
		—	GTETRGD	GTETRGH	—	—	IRQ15	TEND3	DREQ2
P30	GPIO/TINT_ GP30	—	SDA0	—	—	—	—	—	—
		—	GTIOC4A	GTIOC4AN	GTIOC12A	GTIOC12AN	IRQ0	DACK1	—
P31	GPIO/TINT_ GP31	—	SCL0	—	—	—	—	—	—
		—	GTIOC4B	GTIOC4BN	GTIOC12B	GTIOC12BN	IRQ1	TEND1	—
P32	GPIO/TINT_ GP32	—	SDA1	—	—	—	—	—	—
		—	GTIOC5A	GTIOC5AN	GTIOC13A	GTIOC13AN	IRQ2	DACK2	—
P33	GPIO/TINT_ GP33	—	SCL1	—	—	—	—	—	—
		—	GTIOC5B	GTIOC5BN	GTIOC13B	GTIOC13BN	IRQ3	TEND2	—
P34	GPIO/TINT_ GP34	—	SDA2	TXD3_MISO 3_SDA3	—	—	SSLA0	SSLB0	—
		—	GTIOC6A	GTIOC6AN	GTIOC14A	GTIOC14AN	IRQ4	DACK3	—
P35	GPIO/TINT_ GP35	—	SCL2	RXD3_MISO 3_SCL3	—	—	SSLA1	SSLC0	—
		—	GTIOC6B	GTIOC6BN	GTIOC14B	GTIOC14BN	IRQ5	TEND3	—
P36	GPIO/TINT_ GP36	—	SDA3	SCK3	DE3	CTS3N	SSLA2	SSLB1	—
		—	GTIOC7A	GTIOC7AN	GTIOC15A	GTIOC15AN	IRQ6	DACK4	—
P37	GPIO/TINT_ GP37	—	SCL3	SS3_CTS3N _RTS3N	DE3	—	SSLA3	SSLC1	—
		—	GTIOC7B	GTIOC7BN	GTIOC15B	GTIOC15BN	IRQ7	TEND4	—
P40	GPIO/TINT_ GP40	—	SDA4	TXD4_MISO 4_SDA4	—	—	CTXDP4	—	SSI0_SCK
		—	GTIOC0A	GTIOC0AN	—	—	IRQ8	DACK1	DREQ3
P41	GPIO/TINT_ GP41	—	SCL4	RXD4_MISO 4_SCL4	—	—	CRXDP4	—	SSI0_WS
		—	GTIOC0B	GTIOC0BN	—	—	IRQ9	TEND1	DREQ4

Table 2.2-2 List of Multiplexed Functional Pins (3/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P42	GPIO/TINT_ GP42	—	SDA5	SCK4	DE4	CTS4N	CTX4	—	SSI0_SDAT A
		—	GTIOC1A	GTIOC1AN	—	—	IRQ10	USB21_VBU SEN	USB31_VBU SEN
P43	GPIO/TINT_ GP43	—	SCL5	SS4_CTS4N _RTS4N	DE4	—	CRX4	—	SSI9_SDAT A
		—	GTIOC1B	GTIOC1BN	—	—	IRQ11	USB21_OVR CURN	USB31_OVR CURN
P44	GPIO/TINT_ GP44	—	SDA6	TXD5_MOSI 5_SDA5	—	—	CTXDP5	—	SSI1_SCK
		—	GTIOC2A	GTIOC2AN	—	—	IRQ12	DACK4	DREQ1
P45	GPIO/TINT_ GP45	—	SCL6	RXD5_MISO 5_SCL5	—	—	CRXDP5	—	SSI1_WS
		—	GTIOC2B	GTIOC2BN	—	—	IRQ13	TEND4	DREQ2
P46	GPIO/TINT_ GP46	—	SDA7	SCK5	DE5	CTS5N	CTX5	—	SSI1_SDAT A
		—	GTIOC3A	GTIOC3AN	—	—	IRQ14	DACK2	DREQ3
P47	GPIO/TINT_ GP47	—	SCL7	SS5_CTS5N _RTS5N	DE5	—	CRX5	—	SSI2_SDAT A
		—	GTIOC3B	GTIOC3BN	—	—	IRQ15	TEND2	DREQ4
P50	GPIO/TINT_ GP50	—	TXD0_MOSI 0_SDA0	—	—	—	—	—	—
		—	—	—	GTIOC8A	GTIOC8AN	IRQ0	—	—
P51	GPIO/TINT_ GP51	—	RXD0_MISO 0_SCL0	—	—	—	—	—	—
		—	—	—	GTIOC8B	GTIOC8BN	IRQ1	—	—
P52	GPIO/TINT_ GP52	—	TXD1_MOSI 1_SDA1	SCK0	DE0	CTS0N	—	—	—
		—	—	—	GTIOC10A	GTIOC10AN	IRQ4	—	—
P53	GPIO/TINT_ GP53	—	RXD1_MISO 1_SCL1	SS0_CTS0N _RTS0N	DE0	—	—	—	—
		—	—	—	GTIOC10B	GTIOC10BN	IRQ5	—	—
P54	GPIO/TINT_ GP54	—	TXD2_MOSI 2_SDA2	—	—	—	—	—	—
		—	—	—	GTIOC12A	GTIOC12AN	IRQ8	—	—

Table 2.2-2 List of Multiplexed Functional Pins (4/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P55	GPIO/TINT_ GP55	—	RXD2_MISO 2_SCL2	—	—	—	—	—	—
		—	—	—	GTIOC12B	GTIOC12BN	IRQ9	—	—
P56	GPIO/TINT_ GP56	—	TXD3_MOSI 3_SDA3	SCK2	DE2	CTS2N	—	—	—
		—	GTETRGA	GTETRGE	GTIOC14A	GTIOC14AN	IRQ12	—	—
P57	GPIO/TINT_ GP57	—	RXD3_MISO 3_SCL3	SS2_CTS2N _RTS2N	DE2	—	—	—	—
		—	GTETRGA	GTETRGE	GTIOC14B	GTIOC14BN	IRQ13	—	—
P60	GPIO/TINT_ GP60	—	SCK0	DE0	CTS0N	SDA4	—	TXD2_MOSI 2_SDA2	AUDIO_CLK B
		SPDIF0_OUT	GTETRGA	GTETRGE	GTIOC9A	GTIOC9AN	IRQ2	USB30_VBUS SEN	USB20_VBUS SEN
P61	GPIO/TINT_ GP61	—	SS0_CTS0N _RTS0N	DE0	—	SCL4	—	RXD2_MISO 2_SCL2	AUDIO_CLK OUT
		SPDIF0_IN	GTETRGA	GTETRGE	GTIOC9B	GTIOC9BN	IRQ3	USB30_OVR CURN	USB20_OVR CURN
P62	GPIO/TINT_ GP62	—	SCK1	DE1	CTS1N	SDA5	—	TXD3_MOSI 3_SDA3	AUDIO_CLK C
		SPDIF1_OUT	GTETRGA	GTETRGE	GTIOC11A	GTIOC11AN	IRQ6	USB31_VBUS SEN	USB21_VBUS SEN
P63	GPIO/TINT_ GP63	—	SS1_CTS1N _RTS1N	DE1	—	SCL5	—	RXD3_MISO 3_SCL3	AUDIO_CLK OUT
		SPDIF1_IN	GTETRGA	GTETRGE	GTIOC11B	GTIOC11BN	IRQ7	USB31_OVR CURN	USB21_OVR CURN
P64	GPIO/TINT_ GP64	—	SCK2	DE2	CTS2N	SDA6	—	TXD6_MOSI 6_SDA6	AUDIO_CLK B
		SPDIF2_OUT	GTETRGA	GTETRGE	GTIOC13A	GTIOC13AN	IRQ10	USB20_VBUS SEN	USB30_VBUS SEN
P65	GPIO/TINT_ GP65	—	SS2_CTS2N _RTS2N	DE2	—	SCL6	—	RXD6_MISO 6_SCL6	AUDIO_CLK C
		SPDIF2_IN	GTETRGA	GTETRGE	GTIOC13B	GTIOC13BN	IRQ11	USB20_OVR CURN	USB30_OVR CURN
P66	GPIO/TINT_ GP66	—	SCK3	DE3	CTS3N	SDA7	—	TXD7_MOSI 7_SDA7	SSI6_SCK
		—	GTETRGA	GTETRGE	GTIOC15A	GTIOC15AN	IRQ14	USB21_VBUS SEN	USB31_VBUS SEN

Table 2.2-2 List of Multiplexed Functional Pins (5/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P67	GPIO/TINT_ GP67	—	SS3_CTS3N _RTS3N	DE3	—	SCL7	—	RXD7_MISO 7_SCL7	SSI6_WS
		—	GTETRGD	GTETRGH	GTIOC15B	GTIOC15BN	IRQ15	USB21_OVR CURN	USB31_OVR CURN
P70	GPIO/TINT_ GP70	—	TXD4_MOSI 4_SDA4	—	—	—	CTXDP0	—	SSI6_SDAT A
		AUDIO_CLK B	GTIOC0A	GTIOC0AN	—	—	IRQ0	DACK1	—
P71	GPIO/TINT_ GP71	—	RXD4_MISO 4_SCL4	—	—	—	CRXDP0	—	SSI5_SCK
		AUDIO_CLK C	GTIOC0B	GTIOC0BN	—	—	IRQ1	TEND1	—
P72	GPIO/TINT_ GP72	—	TXD5_MOSI 5_SDA5	—	—	—	CTXDP1	—	SSI5_SDAT A
		SPDIF1_OU T	GTIOC2A	GTIOC2AN	—	—	IRQ4	DACK3	—
P73	GPIO/TINT_ GP73	—	RXD5_MISO 5_SCL5	—	—	—	CRXDP1	—	SSI7_SCK
		SPDIF1_IN	GTIOC2B	GTIOC2BN	—	—	IRQ5	TEND3	—
P74	GPIO/TINT_ GP74	—	TXD6_MOSI 6_SDA6	—	—	—	CTXDP2	—	SSI3_SCK
		—	GTIOC4A	GTIOC4AN	—	—	IRQ8	DACK3	DREQ1
P75	GPIO/TINT_ GP75	—	RXD6_MISO 6_SCL6	—	—	—	CRXDP2	—	SSI3_WS
		—	GTIOC4B	GTIOC4BN	—	—	IRQ9	TEND3	DREQ2
P76	GPIO/TINT_ GP76	—	TXD7_MOSI 7_SDA7	—	—	—	CTXDP3	—	SSI5_SCK
		SSI6_SCK	GTIOC6A	GTIOC6AN	—	—	IRQ12	DACK1	DREQ3
P77	GPIO/TINT_ GP77	—	RXD7_MISO 7_SCL7	—	—	—	CRXDP3	—	SSI5_WS
		SSI6_WS	GTIOC6B	GTIOC6BN	—	—	IRQ13	TEND1	DREQ4
P80	GPIO/TINT_ GP80	—	SCK4	DE4	CTS4N	—	CTX0	TXD8_MOSI 8_SDA8	SSI5_WS
		SPDIF0_OU T	GTIOC1A	GTIOC1AN	—	—	IRQ2	DACK2	—

Table 2.2-2 List of Multiplexed Functional Pins (6/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P81	GPIO/TINT_ GP81	—	SS4_CTS4N _RTS4N	DE4	—	—	CRX0	RXD8_MISO 8_SCL8	SSI8_SDAT A
		SPDIF0_IN	GTIOC1B	GTIOC1BN	—	—	IRQ3	TEND2	—
P82	GPIO/TINT_ GP82	—	SCK5	DE5	CTS5N	—	CTX1	TXD9_MOSI 9_SDA9	SSI7_WS
		SPDIF2_OUT	GTIOC3A	GTIOC3AN	—	—	IRQ6	DACK4	—
P83	GPIO/TINT_ GP83	—	SS5_CTS5N _RTS5N	DE5	—	—	CRX1	RXD9_MISO 9_SCL9	SSI7_SDAT A
		SPDIF2_IN	GTIOC3B	GTIOC3BN	—	—	IRQ7	TEND4	—
P84	GPIO/TINT_ GP84	—	SCK6	DE6	CTS6N	—	CTX2	TXD4_MOSI 4_SDA4	SSI3_SDAT A
		—	GTIOC5A	GTIOC5AN	—	—	IRQ10	USB30_VBU SEN	USB20_VBU SEN
P85	GPIO/TINT_ GP85	—	SS6_CTS6N _RTS6N	DE6	—	—	CRX2	RXD4_MISO 4_SCL4	SSI4_SDAT A
		—	GTIOC5B	GTIOC5BN	—	—	IRQ11	USB30_OVR CURN	USB20_OVR CURN
P86	GPIO/TINT_ GP86	—	SCK7	DE7	CTS7N	—	CTX3	TXD5_MOSI 5_SDA5	SSI5_SDAT A
		—	GTIOC7A	GTIOC7AN	—	—	IRQ14	USB31_VBU SEN	USB21_VBU SEN
P87	GPIO/TINT_ GP87	—	SS7_CTS7N _RTS7N	DE7	—	—	CRX3	RXD5_MISO 5_SCL5	SSI6_SDAT A
		—	GTIOC7B	GTIOC7BN	—	—	IRQ15	USB31_OVR CURN	USB21_OVR CURN
P90	GPIO/TINT_ GP90	—	MOSIA	TXD6_MOSI 6_SDA6	—	—	—	—	—
		—	—	—	—	—	IRQ0	—	—
P91	GPIO/TINT_ GP91	—	MISOA	RXD6_MISO 6_SCL6	—	—	—	—	—
		—	—	—	—	—	IRQ1	—	—
P92	GPIO/TINT_ GP92	—	RSPCKA	SCK6	DE6	CTS6N	—	TXD0_MOSI 0_SDA0	—
		—	—	—	—	—	IRQ2	—	—
P93	GPIO/TINT_ GP93	—	SSLA0	SS6_CTS6N _RTS6N	DE6	—	—	RXD0_MISO 0_SCL0	AUDIO_CLK B
		—	—	—	—	—	IRQ3	SD1WP	SD0WP

Table 2.2-2 List of Multiplexed Functional Pins (7/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P94	GPIO/TINT_ GP94	—	SSLA1	TXD7_MOSI 7_SDA7	—	—	—	—	AUDIO_CLK C
		SPDIF0_OUT	GTIOC8A	GTIOC8AN	GTIOC4A	GTIOC4AN	IRQ4	SD1CD	SD0CD
P95	GPIO/TINT_ GP95	—	SSLA2	RXD7_MISO 7_SCL7	—	—	—	—	SSI0_SCK
		SPDIF0_IN	GTIOC8B	GTIOC8BN	GTIOC4B	GTIOC4BN	IRQ5	USB20_VBU SEN	USB30_VBU SEN
P96	GPIO/TINT_ GP96	—	SSLA3	SCK7	DE7	CTS7N	—	TXD1_MOSI 1_SDA1	SSI0_WS
		AUDIO_CLK OUT	GTIOC9A	GTIOC9AN	GTIOC5A	GTIOC5AN	IRQ6	USB20_OVR CURN	USB30_OVR CURN
P97	GPIO/TINT_ GP97	—	ADTRG	SS7_CTS7N _RTS7N	DE7	—	—	RXD1_MISO 1_SCL1	SSI0_SDAT A
		AUDIO_CLK OUT	GTIOC9B	GTIOC9BN	GTIOC5B	GTIOC5BN	IRQ7	—	—
PA0	GPIO/TINT_ GPA0	—	SD0IOVS	—	—	—	—	—	—
		—	—	—	—	—	IRQ8	SD1WP	SD2WP
PA1	GPIO/TINT_ GPA1	—	SD0PWEN	—	—	—	—	—	—
		—	—	—	—	—	IRQ9	SD1CD	SD2CD
PA2	GPIO/TINT_ GPA2	—	SD1IOVS	—	—	—	—	—	—
		—	—	—	—	—	IRQ10	—	SD2WP
PA3	GPIO/TINT_ GPA3	—	SD1PWEN	—	—	—	—	—	—
		—	—	—	—	—	IRQ11	—	SD2CD
PA4	GPIO/TINT_ GPA4	—	SD2IOVS	SS8_CTS8N _RTS8N	DE8	SSLB0	SSLC3	—	AUDIO_CLK OUT
		SPDIF1_OUT	GTIOC10A	GTIOC10AN	GTIOC6A	GTIOC6AN	IRQ12	DACK1	SD0WP
PA5	GPIO/TINT_ GPA5	—	SD2PWEN	CTS8N	DE8	SSLB1	SSLC2	—	SSI9_WS
		SPDIF1_IN	GTIOC10B	GTIOC10BN	GTIOC6B	GTIOC6BN	IRQ13	TEND1	SD0CD
PA6	GPIO/TINT_ GPA6	—	SD2WP	CTS9N	DE9	SSLB2	SSLC1	—	SSI9_SDAT A
		SPDIF2_OUT	GTIOC11A	GTIOC11AN	GTIOC7A	GTIOC7AN	IRQ14	DACK3	SD1WP
PA7	GPIO/TINT_ GPA7	—	SD2CD	SS9_CTS9N _RTS9N	DE9	SSLB3	SSLC0	—	SSI9_SCK
		SPDIF2_IN	GTIOC11B	GTIOC11BN	GTIOC7B	GTIOC7BN	IRQ15	TEND3	SD1CD
PB0	GPIO/TINT_ GPB0	—	SD2CLK	SCK8	DE8	RSPCKB	—	—	SSI1_SCK
		—	—	—	—	—	IRQ0	USB30_VBU SEN	USB31_VBU SEN

Table 2.2-2 List of Multiplexed Functional Pins (8/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
PB1	GPIO/TINT_ GPB1	—	SD2DAT0	TXD8_MOSI 8_SDA8	—	MOSIB	—	—	SSI1_WS
		—	—	—	—	—	IRQ1	USB30_OVR CURN	USB31_OVR CURN
PB2	GPIO/TINT_ GPB2	—	SD2DAT1	RXD8_MISO 8_SCL8	—	MISOB	—	—	SSI1_SDAT A
		—	—	—	—	—	IRQ2	TEND4	DREQ2
PB3	GPIO/TINT_ GPB3	—	SD2DAT2	RXD9_MISO 9_SCL9	—	—	MISOC	—	SSI2_SCK
		—	—	—	—	—	IRQ3	DACK4	DREQ1
PB4	GPIO/TINT_ GPB4	—	SD2DAT3	TXD9_MOSI 9_SDA9	—	—	MOSIC	—	SSI2_WS
		—	—	—	—	—	IRQ4	DACK2	DREQ3
PB5	GPIO/TINT_ GPB5	—	SD2CMD	SCK9	DE9	—	RSPCKC	—	SSI2_SDAT A
		—	—	—	—	—	IRQ5	TEND2	DREQ4

Note: —: Reserved functions

2.3 Pin Functions of Functional Blocks

Table 2.3-1 List of Pin Functions (1/8)

Classification	Pin Name	I/O	Function
Clock	QXTAL	Out	24-MHz main clocks. These pins are to connect a 24-MHz crystal oscillator. When an external clock signal is used, the QXTAL pin should be open.
	QEXTAL	In	
	EMXTAL	Out	Reserved pins.
	EMEXTAL	In	The EMXTAL pin should be open. The EMEXTAL pin should be connected to V _{ss} .
	RTXOUT	Out	32.768-kHz real-time clocks. These pins are to connect a 32.768-kHz crystal oscillator. When an external clock signal is used, the RTXOUT pin should be open.
	RTXIN	In	
	AUDIO_XTAL	Out	4- to 48-MHz audio clocks. These pins are to connect a crystal oscillator. When an external clock signal is used, the clock frequency is allowed 50-MHz max. and the Audio_XTAL pin should be open.
	AUDIO_EXTAL	In	
	AUDIO_CLKB	In	Max. 50-MHz audio clock B
	AUDIO_CLKC	In	Max. 50-MHz audio clock C
	AUDIO_CLKOUT	Out	Max. 25-MHz audio clock out
Boot mode control	BOOTSELCPU	In	Select the cold boot CPU. Low: CM33, High: CA55
	BOOTPLLCA1	In	Input the CA55 frequency at the CA55 cold boot. BOOTPLLCA[1:0] = [Low:Low]: 1.1 GHz BOOTPLLCA[1:0] = [Low:High]: 1.5 GHz* ¹ BOOTPLLCA[1:0] = [High:Low]: 1.6 GHz* ¹ BOOTPLLCA[1:0] = [High:High]: 1.7 GHz* ¹ <i>Note 1.</i> Enabled when VDD09_CA55 is at 0.9 V.
	BOOTPLLCA0	In	
	MD_BOOT4	In	
	MD_BOOT3	In	
	MD_BOOT2	In	Select the boot device IO voltage Low: 3.3 V, High: 1.8 V <i>Note:</i> Enabled in boot mode 1 and boot mode 2 only
	MD_BOOT1	In	Input the boot mode select signal. MD_BOOT[1:0] = [Low:Low]: eSD* ¹ (boot mode 0) MD_BOOT[1:0] = [Low:High]: eMMC* ¹ (boot mode 1) MD_BOOT[1:0] = [High:Low]: xSPI (boot mode 2) MD_BOOT[1:0] = [High:High]: SCIF download (boot mode 3) <i>Note 1.</i> Enable CA55 cold boot only
	MD_BOOT0	In	
	MD_CLKS	In	
			Select SSCG OFF or ON Low: OFF, High: ON
System controller	QRESN	In	Input the reset signal. The reset state is entered when this signal goes low.
	QBYPASS	In	Select Main CLK oscillation mode Low: Crystal, High: External clock
	BSCANP	In	Select boundary scan mode Low: Not selected, High: Selected
Interrupt	NMI	In	Input interrupt trigger signal to all CPUs
	IRQ0 to 15	In	Input the external interrupt request signals
	TINT0 to 31	In	Input the external interrupt request signals

Table 2.3-1 List of Pin Functions (2/8)

Classification	Pin Name	I/O	Function
Power controller	QRESNSEL	In	Select the internal reset signal to be generated Low: Generated by the PWC High: Generated by the QRESN
	PWEN0	Out	Power enable for 1.8-V power supply to OTP and ADC (active high)*2
	PWEN1	Out	Power enable for 1.8-V power supply to MIPI DSI and MIPI CSI-2 (active high)*2
	PWEN2	Out	Power enable for 1.2-V power supply to MIPI DSI (active high)*2
Debugger interface	TMS_SWDIO	I/O	Test mode select pin. Functions as the SWDIO pin in serial wire debug (SWD) mode.
	TCK_SWCLK	In	Test clock pin. Functions as the SWCLK pin in serial wire debug (SWD) mode.
	TDO	Out	Test data output pin.
	TDI	In	Test data input pin.
	TRSTN	In	Test reset pin.
Direct memory access controller (DMAC)	DREQ0 to 4	In	Input DMAC request signal from the external device
	DACK0 to 4	Out	Output the acknowledge signal which indicates acceptance of DMAC request to the external device
	TEND0 to 4	Out	Output DMAC end signal
Watchdog timer (WDT)	WDTUDFCM	Out	Output the CM33_WDT underflow error signal with active low. This pin sets Nch open drain mode. (Register setting is possible.)
	WDTUDFCA	Out	Output the CA55_WDT underflow error signal with active low. This pin sets Nch open drain mode. (Register setting is possible.)
SCIF download interface	SCIF_RXD	In	UART receive pin for SCIF
	SCIF_TXD	Out	UART transfer pin for SCIF
12-bit A/D converter interface	ANI000 to 007	In	Input the ADC signals
	ADTRG	In	Input the ADC trigger signal
Expanded serial peripheral interface (xSPI)	XSPI0_CKP	Out	Clock output pins. CKP and CKN waves have opposite phase.
	XSPI0_CKN	Out	
	XSPI0_DS	I/O	Read data strobe / Write data mask
	XSPI0_IO0 to 7	I/O	Input/output data 0 to data 7
	XSPI0_CS0N	Out	Output the chip select signal for the channel 0. Low: Selected, High: Not selected
	XSPI0_RESET0N	Out	Output the reset status signal for the channel 0. Low: reset status
	XSPI0_RSTO0N	In	Input the reset status signal from the channel 0
	XSPI0_INT0N	In	Input the interrupt signal from the channel 0
	XSPI0_ECS0N	In	Input the error correction status from the channel 0
	XSPI0_WP0N	Out	Output the write-protection signal for the channel 0
	XSPI0_CS1N	Out	Output the chip select signal for the channel 1 Low: Selected, High: Not selected
	XSPI0_RESET1N	Out	Output the reset status signal for the channel 1 Low: reset status
	XSPI0_RSTO1N	In	Input the reset status signal from the channel 1
	XSPI0_INT1N	In	Input the interrupt signal from the channel 1
	XSPI0_ECS1N	In	Input the error correction status from the channel 1
	XSPI0_WP1N	Out	Output the write-protection signal for the channel 1

Table 2.3-1 List of Pin Functions (3/8)

Classification	Pin Name	I/O	Function
DDR memory interface channel 0, 1	DDRn_DQA0 to 15, DDRn_DQB0 to 15	I/O	DRAM data bits
	DDRn_DMIA0 to 1, DDRn_DMIB0 to 1	I/O	DRAM data mask inversion
	DDRn_DQSAT0 to 1, DDRn_DQSBT0 to 1	I/O	DRAM data strobe (positive)
	DDRn_DQSAC0 to 1, DDRn_DQSBC0 to 1	I/O	DRAM data strobe (negative)
	DDRn_CKEA0 to 1, DDRn_CKEB0 to 1	I/O	DRAM clock enable
	DDRn_CAA0 to 5, DDRn_CAB0 to 5	I/O	DRAM address bits and command bits
	DDRn_CSA0 to 1, DDRn_CSB0 to 1	I/O	DRAM chip select
	DDRn_CKAT, DDRn_CKBT	I/O	DRAM clock (positive)
	DDRn_CKAC, DDRn_CKBC	I/O	DRAM clock (negative)
	DDRn_RESETN	Out	Output DRAM reset signal
	DDRn_DTEST	I/O	Digital observation pin
	DDRn_ATEST	I/O	Voltage reference for receivers and analog test point for debug
	DDRn_ZN	—	Connect calibration external reference resistor (120Ω ± 1%)
SD/eMMC interface	SD0CLK	Out	Output the clock signal to external SD/eMMC device
	SD0CMD	I/O	Input/output the command code from/to external SD/eMMC device
	SD0DAT0 to 7	I/O	Input/output data 0 to data 7
	SD0RSTN	Out	Output the reset signal to external eMMC device
	SD0WP	In	Input the write-protection signal from external SD device
	SD0CD	In	Input the card-detect signal from external SD slot
	SD0PWEN	Out	Output the power-enable signal to power supply IC for SD device Low: Disabled, High: Enabled
	SD0IOVS	Out	Output the IO voltage level signal to SD device Low: 3.3 V, High: 1.8 V
SD interface	SD1CLK, SD2CLK	Out	Output the clock signals to external SD device
	SD1CMD, SD2CMD	Out	Input/output the command code from/to external SD device
	SD1DAT0 to 3, SD2DAT0 to 3	I/O	Input/output data 0 to data 3
	SD1WP, SD2WP	In	Input the write-protection signals from external SD device
	SD1CD, SD2CD	In	Input the card-detect signals from external SD slot
	SD1PWEN, SD2PWEN	Out	Output the power-enable signals to the power supply IC for SD device Low: Disabled, High: Enabled
	SD1IOVS, SD2IOVS	Out	Output the IO voltage level signals to SD device Low: 3.3 V, High: 1.8 V

Table 2.3-1 List of Pin Functions (4/8)

Classification	Pin Name	I/O	Function
USB2.0 channel 0	USB20_DP	I/O	USB2.0 D+ signal
	USB20_DM	I/O	USB2.0 D- signal
	USB20_OTGID	In	Input OTG ID (pulled up by the internal resistor) Low: Host, High: Peripheral
	USB20_VUBUSIN	In	Input USB VBUS detect signal*1
	USB20_OTGEXICEN	Out	OTG power supply IC control pin
	USB20_VBUSEN	Out	VBUS control signal (active high)
	USB20_OVRCURN	In	Overcurrent detection (active low)
	USB20_TXRTUNE	In	USB transmitter tune pin. This analog signal connects to V _{SS} via an external resistor (200Ω ±1%) that adjusts the USB PHY's high-speed source impedance.
USB2.0 channel 1	USB21_DP	I/O	USB2.0 D+ signal
	USB21_DM	I/O	USB2.0 D- signal
	USB21_VBUSEN	Out	VBUS control signal (active high)
	USB21_OVRCURN	In	Overcurrent detection (active low)
	USB21_TXRTUNE	In	USB transmitter tune pin. This analog signal connects to V _{SS} via an external resistor (200Ω ±1%) that adjusts the USB PHY's high-speed source impedance.
USB3.2 channel 0, 1	USB30_DP, USB31_DP	I/O	USB2.0 D+ signals
	USB30_DM, USB31_DM	I/O	USB2.0 D- signals
	USB30_RX0M, USB31_RX0M	In	USB3.2 super-speed plus differential receive pair (negative)
	USB30_RX0P, USB31_RX0P	In	USB3.2 super-speed plus differential receive pair (positive)
	USB30_TX0M, USB31_TX0M	Out	USB3.2 super-speed plus differential transfer pair (negative)
	USB30_TX0P, USB31_TX0P	Out	USB3.2 super-speed plus differential transfer pair (positive)
	USB30_VBUSEN, USB31_VBUSEN	Out	VBUS control signals (active high)
	USB30_OVRCURN, USB31_OVRCURN	In	Overcurrent detection (active low)
	USB3_USRESREF	—	USB3 reference resistor with 200Ω (1%, 100 ppm/°C) to V _{SS}
	USB30_TXRTUNE, USB31_TXRTUNE	—	USB transmitter tune pin. This analog signal connects to V _{SS} via an external resistor (200Ω ±1%) that adjusts the USB PHY's high-speed source impedance.

Table 2.3-1 List of Pin Functions (5/8)

Classification	Pin Name	I/O	Function
PCIe Gen3	PCIE_TXDPL0	Out	PCIe TX data (positive) of Lane 0 (4-lane × 1) or PCIe TX data (positive) of Lane 0 (2-lane × 2)
	PCIE_TXDNL0	Out	PCIe TX data (negative) of Lane 0 (4-lane × 1) or PCIe TX data (negative) of Lane 0 (2-lane × 2)
	PCIE_TXDPL1	Out	PCIe TX data (positive) of Lane 1 (4-lane × 1) or PCIe TX data (positive) of Lane 1 (2-lane × 2)
	PCIE_TXDNL1	Out	PCIe TX data (negative) of Lane 1 (4-lane × 1) or PCIe TX data (negative) of Lane 1 (2-lane × 2)
	PCIE_TXDPL2	Out	PCIe TX data (positive) of Lane 2 (4-lane × 1) or PCIe TX data (positive) of Lane 0 (2-lane × 2)
	PCIE_TXDNL2	Out	PCIe TX data (negative) of Lane 2 (4-lane × 1) or PCIe TX data (negative) of Lane 0 (2-lane × 2)
	PCIE_TXDPL3	Out	PCIe TX data (positive) of Lane 3 (4-lane × 1) or PCIe TX data (positive) of Lane 1 (2-lane × 2)
	PCIE_TXDNL3	Out	PCIe TX data (negative) of Lane 3 (4-lane × 1) or PCIe TX data (negative) of Lane 1 (2-lane × 2)
	PCIE_RXDPL0	In	PCIe RX data (positive) of Lane 0 (4-lane × 1) or PCIe RX data (positive) of Lane 0 (2-lane × 2)
	PCIE_RXDNL0	In	PCIe RX data (negative) of Lane 0 (4-lane × 1) or PCIe RX data (negative) of Lane 0 (2-lane × 2)
	PCIE_RXDPL1	In	PCIe RX data (positive) of Lane 1 (4-lane × 1) or PCIe RX data (positive) of Lane 1 (2-lane × 2)
	PCIE_RXDNL1	In	PCIe RX data (negative) of Lane 1 (4-lane × 1) or PCIe RX data (negative) of Lane 1 (2-lane × 2)
	PCIE_RXDPL2	In	PCIe RX data (positive) of Lane 2 (4-lane × 1) or PCIe RX data (positive) of Lane 0 (2-lane × 2)
	PCIE_RXDNL2	In	PCIe RX data (negative) of Lane 2 (4-lane × 1) or PCIe RX data (negative) of Lane 0 (2-lane × 2)
	PCIE_RXDPL3	In	PCIe RX data (positive) of Lane 3 (4-lane × 1) or PCIe RX data (positive) of Lane 1 (2-lane × 2)
	PCIE_RXDNL3	In	PCIe RX data (negative) of Lane 3 (4-lane × 1) or PCIe RX data (negative) of Lane 1 (2-lane × 2)
	PCIE_REFCLKP0	In	Differential reference clock (positive) for 4-lane × 1 mode and 2-lane × 2 mode
	PCIE_REFCLKN0	In	Differential reference clock (negative) for 4-lane × 1 mode and 2-lane × 2 mode
	PCIE_REFCLKP1	In	Differential reference clock (positive) for 2-lane × 2 mode only
	PCIE_REFCLKN1	In	Differential reference clock (negative) for 2-lane × 2 mode only
	PCIE0_RSTOUTB	Out	Output the reset signal for 4-lane × 1 mode and 2-lane × 2 mode
	PCIE1_RSTOUTB	Out	Output the reset signal for 2-lane × 2 mode only

Table 2.3-1 List of Pin Functions (6/8)

Classification	Pin Name	I/O	Function
Gb Ethernet channel 0, 1	ET0_MDIO, ET1_MDIO	I/O	Management data I/O
	ET0_MDC, ET1_MDC	Out	Management data clocks
	ET0_RXCTL_RXDV, ET1_RXCTL_RXDV	In	RX control/data valid
	ET0_TXCTL_TXEN, ET1_TXCTL_TXEN	Out	TX control/data enable
	ET0_TXER, ET1_TXER	Out	TX data error (MII mode)
	ET0_RXER, ET1_RXER	In	RX data error (MII mode)
	ET0_RXC_RXCLK, ET1_RXC_RXCLK	In	RX clocks
	ET0_TXC_TXCLK, ET1_TXC_TXCLK	I/O	TX clocks
	ET0_CRS, ET1_CRS	In	Carrier sense (MII mode)
	ET0_COL, ET1_COL	In	Collision detection (MII mode)
	ET0_TXD0, ET1_TXD0	Out	TX data 0
	ET0_TXD1, ET1_TXD1	Out	TX data 1
	ET0_TXD2, ET1_TXD2	Out	TX data 2
	ET0_TXD3, ET1_TXD3	Out	TX data 3
	ET0_RXD0, ET1_RXD0	In	RX data 0
	ET0_RXD1, ET1_RXD1	In	RX data 1
	ET0_RXD2, ET1_RXD2	In	RX data 2
	ET0_RXD3, ET1_RXD3	In	RX data 3
	ET0_PHYINTR, ET1_PHYINTR	In	PHY interrupt signals
MIPI DSI	DSI_DPCLK	Out	Output clocks (positive)
	DSI_DNCLK	Out	Output clocks (negative)
	DSI_DPDATA0 to 3	Out	TX data 0 to TX data 3 (positive)
	DSI_DNDATA0 to 3	Out	TX data 0 to TX data 3 (negative)
	DSI_VREG0P4V	—	Connect this pin to V _{SS} via a 2.2-nF capacitor
MIPI CSI-2 channel n (n = 0 to 3)	CSIn_CLKP	In	Input clocks (positive)
	CSIn_CLKN	In	Input clocks (negative)
	CSIn_DATA0P to CSIn_DATA3P	In	RX data 0 to RX data 3 (positive)
	CSIn_DATA0N to CSIn_DATA3N	In	RX data 0 to RX data 3 (negative)

Table 2.3-1 List of Pin Functions (7/8)

Classification	Pin Name	I/O	Function
CANFD interface channel n (n = 0 to 5)	CRXn	In	RX data 0 to RX data 5
	CTXn	Out	TX data 0 to TX data 5
	CRXDPn	Out	RX data 0 to RX data 5 phase signal
	CTXDPn	Out	TX data 0 to TX data 5 phase signal
Serial peripheral interface (RSPi) channel x (x = A, B, C)	RSPCKx	I/O	Synchronous clock signal
	MOSIx	I/O	Data of Main-Out / Sub-In
	MISOx	I/O	Data of Main-In / Sub-Out
	SSLx0 to 3	I/O*3	Chip select pins
Serial communication interface (RSCI) channel n (n = 0 to 9)	RXDn	In	Input the receive data (asynchronous mode / clock synchronous mode / simple SPI mode / smart card mode)
	TXDn	Out	Output the transmission data (asynchronous mode / clock synchronous mode / simple SPI mode / smart card mode)
	SCKn	I/O	Clock pins (clock synchronous mode / simple SPI mode / smart card mode)
	CTSnN	In	Input the start of transmission as the hardware flow control signals (asynchronous mode / clock synchronous mode)
	RTSnN	Out	Output the reception as the hardware flow control signals (asynchronous mode / clock synchronous mode)
	MOSIn	I/O	Data of Main-Out / Sub-In (simple SPI mode)
	MISOn	I/O	Data of Main-In / Sub-Out (simple SPI mode)
	SCLn	I/O	I2C clocks (simple I2C mode)
	SDAn	I/O	I2C data (simple I2C mode)
	SSn	In	Input chip selector (simple SPI mode)
	DEn	Out	Output driver enable signal for half duplex (asynchronous mode)
	SCLn	I/O	Clock pins with Nch open drain
	SDAn	I/O	Data pins with Nch open drain
I2C bus interface (RiIC) channel n (n = 0 to 8)	SCLn	I/O	Clock pins with Nch open drain
	SDAn	I/O	Data pins with Nch open drain
I3C bus interface (I3C)	SCL30	I/O	Clock pin
	SDA30	I/O	Data pin
General purpose timer (GPT)	GTIOC0A to 15A, GTIOC0B to 15B, GTIOC0AN to 15AN, GTIOC0BN to 15BN	I/O	Input capture for pulse width, output timer compare, and output PWM signals "nX" and "nXN" are anti-phase signals (X = A or B, n = 0 to 15).
	GTETRGA to GTETRGH	In	Input disable-output request signals for GPT outputs
Compare match timer (CMTW) channel n (n = 0 to 3)	TICn0, TICn1	In	Input capture signals
	TOCn0, TOCn1	Out	Output compare signals
Pulse density modulation interface (PDM) channel n (n = 0 to 5)	PDMDAT00 to 02, PDMDAT10 to 12	In	Input PDM data
	PDMCLK00 to 02, PDMCLK10 to 12	Out	Output PDM sampling clocks
Serial sound interface (SSIU) channel n	SSIn_SDATa	I/O	Serial sound data (TDM supported) (n = 0 to 9)**4
	SSIn_SCK	I/O	Serial clock (n = 0 to 7, 9)**4
	SSIn_WS	I/O	Word select (n = 0 to 7, 9)**4
SPDIF channel n (n = 0 to 2)	SPDIFn_OUT	Out	Output SPDIF data
	SPDIFn_IN	In	Input SPDIF data

Table 2.3-1 List of Pin Functions (8/8)

Classification	Pin Name	I/O	Function
I/O ports	P00 to P15	I/O	General purpose input/output pins with 3.3-V tolerance.
	P20 and P21	I/O	General purpose input/output pins included with I3C functions with 1.8-V tolerance.
	P30 to P47	I/O	General purpose input/output pins with 3.3-V tolerance.
	P50 to P57	I/O	General purpose input/output pins with 3.3-V tolerance.
	P60 to P67	I/O	General purpose input/output pins with 3.3-V tolerance. Selectable to use ELC function pins/groups.
	P70 to P77	I/O	General purpose input/output pins with 3.3-V tolerance.
	P80 to P87	I/O	General purpose input/output pins with 3.3-V tolerance. Selectable to use ELC function pins/groups.
	P90 to P92	I/O	General purpose input/output pins without 3.3-V tolerance.
	P93 to PA7	I/O	General purpose input/output pins with 3.3-V tolerance.
	PB0 to PB5	I/O	General purpose input/output pins without 3.3-V tolerance.

Note 1. Since this LSI has a resistor mounted between the USB20_VUBUSIN pin and V_{SS} , connect the pin to the USVBUS pin via a 30-k Ω ($\pm 1\%$) resistor. The schematic diagram is shown in **Figure 2.3-1**.

Note 2. QRESNSEL should be at the low level.

Note 3. SSLx1 to SSLx3 are output only.

Note 4. Half duplex: Ch. 0 to 9
Full duplex: Pairing ch. 0&9, 1&2, 3&4, 5&6, and 7&8

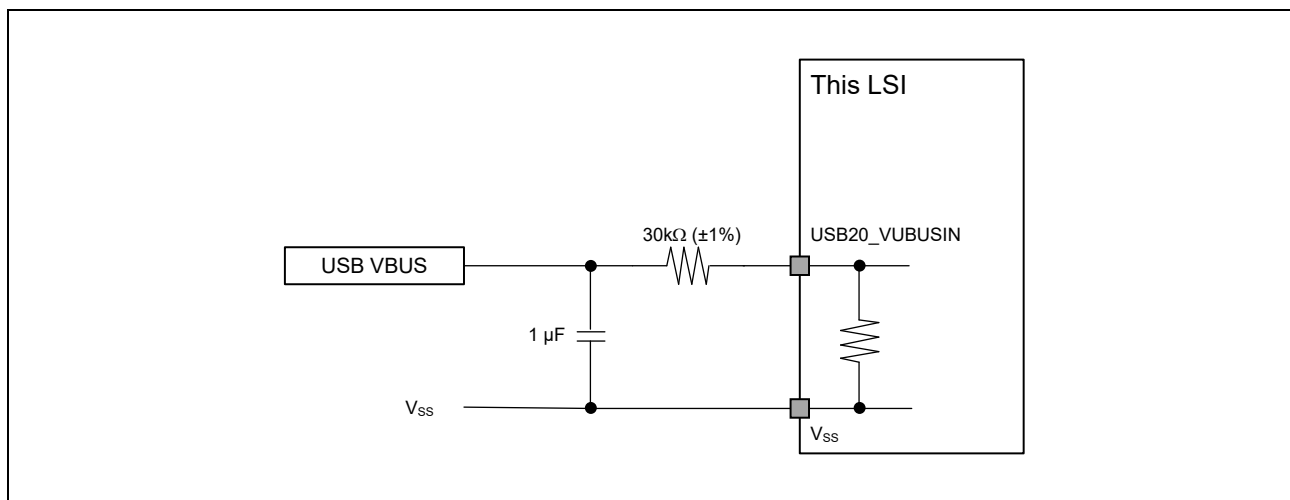


Figure 2.3-1 Connection Diagram of Resistor to USB20_VUBUSIN

2.4 Handling of Unused I/Os and Power Pins

For functions that are not used, the associated I/O pins and power pins should be handled as recommended to help reduce overall system power consumption and ensure proper electrical conditions.

The following tables show the recommended handling of unused I/O pins and power pins. For functions not listed here, refer to the "Pin State when not in Use" column in **Table 2.2-1**.

Table 2.4-1 Recommended Handling of I/O Pins and Power Pins for Unused JTAG Function

Unused Function	Pin Name	Recommended Handling
JTAG	TMS_SWDIO, TCK_SWCLK, TDO, TDI, TRSTN, VDD1833_JTAG, VDD1833_PRE18_JTAG	Open

Table 2.4-2 Recommended Handling of I/O Pins and Power Pins for Unused xSPI Function

Unused Function	Pin Name	Recommended Handling
xSPI0	XSPI0_CKP, XSPI0_KN, XSPI0_CS0N, XSPI0_DS, XSPI0_IO0 to 7, XSPI0_RESET0N, XSPI0_RST00N, XSPI0_INT0N, XSPI0_ECS0N, VDD1833_XSPI, VDD1833_PRE18_XSPI	Open

Table 2.4-3 Recommended Handling of I/O Pins and Power Pins for Unused SD Functions

Unused Function	Pin Name	Recommended Handling
SD0	SD0CLK, SD0CMD, SD0DAT0 to 7, SD0RSTN, VDD1833_SD0, VDD1833_PRE18_SD0	Open
SD1	SD1CLK, SD1CMD, SD1DAT0 to 3, VDD1833_SD1, VDD1833_PRE18_SD1	Open

Table 2.4-4 Recommended Handling of I/O Pins and Power Pins for Unused USB2 Functions

Unused Function	Pin Name	Recommended Handling
USB20	USB20_DP, USB20_DM, USB20_OTGID, USB20_VUBUSIN, USB20_OTGEXICEN, USB20_TXRTUNE	Open
	USB20_USVDD33, USB20_USVDD18, USB20_USDVDD	Connect to V _{SS}
USB21	USB21_DP, USB21_DM, USB21_TXRTUNE	Open
	USB21_USVDD33, USB21_USVDD18, USB21_USDVDD	Connect to V _{SS}

Table 2.4-5 Recommended Handling of I/O Pins and Power Pins for Unused USB3 Functions

Unused Function	Pin Name	Recommended Handling
USB30	USB30_DP, USB30_DM, USB30_RX0M, USB30_RX0P, USB30_TX0M, USB30_TX0P, USB30_TXRTUNE	Open
	USB30_USVPH, USB30_USVPTX, USB30_USVDD33, USB30_USVDD18, USB30_USDVDD	Keep powered
USB31	USB31_DP, USB31_DM, USB31_RX0M, USB31_RX0P, USB31_TX0M, USB31_TX0P, USB31_TXRTUNE	Open
	USB31_USVPH, USB31_USVPTX, USB31_USVDD33, USB31_USVDD18, USB31_USDVDD	Keep powered
Both USB30 and USB31	USB30_DP, USB30_DM, USB30_RX0M, USB30_RX0P, USB30_TX0M, USB30_TX0P, USB30_TXRTUNE, USB31_DP, USB31_DM, USB31_RX0M, USB31_RX0P, USB31_TX0M, USB31_TX0P, USB31_TXRTUNE, USB3_USRESREF	Open
	USB30_USVPH, USB30_USVPTX, USB30_USVDD33, USB30_USVDD18, USB30_USDVDD, USB31_USVPH, USB31_USVPTX, USB31_USVDD33, USB31_USVDD18, USB31_USDVDD	Connect to V _{SS}

Table 2.4-6 Recommended Handling of I/O Pins and Power Pins for Unused PCIe Function

Unused Function	Pin Name	Recommended Handling
PCIe (Lane 0 to Lane 3)	PCIE_TXDPL0, PCIE_TXDNL0, PCIE_TXDPL1, PCIE_TXDNL1, PCIE_TXDPL2, PCIE_TXDNL2, PCIE_TXDPL3, PCIE_TXDNL3, PCIE_RXDPL0, PCIE_RXDNL0, PCIE_RXDPL1, PCIE_RXDNL1, PCIE_RXDPL2, PCIE_RXDNL2, PCIE_RXDPL3, PCIE_RXDNL3, PCIE_REFCLKP0, PCIE_REFCLKN0, PCIE_REFCLKP1, PCIE_REFCLKN1, PCIE0_RSTOUTB, PCIE1_RSTOUTB	Open
	PCIE_VCC18ACMN, PCIE_VCC18AL01, PCIE_VCC18AL23, PCIE_VCC08AL01, PCIE_VCC08AL23	Connect to V _{SS}

Table 2.4-7 Recommended Handling of I/O Pins and Power Pins for Unused GBETH Functions

Unused Function	Pin Name	Recommended Handling
GBETH0	ET0_MDIO, ET0_MDC, ET0_RXCTL_RXDV, ET0_TXCTL_TXEN, ET0_TXER, ET0_RXER, ET0_RXC_RXCLK, ET0_TXC_TXCLK, ET0_CRS, ET0_COL, ET0_TXD0, ET0_TXD1, ET0_TXD2, ET0_TXD3, ET0_RXD0, ET0_RXD1, ET0_RXD2, ET0_RXD3, ET0_PHYINTR, VDD1833_ET0, VDD1833_PRE18_ET0	Open
GBETH1	ET1_MDIO, ET1_MDC, ET1_RXCTL_RXDV, ET1_TXCTL_TXEN, ET1_TXER, ET1_RXER, ET1_RXC_RXCLK, ET1_TXC_TXCLK, ET1_CRS, ET1_COL, ET1_TXD0, ET1_TXD1, ET1_TXD2, ET1_TXD3, ET1_RXD0, ET1_RXD1, ET1_RXD2, ET1_RXD3, ET1_PHYINTR, VDD1833_ET1, VDD1833_PRE18_ET1	Open

Table 2.4-8 Recommended Handling of I/O Pins and Power Pins for Unused MIPI DSI Function

Unused Function	Pin Name	Recommended Handling
DSI	DSI_DPCLK, DSI_DNCLK, DSI_DPDATA0, DSI_DNDATA0, DSI_DPDATA1, DSI_DNDATA1, DSI_DPDATA2, DSI_DNDATA2, DSI_DPDATA3, DSI_DNDATA3, DSI_VREG0P4V, DSI_VDD18, DSI_VDD12	Open
	DSI_VDD0P8	Keep powered

Table 2.4-9 Recommended Handling of I/O Pins and Power Pins for Unused MIPI CSI Functions

Unused Function	Pin Name	Recommended Handling
CSI0	CSI0_CLKP, CSI0_CLKN, CSI0_DATA0P, CSI0_DATA0N, CSI0_DATA1P, CSI0_DATA1N, CSI0_DATA2P, CSI0_DATA2N, CSI0_DATA3P, CSI0_DATA3N, CSI0_MSVDD18	Open
	CSI0_MSVDD0P8	Keep powered
CSI1	CSI1_CLKP, CSI1_CLKN, CSI1_DATA0P, CSI1_DATA0N, CSI1_DATA1P, CSI1_DATA1N, CSI1_DATA2P, CSI1_DATA2N, CSI1_DATA3P, CSI1_DATA3N, CSI1_MSVDD18	Open
	CSI1_MSVDD0P8	Keep powered
CSI2	CSI2_CLKP, CSI2_CLKN, CSI2_DATA0P, CSI2_DATA0N, CSI2_DATA1P, CSI2_DATA1N, CSI2_DATA2P, CSI2_DATA2N, CSI2_DATA3P, CSI2_DATA3N, CSI2_MSVDD18	Open
	CSI2_MSVDD0P8	Keep powered
CSI3	CSI3_CLKP, CSI3_CLKN, CSI3_DATA0P, CSI3_DATA0N, CSI3_DATA1P, CSI3_DATA1N, CSI3_DATA2P, CSI3_DATA2N, CSI3_DATA3P, CSI3_DATA3N, CSI3_MSVDD18	Open
	CSI3_MSVDD0P8	Keep powered

Table 2.4-10 Recommended Handling of I/O Pins and Power Pins for Unused DDR Functions

Unused Function	Pin Name	Recommended Handling
DDR0	DDR0_DQA0, DDR0_DQA1, DDR0_DQA2, DDR0_DQA3, DDR0_DQA4, DDR0_DQA5, DDR0_DQA6, DDR0_DQA7, DDR0_DMIA0, DDR0_DQSAT0, DDR0_DQSAC0, DDR0_DQA8, DDR0_DQA9, DDR0_DQA10, DDR0_DQA11, DDR0_DQA12, DDR0_DQA13, DDR0_DQA14, DDR0_DQA15, DDR0_DMIA1, DDR0_DQSAT1, DDR0_DQSAC1, DDR0_QB0, DDR0_QB1, DDR0_QB2, DDR0_QB3, DDR0_QB4, DDR0_QB5, DDR0_QB6, DDR0_QB7, DDR0_QB8, DDR0_QB9, DDR0_QB10, DDR0_QB11, DDR0_QB12, DDR0_QB13, DDR0_QB14, DDR0_QB15, DDR0_DMIB1, DDR0_DQSBT1, DDR0_DQSBC1, DDR0_CKEA0, DDR0_CKEA1, DDR0_CAA0, DDR0_CAA1, DDR0_CKAT, DDR0_CKAC, DDR0_CSA0, DDR0_CSA1, DDR0_CAA2, DDR0_CAA3, DDR0_CAA4, DDR0_CAA5, DDR0_CKEB0, DDR0_CKEB1, DDR0_CAB0, DDR0_CAB1, DDR0_CKBT, DDR0_CKBC, DDR0_CSB0, DDR0_CSB1, DDR0_CAB2, DDR0_CAB3, DDR0_CAB4, DDR0_CAB5, DDR0_RESETN, DDR0_DTEST, DDR0_ATEST, DDR0_ZN	Open
	DDR0_VDDQ, DDR0_VDDQLP, DDR0_VAA	Connect to V _{SS}
DDR1	DDR1_DQA0, DDR1_DQA1, DDR1_DQA2, DDR1_DQA3, DDR1_DQA4, DDR1_DQA5, DDR1_DQA6, DDR1_DQA7, DDR1_DMIA0, DDR1_DQSAT0, DDR1_DQSAC0, DDR1_DQA8, DDR1_DQA9, DDR1_DQA10, DDR1_DQA11, DDR1_DQA12, DDR1_DQA13, DDR1_DQA14, DDR1_DQA15, DDR1_DMIA1, DDR1_DQSAT1, DDR1_DQSAC1, DDR1_QB0, DDR1_QB1, DDR1_QB2, DDR1_QB3, DDR1_QB4, DDR1_QB5, DDR1_QB6, DDR1_QB7, DDR1_QB8, DDR1_QB9, DDR1_QB10, DDR1_QB11, DDR1_QB12, DDR1_QB13, DDR1_QB14, DDR1_QB15, DDR1_DMIB1, DDR1_DQSBT1, DDR1_DQSBC1, DDR1_CKEA0, DDR1_CKEA1, DDR1_CAA0, DDR1_CAA1, DDR1_CKAT, DDR1_CKAC, DDR1_CSA0, DDR1_CSA1, DDR1_CAA2, DDR1_CAA3, DDR1_CAA4, DDR1_CAA5, DDR1_CKEB0, DDR1_CKEB1, DDR1_CAB0, DDR1_CAB1, DDR1_CKBT, DDR1_CKBC, DDR1_CSB0, DDR1_CSB1, DDR1_CAB2, DDR1_CAB3, DDR1_CAB4, DDR1_CAB5, DDR1_RESETN, DDR1_DTEST, DDR1_ATEST, DDR1_ZN	Open
	DDR1_VDDQ, DDR1_VDDQLP, DDR1_VAA	Connect to V _{SS}

Section 3 Electrical Characteristics

This section describes the electrical characteristics of this LSI.

3.1 Absolute Maximum Ratings

Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 3.1-1 Absolute Maximum Ratings (1/3)

Unit Name	Item	Symbol	Min.	Max.	Unit
CA55	VDD09_CA55	CA55_V _{DD09}	-0.4	1.2	V
PD_OTHERS	VDD08_OTHERS	OTHERS_V _{DD08}	-0.4	1.2	V
	VDD33_OTHERS	OTHERS_V _{DD33}	-0.4	3.8	V
	VDD33_PRE18_OTHERS	OTHERS_PRE18V _{DD33}	-0.4	2.5	V
	VDD1833_OTHERS_A	OTHERSA_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_OTHERS_A	OTHERSA_PRE18V _{DD1833}	-0.4	2.5	V
	VDD1833_OTHERS_B	OTHERSB_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_OTHERS_B	OTHERSB_PRE18V _{DD1833}	-0.4	2.5	V
	VDD1833_OTHERS_C	OTHERSC_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_OTHERS_C	OTHERSC_PRE18V _{DD1833}	-0.4	2.5	V
	VDD1833_OTHERS_D	OTHERSD_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_OTHERS_D	OTHERSD_PRE18V _{DD1833}	-0.4	2.5	V
PD_AWO	VDD08_AWO	AWO_V _{DD08}	-0.4	1.2	V
	VDD18_AWO	AWO_V _{DD18}	-0.4	2.5	V
	VDD1833_AWO	AWO_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_AWO	AWO_PRE18V _{DD1833}	-0.4	2.5	V
USB30	USB30_USVPH	USB30_USV _{PH}	-0.4	2.5	V
	USB30_USVPTX	USB30_USV _{PTX}	-0.4	1.2	V
	USB30_USVDD33	USB30_USV _{DD33}	-0.4	3.8	V
	USB30_USVDD18	USB30_USV _{DD18}	-0.4	2.5	V
	USB30_USDVDD	USB30_USDV _{DD}	-0.4	1.2	V
USB31	USB31_USVPH	USB31_USV _{PH}	-0.4	2.5	V
	USB31_USVPTX	USB31_USV _{PTX}	-0.4	1.2	V
	USB31_USVDD33	USB31_USV _{DD33}	-0.4	3.8	V
	USB31_USVDD18	USB31_USV _{DD18}	-0.4	2.5	V
	USB31_USDVDD	USB31_USDV _{DD}	-0.4	1.2	V
USB20	USB20_USVDD33	USB20_USV _{DD33}	-0.4	3.8	V
	USB20_USVDD18	USB20_USV _{DD18}	-0.4	2.5	V
	USB20_USDVDD	USB20_USDV _{DD}	-0.4	1.2	V
USB21	USB21_USVDD33	USB21_USV _{DD33}	-0.4	3.8	V
	USB21_USVDD18	USB21_USV _{DD18}	-0.4	2.5	V
	USB21_USDVDD	USB21_USDV _{DD}	-0.4	1.2	V
TSU0	TS0AVDD18	TS0AV _{DD18}	-0.4	2.5	V
	TS0DVDD08A	TS0DV _{DD08A}	-0.4	1.2	V
TSU1	TS1AVDD18	TS1AV _{DD18}	-0.4	2.5	V
	TS1DVDD08A	TS1DV _{DD08A}	-0.4	1.2	V

Table 3.1-1 Absolute Maximum Ratings (2/3)

Unit Name	Item	Symbol	Min.	Max.	Unit
xSPI	VDD1833_XSPI	XSPI_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_XSPI	XSPI_PRE18V _{DD1833}	-0.4	2.5	V
SD0	VDD1833_SD0	SD0_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_SD0	SD0_PRE18V _{DD1833}	-0.4	2.5	V
SD1	VDD1833_SD1	SD1_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_SD1	SD1_PRE18V _{DD1833}	-0.4	2.5	V
SD2	VDD1833_SD2	SD2_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_SD2	SD2_PRE18V _{DD1833}	-0.4	2.5	V
OTP	OTPVDD18	OTP_V _{DD18}	-0.4	2.5	V
DDR0	VDD08_DDR	DDR_V _{DD08}	-0.4	1.2	V
	DDR0_VDDQ	DDR0_V _{DDQ}	-0.4	1.5	V
	DDR0_VDDQLP	DDR0_V _{DDQLP}	-0.4	1.5	V
	DDR0_VAA	DDR0_V _{AA}	-0.4	2.5	V
DDR1	VDD08_DDR	DDR_V _{DD08}	-0.4	1.2	V
	DDR1_VDDQ	DDR1_V _{DDQ}	-0.4	1.5	V
	DDR1_VDDQLP	DDR1_V _{DDQLP}	-0.4	1.5	V
	DDR1_VAA	DDR1_V _{AA}	-0.4	2.5	V
GBETH0	VDD1833_ET0	ET0_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_ET0	ET0_PRE18V _{DD1833}	-0.4	2.5	V
GBETH1	VDD1833_ET1	ET1_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_ET1	ET1_PRE18V _{DD1833}	-0.4	2.5	V
CRU0	CSI0_MSVDD18	CSI0_MSV _{DD18}	-0.4	2.5	V
	CSI0_MSVDD0P8	CSI0_MSV _{DD0P8}	-0.4	1.2	V
CRU1	CSI1_MSVDD18	CSI1_MSV _{DD18}	-0.4	2.5	V
	CSI1_MSVDD0P8	CSI1_MSV _{DD0P8}	-0.4	1.2	V
CRU2	CSI2_MSVDD18	CSI2_MSV _{DD18}	-0.4	2.5	V
	CSI2_MSVDD0P8	CSI2_MSV _{DD0P8}	-0.4	1.2	V
CRU3	CSI3_MSVDD18	CSI3_MSV _{DD18}	-0.4	2.5	V
	CSI3_MSVDD0P8	CSI3_MSV _{DD0P8}	-0.4	1.2	V
DSI	DSI_VDD0P8	DSI_V _{DD0P8}	-0.4	1.2	V
	DSI_VDD12	DSI_V _{DD12}	-0.4	2.5	V
	DSI_VDD18	DSI_V _{DD18}	-0.4	2.5	V
PCIE	PCIE_VCC18ACMN	PCIE_V _{CC18ACMN}	-0.4	2.5	V
	PCIE_VCC18AL01	PCIE_V _{CC18AL01}	-0.4	2.5	V
	PCIE_VCC18AL23	PCIE_V _{CC18AL23}	-0.4	2.5	V
	PCIE_VCC08AL01	PCIE_V _{CC08AL01}	-0.4	1.2	V
	PCIE_VCC08AL23	PCIE_V _{CC08AL23}	-0.4	1.2	V
I3C	VDD1218_I3C	I3C_V _{DD1218}	-0.4	2.5	V
ADC	ADAVDD18	ADAV _{DD18}	-0.4	2.5	V

Table 3.1-1 Absolute Maximum Ratings (3/3)

Unit Name	Item	Symbol	Min.	Max.	Unit
CPG	PLVDD_PLLCM33	PLLCM33_PLV _{DD}	-0.4	2.5	V
	PLVDD_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_PLV _{DD}	-0.4	2.5	V
	PLVDD_PLLCA55	PLICA55_PLV _{DD}	-0.4	2.5	V
	PLVDD_PLLVDO_DSI	PLLVDO_DSI_PLV _{DD}	-0.4	2.5	V
	PLVDD_PLDDR0	PLDDR0_PLV _{DD}	-0.4	2.5	V
	PLVDD_PLDDR1	PLDDR1_PLV _{DD}	-0.4	2.5	V
	PLVDD_PLLETH_GPU	PLLETH_GPU_PLV _{DD}	-0.4	2.5	V
	PLDVDD08_PLLCM33	PLLCM33_PLDV _{DD08}	-0.4	1.2	V
	PLDVDD08_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_PLDV _{DD08}	-0.4	1.2	V
	PLDVDD09_PLICA55	PLICA55_PLDV _{DD09}	-0.4	1.2	V
	PLDVDD08_PLLVDO_DSI	PLLVDO_DSI_PLDV _{DD08}	-0.4	1.2	V
	PLDVDD08_PLDDR0	PLDDR0_PLDV _{DD08}	-0.4	1.2	V
	PLDVDD08_PLDDR1	PLDDR1_PLDV _{DD08}	-0.4	1.2	V
	PLDVDD08_PLLETH_GPU	PLLETH_GPU_PLDV _{DD08}	-0.4	1.2	V
CST	VDD1833_JTAG	JTAG_V _{DD1833}	-0.4	3.8	V
	VDD1833_PRE18_JTAG	JTAG_PRE18V _{DD1833}	-0.4	2.5	V
PWC	VDD18_PWC	PWC_V _{DD18}	-0.4	2.5	V
—	Input voltage (0.6-V I/O)	V _{in06}	-0.4	DDRn_V _{DDQLP} + 0.3 ^{*1}	V
—	Input voltage (1.1-V I/O)	V _{in11}	-0.4	DDRn_V _{DDQ} + 0.3 ^{*1}	V
—	Input voltage (1.2-V I/O)	V _{in12}	-0.4	V ₁₂ + 0.5 ^{*2}	V
—	Input voltage (1.8-V I/O)	V _{in18}	-0.4	V ₁₈ + 0.5 ^{*3}	V
—	Input voltage (1.8-V I/O (3.3-V tolerant))* ⁴	V _{in18_tol}	-0.4	3.63	V
—	Input voltage (3.3-V I/O)	V _{in33}	-0.4	3.8	V
—	Analog input voltage (ADC I/O)	V _{ain18}	0	ADAV _{DD18}	V
—	Junction temperature	T _j	-40	125	°C
—	Storage temperature	T _{stg}	-40	150	°C

Note 1. n = 0, 1. The voltage to be applied must be within the absolute maximum rating (1.5 V).

Note 2. The voltage to be applied must be within the absolute maximum rating (2.5 V). V₁₂ indicates the power supply voltage for 1.2-V I/O pins.

Note 3. The voltage to be applied must be within the absolute maximum rating (2.5 V). V₁₈ indicates the power supply voltage for 1.8-V I/O pins. When 1.8 V is used for the 3.3/1.8-V switching I/O, this specification is applied.

Note 4. Pxx pins (with the exceptions of P2x, P90, P91, P92, and PBx)

3.2 Recommended Operating Range

Table 3.2-1 Recommended Operating Range (1/3)

Unit Name	Item	Symbol	Min.	Typ.	Max.	Unit	Note
CA55	VDD09_CA55	CA55_V _{DD09}	0.86	0.9	0.94	V	0.9 V: OD*1
			0.76	0.8	0.84	V	0.8 V: ND*1
PD_OTHERS	VDD08_OTHERS	OTHERS_V _{DD08}	0.76	0.8	0.84	V	*2
	VDD33_OTHERS	OTHERS_V _{DD33}	3.14	3.3	3.46	V	
	VDD33_PRE18_OTHERS	OTHERS_PRE18V _{DD33}	1.71	1.8	1.89	V	
	VDD1833_OTHERS_A	OTHERSA_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_OTHERS_A	OTHERSA_PRE18V _{DD1833}	1.71	1.8	1.89	V	
	VDD1833_OTHERS_B	OTHERSB_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_OTHERS_B	OTHERSB_PRE18V _{DD1833}	1.71	1.8	1.89	V	
	VDD1833_OTHERS_C	OTHERSC_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_OTHERS_C	OTHERSC_PRE18V _{DD1833}	1.71	1.8	1.89	V	
PD_AWO	VDD1833_OTHERS_D	OTHERSD_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_OTHERS_D	OTHERSD_PRE18V _{DD1833}	1.71	1.8	1.89	V	
	VDD08_AWO	AWO_V _{DD08}	0.76	0.8	0.84	V	
	VDD18_AWO	AWO_V _{DD18}	1.71	1.8	1.89	V	
USB30	VDD1833_AWO	AWO_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_AWO	AWO_PRE18V _{DD1833}	1.71	1.8	1.89	V	
	VDD1833_PRE18_AWO	AWO_PRE18V _{DD1833}	1.71	1.8	1.89	V	
USB30	USB30_USVPH	USB30_USV _{PH}	1.71	1.8	1.89	V	
	USB30_USVPTX	USB30_USV _{PTX}	0.76	0.8	0.84	V	
	USB30_USVDD33	USB30_USV _{DD33}	3.14	3.3	3.46	V	
	USB30_USVDD18	USB30_USV _{DD18}	1.71	1.8	1.89	V	
	USB30_USDVDD	USB30_USDV _{DD}	0.76	0.8	0.84	V	
USB31	USB31_USVPH	USB31_USV _{PH}	1.71	1.8	1.89	V	
	USB31_USVPTX	USB31_USV _{PTX}	0.76	0.8	0.84	V	
	USB31_USVDD33	USB31_USV _{DD33}	3.14	3.3	3.46	V	
	USB31_USVDD18	USB31_USV _{DD18}	1.71	1.8	1.89	V	
	USB31_USDVDD	USB31_USDV _{DD}	0.76	0.8	0.84	V	
USB20	USB20_USVDD33	USB20_USV _{DD33}	3.14	3.3	3.46	V	
	USB20_USVDD18	USB20_USV _{DD18}	1.71	1.8	1.89	V	
	USB20_USDVDD	USB20_USDV _{DD}	0.76	0.8	0.84	V	
USB21	USB21_USVDD33	USB21_USV _{DD33}	3.14	3.3	3.46	V	
	USB21_USVDD18	USB21_USV _{DD18}	1.71	1.8	1.89	V	
	USB21_USDVDD	USB21_USDV _{DD}	0.76	0.8	0.84	V	
TSU0	TS0AVDD18	TS0AV _{DD18}	1.71	1.8	1.89	V	
	TS0DVDD08A	TS0DV _{DD08A}	0.76	0.8	0.84	V	
TSU1	TS1AVDD18	TS1AV _{DD18}	1.71	1.8	1.89	V	
	TS1DVDD08A	TS1DV _{DD08A}	0.76	0.8	0.84	V	
xSPI	VDD1833_XSPI	XSPI_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_XSPI	XSPI_PRE18V _{DD1833}	1.71	1.8	1.89	V	

Table 3.2-1 Recommended Operating Range (2/3)

Unit Name	Item	Symbol	Min.	Typ.	Max.	Unit	Note
SD0	VDD1833_SD0	SD0_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_SD0	SD0_PRE18V _{DD1833}	1.71	1.8	1.89	V	
SD1	VDD1833_SD1	SD1_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_SD1	SD1_PRE18V _{DD1833}	1.71	1.8	1.89	V	
SD2	VDD1833_SD2	SD2_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_SD2	SD2_PRE18V _{DD1833}	1.71	1.8	1.89	V	
OTP	OTPVDD18	OTP_V _{DD18}	1.71	1.8	1.89	V	
DDR0	VDD08_DDR	DDR_V _{DD08}	0.76	0.8	0.84	V	*2
	DDR0_VDDQ	DDR0_V _{DDQ}	1.06	1.1	1.17	V	
	DDR0_VDDQLP	DDR0_V _{DDQLP}	0.57	0.6	0.65	V	0.6 V: LPDDR4X
			1.06	1.1	1.17	V	1.1 V: LPDDR4
	DDR0_VAA	DDR0_V _{AA}	1.71	1.8	1.89	V	
DDR1	VDD08_DDR	DDR_V _{DD08}	0.76	0.8	0.84	V	*2
	DDR1_VDDQ	DDR1_V _{DDQ}	1.06	1.1	1.17	V	
	DDR1_VDDQLP	DDR1_V _{DDQLP}	0.57	0.6	0.65	V	0.6 V: LPDDR4X
			1.06	1.1	1.17	V	1.1 V: LPDDR4
	DDR1_VAA	DDR1_V _{AA}	1.71	1.8	1.89	V	
GBETH0	VDD1833_ET0	ET0_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_ET0	ET0_PRE18V _{DD1833}	1.71	1.8	1.89	V	
GBETH1	VDD1833_ET1	ET1_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_ET1	ET1_PRE18V _{DD1833}	1.71	1.8	1.89	V	
CRU0	CSI0_MSVDD18	CSI0_MSV _{DD18}	1.71	1.8	1.89	V	
	CSI0_MSVDD0P8	CSI0_MSV _{DD0P8}	0.76	0.8	0.84	V	
CRU1	CSI1_MSVDD18	CSI1_MSV _{DD18}	1.71	1.8	1.89	V	
	CSI1_MSVDD0P8	CSI1_MSV _{DD0P8}	0.76	0.8	0.84	V	
CRU2	CSI2_MSVDD18	CSI2_MSV _{DD18}	1.71	1.8	1.89	V	
	CSI2_MSVDD0P8	CSI2_MSV _{DD0P8}	0.76	0.8	0.84	V	
CRU3	CSI3_MSVDD18	CSI3_MSV _{DD18}	1.71	1.8	1.89	V	
	CSI3_MSVDD0P8	CSI3_MSV _{DD0P8}	0.76	0.8	0.84	V	
DSI	DSI_VDD0P8	DSI_V _{DD0P8}	0.76	0.8	0.84	V	
	DSI_VDD12	DSI_V _{DD12}	1.14	1.2	1.26	V	
	DSI_VDD18	DSI_V _{DD18}	1.71	1.8	1.89	V	
PCIE	PCIE_VCC18ACMN	PCIE_V _{CC18ACMN}	1.71	1.8	1.89	V	
	PCIE_VCC18AL01	PCIE_V _{CC18AL01}	1.71	1.8	1.89	V	
	PCIE_VCC18AL23	PCIE_V _{CC18AL23}	1.71	1.8	1.89	V	
	PCIE_VCC08AL01	PCIE_V _{CC08AL01}	0.76	0.8	0.84	V	
	PCIE_VCC08AL23	PCIE_V _{CC08AL23}	0.76	0.8	0.84	V	
I3C	VDD1218_I3C	I3C_V _{DD1218}	1.71	1.8	1.89	V	
			1.14	1.2	1.26	V	
ADC	ADAVDD18	ADAV _{DD18}	1.71	1.8	1.89	V	

Table 3.2-1 Recommended Operating Range (3/3)

Unit Name	Item	Symbol	Min.	Typ.	Max.	Unit	Note
CPG	PLVDD_PLLCM33	PLLCM33_PLV _{DD}	1.71	1.8	1.89	V	
	PLVDD_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_PLV _{DD}	1.71	1.8	1.89	V	
	PLVDD_PLLCA55	PLLCA55_PLV _{DD}	1.71	1.8	1.89	V	
	PLVDD_PLLVDO_DSI	PLLVDO_DSI_PLV _{DD}	1.71	1.8	1.89	V	
	PLVDD_PLLDDR0	PLDDR0_PLV _{DD}	1.71	1.8	1.89	V	
	PLVDD_PLLDDR1	PLDDR1_PLV _{DD}	1.71	1.8	1.89	V	
	PLVDD_PLLETH_GPU	PLLETH_GPU_PLV _{DD}	1.71	1.8	1.89	V	
	PLDVDD08_PLLCM33	PLLCM33_PLDV _{DD08}	0.76	0.8	0.84	V	
	PLDVDD08_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_PLD _{VDD08}	0.76	0.8	0.84	V	
	PLDVDD09_PLLCA55	PLLCA55_PLDV _{DD09}	0.86	0.9	0.94	V	0.9 V: OD*1
			0.76	0.8	0.84	V	0.8 V: ND*1
	PLDVDD08_PLLVDO_DSI	PLLVDO_DSI_PLDV _{DD08}	0.76	0.8	0.84	V	
	PLDVDD08_PLDDR0	PLDDR0_PLDV _{DD08}	0.76	0.8	0.84	V	
	PLDVDD08_PLDDR1	PLDDR1_PLDV _{DD08}	0.76	0.8	0.84	V	
	PLDVDD08_PLLETH_GPU	PLLETH_GPU_PLDV _{DD08}	0.76	0.8	0.84	V	
CST	VDD1833_JTAG	JTAG_V _{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_JTAG	JTAG_PRE18V _{DD1833}	1.71	1.8	1.89	V	
PWC	VDD18_PWC	PWC_V _{DD18}	1.71	1.8	1.89	V	

Note 1. OD: Over drive (up to 1.8-GHz operation frequency)
 ND: Normal drive (up to 1.1-GHz operation frequency)

Note 2. To avoid the possibility of noise, separating this power supply from other power supply terminals is recommended.

3.3 Power-On/Off Sequence

3.3.1 CM33 Boot Mode (PWC Enabled)

The state diagram of CM33 cold boot is shown in **Figure 3.3-1**. The boot mode states (1) to (4) refer to the sequence of (1) to (4) in **Figure 3.3-2**.

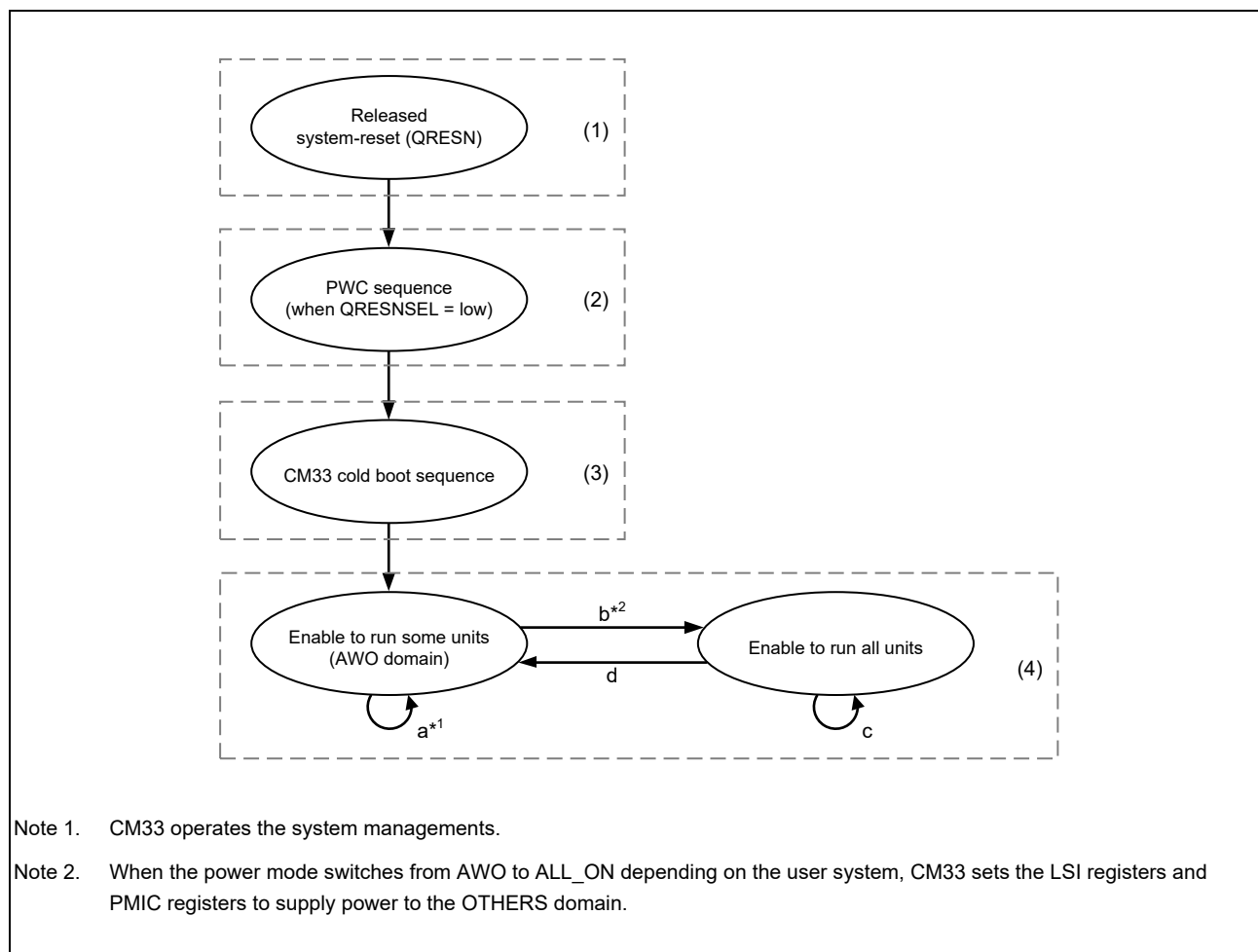
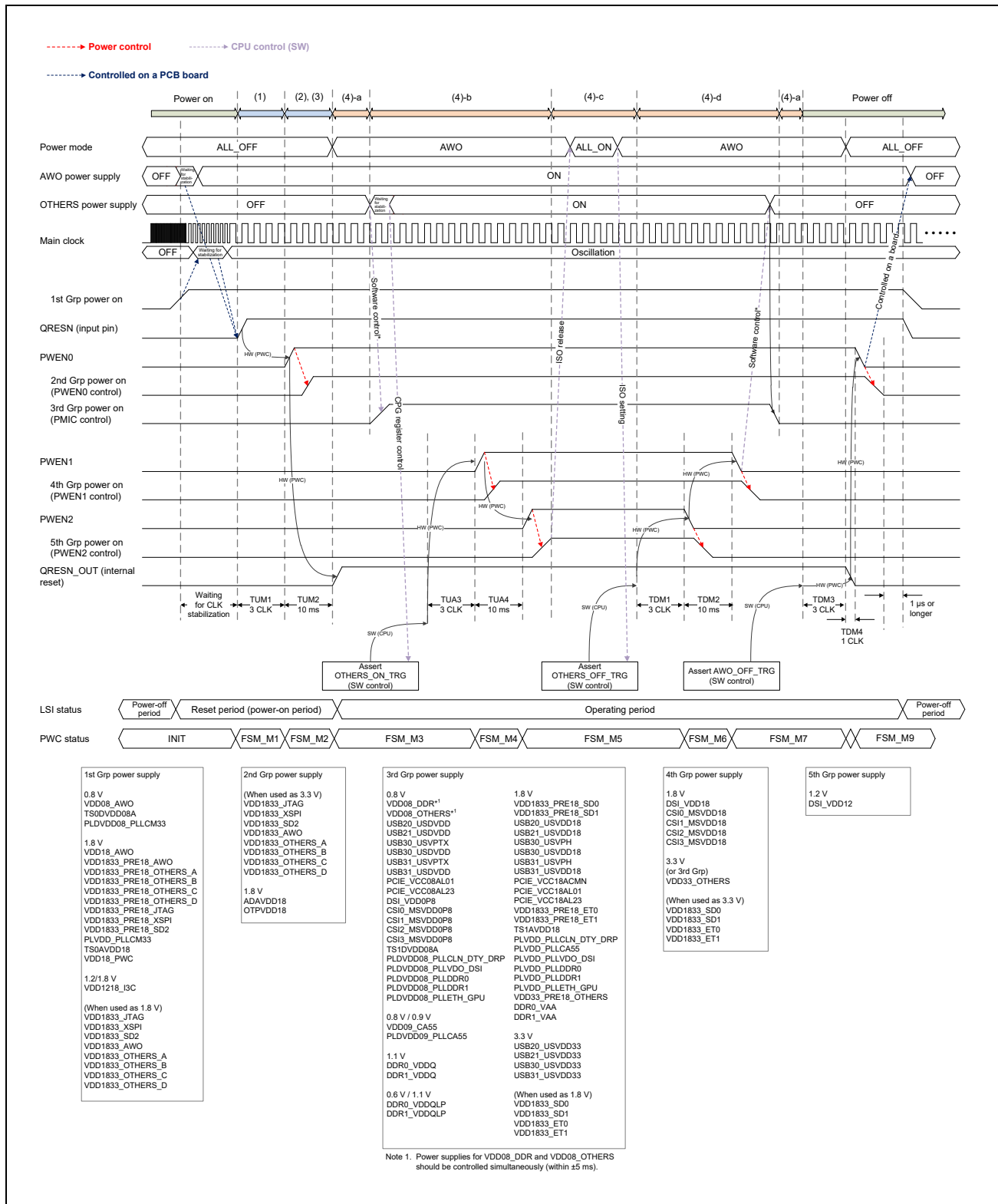


Figure 3.3-1 CM33 Boot State Diagram



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Software control: RIIC or PFC (GPIO) control

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation. In addition, ensure that each clock is applied only after the corresponding I/O power supply has been enabled.

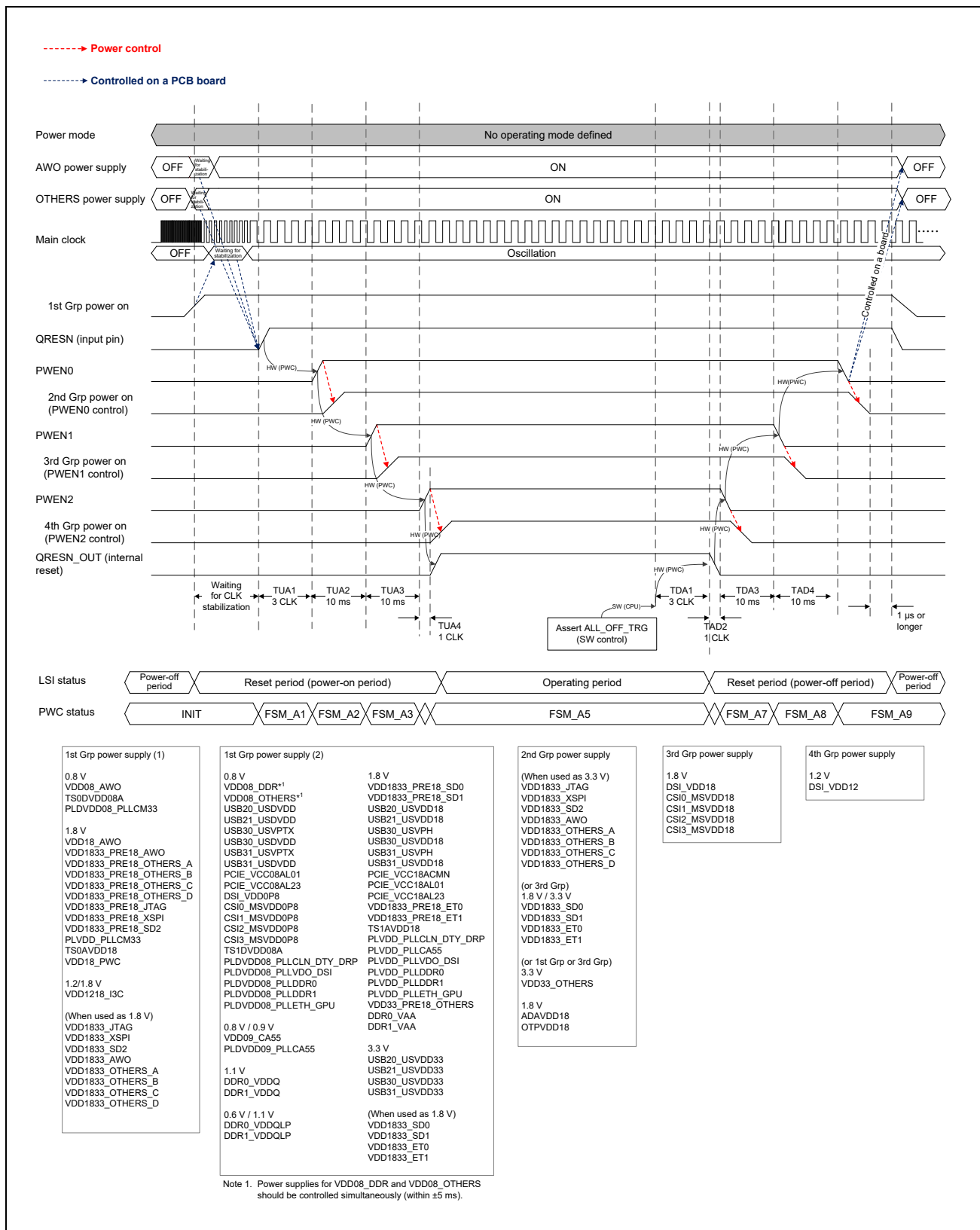
Note: Refer to the notes in **Section 3.3.3** and **Section 3.3.4** for details on the restrictions on the rise time and fall time of each power supply.

Note: When the QRESN pin becomes low, the PWEN0 to PWEN2 pins become low simultaneously.

Note: When using the PWC, set QRESN to the low level at the same time as or after the 1st Grp power off.

Figure 3.3-2 Power-On/Power-Off Sequence (CM33 Boot)

3.3.2 CA55 Boot Mode (PWC Enabled)



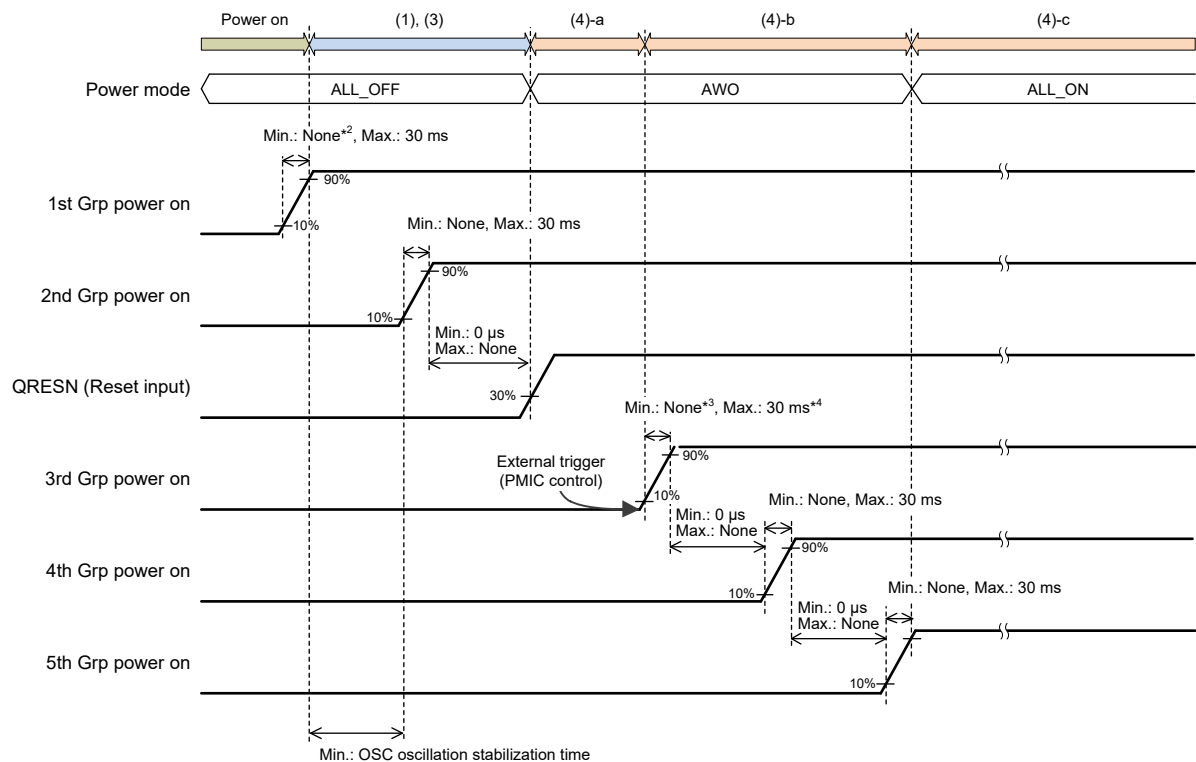
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- Note:** The clock stabilization time depends on the board design. Make the setting according to the results of evaluation. In addition, ensure that each clock is applied only after the corresponding I/O power supply has been enabled.
- Note:** Refer to the notes in **Section 3.3.5** and **Section 3.3.6** for details on the restrictions on the rise time and fall time of each power supply.
- Note:** When the QRESN pin becomes low, the PWEN0 to PWEN2 pins become low simultaneously.
- Note:** When using the PWC, set QRESN to the low level at the same time as or after the 1st Grp power off.

Figure 3.3-3 Power-On/Power-Off Sequence (CA55 Boot)

3.3.3 Power-On Sequence – CM33 Boot Mode (PWC Disabled)



1st Grp power supply

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_OTHERS_A
VDD1833_PRE18_OTHERS_B
VDD1833_PRE18_OTHERS_C
VDD1833_PRE18_OTHERS_D
VDD1833_PRE18_JTAG
VDD1833_PRE18_XSPI
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1.8 V
ADA/VDD18
OTP/VDD18

3rd Grp power supply

0.8 V
VDD08_DDR*¹
VDD08_OTHERS*¹
USB20_USDVDD
USB21_USDVDD
USB30_USVPTX
USB30_USDVDD
USB31_USVPTX
USB31_USDVDD
PCIE_VCC08AL01
PCIE_VCC08AL23
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
CSI2_MSVDD0P8
CSI3_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLDDR0
PLDVDD08_PLDDR1
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLCA55

1.1 V
DDR0_VDDQ
DDR1_VDDQ

0.6 V / 1.1 V
DDR0_VDDQLP
DDR1_VDDQLP

1.8 V
VDD1833_PRE18_SD0
VDD1833_PRE18_SD1
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
USB31_USVPH
USB31_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
PCIE_VCC18AL23
VDD1833_PRE18_ET0
VDD1833_PRE18_ET1
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLDDR0
PLVDD_PLDDR1
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA
DDR1_VAA

3.3 V
USB20_USVDD33
USB21_USVDD33
USB30_USVDD33
USB31_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

4th Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18
CSI2_MSVDD18
CSI3_MSVDD18

3.3 V
(or 3rd Grp)
VDD33_OTHERS

(When used as 3.3 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

5th Grp power supply

1.2 V
DSI_VDD12

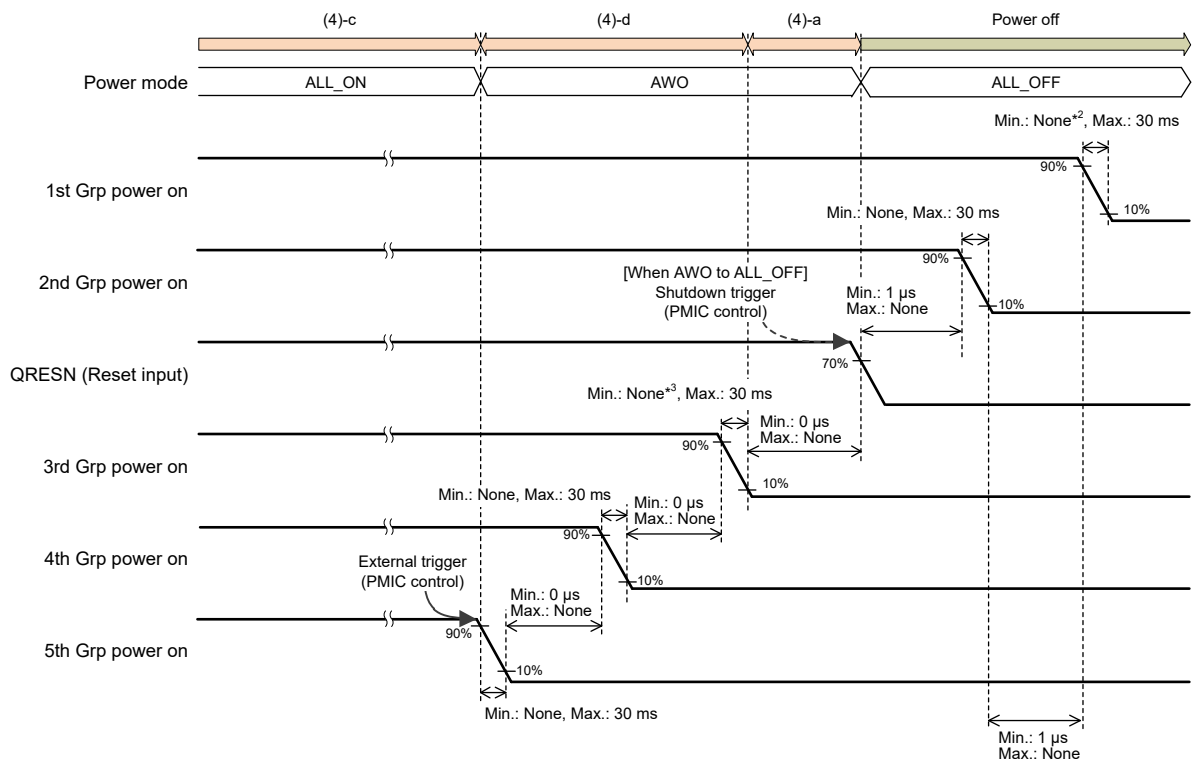
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- Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ± 5 ms).
- Note 2. TS0DVDD08A, TS0AVDD18: Min. 10 μ s
- Note 3. – DDR0_VDDQ, DDR0_VDDQLP, DDR1_VDDQ, DDR1_VDDQLP (1.1 V): Min. 180 μ s
 – DDR0_VDDQLP, DDR1_VDDQLP (0.6 V): Min. 100 μ s
 – DDR0_VAA, DDR1_VAA: Min. 290 μ s
 – VDD08_DDR: Min. 5 μ s
 – USB30_USVPTX, USB31_USVPTX, USB30_USVPH, USB31_USVPH: Min. 10 μ s
 – USB20_USDVDD, USB21_USDVDD, USB30_USDVDD, USB31_USDVDD: Min. 10 μ s
 – USB20_USVDD18, USB21_USVDD18, USB30_USVDD18, USB31_USVDD18: Min. 20 μ s
 – USB20_USVDD33, USB21_USVDD33, USB30_USVDD33, USB31_USVDD33: Min. 30 μ s
 – TS1DVDD08A, TS1AVDD18: Min. 10 μ s
- Note 4. USB20_USDVDD, USB21_USDVDD, USB20_USVDD18, USB21_USVDD18, USB20_USVDD33, USB21_USVDD33, USB30_USDVDD, USB31_USDVDD, USB30_USVDD18, USB31_USVDD18, USB30_USVDD33, USB31_USVDD33: Max. 10 ms
- Note:** The clock stabilization time depends on the board design. Make the setting according to the results of evaluation. In addition, ensure that each clock is applied only after the corresponding I/O power supply has been enabled.
- Note:** The rise time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-4 Power-On Sequence (CM33 Boot Mode)

3.3.4 Power-Off Sequence – CM33 Boot Mode (PWC Disabled)



1st Grp power supply

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_OTHERS_A
VDD1833_PRE18_OTHERS_B
VDD1833_PRE18_OTHERS_C
VDD1833_PRE18_OTHERS_D
VDD1833_PRE18_JTAG
VDD1833_PRE18_XSPI
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1.8 V
ADAVDD18
OTPVDD18

3rd Grp power supply

0.8 V
VDD08_DDR*¹
VDD08_OTHERS*¹
USB20_USDVDD
USB21_USDVDD
USB30_USVPTX
USB30_USDVDD
USB31_USVPTX
USB31_USDVDD
PCIE_VCC08AL01
PCIE_VCC08AL23
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
CSI2_MSVDD0P8
CSI3_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLDDR0
PLDVDD08_PLDDR1
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

1.1 V
DDR0_VDDQ
DDR1_VDDQ

0.6 V / 1.1 V
DDR0_VDDQLP
DDR1_VDDQLP

1.8 V
VDD1833_PRE18_SD0
VDD1833_PRE18_SD1
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
USB31_USVPH
USB31_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
PCIE_VCC18AL23
VDD1833_PRE18_ET0
VDD1833_PRE18_ET1
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLDDR0
PLVDD_PLDDR1
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA
DDR1_VAA

3.3 V
USB20_USVDD33
USB21_USVDD33
USB30_USVDD33
USB31_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

4th Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18
CSI2_MSVDD18
CSI3_MSVDD18

3.3 V
(or 3rd Grp)
VDD33_OTHERS

(When used as 3.3 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

5th Grp power supply

1.2 V
DSI_VDD12

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Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ± 5 ms).

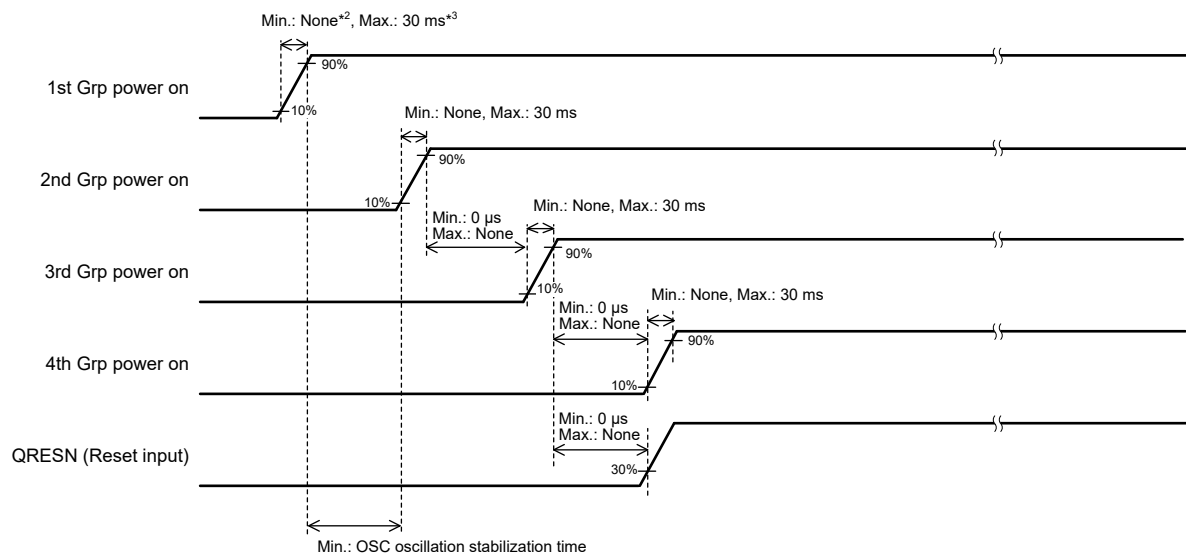
Note 2. TS0DVDD08A, TS0AVDD18: Min. 10 μ s

Note 3. TS1DVDD08A, TS1AVDD18: Min. 10 μ s

Note: The fall time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-5 Power-Off Sequence (CM33 Boot Mode)

3.3.5 Power-On Sequence – CA55 Boot Mode (PWC Disabled)



1st Grp power supply (1)

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_OTHERS_A
VDD1833_PRE18_OTHERS_B
VDD1833_PRE18_OTHERS_C
VDD1833_PRE18_OTHERS_D
VDD1833_PRE18_JTAG
VDD1833_PRE18_XSPI
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1st Grp power supply (2)

0.8 V
VDD08_DDR^{*1}
VDD08_OTHERS^{*1}
USB20_USDVDD
USB21_USDVDD
USB30_USVPTX
USB30_USDVDD
USB31_USVPTX
USB31_USDVDD
PCIE_VCC08AL01
PCIE_VCC08AL23
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
CSI2_MSVDD0P8
CSI3_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLDDR0
PLDVDD08_PLDDR1
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLCCA55

1.1 V
DDR0_VDDQ
DDR1_VDDQ

0.6 V / 1.1 V
DDR0_VDDQLP
DDR1_VDDQLP

1.8 V
VDD1833_PRE18_SD0
VDD1833_PRE18_SD1
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
USB31_USVPH
USB31_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
PCIE_VCC18AL23
VDD1833_PRE18_ET0
VDD1833_PRE18_ET1
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLCCA55
PLVDD_PLLVDO_DSI
PLVDD_PLDDR0
PLVDD_PLDDR1
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA
DDR1_VAA

3.3 V
USB20_USVDD33
USB21_USVDD33
USB30_USVDD33
USB31_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

(or 3rd Grp)
1.8 V / 3.3 V
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

(or 1st Grp or 3rd Grp)
3.3 V
VDD33_OTHERS

1.8 V
ADAVDD18
OTPVDD18

3rd Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18
CSI2_MSVDD18
CSI3_MSVDD18

4th Grp power supply

1.2 V
DSI_VDD12

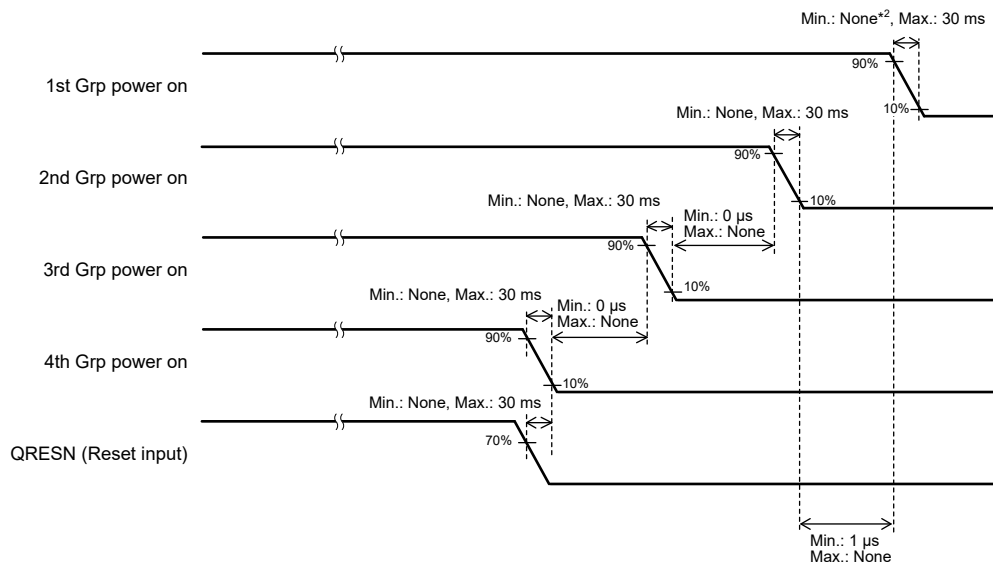
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- Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ± 5 ms).
- Note 2.
- TS0DVDD08A, TS0AVDD18: Min. 10 μ s
 - DDR0_VDDQ, DDR0_VDDQLP, DDR1_VDDQ, DDR1_VDDQLP (1.1 V): Min. 180 μ s
 - DDR0_VDDQLP, DDR1_VDDQLP (0.6 V): Min. 100 μ s
 - DDR0_VAA, DDR1_VAA: Min. 290 μ s
 - VDD08_DDR: Min. 5 μ s
 - USB30_USVPTX, USB31_USVPTX, USB30_USVPH, USB31_USVPH: Min. 10 μ s
 - USB20_USDVDD, USB21_USDVDD, USB30_USDVDD, USB31_USDVDD: Min. 10 μ s
 - USB20_USVDD18, USB21_USVDD18, USB30_USVDD18, USB31_USVDD18: Min. 20 μ s
 - USB20_USVDD33, USB21_USVDD33, USB30_USVDD33, USB31_USVDD33: Min. 30 μ s
 - TS1DVDD08A, TS1AVDD18: Min. 10 μ s
- Note 3. USB20_USDVDD, USB21_USDVDD, USB20_USVDD18, USB21_USVDD18, USB20_USVDD33, USB21_USVDD33, USB30_USDVDD, USB31_USDVDD, USB30_USVDD18, USB31_USVDD18, USB30_USVDD33, USB31_USVDD33: Max. 10 ms
- Note:** The clock stabilization time depends on the board design. Make the setting according to the results of evaluation. In addition, ensure that each clock is applied only after the corresponding I/O power supply has been enabled.
- Note:** The rise time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-6 Power-On Sequence (CA55 Boot Mode)

3.3.6 Power-Off Sequence – CA55 Boot Mode (PWC Disabled)



1st Grp power supply (1)

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_OTHERS_A
VDD1833_PRE18_OTHERS_B
VDD1833_PRE18_OTHERS_C
VDD1833_PRE18_OTHERS_D
VDD1833_PRE18_JTAG
VDD1833_PRE18_XSPI
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1st Grp power supply (2)

0.8 V
VDD08_DDR*¹
VDD08_OTHERS*¹
USB20_USDVDD
USB21_USDVDD
USB30_USVPTX
USB30_USDVDD
USB31_USVPTX
USB31_USDVDD
PCIE_VCC08AL01
PCIE_VCC08AL23
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
CSI2_MSVDD0P8
CSI3_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLLDDR0
PLDVDD08_PLLDDR1
PLDVDD08_PILLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

1.1 V
DDR0_VDDQ
DDR1_VDDQ

0.6 V / 1.1 V
DDR0_VDDQLP
DDR1_VDDQLP

1.8 V
VDD1833_PRE18_SD0
VDD1833_PRE18_SD1
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
USB31_USVPH
USB31_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
PCIE_VCC18AL23
VDD1833_PRE18_ET0
VDD1833_PRE18_ET1
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLLDDR0
PLVDD_PLLDDR1
PLVDD_PILLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA
DDR1_VAA

3.3 V
USB20_USVDD33
USB21_USVDD33
USB30_USVDD33
USB31_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

(or 3rd Grp)
1.8 V / 3.3 V
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

(or 1st Grp or 3rd Grp)
3.3 V
VDD33_OTHERS

1.8 V
ADAVDD18
OTPVDD18

3rd Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18
CSI2_MSVDD18
CSI3_MSVDD18

4th Grp power supply

1.2 V
DSI_VDD12

Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ±5 ms).

Note 2. – TS0DVDD08A, TS0AVDD18: Min. 10 μs
– TS1DVDD08A, TS1AVDD18: Min. 10 μs

Note: The fall time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-7 Power-Off Sequence (CA55 Boot Mode)

3.4 DC Characteristics

3.4.1 Maximum Supply Current

Conditions for the supply current: Power supply voltage = Max. value, Tj = -40 to 125°C

Table 3.4-1 Max. Supply Currents during Operation (1/3)

Unit Name	Item	Symbol	Max.	Unit	Note
CA55	0.8-V (or 0.9-V) power supply current	I _{DD09_CA55}	3031	mA	VDD09_CA55
PD_OTHERS	0.8-V core power supply current	I _{DD08_OTHERS}	14449	mA	VDD08_OTHERS
	3.3-V core power supply current	I _{DD33_OTHERS}	1	mA	VDD33_OTHERS
	Pre-driver power supply current	I _{DD33PRE18_OTHERS}	1	mA	VDD33_PRE18_OTHERS
	Group A I/O power supply current	I _{DD1833_OTHERSA}	26	mA	VDD1833_OTHERS_A
	Group A pre-driver power supply current	I _{DD1833PRE18_OTHERSA}	4	mA	VDD1833_PRE18_OTHERS_A
	Group B I/O power supply current	I _{DD1833_OTHERSB}	26	mA	VDD1833_OTHERS_B
	Group B pre-driver power supply current	I _{DD1833PRE18_OTHERSB}	3	mA	VDD1833_PRE18_OTHERS_B
	Group C I/O power supply current	I _{DD1833_OTHERSC}	26	mA	VDD1833_OTHERS_C
	Group C pre-driver power supply current	I _{DD1833PRE18_OTHERSC}	4	mA	VDD1833_PRE18_OTHERS_C
	Group D I/O power supply current	I _{DD1833_OTHERSD}	13	mA	VDD1833_OTHERS_D
	Group D pre-driver power supply current	I _{DD1833PRE18_OTHERSD}	3	mA	VDD1833_PRE18_OTHERS_D
PD_AWO	0.8-V core power supply current	I _{DD08_AWO}	322	mA	VDD08_AWO
	1.8-V core power supply current	I _{DD18_AWO}	1	mA	VDD18_AWO
	I/O power supply current	I _{DD1833_AWO}	9	mA	VDD1833_AWO
	Pre-driver power supply current	I _{DD1833PRE18_AWO}	2	mA	VDD1833_PRE18_AWO
USB30	1.8-V PHY power supply current	I _{DDUSB30_USVPH}	31	mA	USB30_USVPH
	0.8-V PHY power supply current	I _{DDUSB30_USVPTX}	53	mA	USB30_USVPTX
	3.3-V PHY power supply current	I _{DDUSB30_USVDD33}	12	mA	USB30_USVDD33
	1.8-V PHY power supply current	I _{DDUSB30_USVDD18}	56	mA	USB30_USVDD18
	0.8-V PHY power supply current	I _{DDUSB30_USDVDD}	16	mA	USB30_USDVDD
USB31	1.8-V PHY power supply current	I _{DDUSB31_USVPH}	31	mA	USB31_USVPH
	0.8-V PHY power supply current	I _{DDUSB31_USVPTX}	53	mA	USB31_USVPTX
	3.3-V PHY power supply current	I _{DDUSB31_USVDD33}	12	mA	USB31_USVDD33
	1.8-V PHY power supply current	I _{DDUSB31_USVDD18}	56	mA	USB31_USVDD18
	0.8-V PHY power supply current	I _{DDUSB31_USDVDD}	16	mA	USB31_USDVDD
USB20	3.3-V PHY power supply current	I _{DDUSB20_USVDD33}	12	mA	USB20_USVDD33
	1.8-V PHY power supply current	I _{DDUSB20_USVDD18}	56	mA	USB20_USVDD18
	0.8-V PHY power supply current	I _{DDUSB20_USDVDD}	16	mA	USB20_USDVDD
USB21	3.3-V PHY power supply current	I _{DDUSB21_USVDD33}	12	mA	USB21_USVDD33
	1.8-V PHY power supply current	I _{DDUSB21_USVDD18}	56	mA	USB21_USVDD18
	0.8-V PHY power supply current	I _{DDUSB21_USDVDD}	16	mA	USB21_USDVDD
TSU0	1.8-V power supply current	I _{DDTS0AVDD18}	1	mA	TS0AVDD18
	0.8-V power supply current	I _{DDTS0DVDD08A}	1	mA	TS0DVDD08A
TSU1	1.8-V power supply current	I _{DDTS1AVDD18}	1	mA	TS1AVDD18
	0.8-V power supply current	I _{DDTS1DVDD08A}	1	mA	TS1DVDD08A

Table 3.4-1 Max. Supply Currents during Operation (2/3)

Unit Name	Item	Symbol	Max.	Unit	Note
xSPI	I/O power supply current	I _{DD1833_XSPI}	16	mA	VDD1833_XSPI
	Pre-driver power supply current	I _{DD1833PRE18_XSPI}	4	mA	VDD1833_PRE18_XSPI
SD0	I/O power supply current	I _{DD1833_SD0}	16	mA	VDD1833_SD0
	Pre-driver power supply current	I _{DD1833PRE18_SD0}	2	mA	VDD1833_PRE18_SD0
SD1	I/O power supply current	I _{DD1833_SD1}	10	mA	VDD1833_SD1
	Pre-driver power supply current	I _{DD1833PRE18_SD1}	1	mA	VDD1833_PRE18_SD1
SD2	I/O power supply current	I _{DD1833_SD2}	10	mA	VDD1833_SD2
	Pre-driver power supply current	I _{DD1833PRE18_SD2}	2	mA	VDD1833_PRE18_SD2
OTP	1.8-V power supply current	I _{DDOTPVD18}	6	mA	OTPVDD18
DDR0	0.8-V core power supply current	I _{DD08_DDR}	934	mA	VDD08_DDR
	1.1-V PHY power supply current	I _{DDQ_DDR0}	760	mA	DDR0_VDDQ
	PHY power supply current	I _{DDQLP_DDR0}	242	mA	DDR0_VDDQLP
	1.8-V PLL power supply current	I _{DDVAA_DDR0}	5	mA	DDR0_VAA
DDR1	0.8-V core power supply current	I _{DD08_DDR}	934	mA	VDD08_DDR
	1.1-V PHY power supply current	I _{DDQ_DDR1}	760	mA	DDR1_VDDQ
	PHY power supply current	I _{DDQLP_DDR1}	242	mA	DDR1_VDDQLP
	1.8-V PLL power supply current	I _{DDVAA_DDR1}	5	mA	DDR1_VAA
GBETH0	I/O power supply current	I _{DD1833_ET0}	12	mA	VDD1833_ET0
	Pre-driver power supply current	I _{DD1833PRE18_ET0}	2	mA	VDD1833_PRE18_ET0
GBETH1	I/O power supply current	I _{DD1833_ET1}	12	mA	VDD1833_ET1
	Pre-driver power supply current	I _{DD1833PRE18_ET1}	2	mA	VDD1833_PRE18_ET1
CRU0	1.8-V PHY power supply current	I _{DDMSVDD18_CSI0}	8	mA	CSI0_MSVDD18
	0.8-V core power supply current	I _{DDMSVDD0P8_CSI0}	25	mA	CSI0_MSVDD0P8
CRU1	1.8-V PHY power supply current	I _{DDMSVDD18_CSI1}	8	mA	CSI1_MSVDD18
	0.8-V core power supply current	I _{DDMSVDD0P8_CSI1}	25	mA	CSI1_MSVDD0P8
CRU2	1.8-V PHY power supply current	I _{DDMSVDD18_CSI2}	8	mA	CSI2_MSVDD18
	0.8-V core power supply current	I _{DDMSVDD0P8_CSI2}	25	mA	CSI2_MSVDD0P8
CRU3	1.8-V PHY power supply current	I _{DDMSVDD18_CSI3}	8	mA	CSI3_MSVDD18
	0.8-V core power supply current	I _{DDMSVDD0P8_CSI3}	25	mA	CSI3_MSVDD0P8
DSI	0.8-V core power supply current	I _{DD0P8_DSI}	43	mA	DSI_VDD0P8
	1.2-V PHY power supply current	I _{DD12_DSI}	1	mA	DSI_VDD12
	1.8-V PHY power supply current	I _{DD18_DSI}	8	mA	DSI_VDD18
PCIE	1.8-V power supply current	I _{DDPCIEVCC18ACMN}	19	mA	PCIE_VCC18ACMN
	1.8-V PHY power supply current	I _{DDPCIEVCC18AL01}	53	mA	PCIE_VCC18AL01
	1.8-V PHY power supply current	I _{DDPCIEVCC18AL23}	53	mA	PCIE_VCC18AL23
	0.8-V PHY power supply current	I _{DDPCIEVCC08AL01}	112	mA	PCIE_VCC08AL01
	0.8-V PHY power supply current	I _{DDPCIEVCC08AL23}	112	mA	PCIE_VCC08AL23
I3C	I/O power supply current	I _{DD1218_I3C}	1	mA	VDD1218_I3C
ADC	1.8-V analog power supply current	I _{DDADAVDD18}	1	mA	ADAVDD18

Table 3.4-1 Max. Supply Currents during Operation (3/3)

Unit Name	Item	Symbol	Max.	Unit	Note
CPG	PLLCM33 1.8-V power supply current	$I_{DDPLVDD_PLLCM33}$	2	mA	PLVDD_PLLCM33
	PLLCLN_DTY_DRP 1.8-V power supply current	$I_{DDPLVDD_PLLCLNDTYDRP}$	6	mA	PLVDD_PLLCLN_DTY_DRP
	PLLCA55 1.8-V power supply current	$I_{DDPLVDD_PLLCA55}$	2	mA	PLVDD_PLLCA55
	PLLVDO_DSI 1.8-V power supply current	$I_{DDPLVDD_PLLVDO_DSI}$	4	mA	PLVDD_PLLVDO_DSI
	PLLDDR0 1.8-V power supply current	$I_{DDPLVDD_PLLDDR0}$	2	mA	PLVDD_PLLDDR0
	PLLDDR1 1.8-V power supply current	$I_{DDPLVDD_PLLDDR1}$	2	mA	PLVDD_PLLDDR1
	PLLETH_GPU 1.8-V power supply current	$I_{DDPLVDD_PLLETHGPU}$	4	mA	PLVDD_PLLETH_GPU
	PLLCM33 0.8-V power supply current	$I_{DDPLVDD08_PLLCM33}$	3	mA	PLDVDD08_PLLCM33
	PLLCLN_DTY_DRP 0.8-V power supply current	$I_{DDPLVDD08_PLLCLNDTYDRP}$	8	mA	PLDVDD08_PLLCLN_DTY_DRP
	PLLCA55 0.8-V (or 0.9-V) power supply current	$I_{DDPLVDD08_PLLCA55}$	3	mA	PLDVDD09_PLLCA55
	PLLVDO_DSI 0.8-V power supply current	$I_{DDPLVDD08_PLLVDO_DSI}$	5	mA	PLDVDD08_PLLVDO_DSI
	PLLDDR0 0.8-V power supply current	$I_{DDPLVDD08_PLLDDR0}$	3	mA	PLDVDD08_PLLDDR0
	PLLDDR1 0.8-V power supply current	$I_{DDPLVDD08_PLLDDR1}$	3	mA	PLDVDD08_PLLDDR1
	PLLETH_GPU 0.8-V power supply current	$I_{DDPLVDD08_PLLETHGPU}$	5	mA	PLDVDD08_PLLETH_GPU
CST	I/O power supply current	I_{DD1833_JTAG}	3	mA	VDD1833_JTAG
	Pre-driver power supply current	$I_{DD1833PRE18_JTAG}$	1	mA	VDD1833_PRE18_JTAG
PWC	1.8-V I/O power supply current	I_{DD18_PWC}	1	mA	VDD18_PWC

3.4.2 Standard I/O Characteristics

For the I/O types, refer to the external pin list in **Section 2.2.1, List of External Pins**.

Table 3.4-2 DC Characteristics

$V_{DD} = 1.14 \text{ V to } 1.89 \text{ V}$ (1.8/1.2-V switching I/O type), $V_{DD} = 1.71 \text{ V to } 1.89 \text{ V}$ (1.8-V I/O type and 1.8-V OSC I/O type), $V_{DD} = 1.71 \text{ V to } 3.46 \text{ V}$ (3.3/1.8-V switching I/O types 1, 2 and 3), $V_{DD} = 3.14 \text{ V to } 3.46 \text{ V}$ (3.3-V I/O type) (1/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
High-level input voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{IH}	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	—
	1.8/1.2-V switching I/O type (1.8 V)	V_{IH}	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	—
	1.8-V I/O type	V_{IH}	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	—
	1.8-V OSC I/O type						
	3.3/1.8-V switching I/O type 1						
	3.3/1.8-V switching I/O type 3						
	3.3-V I/O type						
	3.3/1.8-V switching I/O type 2	V_{IH}	$0.7 \times V_{DD}$	—	3.63	V	—
Low-level input voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{IL}	-0.3	—	$0.2 \times V_{DD}$	V	—
	1.8/1.2-V switching I/O type (1.8 V)	V_{IL}	-0.3	—	$0.3 \times V_{DD}$	V	—
	1.8-V I/O type	V_{IL}	-0.3	—	$0.3 \times V_{DD}$	V	—
	1.8-V OSC I/O type						
	3.3/1.8-V switching I/O type 1						
	3.3/1.8-V switching I/O type 2						
	3.3/1.8-V switching I/O type 3						
	3.3-V I/O type						
Hysteresis voltage	1.8/1.2-V switching I/O type	ΔV	$0.1 \times V_{DD}$	—	—	V	—
	1.8-V I/O type						
	3.3/1.8-V switching I/O type 1* ¹	ΔV	$0.08 \times V_{DD}$	—	—	V	—
	3.3/1.8-V switching I/O type 2* ²						
	3.3/1.8-V switching I/O type 3* ¹³	ΔV	0.1	—	—	V	—

Table 3.4-2 DC Characteristics

$V_{DD} = 1.11\text{ V to }1.95\text{ V}$ (1.8/1.2-V switching I/O type), $V_{DD} = 1.65\text{ V to }1.95\text{ V}$ (1.8-V I/O type and 1.8-V OSC I/O type), $V_{DD} = 1.65\text{ V to }3.60\text{ V}$ (3.3/1.8-V switching I/O types 1, 2 and 3), $V_{DD} = 3.00\text{ V to }3.60\text{ V}$ (3.3-V I/O type) (2/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
Input leakage current	1.8/1.2-V switching I/O type (1.2 V)	I_I	-10	—	10	μA	$V_{in} = V_{SS}$ or V_{DD} max & V_{DD} power-on
			-10	—	10	μA	$V_{in} = V_{SS}$ or V_{DD} max & V_{DD} power-off
	1.8/1.2-V switching I/O type (1.8 V)	I_I	-15	—	15	μA	$V_{in} = V_{DD}$ max & V_{DD} power-on
			-18	—	18	μA	$V_{in} = V_{SS}$ or V_{DD} max & V_{DD} power-off
	1.8-V I/O type	I_I	-12	—	12	μA	$V_{in} = V_{DD}$ max & V_{DD} power-on
	1.8-V OSC I/O type						
	3.3/1.8-V switching I/O type 1	I_I	-12	—	12	μA	$V_{in} = V_{DD}$ max & V_{DD} power-on
	3.3/1.8-V switching I/O type 2					μA	$V_{in} = V_{SS}$ or V_{DD} max & V_{DD} power-off
	3.3/1.8-V switching I/O type 3					μA	$V_{in} = V_{DD}$ max & V_{DD} power-on
	3.3-V I/O type	I_{RPD}	10	—	100	μA	$V_{in} = V_{DD}$ max
	1.8/1.2-V switching I/O type* ³						
	1.8/1.2-V switching I/O type* ³ (1.8 V)						
	1.8-V I/O type* ⁵						
	3.3/1.8-V switching I/O type 1* ⁷						
Input pull-down resistor current	3.3/1.8-V switching I/O type 2* ⁹	I_{RPD}	25	—	200	μA	$V_{in} = V_{DD}$ max
	3.3/1.8-V switching I/O type 3* ¹¹						
	1.8/1.2-V switching I/O type* ⁴ (1.2 V)	I_{RPU}	-10	—	-100	μA	$V_{in} = V_{SS}$
	1.8/1.2-V switching I/O type* ⁴ (1.8 V)						
	1.8-V I/O type* ⁶	I_{RPU}	-35	—	-185	μA	$V_{in} = V_{SS}$
	3.3/1.8-V switching I/O type 1* ⁸						
	3.3/1.8-V switching I/O type 2* ¹⁰	I_{RPU}	-25	—	-200	μA	$V_{in} = V_{SS}$
	3.3/1.8-V switching I/O type 3* ¹²						
		I_{RPU}	-18	—	-192	μA	$V_{in} = V_{SS}$

Table 3.4-2 DC Characteristics

$V_{DD} = 1.11\text{ V}$ to 1.95 V (1.8/1.2-V switching I/O type), $V_{DD} = 1.65\text{ V}$ to 1.95 V (1.8-V I/O type and 1.8-V OSC I/O type), $V_{DD} = 1.65\text{ V}$ to 3.60 V (3.3/1.8-V switching I/O types 1, 2 and 3), $V_{DD} = 3.00\text{ V}$ to 3.60 V (3.3-V I/O type) (3/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
High-level output voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -1/-2/-4/-6\text{ mA}$ (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.8 V)	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -2/-4/-8/-12\text{ mA}$ (drive strength X1/X2/X4/X6)
	1.8-V I/O type 1.8-V OSC I/O type	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -2/-4/-8/-12\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (1.8 V) 3.3/1.8-V switching I/O type 2 (1.8V)	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -1.6/-3.2/-6.4/-9.6\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (3.3 V) 3.3/1.8-V switching I/O type 2 (3.3V)	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -2/-4/-8/-12\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (1.8 V)	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -5/-6/-7/-10\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (3.3 V)	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -9/-11/-13/-18\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3-V I/O type	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -2/-4/-8/-12\text{ mA}$ (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.2 V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 1/2/4/6\text{ mA}$ (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.8 V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12\text{ mA}$ (drive strength X1/X2/X4/X6)
Low-level output voltage	1.8-V I/O type 1.8-V OSC I/O type	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (1.8 V) 3.3/1.8-V switching I/O type 2 (1.8V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 1.6/3.2/6.4/9.6\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (3.3 V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 2 (3.3 V)	V_{OL1}	0	—	0.4	V	$I_{OL} = 1.7/3.3/6.5/9.8\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (1.8 V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 5/6/7/10\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (3.3 V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 9/11/13/18\text{ mA}$ (drive strength X1/X2/X4/X6)
	3.3-V I/O type	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12\text{ mA}$ (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.2 V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 1/2/4/6\text{ mA}$ (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.8 V)	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12\text{ mA}$ (drive strength X1/X2/X4/X6)
	1.8-V I/O type 1.8-V OSC I/O type	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12\text{ mA}$ (drive strength X1/X2/X4/X6)

Table 3.4-2 DC Characteristics

$V_{DD} = 1.11\text{ V}$ to 1.95 V (1.8/1.2-V switching I/O type), $V_{DD} = 1.65\text{ V}$ to 1.95 V (1.8-V I/O type and 1.8-V OSC I/O type), $V_{DD} = 1.65\text{ V}$ to 3.60 V (3.3/1.8-V switching I/O types 1, 2 and 3), $V_{DD} = 3.00\text{ V}$ to 3.60 V (3.3-V I/O type) (4/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
Pull-up resistance	1.8/1.2-V switching I/O type* ⁴ (1.2 V)	R_{PU}	15	—	160	k Ω	—
	1.8/1.2-V switching I/O type* ⁴ (1.8 V)	R_{PU}	10	—	50	k Ω	—
	1.8-V I/O type* ⁶	R_{PU}	10	—	50	k Ω	—
	3.3/1.8-V switching I/O type 1* ⁸ (1.8 V)	R_{PU}	10	—	50	k Ω	—
	3.3/1.8-V switching I/O type 2* ¹⁰ (1.8 V)						
	3.3/1.8-V switching I/O type 1* ⁸ (3.3 V)	R_{PU}	10	—	100	k Ω	—
	3.3/1.8-V switching I/O type 2* ¹⁰ (3.3 V)						
	3.3/1.8-V switching I/O type 3* ¹²	R_{PU}	12	—	92	k Ω	—
Pull-down resistance	1.8/1.2-V switching I/O type* ³ (1.2 V)	R_{PD}	15	—	160	k Ω	—
	1.8/1.2-V switching I/O type* ³ (1.8 V)	R_{PD}	15	—	60	k Ω	—
	1.8-V I/O type* ⁵	R_{PD}	15	—	60	k Ω	—
	3.3/1.8-V switching I/O type 1* ⁷ (1.8 V)	R_{PD}	10	—	50	k Ω	—
	3.3/1.8-V switching I/O type 2* ⁹ (1.8 V)						
	3.3/1.8-V switching I/O type 1* ⁷ (3.3 V)	R_{PD}	10	—	100	k Ω	—
	3.3/1.8-V switching I/O type 2* ⁹ (3.3 V)						
	3.3/1.8-V switching I/O type 3* ¹¹	R_{PD}	13	—	92	k Ω	—
Input capacitance	—	C_{in}	—	—	10	pF	—

Note 1. Only for the TRSTN pin

Note 2. When the RIIC function is in use or the schmitt control is on

Note 3. Only for the P20 and P21 pins (when the internal pull-down is enabled)

Note 4. Only for the P20 and P21 pins (when the internal pull-up is enabled)

Note 5. Only for the QBYPASS, BSCANP, MD_BOOT0, MD_BOOT3, MD_BOOT4, BOOTSELCPU, and BOOTPLLCA0 pins

Note 6. Only for the MD_BOOT1, MD_BOOT2, BOOTPLLCA1, and MD_CLKS pins

Note 7. Only for the WDTUDFCA, WDTUDFCM, and SCIF_RXD, SCIF_TXD, XSPI0_CS0N, XSPI0_RESET0N, XSPI0_RST00N, XSPI0_INT0N, and XSPI0_ECS0N pins (when the internal pull-down is enabled)

Note 8. Only for the WDTUDFCA, WDTUDFCM, and SCIF_RXD, SCIF_TXD, XSPI0_CS0N, XSPI0_RESET0N, XSPI0_RST00N, XSPI0_INT0N, and XSPI0_ECS0N pins (when the internal pull-up is enabled)

Note 9. When the internal pull-down is enabled

Note 10. When the internal pull-up is enabled

Note 11. Only for the pins other than SD0CLK, SD0RSTN, SD1CLK, ET0_PHYINTR, and ET1_PHYINTR (when the internal pull-down is enabled)

Note 12. Only for the pins other than SD0CLK, SD0RSTN, SD1CLK, ET0_PHYINTR, and ET1_PHYINTR (when the internal pull-up is enabled)

Note 13. Only for the P90, P91, P92, PB0, PB1, PB2, PB3, PB4, and PB5 pins (when the RIIC function is in use or the schmitt control is on)

3.5 AC Characteristics

Conditions:

VDD18 = VDD18_AWO = VDD1833_* (1.8 V mode)

VDD33 = VDD1833_* (3.3 V mode)

3.5.1 Clock Timing

Table 3.5-1 Clock Timing Table

Item	Symbol	Min.	Max.	Unit	Figures
QEXTAL clock input frequency	f _{EX}	24 -50 ppm	24 +50 ppm	MHz	Figure 3.5-1
QEXTAL clock input cycle time	t _{EXcyc}	41.67	41.67	ns	
AUDIO_EXTAL clock input frequency	f _{EX}	4	48	MHz	
AUDIO_EXTAL clock input cycle time	t _{EXcyc}	20.83	250	ns	
AUDIO_CLKB, AUDIO_CLKC clock input frequency (external clock is input)	f _{EX}	4	50	MHz	
AUDIO_CLKB, AUDIO_CLKC clock input cycle time (external clock is input)	t _{EXcyc}	20	250	ns	
QEXTAL clock input low-level pulse width	t _{EXL}	0.4	0.6	t _{EXcyc}	
QEXTAL clock input high-level pulse width	t _{EXH}	0.4	0.6	t _{EXcyc}	
AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input low-level pulse width	t _{EXL}	0.45	0.55	t _{EXcyc}	
AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input high-level pulse width	t _{EXH}	0.45	0.55	t _{EXcyc}	
QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input rise time	t _{EXr}	—	4	ns	
QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input fall time	t _{EXf}	—	4	ns	
Oscillation stabilization time	T	*1	—	ms	Figure 3.5-2
QEXTAL stable clock input to QRESN rise	t _{STCKRST}	1	—	μs	
Mode hold time	t _{MDH}	100	—	ns	
Mode setup time	t _{MDS}	100	—	ns	

Note 1. The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by a crystal resonator matching test. For details of the stabilization time "T", please contact the crystal manufacturer.

When USB3, MIPI DSI, or USB2 is used, the jitter of the external clock should be less than the values in the table below. On the other hand, when USB3, MIPI DSI, or USB2 is not used, the jitter of the external clock should be less than 80 ps.

Table 3.5-2 QEXTAL Input Clock Jitter Table

Module	Max.	Max.	Unit	Condition
USB3	Reference clock random jitter	2.17	ps, rms	Integrated value from 12 kHz to 20 MHz
		1.57	ps, rms	Integrated value from 2 MHz to 20 MHz
MIPI DSI	Reference clock deterministic jitter	40	ps, pp	
USB2	Reference clock deterministic jitter	40	ps, pp	
Others	Reference clock deterministic jitter	80	ps, pp	

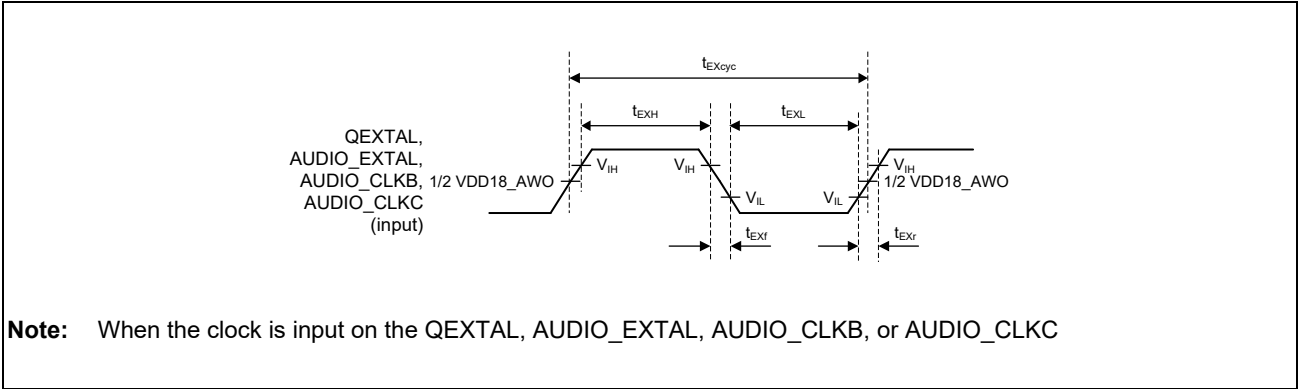


Figure 3.5-1 Clock Input Timing

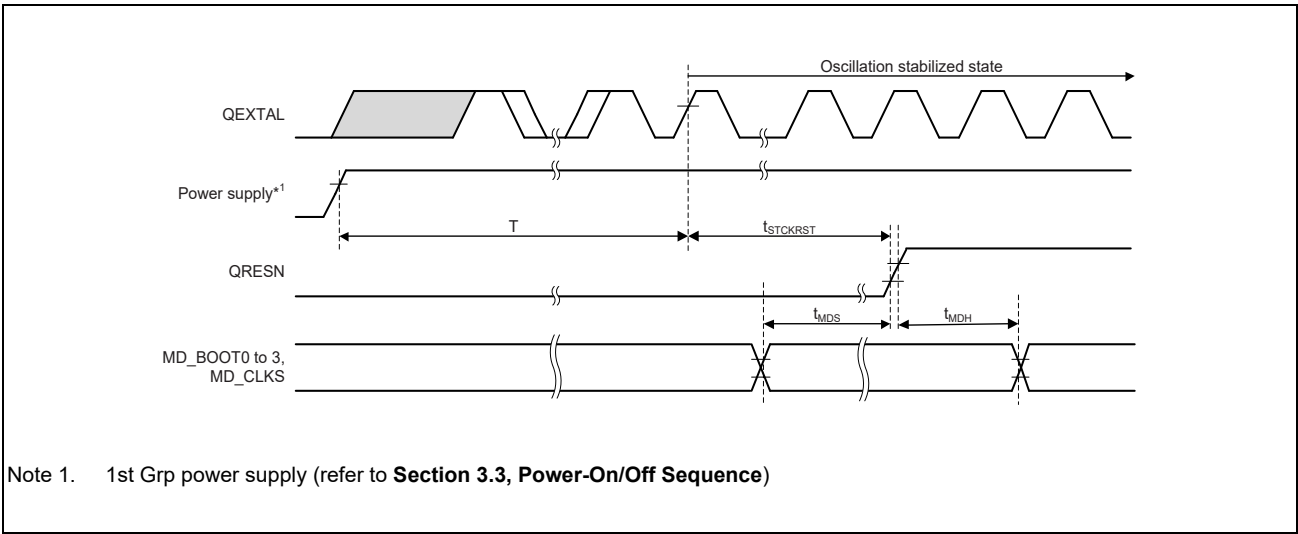


Figure 3.5-2 Power-On Oscillation Settling Time

3.5.2 CMTW Timing

Table 3.5-3 CMTW Timing

Parameter		Symbol	Min.	Max.	Unit	Figure
CMTW	Input capture input pulse width	Single-edge setting	t_{CMTWICW}	1.5	—	Figure 3.5-3
		Both-edge setting		2.5	—	

Note 1. t_{PLoc} : PCLKL cycle

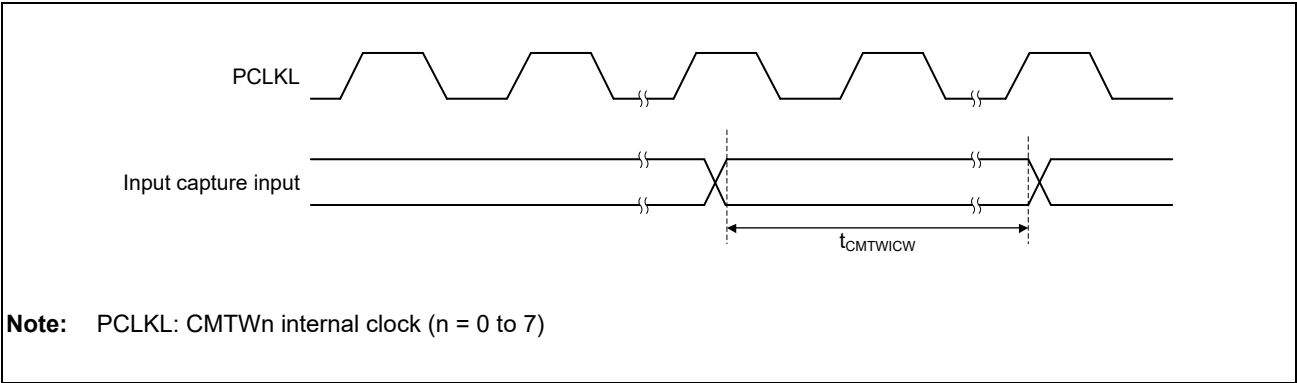


Figure 3.5-3 CMTW Input Capture Input Timing

3.5.3 POEG and GPT Trigger Timings

GPT Conditions: High-drive output is selected in the PFC register.

Table 3.5-4 POEG and GPT Trigger Timings

Parameter		Symbol	Min.	Max.	Unit	Figure
POEG	POEG input trigger pulse width	t_{POEW}	1.5	—	t_{Pcyc}^{*1}	Figure 3.5-4
GPT	Input capture pulse width	Single edge	1.5	—	t_{PDcyc}^{*2}	Figure 3.5-5
		Dual edge	2.5	—		

Note 1. t_{Pcyc} : POEGnx internal clock cycle (x = A to D, n = 0, 1)

Note 2. t_{PDcyc} : GPTn internal clock cycle (n = 0, 1)

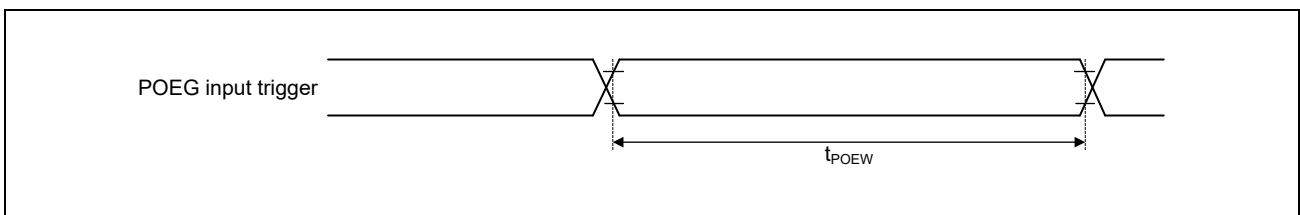


Figure 3.5-4 POEG Input Trigger Timing

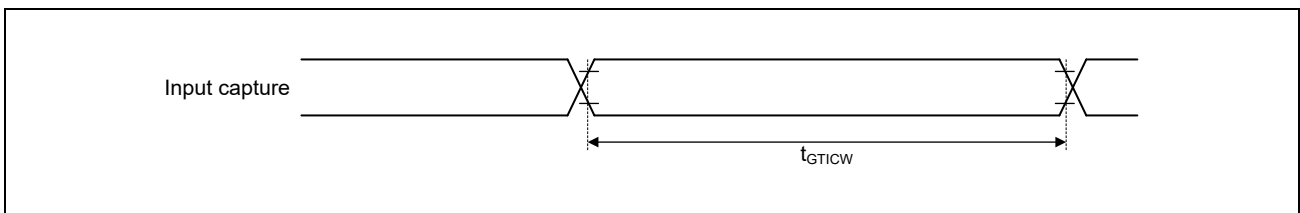


Figure 3.5-5 GPT Input Capture Timing

3.5.4 Watchdog Timer Access Timing

Table 3.5-5 Watchdog Timer Timing

Item	Symbol	Min.	Max.	Unit	Figures
WDTUDFCM / WDTUDFCA output time	t_L	64	64	t_{P1cyc}^{*1}	Figure 3.5-6

Note 1. t_{P1cyc} indicates WDTn loco clock (n = 0 to 3).

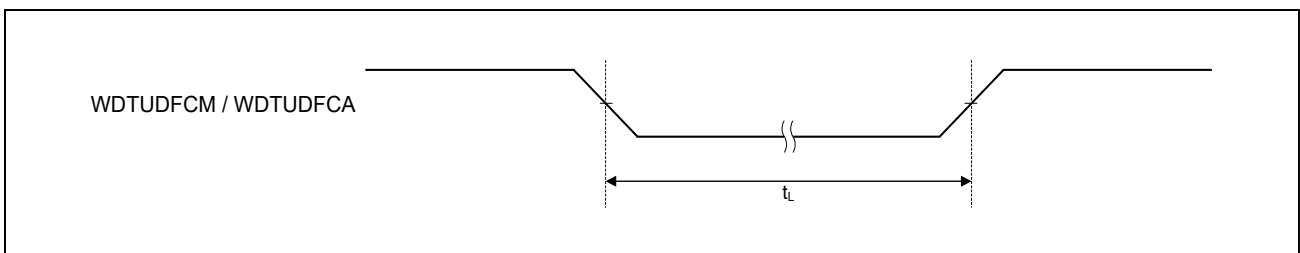


Figure 3.5-6 Watchdog Timer Output Timing

3.5.5 DMAC Timing

Table 3.5-6 DMAC Timing

Item	Symbol	Min.	Max.	Unit	Figures
DREQn pulse width	t_{DREQW}	20	—	t_{cyc}^{*1}	Figure 3.5-7
TENDn pulse width	t_{TENDW}	16	16	$t_{PCLKcyc}^{*2}$	Figure 3.5-8

Note 1. $t_{cyc} = 41.666 \text{ ns}$ (24 MHz)

Note 2. $t_{PCLKcyc} = 10 \text{ ns}$ (100 MHz)

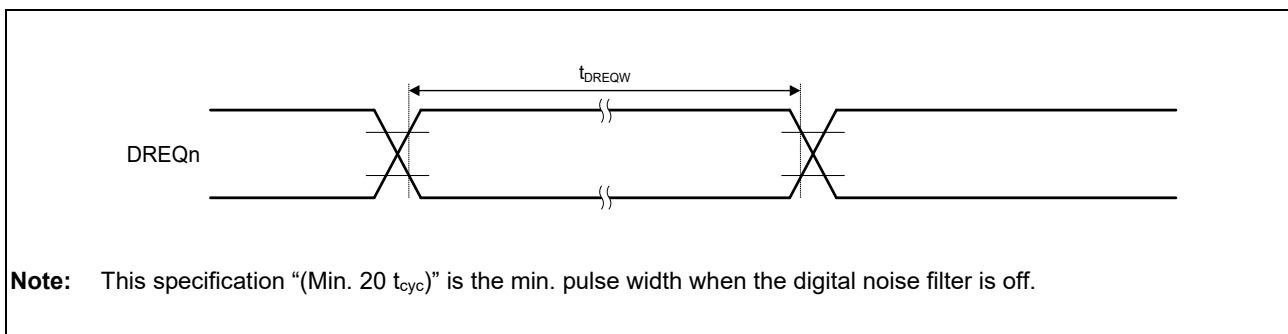


Figure 3.5-7 DMAC DREQn Timing

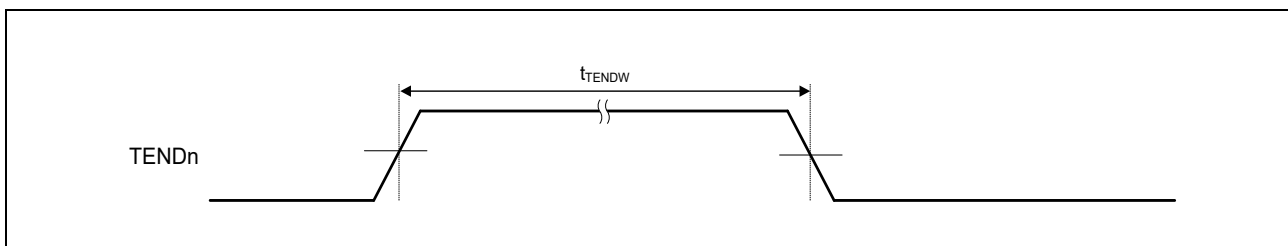


Figure 3.5-8 DMAC TENDn Timing

3.5.6 LPDDR4 PHY Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4D / JEDEC 209-4-1A standard.

3.5.7 SD Access Timing

Conditions:

$$V_{OH} = VDD33 \times 0.7$$

$$V_{OL} = VDD33 \times 0.3$$

$$C = 40 \text{ pF (3.3 V)}$$

Drive strength: $\times 6$

3.5.7.1 SD Access Timing (SDR 3.3-V)

Table 3.5-7 SD AC Access Timing (SDR at 3.3-V Operation)

Item	Symbol	Default Speed Mode (25 MHz)		High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.	Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	40.0	—	20.0	—	ns	Figure 3.5-9
SDnCLK clock high level width	t_{SDWH}	10	—	7	—	ns	
SDnCLK clock low level width	t_{SDWL}	10	—	7	—	ns	
SDnCLK clock rise time	t_{SDLH}	—	10	—	3	ns	
SDnCLK clock fall time	t_{SDHL}	—	10	—	3	ns	
SDnCMD,SDnDATm output delay	t_{SDODLY}	-7.5	2.5	-6.2	2.5	ns	
SDnCMD,SDnDATm input set up time	t_{SDIS}	4.0	—	4.0	—	ns	
SDnCMD,SDnDATm input hold time	t_{SDIH}	2.0	—	2.0	—	ns	
SDnCMD,SDnDATm input data width	t_{SDIDW}	—	—	—	—	ns	

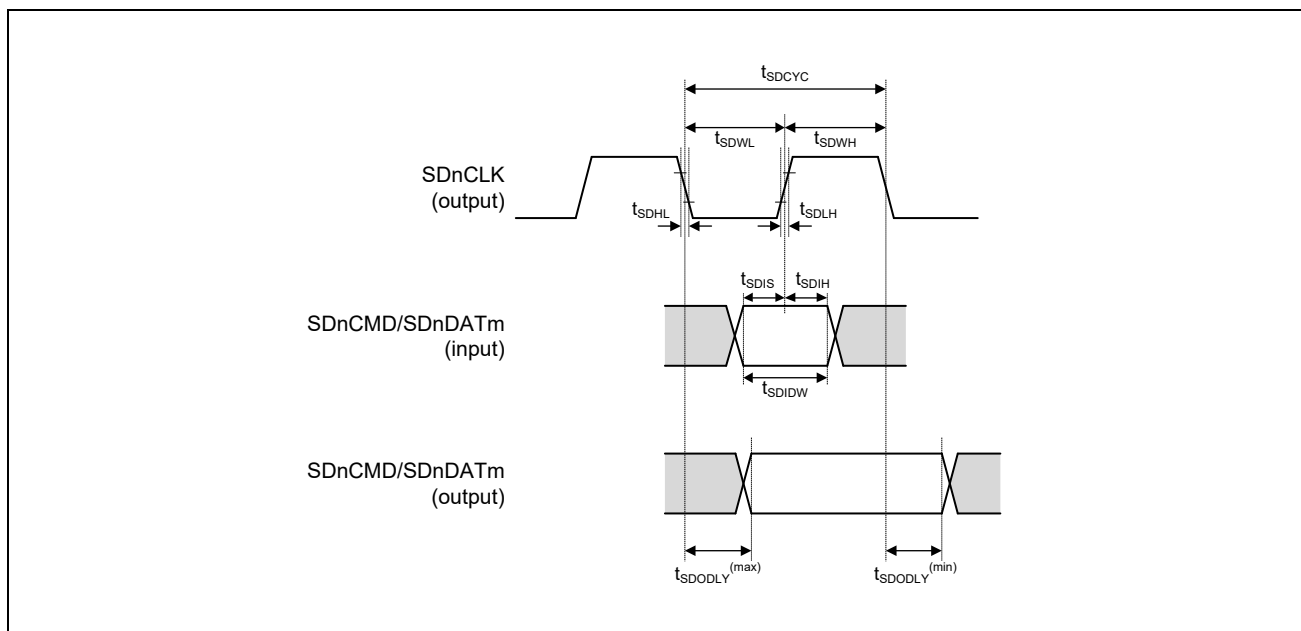


Figure 3.5-9 SDHC Interface Timing (SDR 3.3-V Power Supply)

NOTE

The disclosure of other characteristics of the SD interface needs the conclusion of the following agreement.

- SD Host/Ancillary Product License Agreement (SD HALA)

For details, contact Renesas sales representatives.

3.5.8 eMMC Access Timing

Conditions:

$$V_{OH} = V_{DD18} \times 0.7, V_{OL} = V_{DD18} \times 0.3, C = 15 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{DD33} \times 0.7, V_{OL} = V_{DD33} \times 0.3, C = 30 \text{ pF (3.3 V)}$$

Drive strength: $\times 6$

3.5.8.1 eMMC host interface timing (default)

Table 3.5-8 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	20.0	—	ns	Figure 3.5-10
SDnCLK clock high level width	t_{MMCWH}	7	—	ns	
SDnCLK clock low level width	t_{MMCWL}	7	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3	ns	
SDnCMD/SDnDATm output delay	t_{MMCODY}	-6.2	2.5	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	4.0	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	2.0	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	—	—	ns	

Table 3.5-9 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	20.0	—	ns	Figure 3.5-10
SDnCLK clock high level width	t_{MMCWH}	7	—	ns	
SDnCLK clock low level width	t_{MMCWL}	7	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3	ns	
SDnCMD/SDnDATm output delay	t_{MMCODY}	-4.2	1.6	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	1.3	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	1.878	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	—	—	ns	

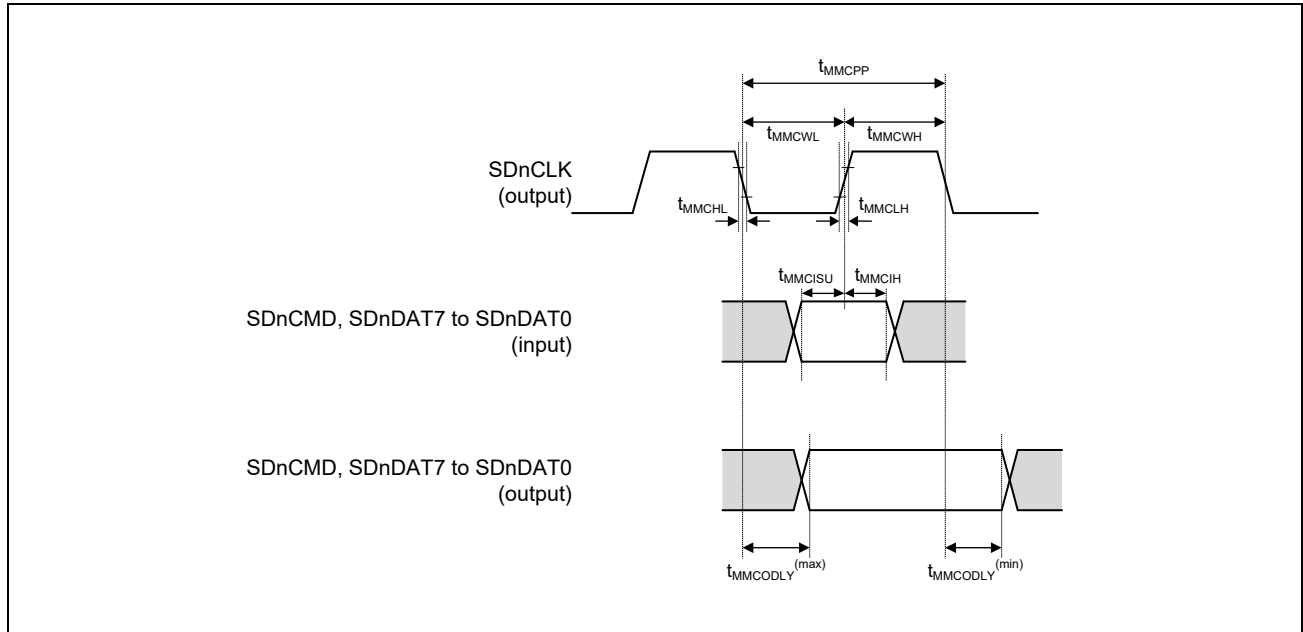


Figure 3.5-10 eMMC Host Interface Timing (MMC Default 1.8-V/3.3-V Power Supply)

3.5.8.2 eMMC host interface timing (HS-SDR)

NOTES

1. The spec of eMMC host interface timing (HS-SDR 3.3-V power supply) is the same as **Table 3.5-8, eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)**.
2. The spec of eMMC host interface timing (HS-SDR 1.8V power supply) is the same as **Table 3.5-9, eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)**.

3.5.8.3 eMMC host interface timing (HS-DDR)

Table 3.5-10 eMMC Host Interface Timing (HS-DDR 3.3-V Power Supply Operation)

Item	Symbol	High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	20.0	—	ns	Figure 3.5-11
SDnCLK clock high level width	t_{SDWH}	9.0	11.0	ns	
SDnCLK clock low level width	t_{SDWL}	9.0	11.0	ns	
SDnCLK clock rise time	t_{SDLH}	—	3.0	ns	
SDnCLK clock fall time	t_{SDHL}	—	3.0	ns	
SDnCMD output delay	t_{SDODLY}	-6.0	6.0	ns	
SDnCMD input set up time	t_{SDIS}	4.8	—	ns	
SDnCMD input hold time	t_{SDIH}	2.5	—	ns	
SDnDATm output delay	t_{SDODLY_DDR}	2.5	6.5	ns	
SDnDATm input set up time	t_{SDIS_DDR}	1.768	—	ns	
SDnDATm input hold time	t_{SDIH_DDR}	1.5	—	ns	

Table 3.5-11 eMMC Host Interface Timing (HS-DDR 1.8-V Power Supply Operation)

Item	Symbol	High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{MMCCYC}	20.0	—	ns	Figure 3.5-11
SDnCLK clock high level width	t_{MMCWH}	9.0	11.0	ns	
SDnCLK clock low level width	t_{MMCWL}	9.0	11.0	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3.0	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3.0	ns	
SDnCMD output delay	$t_{MMCODLY}$	-6.0	3.0	ns	
SDnCMD input set up time	t_{MMCIS}	4.8	—	ns	
SDnCMD input hold time	t_{MMCIH}	2.5	—	ns	
SDnDATm output delay	$t_{MMCODLY_DDR}$	2.5	6.5	ns	
SDnDATm input set up time	t_{MMCIS_DDR}	1.768	—	ns	
SDnDATm input hold time	t_{SMCIIH_DDR}	1.5	—	ns	

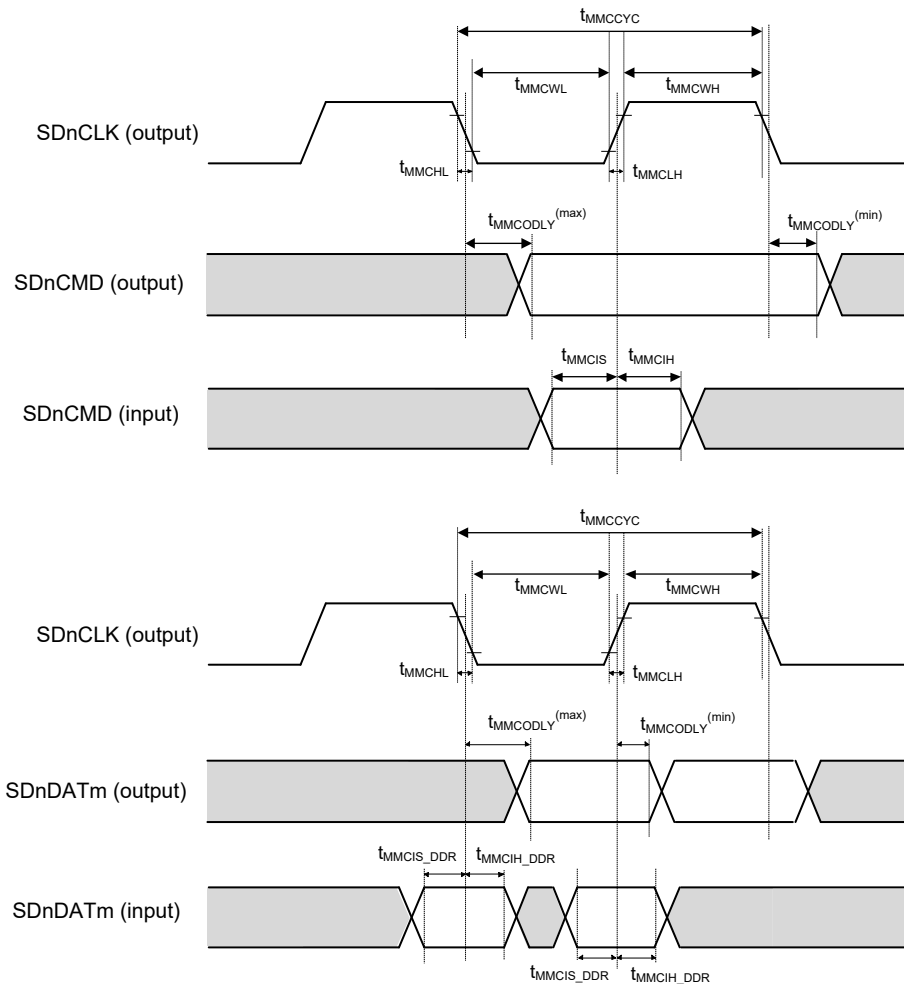


Figure 3.5-11 eMMC Host Interface (MMC Interface HS-DDR Mode 1.8/3.3-V Power Supply Selection)

3.5.8.4 eMMC host interface timing (HS200)

Table 3.5-12 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	$t_{MMC\text{CPP}}$	5.0	10.0	ns	Figure 3.5-12
SDnCLK clock high level width	$t_{MMC\text{WH}}$	1.5	—	ns	
SDnCLK clock low level width	$t_{MMC\text{WL}}$	1.5	—	ns	
SDnCLK clock rise time	$t_{MMC\text{LH}}$	—	1.0	ns	
SDnCLK clock fall time	$t_{MMC\text{HL}}$	—	1.0	ns	
SDnCMD/SDnDATm output delay	$t_{MMC\text{ODLY}}$	-1.7	0.9	ns	
SDnCMD/SDnDATm input setup time	$t_{MMC\text{ISU}}$	—	—	ns	
SDnCMD/SDnDATm input hold time	$t_{MMC\text{IH}}$	—	—	ns	
SDnCMD/SDnDATm input data width	$t_{MMC\text{IDW}}$	2.88	—	ns	

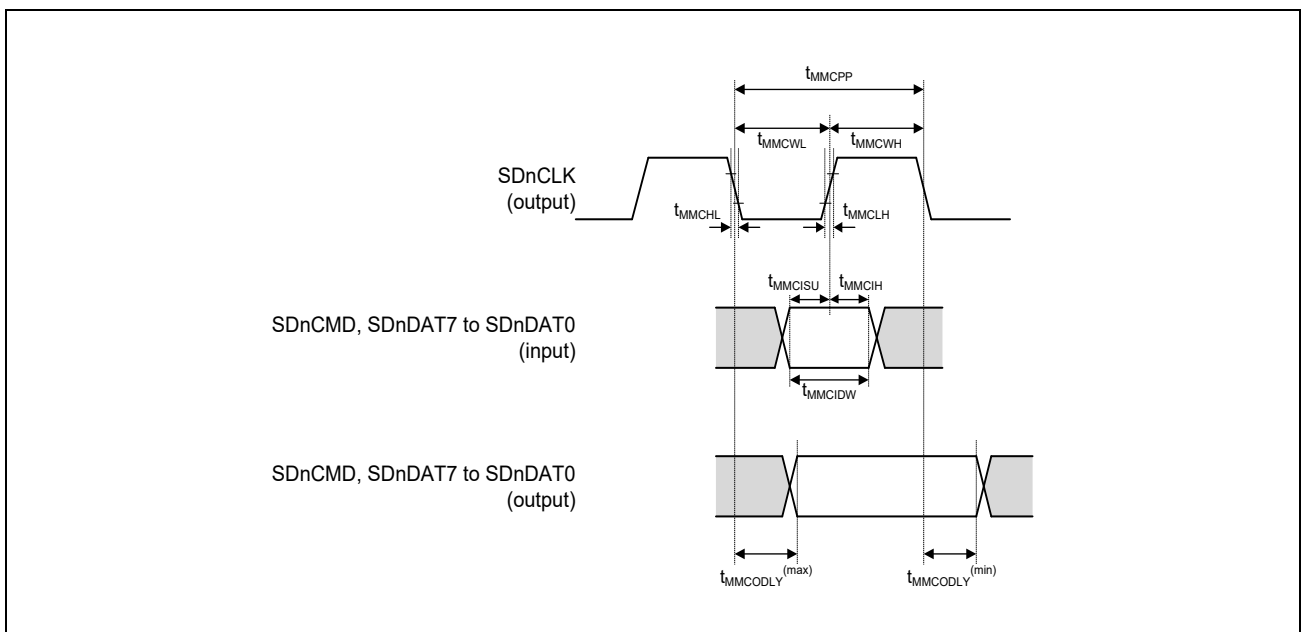


Figure 3.5-12 eMMC Host Interface (MMC Interface HS200 Mode 1.8-V Power Supply Selection)

3.5.9 Ethernet Interface Timing

Conditions:

$$V_{OH} = VDD18 \times 0.5, V_{OL} = VDD18 \times 0.5, C = 15 \text{ pF (RGMII)}$$

$$V_{OH} = VDD33 \times 0.5, V_{OL} = VDD33 \times 0.5, C = 30 \text{ pF (MII)}$$

Drive strength: $\times 2, \times 4$

Table 3.5-13 Ethernet Interface Timing (n = 0, 1)

Parameter			Symbol	Min.	Max.	Unit	Figure
Ethernet (RGMII)	ETn_TXC_TXCLK, ETn_RXC_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	Figure 3.5-13
		100 Mbps		36	44	ns	
		10 Mbps		360	440	ns	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK frequency	1 Gbps	—	125 – 50 ppm	125 + 50 ppm	MHz	
		100 Mbps		25 – 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 – 50 ppm	2.5 + 50 ppm	MHz	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK duty cycle	1 Gbps	—	45	55	%	
		100 Mbps		40	60	%	
		10 Mbps					
	ETn_TXC_TXCLK, ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_RXC_RXCLK, ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV rise/fall time		t_{RGMIIr}, t_{RGMIIl}	—	0.75*1	ns	
	ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXC_TXCLK output skew		$t_{RGMIIos}$	–0.5	0.5	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV setup time		$t_{RGMIIls}$	1	—	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV hold time		t_{RGMIIh}	1	—	ns	
Ethernet (MII)	ETn_TXC_TXCLK, ETn_RXC_RXCLK cycle time	100 Mbps	t_{MIICK}	40	—	ns	Figure 3.5-14
		10 Mbps		400	—	ns	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK frequency	100 Mbps	—	25 – 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 – 50 ppm	2.5 + 50 ppm	MHz	
	ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXER output delay time		t_{MIId}	0	20	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV, ETn_RXER setup time		t_{MIIs}	10	—	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV, ETn_RXER hold time		t_{MIIf}	10	—	ns	

Note 1. The measurement condition of t_{RGMIIr} and t_{RGMIIl} is in FIGURE 3 in Reduced Gigabit Media Independent Interface (RGMII) 12/10/2000 Version 1.3.

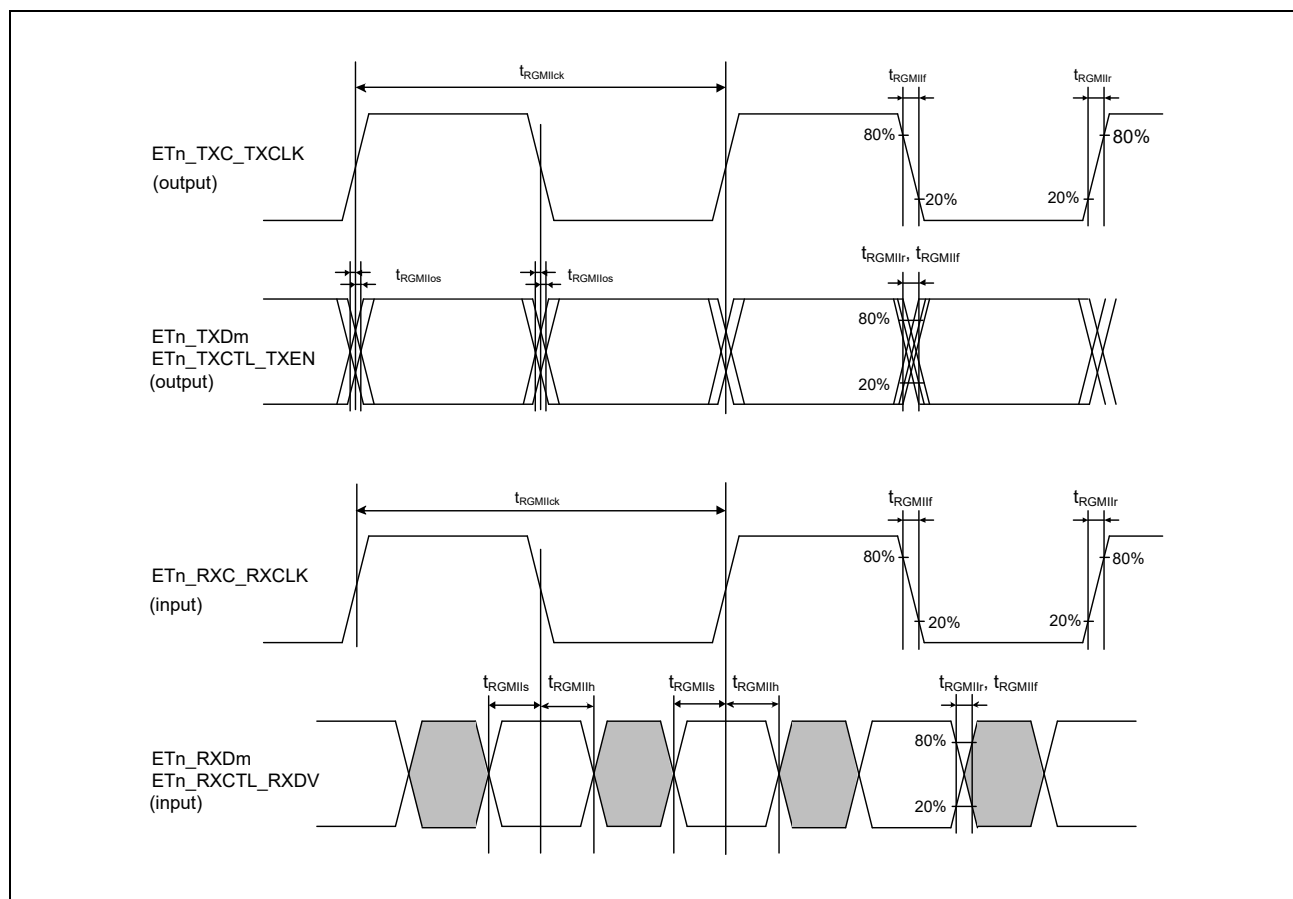


Figure 3.5-13 RGMII Transmission and Reception Timing (n = 0, 1)

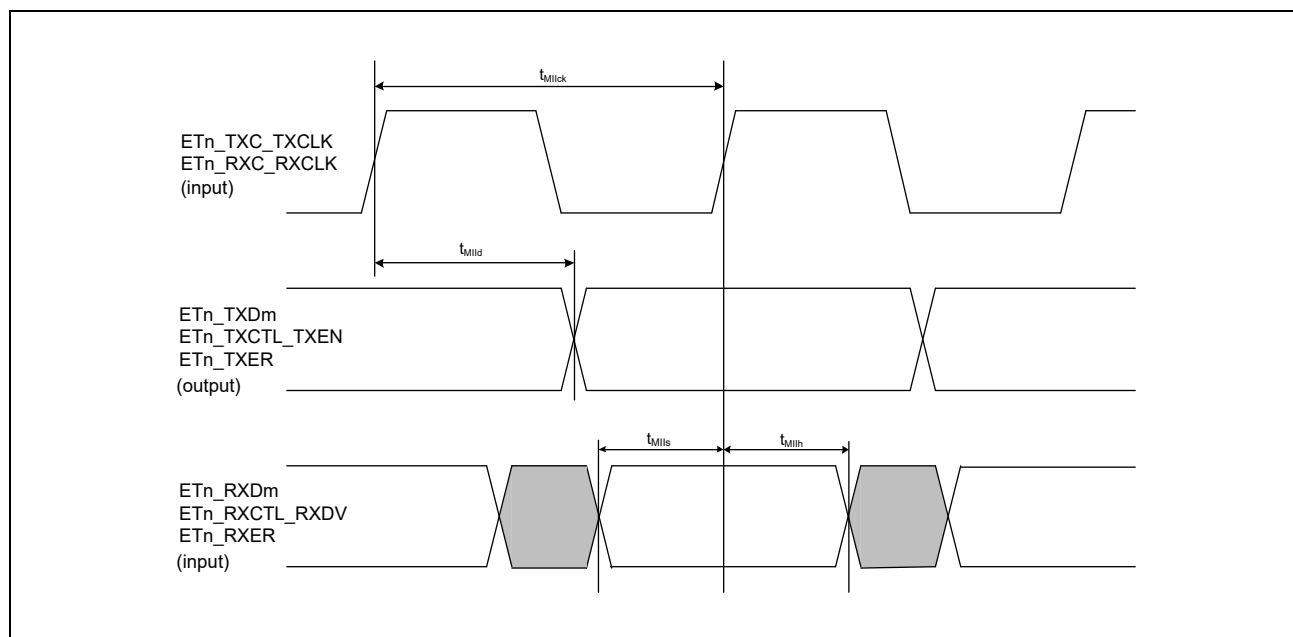


Figure 3.5-14 MII Transmission and Reception Timing (n = 0, 1)

3.5.10 USB 3.2 PHY Characteristics

The USB3 PHY of this LSI is compliant with the following USB 3.2 Gen2x1 standard:

Universal Serial Bus 3.2 Specification

3.5.11 USB 2.0 PHY Characteristics

The USB2 PHY of this LSI is compliant with the following USB 2.0 standard:

Universal Serial Bus 2.0 Specification

3.5.12 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of the PCI Express® Base Specification for Gen1/Gen 2/ Gen 3

3.5.13 xSPI Timing

Conditions:

- Single-end clock

$$V_{OH} = V_{DD18} \times 0.8, V_{OL} = V_{DD18} \times 0.2, C = 15 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{DD33} \times 0.8, V_{OL} = V_{DD33} \times 0.2, C = 15 \text{ pF (3.3 V)}$$

- Data

$$V_{OH} = V_{DD18} \times 0.8, V_{OL} = V_{DD18} \times 0.2, C = 15 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{DD33} \times 0.8, V_{OL} = V_{DD33} \times 0.2, C = 15 \text{ pF (3.3 V)}$$

Drive strength: $\times 6$

Table 3.5-14 xSPI Timing (1/2)

Parameter		Symbol	1.8V		3.3V		Unit	Figure
			Min.	Max.	Min.	Max.		
Cycle time	SDR	t _{PERIOD}	7.5	—	12.5	—	ns	Figure 3.5-15
	DDR		7.5	—	12.5	—	ns	
Clock output slew rate		t _{SRck}	0.75 / 0.56*1	—	1.03	—	V/ns	
Clock duty cycle distortion		t _{CKDCD}	0.0	t _{PERIOD} × 0.05	0.0	t _{PERIOD} × 0.05	ns	
Clock minimum pulse width		t _{CKMPW}	t _{PERIOD} × 0.45	—	t _{PERIOD} × 0.45	—	ns	
Differential clock crossing voltage		V _{OX(AC)}	0.4 × VDD18	0.6 × VDD18	—	—	V	
DS duty cycle distortion		t _{DSDCD}	0.0	t _{PERIOD} × 0.04	0.0	t _{PERIOD} × 0.04	ns	
DS minimum pulse width		t _{DSMPW}	t _{PERIOD} × 0.41	—	t _{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t _{SR}	0.75 / 0.56*1	—	1.03	—	V/ns	
Data input setup time (to CK)	SDR	t _{SU}	2.0	—	2.4	—	ns	Figure 3.5-16
Data input hold time (to CK)		t _H	1.0	—	1.0	—	ns	
Data output delay time		t _{OD}	—	1.6*2	—	1.8*2	ns	
Data output hold time		t _{OH}	−1.5	—	−2.3	—	ns	
Data output buffer off time		t _{BOFF}	−1.5	—	−2.3	—	ns	
Data input setup time (to DS)	DDR*2	t _{SU}	−0.6 / −0.8*1	—	−0.6 / −0.8*1	—	ns	Figure 3.5-17, Figure 3.5-18
Data input hold time (to DS)		t _H	t _{PERIOD} × 0.41 − 0.6 / t _{PERIOD} × 0.41 − 0.8*1	—	t _{PERIOD} × 0.41 − 0.6 / t _{PERIOD} × 0.41 − 0.8*1	—	ns	
Data output setup time (to CK)		t _{SUO}	0.6 / 1.0*1,*4	—	1.0	—	ns	
Data output hold time (to CK)		t _{HO}	0.6 / 1.0*1,*4	—	1.0	—	ns	
CS low to clock high		t _{CSLCKH}	6.0 / 8.0*1,*3	—	8.0*3	—	ns	Figure 3.5-16 to Figure 3.5-18
Clock low to CS high		t _{CKLCSH}	6.0 / 8.0*1	—	8.0	—	ns	
CS high time		t _{CSTD}	1	16	1	16	t _{PERIOD}	

Table 3.5-14 xSPI Timing (2/2)

Parameter	Symbol	1.8V		3.3V		Unit	Figure
		Min.	Max.	Min.	Max.		
DS low to CS high	t_{DSLCSH}	$t_{PERIOD} \times 0.8^{*7}$	—	$t_{PERIOD} \times 0.8^{*7}$	—	ns	Figure 3.5-19
CS high to DS Tri-state	t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low ^{*5}	t_{CSLDL}	0.0	12.5 ^{*6}	0.0	17.4 ^{*6}	ns	
DS Tri-state to CS low	t_{DSTCSL}	0.0	—	0.0	—	ns	
CK low to DS low ^{*8}	t_{CKLDL}	—	$(0.45 + e) \times t_{PERIOD} - 2.0^{*9}$	—	$(0.45 + e) \times t_{PERIOD} - 2.0^{*9}$	ns	

Note: CK: XSPI0_CKP (XSPI0_CKN)
DS: XSPI0_DS
CS: XSPI0_CS0N, XSPI0_CS1N

Note 1. Specification at 133 MHz / Specification at 100 MHz

Note 2. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1b).

Note 3. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1b).

Note 4. The standard value for xSPI266 is 0.8 ns.

Note 5. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.

Note 6. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

Note 7. These are the values when the t_{CLKDSL} constraint is satisfied.

Note 8. This constraint is necessary only to satisfy the t_{DSLCSH} requirement specified in JESD251, which specifies that t_{DSLCSH} must be at least 80% of t_{PERIOD} . Set LIOCFGCSn.CSNEGEX to the appropriate value to ensure the memory specification complies with this constraint.

Note 9. e: LIOCFGCSn.CSNEGEX (e = 0, 1)

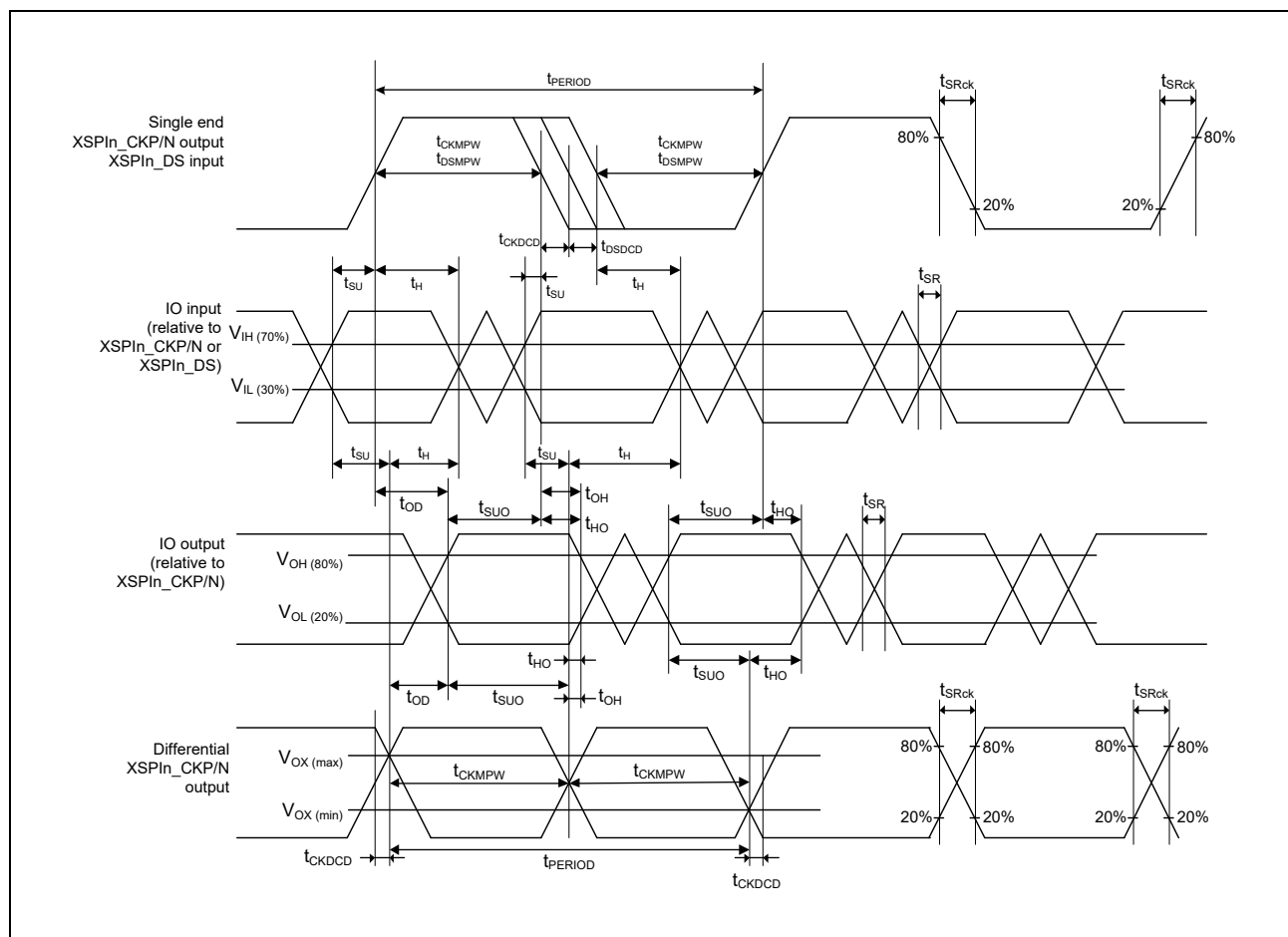


Figure 3.5-15 xSPI Clock / DS Timing

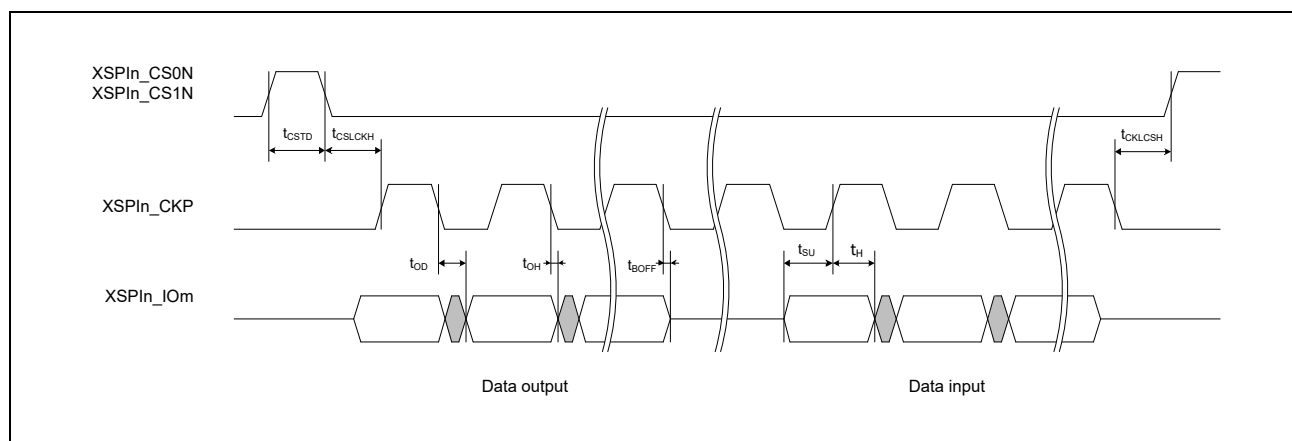


Figure 3.5-16 SDR Transmission and Reception Timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

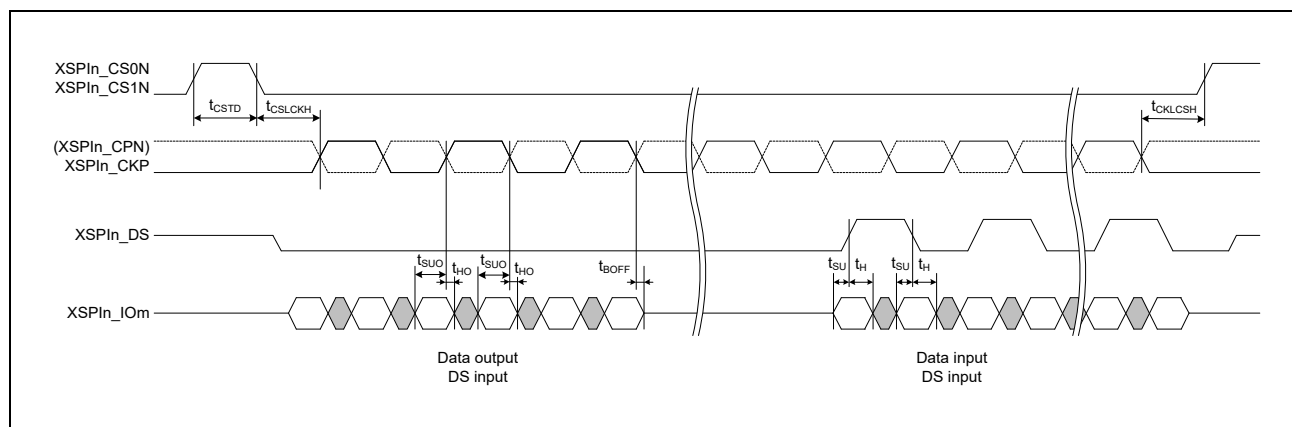


Figure 3.5-17 DDR Transmission and Reception Timing (4S-4D-4D, 8D-8D-8D)

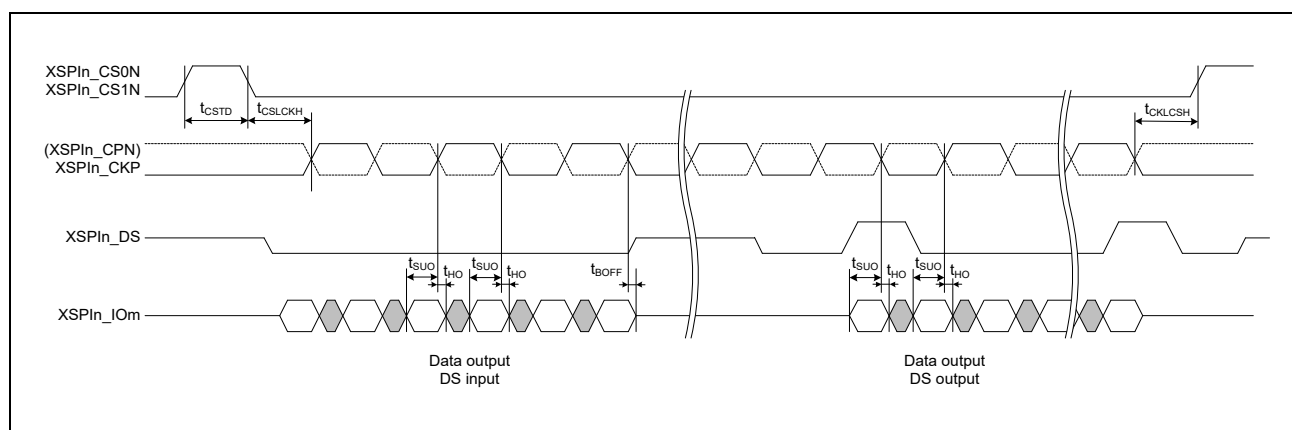


Figure 3.5-18 DDR Transmission and Reception Timing (HyperRAM write)

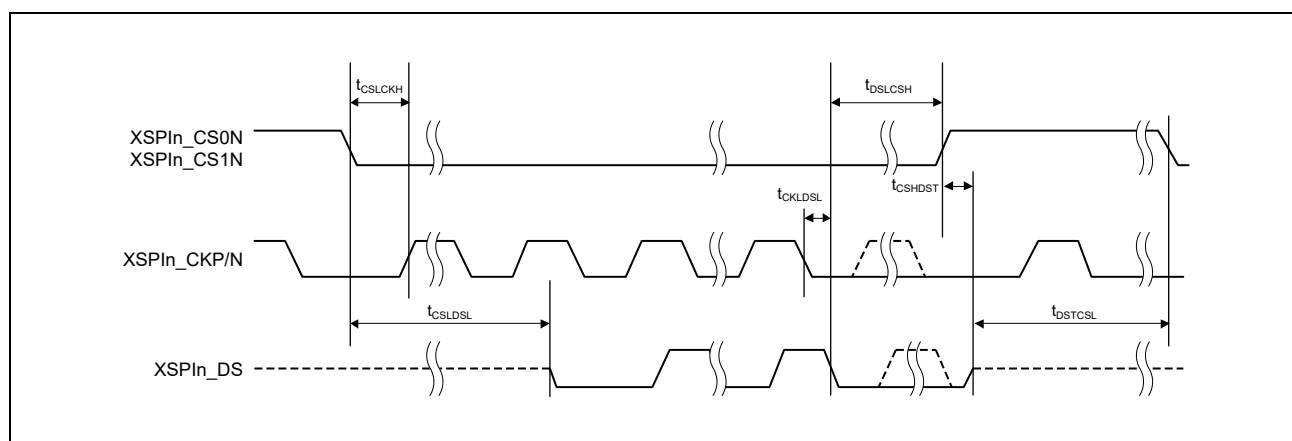


Figure 3.5-19 DS to CS Signal Timing

3.5.14 Serial Communications Interface (RSCI) Access Timing

Conditions:

$$V_{OH} = V_{DD18} \times 0.5, V_{OL} = V_{DD18} \times 0.5, C = 30 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{DD33} \times 0.5, V_{OL} = V_{DD33} \times 0.5, C = 30 \text{ pF (3.3 V)}$$

Drive strength: $\times 2$, $\times 4$ (However, $\times 6$ only for SCL (P93) and SDA (P92) of RSCI0 in simple I2C mode)

Table 3.5-15 RSCI Timing (1/2)

Parameter	Symbol	Min.	Max.	Unit	Figure
RSCI (Asynchronous)	Input clock cycle	t_{Scyc}	4	—	$t_{PSClCyc}$ Figure 3.5-20
	Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}
	Input clock rise time	t_{SCKr}	—	3	ns
	Input clock fall time	t_{SCKf}	—	3	ns
	Output clock cycle	t_{Scyc}	6	—	$t_{PSClCyc}$
	Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}
	Output clock rise time	$V_{DD1833} = 1.8 \text{ V}$	t_{SCKr}	—	6.18^{*2} ns
		$V_{DD1833} = 3.3 \text{ V}$	—	7.9^{*2}	ns
	Output clock fall time	$V_{DD1833} = 1.8 \text{ V}$	t_{SCKf}	—	6.18^{*2} ns
		$V_{DD1833} = 3.3 \text{ V}$	—	7.9^{*2}	ns
RSCI (Simple I2C, Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns Figure 3.5-21
	SDA input fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	$2 \times NF_{cyc}^{*1}$	ns
	Data input setup time	t_{SDAS}	250	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b	—	400	pF
RSCI (Simple I2C, Fast mode)	SDA input rise time	t_{Sr}	—	300	ns Figure 3.5-21
	SDA input fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	$2 \times NF_{cyc}^{*1}$	ns
	Data input setup time	t_{SDAS}	100	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b	—	400	pF

Table 3.5-15 RSCI Timing (2/2)

Parameter		Symbol	Min.	Max.	Unit	Figure
RSCI (Clock sync, Simple SPI)	SCK output clock cycle (master)	t_{SPCyc}	4	65536	$t_{PSClCyc}$	Figure 3.5-22 to Figure 3.5-27
	SCK input clock cycle (slave)		4	65536	$t_{PSClCyc}$	
	SCK clock high-level pulse width	t_{SPCKWH}	0.4	0.6	t_{SPCyc}	
	SCK clock low-level pulse width	t_{SPCKWL}	0.4	0.6	t_{SPCyc}	
	Input clock rise time	t_{SPCKR}	—	3	ns	
	Input clock fall time	t_{SPCKF}	—	3	ns	
	Output clock rise time	$V_{DD1833} = 1.8\text{ V}$	t_{SPCKR}	—	6.18^{*2}	ns
		$V_{DD1833} = 3.3\text{ V}$		—	7.9^{*2}	ns
	Output clock fall time	$V_{DD1833} = 1.8\text{ V}$	t_{SPCKF}	—	6.18^{*2}	ns
		$V_{DD1833} = 3.3\text{ V}$		—	7.9^{*2}	ns
	Data input setup time	Internal clock	t_{SU}	7	—	ns
		External clock		3	—	ns
	Data input hold time	Internal clock	t_H	3	—	ns
		External clock		3	—	ns
	Data output delay time	Internal clock	t_{OD}	—	3	ns
		External clock		—	12	ns
	Data output hold time	Internal clock	t_{OH}	−3	—	ns
		External clock		0	—	ns
	Data rise/fall time	$V_{DD1833} = 1.8\text{ V}$	t_{DR}, t_{DF}	—	6.18^{*2}	ns
		$V_{DD1833} = 3.3\text{ V}$		—	7.9^{*2}	ns
	Slave access time	Internal clock	t_{SA}	—	$3 \times t_{PSClCyc} + 12$	ns
		External clock		—	$3 \times t_{PSClCyc} + 12$	ns
	Slave output release time	Internal clock	t_{REL}	—	$3 \times t_{PSClCyc} + 12$	ns
		External clock		—	$3 \times t_{PSClCyc} + 12$	ns
RSCI (Simple SPI)	SS input setup time	t_{LEAD}	1	—	t_{SPCyc}	Figure 3.5-22 to Figure 3.5-27
	SS input hold time	t_{LAG}	1	—	t_{SPCyc}	
	SS input rise/fall time	t_{SSR}, t_{SSF}	—	3	ns	

Note: $t_{PSClCyc}$: RSCIn operating clock cycle ($n = 0$ to 9)

Note 1. $NF_{cyc} = 4p \times 2q - 1 \times t_{PSClCyc}$
 p: Common Control Register 2 set value ($p = 0, 1, 2, 3$)
 q: Common Control Register 1 set value ($q = 1, 2, 3, 4$)

Note 2. Output transition time from 20% to 80%

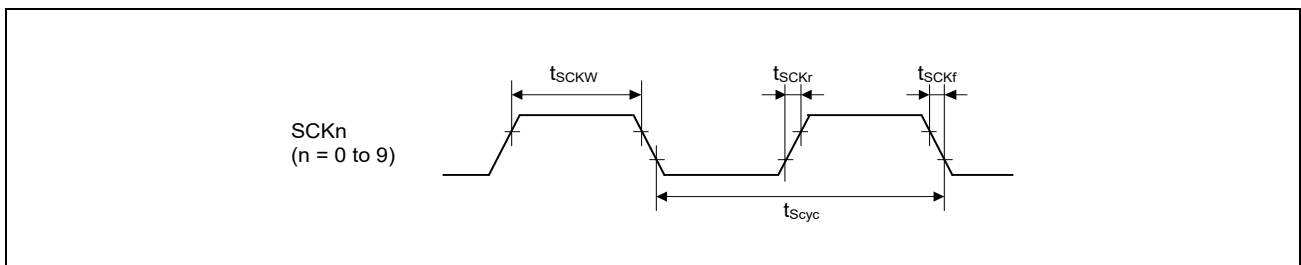


Figure 3.5-20 SCK Clock Input/Output Timing

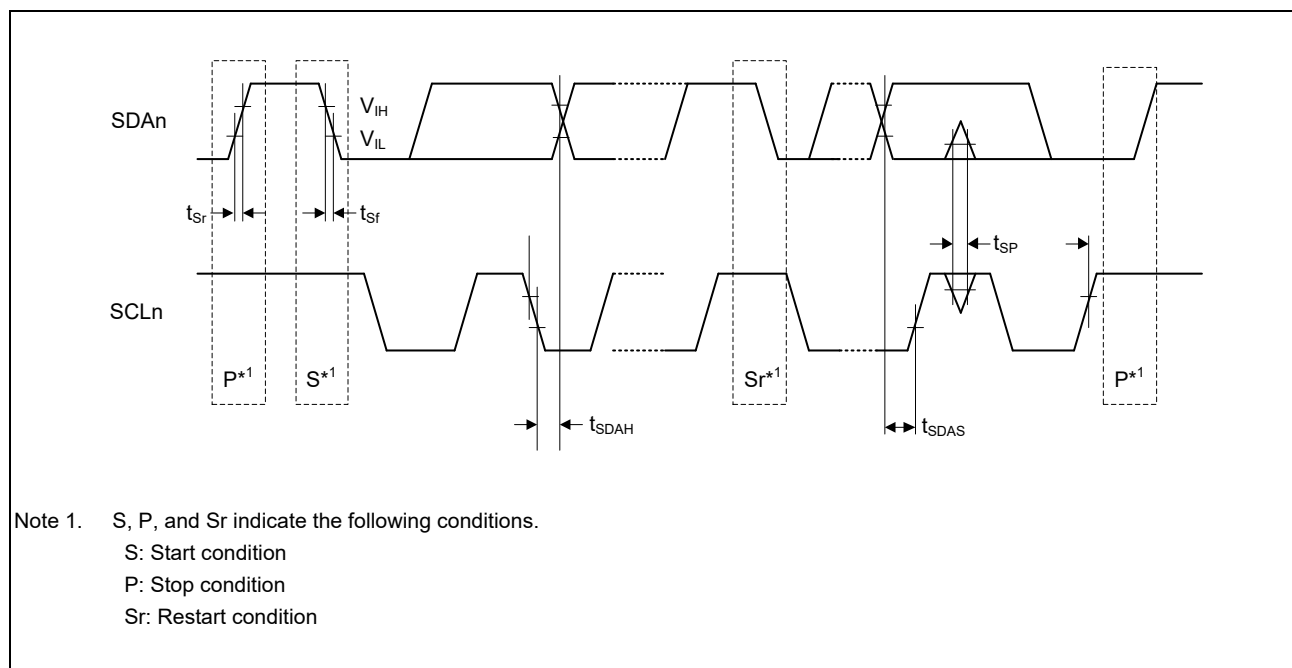


Figure 3.5-21 RSCI Simple I2C Mode Timing

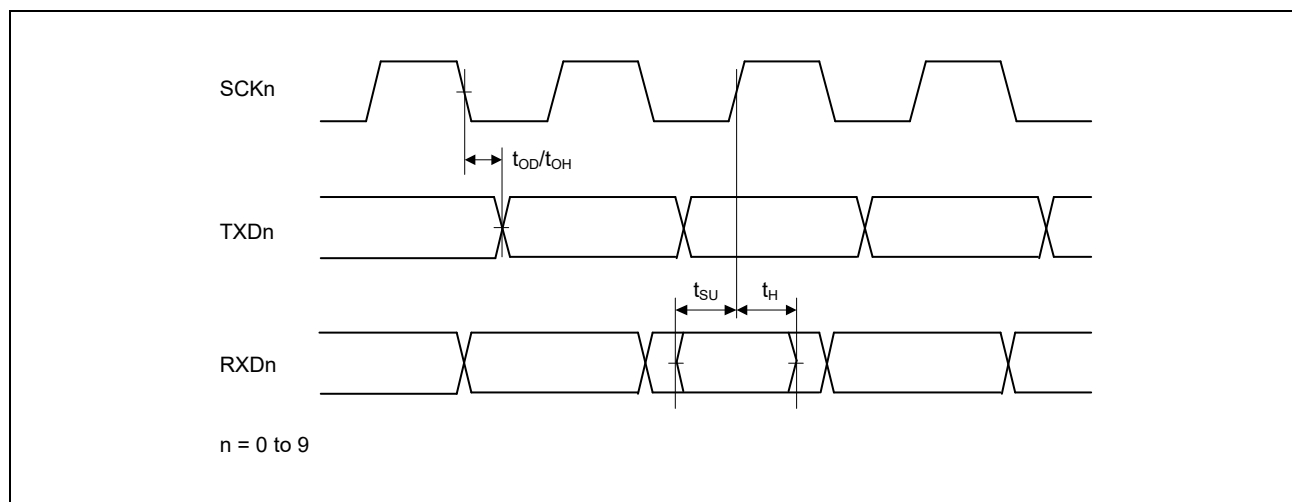


Figure 3.5-22 RSCI Input/Output Timing in Clock Synchronous Mode

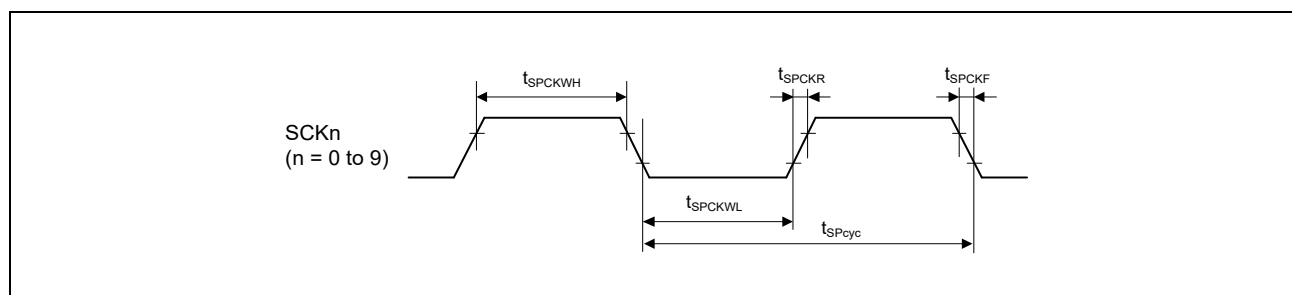


Figure 3.5-23 RSCI Simple SPI Mode Clock Timing

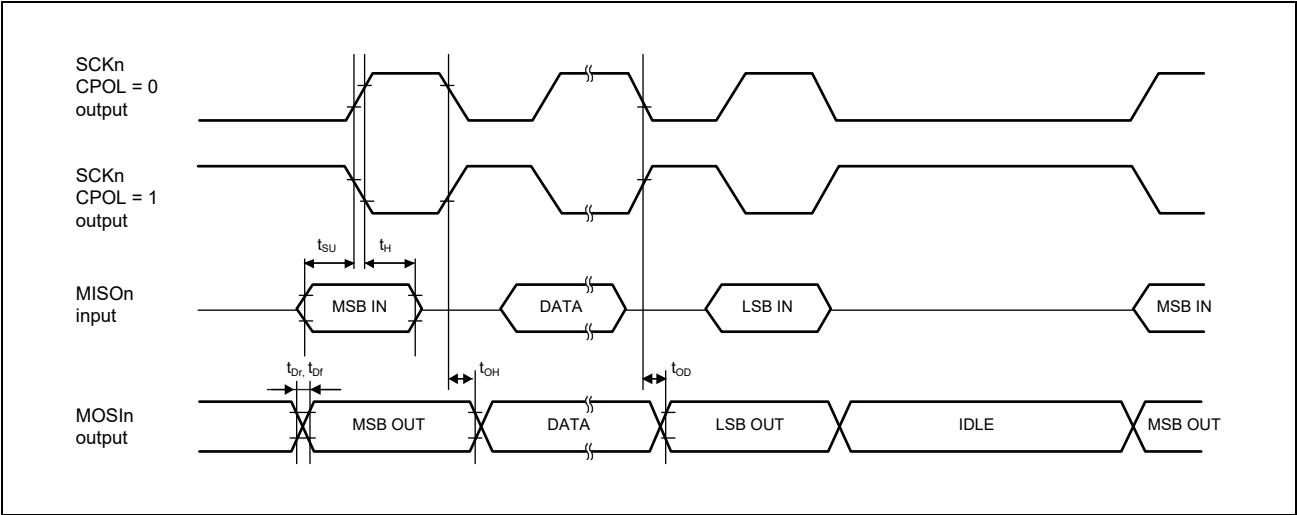


Figure 3.5-24 RSCI Simple SPI Mode Timing for Master when CPHA = 0

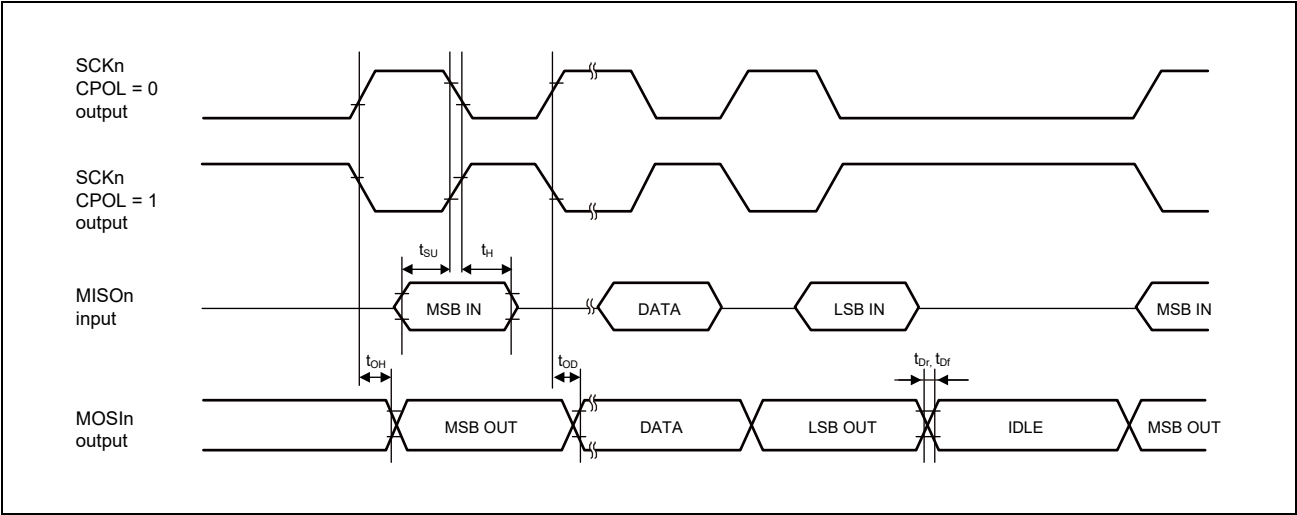


Figure 3.5-25 RSCI Simple SPI Mode Timing for Master when CPHA = 1

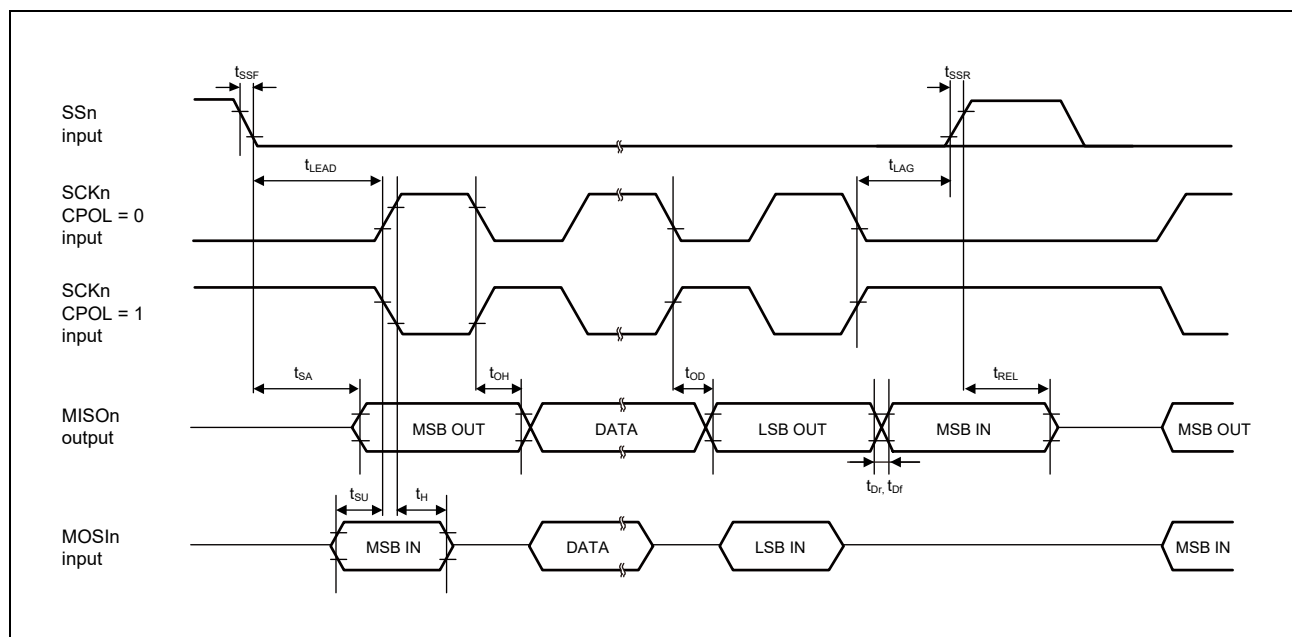


Figure 3.5-26 RSCI Simple SPI Mode Timing for Slave when CPHA = 0

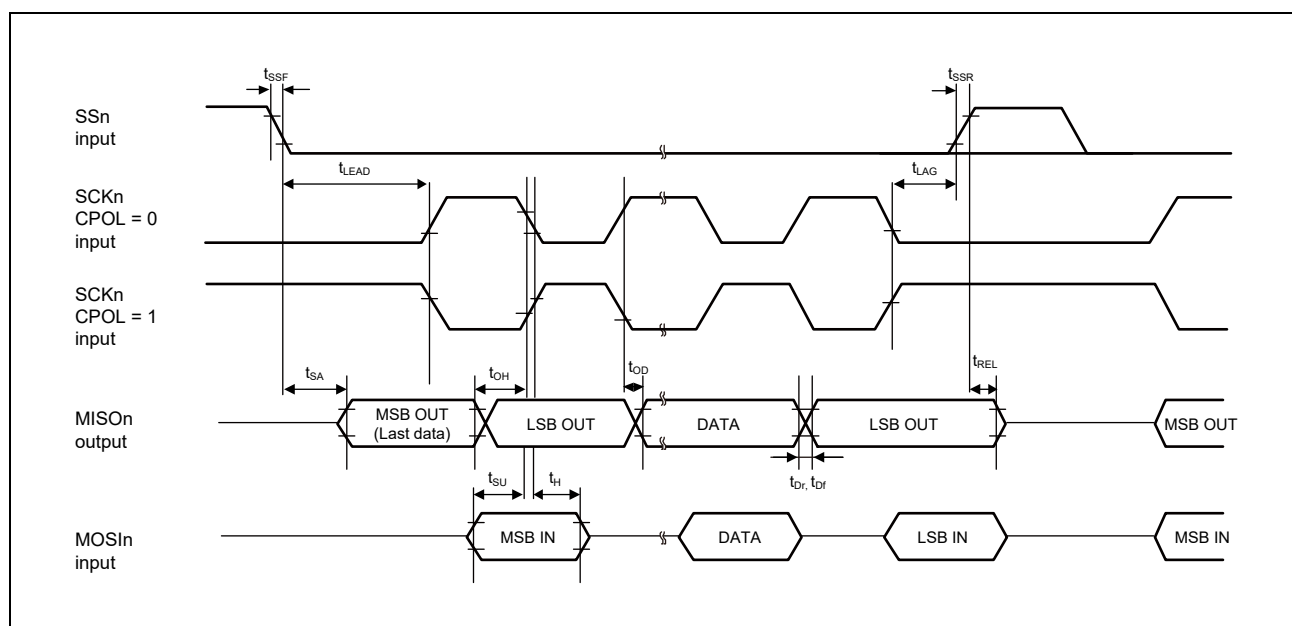


Figure 3.5-27 RSCI Simple SPI Mode Timing for Slave when CPHA = 1

3.5.15 Renesas Serial Peripheral Interface (RSPI) Access Timing

Conditions:

$$V_{OH} = VDD18 \times 0.5, V_{OL} = VDD18 \times 0.5, C = 30 \text{ pF (1.8 V)}$$

$$V_{OH} = VDD33 \times 0.5, V_{OL} = VDD33 \times 0.5, C = 30 \text{ pF (3.3 V)}$$

Drive strength: $\times 6$

Table 3.5-16 RSPI Timing (1/2)

Parameter		Symbol	Min.*1	Max.*1	Unit	Figure
RSPCK clock cycle	Master	t_{SPCyc}	4	4096	t_{SPICyc}	Figure 3.5-28
	Slave		4	4096	t_{SPICyc}	
RSPCK clock high-level pulse width	Master	t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPICyc}	
RSPCK clock low-level pulse width	Master	t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPICyc}	
RSPCK clock rise/fall time	Output	t_{SPCKr}	—	3^{*5}	ns	
	Input	t_{SPCKf}	—	3^{*5}	ns	
Data input setup time	Master	t_{SU}	5	—	ns	Figure 3.5-29 to Figure 3.5-35
	Slave		3	—	ns	
Data input hold time	Master	t_{H}	3	—	ns	
	Slave		3	—	ns	
SSL setup time	Master	t_{LEAD}	$N \times t_{SPCyc} - 3^{*2}$	$N \times t_{SPCyc} + 3^{*2}$	ns	Figure 3.5-29 to Figure 3.5-32
	Slave		5	—	t_{SPICyc}	
SSL hold time	Master	t_{LAG}	$N \times t_{SPCyc} - 3^{*3}$	$N \times t_{SPCyc} + 3^{*3}$	ns	
	Slave		5	—	t_{SPICyc}	
Continuous transmission delay	Master	t_{TD}	$t_{SPCyc} + 2 \times t_{SPICyc}$	$8 \times t_{SPCyc} + 2 \times t_{SPICyc}$	ns	
	Slave		$t_{SPCyc} + 5 \times t_{SPICyc}$	—	ns	
TI-SSP SS input setup time		t_{TISS}	3	—	ns	Figure 3.5-33 to Figure 3.5-35
TI-SSP SS input hold time		t_{TISH}	3	—	ns	
TI-SSP next access time		t_{TIND}	M^{*4}	—	t_{SPICyc}	
TI-SSP Master SS output delay		t_{TISSOD}	-3	3	ns	
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns	
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns	
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	7.5	ns	
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	7.5	ns	
SSL Activation to Data Output Delay		t_{OD1}	—	3	ns	Figure 3.5-29
Data output delay time	Master	t_{OD}	—	3	ns	Figure 3.5-29 to Figure 3.5-35
	Slave		—	7.5	ns	
Data output hold time	Master	t_{OH}	-3	—	ns	
	Slave		3	—	ns	
MOSI, MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	3^{*5}	ns	
	Input		—	1	μs	
SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	3^{*5}	ns	Figure 3.5-29, Figure 3.5-30
	Input		—	1	μs	

Table 3.5-16 RSPI Timing (2/2)

Parameter	Symbol	Min.*1	Max.*1	Unit	Figure
Slave access time	t_{SA}	—	8	ns	Figure 3.5-31,
Slave output release time	t_{REL}	—	8	ns	Figure 3.5-32

Note 1. t_{SPCyc} : RSPI peripheral clock cycle

Note 2. N: SPI Clock Delay Register set value + 1 (1 to 8)

Note 3. N: SPI Slave Select Negation Delay Register set value + 1 (1 to 8)

Note 4. M: SPI Slave Select Negation Delay Register] set value + 2 (2 to 9)

Note 5. Output transition time from 20% to 80%

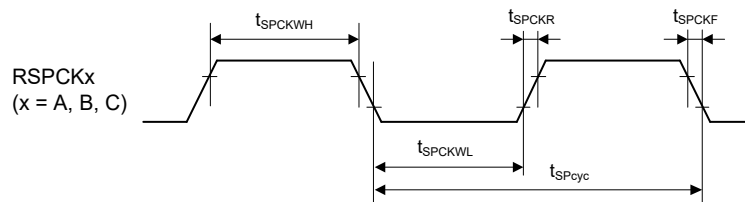
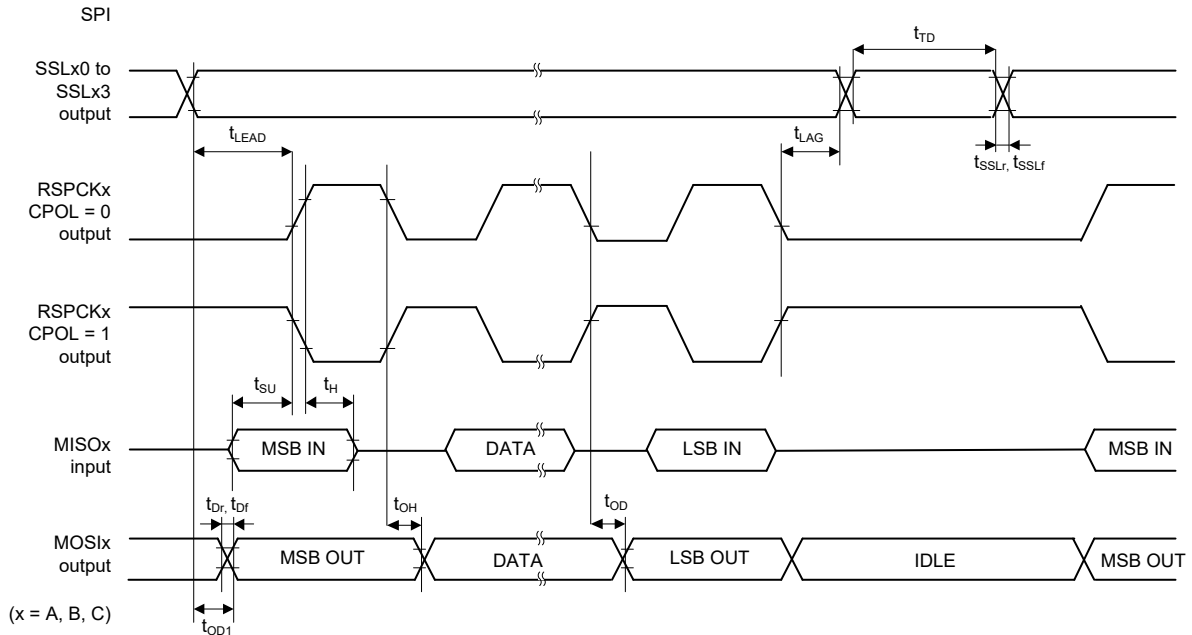


Figure 3.5-28 RSPI Clock Timing



Note: CPOL: Clock polarity setting

Figure 3.5-29 RSPI Timing (Master, Motorola RSPI, CPHA = 0)

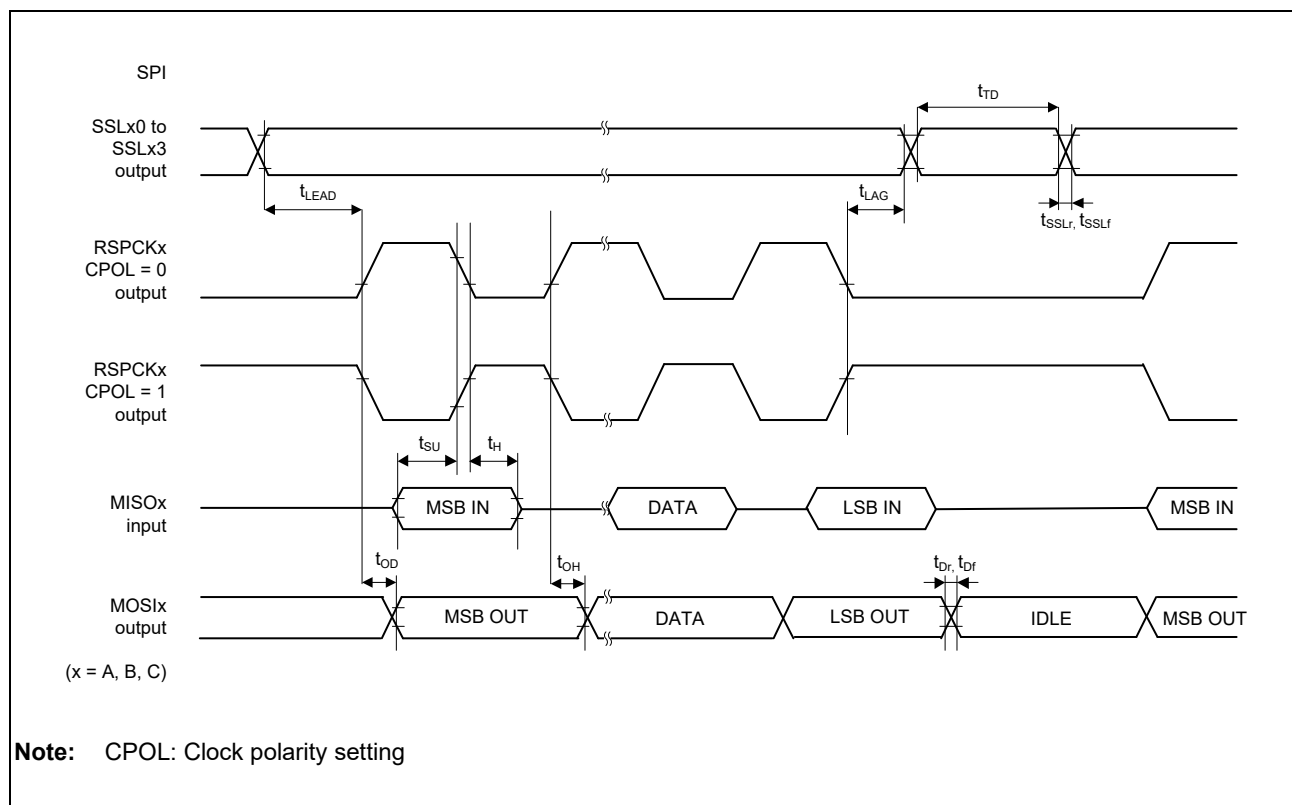


Figure 3.5-30 RSPI Timing (Master, Motorola RSPI, CPHA = 1)

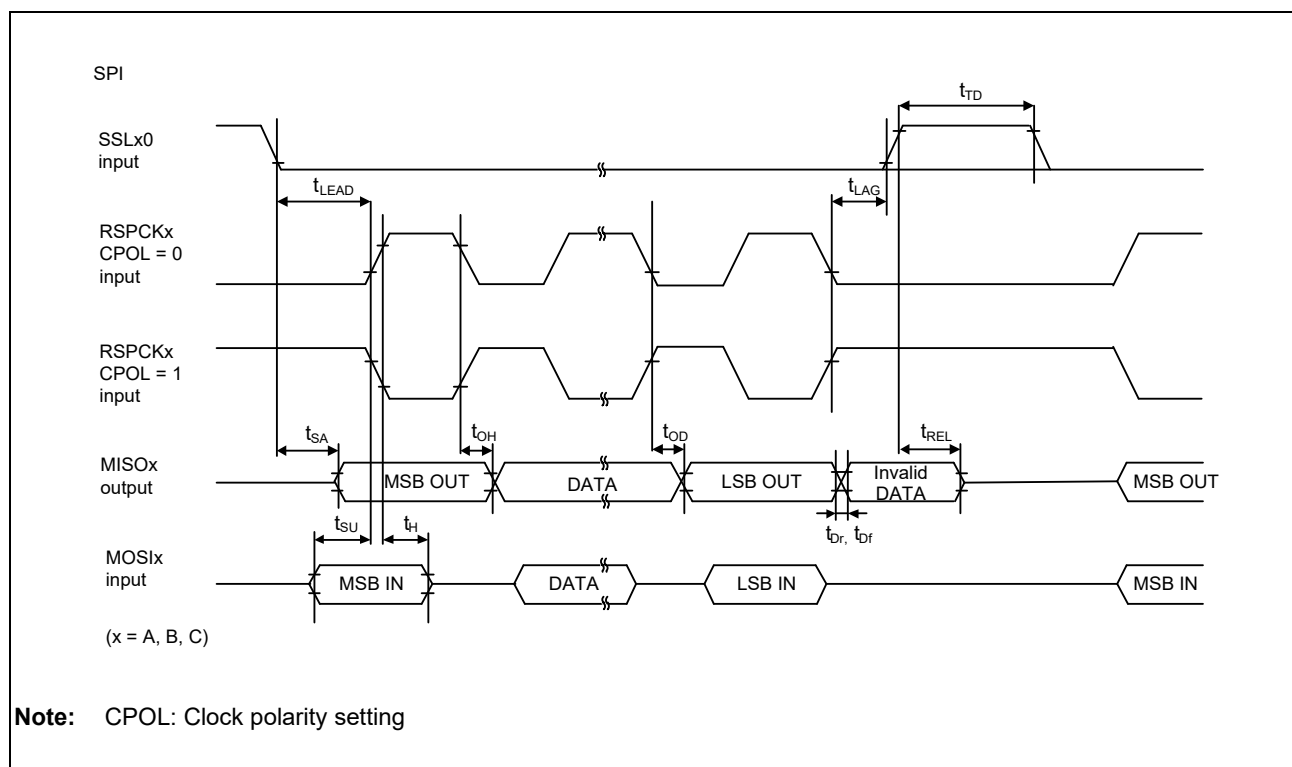


Figure 3.5-31 RSPI Timing (Slave, Motorola RSPI, CPHA = 0)

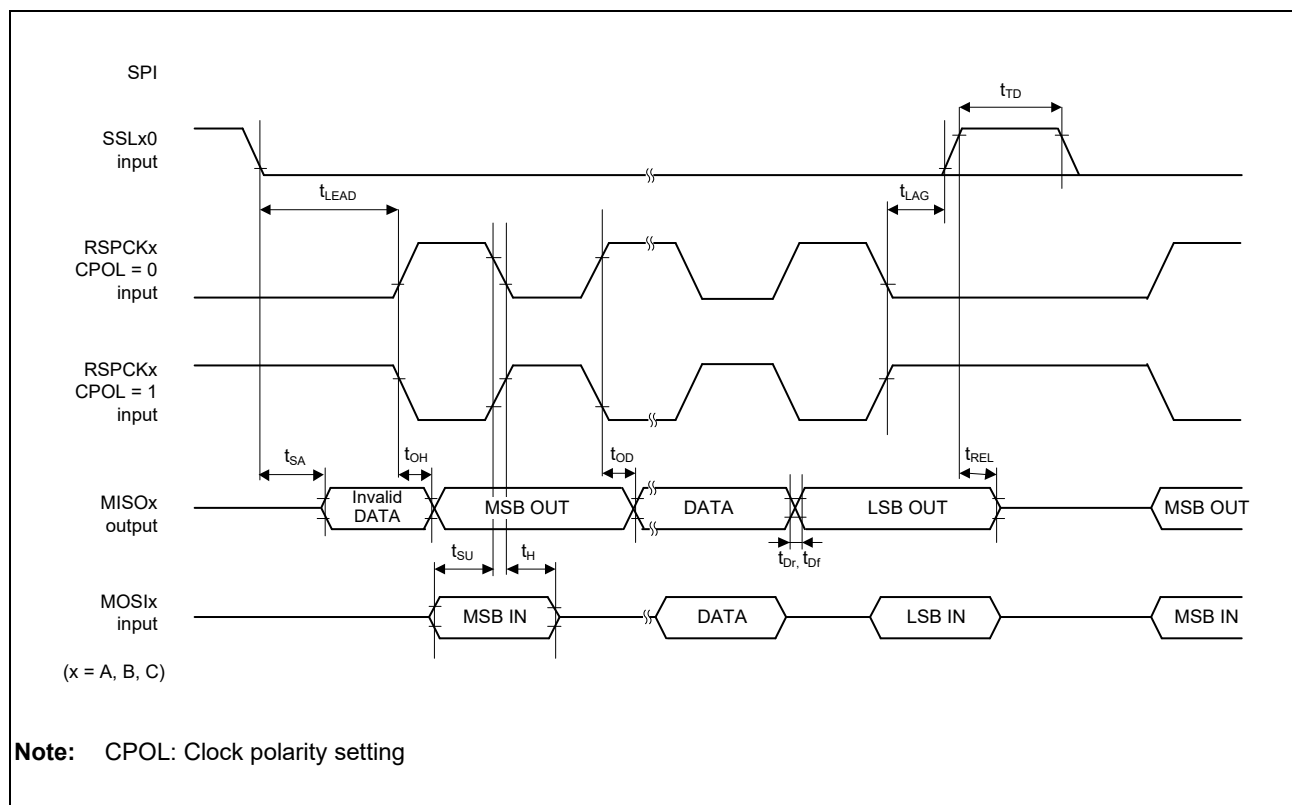


Figure 3.5-32 RSPI Timing (Slave, Motorola RSPI, CPHA = 1)

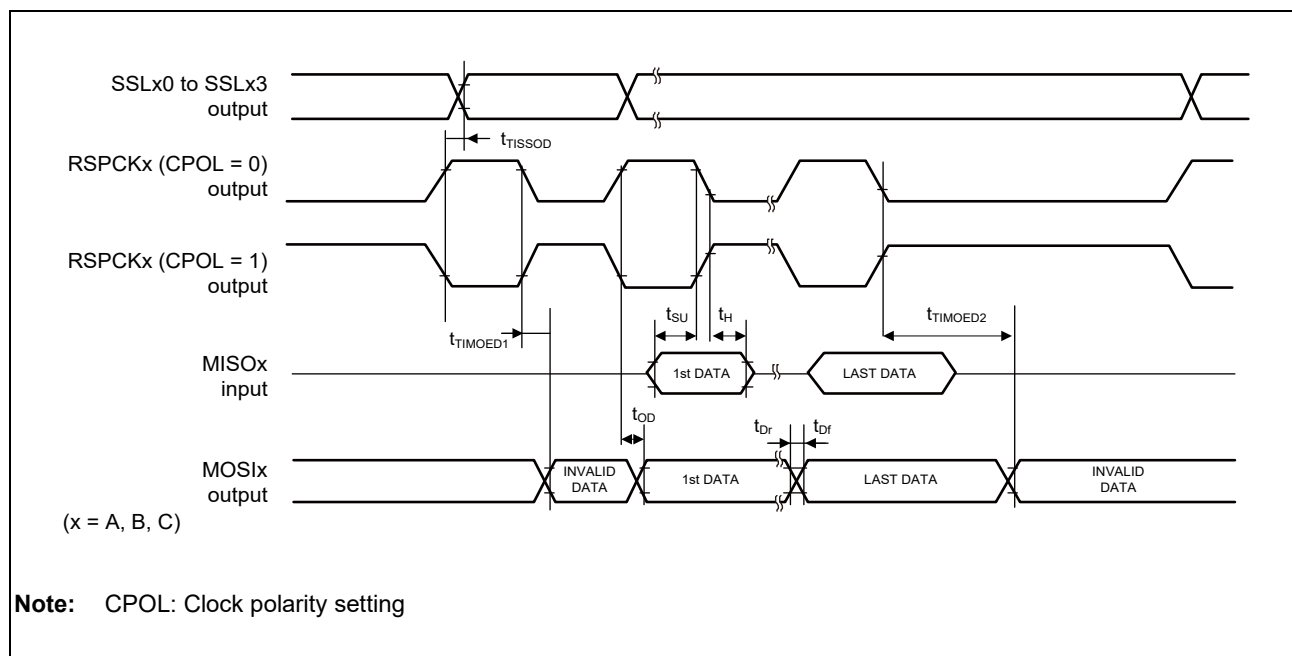


Figure 3.5-33 RSPI Timing (Master, TI SSP)

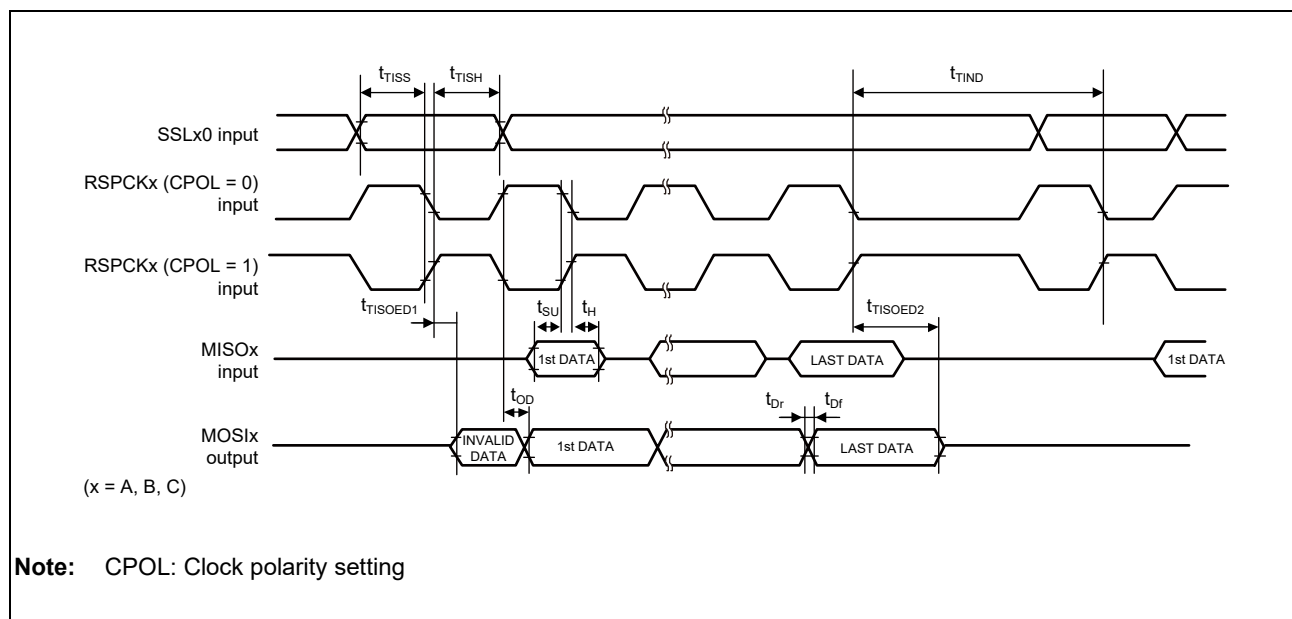


Figure 3.5-34 RSPI Timing (Slave, TI-SSP, with delay in burst transfer)

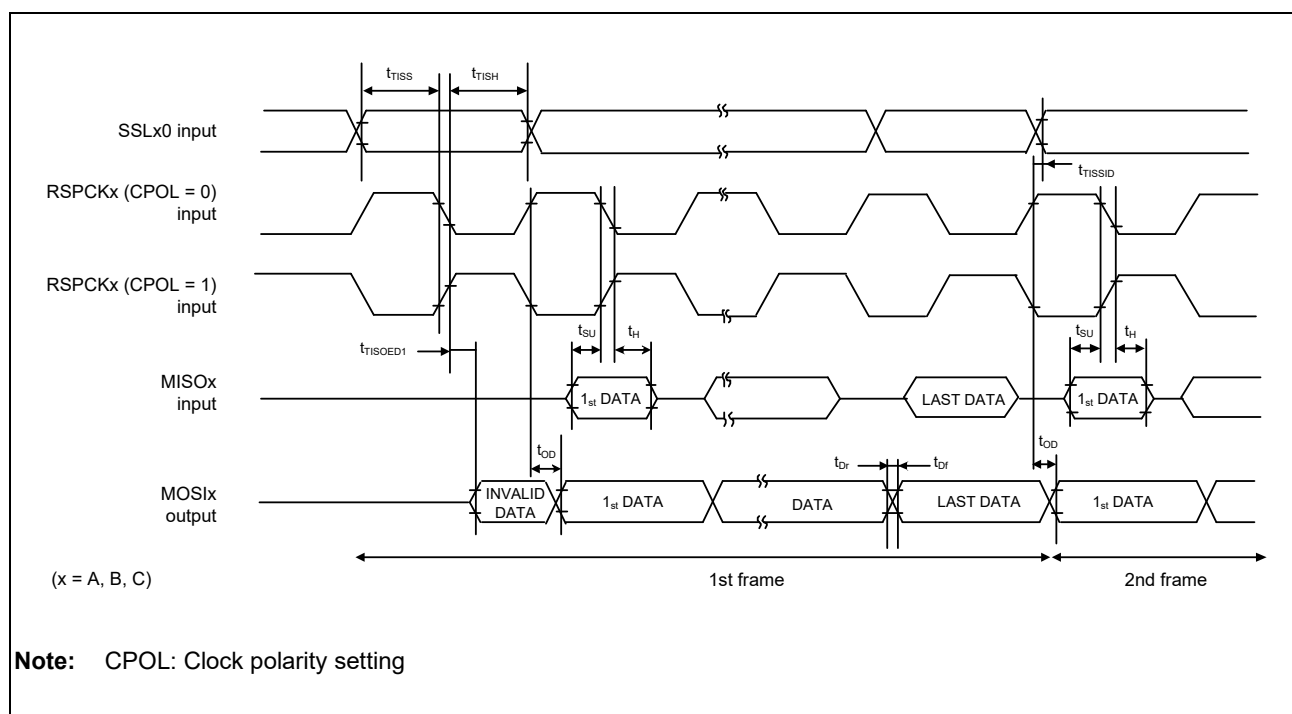


Figure 3.5-35 RSPI Timing (Slave, TI-SSP, without delay in burst transfer)

3.5.16 Renesas IIC Bus Interface (RIIC) Access Timing

Drive strength: $\times 6$

Table 3.5-17 RIIC Timing

Parameter		Symbol	Min. ^{*1,*2}	Max. ^{*1,*2}	Unit	Figure
RIIC (Standard-mode)	SCL cycle time	t _{SCL}	6(12) × t _{IICcyc} + 1300	—	ns	Figure 3.5-36
	SCL high-level pulse width	t _{SCLH}	3(6) × t _{IICcyc} + 300	—	ns	
	SCL low-level pulse width	t _{SCLL}	3(6) × t _{IICcyc} + 300	—	ns	
	SCL, SDA rise time ^{*3}	t _{sr}	—	1000	ns	
	SCL, SDA fall time	t _{sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t _{SP}	0	1(4) × t _{IICcyc}	ns	
	SDA bus free time	t _{BUF}	3(6) × t _{IICcyc} + 300	—	ns	
	Hold time for START condition	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t _{STAS}	1000	—	ns	
	Setup time for STOP condition	t _{STOS}	1000	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load ^{*5}	C _b	—	400	pF	
RIIC (Fast-mode)	SCL cycle time	t _{SCL}	6(12) × t _{IICcyc} + 600	—	ns	Figure 3.5-36
	SCL high-level pulse width	t _{SCLH}	3(6) × t _{IICcyc} + 300	—	ns	
	SCL low-level pulse width	t _{SCLL}	3(6) × t _{IICcyc} + 300	—	ns	
	SCL, SDA rise time ^{*3}	t _{sr}	—	300	ns	
	SCL, SDA fall time	t _{sf}	— ^{*4}	300	ns	
	SCL, SDA spike pulse removal time	t _{SP}	0	1(4) × t _{IICcyc}	ns	
	SDA bus free time	t _{BUF}	3(6) × t _{IICcyc} + 300	—	ns	
	Hold time for START condition	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t _{STAS}	300	—	ns	
	Setup time for STOP condition	t _{STOS}	300	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load ^{*5}	C _b	—	400	pF	
RIIC (Fast-mode Plus)	SCL cycle time	t _{SCL}	6(12) × t _{IICcyc} + 240	—	ns	Figure 3.5-36
	SCL high-level pulse width	t _{SCLH}	3(6) × t _{IICcyc} + 120	—	ns	
	SCL low-level pulse width	t _{SCLL}	3(6) × t _{IICcyc} + 120	—	ns	
	SCL, SDA rise time ^{*3}	t _{sr}	—	120	ns	
	SCL, SDA fall time	t _{sf}	— ^{*4}	120	ns	
	SCL, SDA spike pulse removal time	t _{SP}	0	1(4) × t _{IICcyc}	ns	
	SDA bus free time	t _{BUF}	3(6) × t _{IICcyc} + 120	—	ns	
	Hold time for START condition	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t _{STAS}	300	—	ns	
	Setup time for STOP condition	t _{STOS}	300	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load ^{*5}	C _b	—	550 ^{*6}	pF	

Note 1. t_{IICcyc} : RIIC internal reference clock (RIIC_n_ckm) cycle

- Note 2. The values outside parentheses apply when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The values within parentheses apply when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.
- Note 3. The maximum and minimum values of the pull-up resistor are determined according to Equations (1) and (2) provided in Section 7.1, Pull-up resistor sizing, of the *UM10204, I²C-bus specification and user manual, Rev. 7.0*. For Equation (2), use the I_{OL} value specified under the "Condition" column of "Low-level output voltage" in **Table 3.4-2**. The I/O Type is 3.3/1.8-V switching I/O type 2.
- Note 4. The minimum value is not specified for t_{sf} in Fast-mode or Fast-mode Plus.
- Note 5. C_b is the total capacitance of the bus lines.
- Note 6. When V_{DD} is 3.3 V, the maximum capacitive load that can satisfy $t_{sr} \leq 120$ ns is 400 pF.

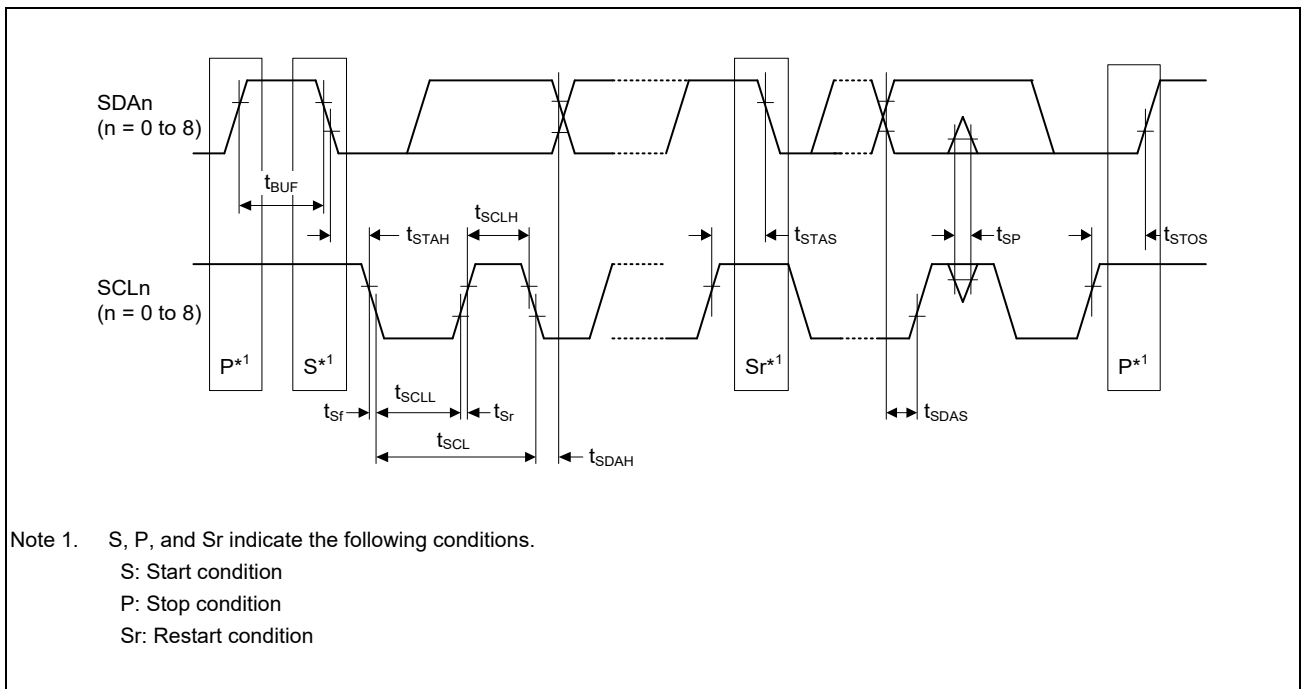


Figure 3.5-36 IIC Bus Interface Input/Output Timing

3.5.17 I3C Timing

Drive strength: $\times 6$

Table 3.5-18 IIC Timing

Parameter	Symbol	Min.*1	Max.	Unit	Figure	
IIC (Standard mode, SMBus)	SCL3n cycle time	t _{SCL}	4(36) × t _{IICcyc} + 4 × t _{Pcyc} + 1300	—	ns	Figure 3.5-37
	SCL3n high-level pulse width	t _{SCLH}	2(18) × t _{IICcyc} + 2 × t _{Pcyc} + 300	—	ns	
	SCL3n low-level pulse width	t _{SCLL}	2(18) × t _{IICcyc} + 2 × t _{Pcyc} + 800	—	ns	
	SCL3n, SDA3n rise time*2	t _{Sr}	—	1000	ns	
	SCL3n, SDA3n fall time	t _{Sf}	—	300	ns	
	SCL3n, SDA3n spike pulse removal time	t _{SP}	0	1(16) × t _{IICcyc}	ns	
	SDA3n bus free time	t _{BUF}	3(20) × t _{IICcyc} + 300	—	ns	
	Hold time for START condition	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t _{STAS}	1000	—	ns	
	Setup time for STOP condition	t _{STOS}	1000	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C _b	—	400	pF	
IIC (Fast mode)	SCL3n cycle time	t _{SCL}	4(36) × t _{IICcyc} + 4 × t _{Pcyc} + 600	—	ns	Figure 3.5-37
	SCL3n high-level pulse width	t _{SCLH}	2(18) × t _{IICcyc} + 2 × t _{Pcyc} + 300	—	ns	
	SCL3n low-level pulse width	t _{SCLL}	2(18) × t _{IICcyc} + 2 × t _{Pcyc} + 300	—	ns	
	SCL3n, SDA3n rise time*2	t _{Sr}	—	300	ns	
	SCL3n, SDA3n fall time	t _{Sf}	—	300	ns	
	SCL3n, SDA3n spike pulse removal time	t _{SP}	0	1(16) × t _{IICcyc}	ns	
	SDA3n bus free time	t _{BUF}	3(20) × t _{IICcyc} + 300	—	ns	
	Hold time for START condition	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t _{STAS}	300	—	ns	
	Setup time for STOP condition	t _{STOS}	300	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C _b	—	400	pF	

Note 1. t_{IICcyc} : I3C internal reference clock (I3C ϕ) cycle, t_{Pcyc} : I3C_0_TCLK cycle
Values in parentheses apply when the digital noise filter stage is 16 clock cycle while the digital filter is enabled.

Note 2. The maximum and minimum values of the pull-up resistor are determined according to Equations (1) and (2) provided in Section 7.1, Pull-up resistor sizing, of the *UM10204, I²C-bus specification and user manual, Rev. 7.0*.
For Equation (2), use the I_{OL} value specified under the "Condition" column of "Low-level output voltage" in **Table 3.4-2**. The I/O Type is 1.8/1.2-V switching I/O type.

Table 3.5-19 IIC Timing (Fast-mode+)

Parameter		Symbol	Min.* ¹	Max.	Unit	Figure
IIC (Fast-mode+)	SCL3n cycle time	t _{SCL}	4(26) × t _{IICcyc} + 4 × t _{Pcyc} + 240	—	ns	Figure 3.5-37
	SCL3n high-level pulse width	t _{SCLH}	2(18) × t _{IICcyc} + 2 × t _{Pcyc} + 120	—	ns	
	SCL3n low-level pulse width	t _{SCLL}	2(18) × t _{IICcyc} + 2 × t _{Pcyc} + 120	—	ns	
	SCL3n, SDA3n rise time* ²	t _{Sr}	—	120	ns	
	SCL3n, SDA3n fall time	t _{Sf}	—	120	ns	
	SCL3n, SDA3n spike pulse removal time	t _{SP}	—	1(16) × t _{IICcyc}	ns	
	SDA3n bus free time	t _{BUF}	3(20) × t _{IICcyc} + 120	—	ns	
	Hold time for START condition	t _{STAH}	t _{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t _{STAS}	260	—	ns	
	Setup time for STOP condition	t _{STOS}	260	—	ns	
	Data setup time	t _{SDAS}	50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C _b	—	550	pF	

Note 1. t_{IICyc} : I3C internal reference clock (I3C ϕ) cycle, t_{Pcyc} : I3C_0_TCLK cycle
Values in parentheses apply when the digital noise filter stage is 16 clock cycle while the digital filter is enabled.

Note 2. The maximum and minimum values of the pull-up resistor are determined according to Equations (1) and (2) provided in Section 7.1, Pull-up resistor sizing, of the *UM10204, I²C-bus specification and user manual, Rev. 7.0*.
For Equation (2), use the I_{OL} value specified under the "Condition" column of "Low-level output voltage" in **Table 3.4-2**. The I/O Type is 1.8/1.2-V switching I/O type.

Table 3.5-20 IIC Timing (HS mode)

Parameter		Symbol	Cb = 100 pF (Max.)		Cb = 400 pF*2		Unit	Figure
			Min.*1	Max.	Min.*1	Max.		
IIC (HS mode)	SCL3n cycle time	t _{SCL}	$3(36) \times t_{IICyc} + 4 \times t_{Pcyc} + 240$	—	$3(36) \times t_{IICyc} + 4 \times t_{Pcyc} + 240$	—	ns	Figure 3.5-37
	SCL3n high-level pulse width	t _{SCLH}	$2(18) \times t_{IICyc} + 2 \times t_{Pcyc} + 120$	—	$2(18) \times t_{IICyc} + 2 \times t_{Pcyc} + 120$	—	ns	
	SCL3n low-level pulse width	t _{SCLL}	$2(18) \times t_{IICyc} + 2 \times t_{Pcyc} + 120$	—	$2(18) \times t_{IICyc} + 2 \times t_{Pcyc} + 120$	—	ns	
	SCL3n rise time	t _{SrCL}	—	40	—	80	ns	
	SCL3n rise time after a repeated START condition and after an acknowledge bit*3	t _{SrCL1}	—	80	—	160	ns	
	SDA3n rise time*3	t _{SrDA}	—	80	—	160	ns	
	SCL3n fall time	t _{SfCL}	—	40	—	80	ns	
	SDA3n fall time	t _{SfDA}	—	80	—	160	ns	
	SCL3n, SDA3n spike pulse removal time	t _{SP}	0	$1(16) \times t_{IICyc}$	0	$1(16) \times t_{IICyc}$	ns	
	Hold time for START condition	t _{STAH}	$t_{IICyc} + 135$	—	$t_{IICyc} + 135$	—	ns	
	Setup time for repeated START condition	t _{STAS}	160	—	160	—	ns	
	Setup time for STOP condition	t _{STOS}	160	—	160	—	ns	
	Data setup time	t _{SDAS}	10	—	10	—	ns	
	Data hold time	t _{SDAH}	0	80	0	150	ns	
	SCL3n, SDA3n capacitive load	C _b	—	100	—	400	pF	

- Note 1. t_{IICyc} : I3C internal reference clock (I3C ϕ) cycle, t_{Pcyc} : I3C_0_TCLK cycle.
Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1b.
- Note 2. For bus line loads C_b between 100 pF and 400 pF, the timing parameters must be linearly interpolated.
- Note 3. The maximum and minimum values of the pull-up resistor are determined according to Equations (1) and (2) provided in Section 7.1, Pull-up resistor sizing, of the *UM10204, I²C-bus specification and user manual, Rev. 7.0*.
For Equation (2), use the I_{OL} value specified under the "Condition" column of "Low-level output voltage" in **Table 3.4-2**. The I/O Type is 1.8/1.2-V switching I/O type.

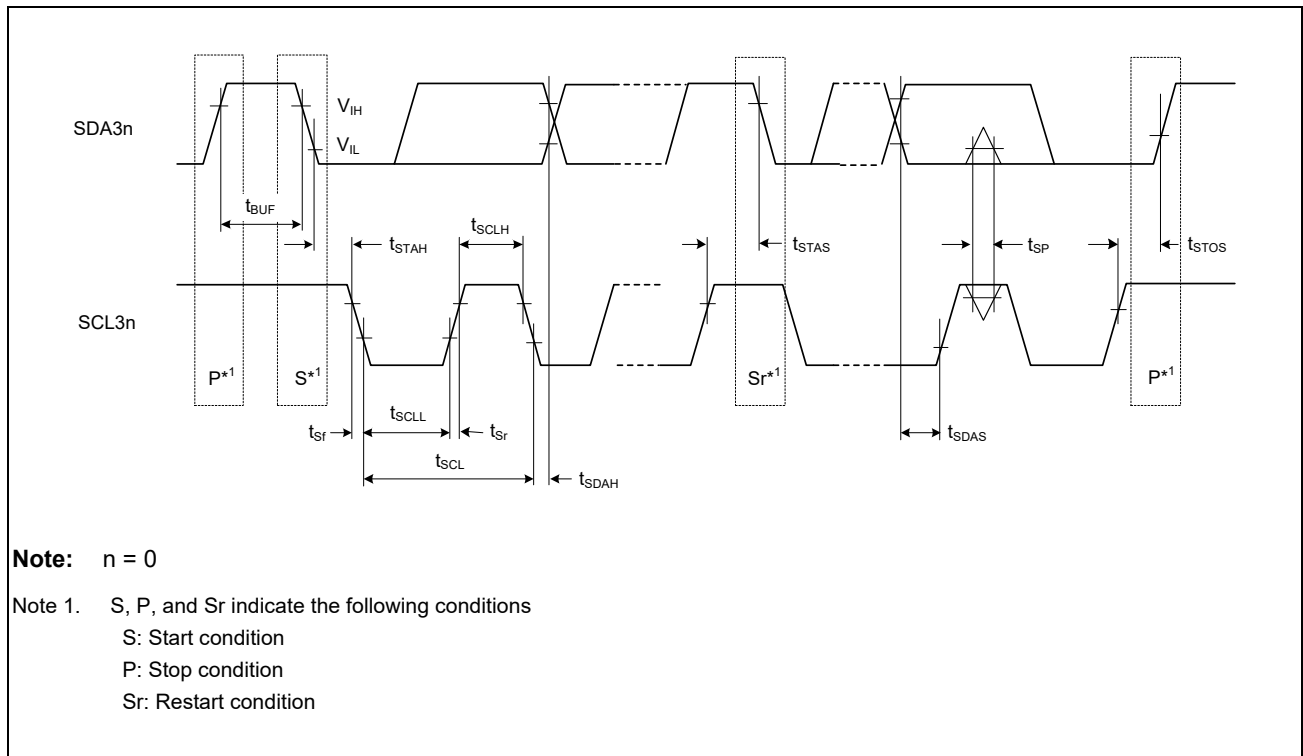


Figure 3.5-37 I3C Bus Interface Input/Output Timing

Table 3.5-21 I3C Timing (Open Drain Timing Parameters)

Parameter	Symbol	Min.	Max.	Unit
SDA3n data setup time open drain mode	$V_{DD1218} = 1.8\text{ V}$ t_{SU_OD}	12	—	ns
	$V_{DD1218} = 1.2\text{ V}$	13.9	—	ns

Note: For timing parameters not listed in the table above, refer to the *MIPI Alliance Specification for I3C*.

Table 3.5-22 I3C Timing (Push-Pull Timing Parameters for SDR)

Parameter	Symbol	Min.	Max.	Unit
SCL3n clock frequency	$V_{DD1218} = 1.8\text{ V}$ f_{SCL}	0.01	12.5	MHz
	$V_{DD1218} = 1.2\text{ V}$	0.01	12.39	MHz
Clock in to data out for a slave	$V_{DD1218} = 1.8\text{ V}$ t_{SCO}	—	12	ns
	$V_{DD1218} = 1.2\text{ V}$	—	12.7	ns
SDA3n signal data setup in push-pull mode	$V_{DD1218} = 1.8\text{ V}$ t_{SU_PP}	12	N/A	ns
	$V_{DD1218} = 1.2\text{ V}$	13.9	N/A	ns

Note: For timing parameters not listed in the table above, refer to the *MIPI Alliance Specification for I3C*.

3.5.18 CANFD Interface Access Timing

Table 3.5-23 CANFD Interface Timing

Parameter		Symbol	CAN		CANFD		Unit	Figures
			Min.	Max.	Min.	Max.		
CANFD	Internal delay time	t_{node}^{*1}	—	100	—	50	ns	Figure 3.5-38
	Transmission rate	—	—	1	—	8	Mbps	

Note 1. Internal delay time (t_{node}) = Internal transmission delay time (t_{output}) + Internal reception delay time (t_{input})

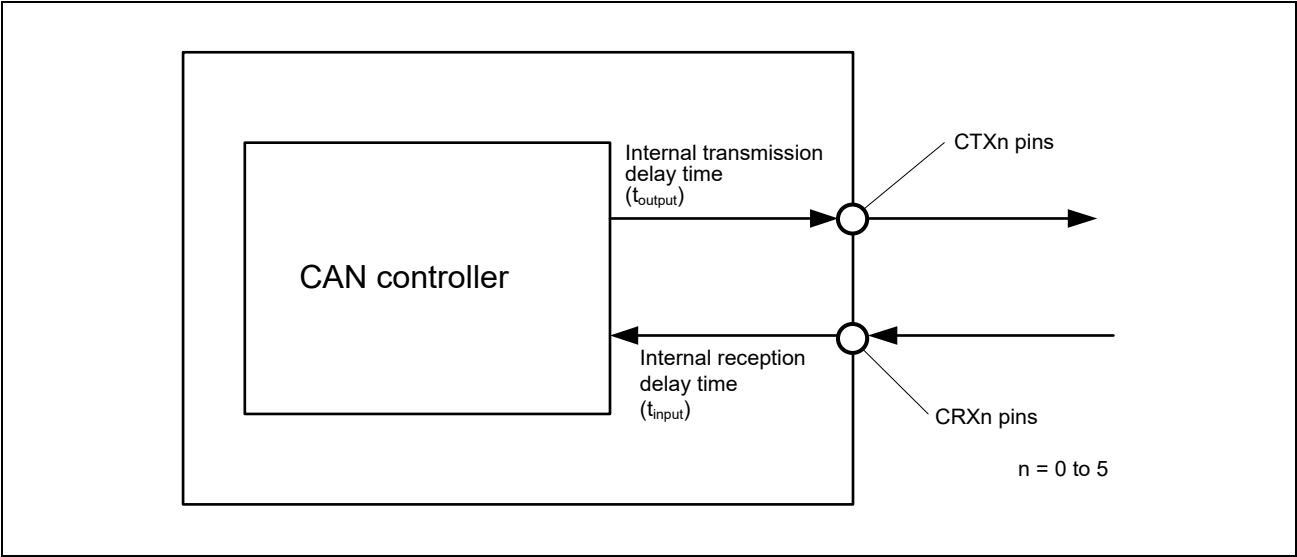


Figure 3.5-38 CANFD Interface Condition

3.5.19 A/D Converter Access Timing

Table 3.5-24 A/D Converter Trigger Timing

Parameter			Symbol	Min.	Max.	Unit*1	Figure
A/D converter	A/D converter trigger input pulse width	ADTRG	t _{TRGW}	1.5	—	t _{PADCyc}	Figure 3.5-39

Note 1. t_{PADCyc}: ADC_0_PCLK cycle

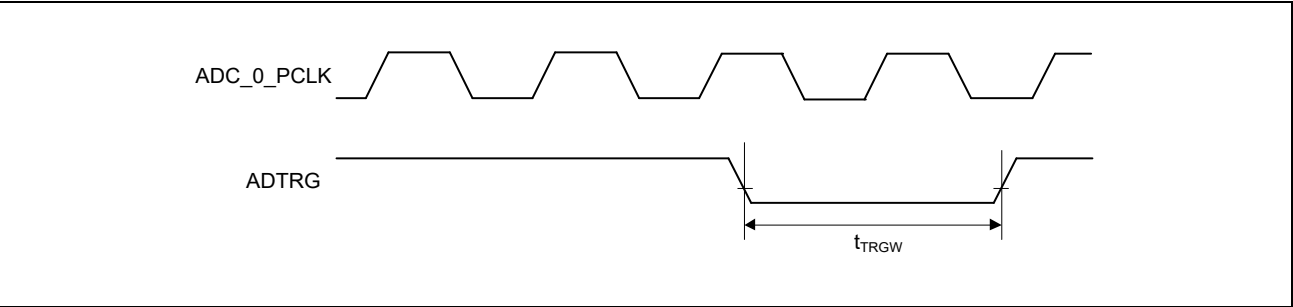


Figure 3.5-39 A/D Converter Trigger Input Timing (ADTRG)

3.5.20 SSIU Timing

Conditions:

$$V_{OH} = VDD18 \times 0.5, V_{OL} = VDD18 \times 0.5, C = 30 \text{ pF}^{*1} (1.8 \text{ V})$$

$$V_{OH} = VDD33 \times 0.5, V_{OL} = VDD33 \times 0.5, C = 30 \text{ pF}^{*1} (3.3 \text{ V})$$

Drive strength: $\times 1, \times 2, \times 4, \times 6$

Note 1. Other than t_{RC}: Rise-edge clock timing

Table 3.5-25 SSIU Signal Timing

Parameter	Symbol	Min.	Max.	Unit	Note	Figure
Output clock cycle	t _O	80	15625	ns	—	Figure 3.5-40
Input clock cycle	t _I	80	15625	ns	—	
Output clock high-cycle	t _{HC}	35 ^{*1}	—	ns	—	
Output clock low-cycle	t _{LC}	35 ^{*1}	—	ns	—	
Input clock high-cycle	t _{HC}	35	—	ns	—	
Input clock low-cycle	t _{LC}	35	—	ns	—	Figure 3.5-41 to Figure 3.5-44
Rise-edge clock timing	t _{RC}	—	20 ^{*2}	ns	Output (100 pF)	
Output delay	t _D	-5	19	ns	—	
Setup time	t _S	15	—	ns	—	
Hold time	t _H	5	—	ns	—	

Note 1. The width at high or low level of the clock signal when the input on AUDIO_CLKA, AUDIO_CLKB, or AUDIO_CLKC is output from SCK without frequency division in master mode is min. 30 ns.

Note 2. Output transition time from 20% to 80%

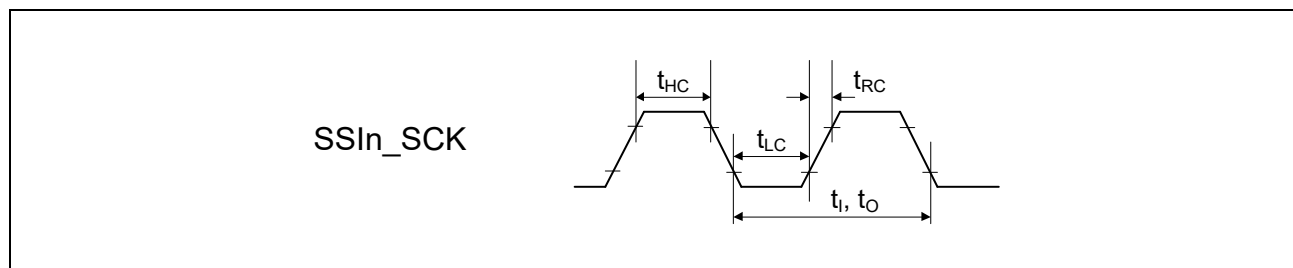


Figure 3.5-40 SCK Clock Input/Output Timing

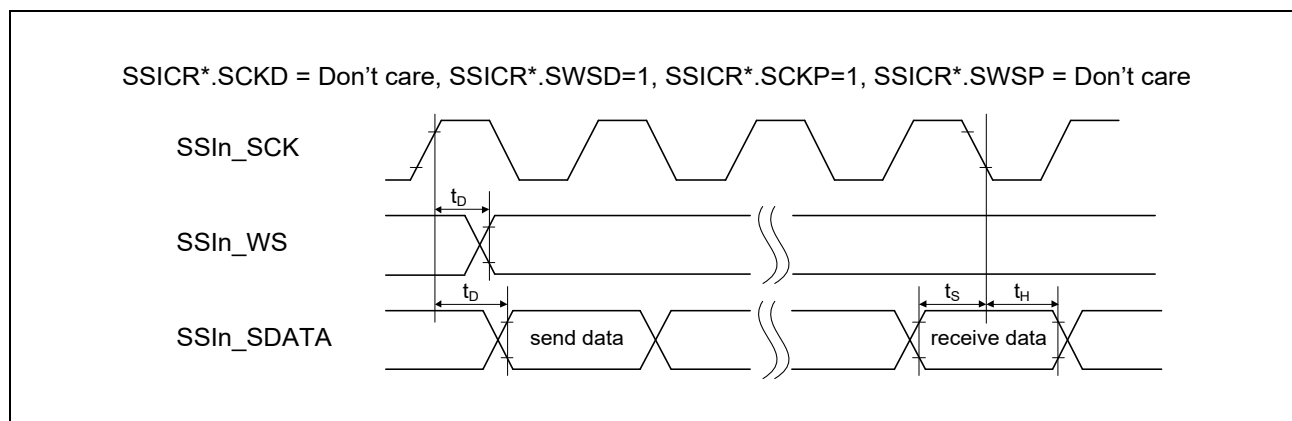


Figure 3.5-41 SSI Timing (1)

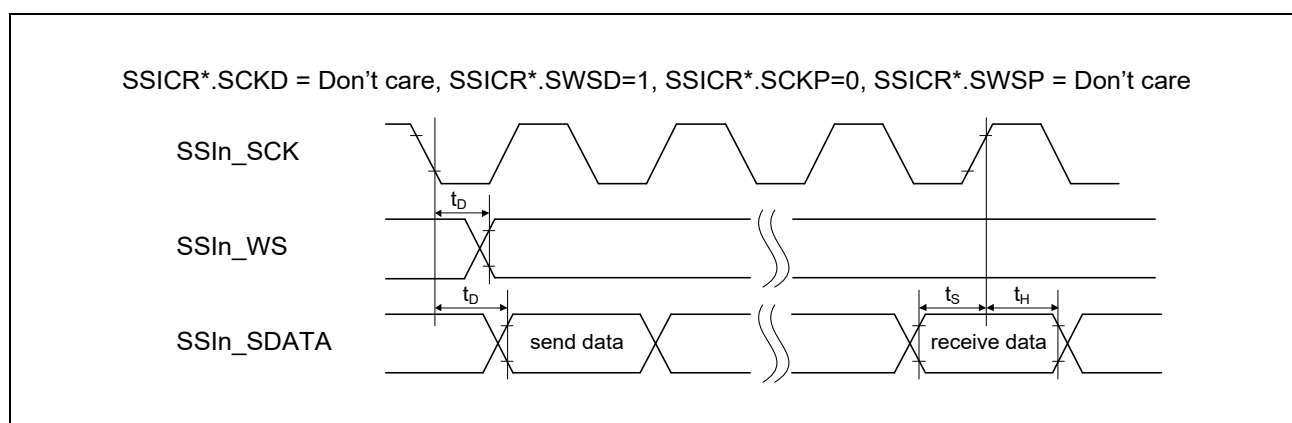


Figure 3.5-42 SSI Timing (2)

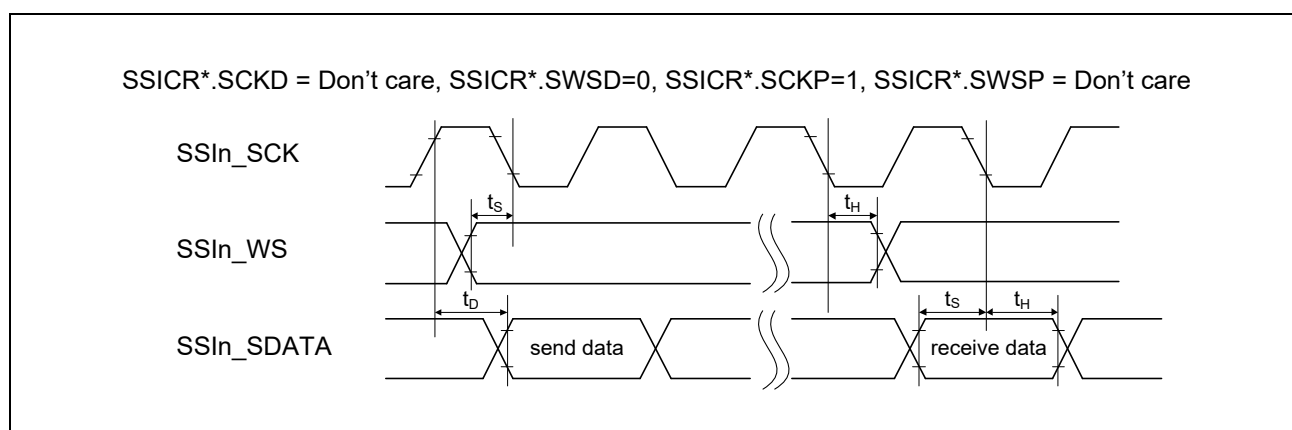


Figure 3.5-43 SSI Timing (3)

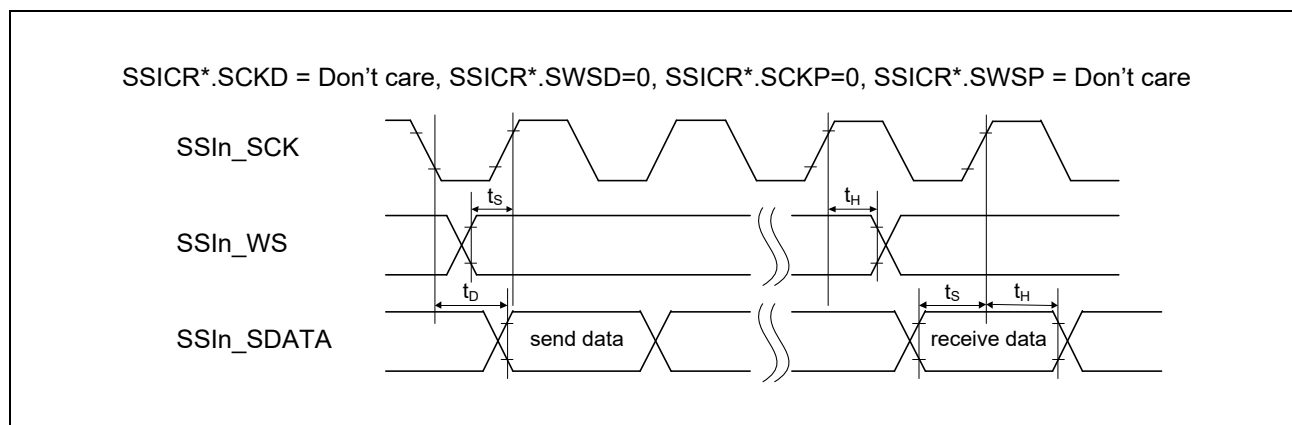


Figure 3.5-44 SSI Timing (4)

3.5.21 PDM Timing

Conditions:

$$V_{OH} = VDD18 \times 0.5, V_{OL} = VDD18 \times 0.5, C = 30 \text{ pF (1.8 V)}$$

$$V_{OH} = VDD33 \times 0.5, V_{OL} = VDD33 \times 0.5, C = 30 \text{ pF (3.3 V)}$$

Drive strength: $\times 1, \times 2, \times 4, \times 6$

Table 3.5-26 PDM Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Figure
Clock period	t_{PSYNC}	2	32	$t_{CCyc} = 208.33 \text{ ns}$ (4.8 MHz)* ¹	Figure 3.5-45
Clock high-level period	t_{PDCKWH}	$t_{PSYNC} \times 0.45$	$t_{PSYNC} \times 0.55$	ns	
Clock low-level period	t_{PDCKWL}	$t_{PSYNC} \times 0.45$	$t_{PSYNC} \times 0.55$	ns	
Clock rise time	t_{R-EDGE}	—	3* ²	ns	
Clock fall time	t_{F-EDGE}	—	3* ²	ns	
Setup time	t_{SU}	15	—	ns	Figure 3.5-46, Figure 3.5-47
Hold time	t_H	0	—	ns	

Note 1. t_{CCyc} is the period of PDMn core clock ($n = 0, 1$).

Note 2. Output transition time from 20% to 80%

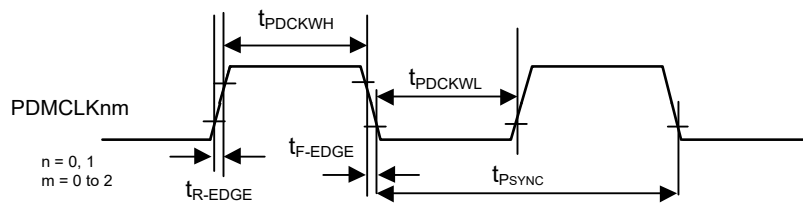


Figure 3.5-45 Timing of Clock Output (PDMCLKnm)

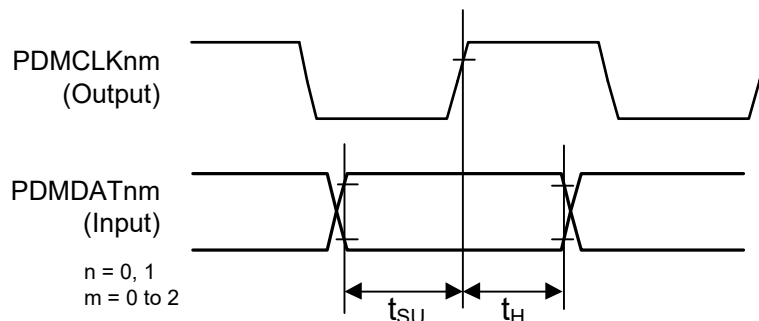


Figure 3.5-46 Timing of Clock Output (Synchronized with the rise of PDMCLKnm)

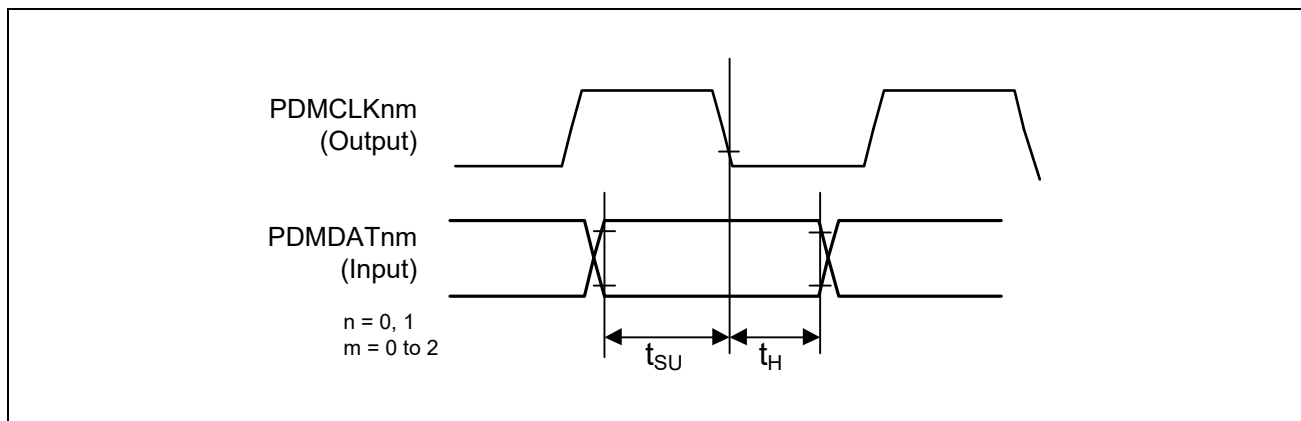


Figure 3.5-47 Timing of Clock Output (Synchronized with the fall of PDMCLKnm)

3.5.22 MIPI CSI-2 PHY Characteristics

The MIPI CSI-2 Rx D-PHY of this LSI is equivalent to the MIPI D-PHY Version 1.2.

For details, refer to the MIPI specification.

3.5.23 MIPI DSI Tx D-PHY Characteristics

The MIPI DSI Tx D-PHY of this LSI is compliant with the MIPI D-PHY Version 1.2.

For details, refer to the MIPI specification.

3.5.24 Control Signal Access Timing

Table 3.5-27 Control Signal Timing

Item	Symbol	Min.	Max.	Unit	Figures
QRESN pulse width	t_{RESW}	1	—	μs	Figure 3.5-48
TRSTN pulse width	t_{TRSW}	1	—	μs	
NMI pulse width	t_{NMIW}	20	—	t_{cyc}^{*1}	Figure 3.5-49
IRQ pulse width	t_{IRQW}	20	—	t_{cyc}^{*1}	
TINT pulse width	t_{TINTW}	20	—	t_{cyc}^{*1}	

Note 1. $t_{cyc} = 41.666 \text{ ns}$ (24 MHz)

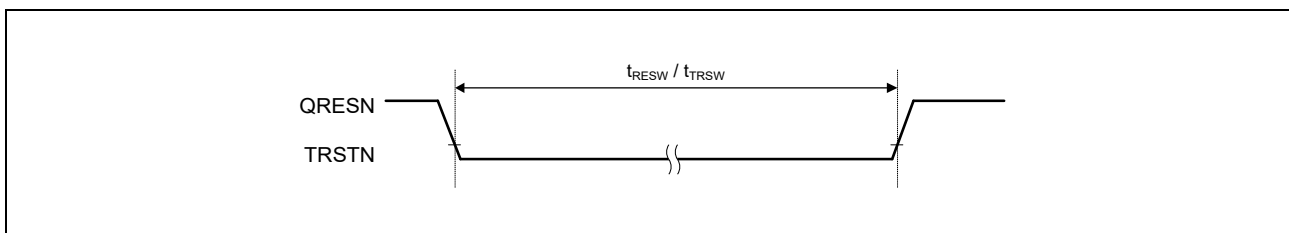


Figure 3.5-48 Reset Input Timing

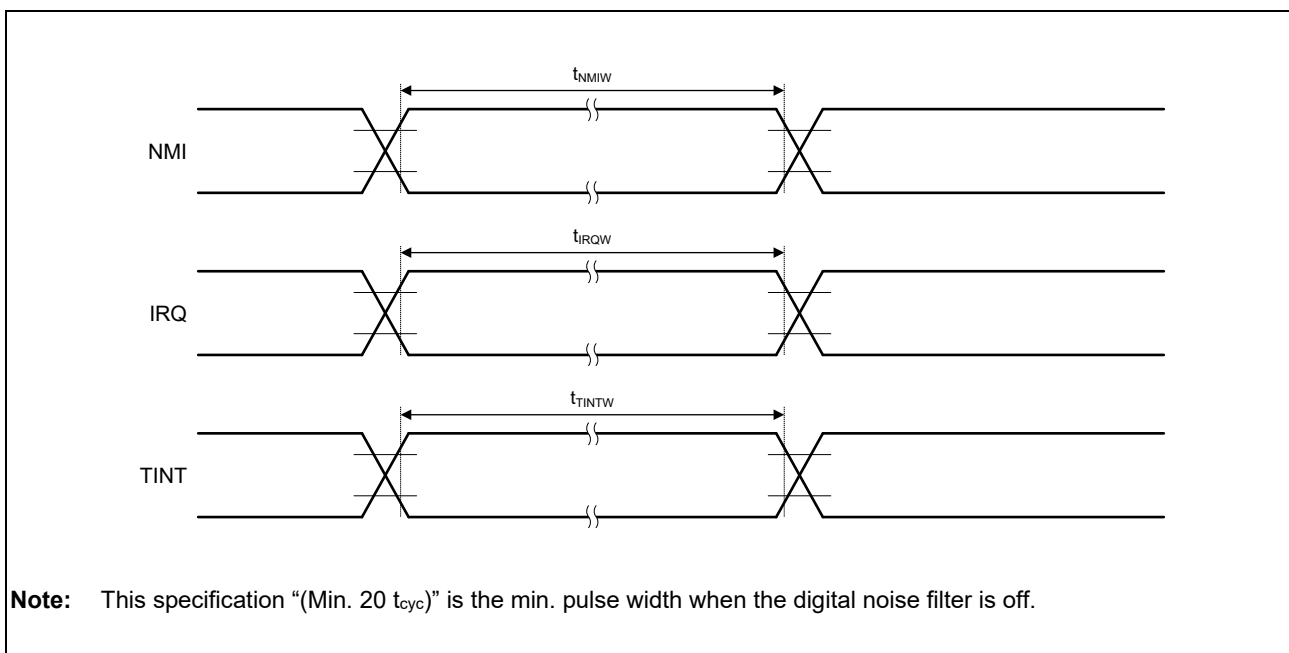


Figure 3.5-49 Interrupt Signal Input Timing

3.5.25 JTAG Debugger Interface Access Timing

Table 3.5-28 Debugger IF Timing

Item	Symbol	Min.	Max.	Unit	Figures
TCK_SWCLK cycle time	t_{TCKcyc}	50	—	ns	Figure 3.5-50
TCK_SWCLK high-level pulse width	t_{TCKH}	20	—	ns	Figure 3.5-51
TCK_SWCLK low-level pulse width	t_{TCKL}	20	—	ns	
TDI setup time	t_{TDIS}	15	—	ns	
TDI hold time	t_{TDIH}	15	—	ns	
TMS_SWDIO setup time	t_{TMSS}	15	—	ns	
TMS_SWDIO hold time	t_{TMSH}	15	—	ns	
TMS_SWDIO delay time	t_{SWDO}	—	14	ns	
TDO delay time	t_{TDOD}	—	14	ns	
Capture register setup time	t_{CAPTS}	10	—	ns	Figure 3.5-52
Capture register hold time	t_{CAPTH}	10	—	ns	
Update register delay time	$t_{UPDATED}$	—	20	ns	

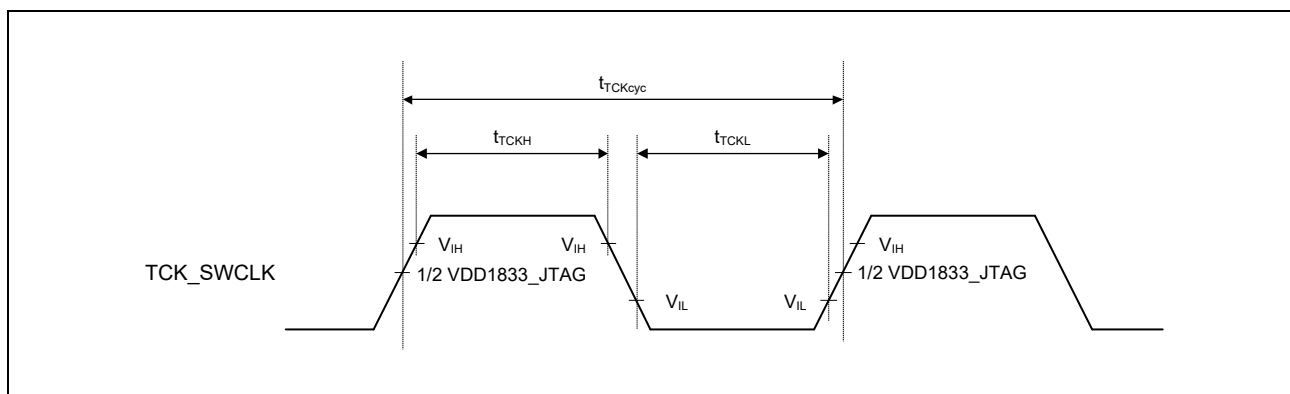


Figure 3.5-50 TCK_SWCLK Input Timing

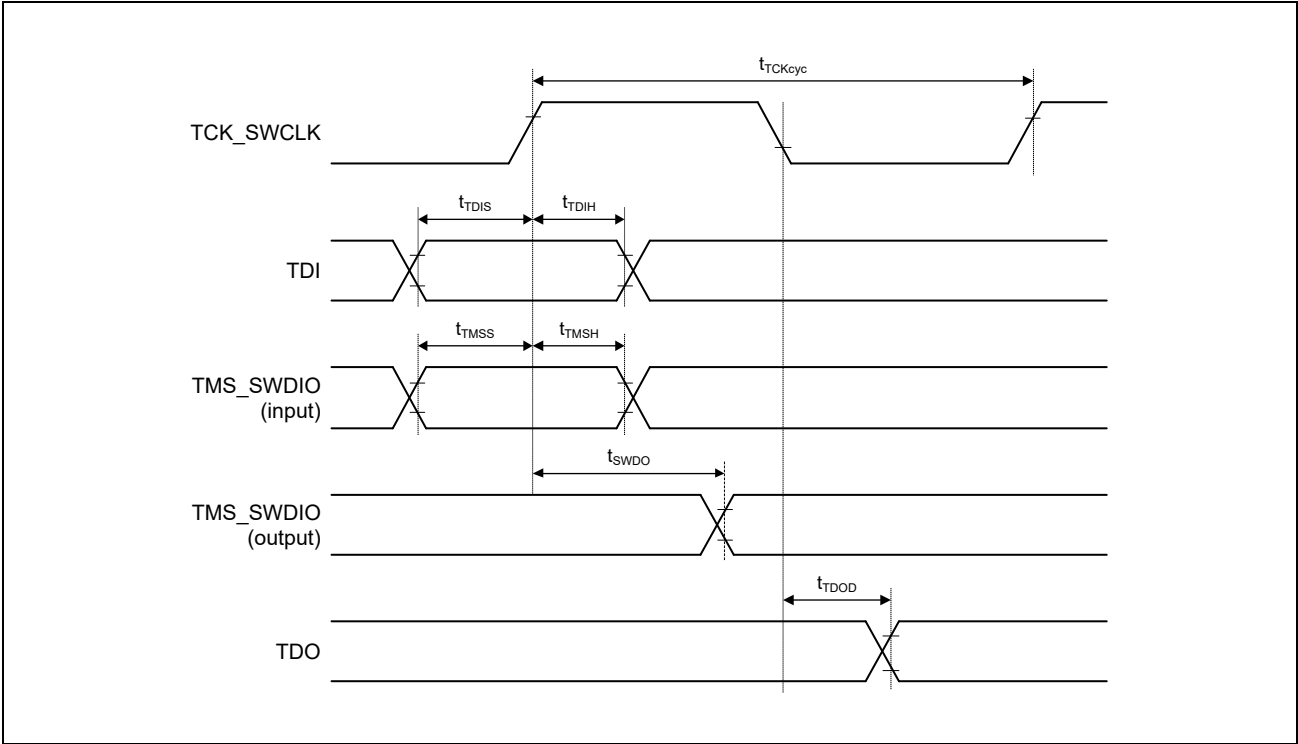


Figure 3.5-51 Data Transfer Timing

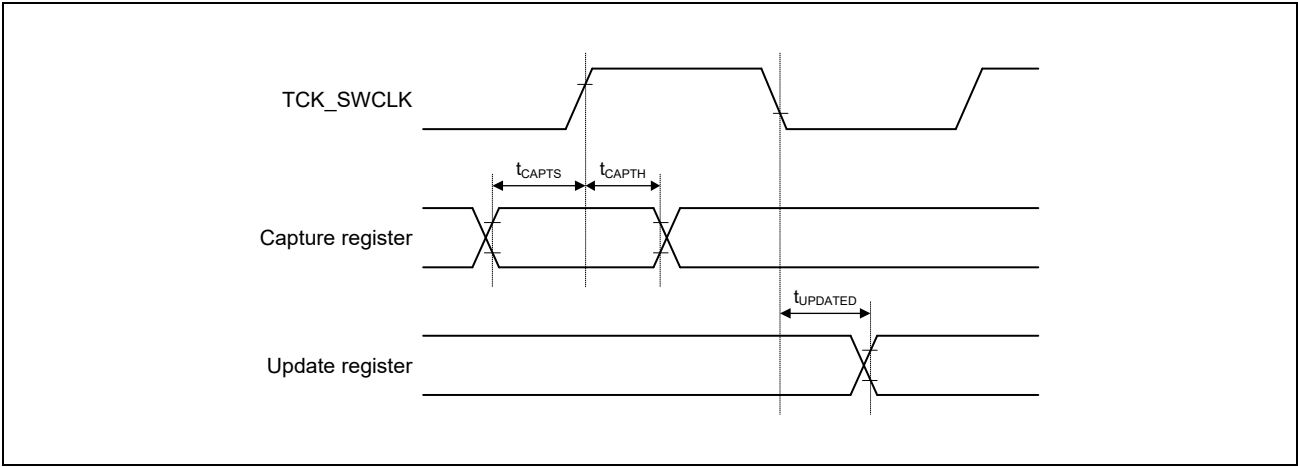


Figure 3.5-52 Boundary Scan Input/Output I/O Timing

3.6 Analog Characteristics

3.6.1 ADC Characteristics

Table 3.6-1 DC Characteristics

Item	Min.	Typ.	Max.	Unit
Resolution	—	12	—	Bit
Analog input capacitance	—	—	13	pF
Analog input range	0	—	ADAVDD18	V
Conversion time*1	0.4	—	4.0	μs
Permissible signal source impedance Max. = 1.0 kΩ				
Offset error	0	—	100	LSB
Full-scale error	-100	—	0	LSB
Quantization error	—	±0.5	—	LSB
DNL differential non-linearity error	—	—	±3.0	LSB
INL integral nonlinearity error	—	—	±6.0	LSB

Note 1. The conversion time is the total of the sampling time and the comparison time.

Table 3.6-2 Recommended External Input Resistance

Item	Symbol	Min.	Typ.	Max.	Unit
External input resistance*1 (ANI000-ANI007)	$R_{I_{ext}}$	—	—	1	kΩ

Note 1. Output resistance of signal generator + Series parasitic resistance between signal source and ADC input.

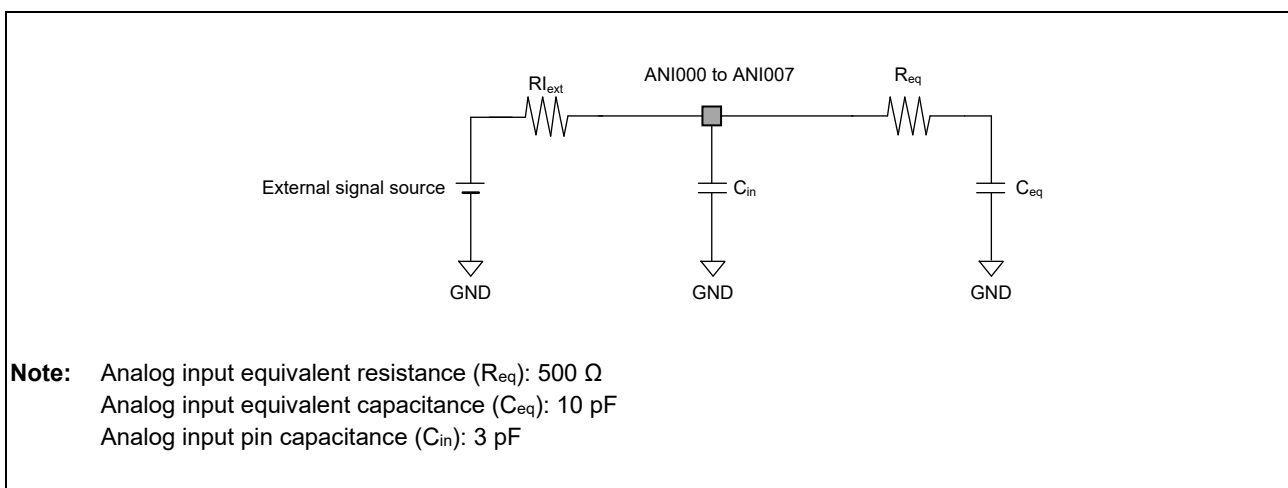


Figure 3.6-1 A/D Converter Equivalent Circuit and Peripheral Configuration Diagram

3.6.2 Temperature Sensor Characteristics

Table 3.6-3 Temperature Sensor Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Accuracy from -40°C to 125°C	Accm40_125	—	±3.0	±5.0	°C	—

3.7 Oscillation Circuits for Connecting Crystal Resonators (OSC)

This LSI chip includes three oscillation circuits (OSC) for connection to crystal resonators, specifically a 24-MHz crystal resonator for the system clock, a crystal resonator with a frequency range of 4 to 48 MHz for the audio clock, and a 32.768-kHz crystal resonator for the real-time clock. **Table 3.7-1** lists the pins for connecting the crystal resonators and the clock frequencies. **Figure 3.7-1** shows an example of the connections with crystal resonators.

Table 3.7-1 Pins for Connecting Crystal Resonators and Clock Frequency

External Pin Name	I/O	Clock Frequency
For the system clock		
QEXTAL	Input	24 MHz (frequency deviation: ±50 ppm)
QXTAL	Output	24 MHz
For the real-time clock		
RTXIN	Input	32.768 kHz (frequency deviation: ±50 ppm)
RTXOUT	Output	32.768 kHz
For the audio clocks		
AUDIO_EXTAL	Input	4 to 48 MHz
AUDIO_XTAL	Output	4 to 48 MHz

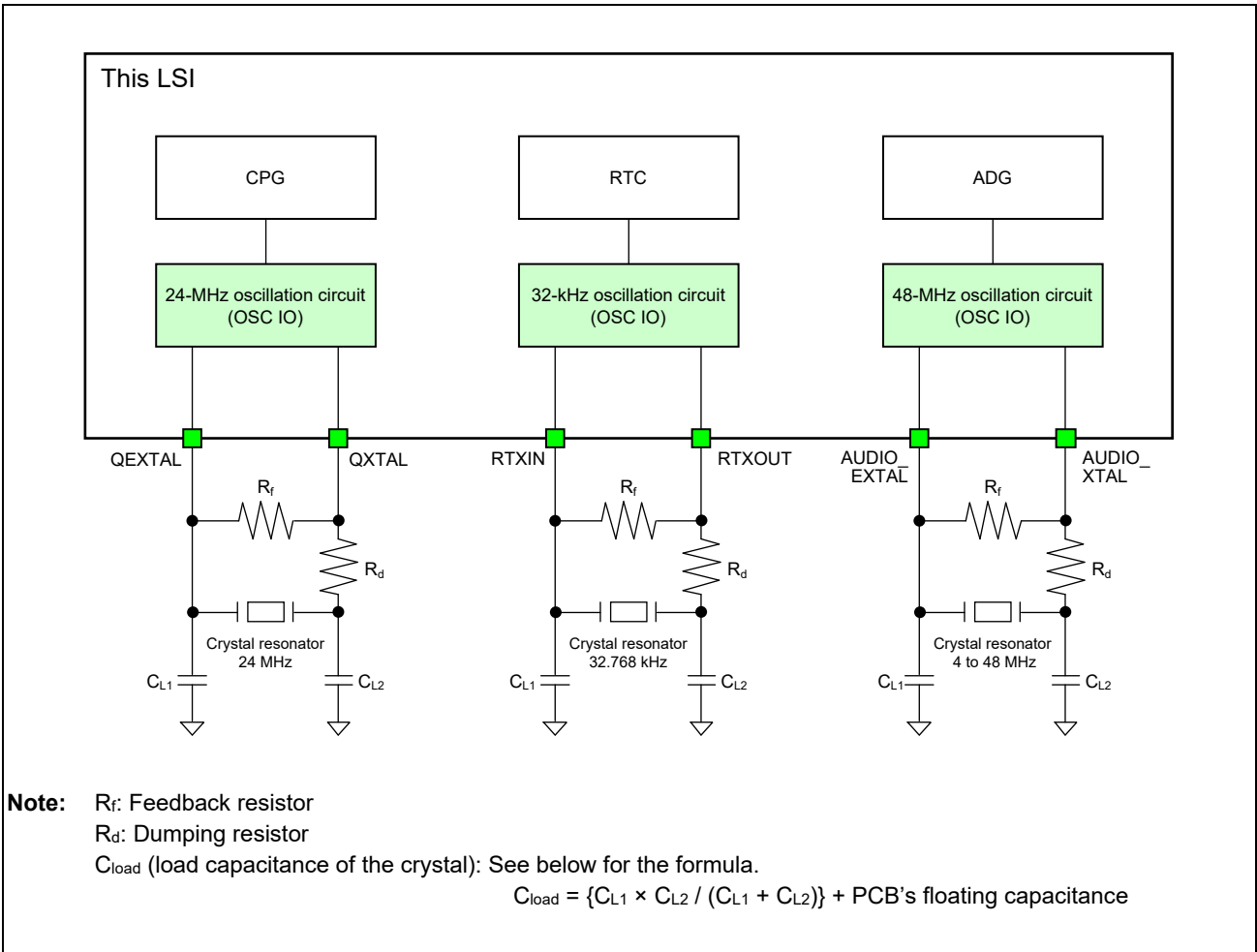


Figure 3.7-1 Example of Connections with Crystal Resonators

Place the crystal resonators and the capacitors C_{L1} and C_{L2} as close as possible to the pins to connect crystal resonators. To avoid interference and to ensure correct oscillation, the grounding points of the capacitors appended to the crystal resonators should be shared, and no wiring patterns should be placed near these components.

The characteristics of the crystal resonators are closely related to the design of the user board. Therefore, the user should sufficiently evaluate them with reference to the example of connection of crystal resonators in **Figure 3.7-1**.

The circuit rating of a crystal resonator depends on the crystal resonator and the stray capacitance of the mounting circuit. Therefore, contact the manufacturer of the crystal resonator before deciding upon the circuit rating. The user should thoroughly evaluate and then set the parameters (resistor and capacitor values).

Table 3.7-2 is a list of recommended values for the crystal resonators.

Table 3.7-2 Recommended Model Values for the Crystal Resonators

Clock Frequency	Model Values for the Crystal Resonators			
	Max. ESR* ¹	Max. C_L * ²	Max. C_0 * ³	Max. Drive Level
32.768 kHz	70 k Ω	12.5 pF	1.4 pF	1 μ W
24 MHz	60 Ω	12 pF	7 pF	100 μ W
48 MHz	50 Ω	10 pF	7 pF	100 μ W

Note 1. ESR means the equivalent series resistor of the crystal resonator.

Note 2. C_L is the load capacitance of the crystal resonator.

Note 3. C_0 is the parallel capacitance of the crystal resonator.

Section 4 Package Dimensions

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HFBGA1368-19x19-0.50	PRBG1368KA-A	2.9

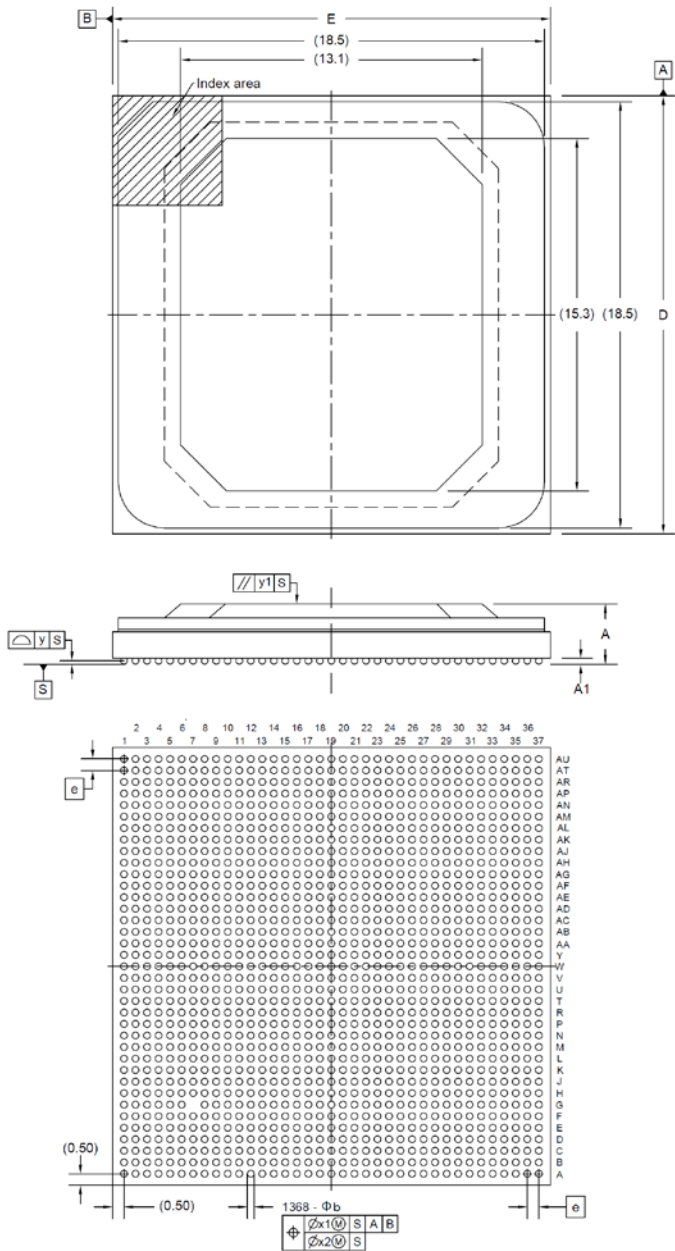


Figure 4-1 Package Dimensions

REVISION HISTORY	RZ/V2H Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Dec 25, 2023	—	First edition issued
1.10	Jun 28, 2024	3	Table 1.2-1 Product Lineup Note, added
		3	Modified "Kbytes" to "Kbyte" of CA55 in Table 1.3-1 CPU
		5	Table 1.3-3 On-chip SRAM and External Memory Interfaces For ECC function of DDR, Note1 added
		5	Modified SD to eSD in Table 1.1-5 Boot
		11	Modified "paring" to "pairing" of SSIU in Table 1.3-8 Audio
		17 to 57	Section 2 Pin, added
		58 to 133	Section 3 Electrical Characteristics, added
1.20	Mar 7, 2025	Section 1 Overview	
		4	Table 1.3-2 Accelerator Engines Image Scaling Unit, Video Codec Unit: The description, modified
		Section 2 Pin	
		42	Table 2.2-1 List of External Pins Note 11, added
		43	2.2.2 List of Multiplexed Functional Pins The main text, modified
		55	Table 2.3-1 List of Pin Functions (5/8) PCIE_REFCLKP0, PCIE_REFCLKN0, PCIE0_RSTOUTB: The function, modified
		Section 3 Electrical Characteristics	
		61	Table 3.1-1 Absolute Maximum Ratings Notes 3 and 5, modified
		67	Figure 3.3-2 Power-On/Power-Off Sequence (CM33 Boot) QRESN, modified Note, modified (The clock settling time → The clock stabilization time) Note, added
		69	Figure 3.3-3 Power-On/Power-Off Sequence (CA55 Boot) QRESN, modified Note, modified (The clock settling time → The clock stabilization time) Note, added
		71	Figure 3.3-4 Power-On Sequence (CM33 Boot Mode) Note, modified (The clock settling time → The clock stabilization time)
		75	Figure 3.3-6 Power-On Sequence (CA55 Boot Mode) Note, modified (The clock settling time → The clock stabilization time)
		84	3.5 AC Characteristics Conditions, modified
		87	3.5.5 DMAC Timing, added
		93	3.5.9 Ethernet Interface Timing Conditions, modified Drive strength, added
		93	Table 3.5-12 Ethernet Interface Timing (n = 0, 1) ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXER output delay time: The min. value, modified Note 1, added

Rev.	Date	Description	
		Page	Summary
1.20	Mar 7, 2025	97	Table 3.5-13 xSPI Timing (2/2) CS low to DS low: The max. value, modified Notes 5 and 6, added
		100	3.5.14 Serial Communications Interface (RSCI) Access Timing Drive strength, modified
		101	Table 3.5-15 RSCI Timing (2/2) RSCI (Clock sync, Simple SPI) and SCK clock rise/fall time, deleted RSCI (Clock sync, Simple SPI), Input clock rise time, Input clock fall time, Output clock rise time, and Output clock fall time, added
		102	Figure 3.5-23 RSCI Simple SPI Mode Clock Timing, modified
		105	Table 3.5-16 RSPI Timing SSL Activation to Data Output Delay, added Notes 1, 2, 3, and 4, modified
		106	Figure 3.5-28 RSPI Clock Timing, modified Figure 3.5-29 RSPI Timing (Master, Motorola RSPI, CPHA = 0), modified
		112	Table 3.5-18 I3C Timing Note 1, modified
		113	Table 3.5-19 IIC Timing (Fast-mode+) Note 1, modified
		114	Table 3.5-20 IIC Timing (HS mode) SCL3n cycle time: The min. values under "Cb = 100 pF" and "Cb = 400 pF", modified Note 1, modified
		116	Table 3.5-21 I3C Timing (Open Drain Timing Parameters) SCL3n clock High period: The min. value and note, modified Clock before STOP (P) condition: The min. value, modified Notes 3 and 4, added
		117	Table 3.5-22 I3C Timing (Push-Pull Timing Parameters for SDR) SCL3n clock High period for Mixed Bus, added Note 3, added
		126	3.5.20 SSIU Timing Condition, modified Drive strength, added
		126	Table 3.5-25 SSIU Signal Timing Note 2, added
		129	3.5.21 PDM Timing Conditions, modified Output load conditions, deleted Drive strength, added
		129	Table 3.5-26 PDM Interface Timing Note 2, added
1.30	Sep 5, 2025	Section 1 Overview	
		14	Figure 1.4-1 Block Diagram, modified (The number of GPT channels, modified)
		15	Table 1.4-1 List of Units (1/2): GPT: Unit Number, modified (each 16 ch. → each 8 ch.)
		Section 3 Electrical Characteristics	
		62	Table 3.2-1 Recommended Operating Range (1/3): PD_OTHERS: VDD33_OTHERS: The Min and Max values, modified
		72	Figure 3.3-5 Power-Off Sequence (CM33 Boot Mode), modified
		82	Table 3.4-2 DC Characteristics: Low-level output voltage: 3.3/1.8-V switching I/O type 2 (3.3V): Symbol, Max, and Condition, modified
		97	Table 3.5-13 xSPI Timing (2/2): DS low to CS high: Min, modified. CK low to DS low, added. Notes 7 to 9, added.

Rev.	Date	Description	
		Page	Summary
1.30	Sep 5, 2025	99	Figure 3.5-19 DS to CS Signal Timing, modified (t_{CKLDSL} , added)
		110	3.5.16 Renesas IIC Bus Interface (RIIC) Access Timing: Conditions, deleted
		110, 111	Table 3.5-16 RIIC Timing: Parameter: The entire column, modified. Note 1, modified. Notes 3 and 6, added. The number of Note, modified (Note 3 → Note 5).
		112	3.5.17 I3C Timing: Conditions, deleted
		112	Table 3.5-17 IIC Timing: The table title, modified. Note 2, added.
		113	Table 3.5-18 IIC Timing (Fast-mode+): Note 2, added
		114	Table 3.5-19 IIC Timing (HS mode): The column title, modified ($C_b = 100\text{ pF} \rightarrow C_b = 100\text{ pF (Max.)}$). The symbols of SCL3n rise time, SCL3n rise time after a repeated START condition and after an acknowledge bit, SDA3n rise time, SCL3n fall time, and SDA3n fall time, modified. Note 2, modified. Note 3, added.
		117	Table 3.5-21 I3C Timing (Push-Pull Timing Parameters for SDR): The symbol of SCL3n clock frequency, modified. Note 1, modified.
		129	Table 3.5-25 PDM Interface Timing: Note 1, modified
		136	3.7 Oscillation Circuits for Connecting Crystal Resonators (OSC): The main text, modified
1.40	Jul 31, 2026	Section 1 Overview	
		4	Table 1.3-2 Accelerator Engines: Video Codec Unit: The description, modified
		6	Table 1.3-5 System, Data Transfer, Enhanced Interrupt Controller Unit, Clock Functions: Message Handling Unit: The description, modified
		7	Table 1.3-6 Various Communication/Storage/Network Interfaces (1/3), modified (PCIe Express® 3.0 → PCI Express® 3.0)
		9	Table 1.3-6 Various Communication/Storage/Network Interfaces (3/3): Renesas Serial Peripheral Interface: Data formats: The description, modified. CRC Calculator: The description, modified (four generating polynomials → five generating polynomials).
		12	Table 1.3-12 General-Purpose I/O Pins: General-purpose I/O ports: The description, modified
		15	Table 1.4-1 List of Units (1/2): PCIe: The function, modified (PCIe Express 3.0 interface → PCI Express 3.0 interface)
		Section 2 Pin	
		30, 31, 42	Table 2.2-1 List of External Pins: Notes 12 and 13, added
		53	Table 2.3-1 List of Pin Functions (3/8): DDR memory interface channel 0, 1: The function, modified
		54	Table 2.3-1 List of Pin Functions (4/8): USB2.0 channel 0: USB20_TXRTUNE: The function, modified
		54	Table 2.3-1 List of Pin Functions (4/8): USB2.0 channel 1: USB21_TXRTUNE: The function, modified
		54	Table 2.3-1 List of Pin Functions (4/8): USB3.2 channel 0, 1: USB30_TXRTUNE and USB31_TXRTUNE: The function, modified
		55	Table 2.3-1 List of Pin Functions (5/8): PCIe Gen3: PCIE_REFCLKP0, PCIE_REFCLKN0, and PCIE0_RSTOUTB: The function, modified (41-lane × 1 mode → 4-lane × 1 mode)
		57	Table 2.3-1 List of Pin Functions (7/8), modified (Pulse density modulation interface (PDM) channel n (n = 0 to 6) → Pulse density modulation interface (PDM) channel n (n = 0 to 5))
		59 to 61	2.4 Handling of Unused I/Os and Power Pins, added
		Section 3 Electrical Characteristics	
		64	Table 3.1-1 Absolute Maximum Ratings (3/3): Input voltage (1.2-V I/O), Input voltage (1.8-V I/O), Input voltage (1.8-V I/O (3.3-V tolerant)), and Input voltage (3.3-V I/O): The max. values, modified. Note 5, deleted.
		70	Figure 3.3-2 Power-On/Power-Off Sequence (CM33 Boot): Note, modified
		72	Figure 3.3-3 Power-On/Power-Off Sequence (CA55 Boot): Note, modified
		74	Figure 3.3-4 Power-On Sequence (CM33 Boot Mode): Note, modified
		78	Figure 3.3-6 Power-On Sequence (CA55 Boot Mode): Note, modified

Rev.	Date	Description	
		Page	Summary
1.40	Jul 31, 2026	81	Table 3.4-1 Max. Supply Currents during Operation (2/3) : CRU0, CRU1, CRU2, and CRU3: 0.8-V core power supply current: The symbols, modified.
		82	Table 3.4-1 Max. Supply Currents during Operation (3/3) : CPG: PLLVDO_DSI 1.8-V power supply current and PLLVDO_DSI 0.8-V power supply current: The symbols, modified.
		83	Table 3.4-2 DC Characteristics V _{DD} = 1.14 V to 1.89 V (1.8/1.2-V switching I/O type), V _{DD} = 1.71 V to 1.89 V (1.8-V I/O type and 1.8-V OSC I/O type), V _{DD} = 1.71 V to 3.46 V (3.3/1.8-V switching I/O types 1, 2 and 3), V _{DD} = 3.14 V to 3.46 V (3.3-V I/O type) (1/4): The table title, modified. External voltage tolerance, deleted. High-level input voltage: 3.3/1.8-V switching I/O type 2: The max. value, modified.
		84	Table 3.4-2 DC Characteristics V _{DD} = 1.11 V to 1.95 V (1.8/1.2-V switching I/O type), V _{DD} = 1.65 V to 1.95 V (1.8-V I/O type and 1.8-V OSC I/O type), V _{DD} = 1.65 V to 3.60 V (3.3/1.8-V switching I/O types 1, 2 and 3), V _{DD} = 3.00 V to 3.60 V (3.3-V I/O type) (2/4) Input pull-down resistor current and Input pull-up resistor current: The symbols, modified.
		87	Table 3.5-1 Clock Timing Table: Oscillation stabilization time and QEXTAL stable clock input to QRESN rise, added. Mode hold time and Mode setup time: The min and max values, modified. Note 1, added.
		87	Table 3.5-2 QEXTAL Input Clock Jitter Table, added
		88	Figure 3.5-2 Power-On Oscillation Settling Time, modified
		111	Figure 3.5-30 RSPI Timing (Master, Motorola RSPI, CPHA = 1), modified (t _{OH} → t _{OD}) (t _{OD} → t _{OH})
		113	Figure 3.5-34 RSPI Timing (Slave, TI-SSP, with delay in burst transfer): MOSI _x output, modified
		114	Table 3.5-17 RIIC Timing: RIIC (Standard-mode): SCL, SDA capacitive load: Note 5, added
		119	Table 3.5-21 I3C Timing (Open Drain Timing Parameters), modified. Table 3.5-22 I3C Timing (Push-Pull Timing Parameters for SDR), modified
		—	Figure 3.5-38 t _{DIG_H} and t _{DIG_L} , Figure 3.5-39 I3C Data Transfer – ACK by Slave, Figure 3.5-40 I3C START Condition Timing, Figure 3.5-41 I3C STOP Condition Timing, Figure 3.5-42 I3C Master Out Timing, Figure 3.5-43 I3C Slave Out Timing, Figure 3.5-44 Master SDR Timing, Figure 3.5-45 T-Bit When Master Ends Read with Repeated START and STOP, and Figure 3.5-46 I3C Timing, deleted

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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Trademarks (continued)

For the “Cortex” notation, it is used as follows;

— Arm® Cortex®-A55

— Arm® Cortex®-R8

— Arm® Cortex®-M33

Note that in each section of the Manual, this may be noted as Cortex-A55, Cortex-R8 and Cortex-M33 respectively.

Examples of trademark or registered trademark used in the document of RZ/V2H;

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