RZ/T1-M Group

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450 MHz, MCU with Arm® Cortex®-R4, on-chip FPU, 747 DMIPS, up to 1 Mbyte of on-chip extended SRAM, MDIO I/F, various communications interfaces such as an SPI multi-I/O bus controller, safety functions, and security functions*1

Features

■ On-chip 32-bit Arm Cortex-R4 processor
- High-speed realtime control with maximum operating frequency of 450 MHz
  Capable of 747 DMIPS (in operation at 450 MHz)
- On-chip 32-bit Arm Cortex-R4 (revision r1p4)
- Tightly coupled memory (TCM) with ECC: 512 Kbytes/32 Kbytes
- Instruction cache/data cache with ECC: 8 Kbytes per cache
- High-speed interrupt
- The FPU supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single-precision and double-precision.
- Harvard architecture with 8-stage pipeline
- Supports the memory protection unit (MPU)
- Arm CoreSight architecture, includes support for debugging through JTAG and SWD interfaces

■ Low power consumption
- Standby mode and module stop function

■ On-chip extended SRAM
- Up to 1 Mbyte of the on-chip extended SRAM with ECC
- 150 MHz

■ Data transfer
- DMAC: 16 channels × 2 units

■ Event link controller
- Module operations can be started by event signals rather than by interrupt handlers.
- Linked operation of modules is available even while the CPU is in the sleep state.

■ Reset and power supply voltage control
- Three reset sources including a pin reset
- Dual power-voltage configuration: 3.3 V, 1.2 V (I/O unit), 1.2 V (internal)

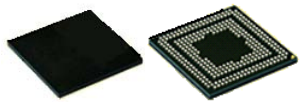
■ Clock functions
- Oscillator input frequency: 25 MHz
- CPU clock frequency: Up to 450 MHz
- Low-speed on-chip oscillator (LOCO): 240 kHz

■ Independent watchdog timer
- Operated by a clock signal obtained by frequency-dividing the clock signal from the low-speed on-chip oscillator: Up to 120 kHz

■ Safety functions
- Register write protection, input clock oscillation stop detection, CRC, IWDTa, and A/D self-diagnosis
- An error control module is incorporated to generate a pin signal output, interrupt, or internal reset in response to errors originating in the various modules.

■ Security functions (optional)*2
- Boot mode with security through encryption

■ Management data input/output interface (MDIO)
- An interface embedded in the optical transceiver modules which are compliant to the CFP MSA specifications: 1 channel (slave)
  Maximum operating frequency: 4 MHz
- Interface for DSP control: 2 channels (1 for slave operation, 1 for master operation*1)
  Maximum operating frequency: 10 MHz



PLBG0112KA-A

■ Various communications interfaces
- SCIFA with 16-byte transmission and reception FIFOs: 4 channels
- I^2C bus interface: 2 channels for transfer at up to 400 kbps
- RSPIa: 2 channels
- SPIBSC: Provides a single interface for multi-I/O compatible serial flash memory

■ Up to 12 extended-function timers
- 16-bit TPUa (6 channels): Input capture, output compare, PWM waveform output
- 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converters
- 12 bits × 2 units (max.)
  (8 channels for unit 0; 8 channels for unit 1)
- Self diagnosis
- Detection of analog input disconnection

■ Temperature sensor for measuring temperature within the chip

■ General-purpose I/O ports
- 5-V tolerance, open drain, input pull-up

■ Multi-function pin controller
- The locations of input/output functions for peripheral modules are selectable from among multiple pins.

■ Operating temperature range
- Tj = -40°C to +110°C
  Tj: Junction temperature

Note 1. Optional
Note 2. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.

1. Overview

1.1 Outline of Specifications

This LSI circuit is a high-performance MCU equipped with the Arm® Cortex®-R4 (CR4) processor with FPU, and incorporating integrated peripheral functions necessary for system configuration. Table 1.1 lists the specifications in outline.

Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	Central processing unit (Cortex-R4)	• Maximum operating frequency 112-pin FBGA: 450 MHz • 32-bit CPU Cortex-R4 designed by Arm (core revision r1p4) • Address space: 4 Gbytes • Instruction cache: 8 Kbytes (with ECC) • Data cache: 8 Kbytes (with ECC) • Tightly coupled memory (TCM) ATCM: 512 Kbytes (with ECC) BTCM: 32 Kbytes (with ECC) • Instruction set: Arm v7-R architecture, so support includes Thumb® and Thumb-2 • Data arrangement Instructions: Little endian Data: Little endian • Memory protection unit (MPU)
	FPU (Cortex-R4)	• Supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single- and double-precision. • Registers 32-bit single-word registers: 32 bits × 32 (can be used as 16 double-word registers: 64 bits × 16)
Memory	On-chip extended SRAM with ECC	• Capacity: Up to 1 Mbyte • Operating frequency: 150 MHz • SEC-DED (single error correction/double error detection)
Operating modes		• Boot mode SPI boot mode (for booting up from serial flash memory)
Clock	Clock generation circuit	• An external resonator can be used as the input clock. • Detection of input clock oscillation stopping • The following clocks are generated. CPU clock: 450 MHz (max.) System clock: 150 MHz (fixed) High-speed peripheral module clock: 150 MHz (fixed) Low-speed peripheral module clock: 75 MHz (fixed) ADCCLK in the 12-bit A/D converter (S12ADCa): 60 MHz (max.) Low-speed on-chip oscillator: 240 kHz (fixed)
Reset		RES# pin reset, error control module (ECM) reset, software reset
Low power	Low-power consumption function	• Standby mode • Module stop function
Interrupt	Vector interrupt controller (VIC)	• Peripheral function interrupts: 96 sources • External interrupts: 8 sources (NMI, IRQ0 to IRQ4, IRQ6, and IRQ7 pins) • Non-maskable interrupts: 2 sources • Sixteen levels specifiable for the order of priority
Data transfer	Direct memory access controller (DMAC)	• 2 units (16 channels for unit 0, 16 channels for unit 1) • Transfer modes: Single transfer mode and block transfer mode • Transfer size Unit 0: 1/2/4/16/32/64 bytes Unit 1: 1/2/4/16 bytes • Activation sources: External interrupts, on-chip peripheral module requests, and software requests

Table 1.1 Outline of Specifications (2 / 4)

Classification	Module/Function	Description
I/O ports	General-purpose I/O ports	• 112-pin FBGA I/O pins: 51 (including seven 1.2-V I/O pins) Input pins: 4 Pull-up/pull-down resistors: 44 5-V tolerance: 4
Event link controller (ELC)		• Event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event link operation is possible for port E.
Multi-function pin controller (MPC)		The locations of input/output functions are selectable from among multiple pins.
Timers	16-bit timer pulse unit (TPUa)	• 16 bits × 6 channels • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Input capture/output compare function • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Digital noise filtering of signals from the input capture pins • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Event linking by the ELC (channel 1 of unit 0 only)
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Digital noise filter function for signals on the input capture pins • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among six counter-input clock signals for each channel (with maximum operating frequency of 75 MHz)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Low-speed on-chip oscillator (LOCO)/2 Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 (with maximum operating frequency of 120 kHz)

Table 1.1 Outline of Specifications (3 / 4)

Classification	Module/Function	Description
Communication function	Serial communication interface with FIFO (SCIFA)	• 4 channels • Serial communications modes: Asynchronous, clock synchronous*2 • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Both the transmission and reception sections are equipped with 16-byte FIFO buffers, allowing continuous transmission and reception. • Bit rate modulation
	I2C bus interface (RIICa)	• 2 channels • Supports I2C bus format • Supports the multi-master • Max. transfer rate: 400 kbps • Event linking by the ELC
	Management data input/ output interface (MDIO)	• 2 channels (1 for slave operation, 1 for master operation*3) Slave: Interface for an optical transceiver module compliant with the CFP MSA specification Master: Interface for DSP control
	Serial peripheral interface (RSPIa)	• 2 channels • RSPI transfer facility Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped automatically with the reception buffer full for master reception • Event linking by the ELC
	SPI multi I/O bus controller (SPIBSC)	• 1 channel • One serial flash memory with multiple I/O bus sizes (single/dual/quad) can be connected. • External address space read mode (built-in read cache) • SPI operating mode • Clock polarity and clock phase can be selected. • Maximum transfer rate: 300 Mbps (for quad)

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
12-bit A/D converter (S12ADCa)		• 12 bits × 2 units (unit 0: 8 channels, unit 1: 8 channels) • 12-bit resolution • Conversion time VREFH0, VREFH1 = 3.0 to 3.6 V Unit 0: 0.483 µs per channel Unit 1: 0.883 µs per channel VREFH0, VREFH1 = 2.5 to 3.0 V Unit 0: 0.883 µs per channel Unit 1: 0.883 µs per channel • Operating mode Scan mode (single scan mode, continuous scan mode, or group scan mode) Group A priority control (only for group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (4 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: VREFL1, VREFH1 × 1/2, VREFH1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (TPUa) trigger, external trigger • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ±1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 0).
Safety	Register write protection function	Protects important registers from being overwritten in cases where a program runs out of control.
	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (32-Ethernet), $X^{16} + X^{12} + X^5 + 1$ (16-CCITT), $X^8 + X^4 + X^3 + X^2 + 1$ (8-SAEJ1850), $X^8 + X^5 + X^3 + X^2 + X + 1$ (8-0x2F)
	Input clock oscillation stop function	Input clock oscillation stop detection: Available
	Clock monitor circuit (CLMA)	Monitors the abnormal output clock frequency from the PLL circuit or low-speed on-chip oscillator.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
	Error control module (ECM)	• Generates an interrupt or internal reset for the error signal input from each module. • Time-out function • The error control is duplicated in the master and the checker.
Security	Secure boot mode*1	As an option, a boot mode with encryption as a security function is available.
Power supply voltage		VDD = PLLVDD0 = PLLVDD1 = VCCQ12 = 1.14 to 1.26 V VCCQ33 = AVCC0 = AVCC1 = 3.0 to 3.6 V VREFH0 = VREFH1 = 2.5 to 3.6 V
Operating temperature		Tj = -40 to +110°C
Package		112-pin FBGA: 6 × 6 mm, 0.5-mm pitch PLBG0112KA-A
Debugging interface		• CoreSight architecture designed by Arm • Debugging function by the JTAG/SWD interface, and trace function by the trace port/ SWV interface

Note 1. See Table 1.3, List of Products, for the products that have the secure boot mode. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.

Note 2. Channel 4 is used only in asynchronous mode.
Note 3. The MDIO master is optional. For the products which have it, see Table 1.3, List of Products.

Table 1.2 List of Functions

Module/Function		RZ/T1-M Group 112 Pins
Interrupt	External interrupt	NMI, IRQ0 to IRQ4, IRQ6, IRQ7
DMA	DMA controller (DMAC)	ch0 to ch31
Timers	16-bit timer pulse unit (TPUa)	ch0 to ch5
	Compare match timer (CMT)	ch0 to ch3
	Compare match timer W (CMTW)	ch0, ch1
	Watchdog timer (WDTA)	ch0
	Independent watchdog timer (IWDTa)	Available
Communication function	Serial communications interface with FIFO (SCIFA)	ch0 to ch2, ch4*3
	Management data input/output interface (MDIO master*1/MDIO slave)	Available
	I^2C bus interface (RIICa)	ch0, ch1
	Serial peripheral interface (RSPIa)	ch0, ch1
	SPI multi I/O bus controller (SPIBSC)	ch0
12-bit A/D converter (S12ADCa)		AN000 to AN007 (unit 0) AN100 to AN107 (unit 1)
Temperature sensor		Available
CRC calculator (CRC)		Available
Data operation circuit (DOC)		Available
Clock monitor circuit (CLMA)		Available
Secure boot mode*2		Optional
Event link controller (ELC)		Available

Note 1. The MDIO master is optional. For the products which have it, see Table 1.3, List of Products.
Note 2. See Table 1.3, List of Products, for the products that have the secure boot mode. Details of this function will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.
Note 3. Channel 4 is used only in asynchronous mode.

1.2 List of Products

Table 1.3 is a list of products.

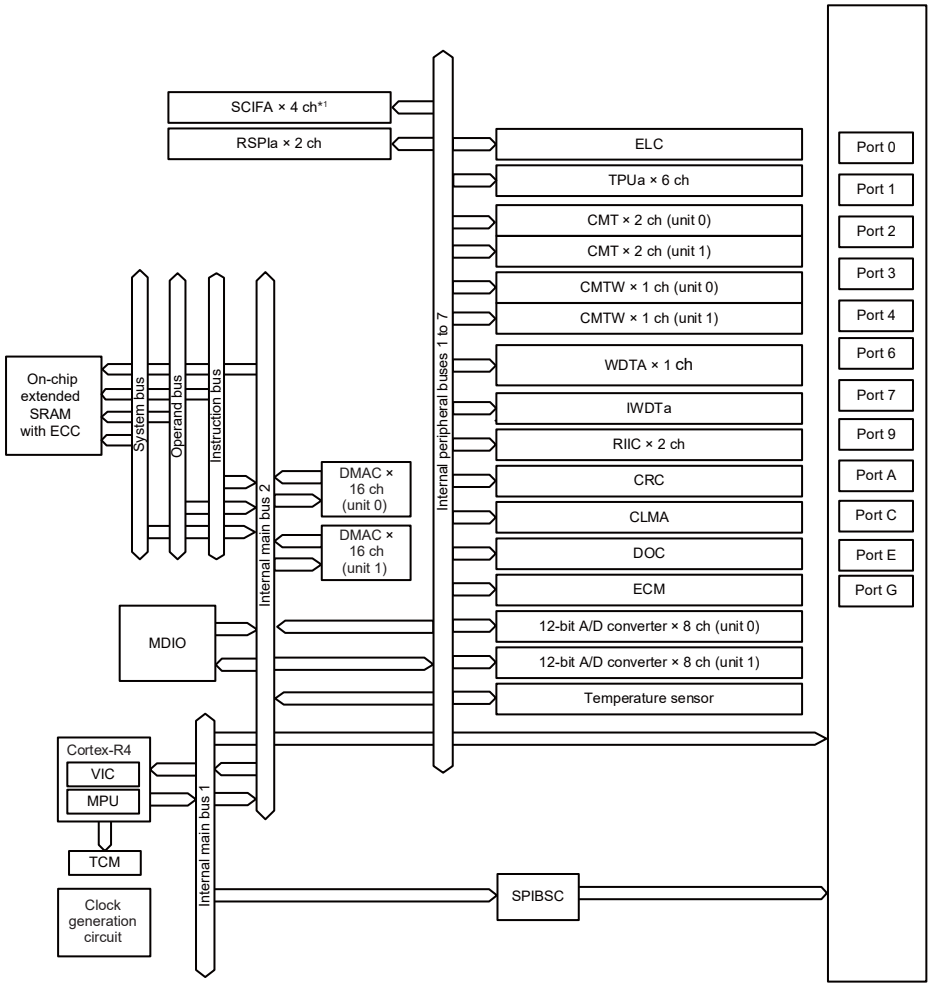
Table 1.3 List of Products

Group	Part No.	Package	CPU	On-Chip Extended SRAM Capacity	Operating Frequency (max.)	Security Function*1	Option
RZ/T1-M	R7S910020CBG	112 pins	Cortex-R4	Not supported	450 MHz	Not supported	Not supported
	R7S910021CBG	112 pins	Cortex-R4	1 Mbyte	450 MHz	Not supported	Not supported
	R7S910120CBG	112 pins	Cortex-R4	Not supported	450 MHz	Available	Not supported
	R7S910121CBG	112 pins	Cortex-R4	1 Mbyte	450 MHz	Available	Not supported
	R7S910022CBG	112 pins	Cortex-R4	Not supported	450 MHz	Not supported	MDIO master
	R7S910023CBG	112 pins	Cortex-R4	1 Mbyte	450 MHz	Not supported	MDIO master
	R7S910122CBG	112 pins	Cortex-R4	Not supported	450 MHz	Available	MDIO master
	R7S910123CBG	112 pins	Cortex-R4	1 Mbyte	450 MHz	Available	MDIO master

Note 1. Details of these functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.

1.3 Block Diagram

Figure 1.1 shows a block diagram.



DMAC:	DMA controller	ELC:	Event link controller
SPIBSC:	SPI multi I/O bus controller	TPUa:	16-bit timer pulse unit
WDTA:	Watchdog timer	CMT:	Compare match timer
IWDTa:	Independent watchdog timer	CMTW:	Compare match timer W
MDIO:	Management data input/output interface	RIICa:	I^2C bus interface
SCIFA:	Serial communication interface with FIFO	CRC:	CRC (cyclic redundancy check) calculator
RSPIa:	Serial peripheral interface	CLMA:	Clock monitor circuit
VIC:	Vector interrupt controller	DOC:	Data operation circuit
MPU:	Memory protection unit	ECM:	Error control module

Note 1. Channel 4 is used only in asynchronous mode.

Figure 1.1 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 3)

Classifications	Pin Name	I/O	Description
Power supply	VDD	Input	Power supply pin. Connect this pin to the system power supply.
	VSS	Input	Ground pin. Connect this pin to the system power supply (0 V).
	VCCQ12	Input	Power supply pin for MDIO pins
	VCCQ33	Input	Power supply pin for I/O pins
	PLLVDD0, PLLVDD1	Input	Power supply pins for the on-chip PLL oscillator
	PLLVSS0, PLLVSS1	Input	Ground pins for the on-chip PLL oscillator. Connect these pins to the system power supply (0 V).
Clock	XTAL	Output	Connected to a crystal resonator.
	EXTAL	Input	
Operating mode control	MD0, MD1	Input	Input the operating mode select signal.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	RSTOUT#	Output	Outputs the reset signal externally.
Debugging interface	TRST#	Input	Test reset pin for on-chip emulator
	TMS	I/O	Test mode select pin for on-chip emulator
	TDI	Input	Test data input pin for on-chip emulator
	TDO	Output	Test data output pin for on-chip emulator
	TCK	Input	Test clock pin for on-chip emulator
	TRACECLK	Output	Outputs the clock for synchronization with the trace data.
	TRACECTL	Output	Outputs the enable signal for trace control.
	TRACEDATA0 to TRACEDATA7	Output	Output the trace data.
Interrupt	NMI	Input	Inputs the non-maskable interrupt request signal.
	IRQ0 to IRQ4, IRQ6, IRQ7	Input	Input the external interrupt request signal.
16-bit timer pulse unit (TPUa)	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins
	TIOCA1, TIOCB1	I/O	TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins
	TIOCA2, TIOCB2	I/O	TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins
	TIOCA4, TIOCB4	I/O	TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins
	TIOCA5, TIOCB5	I/O	TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins
	TCLKA, TCLKB, TCLKC, TCLKD	Input	External clock input pins for TPUa
Compare match timer W (CMTW)	TIC0 to TIC3	Input	CMTW input capture input pins
	TOC0 to TOC3	Output	CMTW output compare output pins

Table 1.4 Pin Functions (2 / 3)

Classifications	Pin Name	I/O	Description
Serial communication interface with FIFO (SCIFA)	SCK0 to SCK2	I/O	Clock I/O pins
	RXD0 to RXD2, RXD4*1	Input	Input the receive data.
	TXD0 to TXD2, TXD4*1	Output	Output the transmit data.
	CTS0# to CTS2#	I/O	Hardware flow control input (transmission enable signal)/general output
	RTS0# to RTS2#	Output	Hardware flow control output (transmission request signal)/general output
I2C bus interface (RIICa)	SCL0, SCL1	I/O	Clock I/O pins. The bus can be directly driven by the N-channel open drain.
	SDA0, SDA1	I/O	Data I/O pins. The bus can be directly driven by the N-channel open drain.
Management data input/ output interface (MDIOM/ MDIO)	MDC	Input	MDIO clock input pin for slave operation (up to 4 MHz)
	MDIO	I/O	MDIO data I/O pin for slave operation
	MMDC1	Output	MDIO clock output pins for master operation (up to 10 MHz)
	MMDIO1	I/O	MDIO data I/O pins for master operation
	PRTADR0	Input	Input pin to select the optical transceiver module for slave operation
	PRTADR1	Input	Input pin to select the optical transceiver module for slave operation
	PRTADR2	Input	Input pin to select the optical transceiver module for slave operation
	PRTADR3	Input	Input pin to select the optical transceiver module for slave operation
	PRTADR4	Input	Input pin to select the optical transceiver module for slave operation
Serial peripheral interface (RSPIa)	RSPCK0, RSPCK1	I/O	Clock I/O pins
	MOSI0, MOSI1	I/O	Master transmit data I/O pins
	MISO0, MISO1	I/O	Slave transmit data I/O pins
	SSL00, SSL10	I/O	Slave select signal I/O pins
	SSL01, SSL02, SSL03, SSL11	Output	Slave select signal output pins
SPI multi I/O bus controller (SPIBSC)	SPBCLK	Output	Clock output pin
	SPBSSL	Output	Slave select signal output pin
	SPBMO/SPBIO0	I/O	Master transmit data/data 0 I/O pin
	SPBMI/SPBIO1	I/O	Master input data/data 1 I/O pin
	SPBIO2, SPBIO3	I/O	Data 2, data 3 I/O pins
12-bit A/D converter (S12ADCa)	AN000 to AN007, AN100 to AN107	Input	Analog input pins for A/D converter
	ADTRG0, ADTRG1	Input	External trigger input pins for the start of A/D conversion
Analog power supply	AVCC0	Input	Analog power supply input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Reference power supply input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.

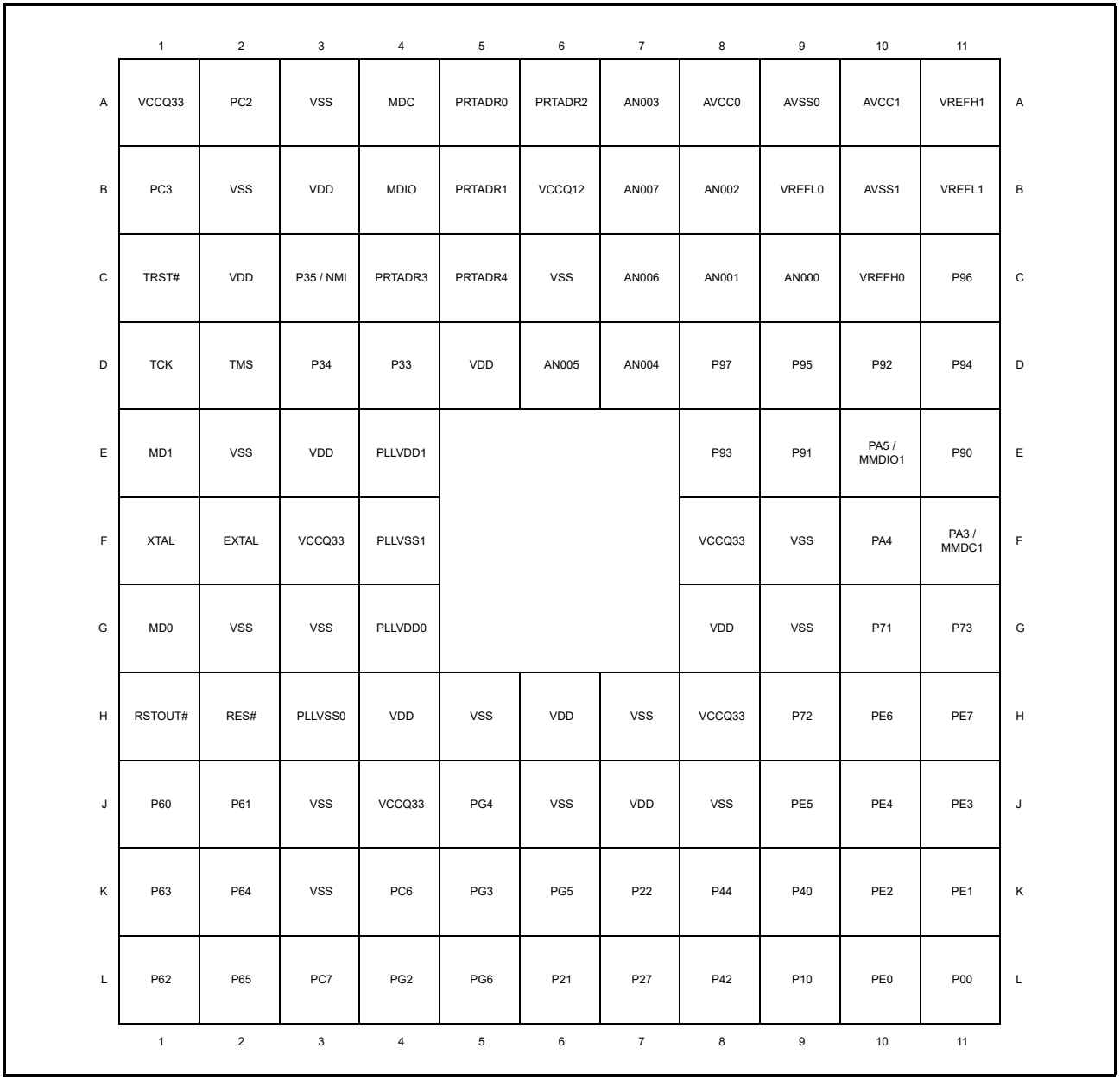
Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC1	Input	Analog power supply input pin for the 12-bit A/D converter (unit 1). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	AVSS1	Input	Analog ground input pin for the 12-bit A/D converter (unit 1). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.
	VREFH1	Input	Reference power supply input pin for the 12-bit A/D converter (unit 1). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	VREFL1	Input	Reference ground pin for the 12-bit A/D converter (unit 1). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.
I/O ports	P00	I/O	1-bit I/O pin
	P10	I/O	1-bit I/O pin
	P21, P22, P27	I/O	3-bit I/O pins
	P33, P34, P35	I/O	3-bit I/O pins
	P40, P42, P44	I/O	3-bit I/O pins
	P50 to P56*2	I/O	7-bit I/O pins
	P60 to P65	I/O	6-bit I/O pins
	P71 to P73	I/O	3-bit I/O pins
	P90 to P97	I/O	8-bit I/O pins
	PA3 to PA5	I/O	3-bit I/O pins
	PC2, PC3, PC6, PC7	Input	4-bit input pins
	PE0 to PE7	I/O	8-bit I/O pins
	PG2 to PG6	I/O	5-bit I/O pins

Note 1. Channel 4 is used only in asynchronous mode.
Note 2. 1.2-V pins

1.5 Pin Assignments

Figure 1.2 shows the pin arrangement. Table 1.5 shows the pin assignments. Table 1.6 shows the list of pin functions.



	1	2	3	4	5	6	7	8	9	10	11	
A	VCCQ33	PC2	VSS	MDC	PRTADR0	PRTADR2	AN003	AVCC0	AVSS0	AVCC1	VREFH1	A
B	PC3	VSS	VDD	MDIO	PRTADR1	VCCQ12	AN007	AN002	VREFL0	AVSS1	VREFL1	B
C	TRST#	VDD	P35 / NMI	PRTADR3	PRTADR4	VSS	AN006	AN001	AN000	VREFH0	P96	C
D	TCK	TMS	P34	P33	VDD	AN005	AN004	P97	P95	P92	P94	D
E	MD1	VSS	VDD	PLLVDD1				P93	P91	PA5 / MMDIO1	P90	E
F	XTAL	EXTAL	VCCQ33	PLLVSS1				VCCQ33	VSS	PA4	PA3 / MMDC1	F
G	MD0	VSS	VSS	PLLVDD0				VDD	VSS	P71	P73	G
H	RSTOUT#	RES#	PLLVSS0	VDD	VSS	VDD	VSS	VCCQ33	P72	PE6	PE7	H
J	P60	P61	VSS	VCCQ33	PG4	VSS	VDD	VSS	PE5	PE4	PE3	J
K	P63	P64	VSS	PC6	PG3	PG5	P22	P44	P40	PE2	PE1	K
L	P62	P65	PC7	PG2	PG6	P21	P27	P42	P10	PE0	P00	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 1.2 Pin Arrangement (112-pin FBGA) (Top View)

Table 1.5 Pin Assignments (112-Pin FBGA) (1 / 3)

Pin Number	Pin Name
A1	VCCQ33
A2	PC2 / SDA0
A3	VSS
A4	P56 / MDC
A5	P54 / PRTADR0
A6	P51 / PRTADR2
A7	AN003
A8	AVCC0
A9	AVSS0
A10	AVCC1
A11	VREFH1
B1	PC3 / RXD4 / SCL0
B2	VSS
B3	VDD
B4	P55 / MDIO
B5	P52 / PRTADR1
B6	VCCQ12
B7	AN007
B8	AN002
B9	VREFL0
B10	AVSS1
B11	VREFL1
C1	TRST#
C2	VDD
C3	P35 / NMI
C4	P53 / PRTADR3
C5	P50 / PRTADR4
C6	VSS
C7	AN006
C8	AN001
C9	AN000
C10	VREFH0
C11	P96 / AN106
D1	TCK
D2	TMS
D3	P34 / TDI
D4	P33 / TDO
D5	VDD
D6	AN005
D7	AN004
D8	P97 / AN107 / IRQ7 / ADTRG1
D9	P95 / AN105 / CTS2#
D10	P92 / AN102 / TOC3 / RXD2
D11	P94 / AN104 / IRQ4 / RTS2#

Table 1.5 Pin Assignments (112-Pin FBGA) (2 / 3)

Pin Number	Pin Name
E1	MD1
E2	VSS
E3	VDD
E4	PLLVDD1
E8	P93 / AN103 / TIC3 / SCK2
E9	P91 / AN101 / TXD2
E10	PA5 / TIOCA4 / TXD2 / MMDIO1
E11	P90 / AN100 / TIOCA5 / TXD4
F1	XTAL
F2	EXTAL
F3	VCCQ33
F4	PLLVSS1
F8	VCCQ33
F9	VSS
F10	PA4 / TIOCA3 / ADTRG0 / RXD2
F11	PA3 / TIOCA2 / SCK2 / MMDC1
G1	MD0
G2	VSS
G3	VSS
G4	PLLVDD0
G8	VDD
G9	VSS
G10	P71 / TOC2 / SCK1 / TRACECTL
G11	P73 / IRQ3 / RXD1 / TRACEDATA1
H1	RSTOUT#
H2	RES#
H3	PLLVSS0
H4	VDD
H5	VSS
H6	VDD
H7	VSS
H8	VCCQ33
H9	P72 / TIC2 / TXD1 / TRACEDATA0
H10	PE6 / IRQ6 / TIOCD0 / RXD1 / MISO0 / TRACEDATA6
H11	PE7 / TIOCD3 / SCK1 / RSPCK0 / TRACEDATA7
J1	P60 / SPBSSL
J2	P61 / SPBIO3
J3	VSS
J4	VCCQ33
J5	PG4 / TOC1 / MOSI1
J6	VSS
J7	VDD
J8	VSS
J9	PE5 / TIOCC3 / TXD1 / MOSI0 / TRACEDATA5
J10	PE4 / TIOCC0 / RTS1# / SSL00 / TRACEDATA4

Table 1.5 Pin Assignments (112-Pin FBGA) (3 / 3)

Pin Number	Pin Name
J11	PE3 / IRQ3 / TIOCB5 / CTS1# / SSL01 / TRACEDATA3
K1	P63 / SPBMO/SPBIO0
K2	P64 / SPBMI/SPBIO1
K3	VSS
K4	PC6 / TCLKC / SCL1
K5	PG3 / TIC1 / MISO1
K6	PG5 / TCLKA / SSL10
K7	P22 / IRQ2 / TIOCD0 / SCK0
K8	P44 / TCLKD / ADTRG0 / CTS0#
K9	P40 / TXD0
K10	PE2 / IRQ2 / TIOCB4 / SSL02 / TRACEDATA2
K11	PE1 / TIOCB3 / SSL03 / TRACEDATA1
L1	P62 / SPBCLK
L2	P65 / SPBIO2
L3	PC7 / TIC0 / SDA1
L4	PG2 / TOC0 / RSPCK1
L5	PG6 / TCLKB / SSL11
L6	P21 / IRQ1 / TIOCB1 / CTS0#
L7	P27 / TIOCB0 / RTS0#
L8	P42 / RXD0
L9	P10 / IRQ0 / TIOCA0 / TRACECLK
L10	PE0 / TIOCB2 / TRACEDATA0
L11	P00 / TIOCA1 / ADTRG1 / TRACECTL

Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (1 / 3)

Pin Number 112-Pin FBGA	Power Supply Clock System Control	I/O Port	Timer (TPUa, CMT2)	Communication (MDIO, SCIFA, RSPIa, RIICa, SPIBSC)	Others	Interrupt	S12ADC
A1	VCCQ33						
A2		PC2		SDA0			
A3	VSS						
A4		P56		MDC			
A5		P54		PRTADR0			
A6		P51		PRTADR2			
A7							AN003
A8	AVCC0						
A9	AVSS0						
A10	AVCC1						
A11	VREFH1						
B1		PC3		RXD4 / SCL0			
B2	VSS						
B3	VDD						
B4		P55		MDIO			
B5		P52		PRTADR1			
B6	VCCQ12						
B7							AN007
B8							AN002
B9	VREFL0						
B10	AVSS1						
B11	VREFL1						
C1	TRST#						
C2	VDD						
C3		P35				NMI	
C4		P53		PRTADR3			
C5		P50		PRTADR4			
C6	VSS						
C7							AN006
C8							AN001
C9							AN000
C10	VREFH0						
C11		P96					AN106
D1	TCK						
D2	TMS						
D3	TDI	P34					
D4	TDO	P33					
D5	VDD						
D6							AN005
D7							AN004
D8		P97				IRQ7	ADTRG1 / AN107

Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (2 / 3)

Pin Number 112-Pin FBGA	Power Supply Clock System Control	I/O Port	Timer (TPUa, CMT2)	Communication (MDIO, SCIFA, RSPIa, RIICa, SPIBSC)	Others	Interrupt	S12ADC
D9		P95		CTS2#			AN105
D10		P92	TOC3	RXD2			AN102
D11		P94		RTS2#		IRQ4	AN104
E1	MD1						
E2	VSS						
E3	VDD						
E4	PLLVDD1						
E8		P93	TIC3	SCK2			AN103
E9		P91		TXD2			AN101
E10		PA5	TIOCA4	TXD2 / MMDIO1			
E11		P90	TIOCA5	TXD4			AN100
F1	XTAL						
F2	EXTAL						
F3	VCCQ33						
F4	PLLVSS1						
F8	VCCQ33						
F9	VSS						
F10		PA4	TIOCA3	RXD2			ADTRG0
F11		PA3	TIOCA2	SCK2 / MMDC1			
G1	MD0						
G2	VSS						
G3	VSS						
G4	PLLVDD0						
G8	VDD						
G9	VSS						
G10	TRACECTL	P71	TOC2	SCK1			
G11	TRACEDATA1	P73		RXD1		IRQ3	
H1	RSTOUT#						
H2	RES#						
H3	PLLVSS0						
H4	VDD						
H5	VSS						
H6	VDD						
H7	VSS						
H8	VCCQ33						
H9	TRACEDATA0	P72	TIC2	TXD1			
H10	TRACEDATA6	PE6	TIOCD0	RXD1 / MISO0		IRQ6	
H11	TRACEDATA7	PE7	TIOCD3	SCK1 / RSPCK0			
J1		P60		SPBSSL			
J2		P61		SPBIO3			
J3	VSS						
J4	VCCQ33						

Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (3 / 3)

Pin Number 112-Pin FBGA	Power Supply Clock System Control	I/O Port	Timer (TPUa, CMT2)	Communication (MDIO, SCIFA, RSPIa, RIICa, SPIBSC)	Others	Interrupt	S12ADC
J5		PG4	TOC1	MOSI1			
J6	VSS						
J7	VDD						
J8	VSS						
J9	TRACEDATA5	PE5	TIOCC3	TXD1 / MOSI0			
J10	TRACEDATA4	PE4	TIOCC0	RTS1# / SSL00			
J11	TRACEDATA3	PE3	TIOCB5	CTS1# / SSL01		IRQ3	
K1		P63		SPBMO / SPBIO0			
K2		P64		SPBMI / SPBIO1			
K3	VSS						
K4		PC6	TCLKC	SCL1			
K5		PG3	TIC1	MISO1			
K6		PG5	TCLKA	SSL10			
K7		P22	TIOCD0	SCK0		IRQ2	
K8		P44	TCLKD	CTS0#			ADTRG0
K9		P40		TXD0			
K10	TRACEDATA2	PE2	TIOCB4	SSL02		IRQ2	
K11	TRACEDATA1	PE1	TIOCB3	SSL03			
L1		P62		SPBCLK			
L2		P65		SPBIO2			
L3		PC7	TIC0	SDA1			
L4		PG2	TOC0	RSPCK1			
L5		PG6	TCLKB	SSL11			
L6		P21	TIOCB1	CTS0#		IRQ1	
L7		P27	TIOCB0	RTS0#			
L8		P42		RXD0			
L9	TRACECLK	P10	TIOCA0			IRQ0	
L10	TRACEDATA0	PE0	TIOCB2				
L11	TRACECTL	P00	TIOCA1				ADTRG1

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = 0 V

Item	Symbol	Value	Unit
Power supply voltage (I/O)	VCCQ33	-0.3 to +4.2	V
Power supply voltage (1.2 V I/O)	VCCQ12	–0.3 to +1.6	V
Power supply voltage (internal)	VDD	-0.3 to +1.6	V
PLL power supply voltage	PLLVDD0, PLLVDD1	-0.3 to +1.6	V
Input voltage (except 1.2-V I/O ports and ports for 5-V tolerant*1)	V_{in1}	-0.3 to VCCQ33 + 0.3*4	V
Input voltage (ports for 5-V tolerant*1)	V_{in2}	-0.3 to +5.5*3	V
Input voltage (1.2 V I/O port)	V_{in3}	–0.3 to VCCQ12 + 0.3*5	V
Analog power supply voltage	AVCC0, AVCC1*2	-0.3 to +4.2	V
Reference power supply voltage	VREFH0, VREFH1	-0.3 to (AVCC0, AVCC1) + 0.3*4	V
Analog input voltage	V_{AN}	-0.3 to (AVCC0, AVCC1) + 0.3*4	V
Operating temperature (junction temperature)	Tj	-40 to +110	°C
Storage temperature	T_{stg}	-55 to +125	°C

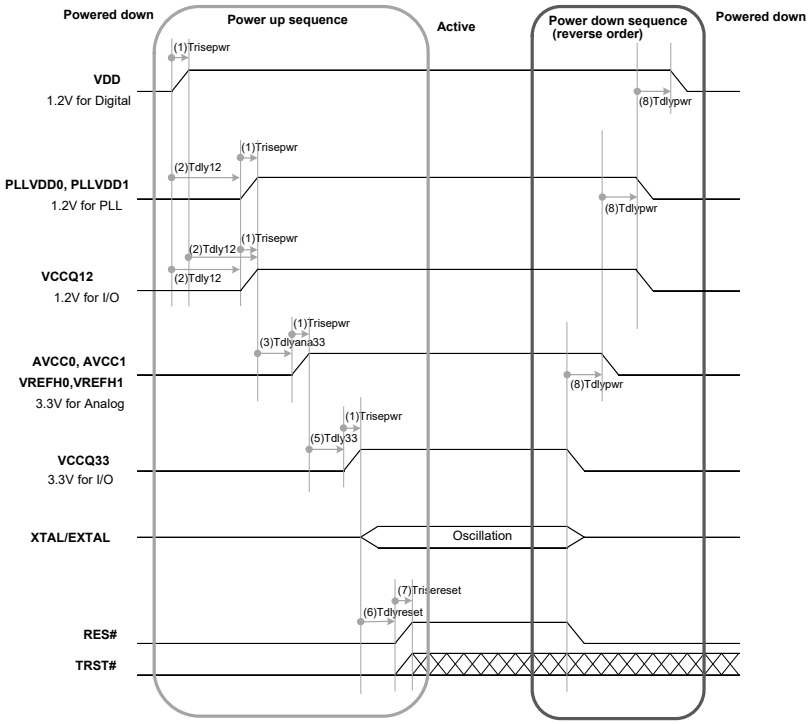
[Usage Notes]

1. Do not directly connect output pins (I/O pins in output state) of IC products to other output pins (including I/O pins in output state) , power pins, or GND pins. However, output pins are directly connectable in an external circuit where timing design is provided to avoid conflict of outputs of high-impedance pins such as I/O pins.
2. If even a single item exceeds the absolute maximum rating for even a moment, it may degrade the product's quality. In other words, the absolute maximum rating is a rated value that potentially causes physical damage to products. Use products with a margin of the absolute maximum rating.
   Specified values and conditions shown in DC characteristics and AC characteristics are the range of normal operation and quality assurance of products.

Note 1. Ports PC2, PC3, PC6, and PC7 are 5-V tolerant.
Note 2. When the A/D converter unit 0 is not to be used, connect the AVCC0 and VREFH0 pins to VCCQ33 and the AVSS0 and VREFL0 pins to VSS, respectively. Do not leave these pins open. In the same way, when the A/D converter unit 1 is not to be used, connect the AVCC1 and VREFH1 pins to VCCQ33 and the AVSS1 and VREFL1 pins to VSS, respectively. Do not leave these pins open.
Note 3. When VCCQ33 is less than 3.0 V, the rated value of ports for 5-V tolerant is 3.6 V.
Note 4. Do not exceed the absolute maximum rating, 4.2 V.
Note 5. Do not exceed the absolute maximum rating, 1.6 V.

2.2 Power On/Off Sequence

Turn on and off each power supply voltage according to the procedure shown in the figure below.
When turning on the power, be sure to fix TRST# pins and RES# pins to the low level. Otherwise, initialization is not performed successfully.



Timing

		Value		
No.	Item	min	typ	max
(1)	Trisepwr	100 µs	—	50 ms
(2)	Tdly12	0 ms	—	100 ms
(3)	Tdlyana33	0 ms	—	100 ms
(4)	Tdly33	0 ms	—	100 ms
(5)	Tdlyreset	10 ms	—	—
(6)	Trisereset	—	—	150 µs
(7)	Tdlypwr	0 ms	—	—

Note 1. Turn on all power supply voltages and reset signals with a monotonic increase and turn off with a monotonic decrease.
Note 2. Do not apply a negative voltage to power supply voltages.
Note 3. Before turning on the power, be sure to make reset pins (TRST# and RES#) active (low). Otherwise, inputs and outputs on the pins may be unstable. If this may also be a problem when turning off the power, make reset pins (TRST# and RES#) active (low.)

Note: If the power on/off sequence is not met (out of operation guarantee range), the pin input state and output state may be undefined.

Figure 2.1 Power On/Off Sequence

2.3 DC Characteristics

- Conditions: VDD = VCCQ12 = PLLVDD0 = PLLVDD1 = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 =3.0 to 3.6 V
  VREFH0 = 2.5 to 3.6 V (when AVCC0 ≥ VREFH0),
  VREFH1 = 2.5 to 3.6 V (when AVCC1 ≥ VREFH1),
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = 0 V,
  Tj = -40 to 110°C

Table 2.2 DC Characteristics (1)

Item	Symbol	min	typ	max	Unit	Test Conditions
Power supply voltage (I/O)	VCCQ33	3.0	3.3	3.6	V	
Power supply voltage (1.2V I/O)	VCCQ12	1.14	1.2	1.26	V	
Power supply voltage (internal)	VDD	1.14	1.2	1.26	V	
PLL power supply voltage	PLLVDD0, PLLVDD1	1.14	1.2	1.26	V	
Analog power supply voltage	AVCC0, AVCC1	3.0	3.3	3.6	V	

Table 2.3 DC Characteristics (2) [Power Supply]

Item	Type	Symbol	typ	max	Unit	Test Conditions
Normal operation	VDD	VIcc	160	440	mA	Tj = -40 to 110ºC R7S910020 R7S910021 R7S910120 R7S910121
			220	511	mA	Tj = -40 to 110ºC R7S910022 R7S910023 R7S910122 R7S910123
	PLLVDD0 + PLLVDD1	PLLIcc	3.2	5	mA	
	VCCQ12	V12Icc	1*1, *2	—	mA	
	VCCQ33	V33Icc	19*1, *2	—	mA	
	AVCC0	AV0Icc	2	5	mA	A/D conversion (unit 0)
	AVCC1	AV1Icc	0.7	1.5	mA	A/D conversion (unit 1)
	VREFH0	VRF0Icc	0.07	0.2	mA	A/D conversion (unit 0)
	VREFH1	VRF1Icc	0.07	0.2	mA	A/D conversion (unit 1)
Standby mode with all modules inactive (reference value)	VDD	VIcc	41	—	mA	
	PLLVDD0 + PLLVDD1	PLLIcc	3.2	—	mA	
	VCCQ12	V12Icc	0.1*1, *2	—	mA	
	VCCQ33	V33Icc	0.35*1, *2	—	mA	
	AVCC0	AV0Icc	0.64	—	µA	
	AVCC1	AV1Icc	0.32	—	µA	
	VREFH0	VRF0Icc	0.24	—	µA	
	VREFH1	VRF1Icc	0.24	—	µA	

Note 1. These values are reference values. The actual operating current greatly depends on the system (such as unsharpened waveforms due to I/O load and toggle frequency). Be sure to measure these current values in the system.
Note 2. V33Icc + V12Icc must be 80 mA or less. (ΣI_{OH} in Table 2.7)

Table 2.4 DC Characteristics (3)*1

Item		Symbol	min	typ	max	Unit	Test Conditions
Schmitt trigger Input voltage	Other than 5-V tolerant pins	V_{IH1}	2.4	—	VCCQ33 + 0.3	V	
		V_{IL1}	–0.3	—	0.8	V	
		ΔV_{T1}	VCCQ33 × 0.05	—	—	V	
	5-V tolerant pins*2	V_{IH2}	VCCQ33 × 0.7	—	5.3*3	V	
		V_{IL2}	–0.3	—	VCCQ33 × 0.3	V	
		ΔV_{T2}	VCCQ33 × 0.05	—	—	V	
Input high level voltage (except for schmitt trigger input pins)		V_{IH3}	2.4	—	VCCQ33 + 0.3	V	
Input low level voltage (except for schmitt trigger input pins)		V_{IL3}	–0.3	—	0.8	V	
Output high level voltage	Other than 5-V tolerant pins	V_{OH}	VCCQ33 – 0.5	—	—	V	I_{OH} = -2 mA
Output low level voltage	Other than 5-V tolerant pins	V_{OL1}	—	—	0.4	V	I_{OL1} = 2 mA
	5-V tolerant pins*2	V_{OL2}	—	—	0.4	V	I_{OL2} = 3 mA
			—	—	0.6	V	I_{OL2} = 6 mA
Input leakage current		$\lvert I_{in} \rvert$	—	—	1.0	µA	$V_{in1} = V_{in2}$ = 0 V $V_{in1} = V_{in2}$ = VCCQ33
Three-state leakage current (off state)	Input/output and output pins excluding 5-V tolerant pins	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in1} = 0 V V_{in1} = VCCQ33
	5-V tolerant pins*2		—	—	5.0	µA	V_{in2} = 0 V V_{in2} = VCCQ33
Input pull-up MOS current and resistance	Ports , P90 to P97	I_{pu1}	–300	—	–30	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = 0 V
		R_{pu1}	10	—	120	kΩ	
	Pins other than the above*4	I_{pu2}	–120	—	–7	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = 0 V
		R_{pu2}	25	—	515	kΩ	
Input pull-down MOS current and resistance	Ports , P90 to P97	I_{pd1}	30	—	300	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = VCCQ33
		R_{pd1}	10	—	120	kΩ	
	Pins other than the above*4	I_{pd2}	7	—	120	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = VCCQ33
		R_{pd2}	25	—	515	kΩ	
Pin capacity	All input/output and input pins	C_{in}	—	—	10	pF	

Note 1. Ports P50 to P56 are not included.
Note 2. Ports PC2, PC3, PC6, and PC7 are 5-V tolerant.
Note 3. When VCCQ33 is less than 3.00 V, do not apply voltage of 3.6 V or higher to 5-V tolerant pins.
Note 4. 5-V tolerant pins are not included.

Table 2.5 DC Characteristics for 1.2-V Pin*1

Item	Symbol	min	typ	max	Unit	Test Conditions
Input high level voltage	V_{IH12}	0.84	—	V_{CCQ12} + 0.3	V	
Input low level voltage	V_{IL12}	-0.3	—	0.36	V	
Input leakage current	I_{IN12}	-100	—	100	µA	
Output high level voltage*2	V_{OH12}	1.0	—	—	V	I_{OH} = -100 µA
Output low level voltage*2	V_{OL12}	—	—	0.2	V	I_{OL} = 100 µA
Output high level current*2	I_{OH12}	—	—	–2	mA	V_{OH} = 1.0 V
Output low level current*2	I_{OL12}	4	—	—	mA	V_{OL} = 0.2 V
Input pull-up MOS current and resistance	I_{pu12}	—	-9	—	µA	VCCQ12 = 1.2V V_{in1} = V_{in2} = 0V
	R_{pu12}	—	133	—	kΩ	
Input pull-down MOS current and resistance	I_{pd12}	—	7.5	—	µA	VCCQ12 = 1.2V V_{in1} = V_{in2} = VCCQ12
	R_{pd12}	—	160	—	kΩ	
Pin capacity	C_{in12}	—	—	10	pF	

Note 1. For P50, P51, P52, P53, P54, P55, and P56 pins.
Note 2. When the DSCR register of P50, P51, P52, P53, P54, P55, and P56 pins is set to 11 (1.2-V driving output).

Table 2.6 DC Characteristics for 12-Bit A/D Converter

Item		Symbol	min	typ	max	Unit	Test Conditions
Analog input voltage	Analog input pin AN00n (n = 0 to 7)	V_{AN00}	VREFL0	—	VREFH0	V	
	Analog input pin AN10n (n = 0 to 7)	V_{AN10}	VREFL1	—	VREFH1	V	

Table 2.7 Permissible Output Currents

Item		Symbol	min	typ	max	Unit
Permissible output low current (average value per pin)	Other than 5-V tolerant pins	I_{OL1}	—	—	2.0	mA
	5-V tolerant pins	I_{OL2}	—	—	3.0	mA
Permissible output low current (maximum value per pin)	Other than 5-V tolerant pins	I_{OL1}	—	—	4.0	mA
	5-V tolerant pins	I_{OL2}	—	—	6.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins	I_{OH}	—	—	-2.0	mA
Permissible output high current (maximum value per pin)	All output pins	I_{OH}	—	—	-4.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	-80	mA

[Usage Note] All output current values shall be within the values in Table 2.7 to ensure the reliability of this LSI.

2.4 AC Characteristics

- Conditions: VDD = VCCQ12 = PLLVDD0 = PLLVDD1 = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = 3.0 to 3.6 V
  VREFH0 = 2.5 to 3.6 V (when AVCC0 ≥ VREFH0),
  VREFH1 = 2.5 to 3.6 V (when AVCC1 ≥ VREFH1),
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = 0 V,
  Tj = -40 to 110°C

Table 2.8 Operating Frequency

Item			Symbol	min	max	Unit
Operating frequency	CPU clock (CPUCLK)	112-pin TFBGA	f	150	450	MHz
	System clock (ICLK)			150		
	Peripheral module clock (PCLKA)			150		
	Peripheral module clock (PCLKB)			75		
	Peripheral module clock (PCLKD)			75		
	Peripheral module clock (PCLKE)			18.75	75	
	Peripheral module clock (PCLKF)			7.5	60	
	Peripheral module clock (PCLKG)			7.5	60	
	Peripheral module clock (PCLKH)			60		
	High-speed serial clock (SERICLK)			120	150	

- 1.2-V I/O clock cycle
  Output load conditions: C = 200 pF

Item	Symbol	min	max	Unit	Test Conditions
Output clock cycle*1	t_{prd}	250	—	ns	Figure 2.2

Note 1. When the DSCR register of the P50, P51, P52, P53, P54, P55, and P56 pins is set to 11 (1.2-V driving output)

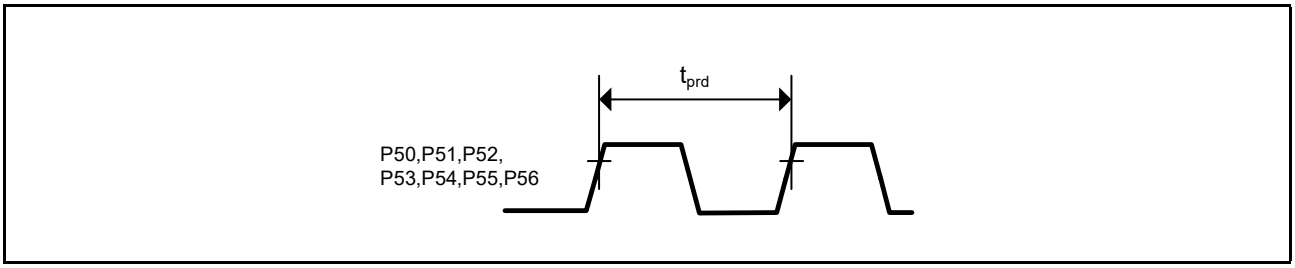


Figure 2.2 1.2-V I/O Clock Cycle

2.4.1 Clock Timing

Table 2.9 XTAL Clock Timing

Item	Symbol	min	typ	max	Unit
XTAL clock oscillator output cycle*1	$t_{XTALcyc}$		40.00 ± 50 ppm		ns

Note 1. When using the XTAL clock, ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.

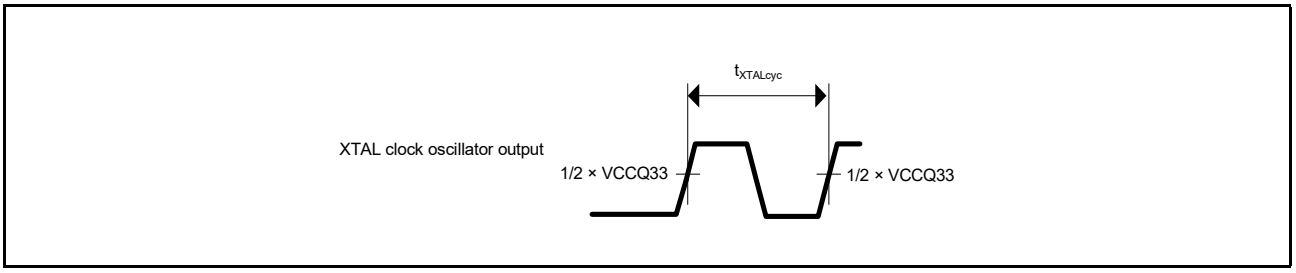


Figure 2.3 XTAL Clock Oscillator Output Timing

Table 2.10 LOCO Clock Timing

Item	Symbol	min	typ	max	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.62	4.17	3.79	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	40	µs	Figure 2.4

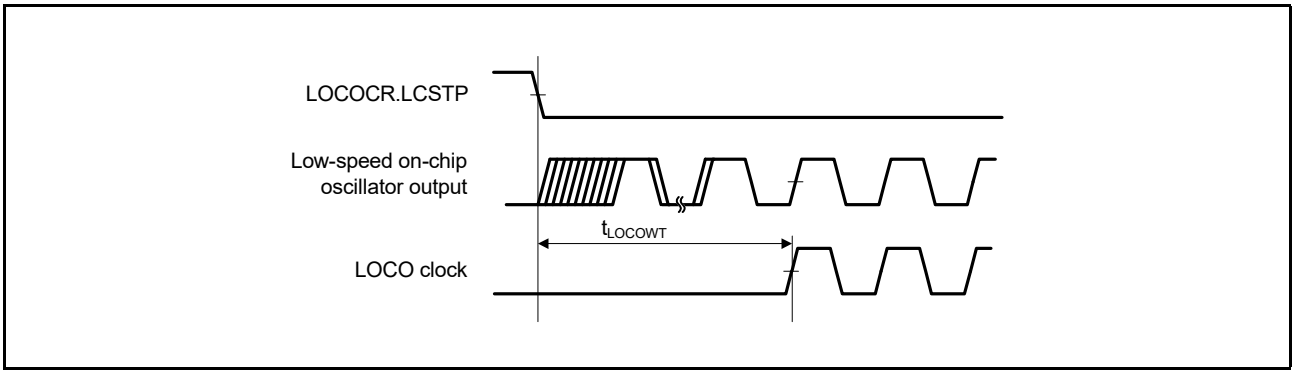


Figure 2.4 LOCO Clock Oscillation Start Timing

2.4.2 Reset Timing and Interrupt Timing

Table 2.11 Reset Timing and Interrupt Timing

Item		Symbol	Min*1	typ	max	Unit	Test Conditions
RES# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	Figure 2.5
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
RES# rising time		$T_{risereset}$	—	—	150	µs	
TRST# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
TRST# rising time		$T_{risereset}$	—	—	150	µs	
NMI pulse width		t_{NMIW}	t_{Icyc} × 2	—	—	ns	Figure 2.6
IRQ pulse width		t_{IRQW}	t_{Icyc} × 2	—	—	ns	Figure 2.7

Note 1. t_{Icyc}: ICLK cycle

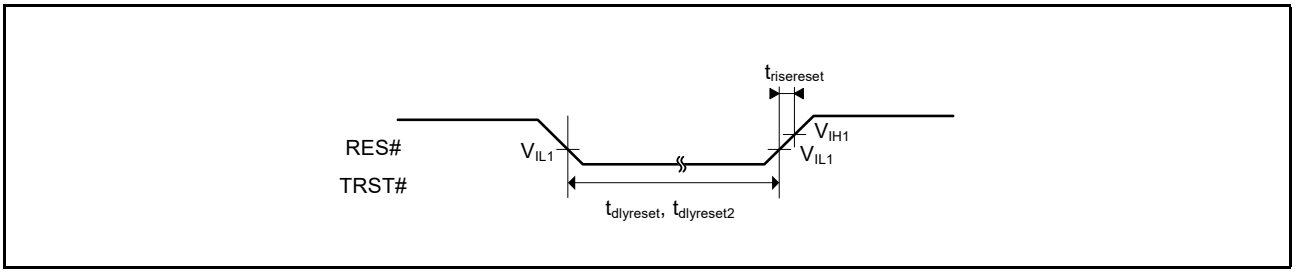


Figure 2.5 Reset Input Timing

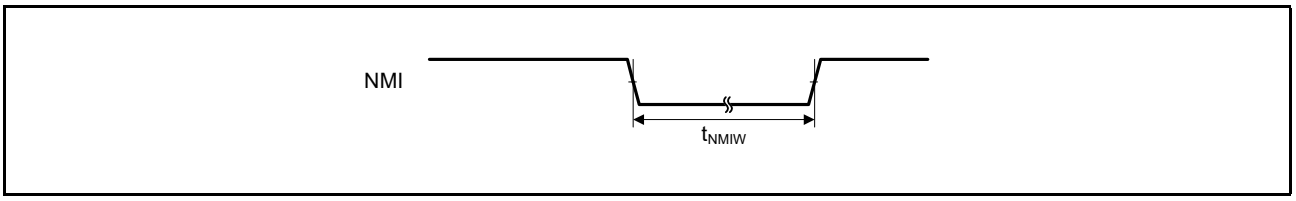


Figure 2.6 NMI Interrupt Input Timing

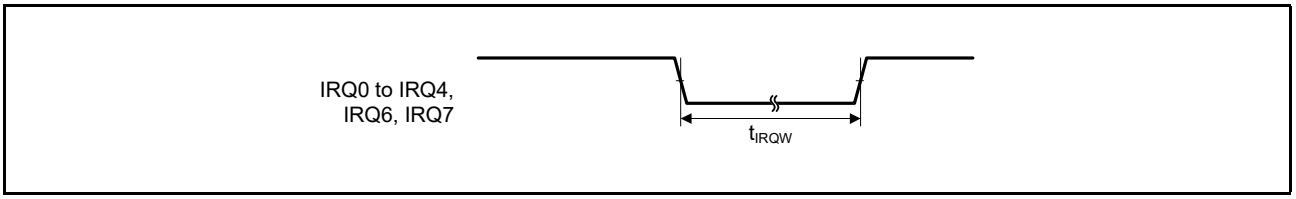


Figure 2.7 IRQ Interrupt Input Timing

2.4.3 On-Chip Peripheral Module Timing

2.4.3.1 I/O Port Timing

Table 2.12 I/O Port Timing

Item		Symbol	min	max	Unit*1	Test Conditions
I/O port	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.8

Note 1. t_{PBcyc}: PCLKB cycle

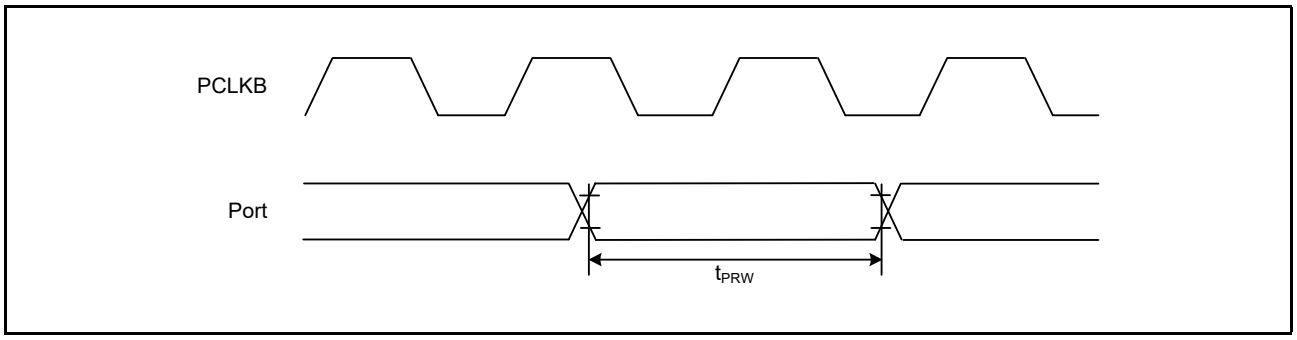


Figure 2.8 I/O Port Input Timing

2.4.3.2 TPUa Timing

Table 2.13 TPUa Timing

Item			Symbol	min	max	Unit*1	Test Conditions
TPUa	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PDcyc}	Figure 2.9
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PDcyc}	Figure 2.10
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PDcyc}: PCLKD cycle

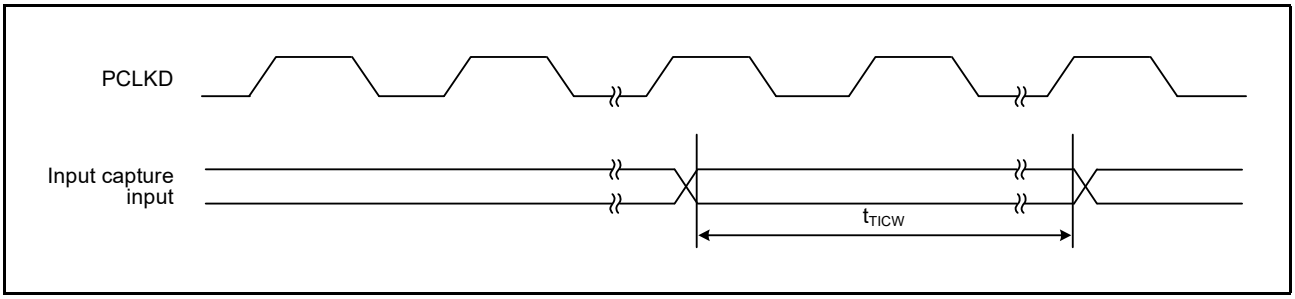


Figure 2.9 TPUa Input Capture Input Timing

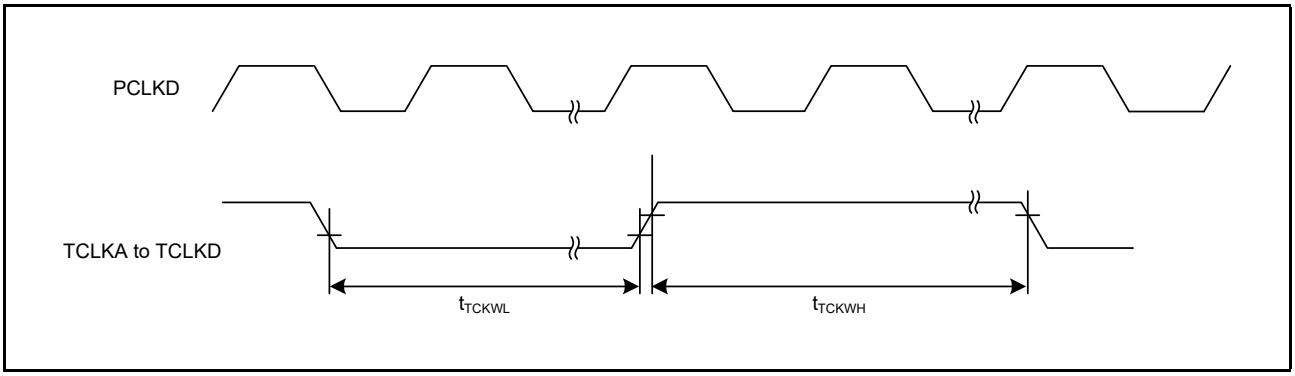


Figure 2.10 TPUa Clock Input Timing

2.4.3.3 CMTW Timing

Table 2.14 CMTW Timing

Item			Symbol	min	max	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PDcyc}	Figure 2.11
		Both-edge setting		2.5	—		

Note 1. t_{PDcyc}: PCLKD cycle

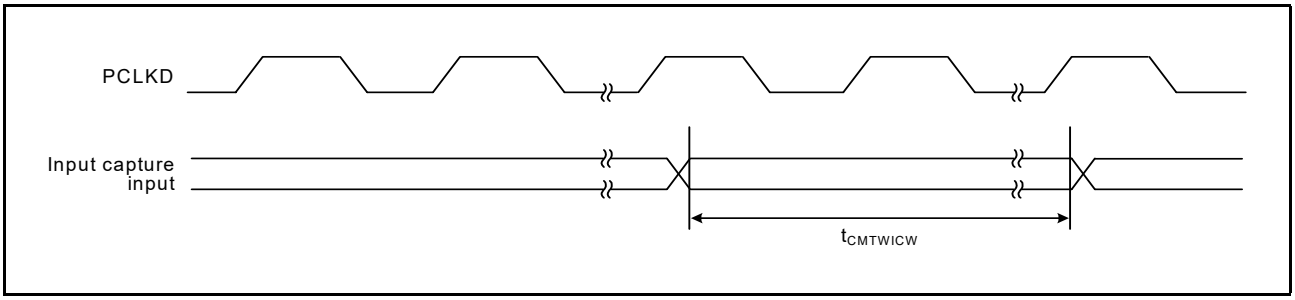


Figure 2.11 CMTW Input Capture Input Timing

2.4.3.4 A/D Converter Trigger Timing

Table 2.15 A/D Converter Trigger Timing

Item			Symbol	min	max	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	ADTRG0	t_{TRGW}	1.5	—	t_{PFcyc}	Figure 2.12
		ADTRG1		1.5		t_{PGcyc}	Figure 2.13

Note 1. t_{PFcyc}: PCLKF cycle, t_{PGcyc}: PCLKG cycle

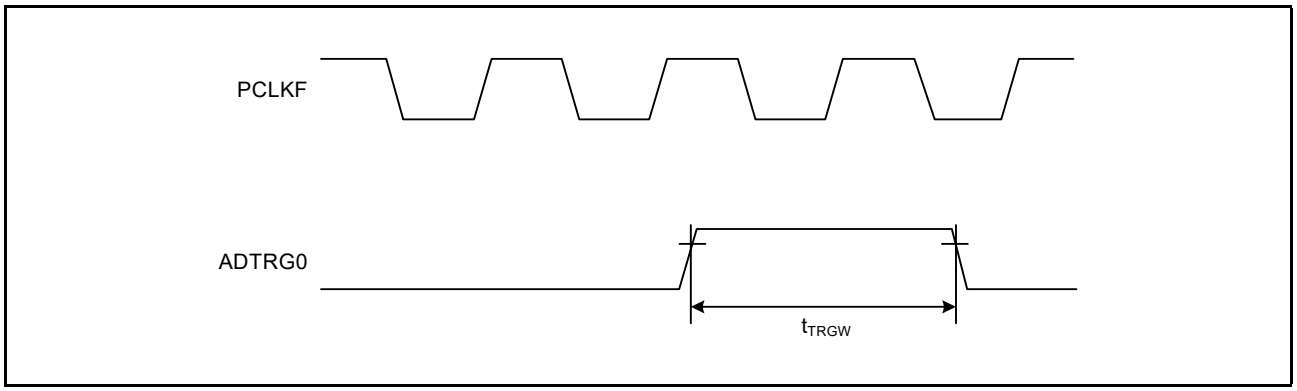


Figure 2.12 A/D Converter Trigger Input Timing (ADTRG0)

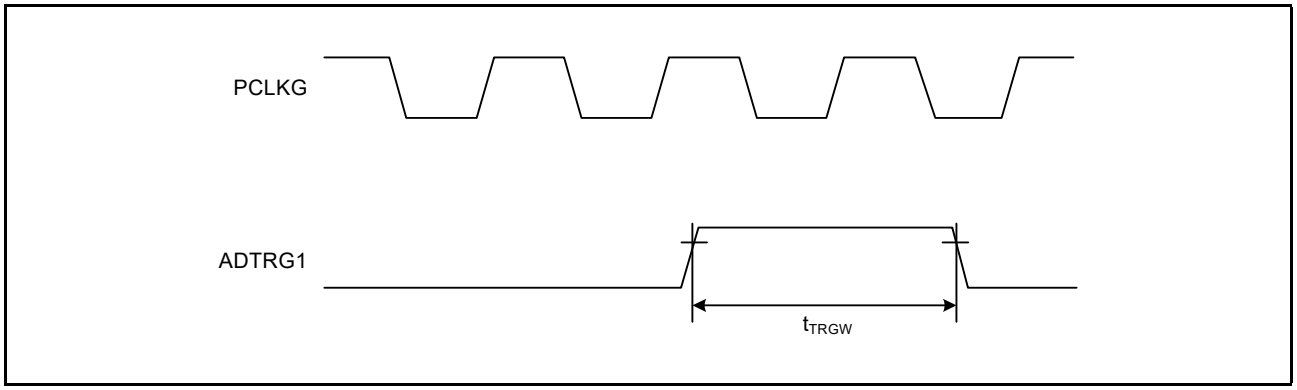


Figure 2.13 A/D Converter Trigger Input Timing (ADTRG1)

2.4.3.5 SCIFA Timing

Table 2.16 SCIFA Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol	min*1	max*1	Unit*1	Test Conditions
SCIFA	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{SEcyc}	Figure 2.14
		Clock synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rising time		t_{SCKr}	—	5	ns	
	Input clock falling time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{SEcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rising time		t_{SCKr}	—	9	ns	
	Output clock falling time		t_{SCKf}	—	9	ns	
	Transmit data delay time	Internal clock	t_{TXD}	-10	10	ns	Figure 2.15
		External clock		3 × t_{SEcyc}	4 × t_{SEcyc} + 20		
	Receive data setup time	Internal clock	t_{RXS}	3 × t_{SEcyc} + 20	—	ns	
		External clock		t_{SEcyc} + 10	—		
	Receive data hold time	Internal clock	t_{RXH}	-3 × t_{SEcyc}	—	ns	
		External clock		2 × t_{SEcyc} + 10	—		

Note 1. t_{SEcyc}: SERICLK cycle
Note 2. When the SEMR.ABCS0 bit = 1 and the SEMR.BGDM bit = 1

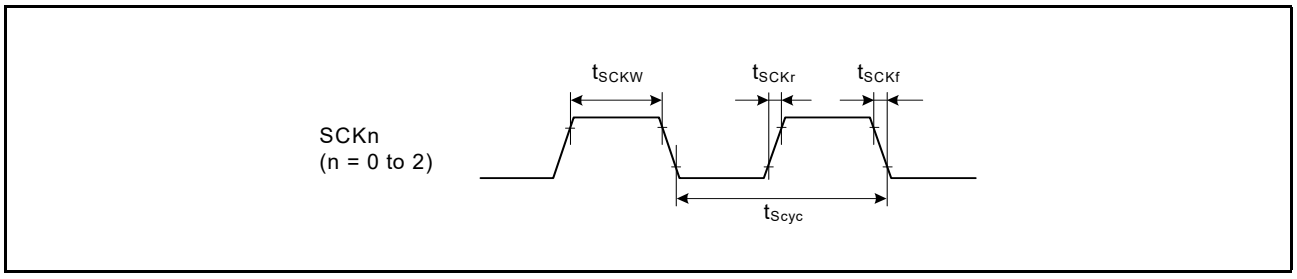


Figure 2.14 SCK Clock Input Timing

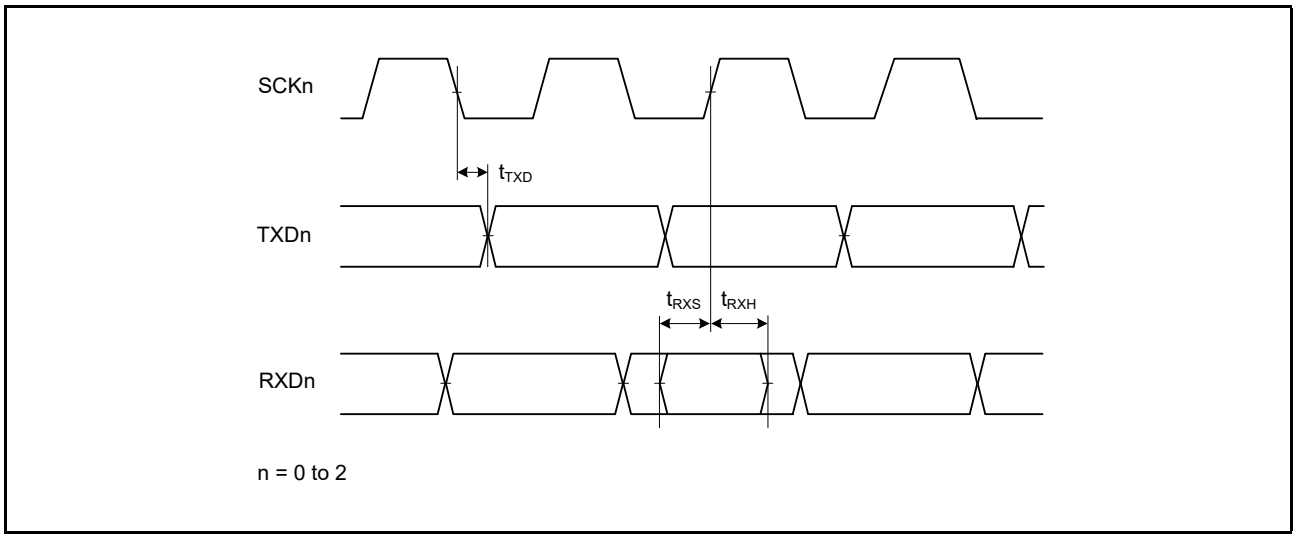


Figure 2.15 SCIFA Input/Output Timing/Clock Synchronous Mode

2.4.3.6 RSPIa Timing

Table 2.17 RSPIa Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol*1	Min*1	Max*1	Unit*1	Test Conditions
RSPIa	RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{SEcyc}	Figure 2.16
		Slave*4		8	4096		
	RSPCK clock high level pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		0.4	—	t_{SPcyc}	
	RSPCK clock low level pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		0.4	—	t_{SPcyc}	
	RSPCK clock rising/falling time	Output	t_{SPCKr}, t_{SPCKf}	—	9	ns	
		Input		—	10	ns	
	Data input setup time	Master	t_{SU}	6	—	ns	Figure 2.17 to Figure 2.20
		Slave		$8 - t_{SEcyc}$	—		
	Data input hold time	Master	t_H	t_{SEcyc}	—	ns	
		Slave		$8 + 2 \times t_{SEcyc}$	—		
	SSL setup time	Master	t_{LEAD}	$N \times t_{Spcyc} - 3$*2	$N \times t_{Spcyc} + 3$*2	ns	
		Slave		4	—	t_{SEcyc}	
	SSL hold time	Master	t_{LAG}	$N \times t_{Spcyc} - 3$*3	$N \times t_{Spcyc} + 3$*3	ns	
		Slave		4	—	t_{SEcyc}	
	Data output delay time	Master	t_{OD}	—	6	ns	
		Slave		—	$3 \times t_{SEcyc} + 20$ *4		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Continuous transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{SEcyc}$	$8 \times t_{SPcyc} + 2 \times t_{SEcyc}$	ns	
		Slave		$4 \times t_{SEcyc}$	—		
	MOSI, MISO rising/falling time	Output	t_{Dr}, t_{Df}	—	9	ns	
		Input		—	10	ns	
	SSL rising/falling time	Output	t_{SSLr}, t_{SSLf}	—	9	ns	
		Input		—	10	ns	
	Slave access time		t_{SA}	—	4	t_{SEcyc}	Figure 2.19, Figure 2.20
	Slave output release time		t_{REL}	—	3	t_{SEcyc}	

Note 1. t_{SEcyc}: SERICLK cycle
Note 2. N = SPCKD set value + 1 (1 to 8)
Note 3. N = SSLND set value + 1 (1 to 8)
Note 4. The data output delay time may become longer than half a cycle of the RSPCK clock depending on the bit rate setting. Be sure to satisfy the conditions required for the electrical characteristics of the master device.

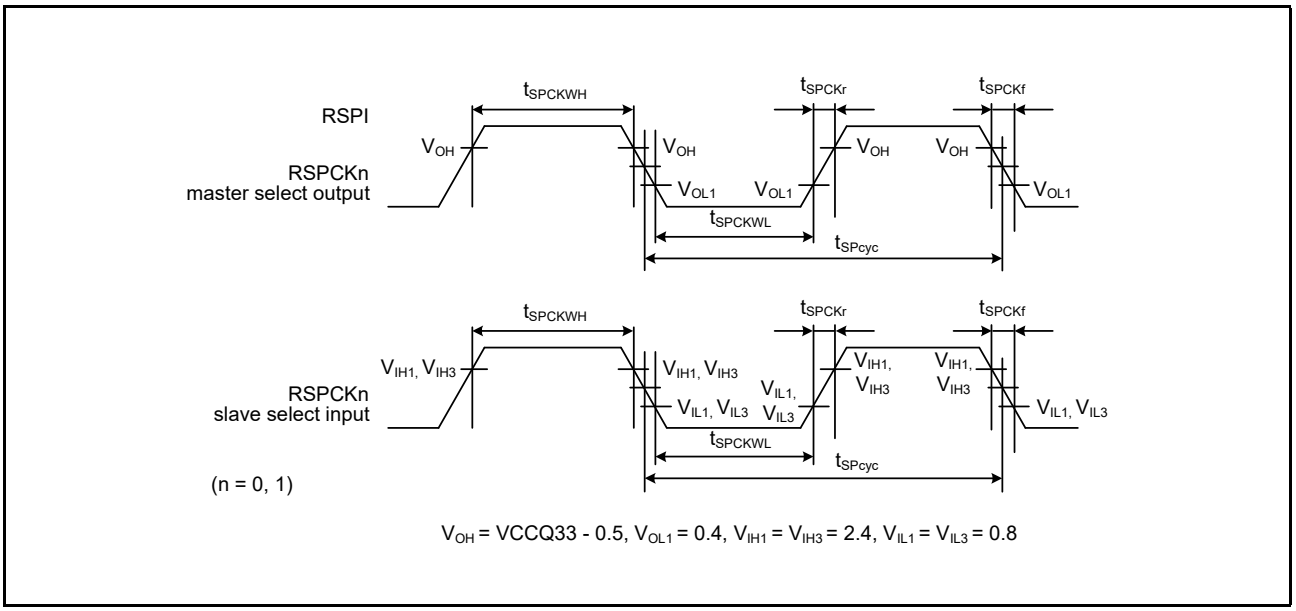


Figure 2.16 RSPIa Clock Timing

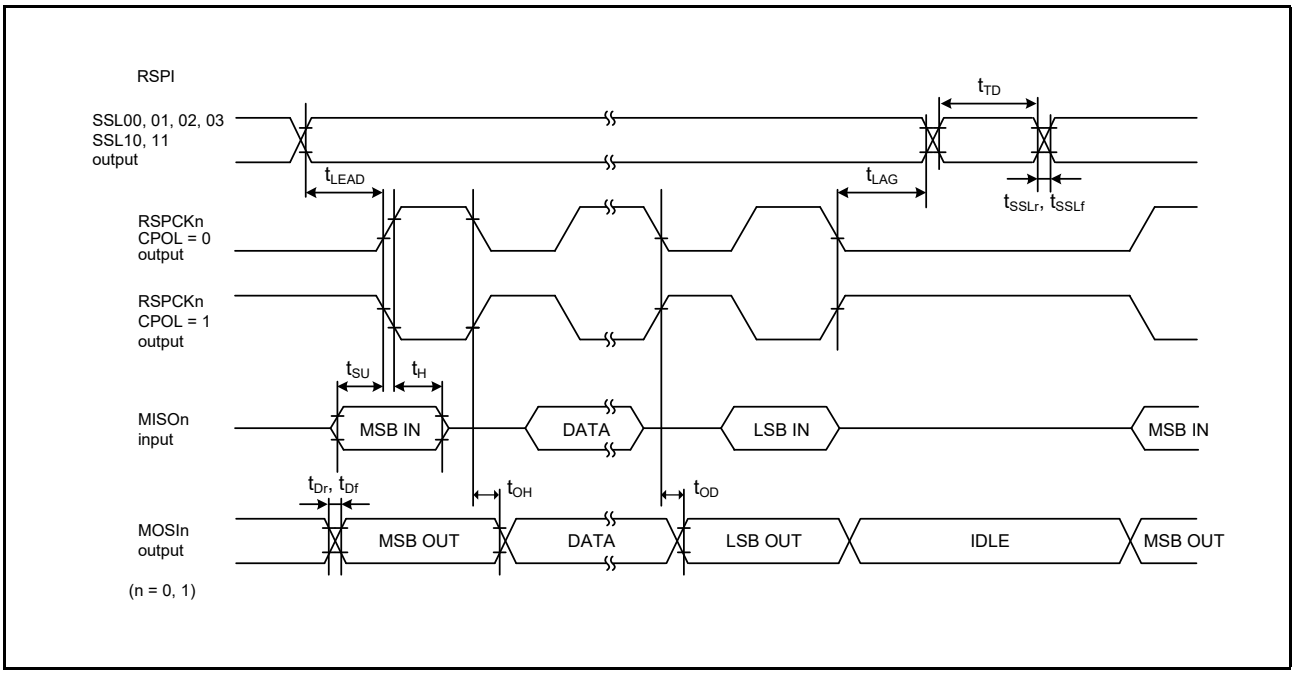


Figure 2.17 RSPIa Timing (Master, CPHA = 0)

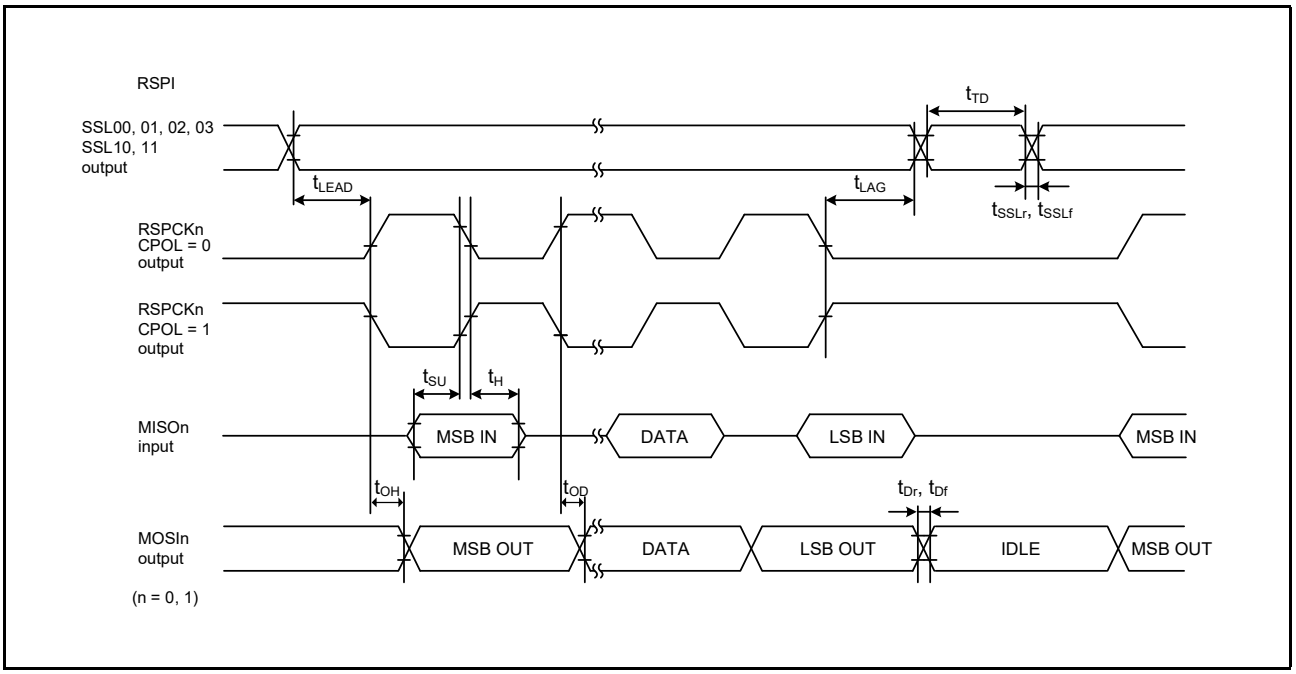


Figure 2.18 RSPIa Timing (Master, CPHA = 1)

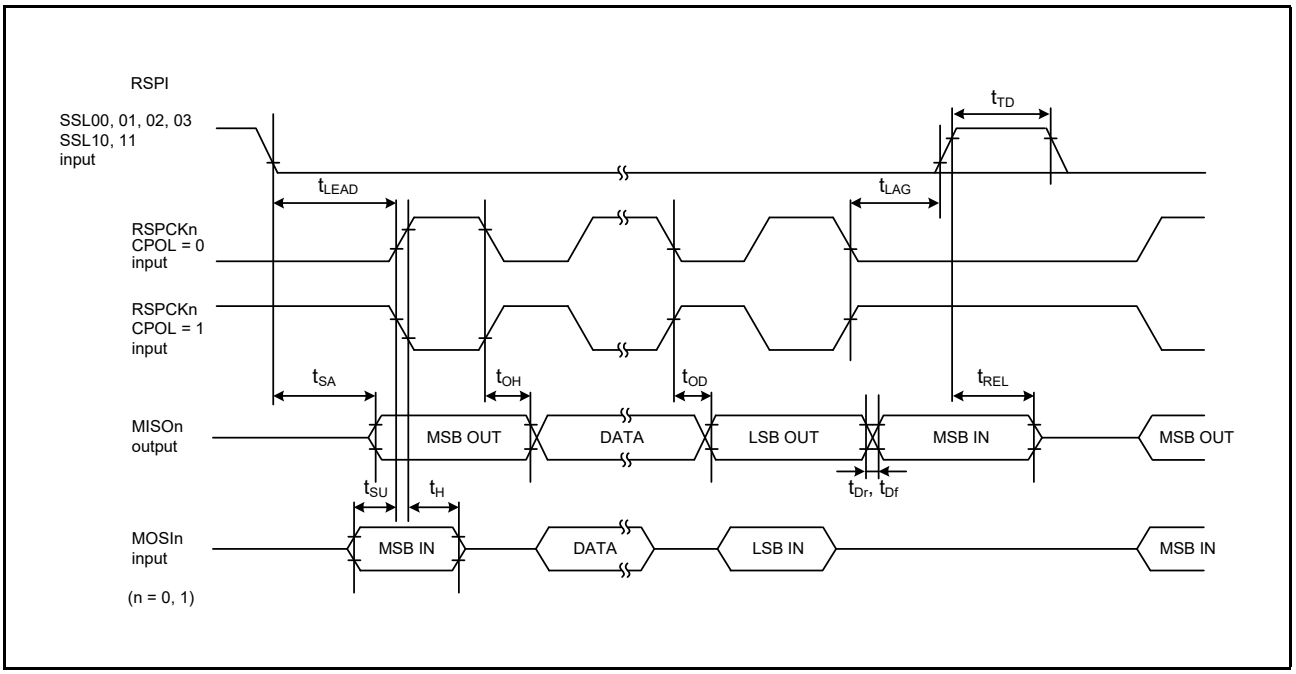


Figure 2.19 RSPI Timing (Slave, CPHA = 0)

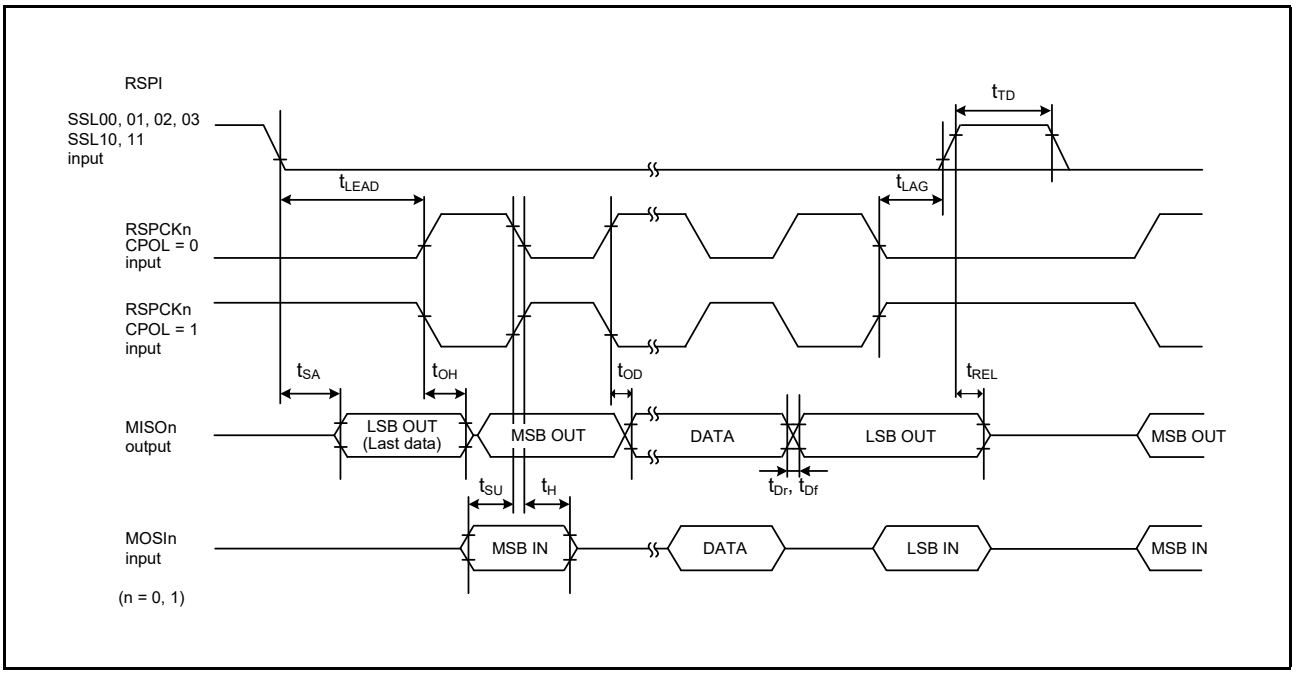


Figure 2.20 RSPI Timing (Slave, CPHA = 1)

2.4.3.7 SPIBSC Timing

Table 2.18 SPIBSC Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min	max	Unit*1	Test Conditions
SPIBSC	SPBCLK clock cycle	t_{SPBcyc}	2	4080	t_{PAcyc}	Figure 2.21
	SPBCLK high level pulse width	t_{SPBWH}	0.45	0.55	t_{SPBcyc}	
	SPBCLK low level pulse width	t_{SPBWL}	0.45	0.55	t_{SPBcyc}	
	Data input setup time	t_{SU}	3.5	—	ns	Figure 2.22, Figure 2.23, Figure 2.24
	Data input hold time	t_{H}	0.5	—	ns	
	SSL setup time	t_{LEAD}	1 × t_{SPBcyc} – 3	8 × t_{SPBcyc}	ns	
	SSL hold time	t_{LAG}	1.5 × t_{SPBcyc}	8.5 × t_{SPBcyc} + 3	ns	
	Continuous transfer delay time	t_{TD}	1	8	t_{SPBcyc}	
	Data output delay time	t_{OD}	—	3.6	ns	
	Data output hold time	t_{OH}	-1	—	ns	
	Data output buffer on time	t_{BON}	—	3.6	ns	Figure 2.25, Figure 2.26, Figure 2.27
	Data output buffer off time	t_{BOFF}	-7	0	ns	

Note 1. t_{PAcyc}: PCLKA cycle

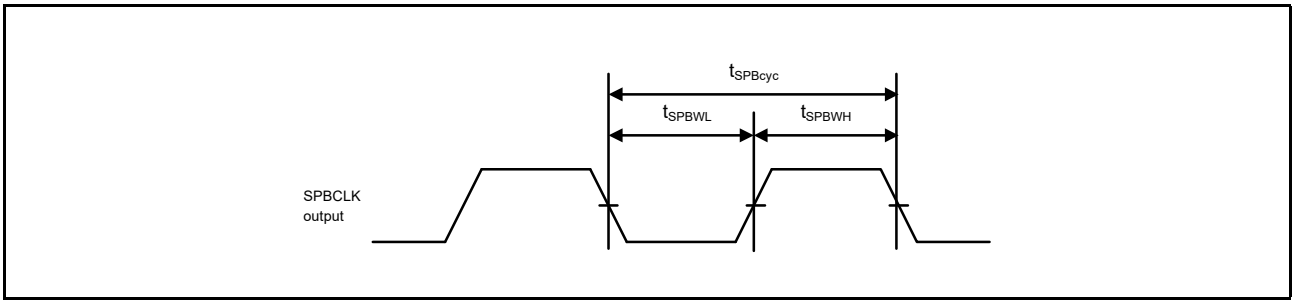


Figure 2.21 SPIBSC Clock Timing

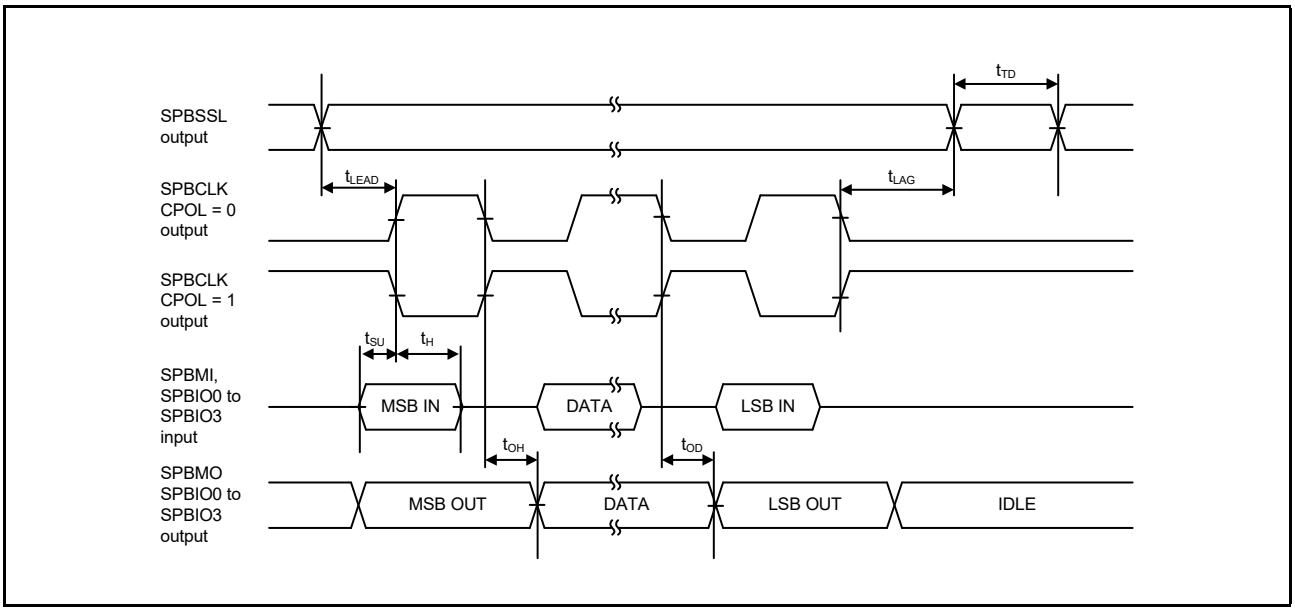


Figure 2.22 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 0)

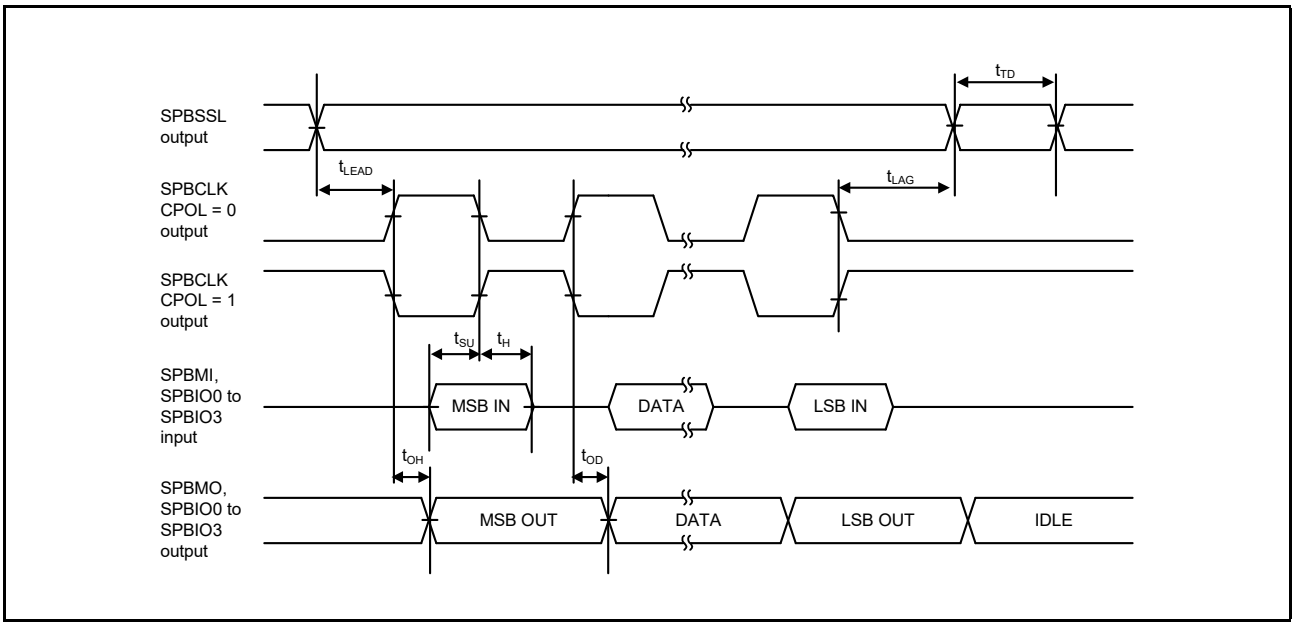


Figure 2.23 SPIBSC Transmit/Receive Timing (CPHAT = 1, CPHAR = 1)

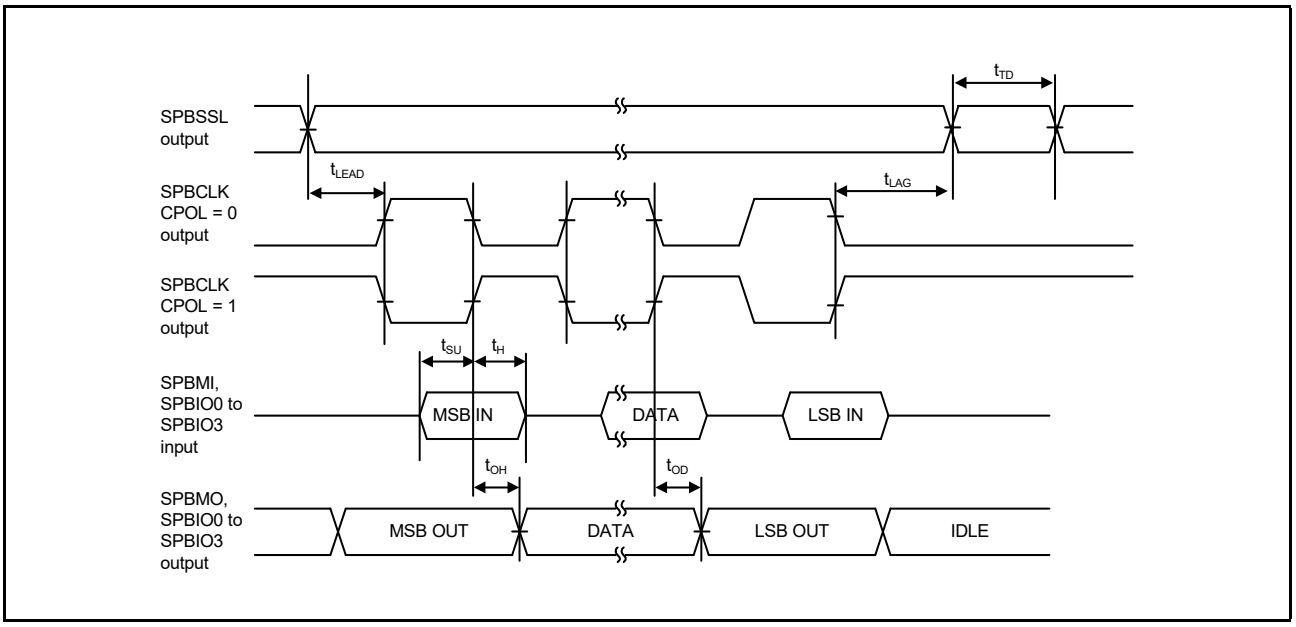


Figure 2.24 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1)

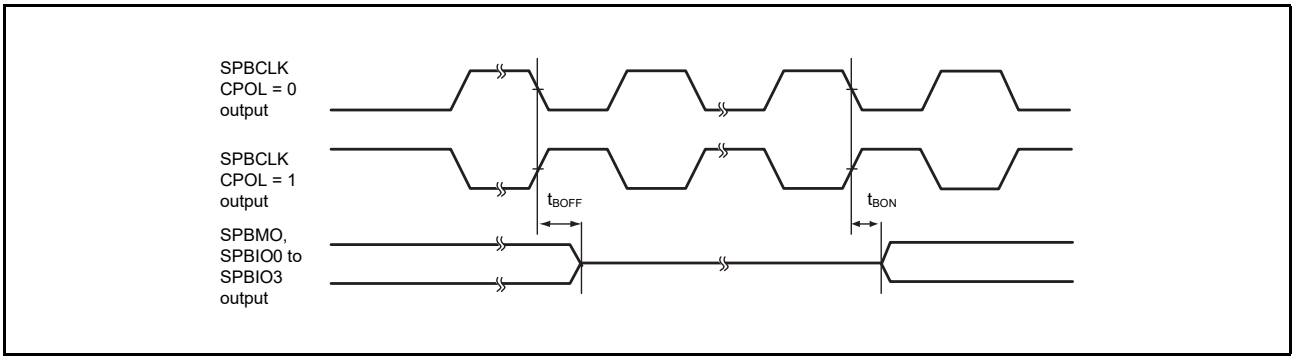


Figure 2.25 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 0)

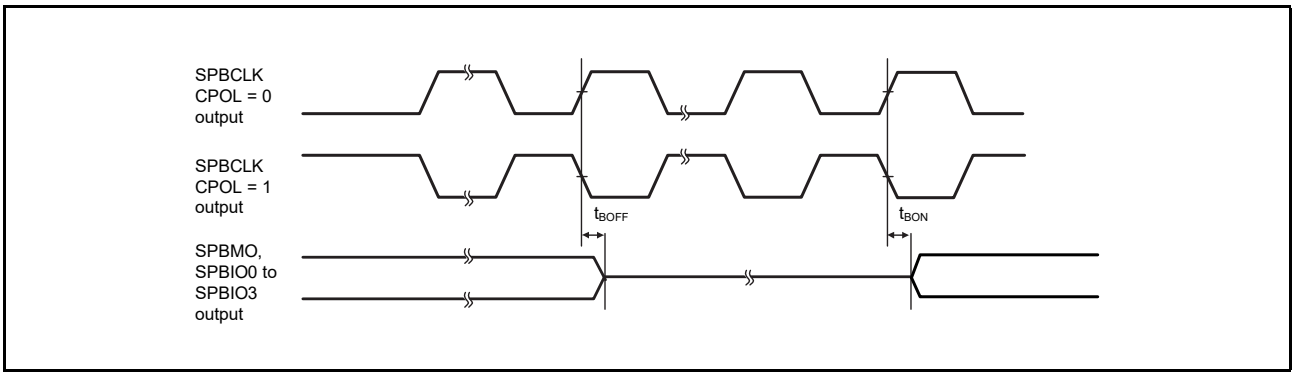


Figure 2.26 SPIBSC Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)

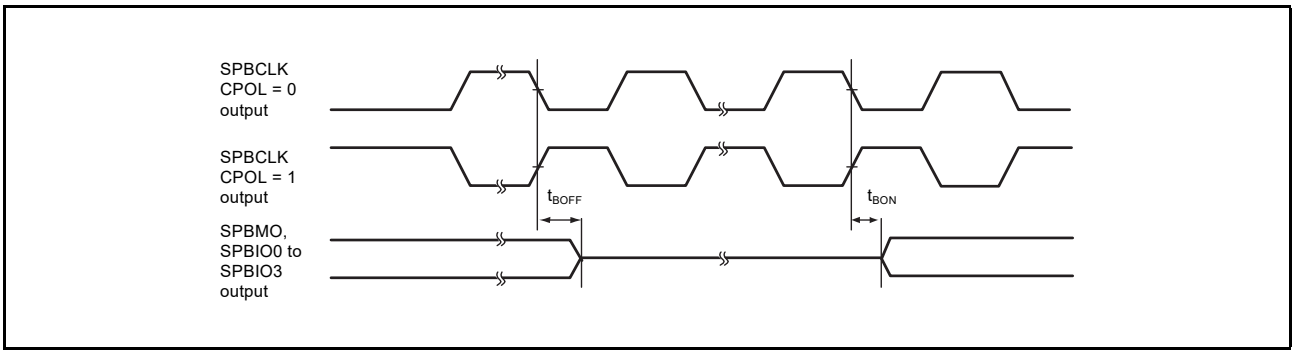


Figure 2.27 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 1)

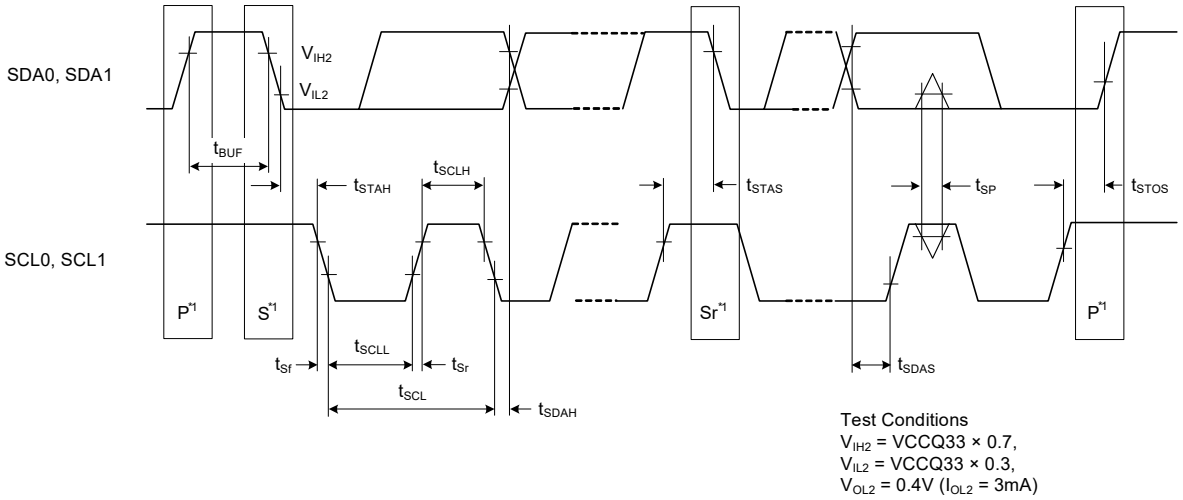
2.4.3.8 RIICa Timing

Table 2.19 RIICa Timing

Output load conditions: V_{OL2} = 0.4 V, I_{OL2} = 3 mA

Item		symbol	min*2	max*2	Unit*1	Test Conditions
RIICa (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.28
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—	1000	ns	
	SCL, SDA input falling time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIICa (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—*4	300	ns	
	SCL, SDA input falling time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle
Note 2. The value out of parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.
Note 3. C_b is the total capacitance of the bus lines.
Note 4. The minimum values are not specified for tsr and tsf in Fast-mode.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.28 RIICa Bus Interface Input/Output Timing

2.4.3.9 Serial Management Interface Timing

(1) Serial Management Interface (Slave) Timing

Table 2.20 Serial Management Interface (Slave) Timing*1

Output load conditions: V_{OH12} = 1.0V, V_{OL12} = 0.2V, C = 30pF

Item	Symbol	min	max	Unit	Test Conditions
MDC input cycle	t_{MDC}	250	—	ns	Figure 2.29
MDIO setup time	t_{SMDIO}	10	—	ns	
MDIO hold time	t_{MHDIO}	10	—	ns	
MDIO output delay time	t_{DMDIO}	—	175	ns	

Note 1. When the DSCR register for the P50, P51, P52, P53, P54, P55, and P56 pins is set to 11 (1.2-V driving output)

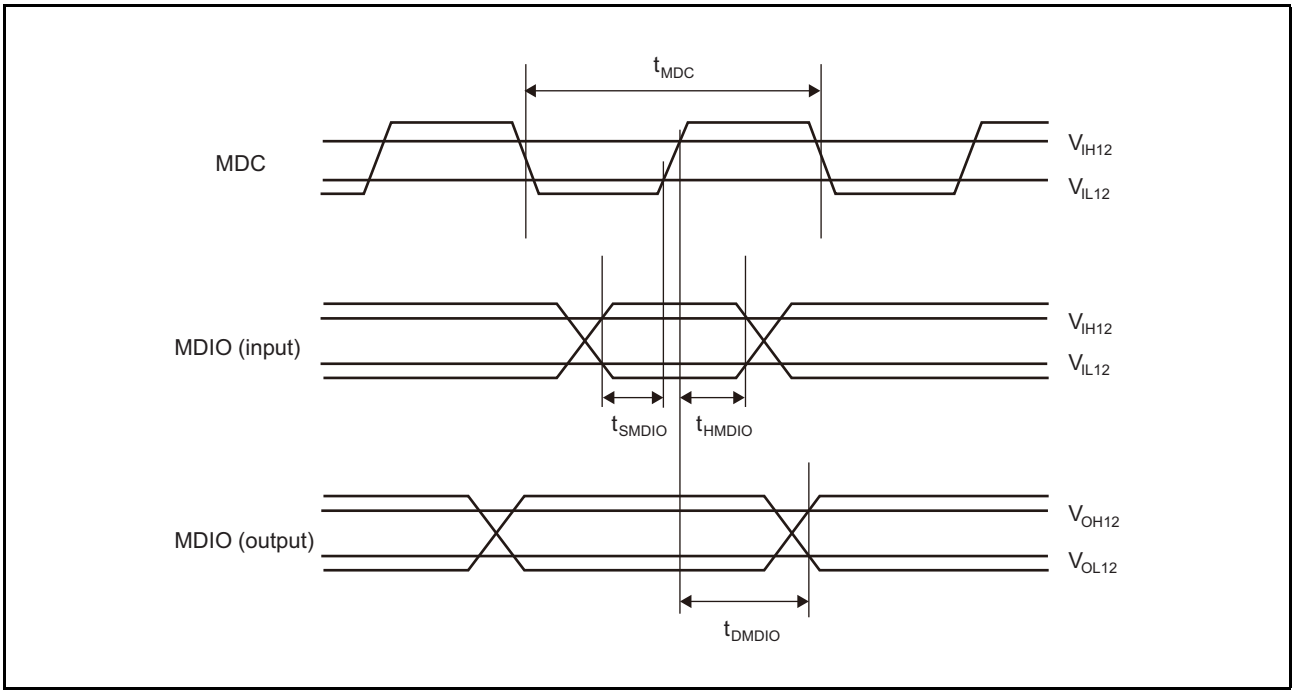


Figure 2.29 Serial Management Interface (Slave) Timing

(2) Serial Management Interface (Master, Channel 1) Timing

Table 2.21 Serial Management Interface (Master, Channel 1) Timing

Output load conditions: V_{OH1} = VCCQ33 – 0.5V, V_{OL1} = 0.4V, C = 30pF

Item	Symbol	min	max	Unit	Test Conditions
MDC output cycle	t_{MMDC1}	100	—	ns	Figure 2.30
MDIO setup time	$t_{SMMDIO1}$	40	—	ns	
MDIO hold time	$t_{HMMDIO1}$	0	—	ns	
MDIO output delay time	$t_{DMMDIO1}$	-20	20	ns	

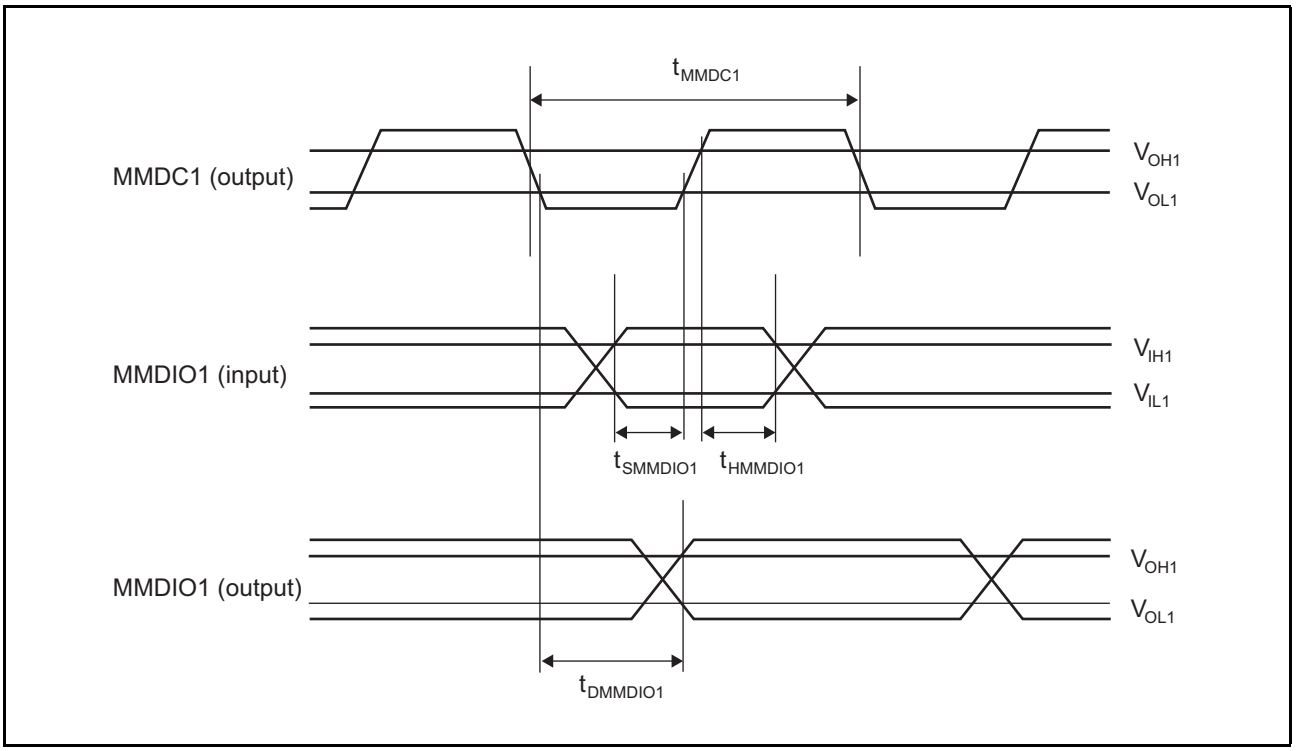


Figure 2.30 Serial Management Interface (Master, Channel 1) Timing

2.5 A/D Conversion Characteristics

- Conditions: VDD = VCCQ12 = PLLVDD0 = PLLVDD1 = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = 3.0 to 3.6 V
  VREFH0 = 3.0 to 3.6 V (AVCC0 ≥ VREFH0),
  VREFH1 = 3.0 to 3.6 V (AVCC1 ≥ VREFH1),
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = 0 V,
  Tj = -40 to 110°C

Table 2.22 12-Bit A/D (Unit 0) Conversion Characteristics 1 (1 / 2)

Item		min	typ	max	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN003) When disconnection detection assistance is in use	Conversion time[*1] (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0 kΩ	1.2 (0.4 + 0.4) [*2]	—	3.6	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 24 states
	Offset error	—	—	±7.5	LSB	
	Full-scale error	—	—	±7.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±7.5	LSB	
	DNL differential nonlinearity error	—	—	±3.0	LSB	
	INL integral nonlinearity error	—	—	±4.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	3.2	µs	Self-diagnosis + 4-channel simultaneous sampling
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN003) When disconnection detection assistance is not in use	Conversion time[*1] (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0 kΩ	1.2 (0.4 + 0.4) [*2]	—	3.6	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 24 states
	Offset error	—	—	±6.5	LSB	
	Full-scale error	—	—	±6.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.5	LSB	
	DNL differential nonlinearity error	—	—	±3.0	LSB	
	INL integral nonlinearity error	—	—	±4.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	3.2	µs	Self-diagnosis + 4-channel simultaneous sampling
	Dynamic range	0.25	—	VREFH0 – 0.25	V	

Table 2.22 12-Bit A/D (Unit 0) Conversion Characteristics 1 (2 / 2)

Item		min	typ	max	Unit	Test Conditions
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0 kΩ	0.483 (0.267)*2	—	—	µs	Sampling in 16 states
	Offset error	—	—	±5.0	LSB	
	Full-scale error	—	—	±5.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	
	DNL differential nonlinearity error	—	—	±2.5	LSB	
	INL integral nonlinearity error	—	—	±3.0	LSB	

Note 1. The conversion time is the total of the sampling time and the comparison time (t_{SPLSH} + t_{CONV} in Figure 30.22 and Figure 30.23 in section 30, 12-Bit A/D Converter (S12ADCa)). The number of sampling states is indicated for each item in Test Conditions.
Note 2. The value in parentheses indicates the sampling time.

Table 2.23 12-Bit A/D (Unit 1) Conversion Characteristics 1

Item		min	typ	max	Unit	Test Conditions
Resolution		8	—	12	Bit	
Conversion time*1 (Operation at PCLKF = 60 MHz)	Permissible signal source impedance Max. = 1.0 kΩ	0.883 (0.667)*2	—	—	µs	Sampling in 40 states
Analog input capacitance		—	—	30	pF	
Offset error		—	—	±6.0	LSB	
Full-scale error		—	—	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	—	±6.0	LSB	
DNL differential nonlinearity error		—	—	±3.0	LSB	
INL integral nonlinearity error		—	—	±4.0	LSB	

Note 1. The conversion time is the total of the sampling time and the comparison time (t_{SPLSH} + t_{CONV} in Figure 30.22 and Figure 30.23 in section 30, 12-Bit A/D Converter (S12ADCa)). The number of sampling states is indicated for each item in Test Conditions.
Note 2. The value in parentheses indicates the sampling time.

- Conditions: VDD = VCCQ12 = PLLVDD0 = PLLVDD1 = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = 3.0 to 3.6 V,
  VREFH0 = 2.5 to 3.0 V (AVCC0 ≥ VREFH0),
  VREFH1 = 2.5 to 3.0 V (AVCC1 ≥ VREFH1),
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = 0 V
  Tj = -40 to 110ºC

Table 2.24 12-Bit A/D (Unit 0) Conversion Characteristics 2

Item		min	typ	max	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN007)	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0kΩ	0.883 (0.667) *2	—	—	µs	Sampling in 40 states
When disconnection detection assistance is not in use	Offset error	—	—	±8.7	LSB	
	Full-scale error	—	—	±8.7	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.7	LSB	
	DNL differential nonlinearity error	—	—	±5.0	LSB	
	INL integral nonlinearity error	—	—	±6.0	LSB	

Note 1. The conversion time is the total of the sampling time and the comparison time (t_{SPLSH} + t_{CONV} in Figure 30.22 and Figure 30.23 in section 30, 12-Bit A/D Converter (S12ADCa), in the RZ/T1-M Group User's Manual:Hardware). The number of sampling states is indicated for each item in Test Conditions.
Note 2. The value in parentheses indicates the sampling time.

Table 2.25 12-Bit A/D (Unit 1) Conversion Characteristics 2

Item		min	typ	max	Unit	Test Conditions
Resolution		8	—	12	Bit	
Conversion time*1 (Operation at PCLKF = 60 MHz)	Permissible signal source impedance Max. = 1.0kΩ	0.883 (0.667)*2	—	—	µs	Sampling in 40 states
Analog input capacitance		—	—	30	pF	
Offset error		—	—	±8.7	LSB	
Full-scale error		—	—	±8.7	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	—	±8.7	LSB	
DNL differential nonlinearity error		—	—	±5.0	LSB	
INL integral nonlinearity error		—	—	±6.0	LSB	

Note 1. The conversion time is the total of the sampling time and the comparison time (t_{SPLSH} + t_{CONV} in Figure 30.22 and Figure 30.23 in section 30, 12-Bit A/D Converter (S12ADCa), in the RZ/T1-M Group User's Manual:Hardware). The number of sampling states is indicated for each item in Test Conditions.
Note 2. The value in parentheses indicates the sampling time.

2.6 Temperature Sensor Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = 0 V,
  Tj = -40 to 110°C

Table 2.26 Temperature Sensor Characteristics

Item	min	typ	max	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (at 25°C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	µs	
Sampling time	4.25	—	—	µs	ADSSTRT.SST[7:0] = 255 states (when PCLKF [ADC (unit0) sampling CLK] = 60 MHz)

2.7 Oscillation Stop Detection Timing

Table 2.27 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	min	typ	max	Unit	Test Conditions
Clock switching time	t_{dr}	—	—	1	ms	Figure 2.31

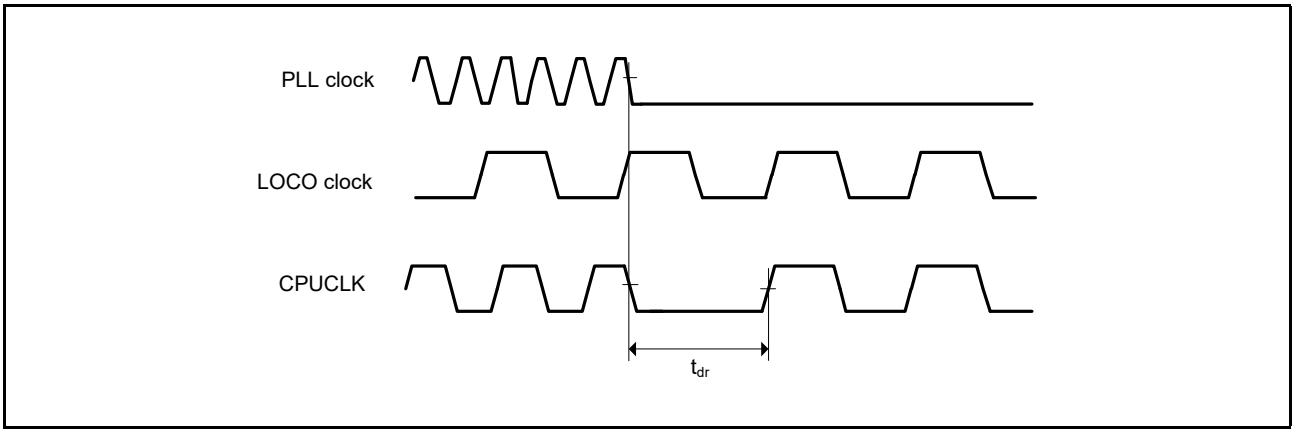


Figure 2.31 Oscillation Stop Detection Timing

2.8 Debug Interface Timing

Table 2.28 Debug Interface Timing

Output load conditions: V_{OH} = VCCQ33 – 0.5 V, V_{OL1} = 0.4 V

Item	Symbol	Min.	Max.	Unit	Reference Figure
TCK cycle time	t_{TCKcyc}	30	—	ns	Figure 2.32
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	5	—	ns	Figure 2.33 Output load: 30 pF
TDI hold time	t_{TDIH}	5	—	ns	
TMS/SWDIO setup time	t_{TMSS}	5	—	ns	
TMS/SWDIO hold time	t_{TMSH}	5	—	ns	
SWDIO delay time	t_{SWDO}	—	15	ns	
TDO delay time	t_{TDOD}	—	15	ns	
Trace clock cycle	t_{TCYC}	26.6	—	ns	Figure 2.34 Output load: 15 pF
Trace data delay time	t_{TDT}	0.25 × t_{TCYC} – 2	0.25 × t_{TCYC} + 2	ns	

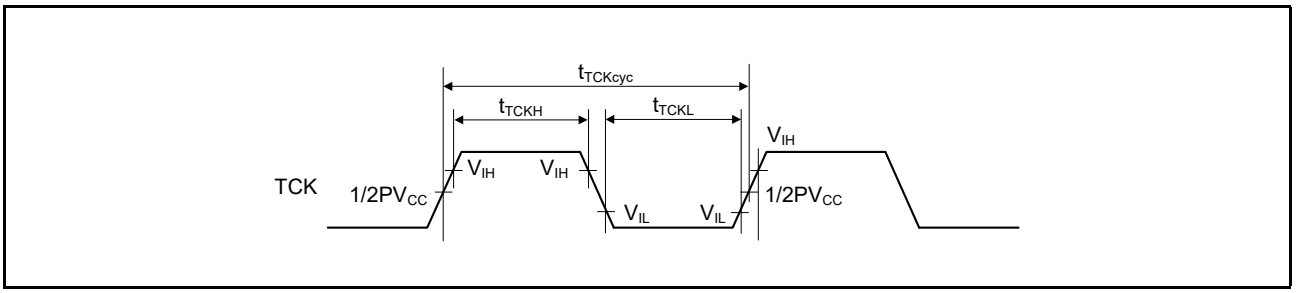


Figure 2.32 TCK Input Timing

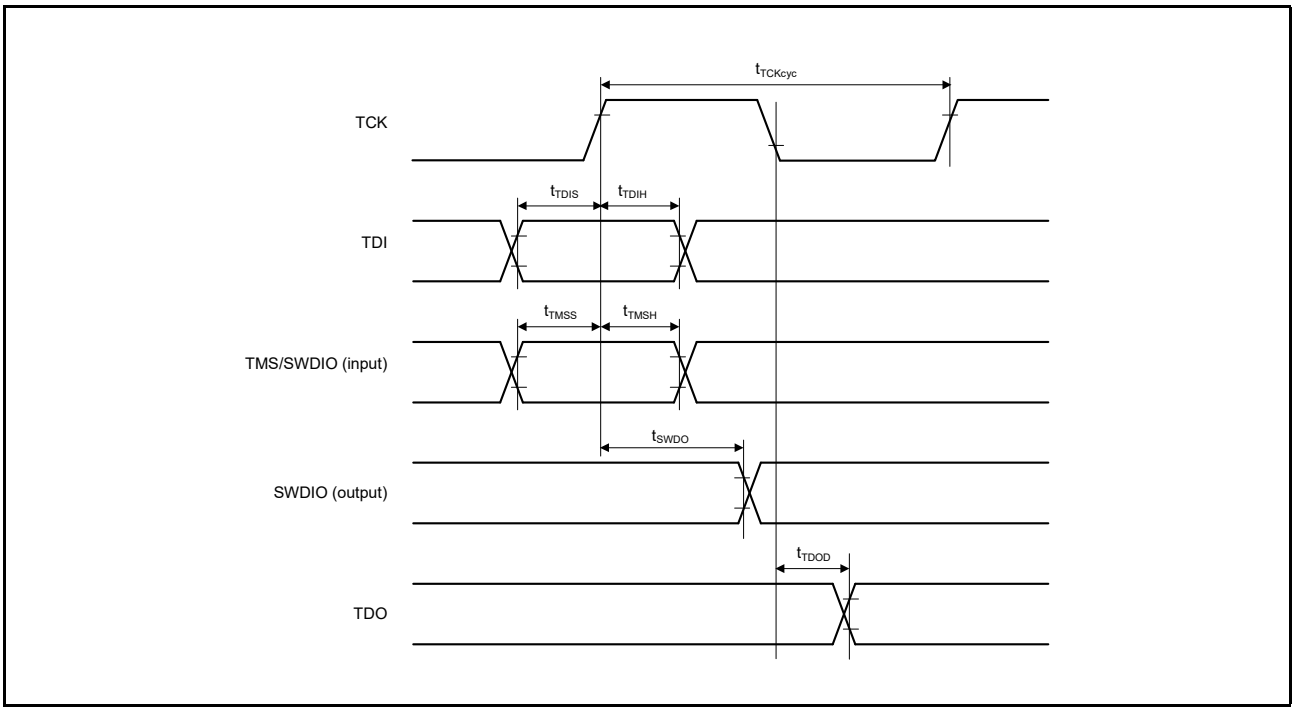


Figure 2.33 Data Transfer Timing

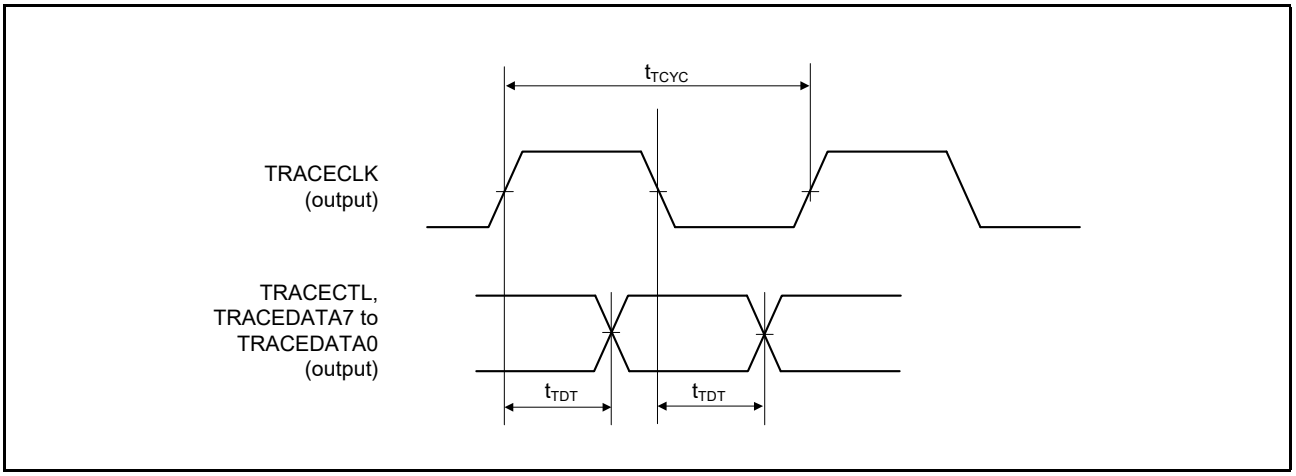


Figure 2.34 Trace Interface Timing

REVISION HISTORY — RZ/T1-M Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.60	Nov. 14, 2014	—	First edition, issued
0.70	Dec. 25, 2014	Features	
		1	■Operating temperature range: Heading title and description corrected
1.10	Aug. 22, 2016	Feature	
		1	Wholly amended
		1. Overview	
		2 to 19	Wholly amended
		2. Electrical Characteristics	
		20 to 51	Newly added
1.20	Mar. 02, 2017	1. Overview	
		2	1.1 Outline of Specifications: Description modified
		5	Table 1.1 Outline of Specifications (4 / 4), 12-bit A/D converter: Conversion time modified
		15	Table 1.5 Pin Assignments (112-Pin FBGA) (2 / 3), Pin number E4: Pin name modified
		17	Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (1 / 3), Pin number B11: Pin name for power supply, clock, and system control, modified
		18	Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (2 / 3), Pin number H3: Pin name for power supply, clock, and system control, modified
		2. Electrical Characteristics	
		23	Table 2.4 DC Characteristics (3)[*1] Item modified: "Input pull-up MOS current and resistance" and "Input pull-down MOS current and resistance" R_{pu1}, R_{pu2}, R_{pd1}, and R_{pd2} were added. Test conditions for "Input pull-down MOS current and resistance" were modified. Note 1 was added. Note 4 was modified. Description on ports P50 to P56 was deleted.
		40	Table 2.18 SPIBSC Timing, Test conditions: Reference figures added
1.30	Apr. 25, 2017	2. Electrical Characteristics	
		40	Figure 2.24 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1): Modified
1.40	Jul. 24, 2017	All	"Cortex-R4F" changed to "Cortex-R4"
		Features	
		1	Management data input/output interface (MDIO), changed
		1. Overview	
		2	Table 1.1 Outline of Specifications (1/4): General-purpose I/O ports: Number of I/O pins changed
		4	Table 1.1 Outline of Specifications (3/4): Management data input/output interface (MDIO): Description changed
		6	Table 1.1 Outline of Specifications: Note 3 added
		7	Table 1.2 List of Functions: MDIO changed to MDIO master/MDIO slave, Note 1 added
		8	Table 1.3 List of Products: Products added, option added
		9	Figure 1.1 Block Diagram, Note 1 deleted
		11	Table 1.4 Pin Functions (2/3): Management data input/output interface Management data input/output interface (MDIOM/MDIO): MDIO changed to MDIOM/MDIO, functions of MDC and MDIO added, MMDC0, MMDC1, MMDIO0, and MMDIO1 pins added, functions of PRTADR0 to PRTADR4 added
		12	Table 1.4 Pin Functions (3/3): I/O ports: P50 to P56 pins added, Note 2 added
		13	Figure 1.2 Pin Arrangement (112-pin FBGA) (Top View): Pin numbers C4, C5, E10, and F11 changed

Rev.	Date	Description	
		Page	Summary
1.40	Jul. 24, 2017	14	Table 1.5 Pin Assignments (112-Pin FBGA) (1/3): Pin names of pin numbers C4 and C5 changed
		15	Table 1.5 Pin Assignments (112-Pin FBGA) (2/3): Pin names of pin numbers E10 and F11 changed
		16	Table 1.5 Pin Assignments (112-Pin FBGA): Note 1 deleted
		17	Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (1/3): Communications pins of pin numbers C4 and C5 changed
		18	Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (2/3): Communications pins of pin numbers E10 and F11 changed
		19	Table 1.6 List of Pins and Pin Functions (112-Pin FBGA): Note 1 deleted
		2. Electrical Characteristics	
		22	Table 2.3 DC Characteristics (2) [Power Supply]: Characteristics in normal operation (VDD) changed
		23	Table 2.4 DC Characteristics (3): Applicable pins for the output high level voltage (VOH) changed
		24	Table 2.5 DC Characteristics for 1.2-V Pin: Input pull-up MOS current and resistance and Input pull-down MOS current and resistance added
		44	2.4.3.9 (1) Serial Management Interface (Slave) Timing: Title added
		44	Table 2.20 Serial Management Interface (Slave) Timing, changed
		44	Figure 2.30 Serial Management Interface Output Timing, deleted
		45	2.4.3.9 (2) Serial Management Interface (Master, Channel 0) Timing, added
		46	2.4.3.9 (3) Serial Management Interface (Master, Channel 1) Timing, added
1.50	Dec. 27, 2017	All	Cortex-R4F changed to Cortex-R4
		1. Overview	
		2	Table 1.1 Outline of Specifications (1 / 4): Description of the clock generation circuit modified
		3	Table 1.1 Outline of Specifications (2 / 4): Description of the independent watchdog timer (IWDTa) modified (120 MHz → 120 kHz)
		10	Table 1.4 Pin Functions (2 / 3): CTS0# to CTS2#: I/O and functional description changed; RTS0# to RTS2#: Functional description changed
		2. Electrical Characteristics	
		33	Table 2.17 RSPIa Timing: Note 2 added; Note 2 changed to Note 3
1.60	May 31, 2019	All	
		—	"ARM" was modified to "Arm"
		Features	
		1	Management data input/output interface (MDIO): Interface for DSP control, modified
		1. Overview	
		2	Table 1.1 Outline of Specifications (1/4): On-chip extended SRAM with ECC: "Operating frequency", added
		2	Table 1.1 Outline of Specifications (1/4): Direct memory access controller (DMAC): Activation sources, modified
		3	Table 1.1 Outline of Specifications (2/4): Compare match timer (CMT): Event linking, modified
		9	Table 1.4 Pin Functions (1/3): 16-bit timer pulse unit (TPUa): The descriptions of the individual pins, modified
		2. Electrical Characteristics	
		45	Table 2.22 Serial Management Interface (Master, Channel 1) Timing: Note 1 added to the title
1.70	Oct 23, 2020	All	Registered trademark symbol added (Arm → Arm®)
		1. Overview	
		8	Figure 1.1 Block Diagram: Unnecessary bus lines, deleted
		10	Table 1.4 Pin Functions (2 / 3): MDIOM/MDIO: Pins MMDC0 and MMDIO0, deleted

Rev.	Date	Description	
		Page	Summary
1.70	Oct 23, 2020	12	Figure 1.2 Block Diagram: Pins MMDC0 and MMDIO0, deleted
		13	Table 1.5 Pin Assignments (112-Pin FBGA) (1 / 3): Pins MMDC0 and MMDIO0, deleted
		16	Table 1.6 List of Pins and Pin Functions (112-Pin FBGA) (1 / 3): Pins MMDC0 and MMDIO0, deleted
		2. Electrical Characteristics	
		22	Table 2.4 DC Characteristics (3) The footnote number added: Three-state leakage current (off state) / 5-V tolerant pins / $\|I_{TSI}\|$ → Three-state leakage current (off state) / 5-V tolerant pins*2 / $\|I_{TSI}\|$
		41	Table 2.19 RIICa Timing: Note 4 modified
		—	2.4.3.9 Serial Management Interface Timing, (2) Serial Management Interface (Master, Channel 0) Timing, deleted Table 2.21 Serial Management Interface (Master, Channel 0) Timing, deleted Figure 2.30 Serial Management Interface (Master, Channel 0) Timing, deleted
		44	Table 2.21 Serial Management Interface (Master, Channel 1) Timing: Note 1 deleted

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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