RZ/G3E Group

RZ Family, RZ/G Series

R01DS0477EJ0115
Rev.1.15
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Features

This LSI includes:

■ CPU

- On-chip Quad 64-bit Arm® Cortex®-A55 Core processors [Quad/Dual option]

  Application processing (up to 1.8 GHz)
- 32-bit Arm® Cortex®-M33 processor

  System management (up to 200 MHz)

■ Boot

- Selectable boot CPU from Arm® Cortex®-M33 or Arm® Cortex®-A55

■ Micro Neural network processing unit (NPU)

- NPU of Arm® Ethos-U55 (1 GHz) [option]

■ Video and Graphics

- H.264/H.265 Video codec unit (VCD)
- 3D Graphics Engine of Arm® Mali-G52
- Image Scaling Unit (VSP)
- Frame Data Processor (FDP)

■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (512-Kbyte on-chip SRAM with ECC)
- External DDR memory interface

  1-channel memory controller for LPDDR4-3200 or LPDDR4X-3200 with a 32-bit bus width
- xSPI interface
- SDHI (eMMC/SD (1-, 4-, 8-bit bus width) supported)

■ Camera and display interfaces

- MIPI CSI-2 (1 ch.: 1, 2, or 4 lanes)
- Selectable 2 display interfaces from the following

  MIPI DSI (1 ch.: 1, 2, or 4 lanes)

  Parallel interface (1 ch.)

  LVDS (2 ch.)

■ Various communication/storage/network interfaces

- Ethernet (2 ch.: 10/100/1000 BASE)
- USB2.0 (1 ch.: Host/Function, 1 ch.: Host-only)
- USB3.2 Gen2 × 1 (Host-only)
- PCIe Gen3 × 1 (1 or 2 lanes)
- CAN/CANFD (compliant with ISO11898-1) (6 ch.)
- SCI (10 ch.: UART/SPI/I2C-host)
- SPI (3 ch.)
- I2C (9 ch.)
- I3C (1 ch.)

■ Extended-function timers

- 32-bit general-purpose timer (16 ch.)
- 32-bit CMTW (8 ch.)

■ Audio

- Asynchronous sampling rate converter unit (SCU) (up to 192 kHz)
- DMAC for Audio (ADMAC) is available to transfer audio formats of I2S with SCU.
- Flexible audio clock generator (ADG) for audio functions.
- I2S (TDM) input/output interfaces (half-duplex 10 ch.; full-duplex 5 ch.)
- SPDIF input/output interfaces (3 ch.)
- Pulse density modulation (PDM) input interfaces (6 ch.)

■ Analog/Digital converter (ADC) and sensors

- 2.5 Msps 12-bit ADC (8 ch.)
- Internal temperature sensors (1 ch.)

■ Security

- Hardware cryptographic engine

NOTE

The products with #AC0 or #BC0 in the part number have the following restrictions.

- Not supported controlling MIPI LCDs with the Display Command Set over MIPI-DSI.
- Not supported the applications of the Ethos-U55 utilizing the LPDDR4/LPDDR4X.

1. Overview

1.1 Outline of Specification

1.1.1 CPU

Item	Description
Application Processor Cortex-A55 (CA55) [Quad/Dual option]	• Arm Cortex-A55 Quad Core 1.8 GHz with 0.9 V, 1.1 GHz with 0.8 V • L1 I-cache 32 Kbytes (with parity) and D-cache 32 Kbytes (with ECC) per core • L2 cache: 0 Kbyte • L3 cache: 1 Mbyte (with ECC) • MMU supported • Neon™ and FPU supported • Cryptographic extension supported • Armv8-A architecture
System Manager Cortex-M33 (CM33)	• Arm Cortex-M33 Processor 200 MHz • FPU supported • DSP Extension supported • Security Extension supported • Armv8-M architecture
Debug Interface	• Arm® CoreSight® architecture • JTAG and SWD interfaces supported • ETF: Total of 60 Kbytes for program flow tracing • JTAG disabling supported [option]

1.1.2 Boot

Item	Description
Boot	• Selectable boot from Arm Cortex-A55 or Arm Cortex-M33 • CA55 boot – Boot Mode 0: Booting from eSD – Boot Mode 1: Booting from eMMC 3.3 V – Boot Mode 2: Booting from a serial flash memory connected to the xSPI bus space 3.3 V – Boot Mode 3: Booting from SCIF download – Boot Mode 4: Booting from USB download – Boot Mode 5: Booting from eMMC 1.8 V – Boot Mode 6: Booting from a serial flash memory connected to the xSPI bus space 1.8 V • CM33 boot – Boot Mode 2: Booting from a serial flash memory connected to the xSPI bus space 3.3 V – Boot Mode 3: Booting from SCIF download – Boot Mode 6: Booting from a serial flash memory connected to the xSPI bus space 1.8 V

1.1.3 NPU

Item	Description
Micro Neural network Processing Unit (NPU) [option]	• Arm Ethos-U55 1.0 GHz • 256MAC • 0.5 TOPS

1.1.4 Graphics Unit

Item	Description
3D Graphics Engine (GE3D)	• Arm Mali-G52 630 MHz • 64 Kbytes L2 cache • Vulkan 1.2 supported • OpenGL ES™ 1.1, 2.0, and 3.2 supported • OpenCL 2.0 full profile supported

1.1.5 Video Processing Unit

Item	Description
Video Codec Unit (VCD)	• H.264/H.265 codec module • Support for encoding and decoding – H.264/AVC (High Profile, level 4.2; Main Profile, level 4.2; Baseline Profile, level 4.2) – H.265/HEVC (Main Profile, level 5) • I-/P-slice supported for H.264/H.265 encoding I-/P-/B-slice supported for H.264/H.265 decoding • Maximum size – (H.264) 1920 × 1080 × 60 fps*1 – (H.265) 3840 × 2160p × 30 fps*1
Frame Data Processor (FDP)	• 1 channel • Tile-Linear conversion supported • 500 Mpix/s for output performance • Supports various image formats • Input: YCbCr444/422/420 • Output: YCbCr444/422/420 and RGB/αRGB • Input image Size (max): 3840 × 2160 • Output image Size (max): 3840 × 2160 • Not support Interlace format
Video Signal Processor (VSP)	• Scaling up & down function • Supports Various Data Formats and Conversion – Color space conversion and changes to the number of colors by dithering – Color keying • Supports combination between pixel alpha and global alpha • Supports generating pre multiplied alpha • Video Processing – Up and down scaling with arbitrary scaling ratio(×16 to ×1/15.9997) – Super resolution processing – Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270° • Picture Quality/Color Correction with 1D/3D Look Up Table (LUT) – Hue, brightness, and saturation adjustment – 1D and 2D histogram • Following functions will be supported by Renesas software portfolio. – γ correction and gain correction – Correction of color • Input image size (max): 3840 × 2160 • Output image size (max): 3840 × 2160

Note 1. Maximum frame rate for this size. The number of streams can be defined within this specification by software.

1.1.6 Internal Memory

Item	Description
System RAM	• 512 Kbytes (with ECC)

1.1.7 External Memory Interface

Item	Description
External Bus Controller for LPDDR4/4X SDRAM (DDR)	• 1 channel • Support LPDDR4X-3200 Bus width: 32-bit Memory Size: Up to 4 GBytes, Single rank (15 mm PKG, 21 mm PKG) • Support LPDDR4-3200 Bus width: 32-bit Memory Size: Up to 4 GBytes, Single rank (15 mm PKG, 21 mm PKG) Memory Size: Up to 8 GBytes, Dual rank (15 mm PKG) • In line ECC supported (support for error detection interrupts) • Auto Refresh/Self Refresh/IO Retention supported • Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported)
xSPI Controller (xSPI)	• 1 channel (2 chip select signals) • Compliant with the xSPI protocol • Protocol mode 1, 4, or 8 pins with SDR or DDR (1S-1S-1S, 4S-4D-4D*1, 8D-8D-8D*1) 2 or 4 pins with SDR (1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S) • Support for XiP mode • Support for up to 256-Mbyte address space (support for up to 128 Mbytes per channel address space in boot sequence)
SD Card Host Interface/ Multimedia Card Interface (SD/MMC)	• 3 channels Channel 0 supports SDHI/e-MMC (boot supported) Channel 1 supports SDHI/e-MMC Channel 2 supports SDHI • SD memory I/O card interface (1-bit/4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD specification version 3.01 • Default, high-speed, UHS-I/SDR50, SDR104 and DDR50 transfer modes supported • Error check function: CRC7 (Command), CRC16 (Data) • Support for card detection and write protection • MMC interface Channel 0 (1-bit/4-bit/8-bit MMC bus) Channel 1 (1-bit/4-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 4.51 • High-speed, HS200 and HS-DDR transfer modes supported

Note 1. DDR access without DS (XSPI0_DS) is not supported.

1.1.8 CPU Peripheral

Item	Description
Clock Pulse Generator (CPG)	• Generates the clocks from an external clock or external resonator (24 MHz). – Maximum Arm Cortex-A55 clock: 1.8 GHz with Over Drive (0.9 V) – Maximum Arm Cortex-M33 clock: 200 MHz – Maximum DDR clock: 800 MHz (LPDDR4/4X-3200) – Maximum 3DGE clock: 630 MHz – Maximum VSP clock: 800 MHz – Maximum NPU clock: 1.0 GHz – Maximum H.264/H.265 clock: 400 MHz – Maximum System Bus clock: 400 MHz • SSC (Spread Spectrum Clock) supported
Direct Memory Access Controller (DMAC)	• 80 channels • Transfer modes: Single transfer mode and block transfer mode • LINK mode (DMA transfer under descriptor control) supported • Transfer size: 1, 2, 4, 8, 16, 32, 64, or 128 bytes • Transfer request: Software trigger, external DMA requests (DREQ) and interrupt requests from peripheral functions • A specific DMA transfer interval can be specified to adjust the bus occupancy.
Interrupt Controller	• Arm® CoreLinkTM Generic Interrupt Controller (GIC-600) for Arm Cortex-A55 (32 priority levels available) • Nested Vectored Interrupt Controller (NVIC) for Arm Cortex-M33 • External Interrupt pins (NMI, IRQ0 to IRQ15, and TINT0 to TINT31) • On-chip peripheral Interrupts: priority level set for each module
Event Link Controller (ELC)	• Up to 455 event signals can be interlinked with the operation of modules • In particular, the operation of timer modules can be started by input event signals • Event-linked operation of signals of 16 ports P10~17, P70~77 is to be possible.
Error Controller	• Error events from CPU and peripherals are captured and merged to interrupt with mask for Arm Cortex-A55 and Arm Cortex-M33 respectively. • System reset can be generated by error events.
Message Handling Unit (MHU)	• Message handling function between Arm Cortex-A55 and Arm Cortex-M33 • Assert interrupt to inform message and response from/to every core
General-purpose I/O (GPIO)	• 141 General-purpose I/O ports

1.1.9 Camera Interface

Item	Description
MIPI CSI-2 Interface with camera image processing (CRU)	• Number of lanes: 1, 2, or 4 lanes • Maximum bandwidth: 2.1 Gbps per lane • Support for the throughput up to FullHD RAW12 60 fps • Support for 4 virtual channels selected from VC0 to VC15 • Support for input data formats: • YUV422 8 bits or 10 bits • RGB444, RGB555, RGB565, RGB666, RGB888 • RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20 • YUV420 8-bits or 10-bits (image processing not supported) • Legacy YUV420 8-bits (image processing not supported) • YUV420 8-bits or 10-bits (chroma shifted pixel sampling) (image processing not supported) • User defined byte-based data • The other formats from the MIPI CSI-2 interface can also be output without image processing. • Generic long packet data types 1 to 4 • User defined 8-bit data types 1 to 8

1.1.10 Display Interfaces

Item	Description
LCD Controller	• 2 channels • 2 planes blending (can blend 2 different size images) • Support Image Processing: – Dither processing (RGB666) – Clipping – RGB Gamma Correction LUT • Support Input Data Format: – RGB565/RGB666/RGB888 – ARGB1555/ARGB4444/ARGB8888 – YCbCr444 8-bit/YCbCr422 8-bit/YCbCr420 8-bit • Selectable 2 display interfaces from the following – 1 channel MIPI DSI (1/2/4-Lane) interface – 1 parallel interface – 2 LVDS interfaces • Support 1920 pixels × 1920 lines Pixel clock must be within the following range – MIPI DSI = 5.4 to 187.5 MHz – Parallel = 5.4 to 87 MHz – LVDS (single) = 25 to 87 MHz – LVDS (dual) = 50 to 174 MHz
MIPI DSI Interface	• 1 channel • The number of Lanes: 1,2, or 4-lane • Support 1920 × 1200, 60 fps (RGB888) • Maximum Bandwidth: 1.5 Gbps per lane • Support Output Data Format: RGB666/RGB888
Parallel Output Interface	• 1 channel • Support WXGA (1280×800), 60 fps • Support Output Data Format: RGB666/RGB888 • CLK/HD/VD timing signal supported
LVDS Interface	• 2 channels • Number of support lanes – Single-link: 4 lanes (Data) + 1 lane (Clock) – Single-link (2 ch.): 8 lanes (Data) + 2 lanes (Clock) – Dual-link：8 lanes (Data) + 2 lanes (Clock) • Single-link target – RGB888 640×480 (VGA) – RGB888 800×480 (QVGA) – RGB888 1366×768 60 Hz (WXGA) – RGB888 1280×800 60 Hz (WXGA) • Dual-link target – RGB888 1920×1200 60 fps (~3.32 Gbps) – RGB888 1920×1080 60 fps (~2.99 Gbps) • Output clock range: 25 to 87 MHz • Clock Duty: 4:3 • Color: 8 bits • ViD: 250 to 450 mV • Vcm (Vos): 1.125 to 1.375 V • SSC supported

1.1.11 Storage and Network

Item	Description
USB3.2 Host (USB3)	• 1 channel • Compliance with USB3.2 Gen2 • Maximum rate: 10 Gbps • Supports Control/Bulk/Interrupt/Isochronous transfer • Internal dedicated DMA
USB2.0 Host/Function (USB2)	• 2 channels (ch. 0: Host-Function, ch. 1: Host only) • Compliance with USB2.0 • Support for On-The-Go (OTG) functionality (ch. 0 only) • Supports Control/Bulk/Interrupt/Isochronous transfer • Internal dedicated DMA
PCI Express 3.0 (PCIE)	• 1 channel • PCIe Gen3 • Root complex or Endpoint selectable • 2-lane
Gigabit Ethernet Interface (GBETH)	• 2 channels • Compliant with IEEE802.3 • Compliant with IEEE802.1Qav, IEEE802.1Qat, IEEE802.1AS • Compliant with IEEE1588-2008 with nano second timer in ch. 0 (master) and ch. 1 (slave) • Supports 10BASE, 100BASE, 1000BASE • Supports full duplex and half duplex • Supports RGMII/MII Interfaces
CANFD Interface (RS-CANFD)	• 6 channels • CAN-FD ISO 11898-1 (2015) compliant • Support up to 8 MHz with payload transfer • Message buffer – 64 transmit message buffers per channel – 256 shared buffers for RXMB and FIFO buffers per channel

1.1.12 Peripheral Module

Item	Description
I3C Bus Interface (I3C)	• 1 channel • Support for 1.2 V and 1.8 V • Master or Slave mode selectable • Support for the multi-master • Compliant with MIPI I3C v1.0 and I3C Basic v1.0 • The following functions are not supported: – Bridge device (I3C v1.0 and I3C Basic v1.0) – Asynchronous timing control async mode 2 & 3 (I3C v1.0) • Support for DMAC and event linking
I2C Bus Interface (RIIC)	• 9 channels • Master or Slave mode selectable • Support for the multi-master • Support for Standard mode (100 kHz), Fast mode (400 kHz), and Fast mode+ (1 MHz) • Support for DMAC and event linking
Renesas Serial Communication Interface (RSCI)	• 10 channels • 6 communication mode – Asynchronous interfaces – 8-bit clock synchronous interface – Simple IIC (master-only) – Simple SPI – Smart card interface – Simple LIN (expanded SCIX mode) • 32-stage FIFO registers for transmission and reception • Clock sources is select from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and Half-duplex communication • Data length: 7 to 9 bits • Bit rate modulation • Double speed mode • Loopback function to enable self-diagnosis • Support for DMAC and event linking • Support for CRC calculation by the CRC unit
Renesas Serial Peripheral Interface (RSPI)	• 3 channels • SPI transfer facility – Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (SPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) – Capable of handling serial transfer as a master or slave • Data formats – Switching between MSB first and LSB first – The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. – 32 bits × 16 stage buffers for transmission and reception – Up to for frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure – 16 stages/channels for MOSI and MISO independently – Double buffers for both transmission and reception • RSPCK can be stopped automatically with the reception buffer full for master reception • Support for DMAC and event linking • Support CRC calculation by the CRC unit

Item	Description
CRC calculator (CRC)	• 1 channel • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: – $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) – $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C) – $X^{16} + X^{15} + X^2 + 1$ (CRC-16) – $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) – $X^8 + X^2 + X + 1$ (CRC-8) • Support for RSCI and RSPI interfaces
Serial Communication Interface with FIFO (SCIF)	• 1 channel • Asynchronous mode • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud-rate generator • Separate 16-byte FIFO registers for transmission and reception

1.1.13 Timer

Item	Description
General PWM Timer (GPT)	• 32 bits × 16 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Enabling synchronized operation of the several counters between 2 units • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Automatic generation of three-phase PWM waveforms incorporating dead times through the combination of three counters • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter functions for signals on the input capture and external trigger pins • Event linking by the ELC • Support for phase counting mode
Port Output Enable for GPT (POEG)	• Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPT • Initiation by detection of oscillation stop or by software
Compare match timer W (CMTW)	• 32 bits × 8 channels • Compare-match, input-capture input, and output-comparison output are available (ch. 0 to ch. 3) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events
Watchdog Timer (WDT)	• 4 channels • A counter underflow can reset the LSI
General Timer (GTM)	• 32 bits × 8 channels • Two operating modes: – Interval timer mode – Free-running comparison mode
Real Time Clock (RTC)	• A 100-year calendar from 2000 to 2099 • BCD code display • Clock source is an oscillator dedicated to RTC (32.768 kHz) • Automatic adjustment function for leap years • Alarm function

1.1.14 Audio Interface

Item	Description
Sampling Rate Converter Unit (SCU)	• 10 channels • Sampling Rate : Max.192 kHz • Asynchronous sampling rate conversion is available • Supports resolutions up to 24 bits • High-sound-quality type (THD + N*1 is −132 dB) and general-sound-quality type (THD + N*1 is −96 dB) • Automatically generates antialiasing filter coefficients • Four modules support one, two, four, six, or eight channels, and six modules support one or two channels. *Note 1.* Total harmonic distortion plus noise.
Audio Clock Generator Unit (ADG)	• Supplies clock signals to the SSIU, SCU and SPDIF module
Direct Access Memory Controller for Audio (ADMAC)	• Allows transfer of L/R data via I2S • 29 channels • Controls data transfer between the audio modules (SSIU, SCU)
Serial Sound Interface Unit (SSIU)	• 10 channels for half-duplex communication with transmit or receive function • 5 channels for full-duplex communication (full-duplex pairing: ch. 0 & 9, ch.1 & 2, ch. 3 & 4, ch. 5 & 6, ch. 7 & 8) • Support for I2S, monaural, and TDM audio formats • Support for master and slave functions • Generation of programmable word clocks and bit clocks • Multi-channel formats • Support for 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support for WS (word select) signal continuation with which the WS signal is not stopped • Support for ADMAC
SPDIF Interface (SPDIF)	• 3 channels • Support of IEC60958 standard (stereo and consumer use modes only) • Sampling Rate: 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Biphase mark encoding • Double buffered data • Parity encoded serial data • Supports DMAC
Pulse Density Modulation (PDM)	• 6 channels • Direction: input • Sampling Rate: 8, 10, 12, 15, 16, 20, 24, 25, 30, 40, or 48 kHz • Capable of filtering 1-bit digital input data and converting them into 20-bit or 16-bit digital data • supports stereo microphone (L/R sampling by rising/falling clock edge) • supports sound activity detector to wake up CPU from WFI • Supports DMAC

1.1.15 Analog

Item	Description
A/D Converter (ADC)	• 8 channels • Resolution: 12 bits • Input range: 0 V to 1.8 V • Conversion rate: 2.5 Msps, 2.0 Msps, 1.0 Msps, 0.5 Msps, 0.25 Msps • Operation mode: Single scan, continuous scan, group scan • Condition for starting A/D conversion – Software trigger – Asynchronous trigger: External ADTRG trigger supported – Synchronous trigger: ELC and GPT timers • Interrupt sources: A/D scan end, window compare match, compare match/mismatch, data register overwrite
Temperature Sensor Unit (TSU)	• 1 unit for internal temperature • Includes a 12-bit A/D convertor per unit • Resolution: 0.0625°C/code • Rang: -40°C to125°C • Precision: ±5°C • Conversion Rate: 14.9 ksps • Operation Mode: Single Scan • Condition for measurement start – Software trigger – Synchronous trigger: ELC • Interrupt sources: conversion end, window compare match

1.1.16 Security

Item	Description
Secure IP (RSIP)	• Security algorism – Common key encryption: AES – Non-common key encryption: RSA, ECC • Other features – TRNG (true-random number generator) – Hash value generation: SHA-1, SHA-2, SHA-3 – Support of Unique ID

1.1.17 Others

Item	Description
Boundary Scan	Boundary scan based on IEEE 1149.1 via JTAG interface is supported. Note that some module pins are not available on this boundary scan.

1.1.18 Power Supply Voltage

Item	Description
Power supply voltage	• VDD (core): 0.8 V • VDD (CA55): 0.8 V@Normal Drive, 0.9 V@OverDrive • VDD (DDR IO): 1.1 V/0.6 V (LPDDR4/4X) • VDD (except DDR IO): 1.2 V, 1.8 V, 3.3 V

1.1.19 Temperature Range

Item	Description
Temperature range	• Tj: −40°C to +125°C

1.1.20 Quality Level

Item	Description
Quality level	• Industrial usage, etc.

1.1.21 Package

Item	Description
Package	• 625 pin FCBGA / 21 mm square / 0.8 mm pitch • 529 pin FCBGA / 15 mm square / 0.5 mm pitch

1.2 Block Diagram

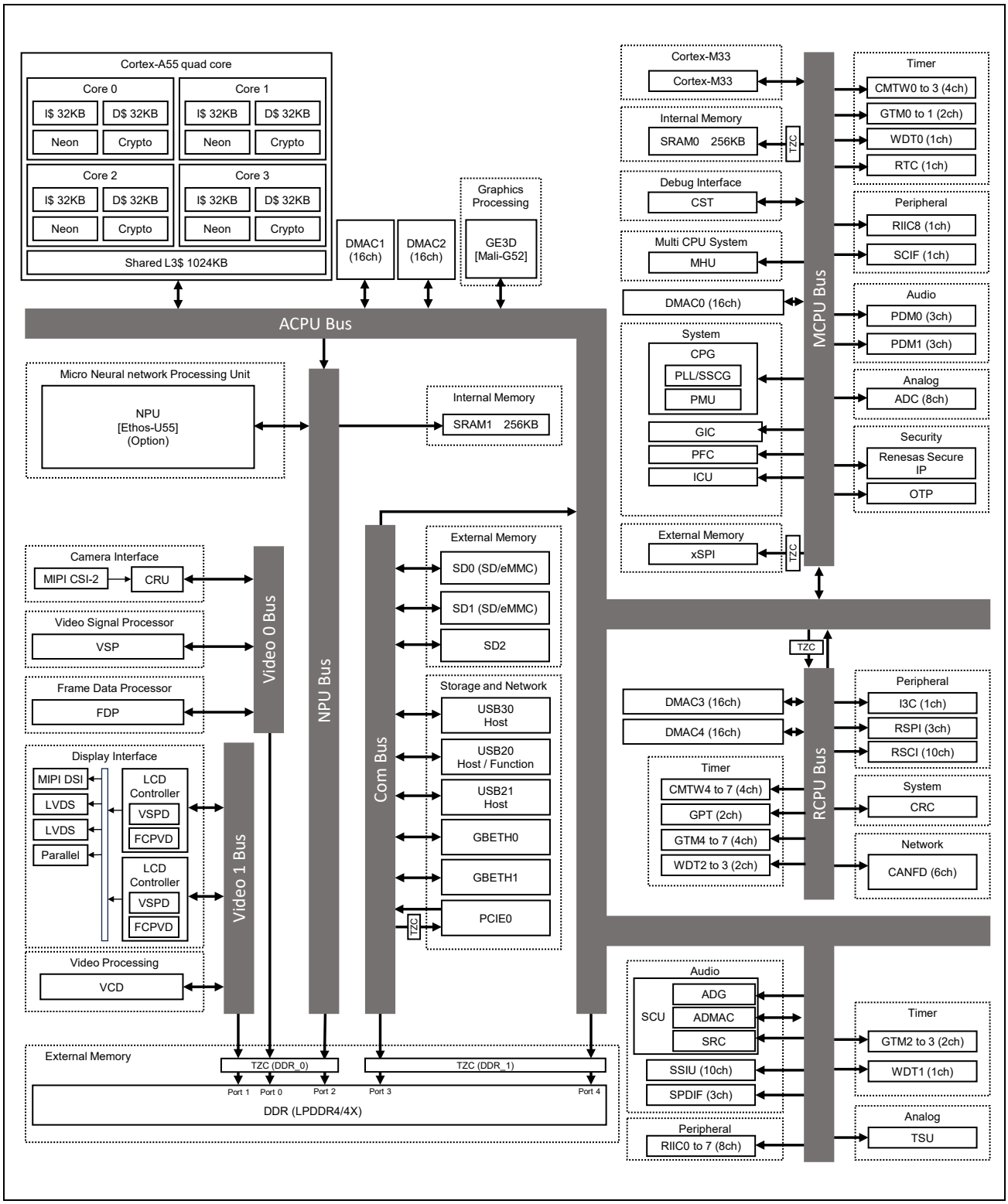


Figure 1.1 Block Diagram

Table 1.1 List of Units (1/2)

Unit Name	Unit Number	Function
ADC	ADC0	A/D converter
ADG	—	Audio clock generator
ADMAC	—	DMAC for audio
CA55	—	Arm Cortex-A55
CANFD	CANFD0	CAN-FD interface
CM33	—	Arm Cortex-M33
CMTW	CMTW0 to CMTW7	Compare match timer
CPG	—	Clock pulse generator
CRC	—	CRC operation unit
CRU	CRU0	Camera data receive unit (MIPI CSI-2 interface)
CST	—	Debug interface (Arm CoreSight)
DDR	DDR0	LPDDR4/4X controller
DMAC	DMAC0 to DMAC4 (each 16 ch.)	Direct memory access (DMA) controller
NPU	—	Micro Neural network processing unit
ELC	—	Event link controller
FDP	—	Frame Data Processor
GBETH	GBETH0, GBETH1	Gigabit Ethernet interface
GE3D	—	3D graphics engine
GIC	—	Generic interrupt controller
GPT	GPT0, GPT1 (each 16 ch.)	General purpose timer
GTM	GTM0 to GTM7	General timer
I3C	I3C0	I3C bus interface
ICU	—	Interrupt control unit
LCDC	—	LCD controller
MHU	—	Message handling unit
OTP	—	One time programmable memory
PCIE	PCIE0	PCIe Express 3.0 interface
PCU	—	Power control unit
PDM	PDM0, PDM1	Pulse density modulation (PDM) interface
PFC	—	Pin function controller
POEG	POEG0, POEG1	Port output enable for GPT
PMU	—	Power management unit
PWC	—	Power sequence controller
RIIC	RIIC0 to RIIC8	I2C bus interface
RSCI	RSCI0 to RSCI9	Serial communication interface
RSPI	RSPI0 to RSPI2	Serial peripheral interface
RTC	—	Real time clock
SCIF	SCIF0	Serial communication interface with FIFO
SD	SD0 to SD2	SD/MMC host interface
Secure IP	—	Trusted secure IP

Table 1.1 List of Units (2/2)

Unit Name	Unit Number	Functional Overview
SRAM	SRAM0 to SRAM11	SRAM
SRC	—	Sampling rate controller
SSIU	—	Serial sound interface unit
SYC	—	System counter
SYS	—	System controller
SYSTEM BUS	—	Internal bus
ACPU Bus	—	A bus connected to Cortex-A55, DDR memory controllers, SRAM, and its peripheral units
RCPU Bus	—	A bus connected to peripheral units
MCPU Bus	—	A bus connected to Cortex-M33, SRAM, its peripheral units, and the system control units
NPU Bus	—	A bus connected to NPU, SRAM, and DDR memory controllers
Video 0 Bus Video 1 Bus	—	A bus connected to image processing units and DDR memory controllers
Com Bus	—	A bus connected to communication interface units and DDR memory controllers
TSU	TSU1	Temperature sensor unit
TZC	—	CoreLink™ TrustZone Address Space Controller
USB2	USB20, USB21	USB2.0 host / function interface
USB3	USB30	USB3.2 host interface
VCD	—	H.265/H.264 multi codec
VSP	—	Video Signal Processor
WDT	WDT0 to WDT3	Watchdog timer
xSPI	xSPI0	xSPI controller

1.3 Product Lineup

Figure 1.2 shows the product part number information. **Table 1.2** shows a list of products.

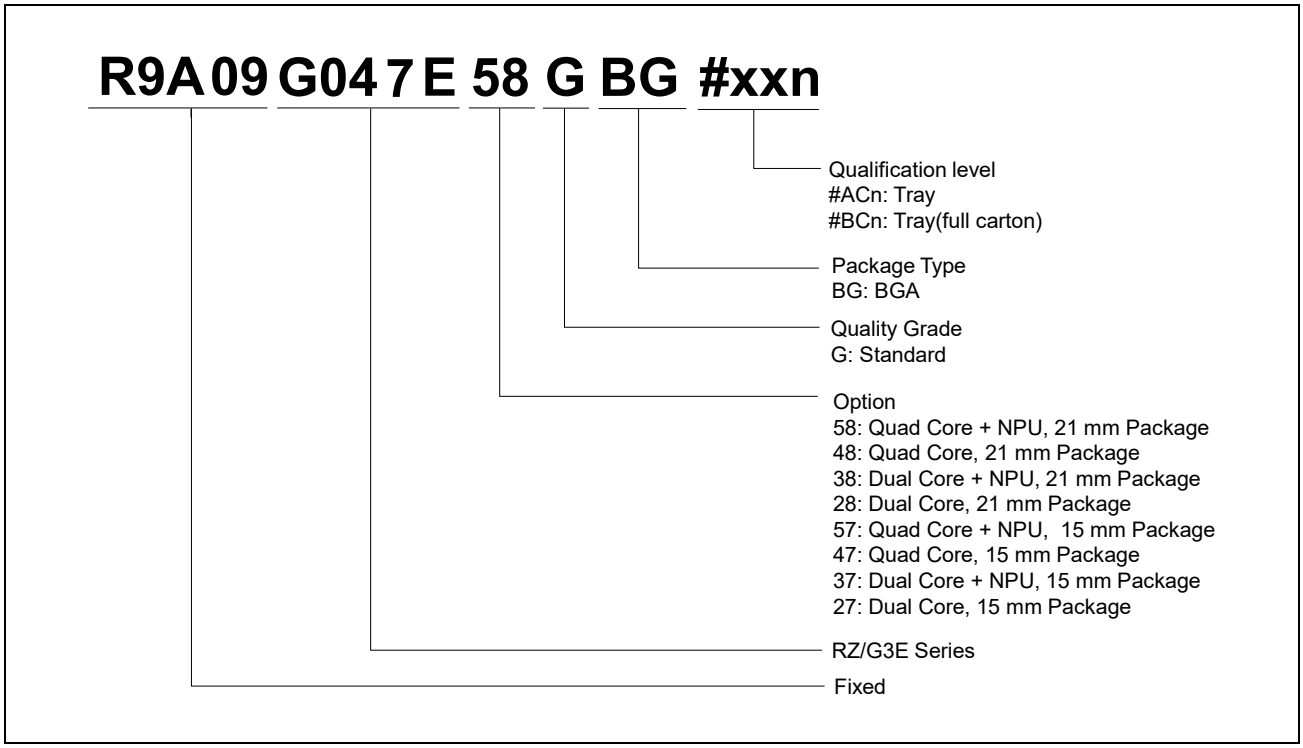


Figure 1.2 Part Numbering Scheme

Table 1.2 Product Lineup

Group	Package	Part Number	NPU	CPU
RZ/G3E	21 mm FCBGA	R9A09G047E58GBG	Ethos-U55	4x Cortex-A55, 1x Cortex-M33
		R9A09G047E48GBG	—	
		R9A09G047E38GBG	Ethos-U55	2x Cortex-A55, 1x Cortex-M33
		R9A09G047E28GBG	—	
	15 mm FCBGA	R9A09G047E57GBG	Ethos-U55	4x Cortex-A55, 1x Cortex-M33
		R9A09G047E47GBG	—	
		R9A09G047E37GBG	Ethos-U55	2x Cortex-A55, 1x Cortex-M33
		R9A09G047E27GBG	—	

Note: The products with #AC0 or #BC0 in the part number have the following restrictions.
— Not supported controlling MIPI LCDs with the Display Command Set over MIPI-DSI.
— Not supported the applications of the Ethos-U55 utilizing the LPDDR4/LPDDR4X.

2. Pin

This section describes the pins of this LSI.

2.1 Pin Assignment

Refer to another excel file for the “ball view” about pin assignment of this LSI.
(Please double-click the icon on the right side)

2.2 External Pins and Multiplexed Functional Pins

Refer to attached excel file for the “pin function list” about information of external pins and multiplexed functional pins of this LSI.
(Please double-click the icon on the right side)

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 3.1 Absolute Maximum Ratings (1/2)

Unit Name	Item	Symbol	Min.	Max.	Unit
CA55	VDD09_CA55	CA55_V_{DD09}	−0.4	1.2	V
PD_OTHERS	VDD08_OTHERS	OTHERS_V_{DD08}	−0.4	1.2	V
	VDD1833_OTHERS	OTHERS_V_{DD33}	−0.4	3.8	V
	VDD1833_PRE18_OTHERS_1	OTHERS1_PRE18V_{DD1833}	−0.4	2.5	V
PD_AWO	VDD08_AWO	AWO_V_{DD08}	−0.4	1.2	V
	VDD18_AWO	AWO_V_{DD18}	−0.4	2.5	V
	VDD1833_AWO	AWO_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_AWO	AWO_PRE18V_{DD1833}	−0.4	2.5	V
USB3 Ch0	USB30_USVPH	USB30_USV_{PH}	−0.4	2.5	V
	USB30_USVPTX	USB30_USV_{PTX}	−0.4	1.2	V
	USB30_USVDD18	USB30_USV_{DD18}	−0.4	2.5	V
USB2 Ch0	USB20_USVDD18	USB20_USV_{DD18}	−0.4	2.5	V
USB2 Ch1	USB21_USVDD18	USB21_USV_{DD18}	−0.4	2.5	V
USB3 Ch0 (for USB2), USB2 Ch0, USB2 Ch1 common	USB2_USVDD33	USB2_USV_{DD33}	−0.4	3.8	V
	USB2_USDVDD	USB2_$USDV_{DD}$	−0.4	1.2	V
xSPI	VDD1833_XSPI	XSPI_V_{DD1833}	−0.4	3.8	V
SD/MMC Ch0	VDD1833_SD0	SD0_V_{DD1833}	−0.4	3.8	V
SD/MMC Ch1	VDD1833_SD1	SD1_V_{DD1833}	−0.4	3.8	V
SD Ch2	VDD1833_SD2	SD2_V_{DD1833}	−0.4	3.8	V
GBETH Ch0	VDD1833_ET0	ET0_V_{DD1833}	−0.4	3.8	V
GBETH Ch1	VDD1833_ET1	ET1_V_{DD1833}	−0.4	3.8	V
SD/MMC Ch0, SD/MMC Ch1, SD Ch2, GBETH Ch0, GBETH Ch1 common	VDD1833_PRE18_OTHERS_2	OTHERS2_PRE18V_{DD1833}	−0.4	2.5	V
OTP	OTPVDD18	OTP_V_{DD18}	−0.4	2.5	V
LPDDR4/LPDDR4X Ch0	DDR0_VDDQ	DDR0_V_{DDQ}	−0.4	1.5	V
	DDR0_VDDQLP	DDR0_V_{DDQLP}	−0.4	1.5	V
	DDR0_VAA	DDR0_V_{AA}	−0.4	2.5	V

Table 3.1 Absolute Maximum Ratings (2/2)

Unit Name	Item	Symbol	Min.	Max.	Unit
MIPI CSI Ch0	CSI0_MSVDD18	CSI0_MSV_{DD18}	−0.4	2.5	V
	CSI0_MSVDD0P8	CSI0_MSV_{DD0P8}	−0.4	1.2	V
MIPI DSI	DSI_VDD0P8	DSI_V_{DD0P8}	−0.4	1.2	V
	DSI_VDD12	DSI_V_{DD12}	−0.4	2.5	V
	DSI_VDD18	DSI_V_{DD18}	−0.4	2.5	V
PCIE	PCIE_VCC18ACMN	PCIE_$V_{CC18ACMN}$	−0.4	2.5	V
	PCIE_VCC18AL01	PCIE_$V_{CC18AL01}$	−0.4	2.5	V
	PCIE_VCC08AL01	PCIE_$V_{CC08AL01}$	−0.4	1.2	V
I3C	VDD1218_I3C	I3C_V_{DD1218}	−0.4	2.5	V
ADC	ADAVDD18	$ADAV_{DD18}$	−0.4	2.5	V
LVDS Ch0, LVDS Ch1 common	LVDS_VCCQ	$LVDSV_{DD18}$	−0.4	2.5	V
CPG	PLVDD_PLLCM33	PLLCM33_PLV_{DD}	−0.4	2.5	V
	PLVDD_PLLCA55	PLLCA55_PLV_{DD}	−0.4	2.5	V
	PLVDD_OTHERS	PLLOTHERS_PLV_{DD}	−0.4	2.5	V
	PLDVDD08_PLLCM33	PLLCM33_$PLDV_{DD08}$	−0.4	1.2	V
	PLDVDD09_PLLCA55	PLLCA55_$PLDV_{DD09}$	−0.4	1.2	V
	PLDVDD08_OTHERS	PLLOTHERS_$PLDV_{DD08}$	−0.4	1.2	V
PWC	VDD18_PWC	PWC_V_{DD18}	−0.4	2.5	V
—	Input voltage (0.6-V I/O)	V_{in06}	−0.4	DDR0_V_{DDQLP} + 0.3*1	V
—	Input voltage (1.1-V I/O)	V_{in11}	−0.4	DDR0_V_{DDQ} + 0.3*1	V
—	Input voltage (1.2-V I/O)	V_{in12}	−0.4	V_{12} + 0.3*2	V
—	Input voltage (1.8-V I/O)	V_{in18}	−0.4	V_{18} + 0.3*3	V
—	Input voltage (1.8-V I/O (3.3-V tolerant))*4	V_{in18_tol}	−0.4	3.6	V
—	Input voltage (3.3-V I/O)	V_{in33}	−0.4	V_{33} + 0.3*5	V
—	Analog input voltage (ADC I/O)	V_{ain18}	0	$ADAV_{DD18}$	V
—	Junction temperature	T_j	−40	125	°C
—	Storage temperature	T_{stg}	−40	150	°C

Note 1. The voltage to be applied must be within the absolute maximum rating (1.5 V).

Note 2. The voltage to be applied must be within the absolute maximum rating (2.5 V). V_{12} indicates the power supply voltage for 1.2-V I/O pins.

Note 3. The voltage to be applied must be within the absolute maximum rating (2.5 V). V_{18} indicates the power supply voltage for 1.8-V I/O pins. When 1.8-V is used for the 3.3/1.8-V switching I/O, this specification is applied.

Note 4. PS0 to PS3, PJ0 to PJ4

Note 5. The voltage to be applied must be within the absolute maximum rating (3.8 V). V_{33} indicates the power supply voltage for 3.3-V I/O pins. When 3.3-V is used for the 3.3/1.8-V switching I/O, this specification is applied.

3.2 Recommended Operating Range

Table 3.2 Recommended Operating Range (1/2)

Unit Name	Item	Symbol	Min.	Typ.	Max.	Unit	Note
CA55	VDD09_CA55	CA55_V_{DD09}	0.86	0.9	0.94	V	0.9 V: OD*1
			0.76	0.8	0.84	V	0.8 V: ND*1
PD_OTHERS	VDD08_OTHERS	OTHERS_V_{DD08}	0.76	0.8	0.84	V	*2
	VDD1833_OTHERS	OTHERS_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_OTHERS_1	OTHERS1_PRE18V_{DD1833}	1.71	1.8	1.89	V	
PD_AWO	VDD08_AWO	AWO_V_{DD08}	0.76	0.8	0.84	V	
	VDD18_AWO	AWO_V_{DD18}	1.71	1.8	1.89	V	
	VDD1833_AWO	AWO_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_AWO	AWO_PRE18V_{DD1833}	1.71	1.8	1.89	V	
USB3 Ch0	USB30_USVPH	USB30_USV_{PH}	1.71	1.8	1.89	V	
	USB30_USVPTX	USB30_USV_{PTX}	0.76	0.8	0.84	V	
	USB30_USVDD18	USB30_USV_{DD18}	1.71	1.8	1.89	V	
USB2 Ch0	USB20_USVDD18	USB20_USV_{DD18}	1.71	1.8	1.89	V	
USB2 Ch1	USB21_USVDD18	USB21_USV_{DD18}	1.71	1.8	1.89	V	
USB3 Ch0 (for USB2), USB2 Ch0, USB2 Ch1 common	USB2_USVDD33	USB2_USV_{DD33}	3.14	3.3	3.46	V	
	USB2_USDVDD	USB2_$USDV_{DD}$	0.76	0.8	0.84	V	
xSPI	VDD1833_XSPI	XSPI_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
SD/MMC Ch0	VDD1833_SD0	SD0_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
SD/MMC Ch1	VDD1833_SD1	SD1_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
SD Ch2	VDD1833_SD2	SD2_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
GBETH Ch0	VDD1833_ET0	ET0_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
GBETH Ch1	VDD1833_ET1	ET1_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
SD/MMC Ch0, SD/MMC Ch1, SD Ch2, GBETH Ch0, GBETH Ch1 common	VDD1833_PRE18_OTHERS_2	OTHERS2_PRE18V_{DD1833}	1.71	1.8	1.89	V	
OTP	OTPVDD18	OTP_V_{DD18}	1.71	1.8	1.89	V	
LPDDR4/LPDDR4X Ch0	DDR0_VDDQ	DDR0_V_{DDQ}	1.06	1.1	1.17	V	
	DDR0_VDDQLP	DDR0_V_{DDQLP}	0.57	0.6	0.65	V	0.6 V: LPDDR4X
			1.06	1.1	1.17	V	1.1 V: LPDDR4
	DDR0_VAA	DDR0_V_{AA}	1.71	1.8	1.89	V	

Table 3.2 Recommended Operating Range (2/2)

Unit Name	Item	Symbol	Min.	Typ.	Max.	Unit	Note
MIPI CSI Ch0	CSI0_MSVDD18	$CSI0\_MSV_{DD18}$	1.71	1.8	1.89	V	
	CSI0_MSVDD0P8	$CSI0\_MSV_{DD0P8}$	0.76	0.8	0.84	V	
MIPI DSI	DSI_VDD0P8	DSI_V_{DD0P8}	0.76	0.8	0.84	V	
	DSI_VDD12	DSI_V_{DD12}	1.14	1.2	1.26	V	
	DSI_VDD18	DSI_V_{DD18}	1.71	1.8	1.89	V	
PCIE	PCIE_VCC18ACMN	$PCIE\_V_{CC18ACMN}$	1.71	1.8	1.89	V	
	PCIE_VCC18AL01	$PCIE\_V_{CC18AL01}$	1.71	1.8	1.89	V	
	PCIE_VCC08AL01	$PCIE\_V_{CC08AL01}$	0.76	0.8	0.84	V	
I3C	VDD1218_I3C	$I3C\_V_{DD1218}$	1.71	1.8	1.89	V	
			1.14	1.2	1.26	V	
ADC	ADAVDD18	$ADAV_{DD18}$	1.71	1.8	1.89	V	
LVDS Ch0, LVDS Ch1 common	LVDS_VCCQ	$LVDSV_{DD18}$	1.71	1.8	1.89	V	
CPG	PLVDD_PLLCM33	$PLLCM33\_PLV_{DD}$	1.71	1.8	1.89	V	
	PLVDD_PLLCA55	$PLLCA55\_PLV_{DD}$	1.71	1.8	1.89	V	
	PLVDD_OTHERS	$PLLOTHERS\_PLV_{DD}$	1.71	1.8	1.89	V	
	PLDVDD08_PLLCM33	$PLLCM33\_PLDV_{DD08}$	0.76	0.8	0.84	V	
	PLDVDD09_PLLCA55	$PLLCA55\_PLDV_{DD09}$	0.86	0.9	0.94	V	0.9 V: OD*1
			0.76	0.8	0.84	V	0.8 V: ND*1
	PLDVDD08_OTHERS	$PLLOTHERS\_PLDV_{DD08}$	0.76	0.8	0.84	V	
PWC	VDD18_PWC	PWC_V_{DD18}	1.71	1.8	1.89	V	

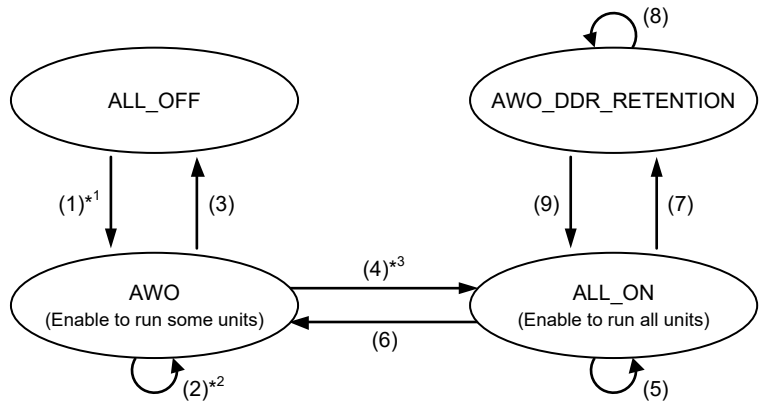
Note 1. OD: Over drive (up to 1.8-GHz operation frequency)
ND: Normal drive (up to 1.1-GHz operation frequency)

Note 2. To avoid the possibility of noise, separating this power supply from other power supply terminals is recommended.

3.3 Power-On/Off Sequence

3.3.1 CM33 Boot Mode (State Diagram)

The state diagram of CM33 cold boot is shown in **Figure 3.1**. The boot mode states (1) to (9) refer to the sequence of (1) to (9) in **Figure 3.2** to **Figure 3.5**.



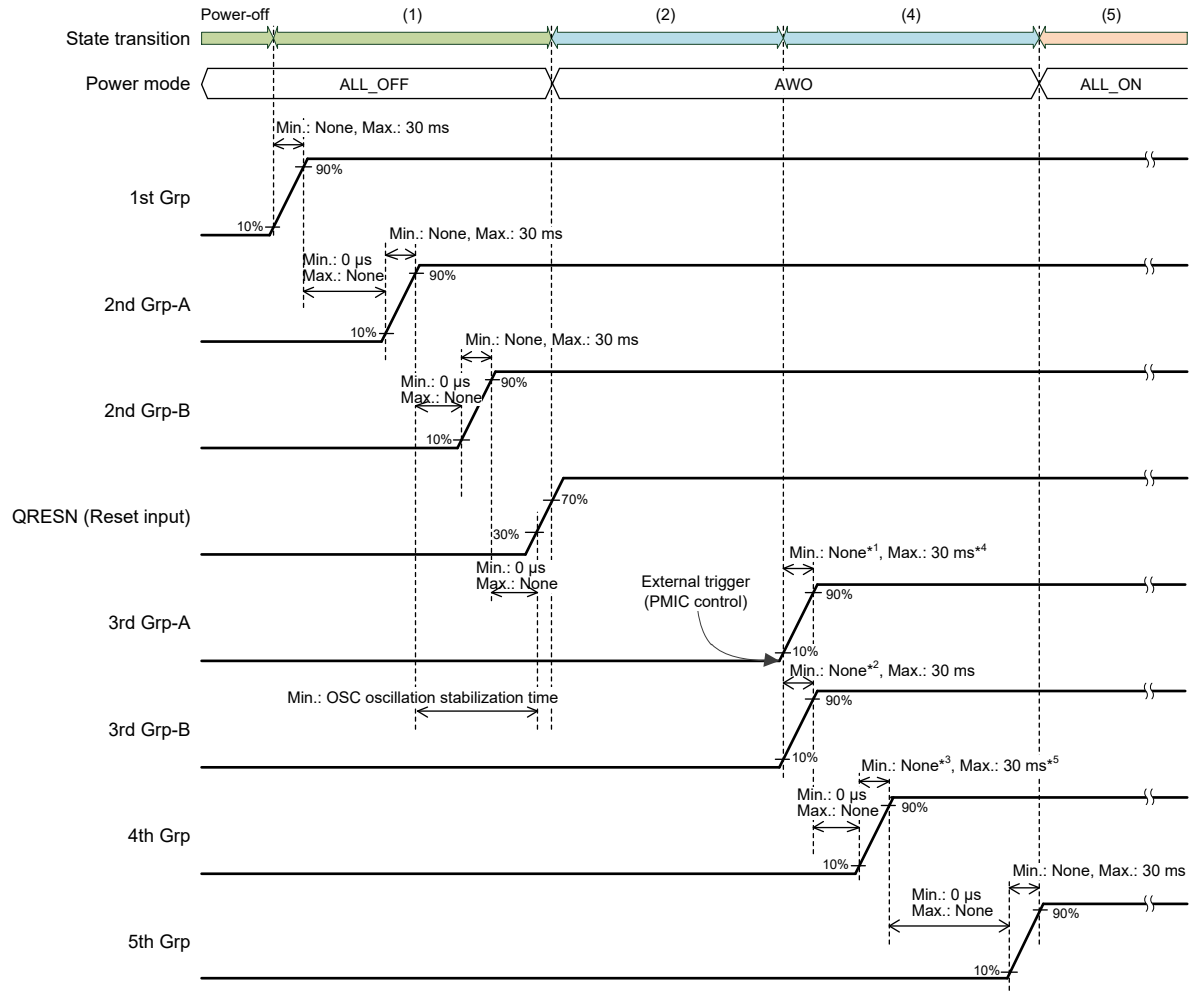
Note 1. CM33 cold boot sequence.

Note 2. CM33 operates the system managements.

Note 3. When the power mode switches from AWO to ALL_ON depending on the user system, CM33 sets the LSI registers and PMIC registers to supply power to the OTHERS domain.

Figure 3.1 CM33 Boot State Diagram

3.3.2 CM33 Boot Mode (Power-On)



1st Grp power supply
0.8 V
VDD08_AWO
PLDVDD08_PLLCM33

2nd Grp-A power supply
1.8 V
ADAVDD18
OTPVDD18
VDD1833_PRE18_AWO
VDD18_AWO
VDD18_PWC
PLVDD_PLLCM33

(When used as 1.8 V)
VDD1833_AWO
VDD1833_XSPI

2nd Grp-B power supply
(When used as 3.3 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-A power supply
0.8 V
USB2_USDVDD
USB30_USVPTX
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
PLDVDD08_OTHERS
VDD08_OTHERS

0.8/0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

3rd Grp-B power supply
1.1 V
DDR0_VDDQ

0.6/1.1 V
DDR0_VDDQLP

4th Grp power supply
1.8 V
VDD1833_PRE18_OTHERS_1
VDD1833_PRE18_OTHERS_2
DSI_VDD18
CSI0_MSVDD18
LVDS_VCCQ
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
DDR0_VAA
PLVDD_PLLCA55
PLVDD_OTHERS
PCIE_VCC18ACMN
PCIE_VCC18AL01

(When used as 1.8 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

1.2/1.8 V
VDD1218_I3C

3.3 V
USB2_USVDD33

5th Grp power supply
1.2 V
DSI_VDD12
(When used as 3.3 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

Note 1. VDD08_OTHERS, USB30_USVPTX, USB2_USDVDD: Min. 10 µs

Note 2. DDR0_VDDQ, DDR0_VDDQLP (1.1 V): Min. 180 µs
DDR0_VDDQLP (0.6 V): Min. 100 µs

Note 3. VDD1833_PRE18_OTHERS_1: Min. 10 µs
DDR0_VAA: Min. 290 µs
USB2_USVDD33: Min.30 µs
USB20_USVDD18, USB21_USVDD18, USB30_USVDD18: Min. 20 µs
USB30_USVPH: Min. 10 µs

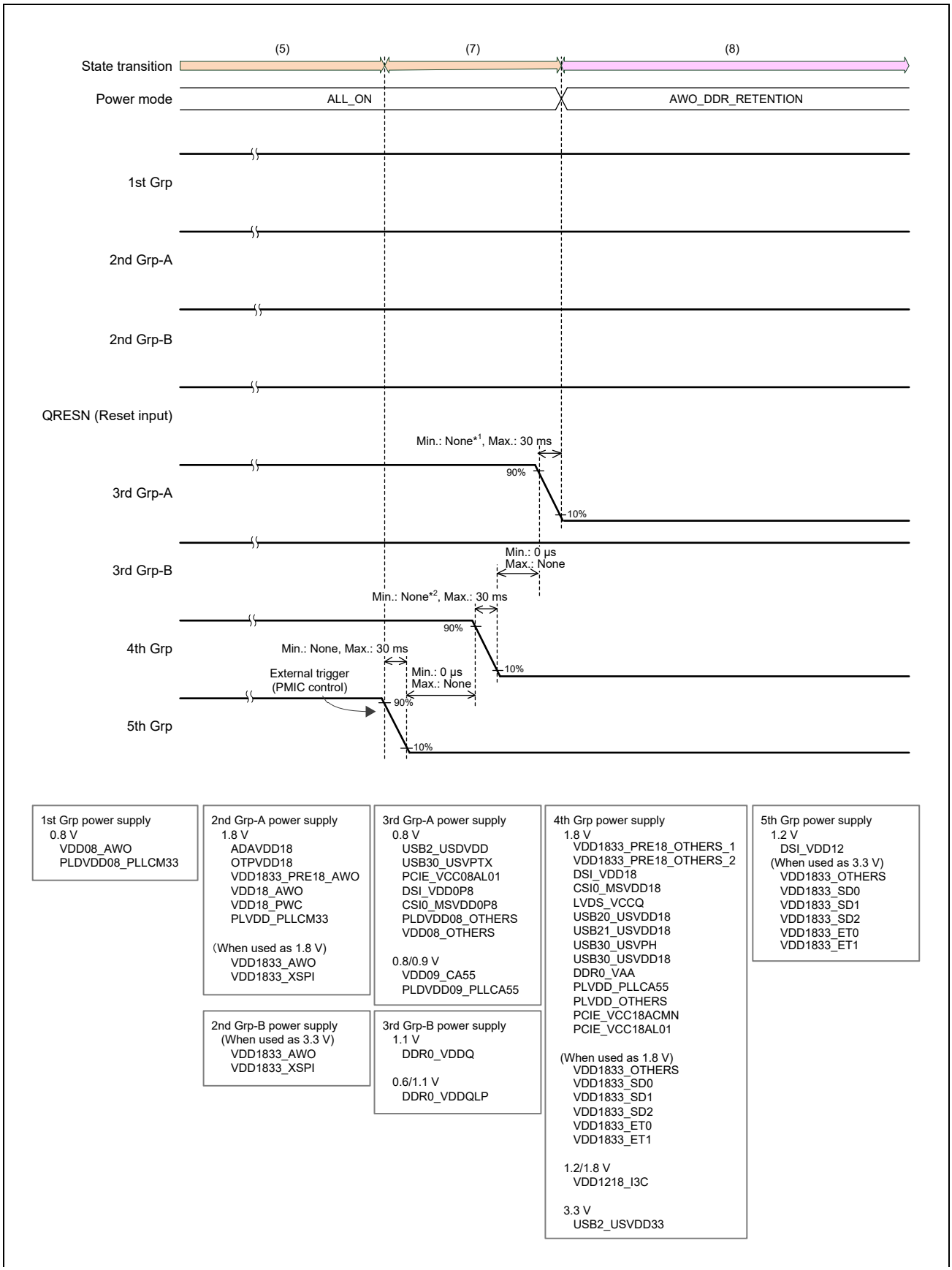
Note 4. USB2_USDVDD: Max. 10 ms

Note 5. USB20_USVDD18, USB21_USVDD18, USB30_USVDD18, USB2_USVDD33: Max. 10 ms

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Figure 3.2 Power-On Sequence (CM33 Boot)

3.3.3 CM33 Boot Mode (DDR Retention Enter)



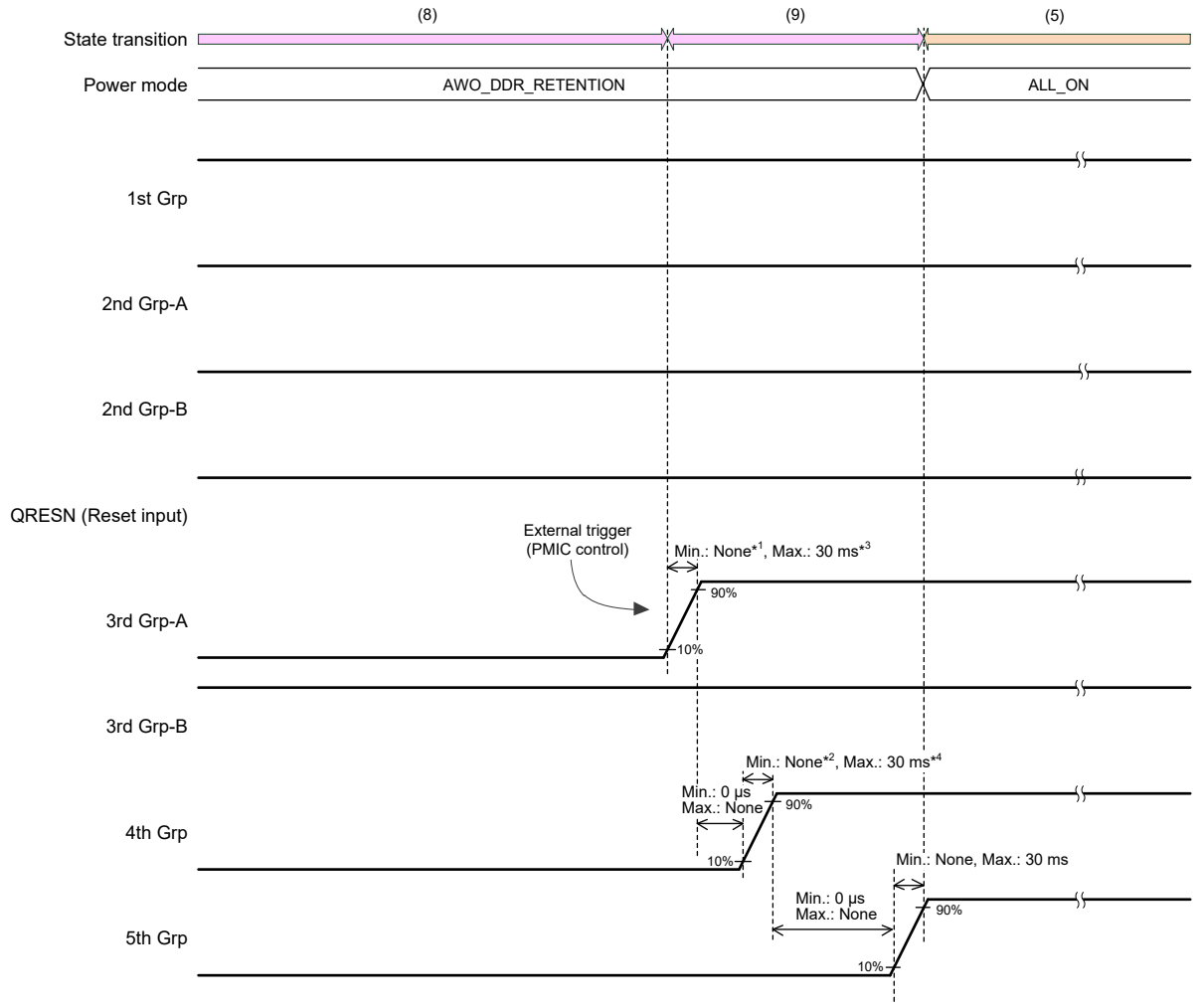
Note 1. VDD08_OTHERS: Min. 10 µs

Note 2. VDD1833_PRE18_OTHERS_1: Min. 10 µs

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Figure 3.3 DDR Retention Enter Sequence (CM33 Boot Mode)

3.3.4 CM33 Boot Mode (DDR Retention Exit)



1st Grp power supply
0.8 V
VDD08_AWO
PLDVDD08_PLLCM33

2nd Grp-A power supply
1.8 V
ADAVDD18
OTPVDD18
VDD1833_PRE18_AWO
VDD18_AWO
VDD18_PWC
PLVDD_PLLCM33

(When used as 1.8 V)
VDD1833_AWO
VDD1833_XSPI

2nd Grp-B power supply
(When used as 3.3 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-A power supply
0.8 V
USB2_USDVDD
USB30_USVPTX
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
PLDVDD08_OTHERS
VDD08_OTHERS

0.8/0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

3rd Grp-B power supply
1.1 V
DDR0_VDDQ

0.6/1.1 V
DDR0_VDDQLP

4th Grp power supply
1.8 V
VDD1833_PRE18_OTHERS_1
VDD1833_PRE18_OTHERS_2
DSI_VDD18
CSI0_MSVDD18
LVDS_VCCQ
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
DDR0_VAA
PLVDD_PLLCA55
PLVDD_OTHERS
PCIE_VCC18ACMN
PCIE_VCC18AL01

(When used as 1.8 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

1.2/1.8 V
VDD1218_I3C

3.3 V
USB2_USVDD33

5th Grp power supply
1.2 V
DSI_VDD12
(When used as 3.3 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

Note 1. VDD08_OTHERS, USB30_USVPTX, USB2_USDVDD: Min. 10 µs

Note 2. VDD1833_PRE18_OTHERS_1: Min. 10 µs
DDR0_VAA: Min. 290 µs
USB2_USVDD33: Min.30 µs
USB20_USVDD18, USB21_USVDD18, USB30_USVDD18: Min. 20 µs
USB30_USVPH: Min. 10 µs

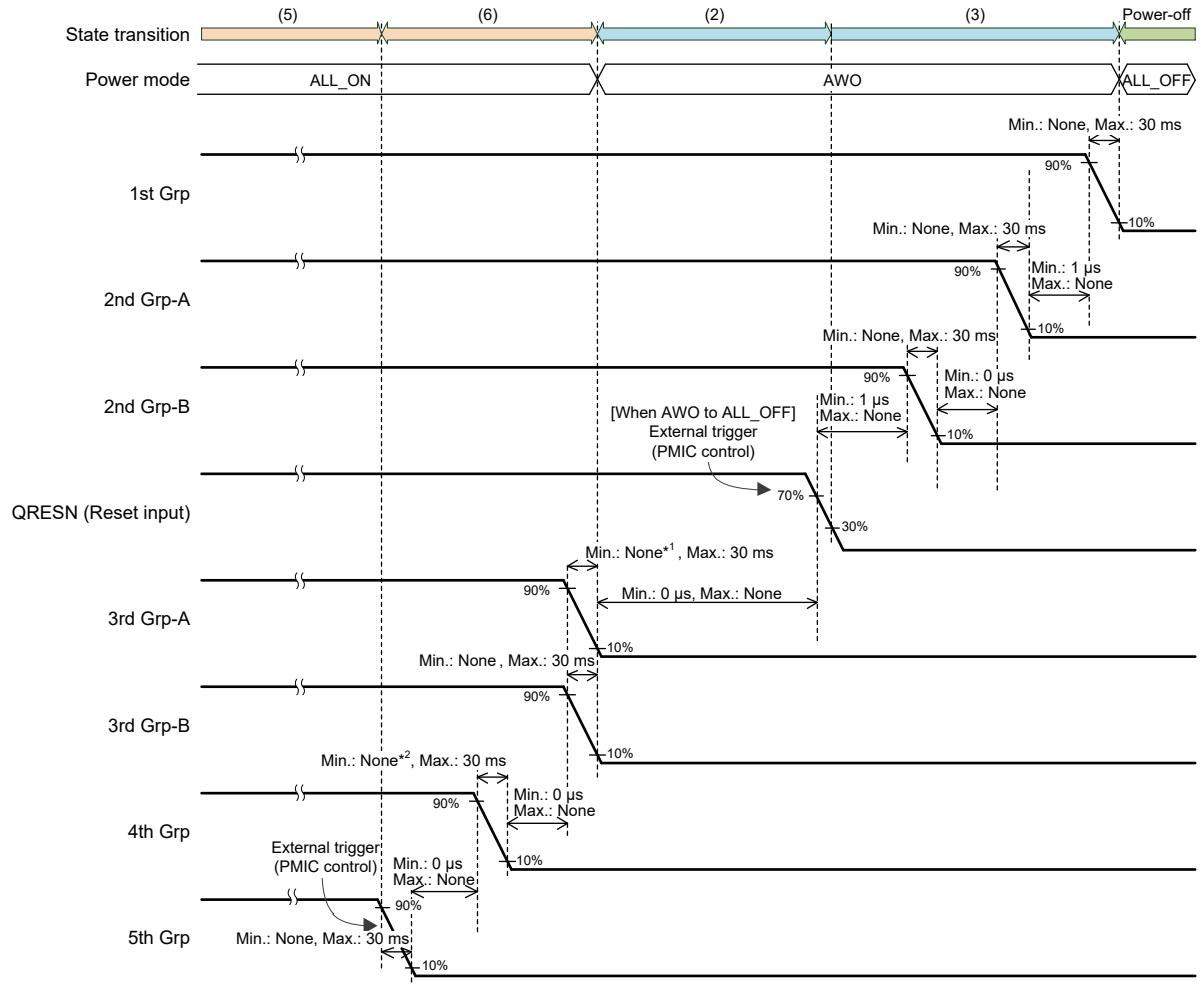
Note 3. USB2_USDVDD: Max. 10 ms

Note 4. USB20_USVDD18, USB21_USVDD18, USB30_USVDD18, USB2_USVDD33: Max. 10 ms

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Figure 3.4 DDR Retention Exit Sequence (CM33 Boot Mode)

3.3.5 CM33 Boot Mode (Power-Off)



1st Grp power supply
0.8 V
VDD08_AWO
PLDVDD08_PLLCM33

2nd Grp-A power supply
1.8 V
ADAVDD18
OTPVDD18
VDD1833_PRE18_AWO
VDD18_AWO
VDD18_PWC
PLVDD_PLLCM33

(When used as 1.8 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-A power supply
0.8 V
USB2_USDVDD
USB30_USVPTX
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
PLDVDD08_OTHERS
VDD08_OTHERS

0.8/0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

4th Grp power supply
1.8 V
VDD1833_PRE18_OTHERS_1
VDD1833_PRE18_OTHERS_2
DSI_VDD18
CSI0_MSVDD18
LVDS_VCCQ
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
DDR0_VAA
PLVDD_PLLCA55
PLVDD_OTHERS
PCIE_VCC18ACMN
PCIE_VCC18AL01

(When used as 1.8 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

1.2/1.8 V
VDD1218_I3C

3.3 V
USB2_USVDD33

5th Grp power supply
1.2 V
DSI_VDD12
(When used as 3.3 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

2nd Grp-B power supply
(When used as 3.3 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-B power supply
1.1 V
DDR0_VDDQ

0.6/1.1 V
DDR0_VDDQLP

Note 1. VDD08_OTHERS: Min. 10 µs

Note 2. VDD1833_PRE18_OTHERS_1: Min. 10 µs

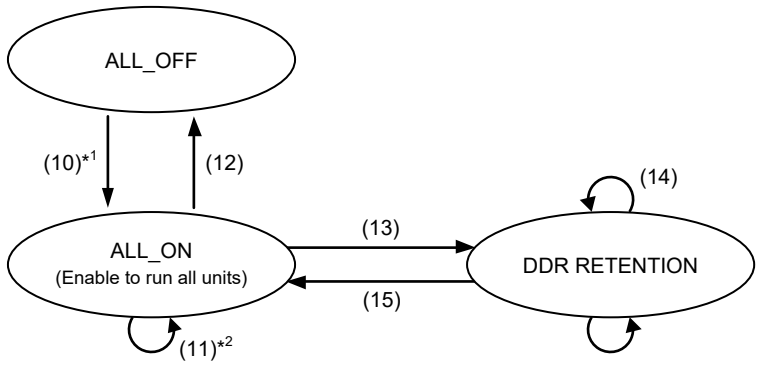
Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Note: The fall time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.5 Power-Off Sequence (CM33 Boot Mode)

3.3.6 CA55 Boot Mode (State Diagram)

The state diagram of CA55 cold boot is shown in **Figure 3.6**. The boot mode states (10) to (15) refer to the sequence of (10) to (15) in **Figure 3.7** to **Figure 3.10**.

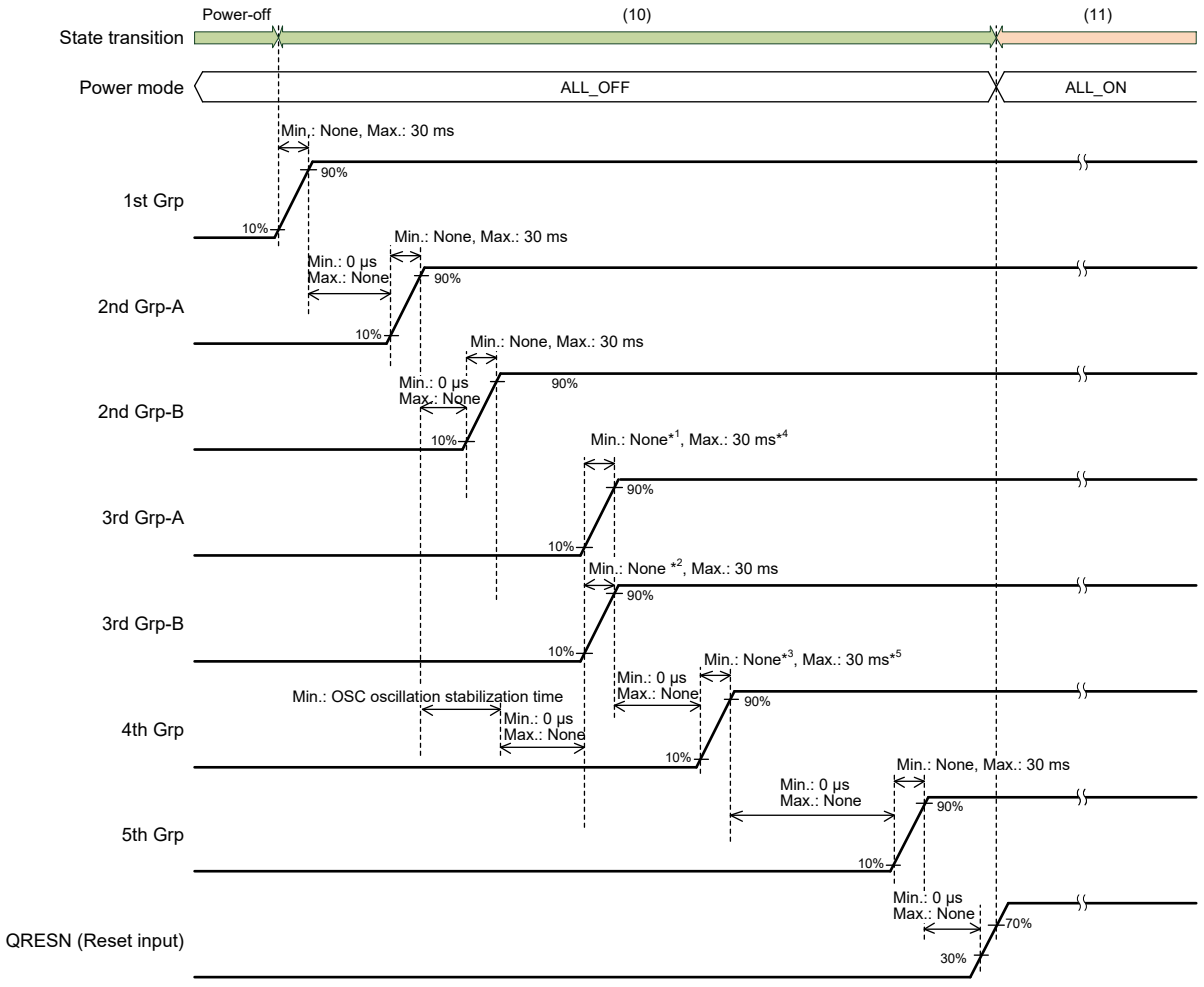


Note 1. CA55 cold boot sequence.

Note 2. CA55 operates the system managements.

Figure 3.6 CA55 Boot State Diagram

3.3.7 CA55 Boot Mode (Power-On)



1st Grp power supply
0.8 V
VDD08_AWO
PLDVDD08_PLLCM33

2nd Grp-A power supply
1.8 V
ADAVDD18
OTPVDD18
VDD1833_PRE18_AWO
VDD18_AWO
VDD18_PWC
PLVDD_PLLCM33

(When used as 1.8 V)
VDD1833_AWO
VDD1833_XSPI

2nd Grp-B power supply
(When used as 3.3 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-A power supply
0.8 V
USB2_USDVDD
USB30_USVPTX
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
PLDVDD08_OTHERS
VDD08_OTHERS

0.8/0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

3rd Grp-B power supply
1.1 V
DDR0_VDDQ

0.6/1.1 V
DDR0_VDDQLP

4th Grp power supply
1.8 V
VDD1833_PRE18_OTHERS_1
VDD1833_PRE18_OTHERS_2
DSI_VDD18
CSI0_MSVDD18
LVDS_VCCQ
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
DDR0_VAA
PLVDD_PLLCA55
PLVDD_OTHERS
PCIE_VCC18ACMN
PCIE_VCC18AL01

(When used as 1.8 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

1.2/1.8 V
VDD1218_I3C

3.3 V
USB2_USVDD33

5th Grp power supply
1.2 V
DSI_VDD12
(When used as 3.3 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

Note 1. VDD08_OTHERS, USB30_USVPTX, USB2_USDVDD: Min. 10 µs

Note 2. DDR0_VDDQ, DDR0_VDDQLP (1.1 V): Min. 180 µs

Note 3. VDD1833_PRE18_OTHERS_1: Min. 10 µs
DDR0_VAA: Min. 290 µs
USB2_USVDD33: Min.30 µs
USB20_USVDD18, USB21_USVDD18, USB30_USVDD18: Min. 20 µs
USB30_USVPH: Min. 10 µs

Note 4. USB2_USDVDD: Max. 10 ms

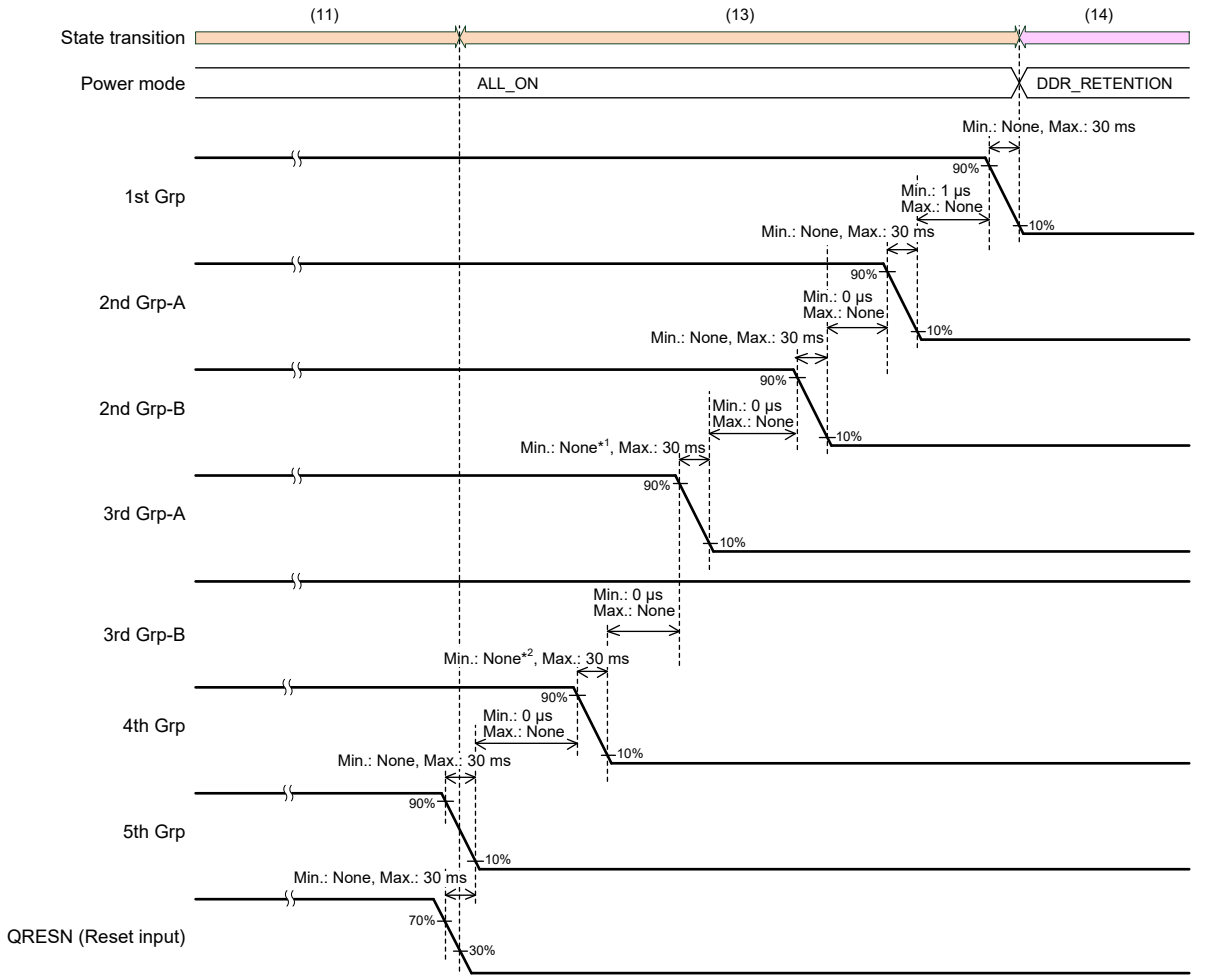
Note 5. USB20_USVDD18, USB21_USVDD18, USB30_USVDD18, USB2_USVDD33: Max. 10 ms

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Note: The rise time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.7 Power-On Sequence (CA55 Boot Mode)

3.3.8 CA55 Boot Mode (DDR Retention Enter)



1st Grp power supply
0.8 V
VDD08_AWO
PLDVDD08_PLLCM33

2nd Grp-A power supply
1.8 V
ADAVDD18
OTPVDD18
VDD1833_PRE18_AWO
VDD18_AWO
VDD18_PWC
PLVDD_PLLCM33

(When used as 1.8 V)
VDD1833_AWO
VDD1833_XSPI

2nd Grp-B power supply
(When used as 3.3 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-A power supply
0.8 V
USB2_USDVDD
USB30_USVPTX
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
PLDVDD08_OTHERS
VDD08_OTHERS

0.8/0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

3rd Grp-B power supply
1.1 V
DDR0_VDDQ

0.6/1.1 V
DDR0_VDDQLP

4th Grp power supply
1.8 V
VDD1833_PRE18_OTHERS_1
VDD1833_PRE18_OTHERS_2
DSI_VDD18
CSI0_MSVDD18
LVDS_VCCQ
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
DDR0_VAA
PLVDD_PLLCA55
PLVDD_OTHERS
PCIE_VCC18ACMN
PCIE_VCC18AL01

(When used as 1.8 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

1.2/1.8 V
VDD1218_I3C

3.3 V
USB2_USVDD33

5th Grp power supply
1.2 V
DSI_VDD12
(When used as 3.3 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

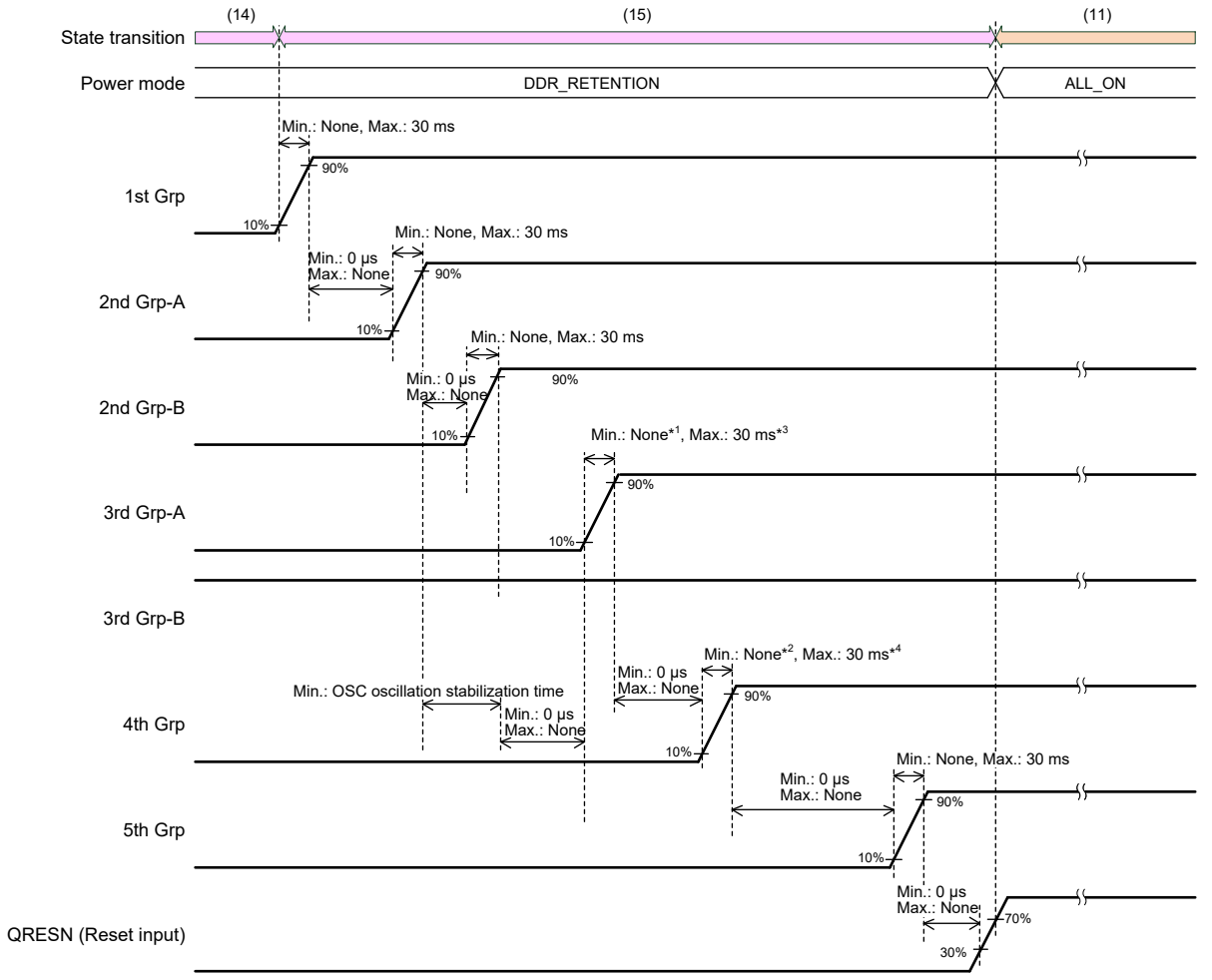
Note 1. VDD08_OTHERS: Min. 10 µs

Note 2. VDD1833_PRE18_OTHERS_1: Min. 10 µs

Note: The fall time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.8 DDR Retention Enter Sequence (CA55 Boot Mode)

3.3.9 CA55 Boot Mode (DDR retention exit)



1st Grp power supply
0.8 V
VDD08_AWO
PLDVDD08_PLLCM33

2nd Grp-A power supply
1.8 V
ADAVDD18
OTPVDD18
VDD1833_PRE18_AWO
VDD18_AWO
VDD18_PWC
PLVDD_PLLCM33

(When used as 1.8 V)
VDD1833_AWO
VDD1833_XSPI

2nd Grp-B power supply
(When used as 3.3 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-A power supply
0.8 V
USB2_USDVDD
USB30_USVPTX
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
PLDVDD08_OTHERS
VDD08_OTHERS

0.8/0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

3rd Grp-B power supply
1.1 V
DDR0_VDDQ

0.6/1.1 V
DDR0_VDDQLP

4th Grp power supply
1.8 V
VDD1833_PRE18_OTHERS_1
VDD1833_PRE18_OTHERS_2
DSI_VDD18
CSI0_MSVDD18
LVDS_VCCQ
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
DDR0_VAA
PLVDD_PLLCA55
PLVDD_OTHERS
PCIE_VCC18ACMN
PCIE_VCC18AL01

(When used as 1.8 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

1.2/1.8 V
VDD1218_I3C

3.3 V
USB2_USVDD33

5th Grp power supply
1.2 V
DSI_VDD12
(When used as 3.3 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

Note 1. VDD08_OTHERS, USB30_USVPTX, USB2_USDVDD: Min. 10 µs

Note 2. VDD1833_PRE18_OTHERS_1: Min. 10 µs
DDR0_VAA: Min. 290 µs
USB2_USVDD33: Min.30 µs
USB20_USVDD18, USB21_USVDD18, USB30_USVDD18: Min. 20 µs
USB30_USVPH: Min. 10 µs

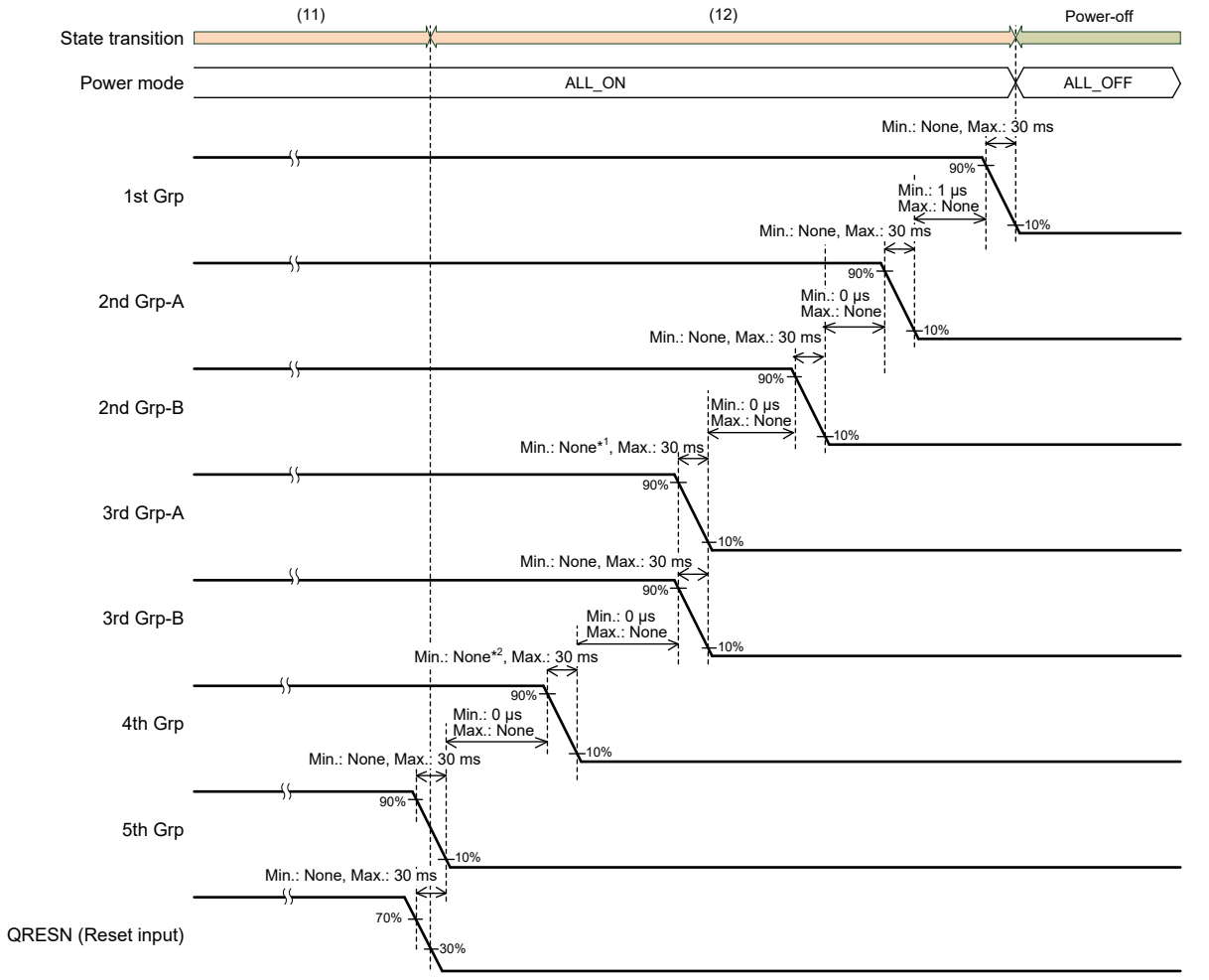
Note 3. USB2_USDVDD: Max. 10 ms

Note 4. USB20_USVDD18, USB21_USVDD18, USB30_USVDD18, USB2_USVDD33: Max. 10 ms

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Figure 3.9 DDR Retention Exit Sequence (CA55 Boot Mode)

3.3.10 CA55 Boot Mode (Power-Off)



1st Grp power supply
0.8 V
VDD08_AWO
PLDVDD08_PLLCM33

2nd Grp-A power supply
1.8 V
ADAVDD18
OTPVDD18
VDD1833_PRE18_AWO
VDD18_AWO
VDD18_PWC
PLVDD_PLLCM33

(When used as 1.8 V)
VDD1833_AWO
VDD1833_XSPI

2nd Grp-B power supply
(When used as 3.3 V)
VDD1833_AWO
VDD1833_XSPI

3rd Grp-A power supply
0.8 V
USB2_USDVDD
USB30_USVPTX
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
PLDVDD08_OTHERS
VDD08_OTHERS

0.8/0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

3rd Grp-B power supply
1.1 V
DDR0_VDDQ

0.6/1.1 V
DDR0_VDDQLP

4th Grp power supply
1.8 V
VDD1833_PRE18_OTHERS_1
VDD1833_PRE18_OTHERS_2
DSI_VDD18
CSI0_MSVDD18
LVDS_VCCQ
USB20_USVDD18
USB21_USVDD18
USB30_USVPH
USB30_USVDD18
DDR0_VAA
PLVDD_PLLCA55
PLVDD_OTHERS
PCIE_VCC18ACMN
PCIE_VCC18AL01

(When used as 1.8 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

1.2/1.8 V
VDD1218_I3C

3.3 V
USB2_USVDD33

5th Grp power supply
1.2 V
DSI_VDD12
(When used as 3.3 V)
VDD1833_OTHERS
VDD1833_SD0
VDD1833_SD1
VDD1833_SD2
VDD1833_ET0
VDD1833_ET1

Note 1. VDD08_OTHERS: Min. 10 µs

Note 2. VDD1833_PRE18_OTHERS_1: Min. 10 µs

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Figure 3.10 Power-Off Sequence (CA55 Boot Mode)

3.4 DC Characteristics

3.4.1 Maximum Supply Current

Conditions for the supply current: Power supply voltage = Max. value, T_j = −40 to 125ºC

Table 3.3 Max. Supply Currents during Operation (1/2)

Unit Name	Item	Symbol	Max.	Unit	Note
CA55	0.8-V (or 0.9-V) power supply current	I_{DD09_CA55}	3014	mA	VDD09_CA55
PD_OTHERS	0.8-V core power supply current	I_{DD08_OTHERS}	3484	mA	VDD08_OTHERS
	I/O power supply current	I_{DD1833_OTHERS}	75	mA	VDD1833_OTHERS
	pre-driver power supply	$I_{DD1833PRE18\_OTHERS1}$	4	mA	VDD1833_PRE18_OTHERS_1
PD_AWO	0.8-V core power supply current	I_{DD08_AWO}	192	mA	VDD08_AWO
	1.8-V core power supply current	I_{DD18_AWO}	4	mA	VDD18_AWO
	I/O power supply current	I_{DD1833_AWO}	13	mA	VDD1833_AWO
	Pre-driver power supply current	$I_{DD1833PRE18\_AWO}$	2	mA	VDD1833_PRE18_AWO
USB3 Ch0	1.8-V PHY power supply current	$I_{DDUSB30\_USVPH}$	33	mA	USB30_USVPH
	0.8-V PHY power supply current	$I_{DDUSB30\_USVPTX}$	59	mA	USB30_USVPTX
	1.8-V PHY power supply current*1	$I_{DDUSB30\_USVDD18}$	20	mA	USB30_USVDD18
USB2 Ch0	1.8-V PHY power supply current	$I_{DDUSB20\_USVDD18}$	20	mA	USB20_USVDD18
USB2 Ch1	1.8-V PHY power supply current	$I_{DDUSB21\_USVDD18}$	20	mA	USB21_USVDD18
USB3 Ch0 (for USB2), USB2 Ch0, USB2 Ch1 common	3.3-V PHY power supply current	$I_{DDUSB2\_USVDD33}$	39	mA	USB2_USVDD33
	0.8-V PHY power supply current	I_{DDUSB2_USDVDD}	30	mA	USB2_USDVDD
xSPI	I/O power supply current	I_{DD1833_XSPI}	25	mA	VDD1833_XSPI
SD/MMC Ch0	I/O power supply current	I_{DD1833_SD0}	17	mA	VDD1833_SD0
SD/MMC Ch1	I/O power supply current	I_{DD1833_SD1}	10	mA	VDD1833_SD1
SD Ch2	I/O power supply current	I_{DD1833_SD2}	10	mA	VDD1833_SD2
SD/MMC Ch0, SD/MMC Ch1, SD Ch2, GBETH Ch0, GBETH Ch1 common	pre-driver power supply	$I_{DD1833PRE18\_OTHERS2}$	7	mA	VDD1833_PRE18_OTHERS_2
OTP	1.8-V power supply current	$I_{DDOTPVDD18}$	6	mA	OTPVDD18
LPDDR4/LPDDR4X Ch0	1.1-V PHY power supply current	I_{DDQ_DDR0}	760	mA	DDR0_VDDQ
	PHY power supply current	I_{DDQLP_DDR0}	253	mA	DDR0_VDDQLP
	1.8-V PLL power supply current	I_{DDVAA_DDR0}	5	mA	DDR0_VAA
GBETH Ch0	I/O power supply current	I_{DD1833_ET0}	9	mA	VDD1833_ET0
GBETH Ch1	I/O power supply current	I_{DD1833_ET1}	9	mA	VDD1833_ET1
MIPI CSI Ch0	1.8-V PHY power supply current	$I_{DDMSVDD18\_CSI0}$	11	mA	CSI0_MSVDD18
	0.8-V core power supply current	$I_{DDMSVDD0P8\_CS0}$	39	mA	CSI0_MSVDD0P8
MIPI DSI	0.8-V core power supply current	I_{DD0P8_DSI}	112	mA	DSI_VDD0P8
	1.2-V PHY power supply current	I_{DD12_DSI}	8	mA	DSI_VDD12
	1.8-V PHY power supply current	I_{DD18_DSI}	11	mA	DSI_VDD18

Table 3.3 Max. Supply Currents during Operation (2/2)

Unit Name	Item	Symbol	Max.	Unit	Note
PCIE	1.8-V power supply current	$I_{DDPCIEVCC18ACMN}$	18	mA	PCIE_VCC18ACMN
	1.8-V PHY power supply current	$I_{DDPCIEVCC18AL01}$	53	mA	PCIE_VCC18AL01
	0.8-V PHY power supply current	$I_{DDPCIEVCC08AL01}$	83	mA	PCIE_VCC08AL01
I3C	I/O power supply current	I_{DD1218_I3C}	2	mA	VDD1218_I3C
ADC	1.8-V analog power supply current	$I_{DDADAVDD18}$	2	mA	ADAVDD18
LVDS Ch0, LVDS Ch1 common	LVDS 1.8V power supply current	$I_{DDLVDSVDD18}$	91	mA	LVDS_VCCQ
CPG	PLLCM33 1.8-V power supply current	$I_{DDPLVDD\_PLLCM33}$	2	mA	PLVDD_PLLCM33
	PLLCA55 1.8-V power supply current	$I_{DDPLVDD\_PLLCA55}$	2	mA	PLVDD_PLLCA55
	PLLVDD_OTHERS 1.8-V power supply current	$I_{DDPLVDD\_PLLOTHERS}$	15	mA	PLVDD_OTHERS
	PLLCM33 0.8-V power supply current	$I_{DDPLVDD08\_PLLCM33}$	3	mA	PLDVDD08_PLLCM33
	PLLCA55 0.8-V power supply current	$I_{DDPLVDD08\_PLLCA55}$	3	mA	PLDVDD09_PLLCA55
	PLLVDD_OTHERS 0.8-V power supply current	$I_{DDPLVDD08\_PLLOTHERS}$	18	mA	PLDVDD08_OTHERS
PWC	1.8-V I/O power supply current	I_{DD18_PWC}	2	mA	VDD18_PWC

3.4.2 Standard I/O Characteristics

For the I/O types, refer to the external pin list in **2.2 External Pins and Multiplexed Functional Pins**.

Table 3.4 DC Characteristics (Standard I/O)

V_{DD} = 1.14 V to 1.89 V (1.8/1.2-V switching I/O type), V_{DD} = 1.71 V to 1.89 V (3.3/1.8-V switching I/O types 3*[13], 4*[13] and 1.8-V OSC I/O type), V_{DD} = 1.71 V to 3.46 V (3.3/1.8-V switching I/O types 1, 2)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
External voltage tolerance	3.3/1.8-V switching I/O type 3	V_{TOL}	—	—	3.6	V	V_{DD} power-off & on
High-level input voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{IH}	0.8 × V_{DD}	—	V_{DD} + 0.3	V	—
	1.8/1.2-V switching I/O type (1.8 V)	V_{IH}	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
	1.8-V OSC I/O type 3.3/1.8-V switching I/O type 2 (1.8 V)	V_{IH}	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
	3.3/1.8-V switching I/O type 1 3.3/1.8-V switching I/O type 3 3.3/1.8-V switching I/O type 4 (1.8 V)	V_{IH}	0.75 × V_{DD}	—	V_{DD} + 0.3	V	—
	3.3/1.8-V switching I/O type 1 3.3/1.8-V switching I/O type 2 (3.3 V)	V_{IH}	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low-level input voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{IL}	−0.3	—	0.2 × V_{DD}	V	—
	1.8/1.2-V switching I/O type (1.8 V)	V_{IL}	−0.3	—	0.3 × V_{DD}	V	—
	1.8-V OSC I/O type 3.3/1.8-V switching I/O type 1 3.3/1.8-V switching I/O type 2 3.3/1.8-V switching I/O type 3 3.3/1.8-V switching I/O type 4 (1.8 V)	V_{IL}	−0.3	—	0.3 × V_{DD}	V	—
	3.3/1.8-V switching I/O type 1 3.3/1.8-V switching I/O type 2 (3.3 V)	V_{IL}	−0.3	—	0.3 × V_{DD}	V	—
Hysteresis voltage	1.8/1.2-V switching I/O type	ΔV	0.1 × V_{DD}	—	—	V	—
	3.3/1.8-V switching I/O type 3*[2] 3.3/1.8-V switching I/O type 4*[1]	ΔV	0.08 × V_{DD}	—	—	V	—
	3.3/1.8-V switching I/O type 2*[14]	ΔV	0.1	—	—	V	—

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
Input leakage current	1.8/1.2-V switching I/O type (1.2 V)	I_I	−10	—	10	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-on
			−10	—	10	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-off
	1.8/1.2-V switching I/O type (1.8 V)	I_I	−18	—	18	µA	V_{in} = V_{DD} max & V_{DD} power-on
			−18	—	18	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-off
	1.8-V OSC I/O type 3.3/1.8-V switching I/O type 1	I_I	−12	—	12	µA	V_{in} = V_{DD} max & V_{DD} power-on
	3.3/1.8-V switching I/O type 3	I_I	−18	—	18	µA	V_{in} = V_{DD} max & V_{DD} power-on
			−18	—	18	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-off
	3.3/1.8-V switching I/O type 2 3.3/1.8-V switching I/O type 4	I_I	−12	—	12	µA	V_{in} = V_{DD} max & V_{DD} power-on
Input pull-down resistor current	1.8/1.2-V switching I/O type*3 (1.2 V)	I_{RPU}	10	—	100	µA	V_{in} = V_{DD} max
	1.8/1.2-V switching I/O type*3 (1.8 V)	I_{RPU}	25	—	130	µA	V_{in} = V_{DD} max
	3.3/1.8-V switching I/O type 1*7 3.3/1.8-V switching I/O type 3*9 3.3/1.8-V switching I/O type 4*5	I_{RPU}	25	—	200	µA	V_{in} = V_{DD} max
	3.3/1.8-V switching I/O type 2*11	I_{RPU}	18	—	148	µA	V_{in} = V_{DD} max
Input pull-up resistor current	1.8/1.2-V switching I/O type*4 (1.2 V)	I_{RPD}	−10	—	−100	µA	V_{in} = V_{SS}
	1.8/1.2-V switching I/O type*4 (1.8 V)	I_{RPD}	−35	—	−185	µA	V_{in} = V_{SS}
	3.3/1.8-V switching I/O type 1*8 3.3/1.8-V switching I/O type 3*10 3.3/1.8-V switching I/O type 4*6	I_{RPD}	−25	—	−200	µA	V_{in} = V_{SS}
	3.3/1.8-V switching I/O type 2*12	I_{RPD}	−18	—	−192	µA	V_{in} = V_{SS}

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
High-level output voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1/−2/−4/−6 mA (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.8 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	1.8-V OSC I/O type	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (1.8 V) 3.3/1.8-V switching I/O type 3 (1.8V) 3.3/1.8-V switching I/O type 4 (1.8V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.6/−3.2/−6.4/−9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (3.3 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 2 (1.8 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −5/−6/−7/−10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 2 (3.3 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −9/−11/−13/−18 mA (drive strength X1/X2/X4/X6)
Low-level output voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1/2/4/6 mA (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.8 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	1.8-V OSC I/O type	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (1.8 V) 3.3/1.8-V switching I/O type 3 (1.8V) 3.3/1.8-V switching I/O type 4 (1.8V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.6/3.2/6.4/9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (3.3 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 2 (1.8 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 5/6/7/10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 2 (3.3 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 9/11/13/18 mA (drive strength X1/X2/X4/X6)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
Pull-up resistance	1.8/1.2-V switching I/O type*4 (1.2 V)	R_{PU}	15	—	160	kΩ	—
	1.8/1.2-V switching I/O type*4 (1.8 V)	R_{PU}	10	—	50	kΩ	—
	3.3/1.8-V switching I/O type 1*8 (1.8 V) 3.3/1.8-V switching I/O type 3*10 (1.8 V) 3.3/1.8-V switching I/O type 4*6 (1.8 V)	R_{PU}	10	—	50	kΩ	—
	3.3/1.8-V switching I/O type 1*8 (3.3 V)	R_{PU}	10	—	100	kΩ	—
	3.3/1.8-V switching I/O type 2*12	R_{PU}	12	—	92	kΩ	—
Pull-down resistance	1.8/1.2-V switching I/O type*3 (1.2 V)	R_{PD}	15	—	160	kΩ	—
	1.8/1.2-V switching I/O type*3 (1.8 V)	R_{PD}	15	—	60	kΩ	—
	3.3/1.8-V switching I/O type 1*7 (1.8 V) 3.3/1.8-V switching I/O type 3*9 (1.8 V) 3.3/1.8-V switching I/O type 4*5 (1.8 V)	R_{PD}	10	—	50	kΩ	—
	3.3/1.8-V switching I/O type 1*7 (3.3 V)	R_{PD}	10	—	100	kΩ	—
	3.3/1.8-V switching I/O type 2*11	R_{PD}	13	—	92	kΩ	—
Input capacitance	—	C_{in}	—	—	10	pF	

Note 1. Only for the QRESN and QRESNSEL pin

Note 2. When the RIIC function is in use or the value of the PFC_SMT_mn register is 1

Note 3. Only for the P20 and P21 pins (when the value of the PFC_PUPD_mn register is 10b)

Note 4. Only for the P20 and P21 pins (when the value of the PFC_PUPD_mn register is 11b)

Note 5. Only for the QBYPASS, BSCANP, MD_BOOT0, MD_BOOT3, and BOOTSELCPU pins

Note 6. Only for the MD_BOOT1, MD_BOOT2 and MD_CLKS pins

Note 7. Only for the WDTUDFCA, WDTUDFCM, and SCIF_RXD, SCIF_TXD pins (when the value of the PFC_PUPD_mn register is 10b)

Note 8. Only for the WDTUDFCA, WDTUDFCM, and SCIF_RXD, SCIF_TXD pins (when the value of the PFC_PUPD_mn register is 11b)

Note 9. When the value of the PFC_PUPD_mn register is 10b

Note 10. When the value of the PFC_PUPD_mn register is 11b

Note 11. Only for the pins other than SD0CLK, SD0RSTN, SD0PWEN, and SD0IOVS (when the value of the PFC_PUPD_mn register is 10b)

Note 12. Only for the pins other than SD0CLK, SD0RSTN, SD0PWEN, and SD0IOVS (when the value of the PFC_PUPD_mn register is 11b)

Note 13. This type IO can be available both 3.3 V and 1.8 V buffers, but it is fixed at 1.8 V buffer.

Note 14. Only for the pins other than SD0CLK, SD0CMD, SD0DAT0-SD0DAT7, SD0PWEN, SD0IOVS, and SD0RSTN (when the RIIC function is in use or the value of the PFC_SMT_mn register is 1)

Table 3.5 DC Characteristics (LVDS)

V_{DD} = 1.71 V to 1.89 V (I/O type[LVDS])

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
Output differential voltage	LVDS	|VOD|	250	—	450	mV	TIA-EIA-644 Termination load = 100Ω
Output offset voltage	LVDS	VOS	1.125	—	1.375	V	TIA-EIA-644 Termination load = 100Ω
Change in |VOD| between 0 and 1	LVDS	ΔVOD	—	—	50	mV	TIA-EIA-644 Termination load = 100Ω
Change in VOS between 0 and 1	LVDS	ΔVOS	—	—	50	mV	TIA-EIA-644 Termination load = 100Ω

3.5 AC Characteristics

Conditions:

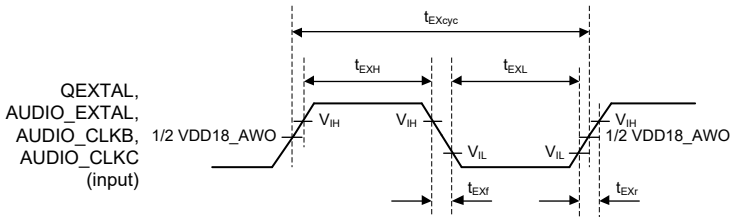
VDD18 = VDD18_AWO = ADAVDD18 = VDD1833_* (1.8 V mode)

VDD33 = VDD1833_* (3.3 V mode)

3.5.1 Clock Timing

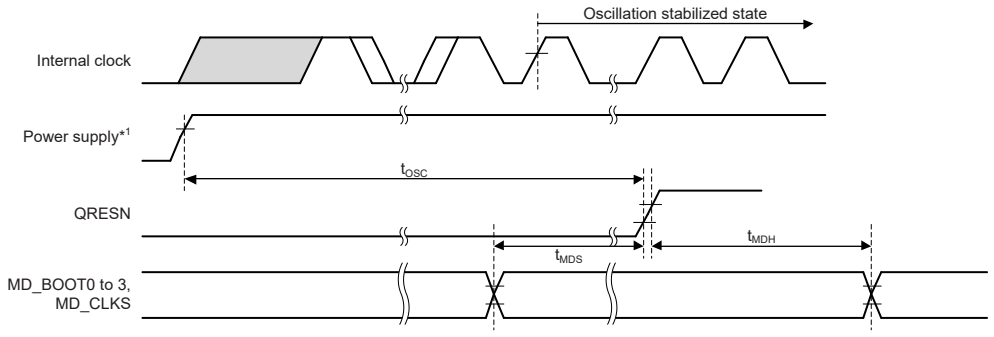
Table 3.6 Clock Timing Table

Item	Symbol	Min.	Max.	Unit	Figures
QEXTAL clock input frequency	f_{EX}	24 −50 ppm	24 +50 ppm	MHz	**Figure 3.11**
QEXTAL clock input cycle time	t_{EXcyc}	41.67	41.67	ns	
AUDIO_EXTAL clock input frequency	f_{EX}	4	48	MHz	
AUDIO_EXTAL clock input cycle time	t_{EXcyc}	20.83	250	ns	
AUDIO_CLKB, AUDIO_CLKC clock input frequency (external clock is input)	f_{EX}	4	50	MHz	
AUDIO_CLKB, AUDIO_CLKC clock input cycle time (external clock is input)	t_{EXcyc}	20	250	ns	
QEXTAL clock input low-level pulse width	t_{EXL}	0.4	0.6	t_{EXcyc}	
QEXTAL clock input high-level pulse width	t_{EXH}	0.4	0.6	t_{EXcyc}	
AUDIO_XTAL, AUDIO_CLKB, AUDIO_CLKC clock input low-level pulse width	t_{EXL}	0.45	0.55	t_{EXcyc}	
AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input high-level pulse width	t_{EXH}	0.45	0.55	t_{EXcyc}	
QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input rise time	t_{EXr}	—	4	ns	
QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input fall time	t_{EXf}	—	4	ns	
Mode hold time	t_{MDH}	—	100	ns	**Figure 3.12**
Mode setup time	t_{MDS}	—	100	ns	



Note: When the clock is input on the QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, or AUDIO_CLKC

Figure 3.11 Clock Input Timing



Note 1. 1st Grp power supply (refer to **3.3 Power-On/Off Sequence**)

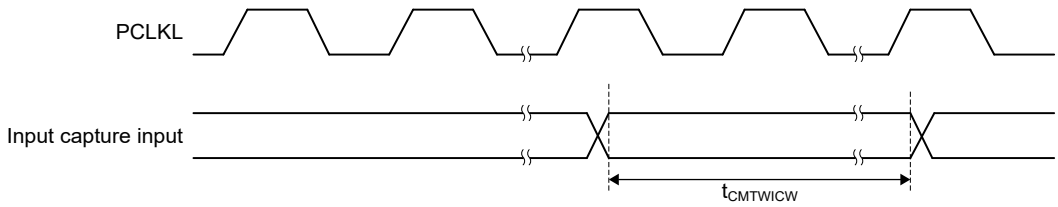
Figure 3.12 Power-On Oscillation Settling Time

3.5.2 CMTW Timing

Table 3.7 CMTW Timing

Parameter			Symbol	Min.	Max.	Unit	Figure
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PLcyc}*1	**Figure 3.13**
		Both-edge setting		2.5	—		

Note 1. t_{PLcyc}: PCLKL cycle



Note: PCLKL: CMTWn_clkm (n = 0 to 7)

Figure 3.13 CMTW Input Capture Input Timing

3.5.3 POEG and GPT Trigger Timings

GPT Conditions: High-drive output is selected in the PFC register.

Table 3.8 POEG and GPT Trigger Timings

Parameter			Symbol	Min.	Max.	Unit	Figure
POEG	POEG input trigger pulse width		t_{POEW}	1.5	—	t_{Pcyc}*1	**Figure 3.14**
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}*2	**Figure 3.15**
		Dual edge	t_{GTICW}	2.5	—		

Note 1. t_{Pcyc}: POEGx_n_PCLK cycle (x = A to D, n = 0, 1)

Note 2. t_{PDcyc}: GPT_n_clks_gpt cycle (n = 0, 1)

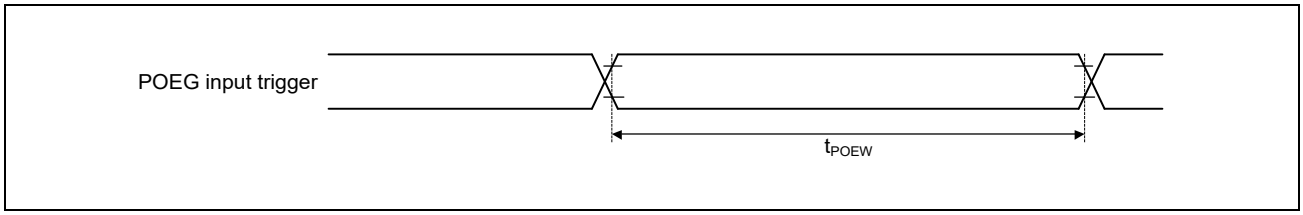


Figure 3.14 POEG Input Trigger Timing

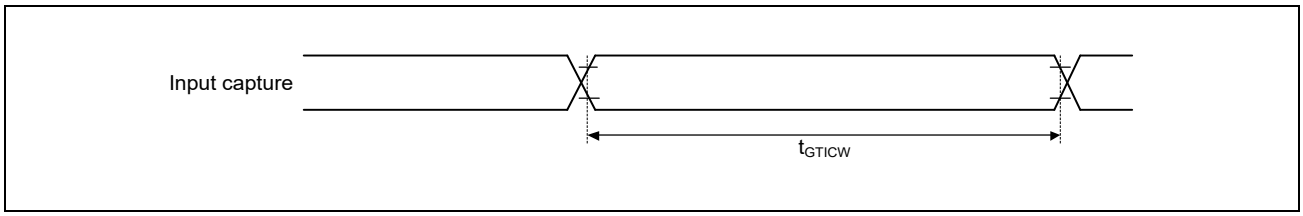


Figure 3.15 GPT Input Capture Timing

3.5.4 Watchdog Timer Access Timing

Table 3.9 Watchdog Timer Timing

Item	Symbol	Min.	Max.	Unit	Figures
WDTUDFCM / WDTUDFCA output time	t_L	64	64	t_{P1cyc}*1	**Figure 3.16**

Note 1. t_{P1cyc} indicates peripheral clock WDT_n_clk_loco (n = 0 to 3).

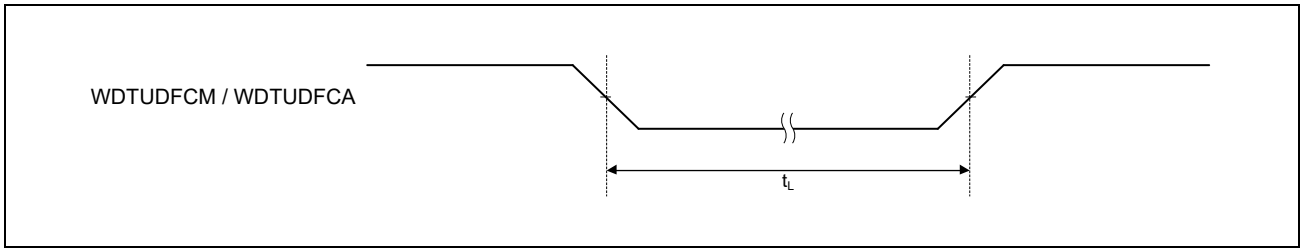


Figure 3.16 Watchdog Timer Output Timing

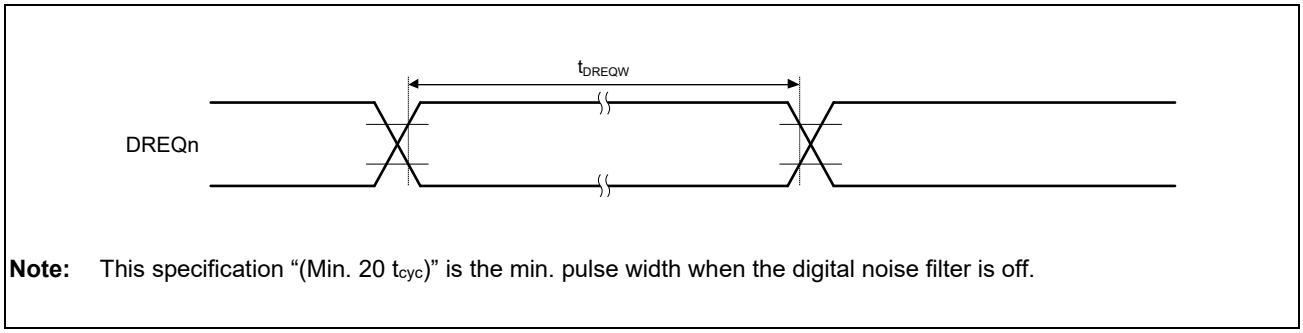
3.5.5 DMAC Timing

Table 3.10 DMAC Timing

Item	Symbol	Min.	Max.	Unit	Figures
DREQn pulse width	t_{DREQW}	20	—	t_{cyc}*1	**Figure 3.17**
TENDn pulse width	t_{TENDW}	16	16	$t_{PCLKcyc}$*2	**Figure 3.18**

Note 1. t_{cyc} = 41.666 ns (24 MHz)

Note 2. $t_{PCLKcyc}$ = 10 ns (100 MHz): ICU_0_PCLK_I cycle



Note: This specification “(Min. 20 t_{cyc})” is the min. pulse width when the digital noise filter is off.

Figure 3.17 DMAC DREQn Timing

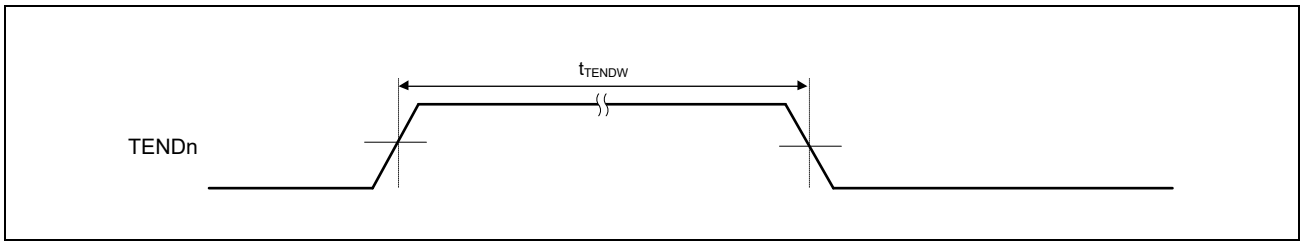


Figure 3.18 DMAC TENDn Timing

3.5.6 LPDDR4 PHY Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4B / JEDEC 209-4-1 standard.

3.5.7 SD Access Timing

Conditions:

V_{OH} = VDD33 × 0.7

V_{OL} = VDD33 × 0.3

C = 40 pF (3.3 V)

Drive strength: ×6

3.5.7.1 SD Access Timing (SDR 3.3-V)

Table 3.11 SD AC Access Timing (SDR at 3.3-V Operation)

Item	Symbol	Default Speed Mode (25 MHz)		High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.	Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	40.0	—	20.0	—	ns	**Figure 3.19**
SDnCLK clock high level width	t_{SDWH}	10	—	7	—	ns	
SDnCLK clock low level width	t_{SDWL}	10	—	7	—	ns	
SDnCLK clock rise time	t_{SDLH}	—	10	—	3	ns	
SDnCLK clock fall time	t_{SDHL}	—	10	—	3	ns	
SDnCMD,SDnDATm output delay	t_{SDODLY}	−7.5	2.5	−6.2	2.5	ns	
SDnCMD,SDnDATm input set up time	t_{SDIS}	4.0	—	4.0	—	ns	
SDnCMD,SDnDATm input hold time	t_{SDIH}	2.0	—	2.0	—	ns	
SDnCMD,SDnDATm input data width	t_{SDIDW}	—	—	—	—	ns	

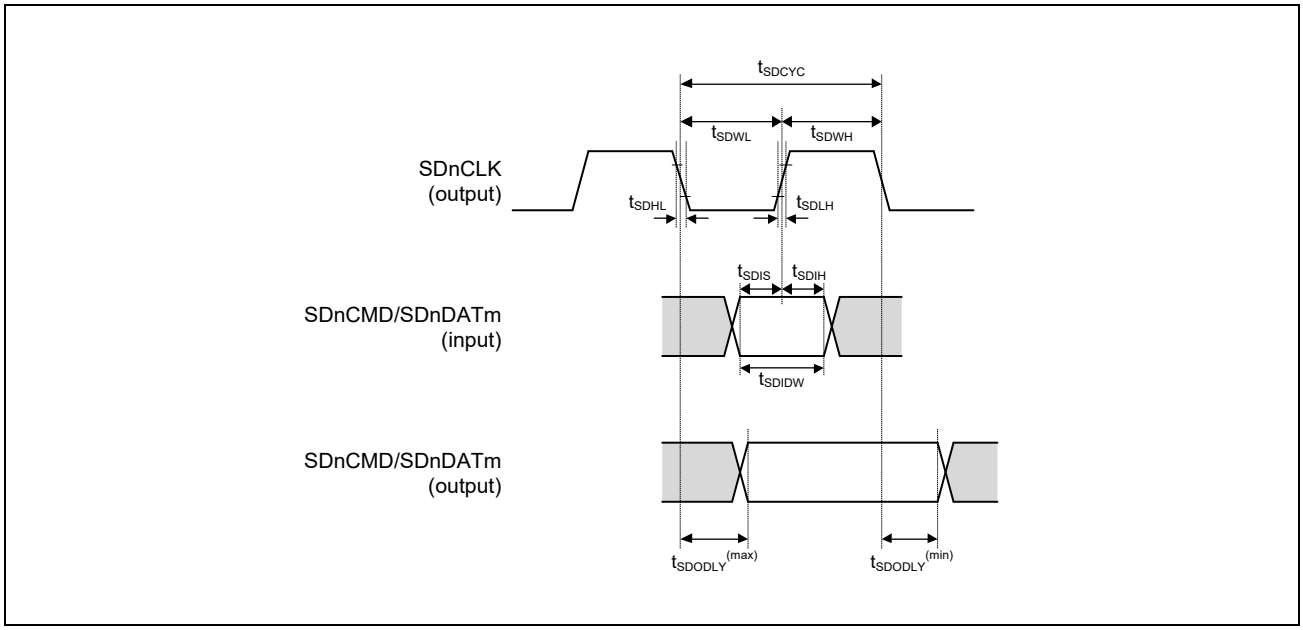


Figure 3.19 SDHC Interface Timing (SDR 3.3-V Power Supply)

NOTE

The disclosure of other characteristics of the SD interface needs the conclusion of the following agreement.

- SD Host/Ancillary Product License Agreement (SD HALA)

For details, contact Renesas sales representatives.

3.5.8 eMMC Access Timing

Conditions:

V_{OH} = VDD18 × 0.7, V_{OL} = VDD18 × 0.3, C = 15 pF (1.8 V)

V_{OH} = VDD33 × 0.7, V_{OL} = VDD33 × 0.3, C = 30 pF (3.3 V)

Drive strength: ×6

3.5.8.1 eMMC host interface timing (default)

Table 3.12 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	20.0	—	ns	**Figure 3.20**
SDnCLK clock high level width	t_{MMCWH}	7	—	ns	
SDnCLK clock low level width	t_{MMCWL}	7	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−6.2	2.5	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	4.0	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	2.0	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	—	—	ns	

Table 3.13 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	20.0	—	ns	**Figure 3.20**
SDnCLK clock high level width	t_{MMCWH}	7	—	ns	
SDnCLK clock low level width	t_{MMCWL}	7	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−4.2	1.6	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	1.3	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	1.878	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	—	—	ns	

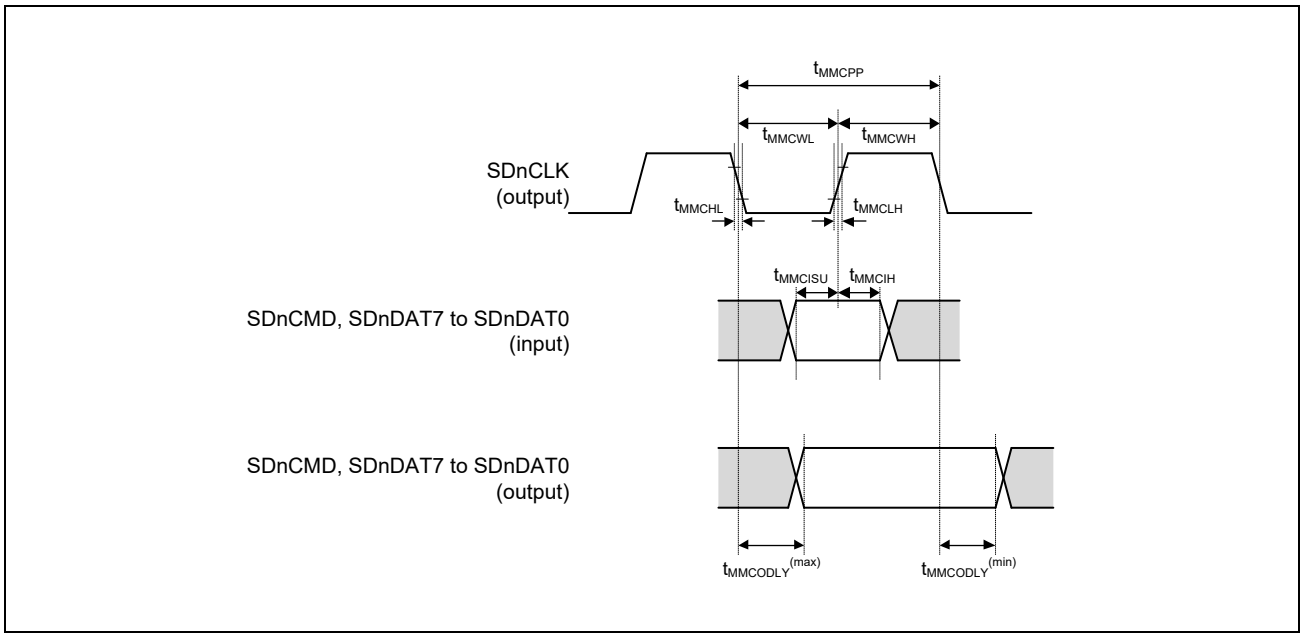


Figure 3.20 eMMC Host Interface Timing (MMC Default 1.8-V/3.3-V Power Supply)

3.5.8.2 eMMC host interface timing (HS-SDR)

NOTES

1. The spec of eMMC host interface timing (HS-SDR 3.3-V power supply) is the same as **Table 3.12 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)**.
2. The spec of eMMC host interface timing (HS-SDR 1.8V power supply) is the same as **Table 3.13 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)**.

3.5.8.3 eMMC host interface timing (HS-DDR)

Table 3.14 eMMC Host Interface Timing (HS-DDR 3.3-V Power Supply Operation)

Item	Symbol	High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	20.0	—	ns	**Figure 3.21**
SDnCLK clock high level width	t_{SDWH}	9.0	11.0	ns	
SDnCLK clock low level width	t_{SDWL}	9.0	11.0	ns	
SDnCLK clock rise time	t_{SDLH}	—	3.0	ns	
SDnCLK clock fall time	t_{SDHL}	—	3.0	ns	
SDnCMD output delay	t_{SDODLY}	−6.0	6.0	ns	
SDnCMD input set up time	t_{SDIS}	4.8	—	ns	
SDnCMD input hold time	t_{SDIH}	2.5	—	ns	
SDnDATm output delay	t_{SDODLY_DDR}	2.5	6.5	ns	
SDnDATm input set up time	t_{SDIS_DDR}	1.768	—	ns	
SDnDATm input hold time	t_{SDIH_DDR}	1.5	—	ns	

Table 3.15 eMMC Host Interface Timing (HS-DDR 1.8-V Power Supply Operation)

Item	Symbol	High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{MMCCYC}	20.0	—	ns	**Figure 3.21**
SDnCLK clock high level width	t_{MMCWH}	9.0	11.0	ns	
SDnCLK clock low level width	t_{MMCWL}	9.0	11.0	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3.0	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3.0	ns	
SDnCMD output delay	$t_{MMCODLY}$	−6.0	3.0	ns	
SDnCMD input set up time	t_{MMCIS}	4.8	—	ns	
SDnCMD input hold time	t_{MMCIH}	2.5	—	ns	
SDnDATm output delay	$t_{MMCODLY\_DDR}$	2.5	6.5	ns	
SDnDATm input set up time	t_{MMCIS_DDR}	1.768	—	ns	
SDnDATm input hold time	t_{SMMCIH_DDR}	1.5	—	ns	

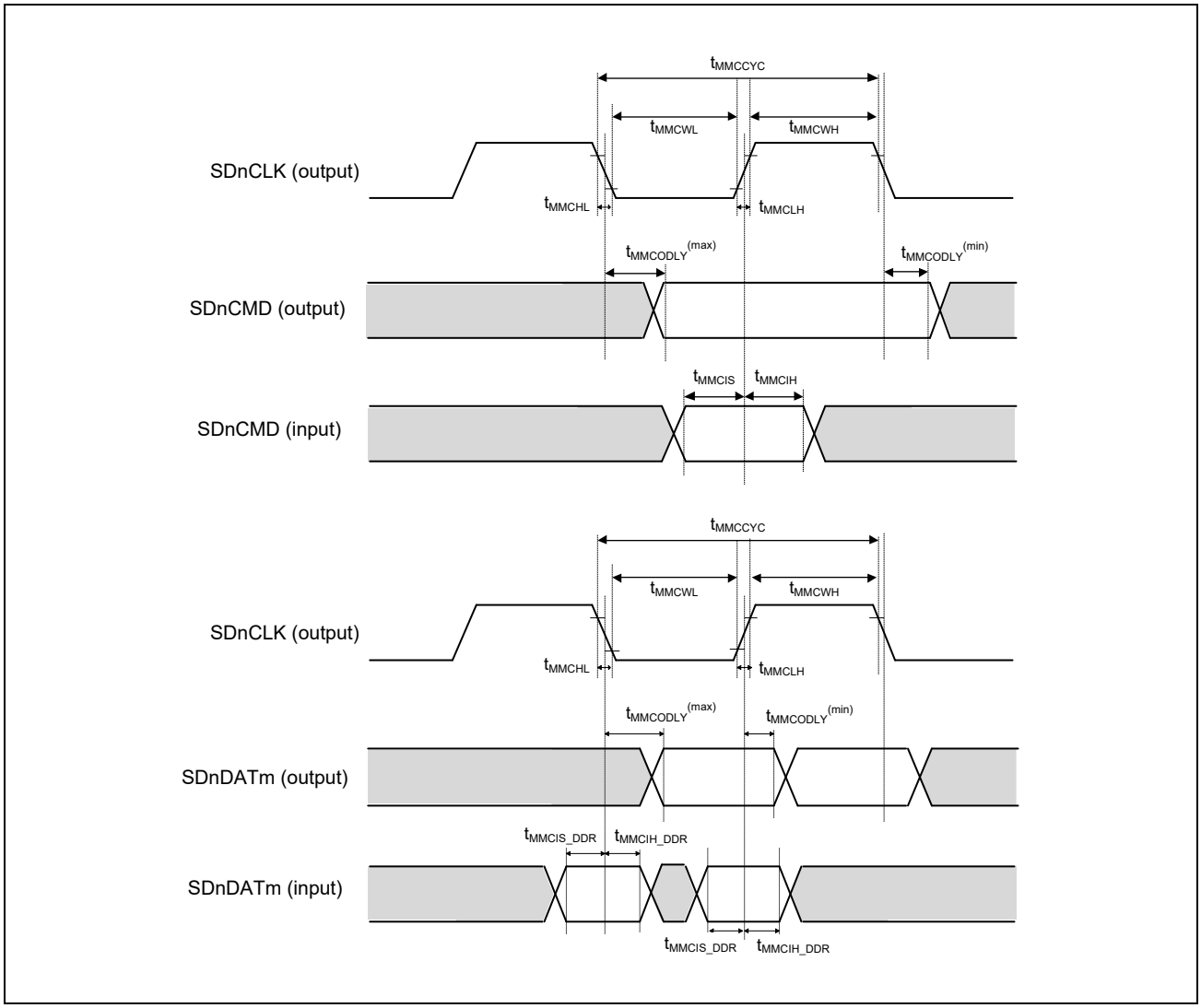


Figure 3.21 eMMC Host Interface (MMC Interface HS-DDR Mode 1.8/3.3-V Power Supply Selection)

3.5.8.4 eMMC host interface timing (HS200)

Table 3.16 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	5.0	10.0	ns	**Figure 3.22**
SDnCLK clock high level width	t_{MMCWH}	1.5	—	ns	
SDnCLK clock low level width	t_{MMCWL}	1.5	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	1.0	ns	
SDnCLK clock fall time	t_{MMCHL}	—	1.0	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−1.7	0.9	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	—	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	—	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	2.88	—	ns	

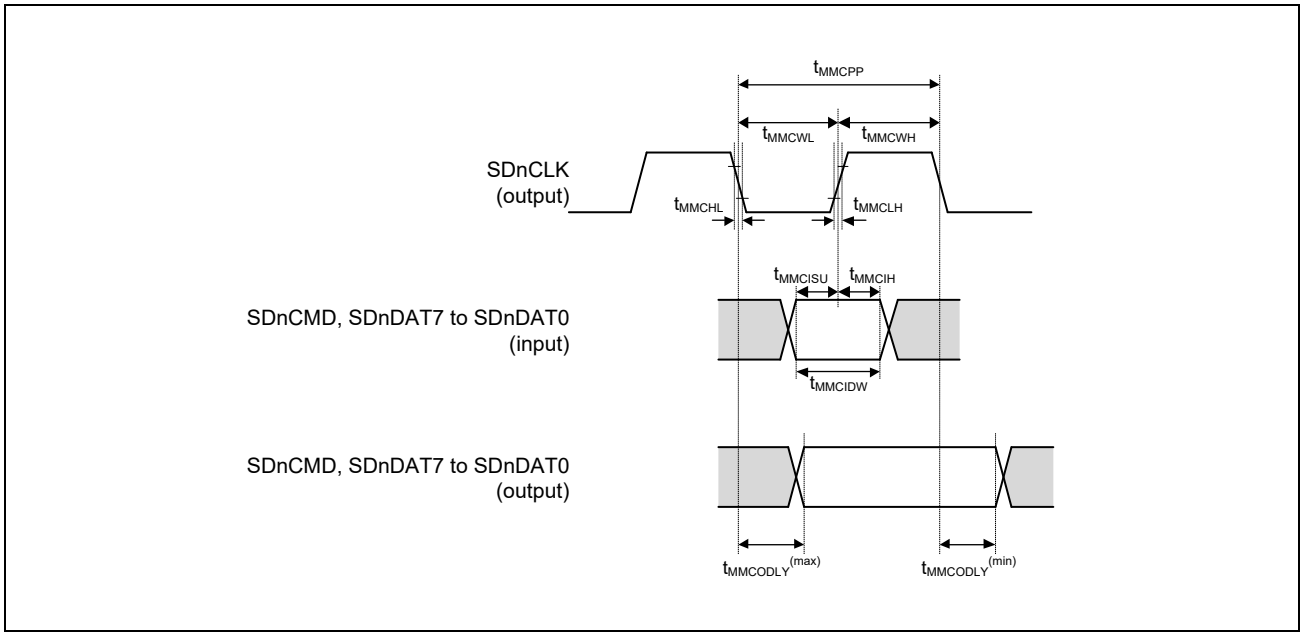


Figure 3.22 eMMC Host Interface (MMC Interface HS200 Mode 1.8-V Power Supply Selection)

3.5.9 Ethernet Interface Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5

C = 15 pF (RGMII), 30 pF (MII)

Drive strength: ×2, ×4

Table 3.17 Ethernet Interface Timing (n = 0, 1)

Parameter			Symbol	Min.	Max.	Unit	Figure
Ethernet (RGMII)	ETn_TXC_TXCLK, ETn_RXC_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	**Figure 3.23**
		100 Mbps	$t_{RGMIIck}$	36	44	ns	
		10 Mbps	$t_{RGMIIck}$	360	440	ns	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK frequency	1 Gbps	—	125 − 50 ppm	125 + 50 ppm	MHz	
		100 Mbps	—	25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps	—	2.5 − 50 ppm	2.5 + 50 ppm	MHz	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK duty cycle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps	—	40	60	%	
	ETn_TXC_TXCLK, ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_RXC_RXCLK, ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV rise/fall time		t_{RGMIIr}, t_{RGMIIf}	—	0.75*1	ns	
	ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXC_TXCLK output skew		$t_{RGMIIos}$	−0.5	0.5	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV setup time		t_{RGMIIs}	1	—	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV hold time		t_{RGMIIh}	1	—	ns	
Ethernet (MII)	ETn_TXCLK, ETn_RXCLK cycle time	100 Mbps	t_{MIIck}	40	—	ns	**Figure 3.24**
		10 Mbps	t_{MIIck}	400	—	ns	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK frequency	100 Mbps	—	25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps	—	2.5 − 50 ppm	2.5 + 50 ppm	MHz	
	ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXER output delay time		t_{MIId}	0	20	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV, ETn_RXER setup time		t_{MIIs}	10	—	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV, ETn_RXER hold time		t_{MIIh}	10	—	ns	

Note 1. The measurement condition of t_{RGMIIr} and t_{RGMIIf} is in FIGURE 3 in Reduced Gigabit Media Independent Interface (RGMII) 12/10/2000 Version 1.3.

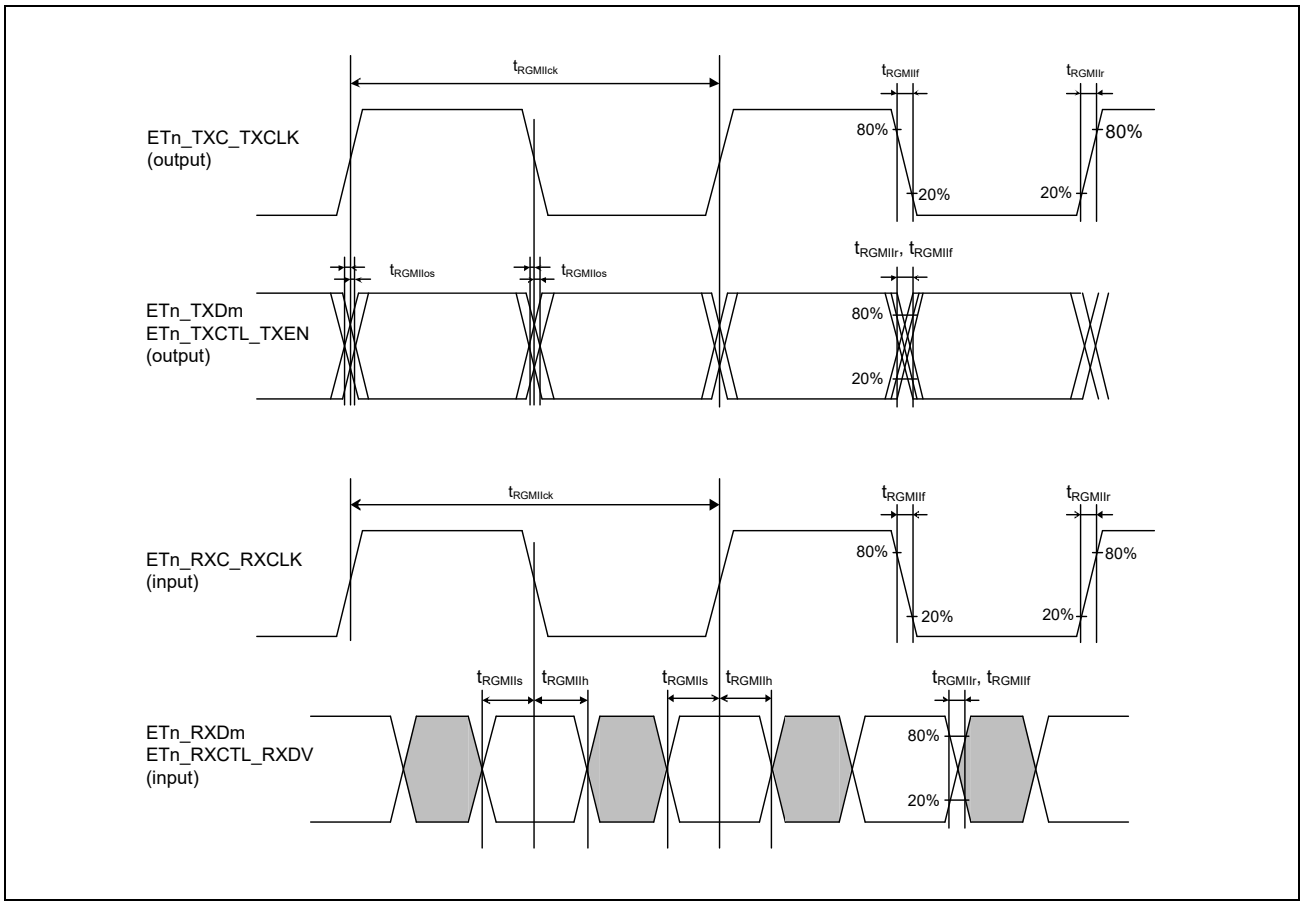


Figure 3.23 RGMII Transmission and Reception Timing (n = 0, 1)

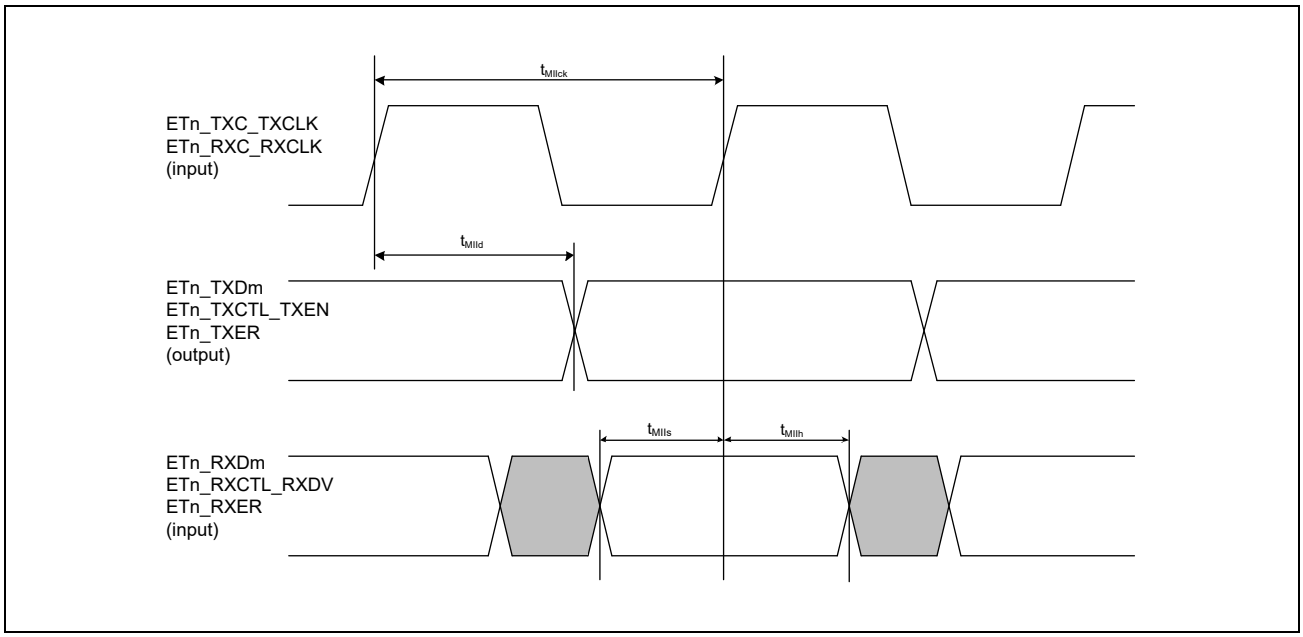


Figure 3.24 MII Transmission and Reception Timing (n = 0, 1)

3.5.10 USB 3.2 PHY Characteristics

The USB3 PHY of this LSI is compliant with the following USB 3.2 Gen2x1 standard:

Universal Serial Bus 3.2 Specification

3.5.11 USB 2.0 PHY Characteristics

The USB2 PHY of this LSI is compliant with the following USB 2.0 standard:

Universal Serial Bus 2.0 Specification

3.5.12 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of the PCI Express® Base Specification for Gen1/Gen 2/ Gen 3

3.5.13 xSPI Timing

Conditions:

- Single-end clock

  V_{OH} = VDD18 × 0.8, V_{OL} = VDD18 × 0.2, C = 15 pF (1.8 V)
  V_{OH} = VDD33 × 0.8, V_{OL} = VDD33 × 0.2, C = 15 pF (3.3 V)

- Data

  V_{OH} = VDD18 × 0.8, V_{OL} = VDD18 × 0.2, C = 15 pF (1.8 V)
  V_{OH} = VDD33 × 0.8, V_{OL} = VDD33 × 0.2, C = 15 pF (3.3 V)

Drive strength: ×6

Table 3.18 xSPI Timing (1/2)

Parameter		Symbol	1.8V		3.3V		Unit	Figure
			Min.	Max.	Min.	Max.		
Cycle time	SDR	t_{PERIOD}	7.5	—	12.5	—	ns	**Figure 3.25**
	DDR	t_{PERIOD}	7.5	—	12.5	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56*1	—	1.03	—	V/ns	
Clock duty cycle distortion		t_{CKDCD}	0.0	t_{PERIOD} × 0.05	0.0	t_{PERIOD} × 0.05	ns	
Clock minimum pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
Differential clock crossing voltage		$V_{OX(AC)}$	0.4 × VDD18	0.6 × VDD18	—	—	V	
DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*1	—	1.03	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	2.4	—	ns	**Figure 3.26**
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time		t_{OD}	—	1.6*2	—	1.8*2	ns	
Data output hold time		t_{OH}	−1.5	—	−2.3	—	ns	
Data output buffer off time		t_{BOFF}	−1.5	—	−2.3	—	ns	
Data input setup time (to DS)	DDR*2	t_{SU}	−0.6/−0.8*1	—	−0.6/−0.8*1	—	ns	**Figure 3.27**, **Figure 3.28**
Data input hold time (to DS)		t_{H}	t_{PERIOD} × 0.41 − 0.6/0.8*1	—	t_{PERIOD} × 0.41 – 0.6/0.8*1	—	ns	
Data output setup time (to CK)		t_{SUO}	0.6 / 1.0*1,*4	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	0.6 / 1.0*1,*4	—	1.0	—	ns	
CS low to clock high		t_{CSLCKH}	6.0/8.0*1,*3	—	8.0*3	—	ns	**Figure 3.26** to **Figure 3.28**
Clock low to CS high		t_{CKLCSH}	6.0/8.0*1	—	8.0	—	ns	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	

Table 3.18 xSPI Timing (2/2)

Parameter	Symbol	1.8 V		3.3 V		Unit	Figure
		Min.	Max.	Min.	Max.		
DS low to CS high	t_{DSLCSH}	t_{PERIOD} × 0.8*7	—	t_{PERIOD} × 0.8*7	—	ns	**Figure 3.29**
CS high to DS Tri-state	t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low*5	t_{CSLDSL}	0.0	12.5*6	0.0	17.4*6	ns	
DS Tri-state to CS low	t_{DSTCSL}	0.0	—	0.0	—	ns	
CK low to DS low*8	t_{CKLDSL}	—	(0.45 + e) × t_{PERIOD} – 2.0*9	—	(0.45 + e) × t_{PERIOD} – 2.0*9	ns	

Note: CK: XSPI0_CKP (XSPI0_CKN)
DS: XSPI0_DS
CS: XSPI0_CS0N, XSPI0_CS1N

Note 1. Specification at 133 MHz / Specification at 100 MHz

Note 2. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1b).

Note 3. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1b).

Note 4. The standard value for xSPI266 is 0.8 ns.

Note 5. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.

Note 6. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

Note 7. These are the values when the t_{CKLDSL} constraint is satisfied.

Note 8. This constraint is necessary only to satisfy the t_{DSLCSH} requirement specified in JESD251, which specifies that t_{DSLCSH} must be at least 80% of t_{PERIOD}. Set LIOCFGCSn.CSNEGEX to the appropriate value to ensure the memory specification complies with this constraint.

Note 9. e: LIOCFGCSn.CSNEGEX (e = 0, 1)

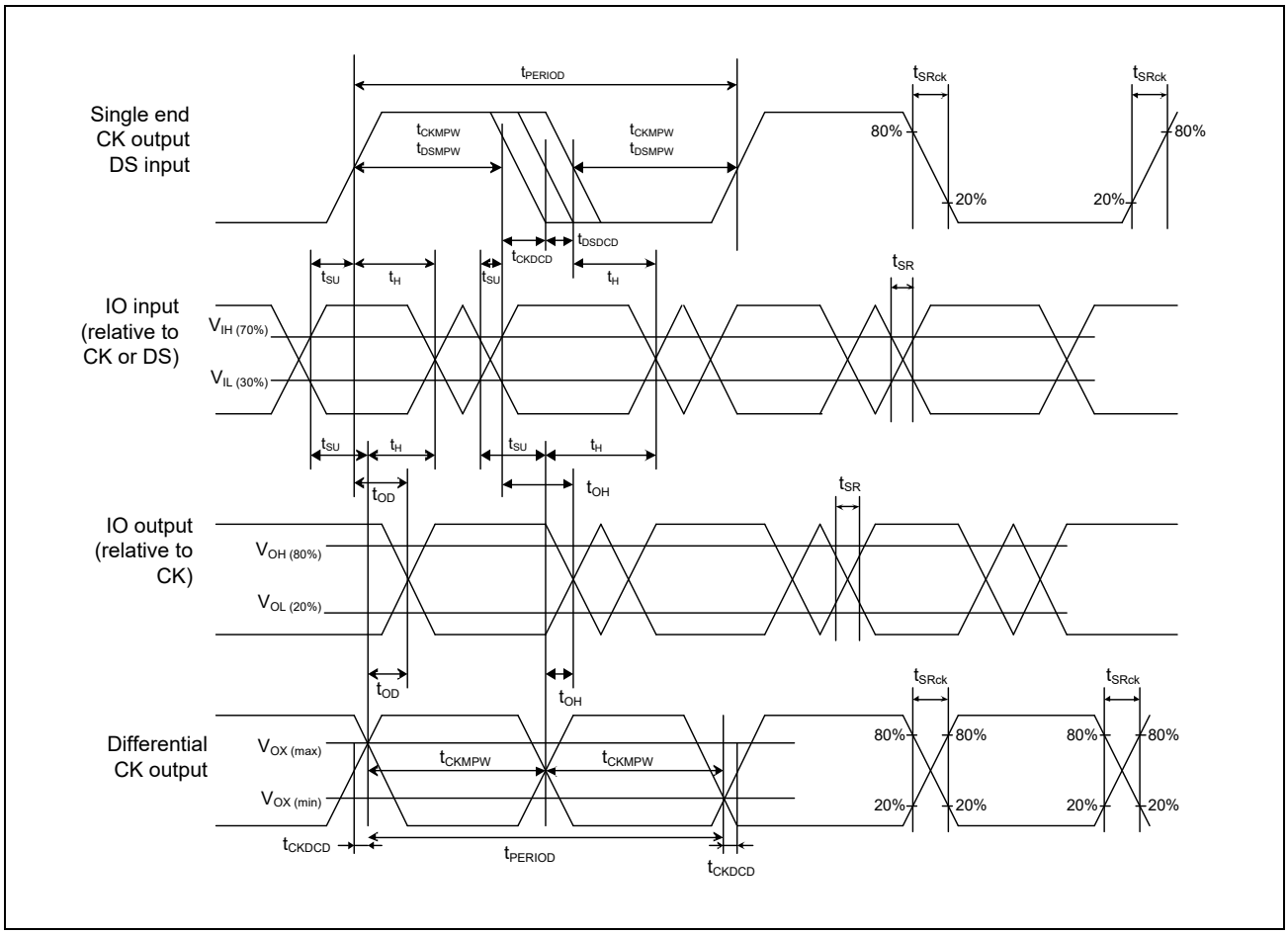


Figure 3.25 xSPI Clock / DS Timing

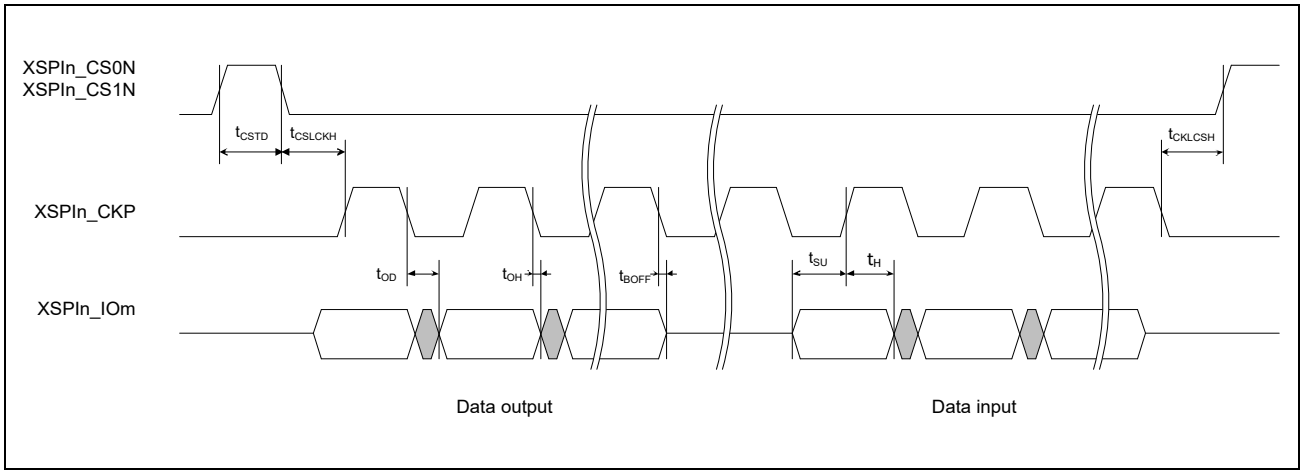


Figure 3.26 SDR Transmission and Reception Timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

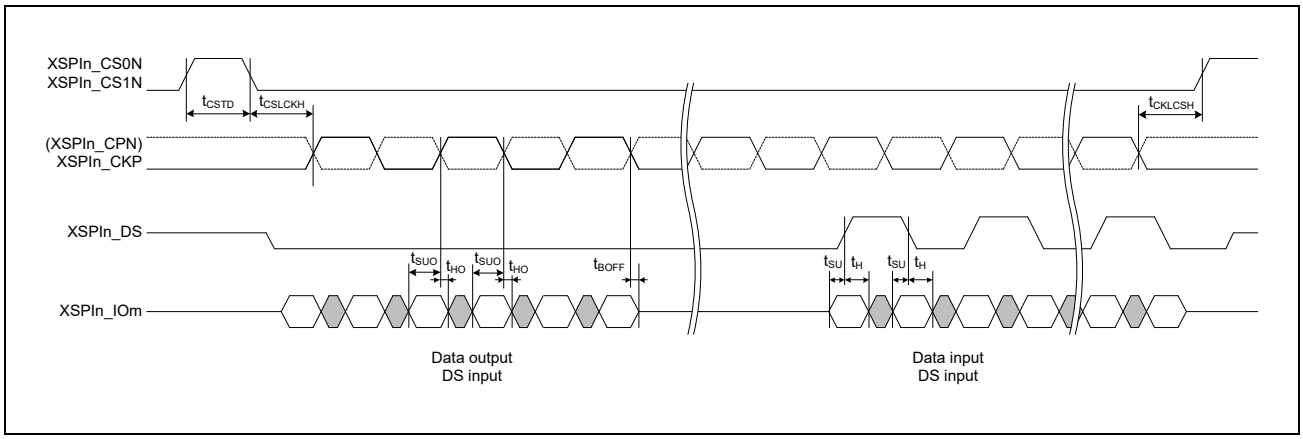


Figure 3.27 DDR Transmission and Reception Timing (4S-4D-4D, 8D-8D-8D)

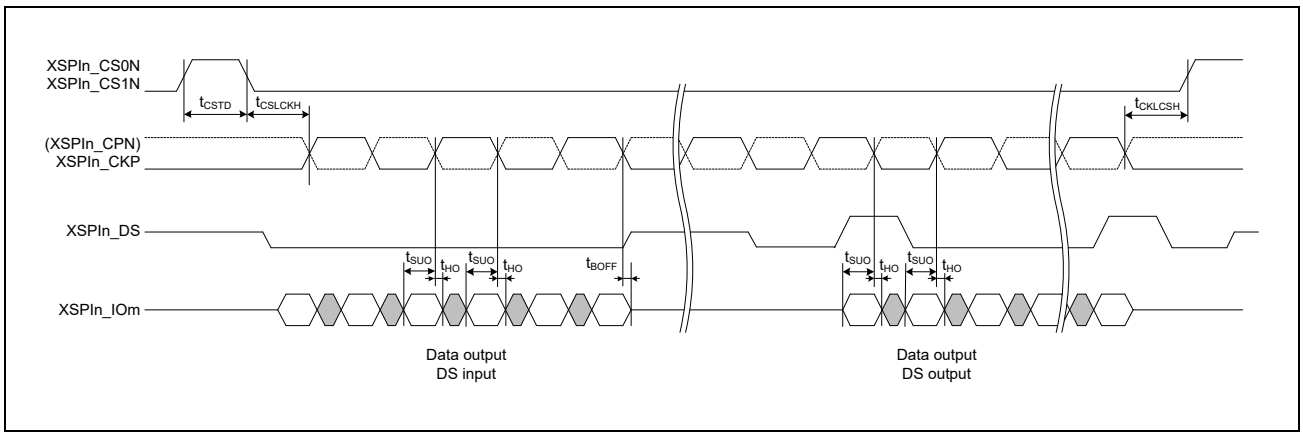


Figure 3.28 DDR Transmission and Reception Timing (HyperRAM write)

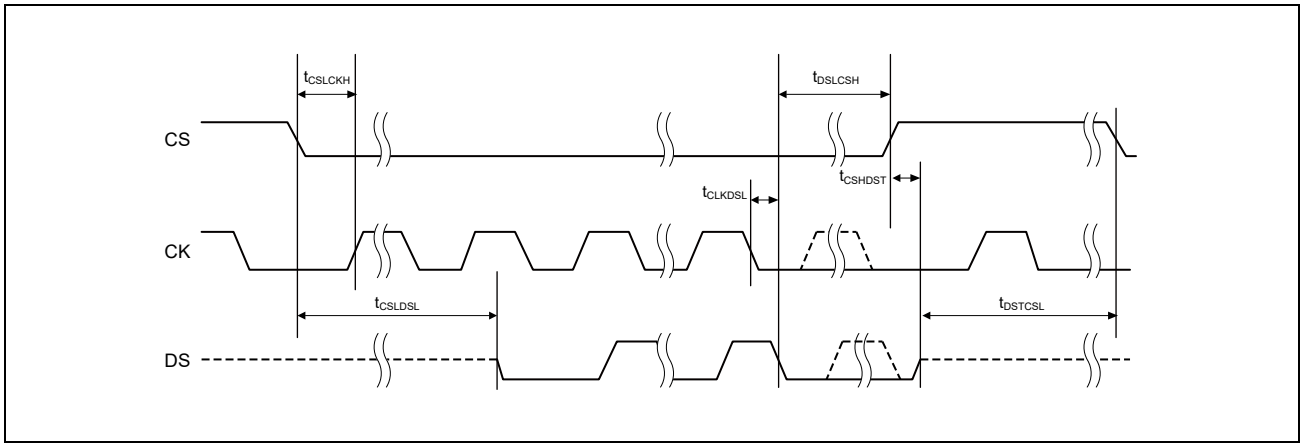


Figure 3.29 DS to CS Signal Timing

3.5.14 Serial Communications Interface (RSCI) Access Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (3.3 V)

Drive strength: ×2, ×4 (However, ×6 only for SCL (P00) and SDA (P01) of RSCI0 in simple I2C mode)

Table 3.19 RSCI Timing (1/2)

Parameter			Symbol	Min.	Max.	Unit	Figure
RSCI (Asynchronous)	Input clock cycle		t_{Scyc}	4	—	$t_{PSCIcyc}$	**Figure 3.30**
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	3	ns	
	Input clock fall time		t_{SCKf}	—	3	ns	
	Output clock cycle		t_{Scyc}	6	—	$t_{PSCIcyc}$	
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	V_{DD1833} = 1.8 V	t_{SCKr}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Output clock fall time	V_{DD1833} = 1.8 V	t_{SCKf}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
RSCI (Simple I2C, Standard mode)	SDA input rise time		t_{Sr}	—	1000	ns	**Figure 3.31**
	SDA input fall time		t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	2 × NFcyc*1	ns	
	Data input setup time		t_{SDAS}	250	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b	—	400	pF	
RSCI (Simple I2C, Fast mode)	SDA input rise time		t_{Sr}	—	300	ns	**Figure 3.31**
	SDA input fall time		t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	2 × NFcyc*1	ns	
	Data input setup time		t_{SDAS}	100	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b	—	400	pF	

Table 3.19 RSCI Timing (2/2)

Parameter			Symbol	Min.	Max.	Unit	Figure
RSCI (Clock sync, Simple SPI)	SCK output clock cycle (master)		t_{SPcyc}	4	65536	$t_{PSCIcyc}$	**Figure 3.32** to **Figure 3.37**
	SCK input clock cycle (slave)			4	65536	$t_{PSCIcyc}$	
	SCK clock high-level pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low-level pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Input clock rise time		t_{SPCKR}	—	3	ns	
	Input clock fall time		t_{SPCKF}	—	3	ns	
	Output clock rise time	V_{DD1833} = 1.8 V	t_{SPCKR}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Output clock fall time	V_{DD1833} = 1.8 V	t_{SPCKF}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Data input setup time	Internal clock	t_{SU}	7	—	ns	
		External clock		3	—	ns	
	Data input hold time	Internal clock	t_H	3	—	ns	
		External clock		3	—	ns	
	Data output delay time	Internal clock	t_{OD}	—	3	ns	
		External clock		—	12	ns	
	Data output hold time	Internal clock	t_{OH}	−3	—	ns	
		External clock		0	—	ns	
	Data rise/fall time	V_{DD1833} = 1.8 V	t_{DR}, t_{DF}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Slave access time	Internal clock	t_{SA}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12	ns	
	Slave output release time	Internal clock	t_{REL}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12	ns	
RSCI (Simple SPI)	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	**Figure 3.32** to **Figure 3.37**
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSR}, t_{SSF}	—	3	ns	

Note: $t_{PSCIcyc}$: RSCI_n_TCLK cycle (n = 1 to 9)

Note 1. NFcyc = 4p × 2q − 1 × $t_{PSCIcyc}$
p: CCR2.CKS[1:0] (p = 0, 1, 2, 3)
q: CCR1.NFCS[2:0] (q = 1, 2, 3, 4)

Note 2. Output transition time from 20% to 80%

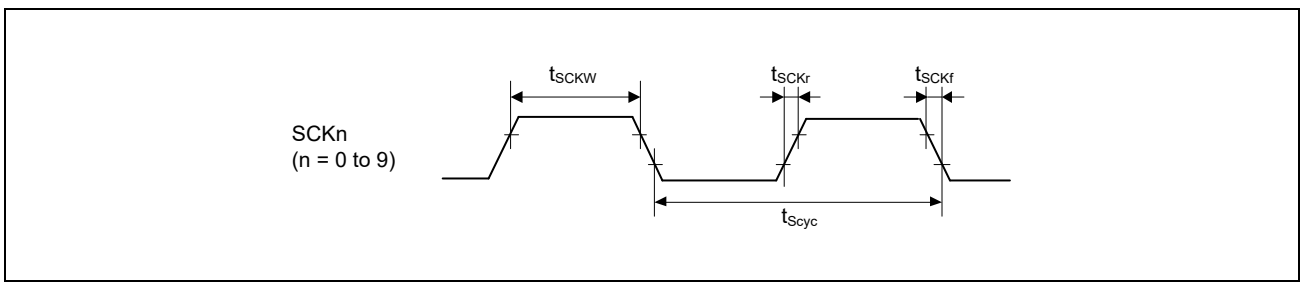
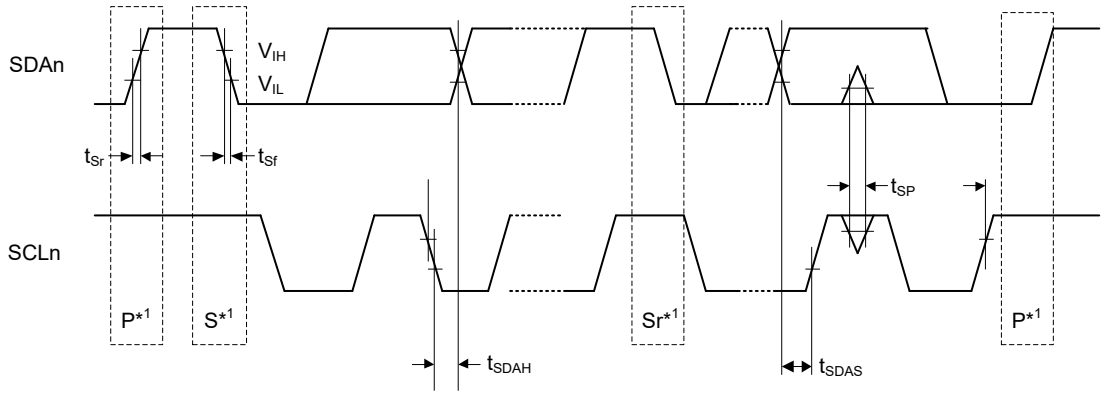


Figure 3.30 SCK Clock Input/Output Timing



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 3.31 RSCI Simple I2C Mode Timing

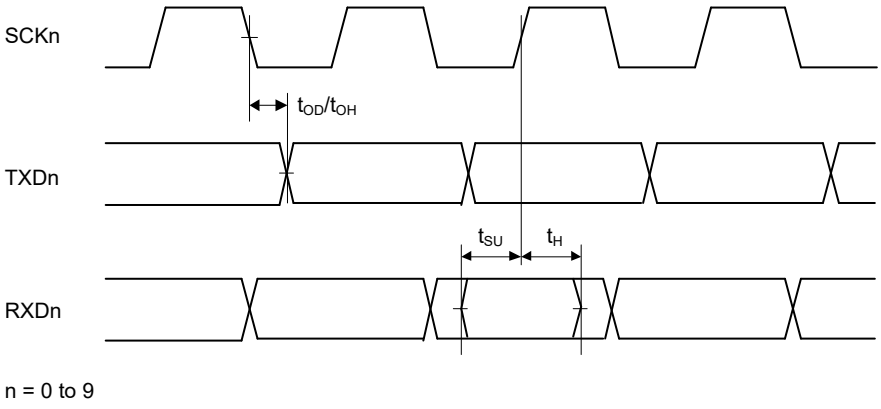


Figure 3.32 RSCI Input/Output Timing in Clock Synchronous Mode

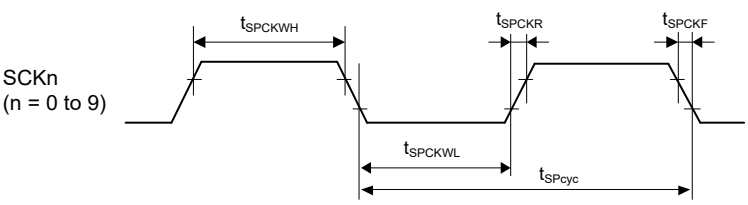


Figure 3.33 RSCI Simple SPI Mode Clock Timing

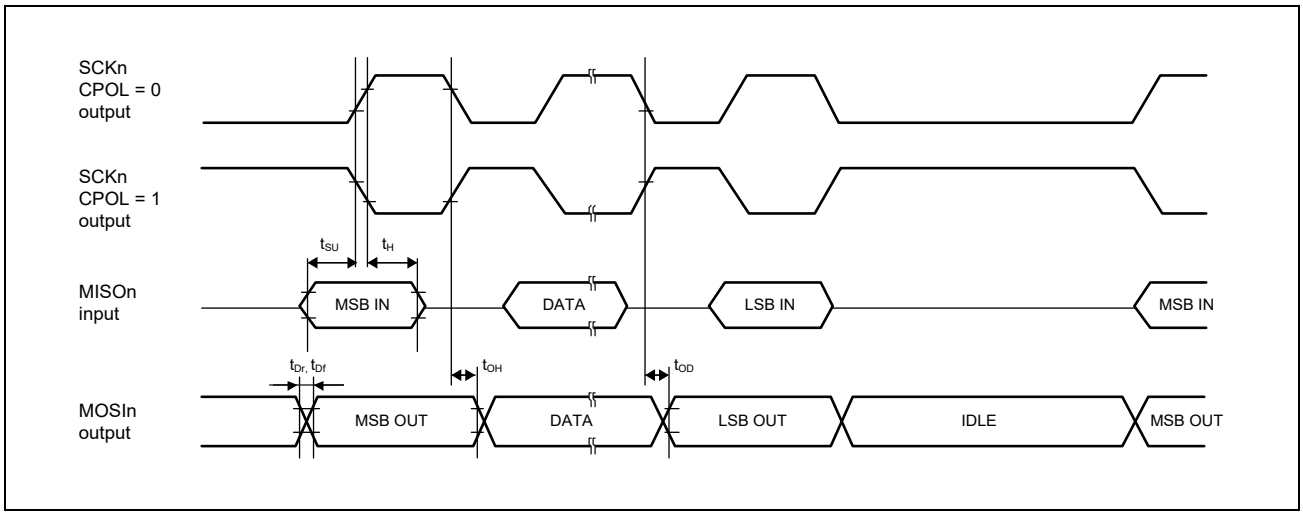


Figure 3.34 RSCI Simple SPI Mode Timing for Master when CPHA = 0

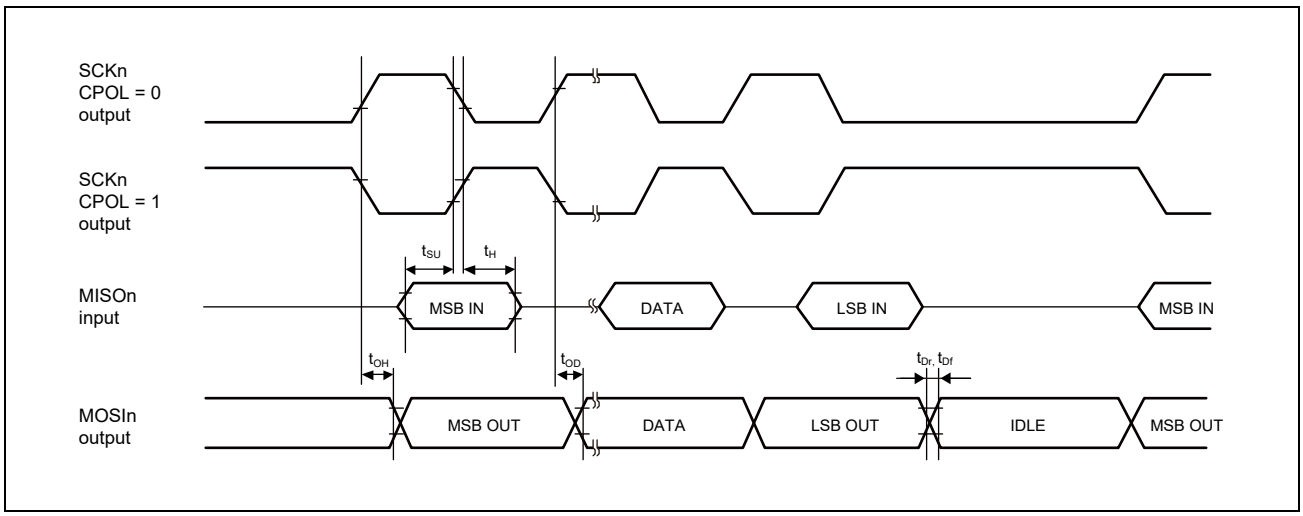


Figure 3.35 RSCI Simple SPI Mode Timing for Master when CPHA = 1

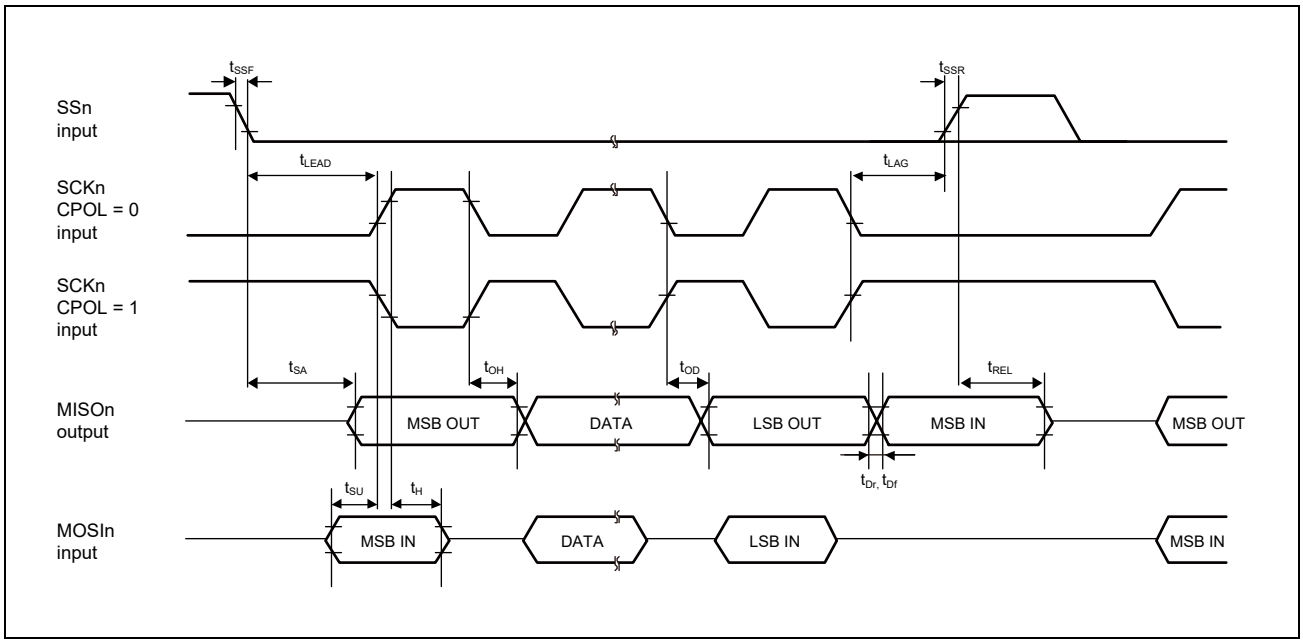


Figure 3.36 RSCI Simple SPI Mode Timing for Slave when CPHA = 0

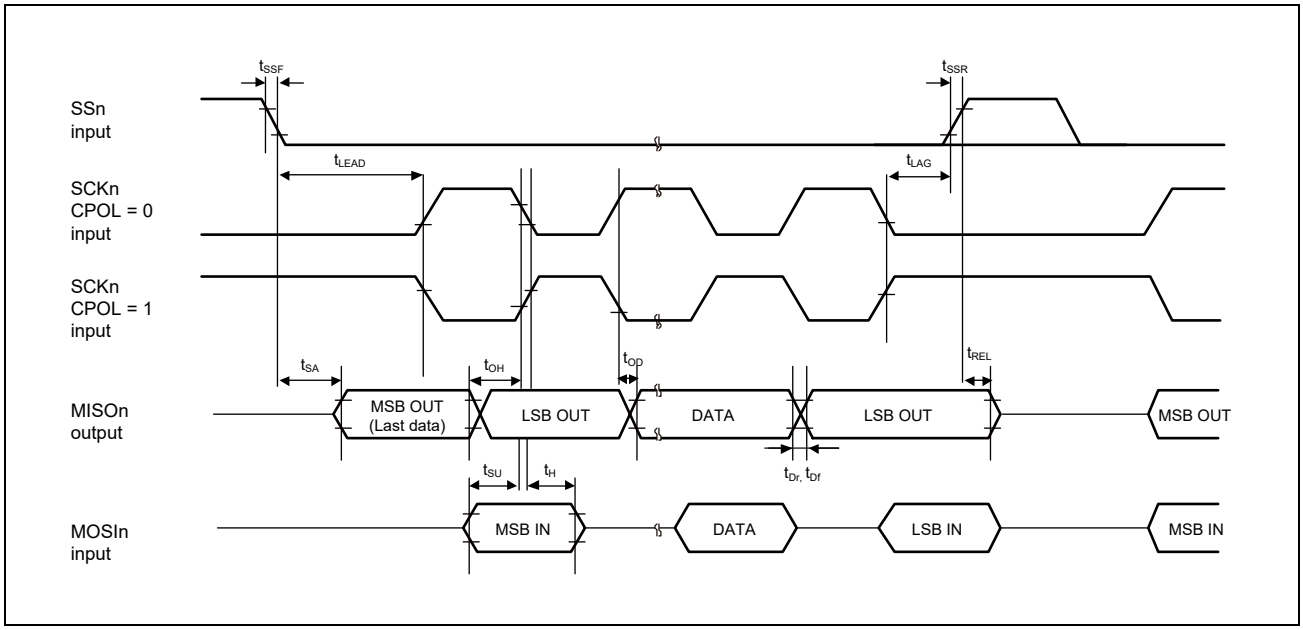


Figure 3.37 RSCI Simple SPI Mode Timing for Slave when CPHA = 1

3.5.15 Renesas Serial Peripheral Interface (RSPI) Access Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (3.3 V)

Drive strength: ×6

Table 3.20 RSPI Timing (1/2)

Parameter		Symbol	Min.*1	Max.*1	Unit	Figure
RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{SPIcyc}	**Figure 3.38**
	Slave		4 / 8*6	4096	t_{SPIcyc}	
RSPCK clock high-level pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock low-level pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	3*5	ns	
	Input		—	3*5	ns	
Data input setup time	Master	t_{SU}	5	—	ns	**Figure 3.39** to **Figure 3.45**
	Slave		3	—	ns	
Data input hold time	Master	t_H	3	—	ns	
	Slave		3	—	ns	
SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc} - 3$*2	$N \times t_{SPcyc} + 3$*2	ns	**Figure 3.39** to **Figure 3.42**
	Slave		5	—	t_{SPIcyc}	
SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc} - 3$*3	$N \times t_{SPcyc} + 3$*3	ns	
	Slave		5	—	t_{SPIcyc}	
Continuous transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{SPIcyc}$	$8 \times t_{SPcyc} + 2 \times t_{SPIcyc}$	ns	
	Slave		$t_{SPcyc} + 5 \times t_{SPIcyc}$	—	ns	
TI-SSP SS input setup time		t_{TISS}	3	—	ns	**Figure 3.43** to **Figure 3.45**
TI-SSP SS input hold time		t_{TISH}	3	—	ns	
TI-SSP next access time		t_{TIND}	M*4	—	t_{SPIcyc}	
TI-SSP Master SS output delay		t_{TISSOD}	−3	3	ns	
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns	
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns	
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	7.5 / 10*6	ns	
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	7.5 / 10*6	ns	
SSL Activation to Data Output Delay		t_{OD1}	—	3	ns	**Figure 3.39**
Data output delay time	Master	t_{OD}	—	3	ns	**Figure 3.39** to **Figure 3.45**
	Slave		—	7.5 / 10*6	ns	
Data output hold time	Master	t_{OH}	−3	—	ns	
	Slave		3	—	ns	
MOSI, MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	3*5	ns	
	Input		—	1	µs	
SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	3*5	ns	**Figure 3.39**, **Figure 3.40**
	Input		—	1	µs	

Table 3.20 RSPI Timing (2/2)

Parameter	Symbol	Min.*1	Max.*1	Unit	Figure
Slave access time	t_{SA}	—	8 / 10*6	ns	**Figure 3.41**, **Figure 3.42**
Slave output release time	t_{REL}	—	8 / 10*6	ns	

Note 1. t_{SPIcyc}: RSPI_n_TCLK cycle (n = 0 to 2)

Note 2. RSPIm_SPCKD.SCKDL[2:0] set value + 1 (1 to 8)

Note 3. RSPIm_SSLND.SLNDL[2:0] set value + 1 (1 to 8)

Note 4. RSPIm_SSLND.SLNDL[2:0] set value + 2 (2 to 9)

Note 5. Output transition time from 20% to 80%

Note 6. This value when PMx, P3x pins are used as RSPI (x = 0 to 7)

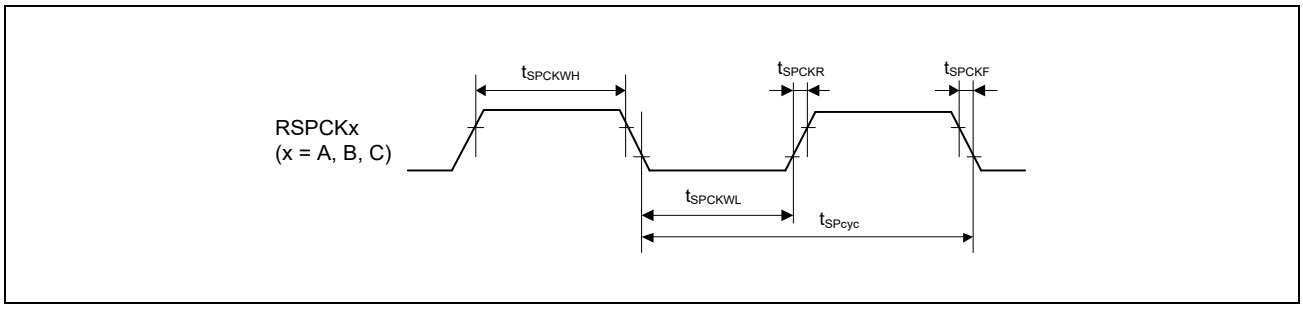


Figure 3.38 RSPI Clock Timing

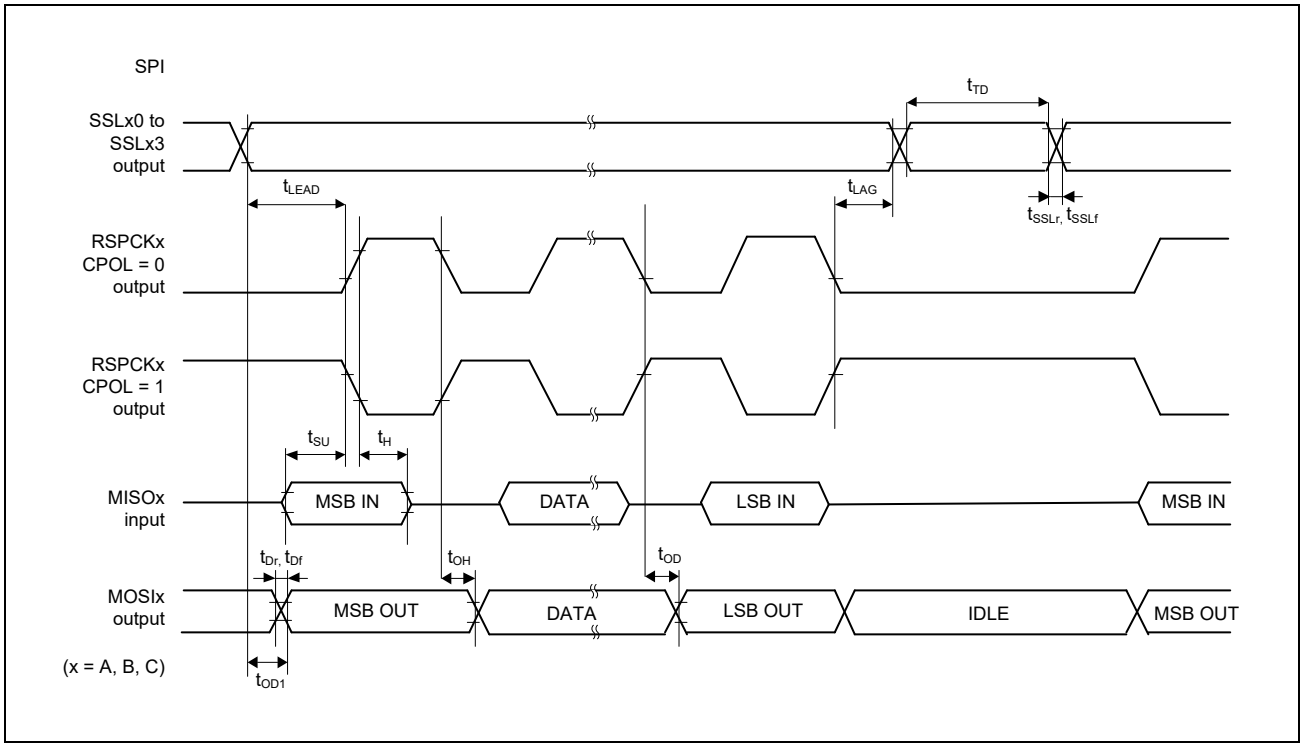


Figure 3.39 RSPI Timing (Master, Motorola RSPI, CPHA = 0)

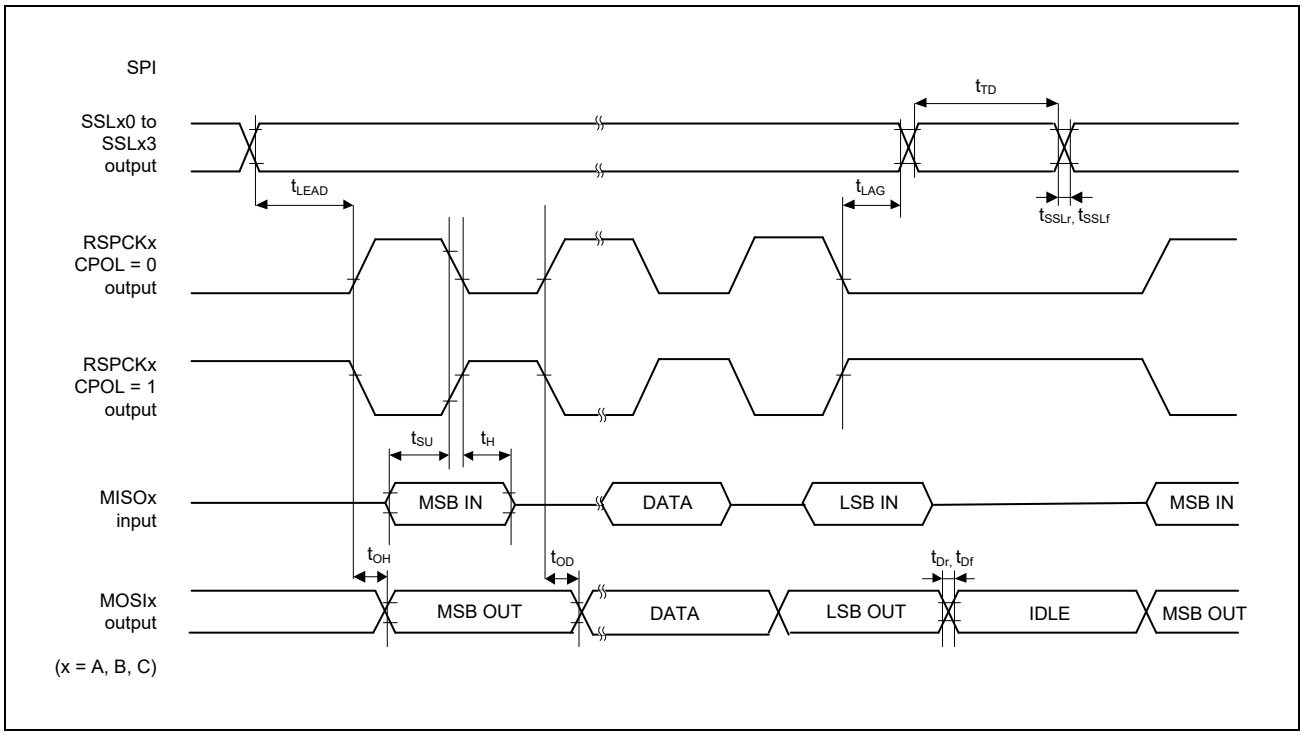


Figure 3.40 RSPI Timing (Master, Motorola RSPI, CPHA = 1)

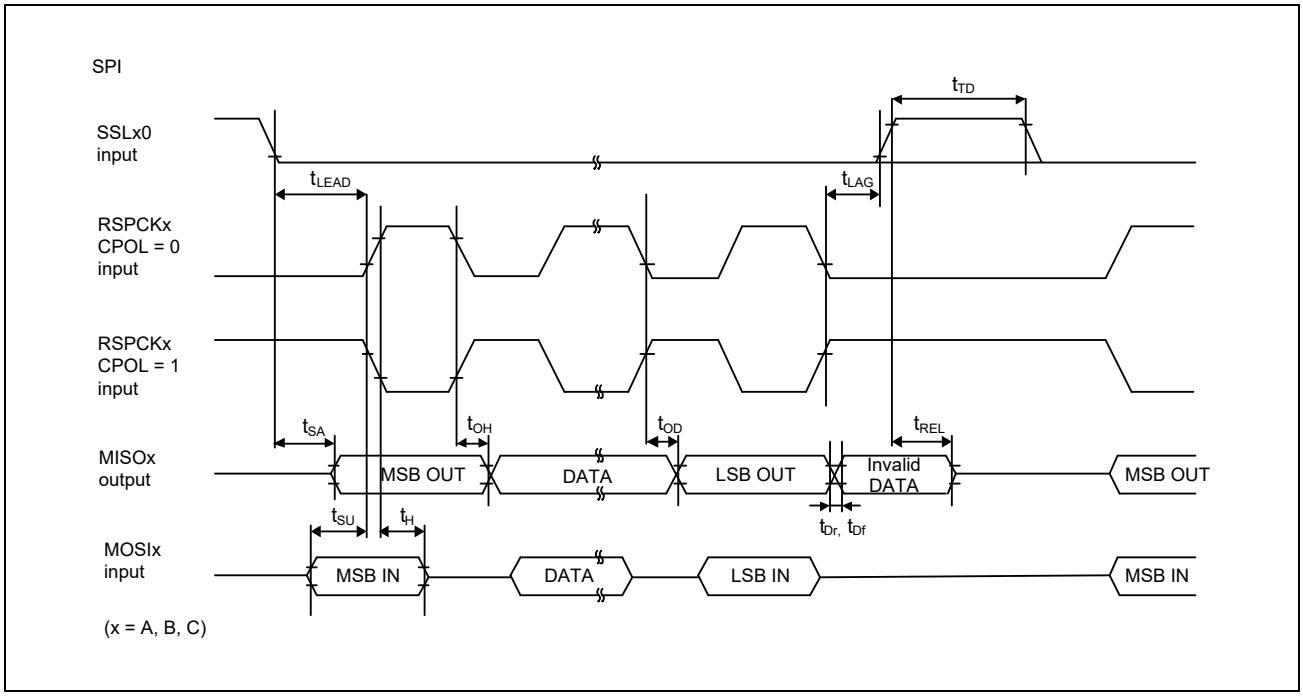


Figure 3.41 RSPI Timing (Slave, Motorola RSPI, CPHA = 0)

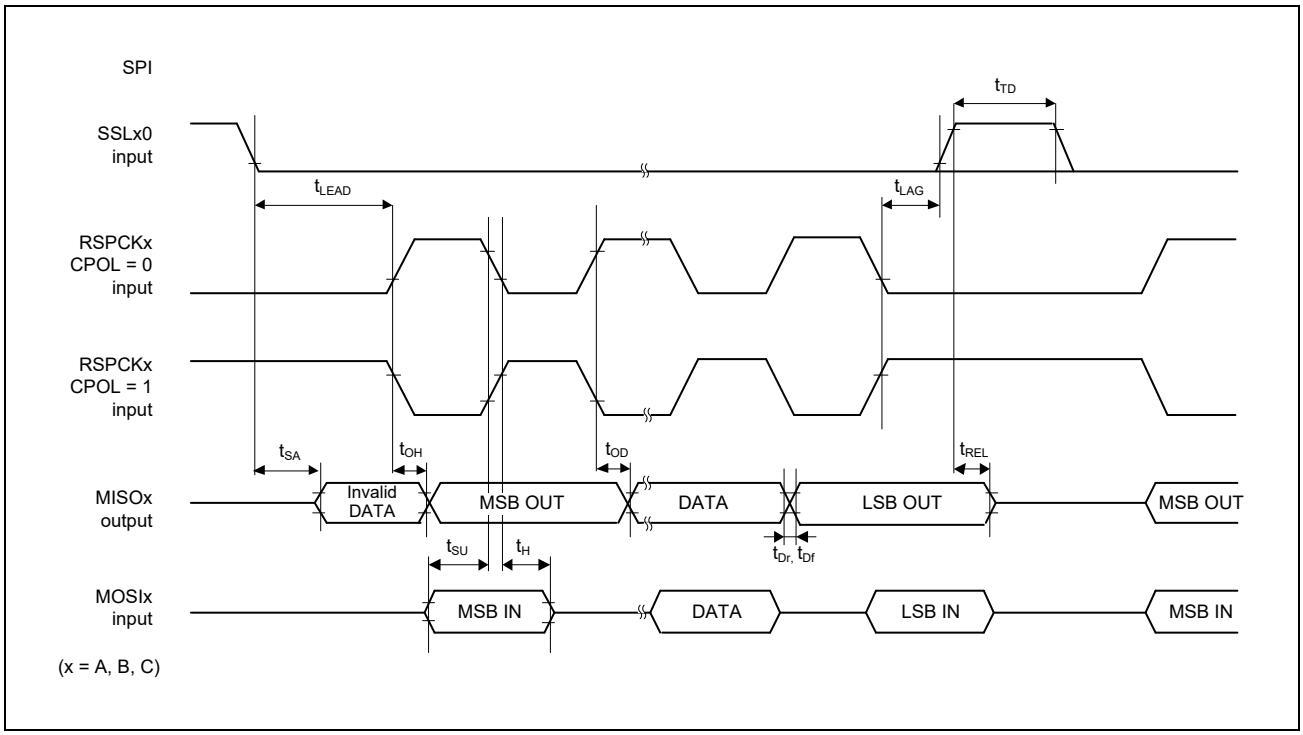


Figure 3.42 RSPI Timing (Slave, Motorola RSPI, CPHA = 1)

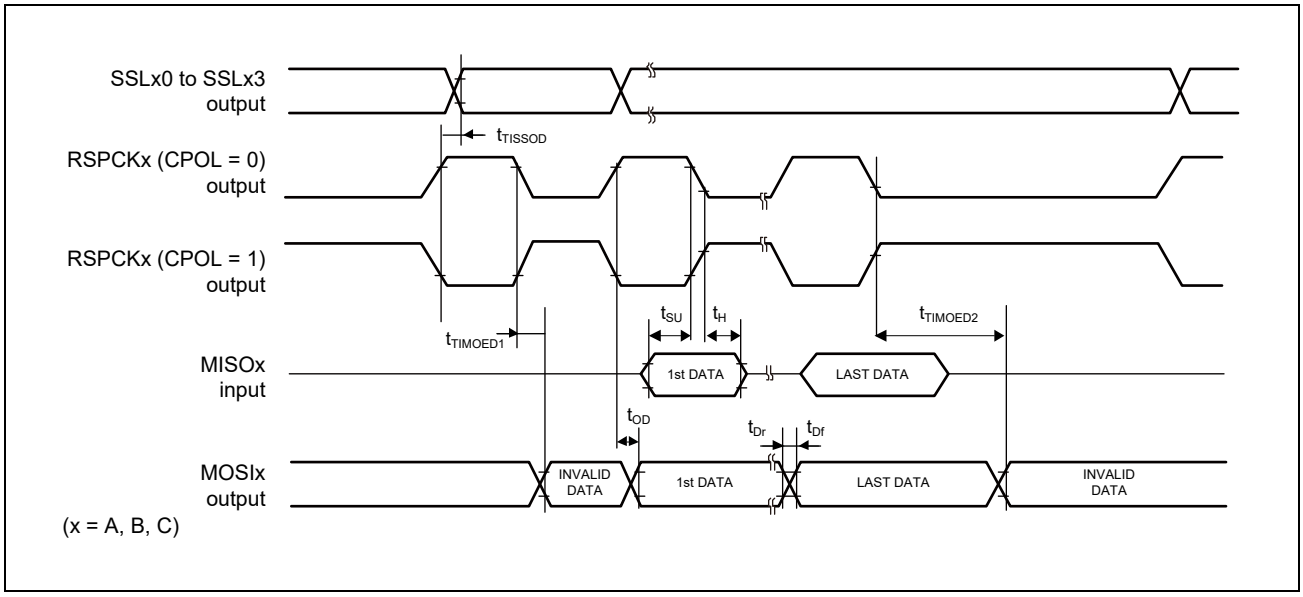


Figure 3.43 RSPI Timing (Master, TI SSP)

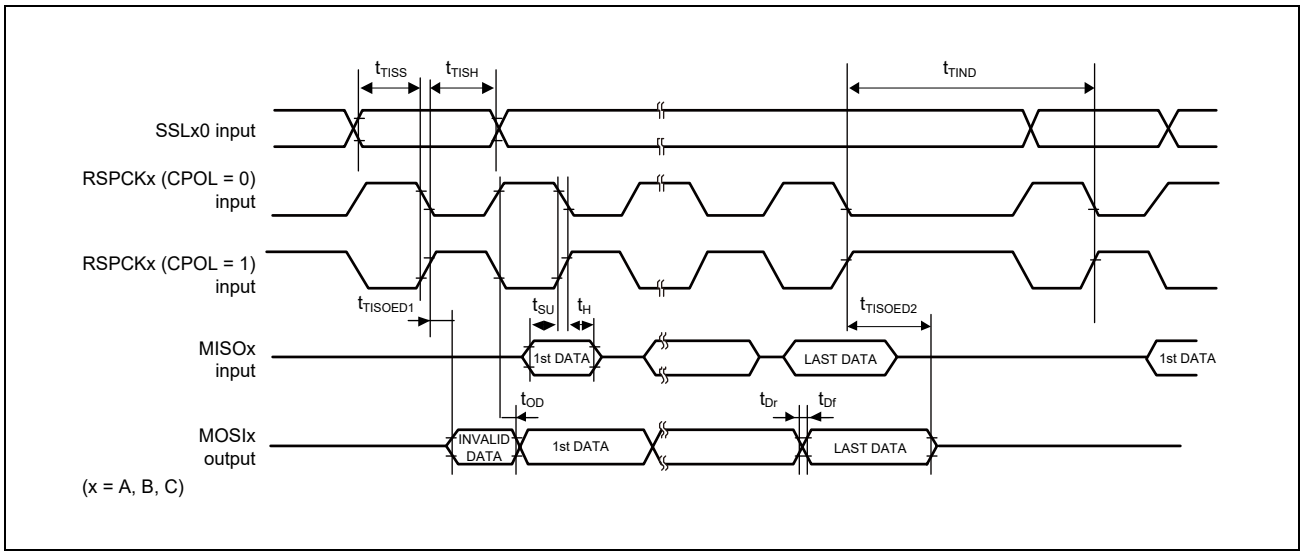


Figure 3.44 RSPI Timing (Slave, TI-SSP, with delay in burst transfer)

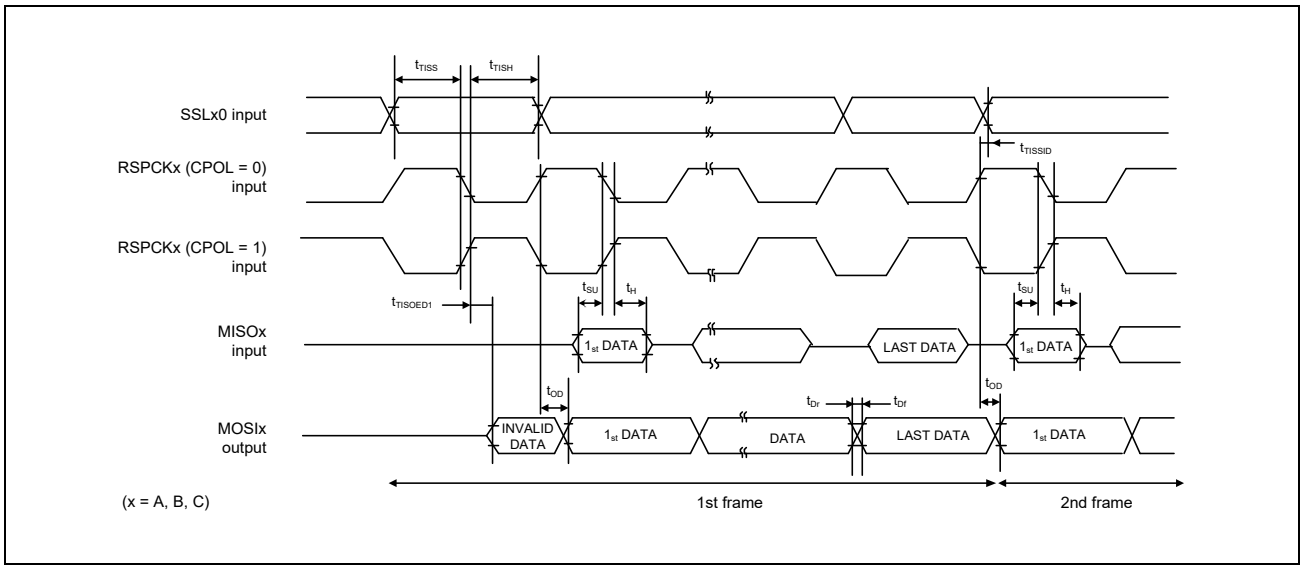


Figure 3.45 RSPI Timing (Slave, TI-SSP, without delay in burst transfer)

3.5.16 Renesas IIC Bus Interface (RIIC) Access Timing

Conditions: V_{OL} = 0.4 V

Drive strength: ×6

Table 3.21 RIIC Timing

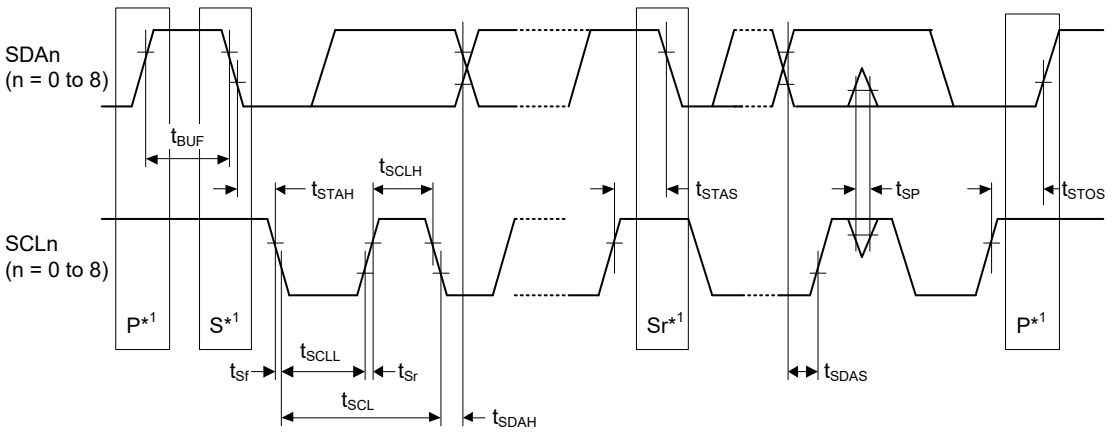
Parameter		Symbol	Min.*1,*2	Max.*1,*2	Unit	Figure
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	**Figure 3.46**
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low-level pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{sr}	—	1000	ns	
	SCL, SDA input fall time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	**Figure 3.46**
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low-level pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{sr}	—*4	300	ns	
	SCL, SDA input fall time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	
RIIC (Fast-mode Plus)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	**Figure 3.46**
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low-level pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rise time	t_{sr}	—*4	120	ns	
	SCL, SDA input fall time	t_{sf}	—*4	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	550	pF	

Note 1. t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle

Note 2. The values outside parentheses apply when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The values within parentheses apply when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.

Note 3. C_b is the total capacitance of the bus lines.

Note 4. The minimum values are not specified for t_{sr} and t_{sf} in Fast-mode or Fast-mode Plus.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 3.46 RIIC Bus Interface Input/Output Timing

3.5.17 I3C Timing

Conditions: V_{OH} = VDD1218_I3C × 0.5, V_{OL} = VDD1218_I3C × 0.5, C = 30 pF (1.2 V or 1.8 V)

Drive strength: ×6

Table 3.22 I3C Timing

Parameter		Symbol	Min.*1	Max.	Unit	Figure
IIC (Standard mode, SMBus)	SCL3n cycle time	t_{SCL}	4(36) × t_{IICcyc} + 4 × t_{Pcyc} + 1300	—	ns	**Figure 3.47**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 800	—	ns	
	SCL3n, SDA3n rise time	t_{Sr}	—	1000	ns	
	SCL3n, SDA3n fall time	t_{Sf}	—	300	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	0	1(16) × t_{IICcyc}	ns	
	SDA3n bus free time	t_{BUF}	3(20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	1000	—	ns	
	Setup time for STOP condition	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C_b	—	400	pF	
IIC (Fast mode)	SCL3n cycle time	t_{SCL}	4(36) × t_{IICcyc} + 4 × t_{Pcyc} + 600	—	ns	**Figure 3.47**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL3n, SDA3n rise time	t_{Sr}	—	300	ns	
	SCL3n, SDA3n fall time	t_{Sf}	—	300	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	0	1(16) × t_{IICcyc}	ns	
	SDA3n bus free time	t_{BUF}	3(20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	300	—	ns	
	Setup time for STOP condition	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: I3C internal reference clock (I3Cϕ) cycle, t_{Pcyc}: I3C_0_TCLK cycle. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with DNFE.DNFE set to 1b.

Table 3.23 IIC Timing (Fast-mode+)

Parameter		Symbol	Min.*1	Max.	Unit	Figure
IIC (Fast-mode+)	SCL3n cycle time	t_{SCL}	4(26) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	ns	**Figure 3.47**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n, SDA3n rise time	t_{Sr}	—	120	ns	
	SCL3n, SDA3n fall time	t_{Sf}	—	120	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	—	1(16) × t_{IICcyc}	ns	
	SDA3n bus free time	t_{BUF}	3(20) × t_{IICcyc} + 120	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	260	—	ns	
	Setup time for STOP condition	t_{STOS}	260	—	ns	
	Data setup time	t_{SDAS}	50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C_b	—	550	pF	

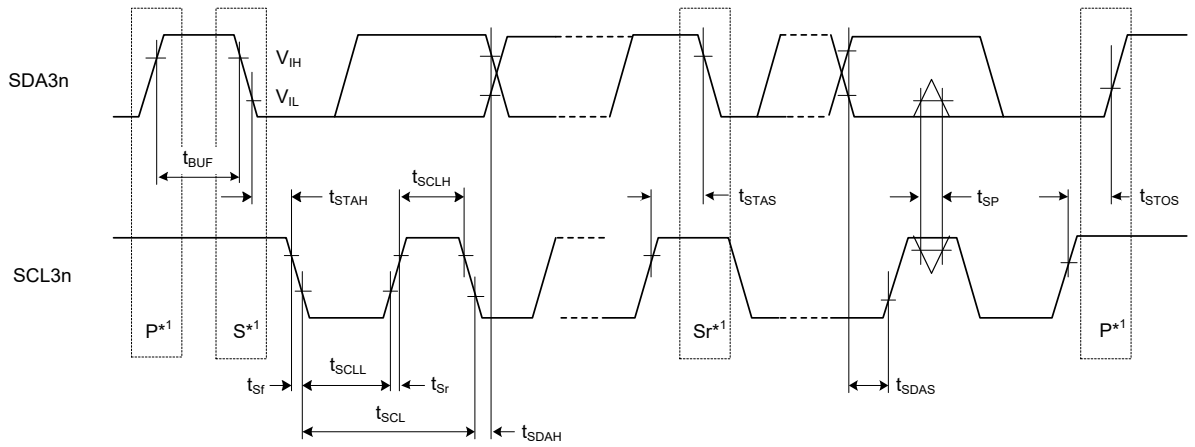
Note 1. t_{IICcyc}: I3C internal reference clock (I3Cϕ) cycle, t_{Pcyc}: I3C_0_TCLK cycle. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1b.

Table 3.24 IIC Timing (HS mode)

Parameter		Symbol	Cb = 100 pF		Cb = 400 pF		Unit	Figure
			Min.*1	Max.	Min.*1	Max.		
IIC (HS mode)	SCL3n cycle time	t_{SCL}	3(36) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	3(36) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	ns	**Figure 3.47**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n rise time	t_{Sr}	—	40	—	80	ns	
	SCL3n rise time after a repeated START condition and after an acknowledge bit	t_{Sr}	—	80	—	160	ns	
	SDA3n rise time	t_{Sr}	—	80	—	160	ns	
	SCL3n fall time	t_{Sf}	—	40	—	80	ns	
	SDA3n fall time	t_{Sf}	—	80	—	160	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	0	1(16) × t_{IICcyc}	0	1(16) × t_{IICcyc}	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	160	—	160	—	ns	
	Setup time for STOP condition	t_{STOS}	160	—	160	—	ns	
	Data setup time	t_{SDAS}	10	—	10	—	ns	
	Data hold time	t_{SDAH}	0	80	0	150	ns	
	SCL3n, SDA3n capacitive load	C_b	—	100	—	400	pF	

Note 1. t_{IICcyc}: I3C internal reference clock (I3Cϕ) cycle, t_{Pcyc}: I3C_0_TCLK cycle. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1b

Note 2. The maximum SCL clock frequency is 1.7 MHz.



Note: n = 0

Note 1. S, P, and Sr indicate the following conditions
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 3.47 I3C Bus Interface Input/Output Timing

Table 3.25 I3C Timing (Open Drain Timing Parameters)

Parameter		Symbol	Min.*1	Max.	Unit	Figure	Notes
SCL3n clock Low period		t_{LOW_OD}	200	—	ns	**Figure 3.50**	1, 2
		$t_{DIG\_OD\_L}$	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	**Figure 3.50**	—
SCL3n clock High period		t_{HIGH}	—	41	ns	**Figure 3.50**	3, 4
		t_{DIG_H}	36 (when 1.8 V) 40 (when 1.2 V)	t_{HIGH} + t_{CF}	ns	**Figure 3.50**	
SDA3n signal fall time		t_{fDA_OD}	t_{CF}	33	ns	**Figure 3.50**	—
SDA3n data setup time open drain mode	V_{DD1218} = 1.8 V	t_{SU_OD}	12	—	ns	**Figure 3.49**, **Figure 3.50**	1
	V_{DD1218} = 1.2 V		13.9	—	ns		
Clock after START (S) condition		t_{CAS}	38.4	For ENTAS0: 1 µ	seconds	**Figure 3.50**	5, 6
				For ENTAS1: 100 µ			
				For ENTAS2: 2 m			
				For ENTAS3: 50 m			
Clock before STOP (P) condition		t_{CBP}	t_{CASmin}/2	—	seconds	**Figure 3.51**	—
Current master to secondary master overlap time during handoff		$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	**Figure 3.56**	—
Bus available condition		t_{AVAL}	1	—	µs	—	7
Bus idle condition		t_{IDLE}	1	—	ms	—	—
Time internal where new master not driving SDA3n low		t_{MMLock}	$t_{AVALmin}$	—	µs	**Figure 3.56**	—

Note 1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_ODmin}.

Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH.

Note 3. This is based on t_{SPIKE}, rise and fall times, and interconnect.

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short bus).

Note 5. On a Legacy Bus where I^2C Devices need to see Start.

Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3

Note 7. On a Mixed Bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 3.26 I3C Timing (Push-Pull Timing Parameters for SDR)

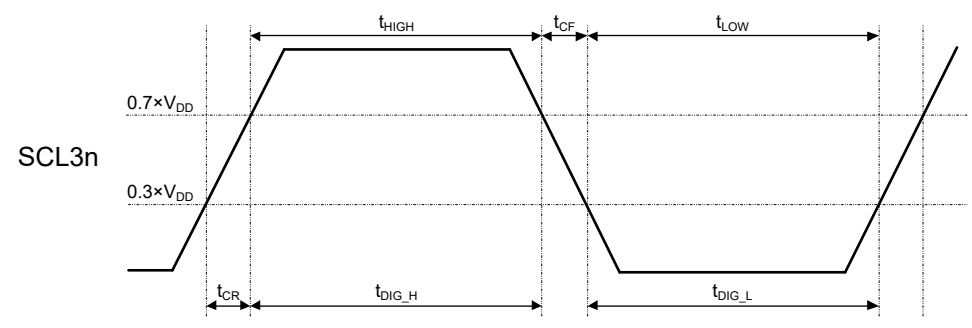
Parameter		Symbol	Min.*1	Max.	Unit	Figure	Notes
SCL3n clock frequency	V_{DD1218} = 1.8 V	t_{SCL}	0.01	12.5	MHz	—	1
	V_{DD1218} = 1.2 V		0.01	12.39	MHz	—	
SCL3n clock Low period		t_{LOW}	24	—	ns	**Figure 3.48**	—
		t_{DIG_L}	32	—	ns	**Figure 3.48**	2, 4
SCL3n clock High period for Mixed Bus		t_{HIGH}	24	—	ns	**Figure 3.48**	—
		t_{DIG_H}	32	45	ns	**Figure 3.48**	2, 3
SCL3n clock High period		t_{HIGH}	24	—	ns	**Figure 3.48**	—
		t_{DIG_H}	32	45	ns	**Figure 3.48**	2
Clock in to data out for a slave	V_{DD1218} = 1.8 V	t_{SCO}	—	12	ns	**Figure 3.53**	—
	V_{DD1218} = 1.2 V		—	12.7	ns		
SCL3n clock rise time		t_{CR}	—	150 × 1/f_{SCL} (capped at 60)	ns	**Figure 3.48**	—
SCL3n clock fall time		t_{CF}	—	150 × 1/f_{SCL} (capped at 60)	ns	**Figure 3.48**	—
SDA3n signal data hold in push-pull mode	Master	t_{HD_PP}	t_{CR} + 3 and t_{CF} + 3	—	—	**Figure 3.52**	4
	Slave		0	—	—	**Figure 3.54**	—
SDA3n signal data setup in push-pull mode	V_{DD1218} = 1.8 V	t_{SU_PP}	12	N/A	ns	**Figure 3.52**, **Figure 3.53**, **Figure 3.54**	—
	V_{DD1218} = 1.2 V		13.9	N/A	ns		
Clock after repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns	**Figure 3.55**	—
Clock before repeated START (Sr)		t_{CBSr}	t_{CASmin}/2	N/A	ns	**Figure 3.55**	—
Capacitive load per bus line (SDA3n / SCL3n)		C_b	—	50	pF	—	—

Note 1. FSCL = 1/(t_{DIG_L} + t_{DIG_H})

Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see **Figure 3.48**)

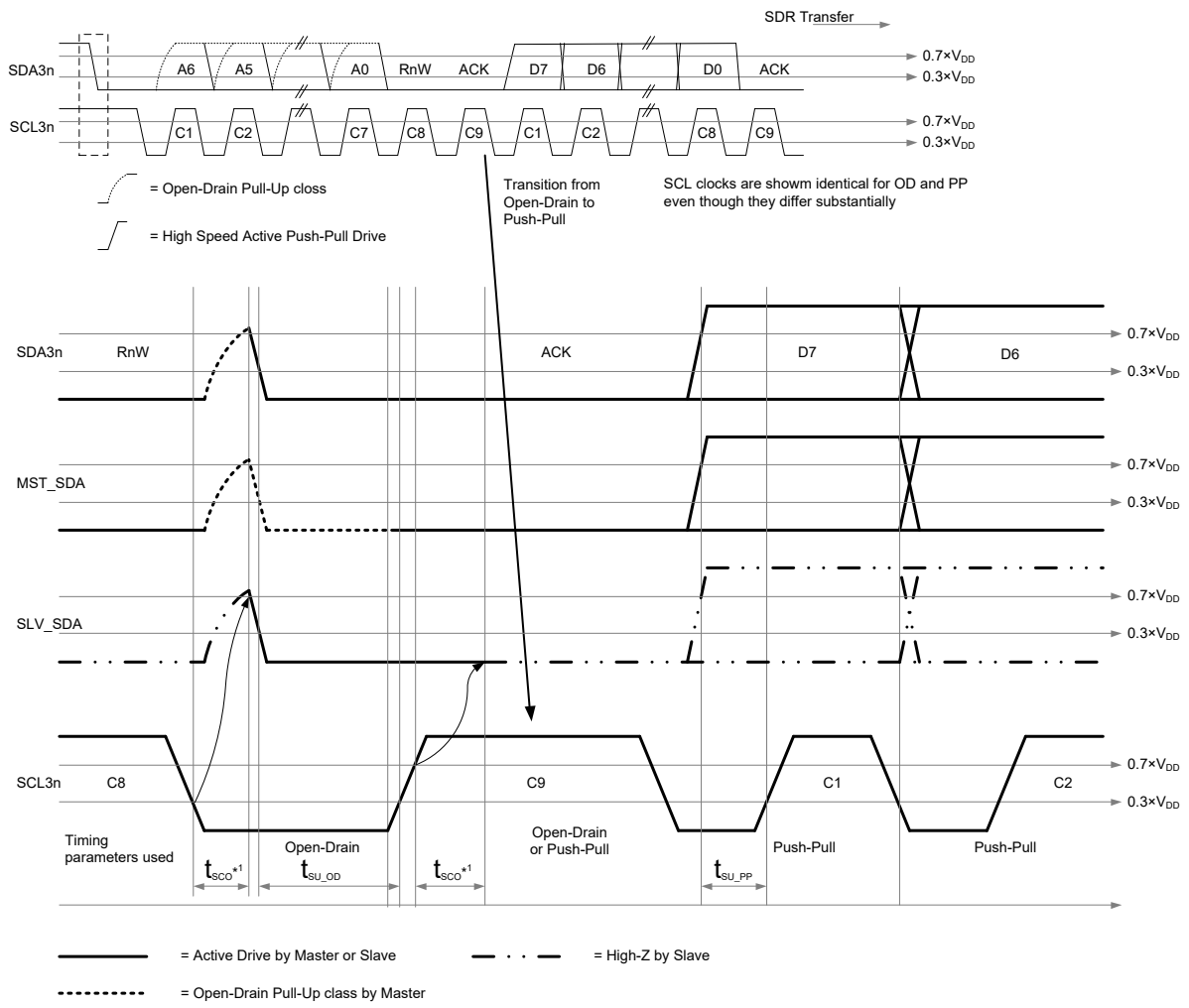
Note 3. When communicating with an I3C Device on a mixed bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.

Note 4. As both edges are used, the hold time must be satisfied for the respective edges, for example, t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.



Note: V_{DD}: VDD1218_I3C

Figure 3.48 t_{DIG_H} and t_{DIG_L}

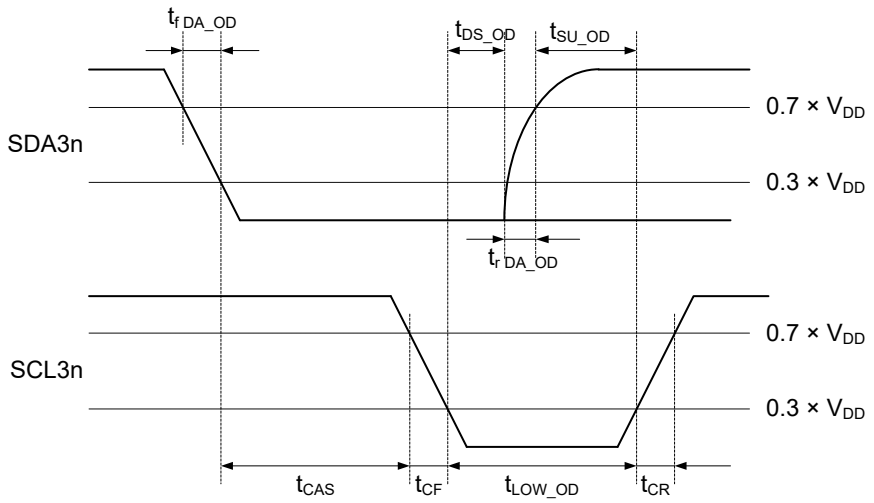


Note: V_{DD}: VDD1218_I3C

Note: Open-Drain: Master releases SDA after a suitable delay from SCL edges
Push-Pull: Master drives SDA after a suitable delay from SCL edges

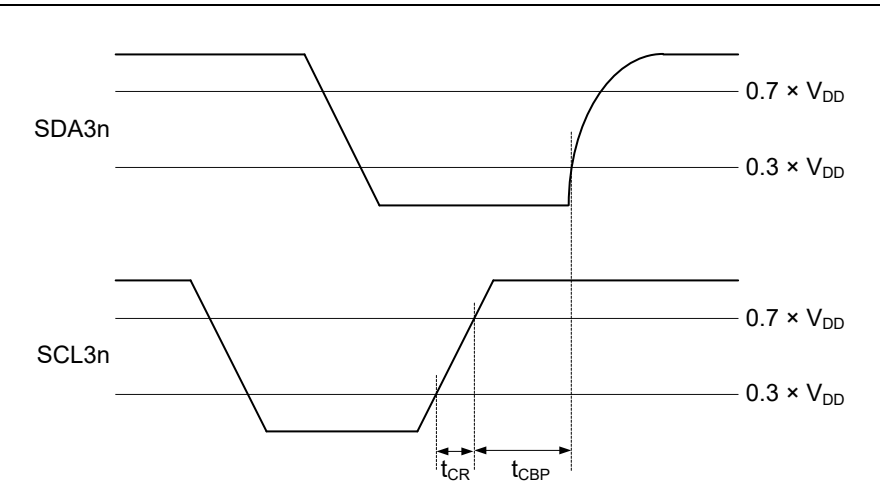
Note 1. t_{SCO} is depicted for informative purposes only

Figure 3.49 I3C Data Transfer – ACK by Slave



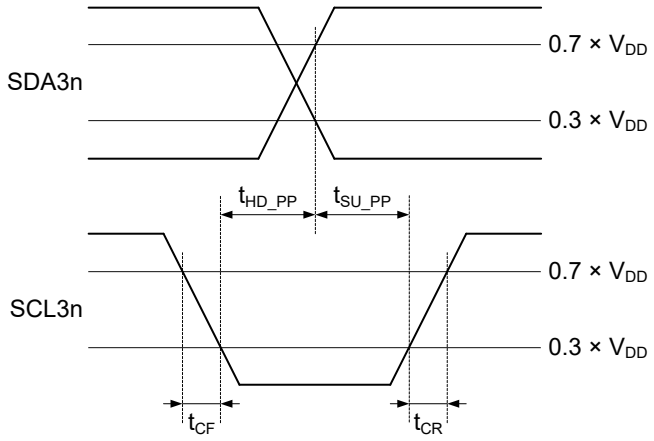
Note: V_{DD}: VDD1218_I3C

Figure 3.50 I3C START Condition Timing



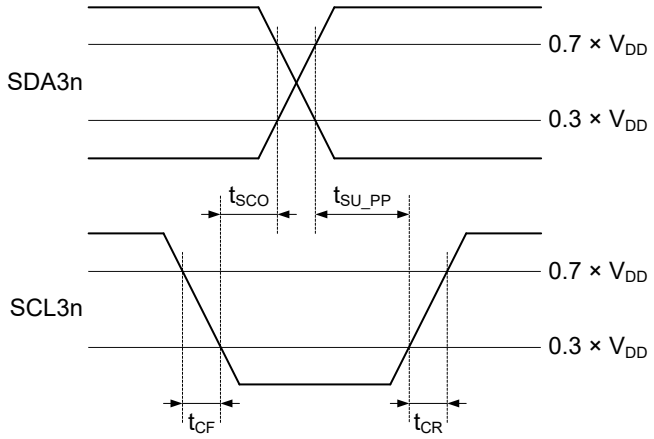
Note: V_{DD}: VDD1218_I3C

Figure 3.51 I3C STOP Condition Timing



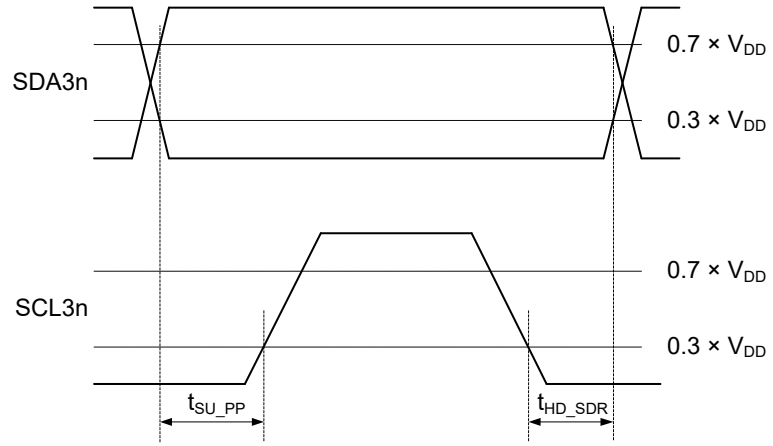
Note: V_{DD}: VDD1218_I3C

Figure 3.52 I3C Master Out Timing



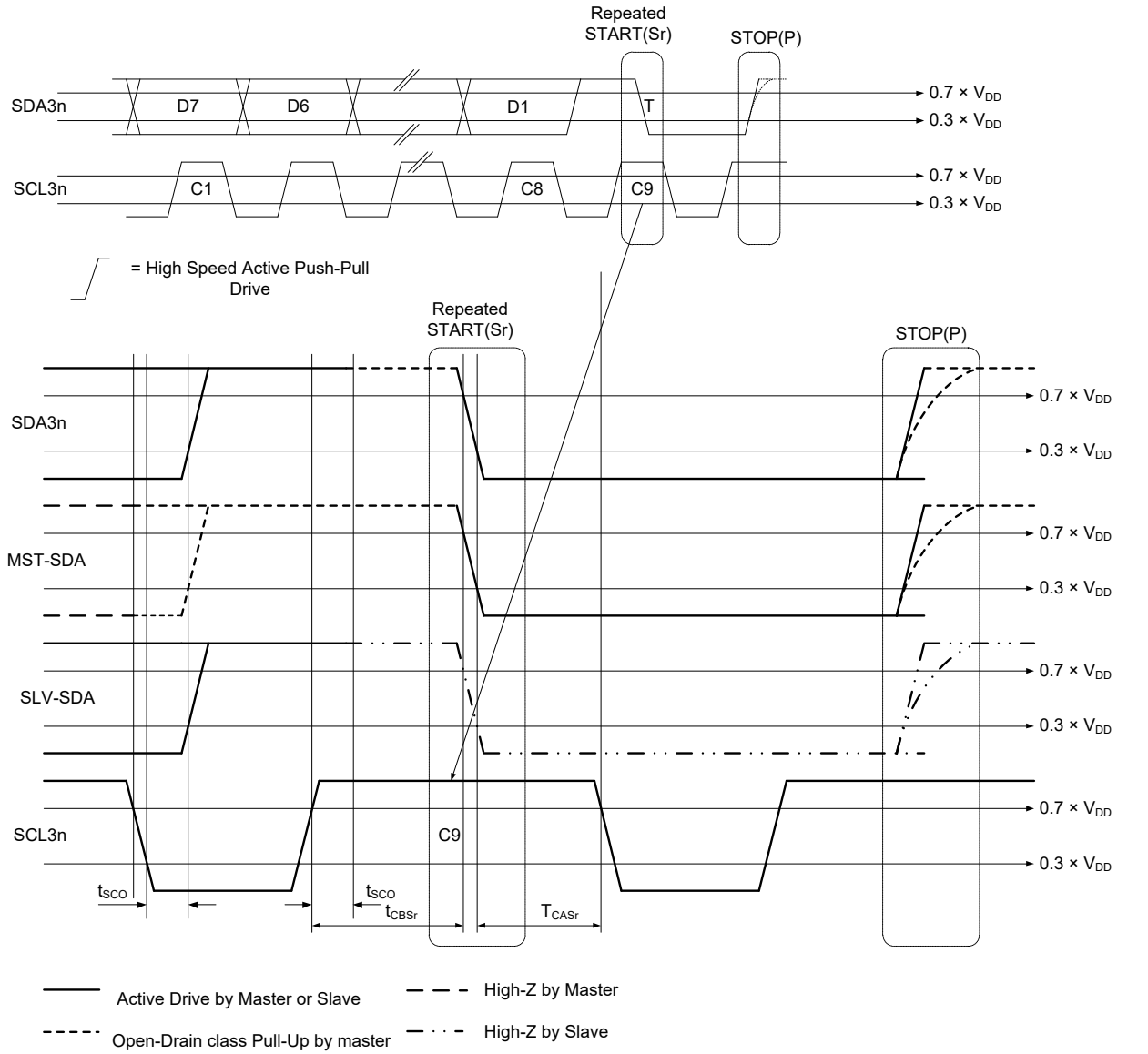
Note: V_{DD}: VDD1218_I3C

Figure 3.53 I3C Slave Out Timing



Note: V_{DD}: VDD1218_I3C

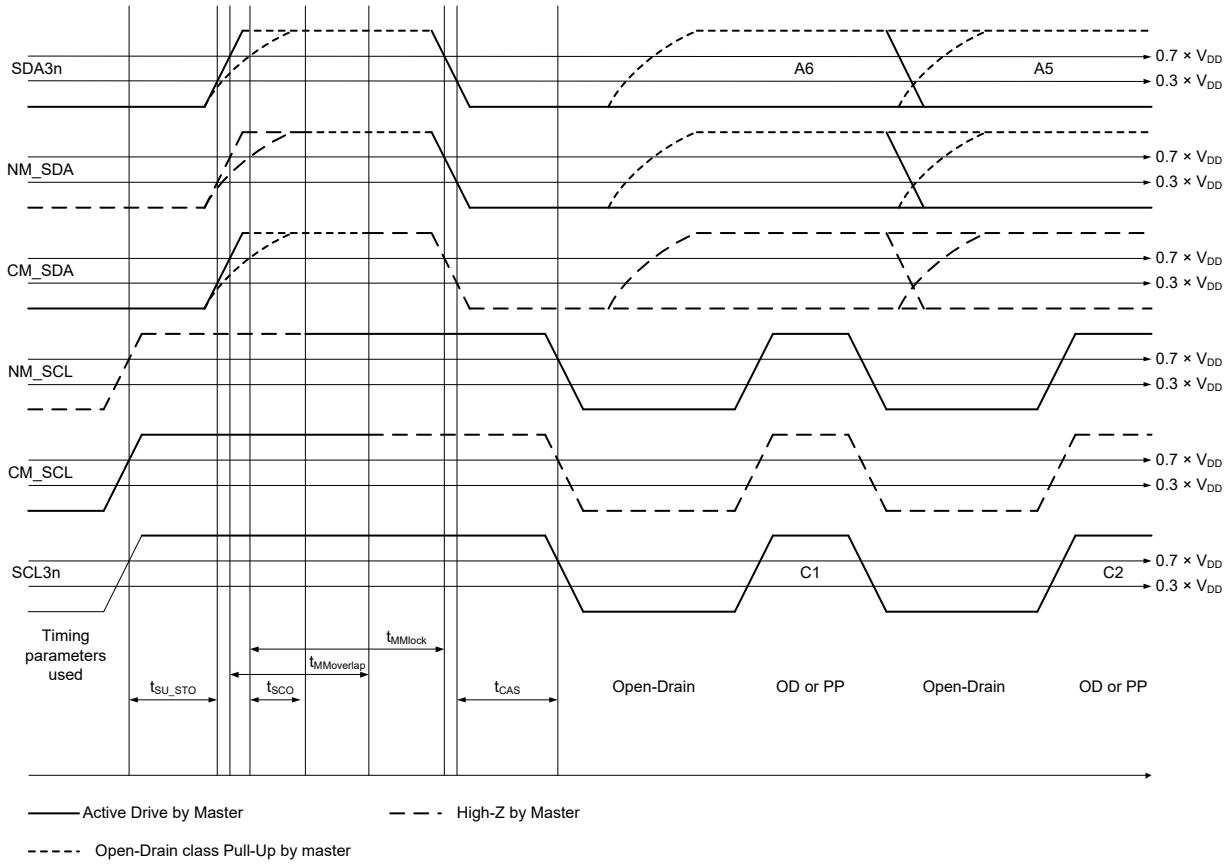
Figure 3.54 Master SDR Timing



Note: V_{DD}: VDD1218_I3C

Note: Sr immediately followed by P is illegal for I^2C Devices; however, many devices are not adversely affected by it.The condition is not illegal for I3C Devices.

Figure 3.55 T-Bit When Master Ends Read with Repeated START and STOP



Note: V_{DD}: VDD1218_I3C

Note: Master releases or drives SDA after a suitable delay from SCL edges

Figure 3.56 I3C Timing

3.5.18 CANFD Interface Access Timing

Table 3.27 CANFD Interface Timing

Parameter		Symbol	CAN		CANFD		Unit	Figures
			Min.	Max.	Min.	Max.		
CANFD	Internal delay time	t_{node}	—	100	—	50	ns	**Figure 3.57**
	Transmission rate	—	—	1	—	8	Mbps	

Note 1. Internal delay time (t_{node}) = Internal transmission delay time (t_{output}) + Internal reception delay time (t_{input})

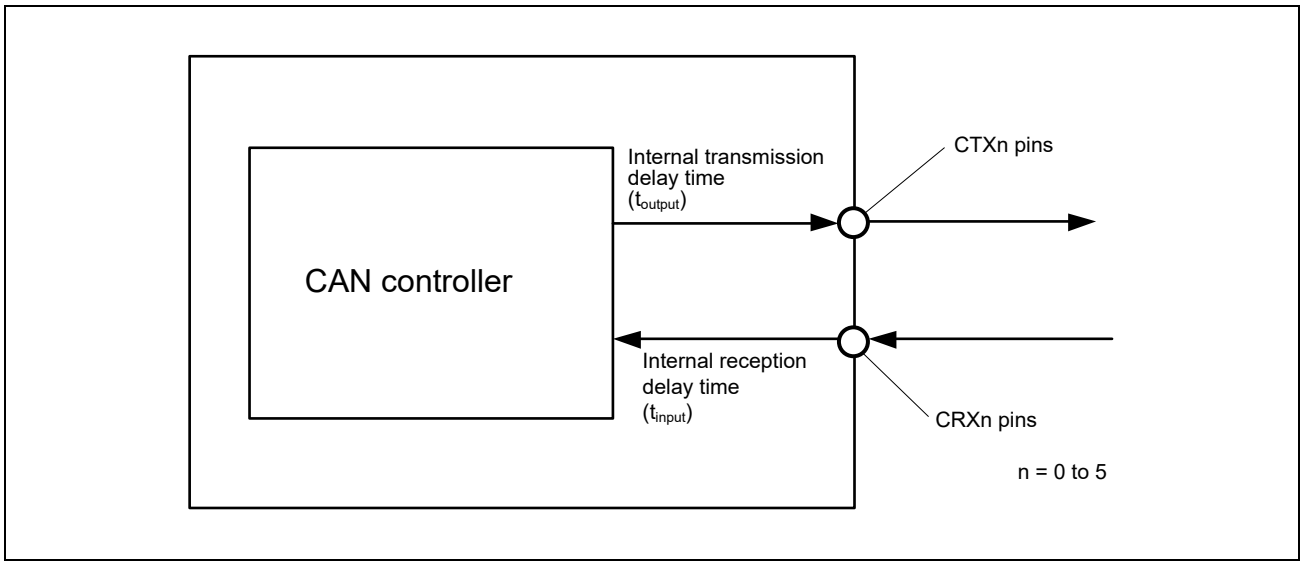


Figure 3.57 CANFD Interface Condition

3.5.19 A/D Converter Access Timing

Table 3.28 A/D Converter Trigger Timing

Parameter			Symbol	Min.	Max.	Unit*1	Figure
A/D converter	A/D converter trigger input pulse width	ADTRG	t_{TRGW}	1.5	—	$t_{PADCcyc}$	**Figure 3.58**

Note 1. $t_{PADCcyc}$: ADC_0_PCLK cycle

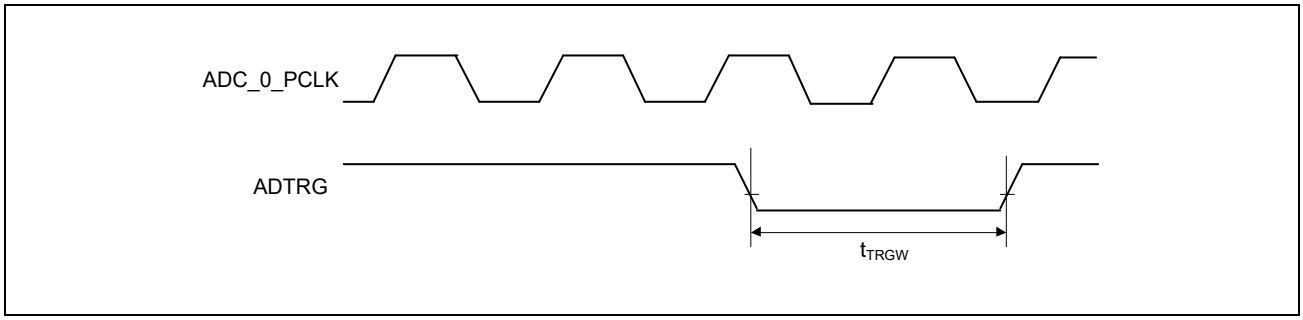


Figure 3.58 A/D Converter Trigger Input Timing (ADTRG)

3.5.20 SSIU Timing

Condition:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF*1 (1.8 V)
V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF*1 (3.3 V)

Drive strength: ×1, ×2, ×4, ×6

Note 1. Other than t_{RC}: Rise-edge clock timing

Table 3.29 SSIU Signal Timing

Parameter	Symbol	Min.	Max.	Unit	Note	Figure
Output clock cycle	t_O	80	15625	ns	—	**Figure 3.59**
Input clock cycle	t_I	80	15625	ns	—	
Output clock high-cycle	t_{HC}	35*1	—	ns	—	
Output clock low-cycle	t_{LC}	35*1	—	ns	—	
Input clock high-cycle	t_{HC}	35	—	ns	—	
Input clock low-cycle	t_{LC}	35	—	ns	—	
Rise-edge clock timing	t_{RC}	—	20*2	ns	Output (100 pF)	
Output delay	t_D	-5	19	ns	—	**Figure 3.60** to **Figure 3.63**
Setup time	t_S	15	—	ns	—	
Hold time	t_H	5	—	ns	—	

Note 1. The width at high or low level of the clock signal when the input on AUDIO_CLKA, AUDIO_CLKB, or AUDIO_CLKC is output from SCK without frequency division in master mode is min. 30 ns.
The relevant registers are as follows:
ADG: Audio Clock Select Register m (AUDIO_CLK_SELm (m = 0 to 2))
SSIU: Control Register (SSICRn (n = 0 to 9))

Note 2. Output transition time from 20% to 80%

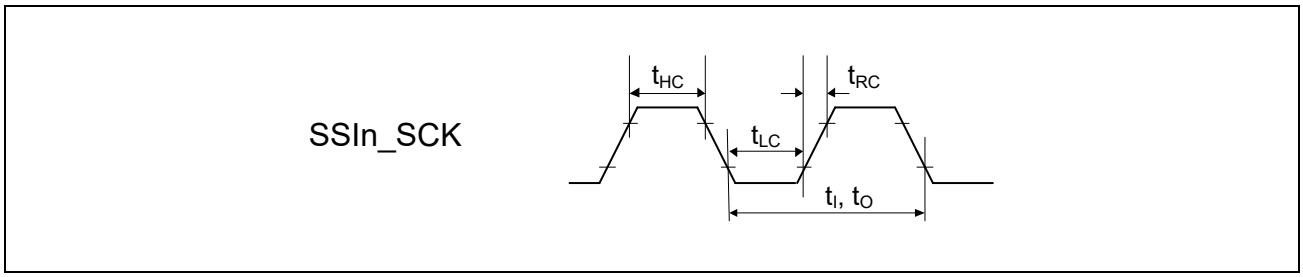


Figure 3.59 SCK Clock Input/Output Timing

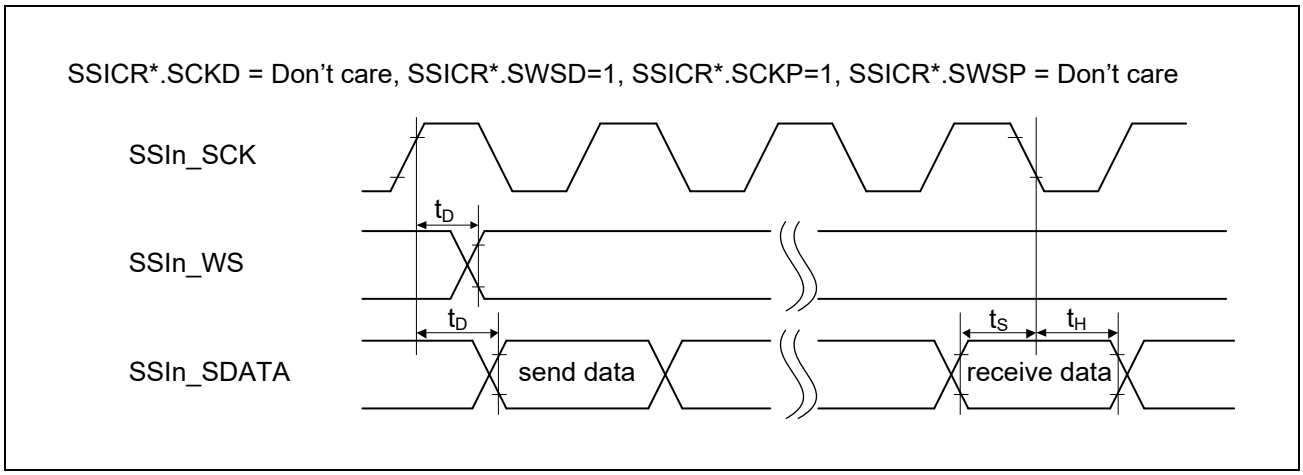


Figure 3.60 SSI Timing (1)

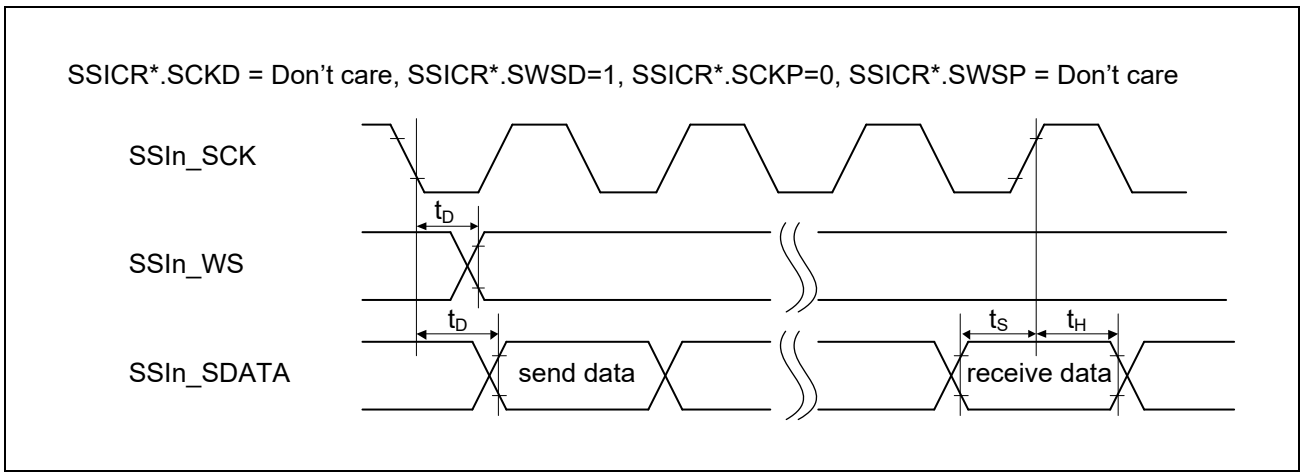


Figure 3.61 SSI Timing (2)

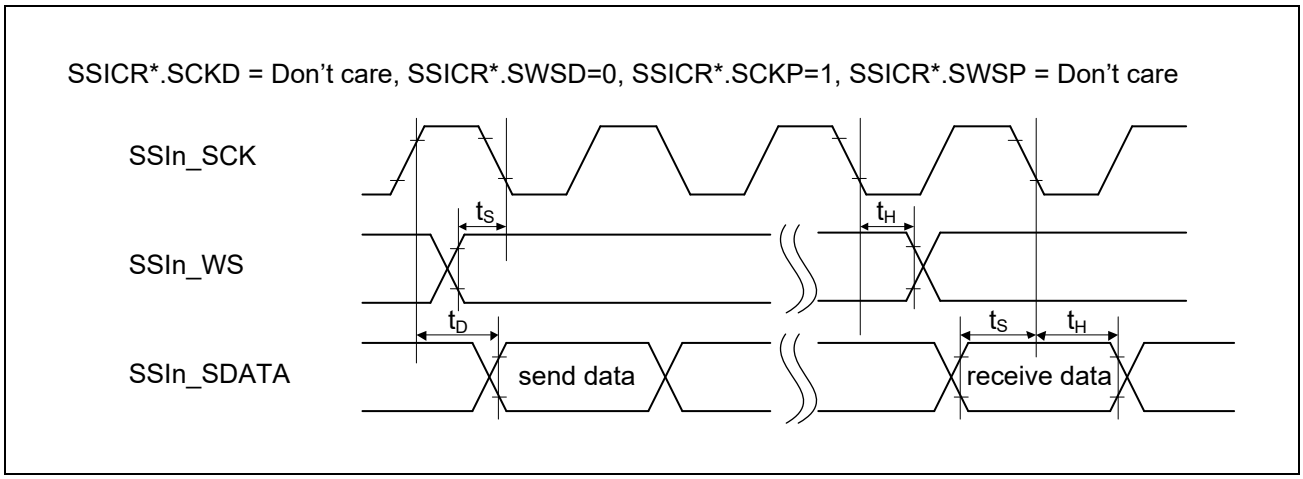


Figure 3.62 SSI Timing (3)

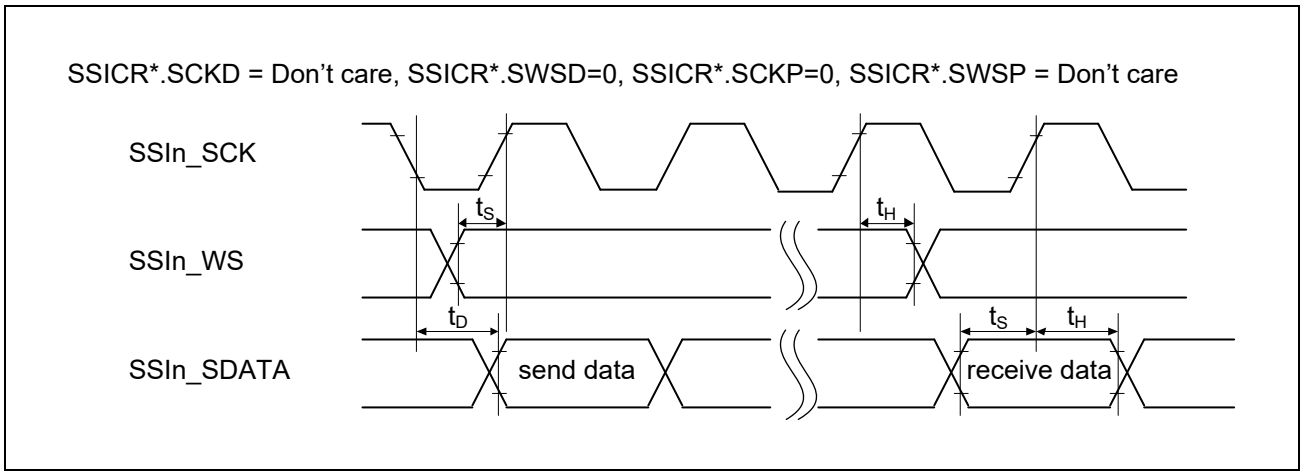


Figure 3.63 SSI Timing (4)

3.5.21 PDM Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (3.3 V)

Drive strength: ×1, ×2, ×4, ×6

Table 3.30 PDM Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Figure
Clock period	t_{PSYNC}	2	32	t_{CCcyc} = 208.33 ns (4.8 MHz)*1	**Figure 3.64**
Clock high-level period	t_{PDCKWH}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	
Clock low-level period	t_{PDCKWL}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	
Clock rise time	t_{R-EDGE}	—	3*2	ns	
Clock fall time	t_{F-EDGE}	—	3*2	ns	
Setup time	t_{su}	15	—	ns	**Figure 3.65**, **Figure 3.66**
Hold time	t_h	0	—	ns	

Note 1. t_{CCcyc} is the period of PDM_n_CCLK (n = 0, 1).

Note 2. Output transition time from 20% to 80%

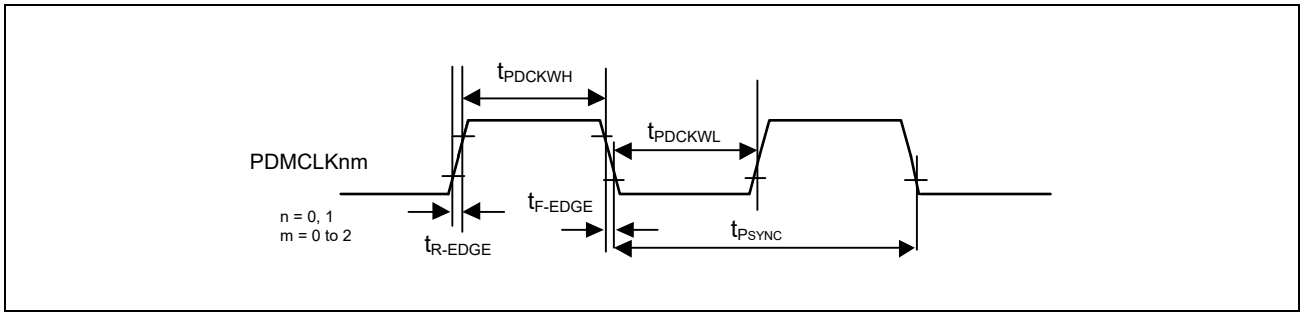


Figure 3.64 Timing of Clock Output (PDMCLKnm)

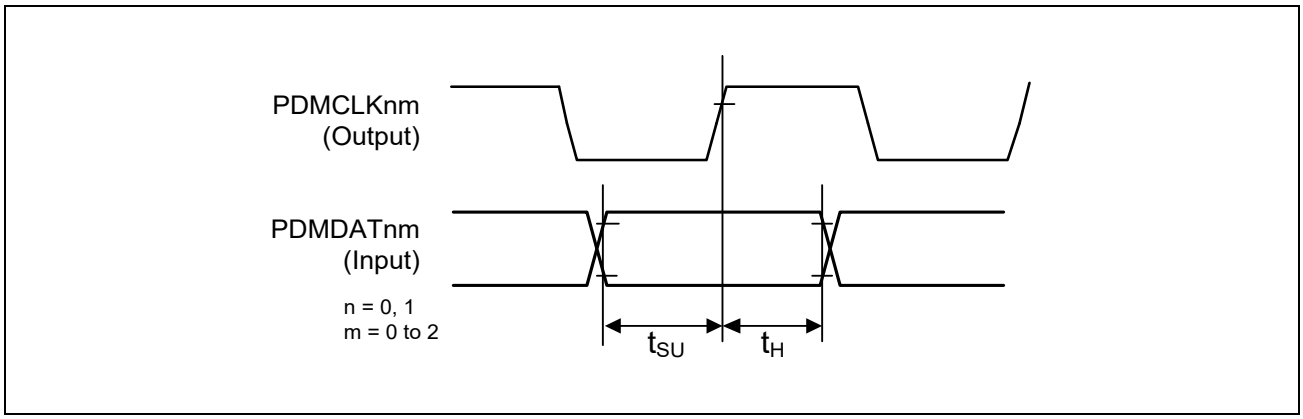


Figure 3.65 Timing of Clock Output (Synchronized with the rise of PDMCLKnm)

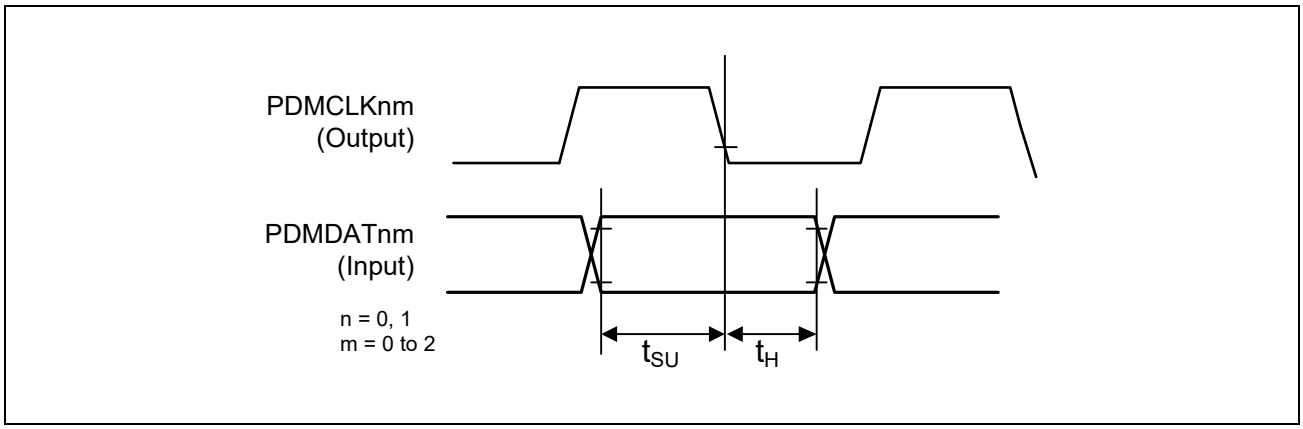


Figure 3.66 Timing of Clock Output (Synchronized with the fall of PDMCLKnm)

3.5.22 MIPI CSI-2 PHY Characteristics

The MIPI CSI-2 Rx D-PHY of this LSI is equivalent to the MIPI D-PHY Version 1.2.

For details, refer to the MIPI specification.

3.5.23 MIPI DSI Tx D-PHY Characteristics

The MIPI DSI Tx D-PHY of this LSI is compliant with the MIPI D-PHY Version 1.2.

For details, refer to the MIPI specification.

3.5.24 Control Signal Access Timing

Table 3.31 Control Signal Timing

Item	Symbol	Min.	Max.	Unit	Figures
QRESN pulse width	t_{RESW}	1	—	µs	**Figure 3.67**
TRSTN pulse width	t_{TRSW}	1	—	µs	
NMI pulse width	t_{NMIW}	20	—	t_{cyc}*1	**Figure 3.68**
IRQ pulse width	t_{IRQW}	20	—	t_{cyc}*1	
TINT pulse width	t_{TINTW}	20	—	t_{cyc}*1	

Note 1. t_{cyc} = 41.666 ns (24 MHz)

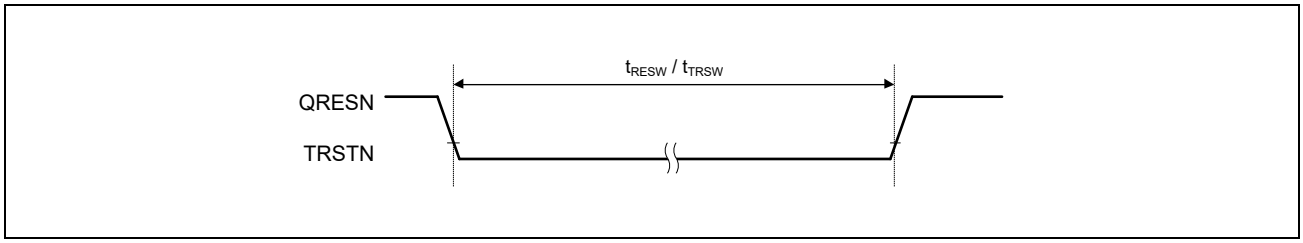
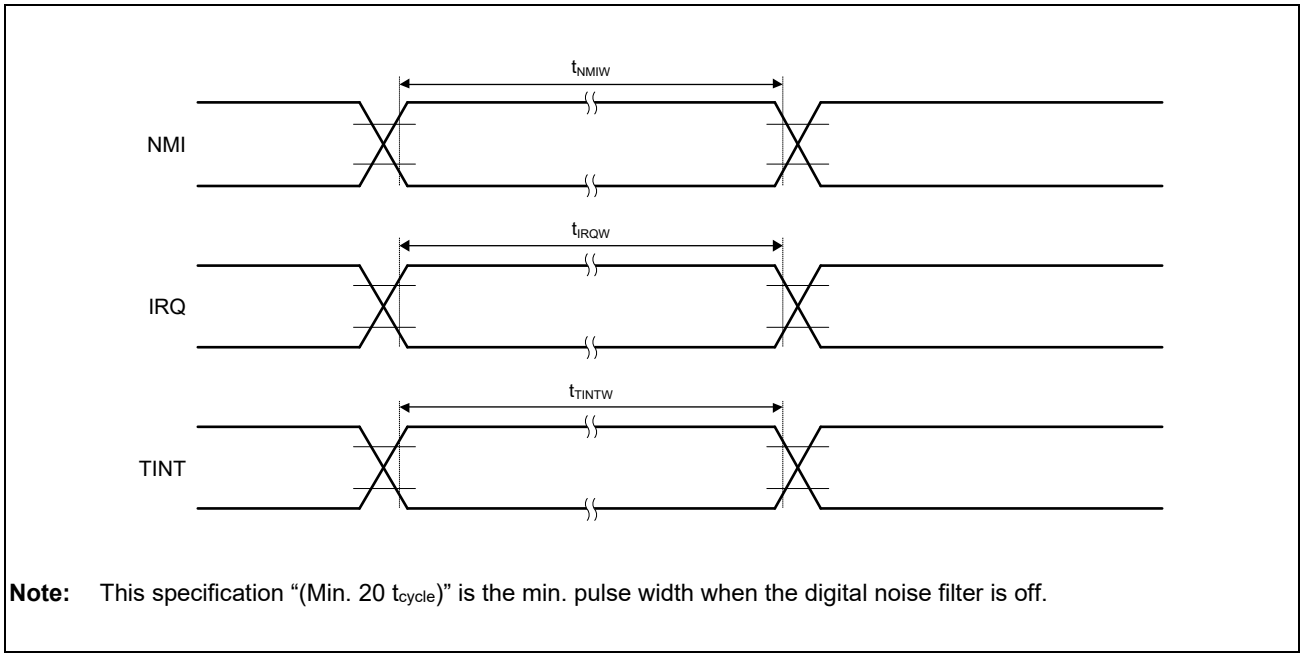


Figure 3.67 Reset Input Timing



Note: This specification “(Min. 20 t_{cycle})” is the min. pulse width when the digital noise filter is off.

Figure 3.68 Interrupt Signal Input Timing

3.5.25 JTAG Debugger Interface Access Timing

Table 3.32 Debugger IF Timing

Item	Symbol	Min.	Max.	Unit	Figures
TCK_SWCLK cycle time	t_{TCKcyc}	50	—	ns	**Figure 3.69**
TCK_SWCLK high-level pulse width	t_{TCKH}	20	—	ns	**Figure 3.70**
TCK_SWCLK low-level pulse width	t_{TCKL}	20	—	ns	
TDI setup time	t_{TDIS}	15	—	ns	
TDI hold time	t_{TDIH}	15	—	ns	
TMS_SWDIO setup time	t_{TMSS}	15	—	ns	
TMS_SWDIO hold time	t_{TMSH}	15	—	ns	
TMS_SWDIO delay time	t_{SWDO}	—	14	ns	
TDO delay time	t_{TDOD}	—	14	ns	
Capture register setup time	t_{CAPTS}	10	—	ns	**Figure 3.71**
Capture register hold time	t_{CAPTH}	10	—	ns	
Update register delay time	$t_{UPDATED}$	—	20	ns	

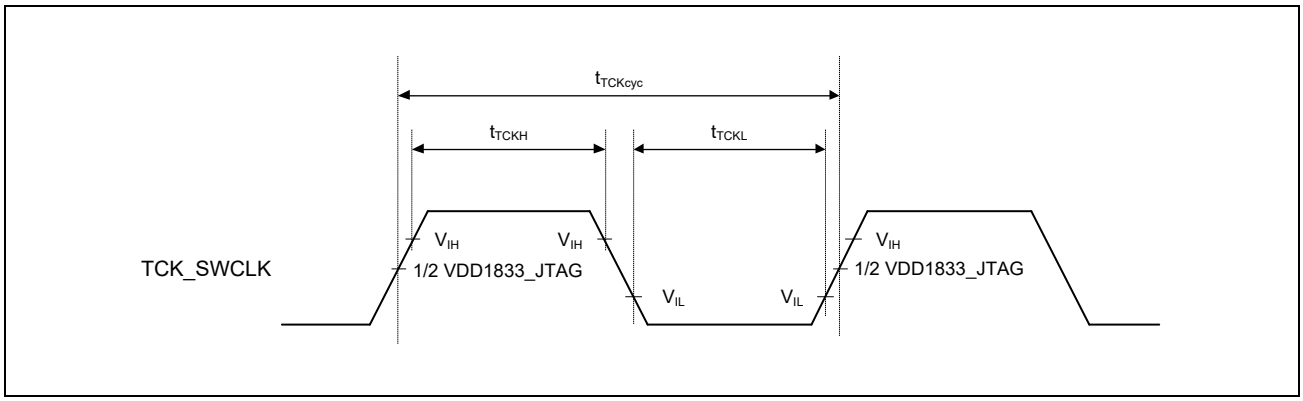


Figure 3.69 TCK_SWCLK Input Timing

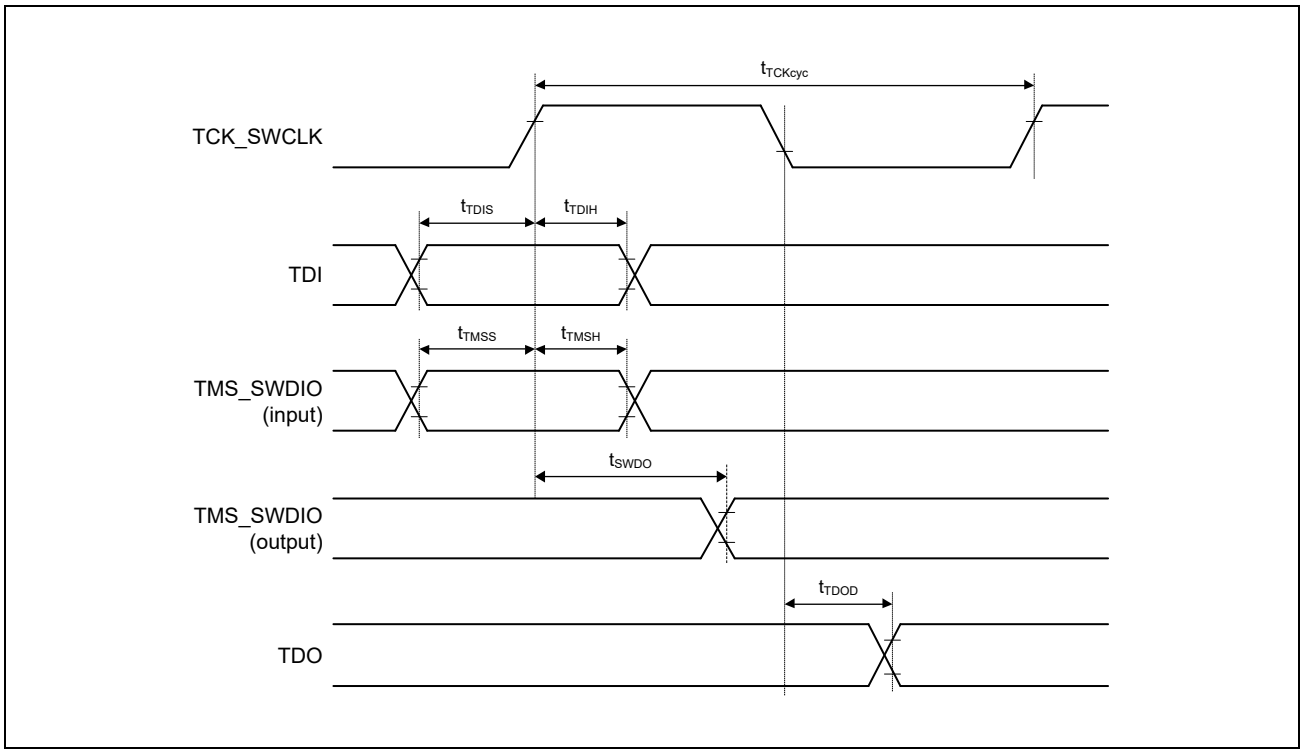


Figure 3.70 Data Transfer Timing

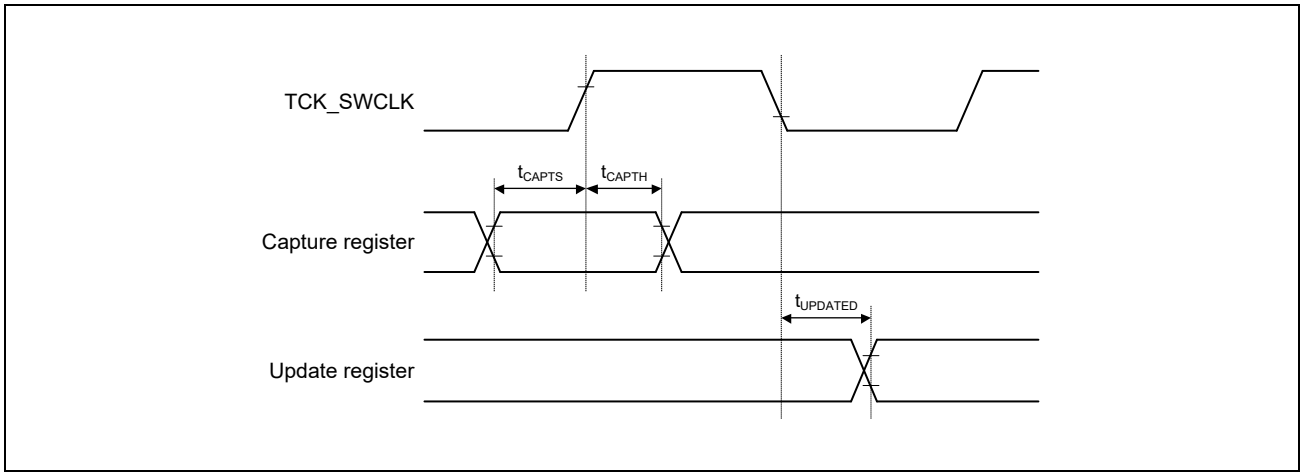


Figure 3.71 Boundary Scan Input/Output I/O Timing

3.5.26 LCDC

Conditions:

V_{OH} = VDD18 × 0.7, V_{OL} = VDD18 × 0.3, C = 30 pF

V_{OH} = VDD33 × 0.7, V_{OL} = VDD33 × 0.3, C = 30 pF

Drive strength: ×6

Table 3.33 LCDC IF Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
LCD_CLK period	t_{Lcyc}	11.49	—	185.19	ns
LCD_CLK low pulse width	t_{LOL}	t_{Lcyc}/2 − 1.06	—	t_{Lcyc}/2 + 1.06	ns
LCD_CLK high pulse width	t_{LOH}	t_{Lcyc}/2 − 1.06	—	t_{Lcyc}/2 + 1.06	ns
LCD_CLK rise time	t_{LOR}	—	—	3	ns
LCD_CLK fall time	t_{LOF}	—	—	3	ns
Data output dealy	t_{DD}	−1.5	—	1.5	ns

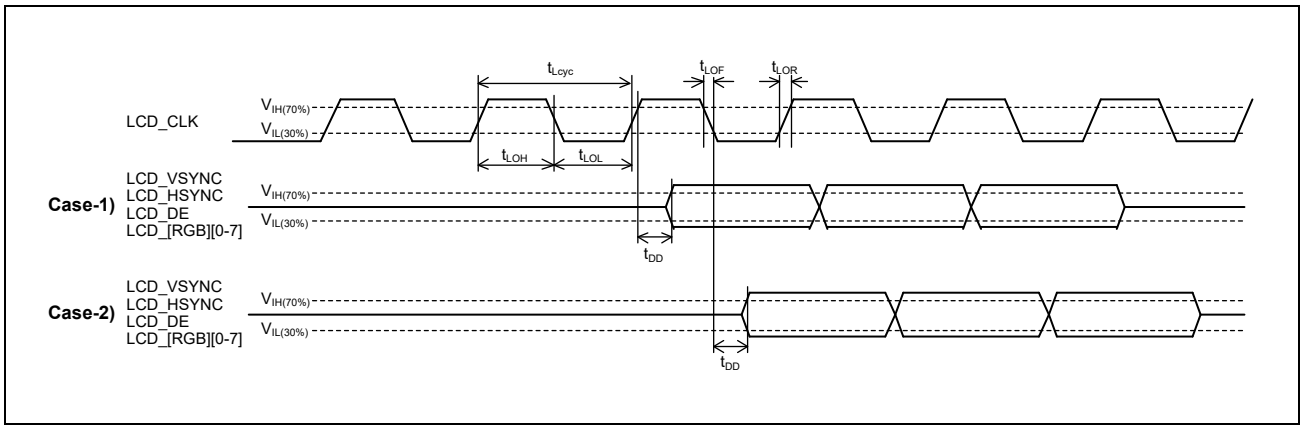


Figure 3.72 Boundary Scan Input/Output I/O Timing

3.5.27 LVDS Interface

Table 3.34 LVDS IF Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Output Clock Frequency of LVDS	$F_{CLKP/CLKN}$	25	—	87	MHz	**Figure 3.73**
Output Clock of LVDS	T_{CP}	11.494	—	40	ns	
Output Data Rate of LVDS	$F_{DAP/DAN}$	175	—	609	Mbps	
LVDS Output Pulse Position 0	T_{PPOS0}	−0.200	0	0.200	ns	
LVDS Output Pulse Position 1	T_{PPOS1}	$(T_{CP}/7) - 0.200$	$(T_{CP}/7)$	$(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 2	T_{PPOS2}	$2(T_{CP}/7) - 0.200$	$2(T_{CP}/7)$	$2(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 3	T_{PPOS3}	$3(T_{CP}/7) - 0.200$	$3(T_{CP}/7)$	$3(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 4	T_{PPOS4}	$4(T_{CP}/7) - 0.200$	$4(T_{CP}/7)$	$4(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 5	T_{PPOS5}	$5(T_{CP}/7) - 0.200$	$5(T_{CP}/7)$	$5(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 6	T_{PPOS6}	$6(T_{CP}/7) - 0.200$	$6(T_{CP}/7)$	$6(T_{CP}/7) + 0.200$	ns	

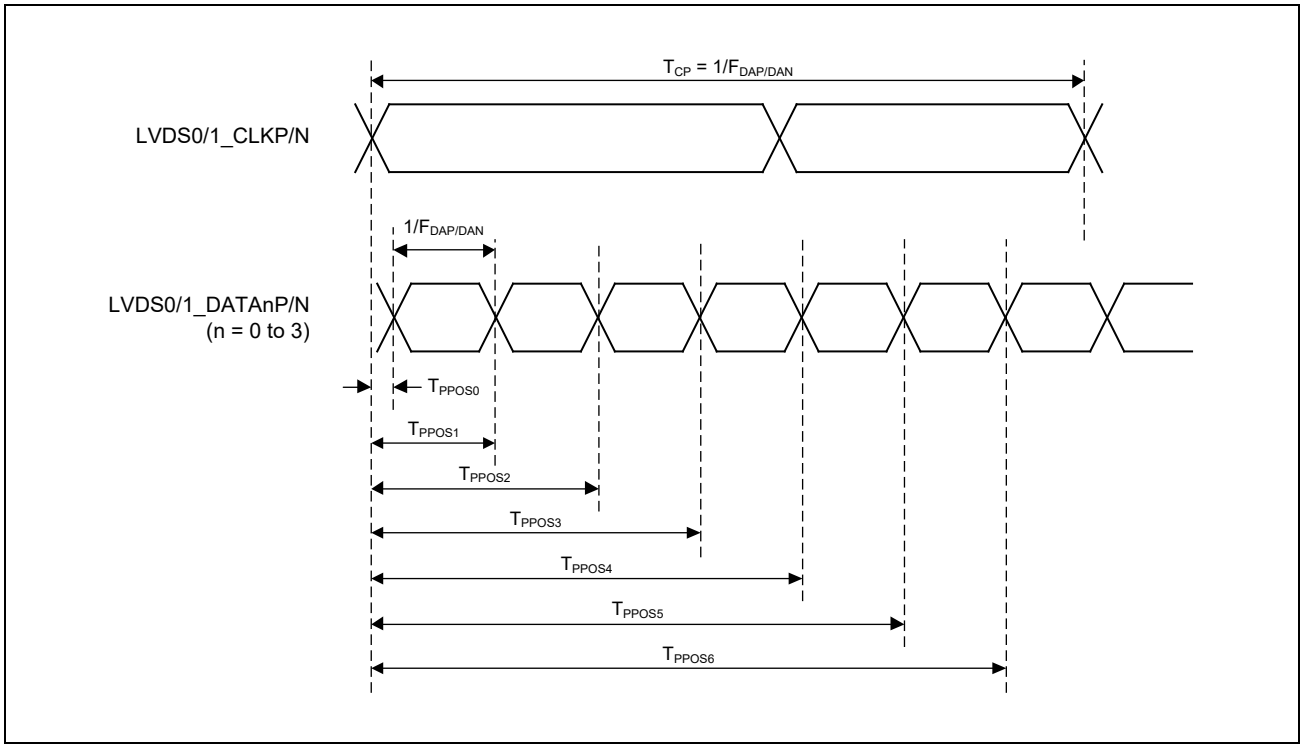


Figure 3.73 T_{CP}, $F_{DAP/DAN}$, T_{PPOS}

3.6 Analog Characteristics

3.6.1 ADC Characteristics

Table 3.35 DC Characteristics

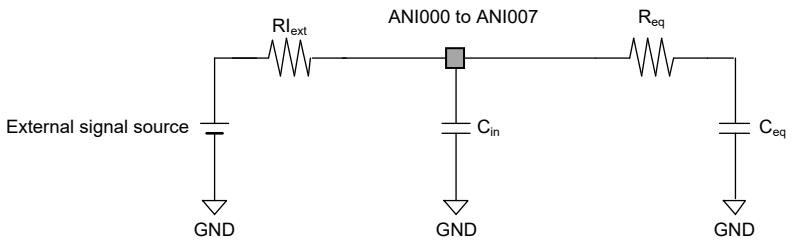
Item	Min.	Typ.	Max.	Unit
Resolution	—	12	—	Bit
Analog input capacitance	—	—	13	pF
Analog input range	0	—	ADAVDD18	V
Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ	0.4	—	4.0	µs
Offset error	0	—	100	LSB
Full-scale error	−100	—	0	LSB
Quantization error	—	±0.5	—	LSB
DNL differential non-linearity error	—	±1.0	±3.0	LSB
INL integral nonlinearity error	—	±2.0	±6.0	LSB

Note 1. The conversion time is the total of the sampling time and the comparison time.

Table 3.36 Recommended External Input Resistance

Item	Symbol	Min.	Typ.	Max.	Unit
External input resistance*1 (ANI000-ANI007)	RI_{ext}	—	—	1	kΩ

Note 1. Output resistance of signal generator + Series parasitic resistance between signal source and ADC input.



Note: Analog input equivalent resistance (R_{eq}): 500Ω
Analog input equivalent capacitance (C_{eq}): 10 pF
Analog input pin capacitance (C_{in}): 3 pF

Figure 3.74 A/D Converter Equivalent Circuit and Peripheral Configuration Diagram

3.6.2 Temperature Sensor Characteristics

Table 3.37 Temperature Sensor Characteristics

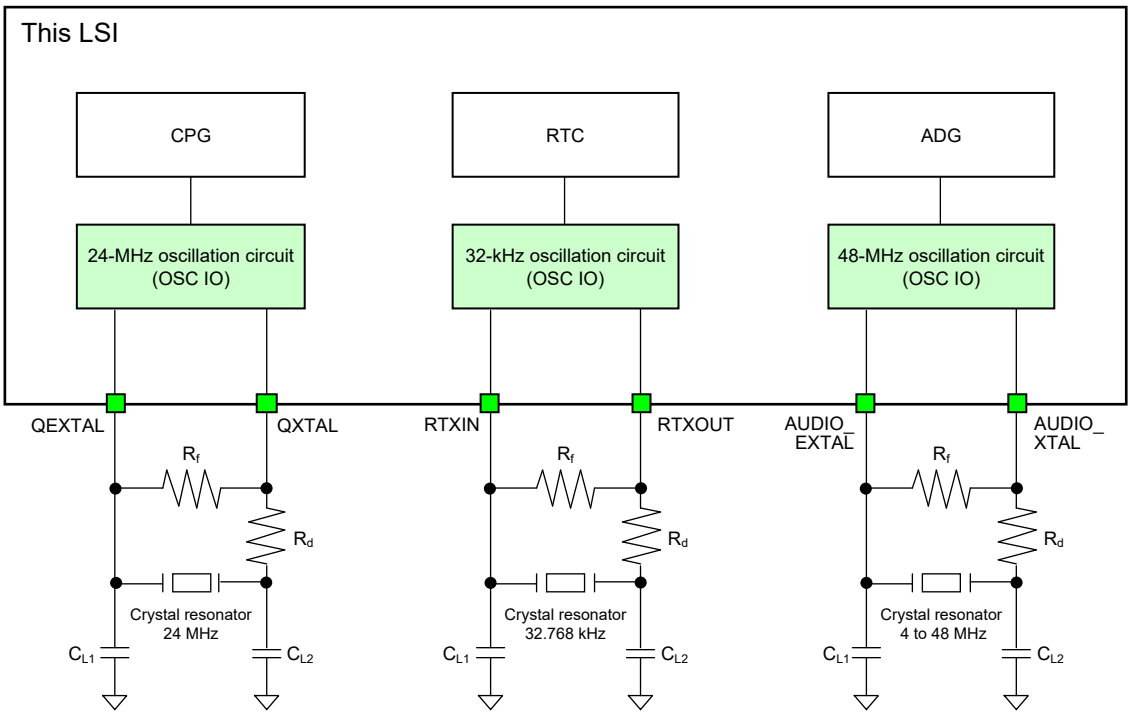
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Accuracy from −40°C to 125°C	Accm40_125	—	±3.0	±5.0	°C	

3.7 Oscillation Circuits for Connecting Crystal Resonators (OSC)

This LSI chip includes three oscillation circuits (OSC) for connection to crystal resonators, specifically a 24-MHz crystal resonator for the system clock, a frequency range between 4 and 48-MHz crystal resonator for the audio clocks and a 32.768-kHz crystal resonator for the real-time clock. **Table 3.38** lists the pins for connecting the crystal resonators and the clock frequencies. **Figure 3.75** shows an example of the connections with crystal resonators.

Table 3.38 Pins for Connecting Crystal Resonators and Clock Frequency

External Pin Name	I/O	Clock Frequency
For the system clock		
QEXTAL	Input	24 MHz (frequency deviation: ±50 ppm)
QXTAL	Output	24 MHz
For the real-time clock		
RTXIN	Input	32.768 kHz (frequency deviation: ±50 ppm)
RTXOUT	Output	32.768 kHz
For the audio clocks		
AUDIO_EXTAL	Input	4 to 48 MHz
AUDIO_XTAL	Output	4 to 48 MHz



Note: R_f: Feedback resistor
R_d: Dumping resistor
C_{load} (load capacitance of the crystal): See below for the formula.

$$C_{load} = \{C_{L1} \times C_{L2} / (C_{L1} + C_{L2})\} + \text{PCB's floating capacitance}$$

Figure 3.75 Example of Connections with Crystal Resonators

Place the crystal resonators and the capacitors C_{L1} and C_{L2} as close as possible to the pins to connect crystal resonators. To avoid interference and to ensure correct oscillation, the grounding points of the capacitors appended to the crystal resonators should be shared, and no wiring patterns should be placed near these components.

The characteristics of the crystal resonators are closely related to the design of the user board. Therefore, the user should sufficiently evaluate them with reference to the example of connection of crystal resonators in **Figure 3.75**.

The circuit rating of a crystal resonator depends on the crystal resonator and the stray capacitance of the mounting circuit. Therefore, contact the manufacturer of the crystal resonator before deciding upon the circuit rating. The user should thoroughly evaluate and then set the parameters (resistor and capacitor values).

Table 3.39 is a list of recommended values for the crystal resonators.

Table 3.39 Recommended Model Values for the Crystal Resonators

	Model Values for the Crystal Resonators			
Clock Frequency	Max. ESR*1	Max. C_L*2	Max. C_0*3	Max. Drive Level
32.768 kHz	70 kΩ	12.5 pF	1.4 pF	1 µW
24 MHz	60 Ω	12 pF	7 pF	100 µW
48 MHz	50 Ω	10 pF	7 pF	100 µW

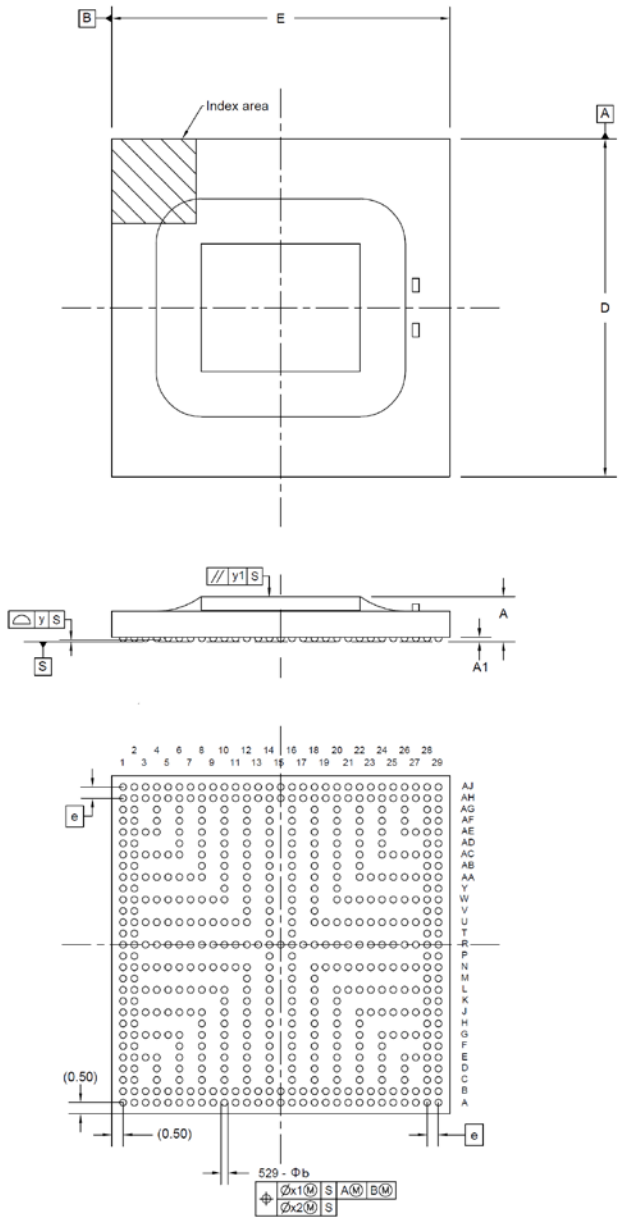
Note 1. ESR means the equivalent series resistor of the crystal resonator.

Note 2. C_L is the load capacitance of the crystal resonator.

Note 3. C_0 is the parallel capacitance of the crystal resonator.

4. Package Dimensions

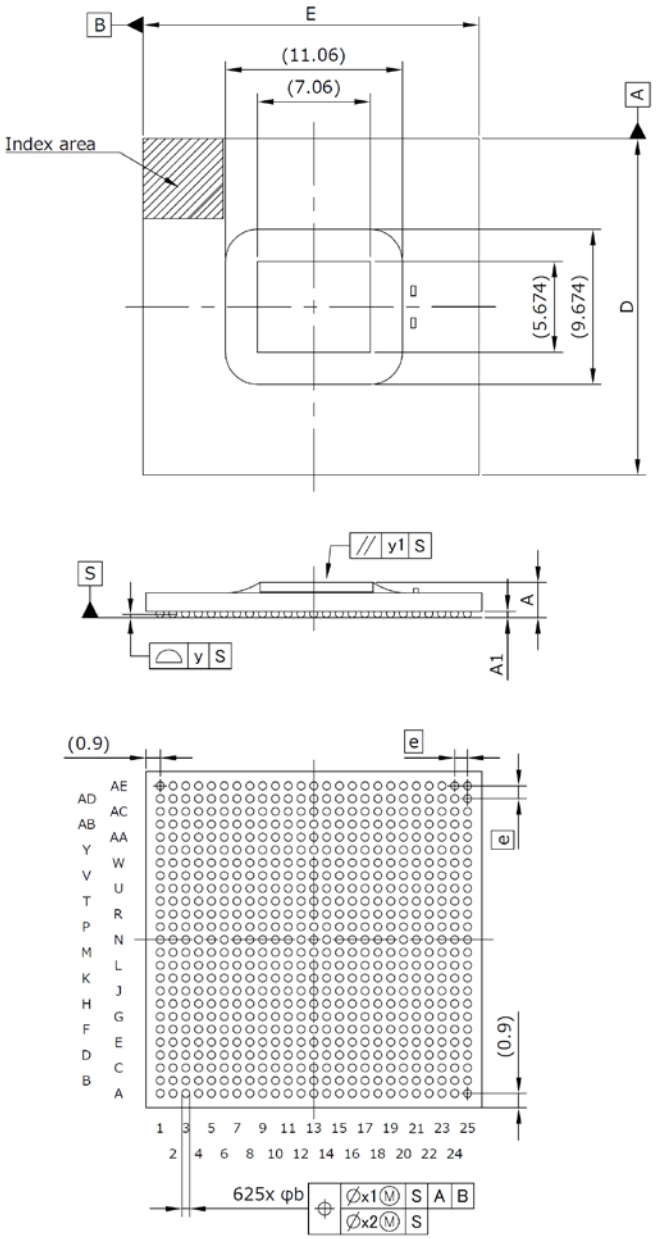
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA529-15x15-0.50	PRBG0529KA-A	0.82



Reference Symbol	Dimension in Millimeters		
	MIN.	NOM.	MAX.
D	14.85	15.00	15.15
E	14.85	15.00	15.15
e	—	0.50	—
A	(1.90)	(2.10)	2.30
A1	0.15	(0.25)	—
b	0.25	0.30	0.35
x1	—	—	0.20
x2	—	—	0.05
y	—	—	0.12
y1	—	—	0.20

Figure 4.1 Package Dimensions (529-pin FCBGA, 15 mm□ BGA 0.5 mm pin-pitch)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA625-21x21-0.80	PRBG0625GA-A	1.7



Reference Symbol	Dimension in Millimeters		
	MIN.	NOM.	MAX.
D	20.85	21.00	21.15
E	20.85	21.00	21.15
A	—	—	2.45
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x1	—	—	0.20
x2	—	—	0.08
y	—	—	0.15
y1	—	—	0.20

Figure 4.2 Package Dimensions (625-pin FCBGA, 21 mm□ BGA 0.8 mm pin-pitch)

REVISION HISTORY	RZ/G3E Group DATASHEET

Rev.	Date	Description	
		Page	Summary
1.00	Oct 31, 2024	—	First edition issued
1.10	Jun 30, 2025	Section 1 Overview	
		2	1.1.1 Features: NOTE added
		4	1.2.5 Video Processing Unit: The functional description (I-/P-slice supported, I-/P-/B-slice supported) was added to the Video Codec Unit (VCD)
		5	1.2.7 External Memory Interface: The functional description of External Bus Controller for LPDDR4/4X SDRAM (DDR), modified (16 ECC regions, deleted)
		6	1.2.8 CPU Peripheral: The external Interrupt pins of the Interrupt Controller, modified
		15	1.2.21 Package, modified
		16	Figure 1.3-1 Block Diagram: An arrow was added from the ACPU Bus to the NPU Bus
		17	Table 1.3-1 List of Units (1/2): GPV Unit, deleted
		19	Table 1.4-1 Product Lineup: Note 1 and Note, added
		20	1.5 External Pins and Multiplexed Functional Pins: Title, modified (Pin Functions → External Pins and Multiplexed Functional Pins), Text, modified
		20	1.6 Pin Assignment: Text, modified
		Section 2 Electrical CharacterIstics	
		21	Table 2.1-1 Absolute Maximum Ratings The Max value of Item: USB30_USVDD18, modified Notes 3 and 5, modified
		27	Figure 2.3-2 Power-On Sequence (CM33 Boot): Note, modified (The clock settling time → The clock stabilization time)
		29	Figure 2.3-3 DDR Retention Enter Sequence (CM33 Boot Mode): Note, modified (The clock settling time → The clock stabilization time)
		31	Figure 2.3-4 DDR Retention Exit Sequence (CM33 Boot Mode): Note, modified (The clock settling time → The clock stabilization time)
		33	Figure 2.3-5 Power-Off Sequence (CM33 Boot Mode): Note, modified (The clock settling time → The clock stabilization time)
		36	Figure 2.3-7 Power-On Sequence (CA55 Boot Mode): Note, modified (The clock settling time → The clock stabilization time)
		40	Figure 2.3-9 DDR Retention Exit Sequence (CA55 Boot Mode): Note, modified (The clock settling time → The clock stabilization time)
		42	Figure 2.3-10 Power-Off Sequence (CA55 Boot Mode): Note, modified (The clock settling time → The clock stabilization time)
		53	2.5.5 DMAC Timing, added
		59	2.5.9 Ethernet Interface Timing: Conditions, modified
		59	Table 2.5-12 Ethernet Interface Timing (n = 0, 1) The Min value of ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, and ETn_TXER output delay time in Parameter: Ethernet(MII), modified Note 1, added
		62	Table 2.5-13 xSPI Timing (2/2) The Min value in Parameter: DS low to CS high, modified The Max value in Parameter: CS low to DS low, modified Parameter: CK low to DS low, added Notes 5 to 9, added
		65	Figure 2.5-19 DS to CS Signal Timing, modified
		66	2.5.14 Serial Communications Interface (RSCI) Access Timing: Drive strength, modified

Rev.	Date	Description	
		Page	Summary
1.10	Jun 30, 2025	67	Table 2.5-14 RSCI Timing (2/2) Parameter: SCK clock rise/fall time, deleted Parameter: Input clock rise time, Input clock fall time, Output clock rise time, and Output clock fall time, added
		68	Figure 2.5-23 RSCI Simple SPI Mode Clock Timing, modified
		71	Table 2.5-15 RSPI Timing Parameter: SSL Activation to Data Output Delay, added Notes 1 to 4, modified
		72	Figure 2.5-28 RSPI Clock Timing, modified
		72	Figure 2.5-29 RSPI Timing (Master, Motorola RSPI, CPHA = 0), modified
		80	Table 2.5-19 IIC Timing (HS mode) The Min value in Parameter: SCL3n cycle time, modified
		82	Table 2.5-20 I3C Timing (Open Drain Timing Parameters) The Min value and Notes in Parameter: SCL3n clock High period, modified Notes in Parameter: Clock after START (S) condition, modified The Min value in Parameter: Clock before STOP (P) condition, modified Notes in Parameter: Bus available condition, modified Notes 3 and 4, added
		83	Table 2.5-21 I3C Timing (Push-Pull Timing Parameters for SDR) Notes in Parameter: SCL3n clock Low period, modified Parameter: SCL3n clock High period for Mixed Bus, added Notes in Parameter: SDA3n signal data hold in push-pull mode, modified Note 3, added
		90	2.5.20 SSIU Timing: Condition, modified
		90	Table 2.5-24 SSIU Signal Timing: Note 2, added
		95	2.5.21 PDM Timing: Condition, modified
		95	Table 2.5-25 PDM Interface Timing: Note 2, added
		104	2.7 Oscillation Circuits for Connecting Crystal Resonators (OSC): The main text, modified
		104	Table 2.7-1 Pins for Connecting Crystal Resonators and Clock Frequency: For the emergency clock, deleted
1.15	Nov 28, 2025	—	Modified the section structure: Added a new section for Pin (Section 2), moved Electrical Characteristics to Section 3, and Package Dimensions to Section 4.
		2	Features: NOTE, modified
		Section 1 Overview	
		19	Table 1.2 Product Lineup: Note 1, deleted

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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