RX23E-B Group
Renesas MCUs

R01DS0402EJ0100
Rev.1.00
Aug 31, 2023

32-MHz, 32-bit RX MCUs with up to 256-KB flash memory,
one low-noise and low-drift 24-bit delta-sigma A/D converter with high-speed data rate of up to 125 kSPS,
rail-to-rail programmable gain instrumentation amplifiers, ±10-V input pins,
a low-drift voltage reference, and on-chip excitation current sources

Features

■ 32-bit RXv2 CPU core
- Max. operating frequency: 32 MHz
  Capable of 64 DMIPS in operation at 32 MHz
- Enhanced DSP: 32-bit multiply-accumulate and 16-bit multiply-subtract instructions supported
- Built-in FPU: 32-bit single-precision floating point (compliant to IEEE754)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported

■ Low power design and architecture
- Operation from a single 1.8-V to 5.5-V supply
- Three low power consumption modes
- Low power timer (LPT) that operates during the software standby state

■ On-chip flash memory for code
- Read cycle of 31.25 ns in 32-MHz operation
- No waiting time when the CPU is reading at full speed
- 128-Kbyte and 256-Kbyte capacities
- On-board or off-board user programming
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory
- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states
- 16- and 32-Kbyte size capacities

■ Data transfer functions
- DMAC: Incorporates four channels
- DTC: Four transfer methods

■ ELC
- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

■ Reset and supply management
- Seven types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- Main clock oscillator frequency: 1 MHz to 20 MHz
- External clock input frequency: Up to 20 MHz
- Sub-clock oscillator frequency: 32.768 kHz
- PLL circuit input: 4 MHz to 8 MHz
- On-chip low- and high-speed oscillators, dedicated on-chip low-speed oscillator for the IWDT
- Clock frequency accuracy measurement circuit (CAC)

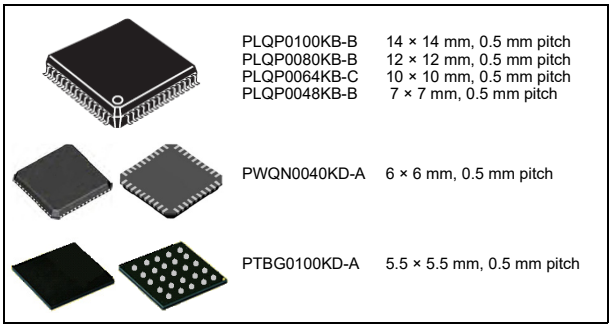
■ Realtime clock
- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable

■ Independent watchdog timer
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnect detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ MPC
- Input/output functions selectable from multiple pins

■ Up to eight communication functions
- CAN (one channel) compliant to ISO11898-1:
  Transfer at up to 1 Mbps
- SCI with many useful functions (up to seven channels), asynchronous mode, clock synchronous mode, smart card interface, reduction of errors in communications using the bit rate modulation function
- I^2C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI (one channel): Transfer at up to 16 Mbps



PLQP0100KB-B	14 × 14 mm, 0.5 mm pitch
PLQP0080KB-B	12 × 12 mm, 0.5 mm pitch
PLQP0064KB-C	10 × 10 mm, 0.5 mm pitch
PLQP0048KB-B	7 × 7 mm, 0.5 mm pitch
PWQN0040KD-A	6 × 6 mm, 0.5 mm pitch
PTBG0100KD-A	5.5 × 5.5 mm, 0.5 mm pitch

■ Up to 12 extended-function timers
- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (two channels)

■ Analog functions
- One 24-bit delta-sigma A/D converter
- A/D converter with up to 24-bit effective resolution (gain = 1, output data rate = 3.8 SPS)
- High-precision programmable gain instrumentation amplifier, 11 nV_{RMS} (gain = 128, output data rate = 3.8 SPS)
- Rail-to-rail programmable gain instrumentation amplifier (gain = 1 to 128)
- Programmable data rate: 3.8 SPS to 125 kSPS (f_{MOD} = 4 MHz)
- Offset drift 4 nV/°C (gain = 64 to 128)
- Gain drift 1 ppm/°C (gain = 1 to 16 (PGA enable))
- Up to eight differential inputs, 16 single-ended inputs
- Four types of digital filters
  Fourth-order sinc filter
  Fourth-order sinc filter + fourth-order sinc filter
  Fifth-order sinc filter
  Fifth-order sinc filter + first-order sinc filter
- Simultaneous 50 Hz/60 Hz rejection (output data rate = 10, 54 SPS)
- Offset error and gain error calibration
- ±10-V input pins
- Delta-sigma A/D input disconnect detection assist
- Delta-sigma A/D reference voltage external input
- Voltage reference
  output voltage: 2.5 V, temperature drift: 8 ppm/°C (T_a = –40 to +85°C), output current: ±10 mA
- Excitation current sources: Up to two
  Output current: 50 µA to 1000 µA, current matching: ±0.2%, drift matching: 5 ppm/°C
- Bias voltage generator
  output voltage: (AVCC0 + AVSS0)/2
- Temperature sensor: Accuracy ±5°C
- Low-side switch: 10 Ω on-resistance
- Low power-supply-voltage detectors
- Delta-sigma A/D input voltage fault detectors
- Delta-sigma A/D reference voltage fault detectors and disconnect detectors
- Excitation current source disconnect detectors
- High-voltage analog common input disconnect detector

■ 12-bit A/D converter
- Capable of conversion within 1.4 µs
- Eight channels
- Sampling time can be set for each channel
- Self-diagnostic function and analog input disconnect detection assistance function

■ 16-bit D/A converter
- One channel
- DNL = ±1LSB, INL = ±5LSB (max, VREFH ≥ 4.5 V)

■ General I/O ports
- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Operating temperature range
- –40°C to +85°C
- –40°C to +105°C

■ Applications
- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 (variable-length instruction format) • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 128/256 Kbytes • 32 MHz: No-wait access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 16/32 Kbytes • 32 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) Operations of the CPU and system sections such as other bus masters are synchronized with the ICLK (at up to 32 MHz). Operation of the MTU2a is synchronized with the PCLKA (at up to 32 MHz). The operating clock for the DSAD is synchronized with the PCLKC (at up to 16 MHz). The operating clock for the S12AD (ADCLK) is synchronized with the PCLKD (at up to 32 MHz). Operations of the peripheral modules other than the MTU2a, DSAD, and S12AD are synchronized with the PCLKB (at up to 32 MHz). Operation of the flash peripheral circuit is synchronized with the FCLK (at up to 32 MHz).
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset

Table 1.1 Outline of Specifications (2/5)

Classification	Module/Function	Description
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels • Voltage detection circuit 2 is capable of monitoring the input voltage on the CMPA2 pin.
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode • Low power timer that operates during the software standby state
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 256 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
Event link controller (ELC)		• Event signals can be connected directly to the module • Operations of timer modules are selectable at event input • Capable of event link operation with port B and port E
I/O ports	General I/O ports	• I/O ports for the 100-pin TFBGA, 100-pin LFQFP without high-voltage input pins I/O pins: 58 Input pin: 1 Pull-up resistors: 59 Open-drain outputs: 58 5-V tolerance: 6 • I/O ports for the100-pin TFBGA, 100-pin LFQFP with high-voltage input pins I/O pins: 58 Input pin: 1 Pull-up resistors: 59 Open-drain outputs: 58 5-V tolerance: 4 • I/O ports for the 80-pin LFQFP I/O pins: 43 Input pin: 1 Pull-up resistors: 44 Open-drain outputs: 43 5-V tolerance: 2 • I/O ports for the 64-pin LFQFP with high-voltage input pins I/O pins: 30 Input pin: 1 Pull-up resistors: 31 Open-drain outputs: 30 5-V tolerance: 2 • I/O ports for the 64-pin LFQFP without high-voltage input pins I/O pins: 27 Input pin: 1 Pull-up resistors: 28 Open-drain outputs: 27 5-V tolerance: 2

Table 1.1 Outline of Specifications (3/5)

Classification	Module/Function	Description
I/O ports	General I/O ports	• I/O ports for the 48-pin LFQFP I/O pins: 17 Input pin: 1 Pull-up resistors: 18 Open-drain outputs: 17 5-V tolerance: 2 • I/O ports for the 40-pin HWQFN with high-voltage input pins I/O pins: 13 Input pin: 1 Pull-up resistors: 14 Open-drain outputs: 13 5-V tolerance: 2 • I/O ports for the 40-pin HWQFN without high-voltage input pins I/O pins: 14 Input pin: 1 Pull-up resistors: 15 Open-drain outputs: 14 5-V tolerance: 2
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset-synchronized PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 unit • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCc)	• Clock sources: Sub clock • Calendar count mode or binary count mode selectable • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt
	Low power timer (LPT)	• 16 bits × 1 channel • Clock source: Sub-clock, dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer

Table 1.1 Outline of Specifications (4/5)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 7 channels (channel 0, 1, 5, 6, 8, 9: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
	Serial peripheral interface (RSPIc)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception • Transmit/receive data can be swapped in byte units • RSPCK can be stopped with the receive buffer full for master reception.
	CAN module (RSCAN)	• 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 Message boxes
LCD controller/driver (LCDC)		• Internal voltage boosting method, capacitor split method, and external resistance division method are switchable. • Segment signal output × common signal output: 40 × 4, 36 × 8
24-bit delta-sigma A/D converter (DSADB)		• 24 bits (8 channels × 1 unit) • Type of A/D conversion: delta-sigma • Digital filter: Fourth-order sinc filter, Fourth-order sinc filter + fourth-order sinc filter, Fifth-order sinc filter, or Fifth-order sinc filter + first-order sinc filter • 24-bit resolution • Data rate: 3.8 SPS to 125 kSPS • Input types: Differential, pseudo-differential, or single-ended • Modulator clock: 4 MHz (typ.), 125 kHz or higher in low-speed operation • Total oversampling ratio: 32 to 1048576 • Includes a programmable gain instrumentation amplifier (PGA) Gain settings: ×1, ×2, ×4, ×8, ×16, ×32, ×64, ×128 PGA bypass function: with or without an analog input buffer • Configuration settings per channel • Conditions for starting A/D conversion: software trigger or ELC • Disconnect detection assist • Selectable reference voltage

Table 1.1 Outline of Specifications (5/5)

Classification	Module/Function	Description
16-bit D/A converter (R16DA)		• 16 bits (1 channel) • Internal output buffer (to support external output) • Selectable reference voltage (to support externally input reference voltages) • Conditions for starting D/A conversion: software trigger or ELC
Analog front end (AFEA)		• Voltage reference (VREF) Output voltage: 2.5V • Output from bias voltage source (VBIAS) Output voltage: (AVCC0 + AVSS0)/2 • Internal temperature sensor (TEMPS) • Excitation current sources (IEXC) Two channels (up to 1000 µA) Output current settings: 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, 1000 µA • Analog multiplexer (AMUX) Select from among external pins, bias voltage sources, internal temperature sensor, excitation current sources, or 16-bit D/A converter • Input in the ±10-V range on the HVAIN pins Four channels • Low-side switch (LSW) On-resistance: 10 Ω (max.) Allowable current: 30 mA (max.) • Voltage detector (VDET) Voltage monitoring of AVCC0 Detection of abnormal voltages at DSAD inputs Detection of abnormal DSAD reference voltages and assistance in detecting disconnection Assistance in detecting disconnection for excitation current source output Detection of abnormal voltages on the HVCOM pin
12-bit A/D converter (S12ADE)		• 12 bits (8 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 32 MHz AVCC0 = 4.5 to 5.5 V (1.8 to 5.5 V when only S12AD is operating)
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 100-pin TFBGA (PTBG0100KD-A) 5.5 ×5.5 mm, 0.5 mm pitch 80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 40-pin HWQFN (PWQN0040KD-A) 6 × 6 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX23E-B Group							
		100 Pins	80 Pins	64 Pins	48 Pins	40 Pins	100 Pins/HV	64 Pins/HV	40 Pins/HV
Interrupts	External interrupts	NMI, IRQ0 to IRQ7					NMI, IRQ0 to IRQ7		
DMA	DMA controller	4 channels (DMAC0 to DMAC3)					4 channels (DMAC0 to DMAC3)		
	Data transfer controller	Available					Available		
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)					6 channels (MTU0 to MTU5)		
	Port output enable 2	POE0# to POE3#, POE8#					POE0# to POE3#, POE8#		
	8-bit timer	2 channels × 2 units					2 channels × 2 units		
	Compare match timer	2 channels × 1 unit					2 channels × 1 unit		
	Realtime clock	Available			Not supported		Available		Not supported
	Low power timer	1 channel					1 channel		
	Independent watchdog timer	Available					Available		
Communication functions	Serial communications interfaces (SCIg)	6 channels (SCI0, 1, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)	3 channels (SCI1, 5, 6)	2 channels (SCI1, 5)	6 channels (SCI0, 1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)	2 channels (SCI1, 5)
	Serial communications interfaces (SCIh)	1 channel (SCI12)					1 channel (SCI12)		
	I²C bus interface	1 channel					1 channel		
	CAN module	1 channel					1 channel		
	Serial peripheral interface	1 channel					1 channel		
LCD controller/driver		40 SEG × 4 COM 36 SEG × 8 COM	31 SEG × 4 COM 27 SEG × 8 COM	Not supported			40 SEG × 4 COM 36 SEG × 8 COM	Not supported	
24-bit delta-sigma A/D converter		1 unit, 8 channels of differential input			1 unit, 6 channels of differential input	1 unit, 4 channels of differential input	1 unit, 8 channels of differential input	1 unit, 6 channels of differential input	1 unit, 4 channels of differential input
16-bit D/A converter		1 channel					1 channel		
Analog front end	Voltage reference	Available					Available		
	Excitation current sources	2 channels					2 channels		
	Analog multiplexer	AIN: 8 channels (16 inputs)			AIN: 6 channels (12 inputs)	AIN: 4 channels (8 inputs)	AIN: 8 channels (16 inputs) HVAIN: 2 channels (4 inputs)	AIN: 4 channels (8 inputs) HVAIN: 2 channels (4 inputs)	AIN: 2 channels (4 inputs) HVAIN: 2 channels (4 inputs)
	Temperature sensor	Available					Available		
	Voltage detector	Available					Available		
12-bit A/D converter (including high-precision channels)		8 channels (8 channels)				6 channels (6 channels)	8 channels (8 channels)	6 channels (6 channels)	2 channels (2 channels)
CRC calculator		Available					Available		
Event link controller		Available					Available		
Packages		100-pin TFBGA 100-pin LFQFP	80-pin LFQFP	64-pin LFQFP	48-pin LFQFP	40-pin HWQFN	100-pin TFBGA 100-pin LFQFP	64-pin LFQFP	40-pin HWQFN

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (max.)	24-bit Delta-Sigma A/D Converter Sampling Rate (max.)	Analog Input Range (max.)	LCD	Operating Temperature
RX23E-B (D-version)	R5F523E6LDBS	PTBG0100KD-A	256 Kbytes	32 Kbytes	8 Kbytes	32 MHz	125 kSPS	10 V	Available	–40 to +85°C
	R5F523E6NDBS	PTBG0100KD-A					31.25 kSPS	5 V	Available	
	R5F523E6LDFP	PLQP0100KB-B					125 kSPS	10 V	Available	
	R5F523E6NDFP	PLQP0100KB-B					31.25 kSPS	5 V	Available	
	R5F523E6JDFN	PLQP0080KB-B					125 kSPS	5 V	Available	
	R5F523E6NDFN	PLQP0080KB-B					31.25 kSPS	5 V	Available	
	R5F523E6BDFM	PLQP0064KB-C					125 kSPS	5 V	Not available	
	R5F523E6KDFM	PLQP0064KB-C						10 V	Not available	
	R5F523E6MDFM	PLQP0064KB-C					31.25 kSPS	5 V	Not available	
	R5F523E6BDFL	PLQP0048KB-B					125 kSPS	5 V	Not available	
	R5F523E6MDFL	PLQP0048KB-B					31.25 kSPS	5 V	Not available	
	R5F523E6BDNF	PWQN0040KD-A					125 kSPS	5 V	Not available	
	R5F523E6KDNF	PWQN0040KD-A						10 V	Not available	
	R5F523E6MDNF	PWQN0040KD-A					31.25 kSPS	5 V	Not available	
	R5F523E5LDBS	PTBG0100KD-A	128 Kbytes	16 Kbytes	8 Kbytes	32 MHz	125 kSPS	10 V	Available	
	R5F523E5NDBS	PTBG0100KD-A					31.25 kSPS	5 V	Available	
	R5F523E5LDFP	PLQP0100KB-B					125 kSPS	10 V	Available	
	R5F523E5NDFP	PLQP0100KB-B					31.25 kSPS	5 V	Available	
	R5F523E5JDFN	PLQP0080KB-B					125 kSPS	5 V	Available	
	R5F523E5NDFN	PLQP0080KB-B					31.25 kSPS	5 V	Available	
	R5F523E5BDFM	PLQP0064KB-C					125 kSPS	5 V	Not available	
	R5F523E5KDFM	PLQP0064KB-C						10 V	Not available	
	R5F523E5MDFM	PLQP0064KB-C					31.25 kSPS	5 V	Not available	
	R5F523E5BDFL	PLQP0048KB-B					125 kSPS	5 V	Not available	
	R5F523E5MDFL	PLQP0048KB-B					31.25 kSPS	5 V	Not available	
	R5F523E5BDNF	PWQN0040KD-A					125 kSPS	5 V	Not available	
	R5F523E5KDNF	PWQN0040KD-A						10 V	Not available	
	R5F523E5MDNF	PWQN0040KD-A					31.25 kSPS	5 V	Not available	
RX23E-B (G-version)	R5F523E6LGBS	PTBG0100KD-A	256 Kbytes	32 Kbytes	8 Kbytes	32 MHz	125 kSPS	10 V	Available	–40 to +105°C
	R5F523E6NGBS	PTBG0100KD-A					31.25 kSPS	5 V	Available	
	R5F523E6LGFP	PLQP0100KB-B					125 kSPS	10 V	Available	
	R5F523E6NGFP	PLQP0100KB-B					31.25 kSPS	5 V	Available	
	R5F523E6JGFN	PLQP0080KB-B					125 kSPS	5 V	Available	
	R5F523E6NGFN	PLQP0080KB-B					31.25 kSPS	5 V	Available	
	R5F523E6BGFM	PLQP0064KB-C					125 kSPS	5 V	Not available	
	R5F523E6KGFM	PLQP0064KB-C						10 V	Not available	
	R5F523E6MGFM	PLQP0064KB-C					31.25 kSPS	5 V	Not available	
	R5F523E6BGFL	PLQP0048KB-B					125 kSPS	5 V	Not available	
	R5F523E6MGFL	PLQP0048KB-B					31.25 kSPS	5 V	Not available	

Table 1.3 List of Products (2/2)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (max.)	24-bit Delta-Sigma A/D Converter Sampling Rate (max.)	Analog Input Range (max.)	LCD	Operating Temperature
RX23E-B (G-version)	R5F523E6BGNF	PWQN0040KD-A	256 Kbytes	32 Kbytes	8 Kbytes	32 MHz	125 kSPS	5 V	Not available	–40 to +105°C
	R5F523E6KGNF	PWQN0040KD-A						10 V	Not available	
	R5F523E6MGNF	PWQN0040KD-A					31.25 kSPS	5 V	Not available	
	R5F523E5LGBS	PTBG0100KD-A	128 Kbytes	16 Kbytes	8 Kbytes	32 MHz	125 kSPS	10 V	Available	
	R5F523E5NGBS	PTBG0100KD-A					31.25 kSPS	5 V	Available	
	R5F523E5LGFP	PLQP0100KB-B					125 kSPS	10 V	Available	
	R5F523E5NGFP	PLQP0100KB-B					31.25 kSPS	5 V	Available	
	R5F523E5JGFN	PLQP0080KB-B					125 kSPS	5 V	Available	
	R5F523E5NGFN	PLQP0080KB-B					31.25 kSPS	5 V	Available	
	R5F523E5BGFM	PLQP0064KB-C					125 kSPS	5 V	Not available	
	R5F523E5KGFM	PLQP0064KB-C						10 V	Not available	
	R5F523E5MGFM	PLQP0064KB-C					31.25 kSPS	5 V	Not available	
	R5F523E5BGFL	PLQP0048KB-B					125 kSPS	5 V	Not available	
	R5F523E5MGFL	PLQP0048KB-B					31.25 kSPS	5 V	Not available	
	R5F523E5BGNF	PWQN0040KD-A					125 kSPS	5 V	Not available	
	R5F523E5KGNF	PWQN0040KD-A						10 V	Not available	
	R5F523E5MGNF	PWQN0040KD-A					31.25 kSPS	5 V	Not available	

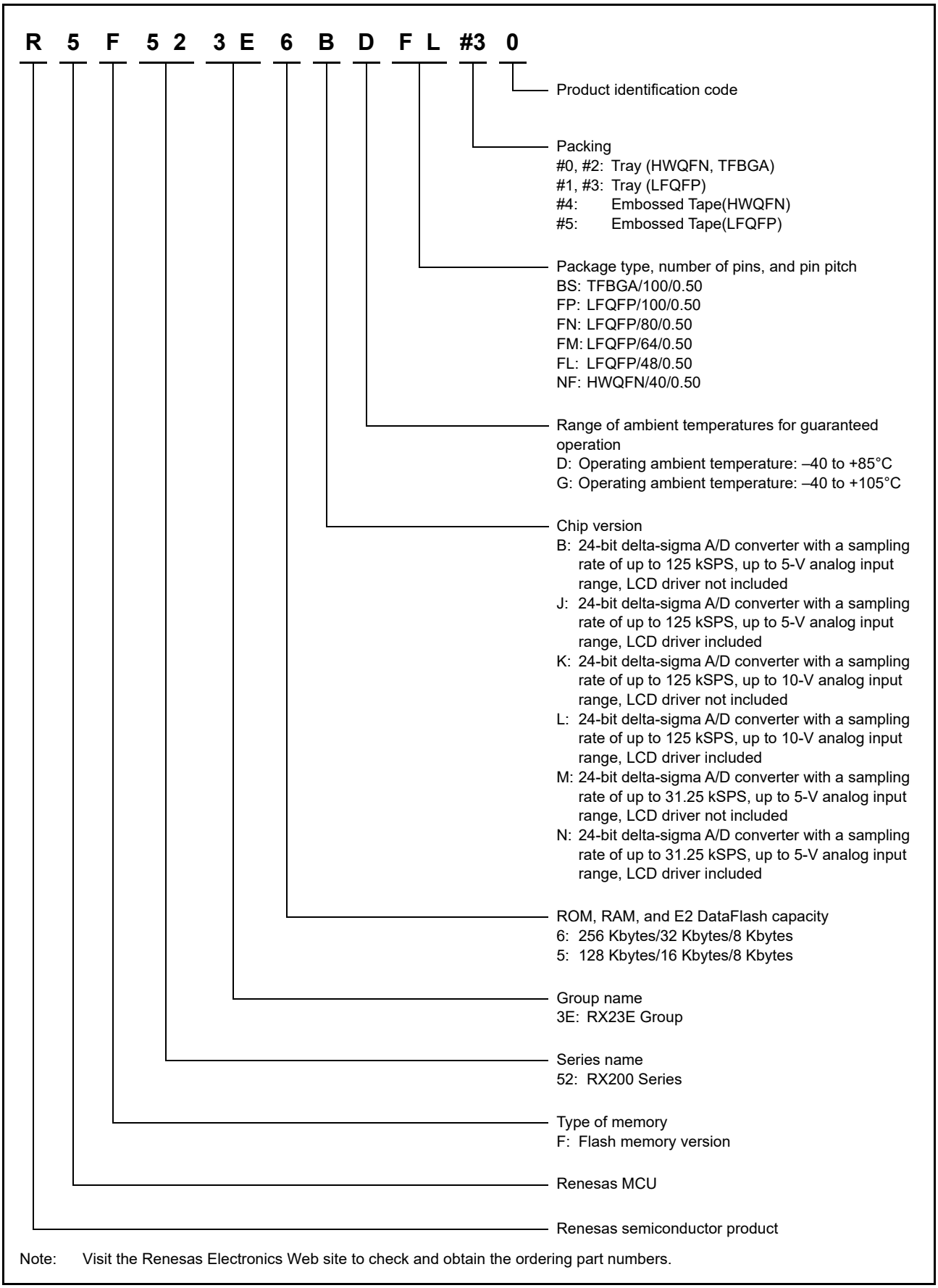
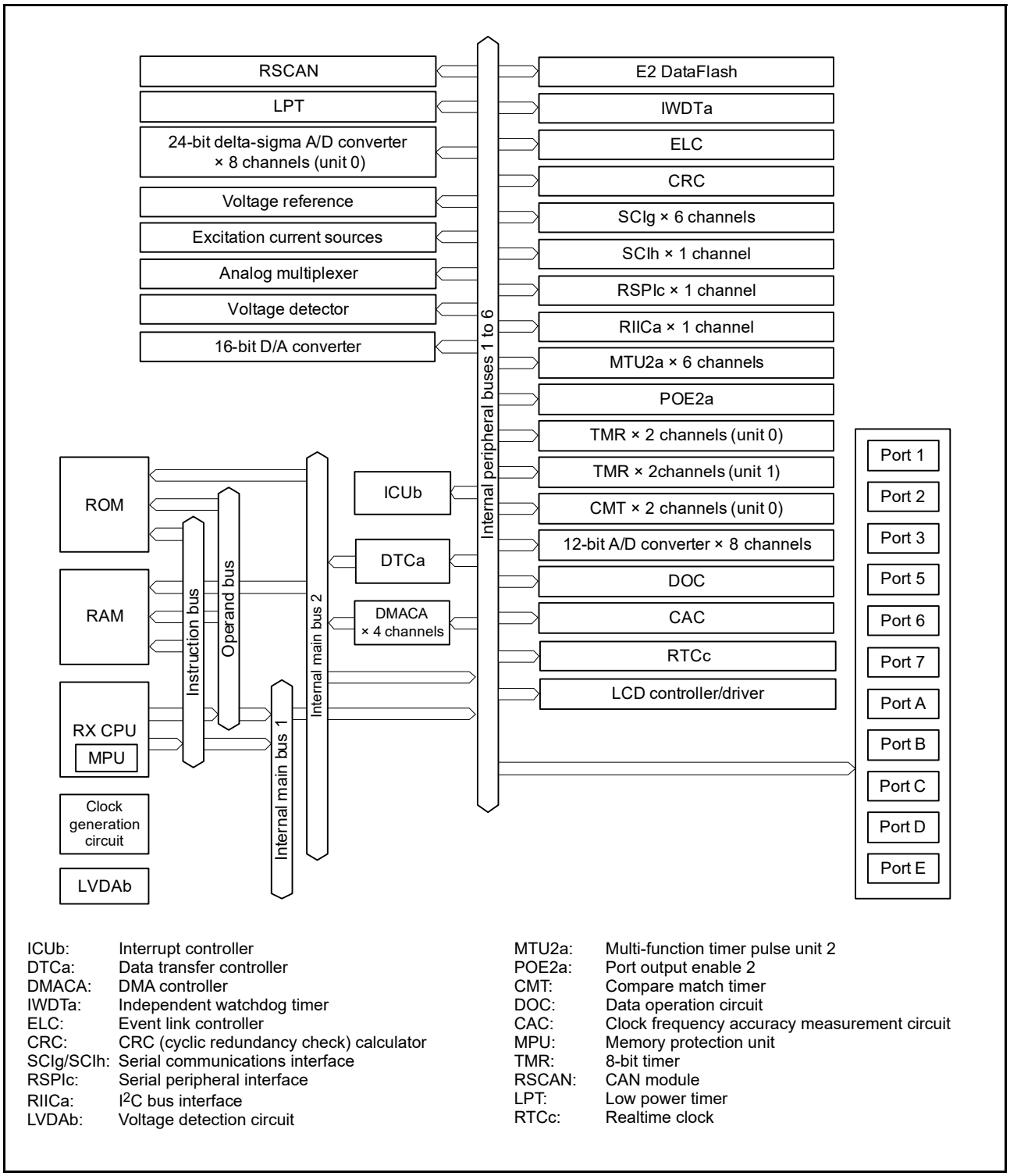


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIg/SCIh: Serial communications interface
RSPIc: Serial peripheral interface
RIICa: I^2C bus interface
LVDAb: Voltage detection circuit
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
CMT: Compare match timer
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit
MPU: Memory protection unit
TMR: 8-bit timer
RSCAN: CAN module
LPT: Low power timer
RTCc: Realtime clock

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.

Table 1.4 Pin Functions (2/3)

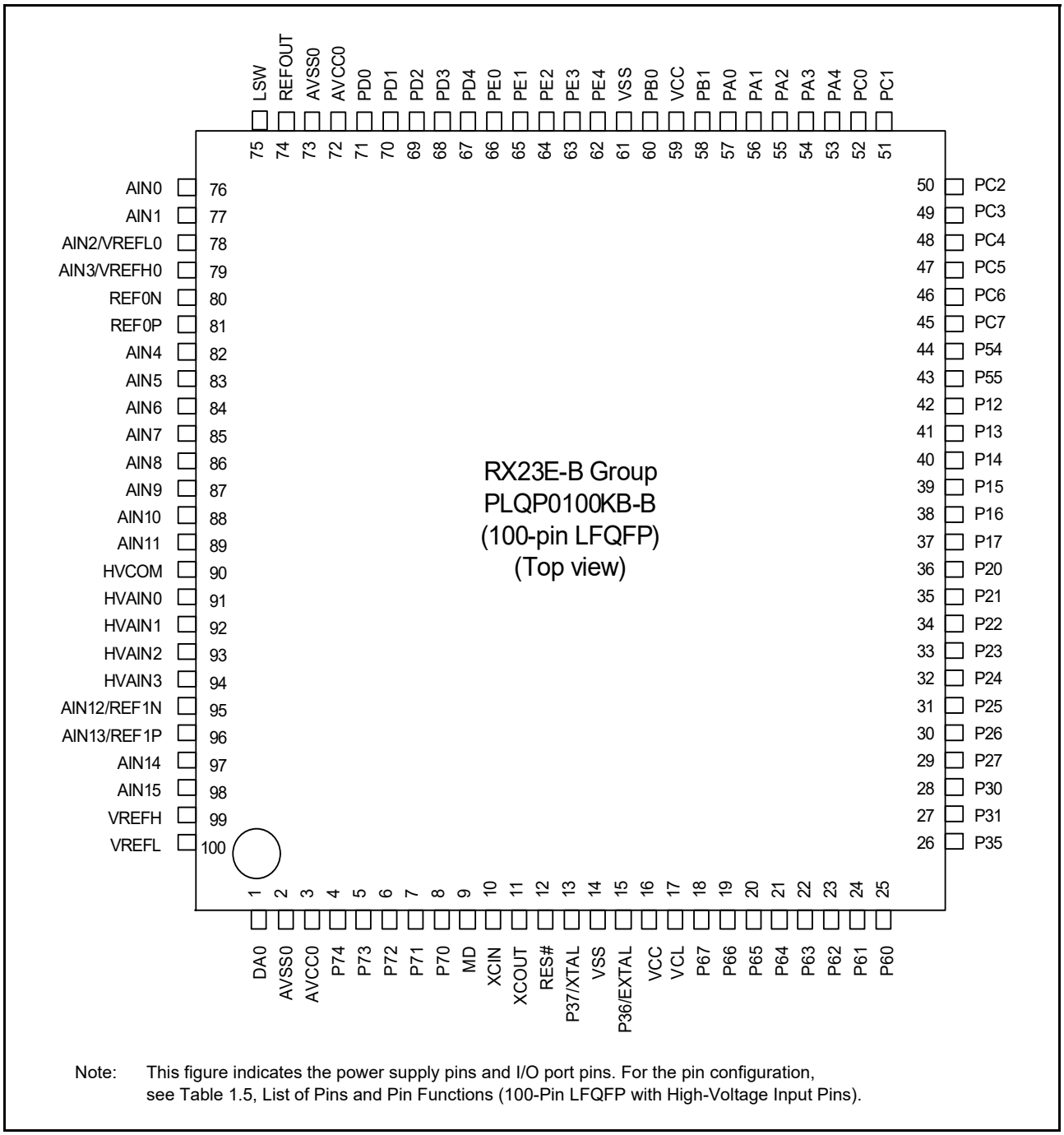
Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I2C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I2C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I2C data.
	• Simple SPI mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	SMISO0, SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS5#, SS6#, SS8#, SS9#	Input	Slave-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I2C mode		
	SSCL12	I/O	Input/output pin for the I2C clock.
	SSDA12	I/O	Input/output pin for the I2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIh.
	TXDX12	Output	Output pin for data transmission by SCIh.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIh.
I2C bus interface	SCL	I/O	Input/output pin for I2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA	I/O	Input/output pin for I2C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
CAN module	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
12-bit A/D converter	AN000 to AN007	Input	Analog input pins for the 12-bit A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
16-bit D/A converter	DA0	Output	Output pins for the analog signals to be processed by the 16-bit D/A converter. When not using a 16-bit D/A converter, leave this pin open-circuit.
Analog front end	REF0P, REF1P	Input	Positive input pins of the reference voltage for the 24-bit delta-sigma A/D converter.
	REF0N, REF1N	Input	Negative input pins of the reference voltage for the 24-bit delta-sigma A/D converter.
	REFOUT	Output	Internal reference voltage output pin. Connect this to AVSS0 via a capacitor (0.47 µF) for stabilizing the internal reference voltage. Place the capacitor close to the pin.
	IEXC0, IEXC1	Output	Excitation current source output pins.
	AIN0, AIN1, AIN4 to AIN7, AIN11 to AIN15	Input	Analog input pins
	AIN2, AIN3, AIN8 to AIN10	I/O	Analog input/output pins
	HVAIN0 to HVAIN3	Input	High-voltage (up to ±10-V) analog input pins
	HVCOM	Input	Ground pin for high-voltage analog inputs
	LSW	Output	Low-side-switch output pin.
Analog power supply	AVCC0	Input	Analog voltage supply pin. Connect this pin to VCC when not using analog functions.
	AVSS0	Input	Analog ground pin. Connect this pin to VSS when not using analog functions.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
	VREFH	Input	Analog reference voltage supply pin for the 16-bit D/A converter. When not using a 16-bit D/A converter , leave this pin open-circuit.
	VREFL	Input	Analog reference ground pin for the 16-bit D/A converter. When not using a 16-bit D/A converter, connect to AVSS0 or connect to AVSS0 via a resistor.
LCD	VL1, VL2, VL3, VL4	I/O	Voltage pins for driving the LCD.
	CAPH, CAPL	I/O	Capacitor connection pins for the LCD controller/driver.
	COM0 to COM7	Output	Common signal output pins for the LCD controller/driver.
	SEG00 to SEG39	Output	Segment signal output pins for the LCD controller/driver.
I/O ports	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30, P31, P35 to P37	I/O	5-bit input/output pins (P35 input pin).
	P54, P55	I/O	2-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P74	I/O	5-bit input/output pins.
	PA0 to PA4	I/O	5-bit input/output pins.
	PB0, PB1	I/O	2-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD4	I/O	5-bit input/output pins.
	PE0 to PE4	I/O	5-bit input/output pins.

1.5 Pin Assignments

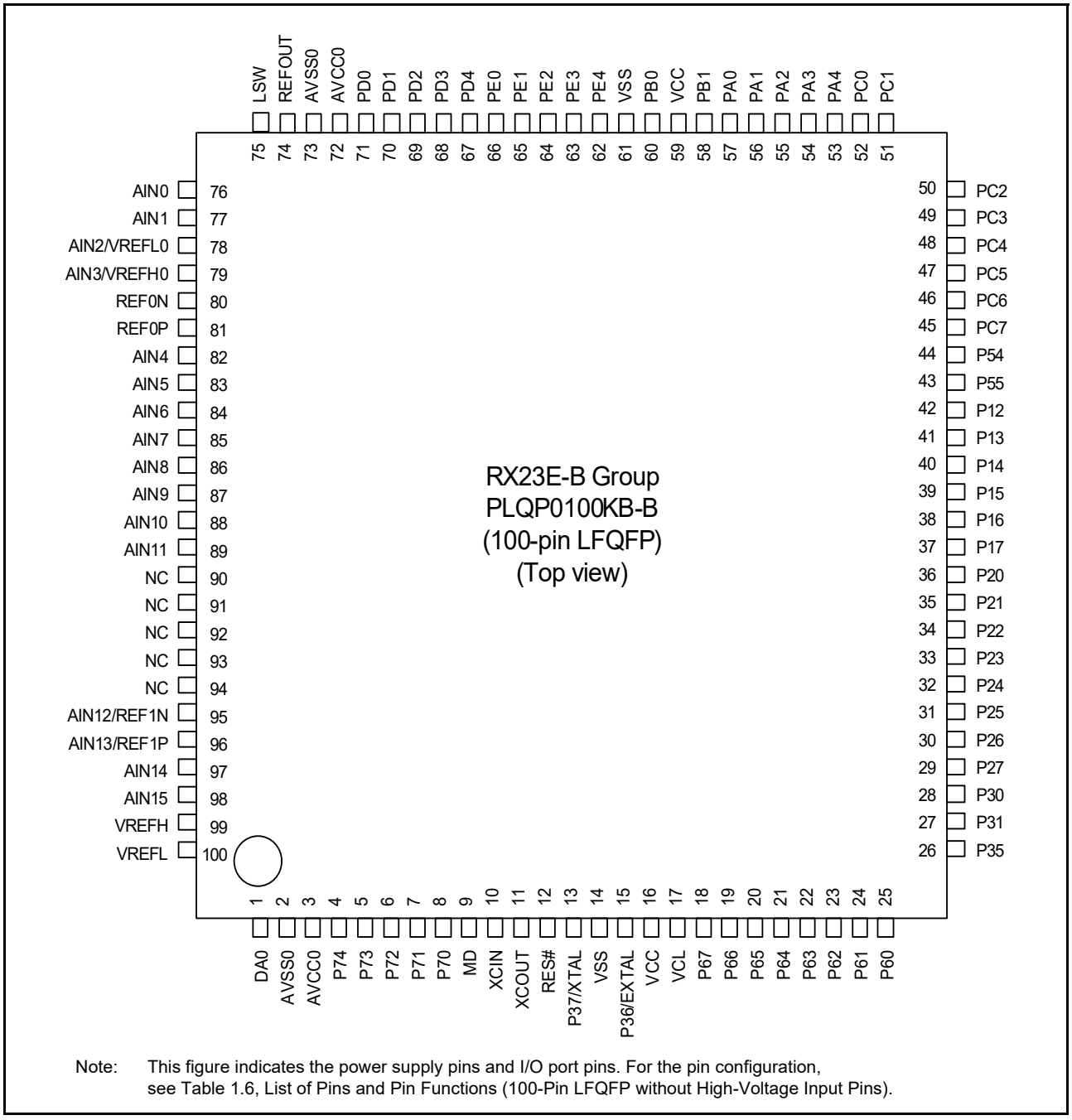
1.5.1 100-Pin LFQFP with High-Voltage Input Pins



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (100-Pin LFQFP with High-Voltage Input Pins).

Figure 1.3 Pin Assignments of the 100-Pin LFQFP with High-Voltage Input Pins

1.5.2 100-Pin LFQFP without High-Voltage Input Pins



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (100-Pin LFQFP without High-Voltage Input Pins).

Figure 1.4 Pin Assignments of the 100-Pin LFQFP without High-Voltage Input Pins

1.5.3 100-Pin TFBGA with High-Voltage Input Pins

RX23E-B Group
100-pin TFBGA)
(Upper Perspective View)

	A	B	C	D	E	F	G	H	J	K	
10	AIN0	LSW	REFOUT	AVSS0	AVCC0	VSS	VCC	PA1	PA4	PC1	10
9	AIN1	AIN2/ VREFL0	AIN4	PD1	PE0	PE4	PB0	PA2	PC0	PC2	9
8	REF0N	AIN3/ VREFH0	AIN5	PD0	PD4	PE3	PB1	PA3	PC3	PC4	8
7	REF0P	AIN6	AIN7	AIN8	PD3	PE2	PA0	PC5	PC6	PC7	7
6	AIN10	AIN11	HVCOM	AIN9	PD2	PE1	P54	P55	P12	P13	6
5	HVAIN0	HVAIN1	HVAIN2	HVAIN3	P21	P20	P14	P15	P16	P17	5
4	AIN12/ REF1N	AIN14	P72	P71	P27	P26	P25	P24	P23	P22	4
3	AIN13/ REF1P	AIN15	P73	P70	MD	VCC	P66	P63	P31	P30	3
2	VREFH	DA0	P74	XCIN	RES#	VSS	P67	P64	P61	P35	2
1	VREFL	AVSS0	AVCC0	XCOUT	P37/XTAL	P36/EXTAL	VCL	P65	P62	P60	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (100-Pin TFBGA with High-Voltage Input Pins).
Note: For the position of A1 pin in the package, see .Appendix 1., Package Dimensions

Figure 1.5 Pin Assignments of the 100-Pin TFBGA with High-Voltage Input Pins

1.5.4 100-Pin TFBGA without High-Voltage Input Pins

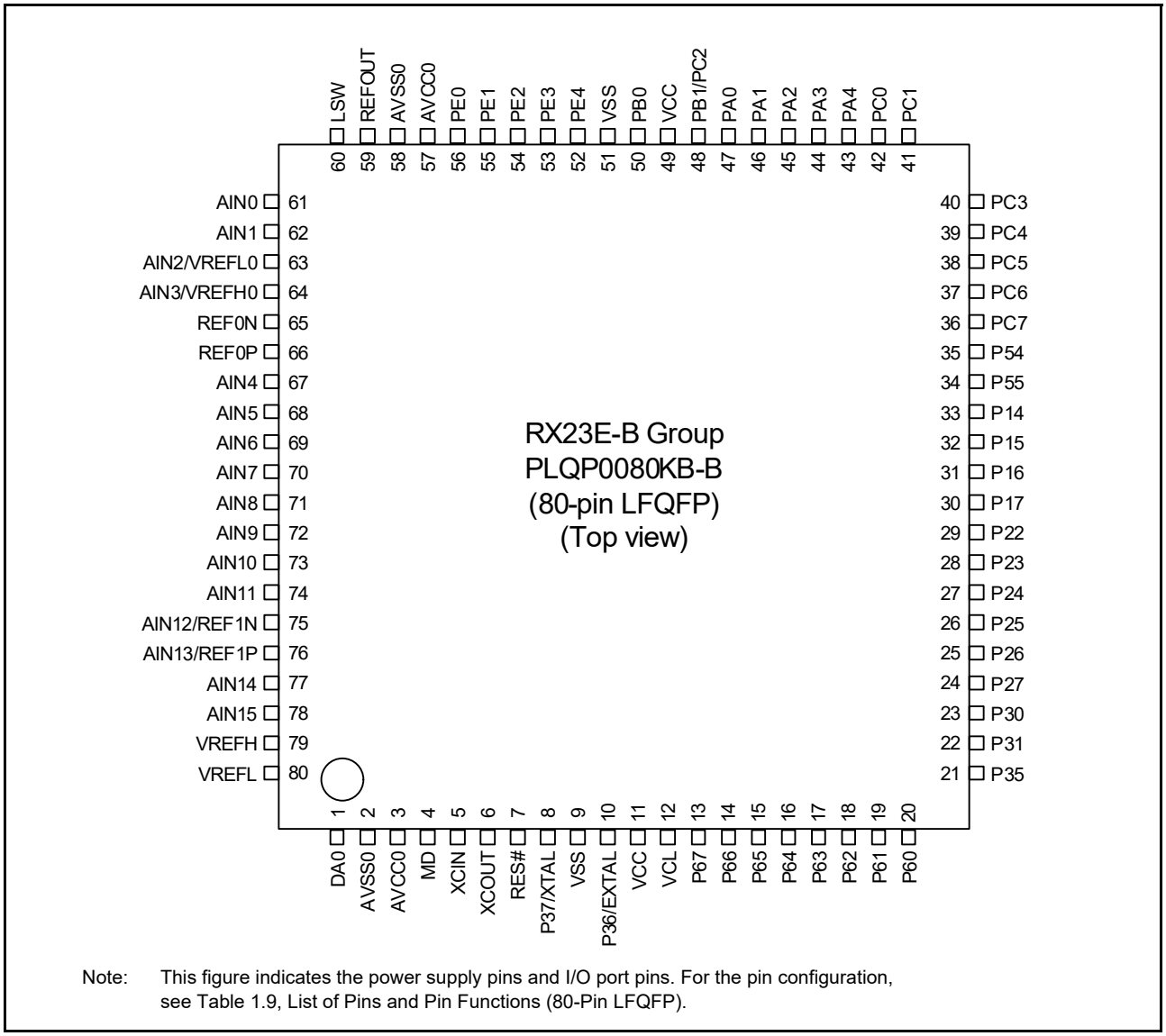
RX23E-B Group
100-pin TFBGA)
(Upper Perspective View)

	A	B	C	D	E	F	G	H	J	K	
10	AIN0	LSW	REFOUT	AVSS0	AVCC0	VSS	VCC	PA1	PA4	PC1	10
9	AIN1	AIN2/ VREFL0	AIN4	PD1	PE0	PE4	PB0	PA2	PC0	PC2	9
8	REF0N	AIN3/ VREFH0	AIN5	PD0	PD4	PE3	PB1	PA3	PC3	PC4	8
7	REF0P	AIN6	AIN7	AIN8	PD3	PE2	PA0	PC5	PC6	PC7	7
6	AIN10	AIN11	NC	AIN9	PD2	PE1	P54	P55	P12	P13	6
5	NC	NC	NC	NC	P21	P20	P14	P15	P16	P17	5
4	AIN12/ REF1N	AIN14	P72	P71	P27	P26	P25	P24	P23	P22	4
3	AIN13/ REF1P	AIN15	P73	P70	MD	VCC	P66	P63	P31	P30	3
2	VREFH	DA0	P74	XCIN	RES#	VSS	P67	P64	P61	P35	2
1	VREFL	AVSS0	AVCC0	XCOUT	P37/XTAL	P36/EXTAL	VCL	P65	P62	P60	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pins and Pin Functions (100-Pin TFBGA without High-Voltage Input Pins).
Note: For the position of A1 pin in the package, see Appendix 1., Package Dimensions.

Figure 1.6 Pin Assignments of the 100-Pin TFBGA without High-Voltage Input Pins

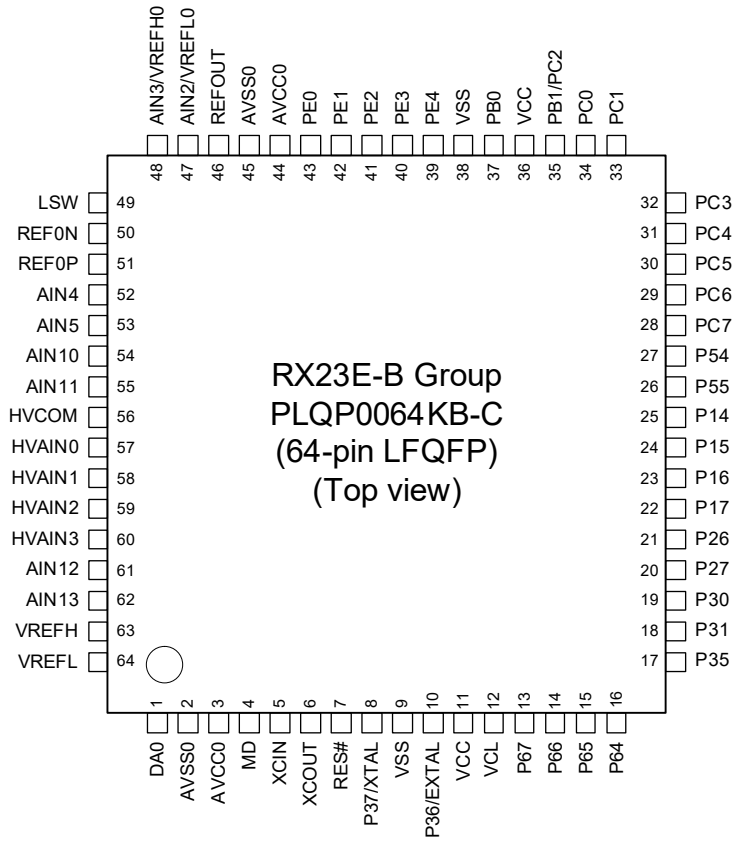
1.5.5 80-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pins and Pin Functions (80-Pin LFQFP).

Figure 1.7 Pin Assignments of the 80-Pin LFQFP

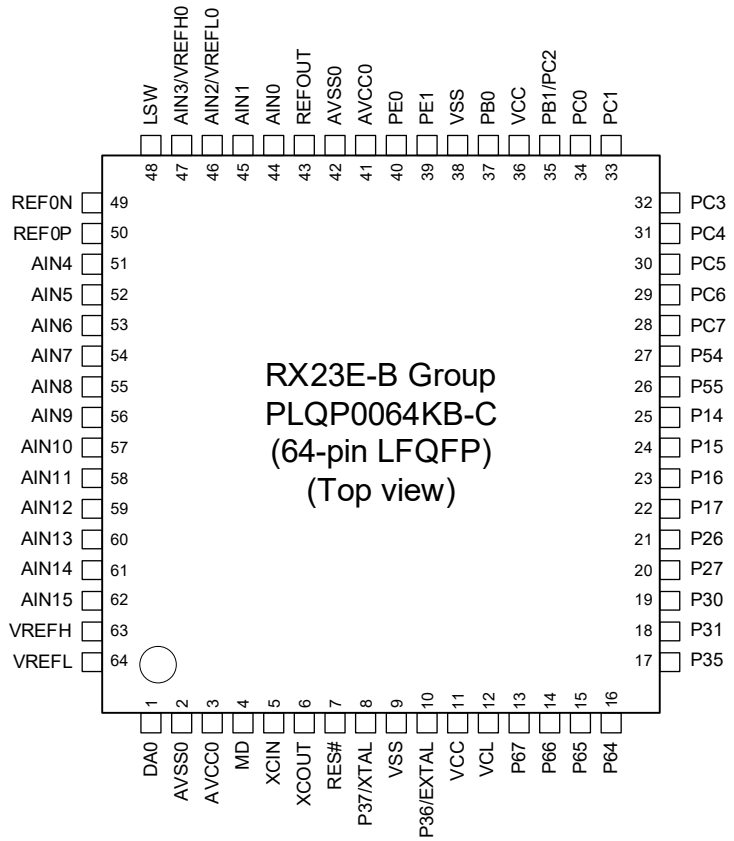
1.5.6 64-Pin LFQFP with High-Voltage Input Pins



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (64-Pin LFQFP with High-Voltage Input Pins).

Figure 1.8 Pin Assignments of the 64-Pin LFQFP with High-Voltage Input Pins

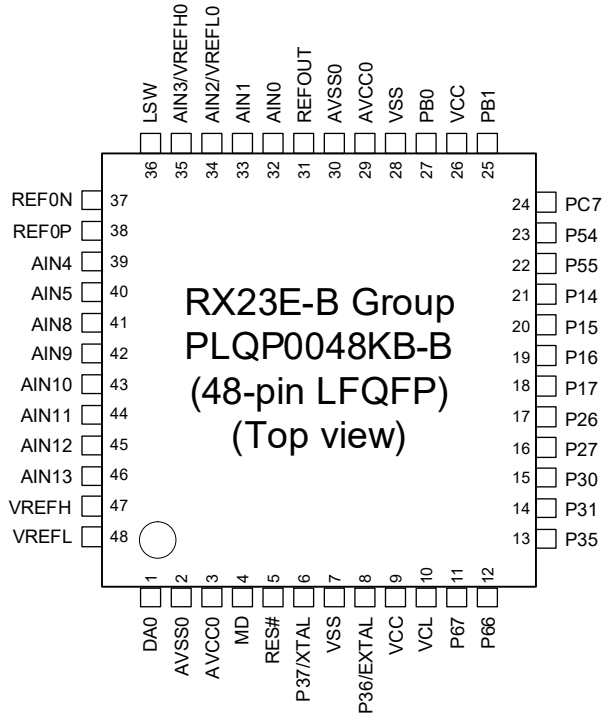
1.5.7 64-Pin LFQFP without High-Voltage Input Pins



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.11, List of Pins and Pin Functions (64-Pin LFQFP without High-Voltage Input Pins).

Figure 1.9 Pin Assignments of the 64-Pin LFQFP without High-Voltage Input Pins

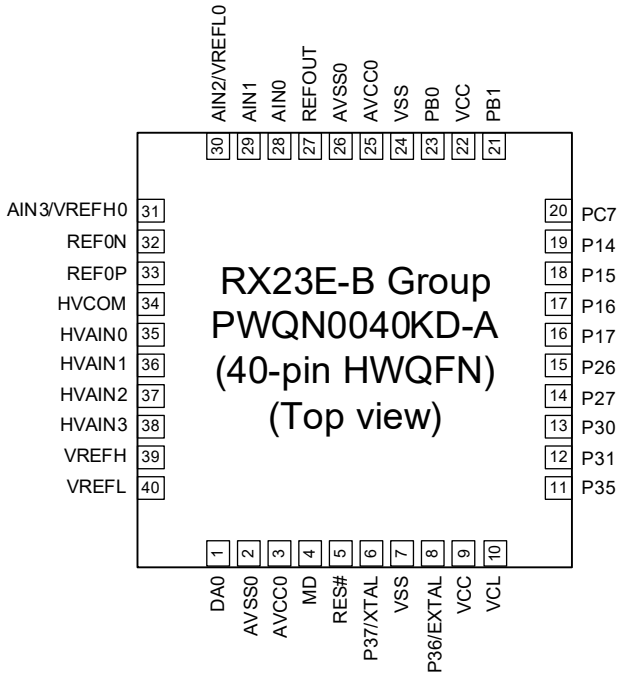
1.5.8 48-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.12, List of Pins and Pin Functions (48-Pin LFQFP).

Figure 1.10 Pin Assignments of the 48-Pin LFQFP

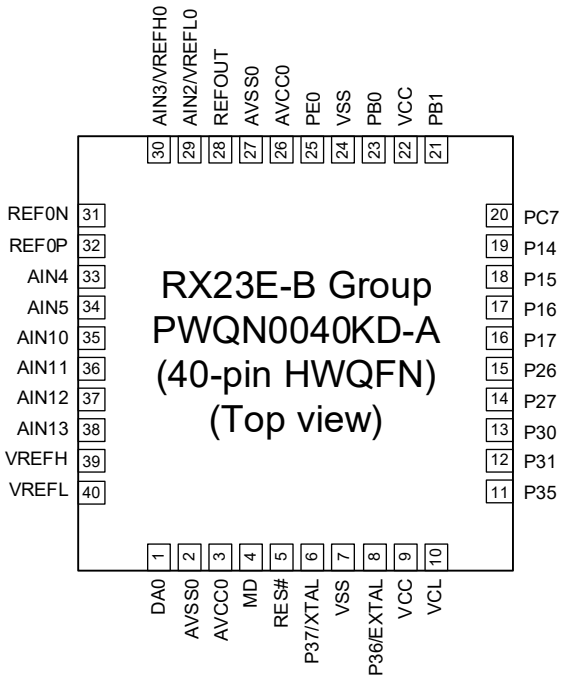
1.5.9 40-Pin HWQFN with High-Voltage Input Pins



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.13, List of Pins and Pin Functions (40-Pin HWQFN with High-Voltage Input Pins).
Note: It is recommended to connect an exposed die pad to VSS.

Figure 1.11 Pin Assignments of the 40-Pin HWQFN with High-Voltage Input Pins

1.5.10 40-Pin HWQFN without High-Voltage Input Pins



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.14, List of Pins and Pin Functions (40-Pin HWQFN without High-Voltage Input Pins).
Note: It is recommended to connect an exposed die pad to VSS.

Figure 1.12 Pin Assignments of the 40-Pin HWQFN without High-Voltage Input Pins

1.6 List of Pins and Pin Functions

1.6.1 100-Pin LFQFP with High-Voltage Input Pins

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP with High-Voltage Input Pins) (1/3)

Pin No. 100-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1						DA0	
2	AVSS0						
3	AVCC0						
4		P74	TMO3/CACREF	SDA			
5		P73	MTIOC3A/TMCI3	CTS0#/RTS0#/SS0#/ SSLA0/SCL			IRQ3
6		P72	MTIOC3C/TMRI3	TXD0/SMOSI0/SSDA0/ MISOA			IRQ2
7		P71	MTIOC3B/MTCLKD	RXD0/SMISO0/SSCL0/ MOSIA			IRQ1
8		P70	MTIOC3D/MTCLKC	SCK0/RSPCKA		CLKOUT	IRQ0
9	MD						FINED
10	XCIN						
11	XCOUT						
12	RES#						
13	XTAL	P37					
14	VSS						
15	EXTAL	P36					
16	VCC						
17	VCL						
18		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6	CAPH		
19		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6	CAPL		
20		P65	MTIOC4B/MTCLKD/ TMO2/POE0#	CTS6#/RTS6#/SS6#	VL1		
21		P64	MTIOC4D/MTCLKC/ RTCOUT	SCK6	VL2	ADTRG0#	
22		P63	MTIOC0A/MTIOC1A/ MTCLKB	SCK8	VL3		
23		P62	MTIOC0C/MTIOC1B/ MTCLKA/TMO1	CTS8#/RTS8#/SS8#	VL4		
24		P61	MTIOC0B/TMCI1	TXD8/SMOSI8/SSDA8/ MISOA/SDA	SEG00		
25		P60	MTIOC0D/TMRI1	RXD8/SMISO8/SSCL8/ MOSIA/SCL	SEG01		
26		P35					NMI
27		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA	SEG02		IRQ1
28		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5	SEG03		IRQ0
29		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#	SEG04		IRQ3
30		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12	SEG05		IRQ2
31		P25	TMCI0	TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	SEG06		IRQ7
32		P24	MTIC5U/TMRI0	RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12	SEG07		IRQ6
33		P23	MTIC5V	CTS9#/RTS9#/SS9#	SEG08		IRQ5
34		P22	MTIC5W	SCK9	SEG09		IRQ4
35		P21	MTIOC1A/RTCOUT	CTS12#/RTS12#/SS12#	SEG10		
36		P20	MTIOC1B	SCK12/RSPCKA	SEG11		

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP with High-Voltage Input Pins) (2/3)

Pin No. 100-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
37		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA	SEG12		IRQ7
38		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	SEG13	ADTRG0#	IRQ6
39		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0	SEG14		IRQ5
40		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	SEG15	CLKOUT	IRQ4
41		P13	MTIOC2A	TXD6/SMOSI6/SSDA6	SEG16		
42		P12	MTIOC2B	RXD6/SMISO6/SSCL6	SEG17		
43		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#	SEG18		
44		P54	MTIC5V/TMRI0	SCK6/SSLA3	SEG19		
45		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1	SEG20		IRQ7
46		PC6	MTIOC4A/POE1#	RXD1/SMISO1/SSCL1	SEG21		IRQ6
47		PC5	MTIOC4C/POE2#	TXD8/SMOSI8/SSDA8	SEG22		IRQ5
48		PC4	MTIOC4B/POE3#	RXD8/SMISO8/SSCL8	SEG23		IRQ4
49		PC3	MTIOC4D/POE8#	CTS8#/RTS8#/SS8#	SEG24		IRQ3
50		PC2		CTS1#/RTS1#/SS1#/ SCK8	SEG25		IRQ2
51		PC1	TMO0	SCK1/SCK8/CRXD0	COM0		IRQ1
52		PC0	MTIOC4A/MTIC5U/ TMCI0	TXD1/SMOSI1/SSDA1/ CTXD0	COM1		IRQ0
53		PA4	MTIOC2A/MTIOC4A	MISOA	COM2		
54		PA3	MTIOC2B/MTIOC4C	TXD9/SMOSI9/SSDA9/ MOSIA	COM3		
55		PA2	MTIOC4B/TMO2	RXD9/SMISO9/SSCL9/ SSLA0	SEG26/COM4		
56		PA1	MTIOC4D/TMCI2	CTS9#/RTS9#/SS9#/ SSLA1	SEG27/COM5		
57		PA0	TMRI2/RTCOUT	SCK9/SSLA3	SEG28/COM6		
58		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2	SEG29/COM7		
59	VCC						
60		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	SEG30	CMPA2	
61	VSS						
62		PE4	MTIOC3A/MTCLKB/ TMO3	TXD5/SMOSI5/SSDA5/ SSLA2	SEG31		IRQ7
63		PE3	MTIOC3C/MTCLKA/ TMCI3	RXD5/SMISO5/SSCL5	SEG32		IRQ6
64		PE2	MTIOC3B/MTCLKD/ TMRI3	CTS5#/RTS5#/SS5#	SEG33		IRQ5
65		PE1	MTIOC3D/MTCLKC	SCK5	SEG34		IRQ4
66		PE0	MTCLKA/CACREF	SSLA3	SEG35		
67		PD4	MTIOC0A/TMO1/POE0#	TXD0/SMOSI0/SSDA0	SEG36		
68		PD3	MTIOC0D/TMCI1/POE1#	RXD0/SMISO0/SSCL0	SEG37		
69		PD2	MTIOC0C/TMRI1/POE2#	CTS0#/RTS0#/SS0#	SEG38		
70		PD1	MTIOC0B/POE3#	SCK0	SEG39		
71		PD0	POE8#			ADTRG0#	
72	AVCC0						
73	AVSS0						
74						REFOUT	
75						LSW	
76						AIN0/AN000	

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP with High-Voltage Input Pins) (3/3)

Pin No. 100-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
77						AIN1/AN001	
78	VREFL0					AIN2/IEXC0/VBIAS	
79	VREFH0					AIN3/IEXC1	
80						REF0N	
81						REF0P	
82						AIN4/AN002	
83						AIN5/AN003	
84						AIN6	
85						AIN7	
86						AIN8/IEXC0	
87						AIN9/IEXC1	
88						AIN10/AN004/VBIAS	
89						AIN11/AN005	
90						HVCOM	
91						HVAIN0	
92						HVAIN1	
93						HVAIN2	
94						HVAIN3	
95						AIN12/AN006/REF1N	
96						AIN13/AN007/REF1P	
97						AIN14	
98						AIN15	
99	VREFH						
100	VREFL						

1.6.2 100-Pin LFQFP without High-Voltage Input Pins

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP without High-Voltage Input Pins) (1/3)

Pin No. 100-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1						DA0	
2	AVSS0						
3	AVCC0						
4		P74	TMO3/CACREF	SDA			
5		P73	MTIOC3A/TMCI3	CTS0#/RTS0#/SS0#/ SSLA0/SCL			IRQ3
6		P72	MTIOC3C/TMRI3	TXD0/SMOSI0/SSDA0/ MISOA			IRQ2
7		P71	MTIOC3B/MTCLKD	RXD0/SMISO0/SSCL0/ MOSIA			IRQ1
8		P70	MTIOC3D/MTCLKC	SCK0/RSPCKA		CLKOUT	IRQ0
9	MD						FINED
10	XCIN						
11	XCOUT						
12	RES#						
13	XTAL	P37					
14	VSS						
15	EXTAL	P36					
16	VCC						
17	VCL						
18		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6	CAPH		
19		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6	CAPL		
20		P65	MTIOC4B/MTCLKD/ TMO2/POE0#	CTS6#/RTS6#/SS6#	VL1		
21		P64	MTIOC4D/MTCLKC/ RTCOUT	SCK6	VL2	ADTRG0#	
22		P63	MTIOC0A/MTIOC1A/ MTCLKB	SCK8	VL3		
23		P62	MTIOC0C/MTIOC1B/ MTCLKA/TMO1	CTS8#/RTS8#/SS8#	VL4		
24		P61	MTIOC0B/TMCI1	TXD8/SMOSI8/SSDA8/ MISOA/SDA	SEG00		
25		P60	MTIOC0D/TMRI1	RXD8/SMISO8/SSCL8/ MOSIA/SCL	SEG01		
26		P35					NMI
27		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA	SEG02		IRQ1
28		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5	SEG03		IRQ0
29		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#	SEG04		IRQ3
30		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12	SEG05		IRQ2
31		P25	TMCI0	TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	SEG06		IRQ7
32		P24	MTIC5U/TMRI0	RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12	SEG07		IRQ6
33		P23	MTIC5V	CTS9#/RTS9#/SS9#	SEG08		IRQ5
34		P22	MTIC5W	SCK9	SEG09		IRQ4
35		P21	MTIOC1A/RTCOUT	CTS12#/RTS12#/SS12#	SEG10		
36		P20	MTIOC1B	SCK12/RSPCKA	SEG11		
37		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA	SEG12		IRQ7

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP without High-Voltage Input Pins) (2/3)

Pin No. 100-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
38		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	SEG13	ADTRG0#	IRQ6
39		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0	SEG14		IRQ5
40		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	SEG15	CLKOUT	IRQ4
41		P13	MTIOC2A	TXD6/SMOSI6/SSDA6	SEG16		
42		P12	MTIOC2B	RXD6/SMISO6/SSCL6	SEG17		
43		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#	SEG18		
44		P54	MTIC5V/TMRI0	SCK6/SSLA3	SEG19		
45		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1	SEG20		IRQ7
46		PC6	MTIOC4A/POE1#	RXD1/SMISO1/SSCL1	SEG21		IRQ6
47		PC5	MTIOC4C/POE2#	TXD8/SMOSI8/SSDA8	SEG22		IRQ5
48		PC4	MTIOC4B/POE3#	RXD8/SMISO8/SSCL8	SEG23		IRQ4
49		PC3	MTIOC4D/POE8#	CTS8#/RTS8#/SS8#	SEG24		IRQ3
50		PC2		CTS1#/RTS1#/SS1#/ SCK8	SEG25		IRQ2
51		PC1	TMO0	SCK1/SCK8/CRXD0	COM0		IRQ1
52		PC0	MTIOC4A/MTIC5U/ TMCI0	TXD1/SMOSI1/SSDA1/ CTXD0	COM1		IRQ0
53		PA4	MTIOC2A/MTIOC4A	MISOA	COM2		
54		PA3	MTIOC2B/MTIOC4C	TXD9/SMOSI9/SSDA9/ MOSIA	COM3		
55		PA2	MTIOC4B/TMO2	RXD9/SMISO9/SSCL9/ SSLA0	SEG26/COM4		
56		PA1	MTIOC4D/TMCI2	CTS9#/RTS9#/SS9#/ SSLA1	SEG27/COM5		
57		PA0	TMRI2/RTCOUT	SCK9/SSLA3	SEG28/COM6		
58		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2	SEG29/COM7		
59	VCC						
60		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	SEG30	CMPA2	
61	VSS						
62		PE4	MTIOC3A/MTCLKB/ TMO3	TXD5/SMOSI5/SSDA5/ SSLA2	SEG31		IRQ7
63		PE3	MTIOC3C/MTCLKA/ TMCI3	RXD5/SMISO5/SSCL5	SEG32		IRQ6
64		PE2	MTIOC3B/MTCLKD/ TMRI3	CTS5#/RTS5#/SS5#	SEG33		IRQ5
65		PE1	MTIOC3D/MTCLKC	SCK5	SEG34		IRQ4
66		PE0	MTCLKA/CACREF	SSLA3	SEG35		
67		PD4	MTIOC0A/TMO1/POE0#	TXD0/SMOSI0/SSDA0	SEG36		
68		PD3	MTIOC0D/TMCI1/POE1#	RXD0/SMISO0/SSCL0	SEG37		
69		PD2	MTIOC0C/TMRI1/POE2#	CTS0#/RTS0#/SS0#	SEG38		
70		PD1	MTIOC0B/POE3#	SCK0	SEG39		
71		PD0	POE8#			ADTRG0#	
72	AVCC0						
73	AVSS0						
74						REFOUT	
75						LSW	
76						AIN0/AN000	
77						AIN1/AN001	
78	VREFL0					AIN2/IEXC0/VBIAS	

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP without High-Voltage Input Pins) (3/3)

Pin No. 100-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
79	VREFH0					AIN3/IEXC1	
80						REF0N	
81						REF0P	
82						AIN4/AN002	
83						AIN5/AN003	
84						AIN6	
85						AIN7	
86						AIN8/IEXC0	
87						AIN9/IEXC1	
88						AIN10/AN004/VBIAS	
89						AIN11/AN005	
90	NC						
91	NC						
92	NC						
93	NC						
94	NC						
95						AIN12/AN006/REF1N	
96						AIN13/AN007/REF1P	
97						AIN14	
98						AIN15	
99	VREFH						
100	VREFL						

1.6.3 100-Pin TFBGA with High-Voltage Input Pins

Table 1.7 List of Pins and Pin Functions (100-Pin TFBGA with High-Voltage Input Pins) (1/3)

Pin No. 100-Pin TFBGA	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
A1	VREFL						
A2	VREFH						
A3						AIN13/AN007/REF1P	
A4						AIN12/AN006/REF1N	
A5						HVAIN0	
A6						AIN10/AN004/VBIAS	
A7						REF0P	
A8						REF0N	
A9						AIN1/AN001	
A10						AIN0/AN000	
B1	AVSS0						
B2						DA0	
B3						AIN15	
B4						AIN14	
B5						HVAIN1	
B6						AIN11/AN005	
B7						AIN6	
B8	VREFH0					AIN3/IEXC1	
B9	VREFL0					AIN2/IEXC0/VBIAS	
B10						LSW	
C1	AVCC0						
C2		P74	TMO3/CACREF	SDA			
C3		P73	MTIOC3A/TMCI3	CTS0#/RTS0#/SS0#/ SSLA0/SCL			IRQ3
C4		P72	MTIOC3C/TMRI3	TXD0/SMOSI0/SSDA0/ MISOA			IRQ2
C5						HVAIN2	
C6						HVCOM	
C7						AIN7	
C8						AIN5/AN003	
C9						AIN4/AN002	
C10						REFOUT	
D1	XCOUT						
D2	XCIN						
D3		P70	MTIOC3D/MTCLKC	SCK0/RSPCKA		CLKOUT	IRQ0
D4		P71	MTIOC3B/MTCLKD	RXD0/SMISO0/SSCL0/ MOSIA			IRQ1
D5						HVAIN3	
D6						AIN9/IEXC1	
D7						AIN8/IEXC0	
D8		PD0	POE8#			ADTRG0#	
D9		PD1	MTIOC0B/POE3#	SCK0	SEG39		
D10	AVSS0						
E1	XTAL	P37					
E2	RES#						
E3	MD						FINED
E4		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#	SEG04		IRQ3
E5		P21	MTIOC1A/RTCOUT	CTS12#/RTS12#/SS12#	SEG10		
E6		PD2	MTIOC0C/TMRI1/POE2#	CTS0#/RTS0#/SS0#	SEG38		
E7		PD3	MTIOC0D/TMCI1/POE1#	RXD0/SMISO0/SSCL0	SEG37		
E8		PD4	MTIOC0A/TMO1/POE0#	TXD0/SMOSI0/SSDA0	SEG36		

Table 1.7 List of Pins and Pin Functions (100-Pin TFBGA with High-Voltage Input Pins) (2/3)

Pin No. 100-Pin TFBGA	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
E9		PE0	MTCLKA/CACREF	SSLA3	SEG35		
E10	AVCC0						
F1	EXTAL	P36					
F2	VSS						
F3	VCC						
F4		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12	SEG05		IRQ2
F5		P20	MTIOC1B	SCK12/RSPCKA	SEG11		
F6		PE1	MTIOC3D/MTCLKC	SCK5	SEG34		IRQ4
F7		PE2	MTIOC3B/MTCLKD/ TMRI3	CTS5#/RTS5#/SS5#	SEG33		IRQ5
F8		PE3	MTIOC3C/MTCLKA/ TMCI3	RXD5/SMISO5/SSCL5	SEG32		IRQ6
F9		PE4	MTIOC3A/MTCLKB/ TMO3	TXD5/SMOSI5/SSDA5/ SSLA2	SEG31		IRQ7
F10	VSS						
G1	VCL						
G2		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6	CAPH		
G3		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6	CAPL		
G4		P25	TMCI0	TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	SEG06		IRQ7
G5		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	SEG15	CLKOUT	IRQ4
G6		P54	MTIC5V/TMRI0	SCK6/SSLA3	SEG19		
G7		PA0	TMRI2/RTCOUT	SCK9/SSLA3	SEG28/COM6		
G8		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2	SEG29/COM7		
G9		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	SEG30	CMPA2	
G10	VCC						
H1		P65	MTIOC4B/MTCLKD/ TMO2/POE0#	CTS6#/RTS6#/SS6#	VL1		
H2		P64	MTIOC4D/MTCLKC/ RTCOUT	SCK6	VL2	ADTRG0#	
H3		P63	MTIOC0A/MTIOC1A/ MTCLKB	SCK8	VL3		
H4		P24	MTIC5U/TMRI0	RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12	SEG07		IRQ6
H5		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0	SEG14		IRQ5
H6		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#	SEG18		
H7		PC5	MTIOC4C/POE2#	TXD8/SMOSI8/SSDA8	SEG22		IRQ5
H8		PA3	MTIOC2B/MTIOC4C	TXD9/SMOSI9/SSDA9/ MOSIA	COM3		
H9		PA2	MTIOC4B/TMO2	RXD9/SMISO9/SSCL9/ SSLA0	SEG26/COM4		
H10		PA1	MTIOC4D/TMCI2	CTS9#/RTS9#/SS9#/ SSLA1	SEG27/COM5		
J1		P62	MTIOC0C/MTIOC1B/ MTCLKA/TMO1	CTS8#/RTS8#/SS8#	VL4		
J2		P61	MTIOC0B/TMCI1	TXD8/SMOSI8/SSDA8/ MISOA/SDA	SEG00		
J3		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA	SEG02		IRQ1
J4		P23	MTIC5V	CTS9#/RTS9#/SS9#	SEG08		IRQ5

Table 1.7 List of Pins and Pin Functions (100-Pin TFBGA with High-Voltage Input Pins) (3/3)

Pin No. 100-Pin TFBGA	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
J5		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	SEG13	ADTRG0#	IRQ6
J6		P12	MTIOC2B	RXD6/SMISO6/SSCL6	SEG17		
J7		PC6	MTIOC4A/POE1#	RXD1/SMISO1/SSCL1	SEG21		IRQ6
J8		PC3	MTIOC4D/POE8#	CTS8#/RTS8#/SS8#	SEG24		IRQ3
J9		PC0	MTIOC4A/MTIC5U/ TMCI0	TXD1/SMOSI1/SSDA1/ CTXD0	COM1		IRQ0
J10		PA4	MTIOC2A/MTIOC4A	MISOA	COM2		
K1		P60	MTIOC0D/TMRI1	RXD8/SMISO8/SSCL8/ MOSIA/SCL	SEG01		
K2		P35					NMI
K3		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5	SEG03		IRQ0
K4		P22	MTIC5W	SCK9	SEG09		IRQ4
K5		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA	SEG12		IRQ7
K6		P13	MTIOC2A	TXD6/SMOSI6/SSDA6	SEG16		
K7		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1	SEG20		IRQ7
K8		PC4	MTIOC4B/POE3#	RXD8/SMISO8/SSCL8	SEG23		IRQ4
K9		PC2		CTS1#/RTS1#/SS1#/ SCK8	SEG25		IRQ2
K10		PC1	TMO0	SCK1/SCK8/CRXD0	COM0		IRQ1

1.6.4 100-Pin TFBGA without High-Voltage Input Pins

Table 1.8 List of Pins and Pin Functions (100-Pin TFBGA without High-Voltage Input Pins) (1/3)

Pin No. 100-Pin TFBGA	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
A1	VREFL						
A2	VREFH						
A3						AIN13/AN007/REF1P	
A4						AIN12/AN006/REF1N	
A5	NC						
A6						AIN10/AN004/VBIAS	
A7						REF0P	
A8						REF0N	
A9						AIN1/AN001	
A10						AIN0/AN000	
B1	AVSS0						
B2						DA0	
B3						AIN15	
B4						AIN14	
B5	NC						
B6						AIN11/AN005	
B7						AIN6	
B8	VREFH0					AIN3/IEXC1	
B9	VREFL0					AIN2/IEXC0/VBIAS	
B10						LSW	
C1	AVCC0						
C2		P74	TMO3/CACREF	SDA			
C3		P73	MTIOC3A/TMCI3	CTS0#/RTS0#/SS0#/ SSLA0/SCL			IRQ3
C4		P72	MTIOC3C/TMRI3	TXD0/SMOSI0/SSDA0/ MISOA			IRQ2
C5	NC						
C6	NC						
C7						AIN7	
C8						AIN5/AN003	
C9						AIN4/AN002	
C10						REFOUT	
D1	XCOUT						
D2	XCIN						
D3		P70	MTIOC3D/MTCLKC	SCK0/RSPCKA		CLKOUT	IRQ0
D4		P71	MTIOC3B/MTCLKD	RXD0/SMISO0/SSCL0/ MOSIA			IRQ1
D5	NC						
D6						AIN9/IEXC1	
D7						AIN8/IEXC0	
D8		PD0	POE8#			ADTRG0#	
D9		PD1	MTIOC0B/POE3#	SCK0	SEG39		
D10	AVSS0						
E1	XTAL	P37					
E2	RES#						
E3	MD						FINED
E4		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#	SEG04		IRQ3
E5		P21	MTIOC1A/RTCOUT	CTS12#/RTS12#/SS12#	SEG10		
E6		PD2	MTIOC0C/TMRI1/POE2#	CTS0#/RTS0#/SS0#	SEG38		
E7		PD3	MTIOC0D/TMCI1/POE1#	RXD0/SMISO0/SSCL0	SEG37		

Table 1.8 List of Pins and Pin Functions (100-Pin TFBGA without High-Voltage Input Pins) (2/3)

Pin No. 100-Pin TFBGA	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
E8		PD4	MTIOC0A/TMO1/POE0#	TXD0/SMOSI0/SSDA0	SEG36		
E9		PE0	MTCLKA/CACREF	SSLA3	SEG35		
E10	AVCC0						
F1	EXTAL	P36					
F2	VSS						
F3	VCC						
F4		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12	SEG05		IRQ2
F5		P20	MTIOC1B	SCK12/RSPCKA	SEG11		
F6		PE1	MTIOC3D/MTCLKC	SCK5	SEG34		IRQ4
F7		PE2	MTIOC3B/MTCLKD/ TMRI3	CTS5#/RTS5#/SS5#	SEG33		IRQ5
F8		PE3	MTIOC3C/MTCLKA/ TMCI3	RXD5/SMISO5/SSCL5	SEG32		IRQ6
F9		PE4	MTIOC3A/MTCLKB/ TMO3	TXD5/SMOSI5/SSDA5/ SSLA2	SEG31		IRQ7
F10	VSS						
G1	VCL						
G2		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6	CAPH		
G3		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6	CAPL		
G4		P25	TMCI0	TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	SEG06		IRQ7
G5		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	SEG15	CLKOUT	IRQ4
G6		P54	MTIC5V/TMRI0	SCK6/SSLA3	SEG19		
G7		PA0	TMRI2/RTCOUT	SCK9/SSLA3	SEG28/COM6		
G8		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2	SEG29/COM7		
G9		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	SEG30	CMPA2	
G10	VCC						
H1		P65	MTIOC4B/MTCLKD/ TMO2/POE0#	CTS6#/RTS6#/SS6#	VL1		
H2		P64	MTIOC4D/MTCLKC/ RTCOUT	SCK6	VL2	ADTRG0#	
H3		P63	MTIOC0A/MTIOC1A/ MTCLKB	SCK8	VL3		
H4		P24	MTIC5U/TMRI0	RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12	SEG07		IRQ6
H5		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0	SEG14		IRQ5
H6		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#	SEG18		
H7		PC5	MTIOC4C/POE2#	TXD8/SMOSI8/SSDA8	SEG22		IRQ5
H8		PA3	MTIOC2B/MTIOC4C	TXD9/SMOSI9/SSDA9/ MOSIA	COM3		
H9		PA2	MTIOC4B/TMO2	RXD9/SMISO9/SSCL9/ SSLA0	SEG26/COM4		
H10		PA1	MTIOC4D/TMCI2	CTS9#/RTS9#/SS9#/ SSLA1	SEG27/COM5		
J1		P62	MTIOC0C/MTIOC1B/ MTCLKA/TMO1	CTS8#/RTS8#/SS8#	VL4		
J2		P61	MTIOC0B/TMCI1	TXD8/SMOSI8/SSDA8/ MISOA/SDA	SEG00		
J3		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA	SEG02		IRQ1

Table 1.8 List of Pins and Pin Functions (100-Pin TFBGA without High-Voltage Input Pins) (3/3)

Pin No. 100-Pin TFBGA	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
J4		P23	MTIC5V	CTS9#/RTS9#/SS9#	SEG08		IRQ5
J5		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	SEG13	ADTRG0#	IRQ6
J6		P12	MTIOC2B	RXD6/SMISO6/SSCL6	SEG17		
J7		PC6	MTIOC4A/POE1#	RXD1/SMISO1/SSCL1	SEG21		IRQ6
J8		PC3	MTIOC4D/POE8#	CTS8#/RTS8#/SS8#	SEG24		IRQ3
J9		PC0	MTIOC4A/MTIC5U/ TMCI0	TXD1/SMOSI1/SSDA1/ CTXD0	COM1		IRQ0
J10		PA4	MTIOC2A/MTIOC4A	MISOA	COM2		
K1		P60	MTIOC0D/TMRI1	RXD8/SMISO8/SSCL8/ MOSIA/SCL	SEG01		
K2		P35					NMI
K3		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5	SEG03		IRQ0
K4		P22	MTIC5W	SCK9	SEG09		IRQ4
K5		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA	SEG12		IRQ7
K6		P13	MTIOC2A	TXD6/SMOSI6/SSDA6	SEG16		
K7		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1	SEG20		IRQ7
K8		PC4	MTIOC4B/POE3#	RXD8/SMISO8/SSCL8	SEG23		IRQ4
K9		PC2		CTS1#/RTS1#/SS1#/ SCK8	SEG25		IRQ2
K10		PC1	TMO0	SCK1/SCK8/CRXD0	COM0		IRQ1

1.6.5 80-Pin LFQFP

Table 1.9 List of Pins and Pin Functions (80-Pin LFQFP) (1/2)

Pin No. 80-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1						DA0	
2	AVSS0						
3	AVCC0						
4	MD						FINED
5	XCIN						
6	XCOUT						
7	RES#						
8	XTAL	P37					
9	VSS						
10	EXTAL	P36					
11	VCC						
12	VCL						
13		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6	CAPH		
14		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6	CAPL		
15		P65	MTIOC4B/MTCLKD/ TMO2/POE0#	CTS6#/RTS6#/SS6#	VL1		
16		P64	MTIOC4D/MTCLKC/ RTCOUT	SCK6	VL2	ADTRG0#	
17		P63	MTIOC0A/MTIOC1A/ MTCLKB	SCK8	VL3		
18		P62	MTIOC0C/MTIOC1B/ MTCLKA/TMO1	CTS8#/RTS8#/SS8#	VL4		
19		P61	MTIOC0B/TMCI1	TXD8/SMOSI8/SSDA8/ MISOA/SDA	SEG00		
20		P60	MTIOC0D/TMRI1	RXD8/SMISO8/SSCL8/ MOSIA/SCL	SEG01		
21		P35					NMI
22		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA	SEG02		IRQ1
23		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5	SEG03		IRQ0
24		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#	SEG04		IRQ3
25		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12	SEG05		IRQ2
26		P25	TMCI0	TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	SEG06		IRQ7
27		P24	MTIC5U/TMRI0	RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12	SEG07		IRQ6
28		P23	MTIC5V	CTS9#/RTS9#/SS9#	SEG08		IRQ5
29		P22	MTIC5W	SCK9	SEG09		IRQ4
30		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA	SEG12		IRQ7
31		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	SEG13	ADTRG0#	IRQ6
32		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0	SEG14		IRQ5
33		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	SEG15	CLKOUT	IRQ4
34		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#	SEG18		
35		P54	MTIC5V/TMRI0	SCK6/SSLA3	SEG19		
36		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1	SEG20		IRQ7

Table 1.9 List of Pins and Pin Functions (80-Pin LFQFP) (2/2)

Pin No. 80-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	LCD	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
37		PC6	MTIOC4A/POE1#	RXD1/SMISO1/SSCL1	SEG21		IRQ6
38		PC5	MTIOC4C/POE2#	TXD8/SMOSI8/SSDA8	SEG22		IRQ5
39		PC4	MTIOC4B/POE3#	RXD8/SMISO8/SSCL8	SEG23		IRQ4
40		PC3	MTIOC4D/POE8#	CTS8#/RTS8#/SS8#	SEG24		IRQ3
41		PC1	TMO0	SCK1/SCK8/CRXD0	COM0		IRQ1
42		PC0	MTIOC4A/MTIC5U/ TMCI0	TXD1/SMOSI1/SSDA1/ CTXD0	COM1		IRQ0
43		PA4	MTIOC2A/MTIOC4A	MISOA	COM2		
44		PA3	MTIOC2B/MTIOC4C	TXD9/SMOSI9/SSDA9/ MOSIA	COM3		
45		PA2	MTIOC4B/TMO2	RXD9/SMISO9/SSCL9/ SSLA0	SEG26/COM4		
46		PA1	MTIOC4D/TMCI2	CTS9#/RTS9#/SS9#/ SSLA1	SEG27/COM5		
47		PA0	TMRI2/RTCOUT	SCK9/SSLA3	SEG28/COM6		
48		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2	SEG29/COM7		
49	VCC						
50		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	SEG30	CMPA2	
51	VSS						
52		PE4	MTIOC3A/MTCLKB/ TMO3	TXD5/SMOSI5/SSDA5/ SSLA2	SEG31		IRQ7
53		PE3	MTIOC3C/MTCLKA/ TMCI3	RXD5/SMISO5/SSCL5	SEG32		IRQ6
54		PE2	MTIOC3B/MTCLKD/ TMRI3	CTS5#/RTS5#/SS5#	SEG33		IRQ5
55		PE1	MTIOC3D/MTCLKC	SCK5	SEG34		IRQ4
56		PE0	MTCLKA/CACREF	SSLA3	SEG35		
57	AVCC0						
58	AVSS0						
59						REFOUT	
60						LSW	
61						AIN0/AN000	
62						AIN1/AN001	
63	VREFL0					AIN2/IEXC0/VBIAS	
64	VREFH0					AIN3/IEXC1	
65						REF0N	
66						REF0P	
67						AIN4/AN002	
68						AIN5/AN003	
69						AIN6	
70						AIN7	
71						AIN8/IEXC0	
72						AIN9/IEXC1	
73						AIN10/AN004/VBIAS	
74						AIN11/AN005	
75						AIN12/AN006/REF1N	
76						AIN13/AN007/REF1P	
77						AIN14	
78						AIN15	
79	VREFH						
80	VREFL						

1.6.6 64-Pin LFQFP with High-Voltage Input Pins

Table 1.10 List of Pins and Pin Functions (64-Pin LFQFP with High-Voltage Input Pins) (1/2)

Pin No. 64-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1					DA0	
2	AVSS0					
3	AVCC0					
4	MD					FINED
5	XCIN					
6	XCOUT					
7	RES#					
8	XTAL	P37				
9	VSS					
10	EXTAL	P36				
11	VCC					
12	VCL					
13		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6		
14		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6		
15		P65	MTIOC4B/MTCLKD/ TMO2/POE0#	CTS6#/RTS6#/SS6#		
16		P64	MTIOC4D/MTCLKC/ RTCOUT	SCK6	ADTRG0#	
17		P35				NMI
18		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA		IRQ1
19		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5		IRQ0
20		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#		IRQ3
21		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12		IRQ2
22		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA		IRQ7
23		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	ADTRG0#	IRQ6
24		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0		IRQ5
25		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	CLKOUT	IRQ4
26		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#		
27		P54	MTIC5V/TMRI0	SCK6/SSLA3		
28		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1		IRQ7
29		PC6	MTIOC4A/POE1#	RXD1/SMISO1/SSCL1		IRQ6
30		PC5	MTIOC4C/POE2#	TXD8/SMOSI8/SSDA8		IRQ5
31		PC4	MTIOC4B/POE3#	RXD8/SMISO8/SSCL8		IRQ4
32		PC3	MTIOC4D/POE8#	CTS8#/RTS8#/SS8#		IRQ3
33		PC1	TMO0	SCK1/SCK8/CRXD0		IRQ1
34		PC0	MTIOC4A/MTIC5U/ TMCI0	TXD1/SMOSI1/SSDA1/ CTXD0		IRQ0
35		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2		
36	VCC					
37		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	CMPA2	
38	VSS					

Table 1.10 List of Pins and Pin Functions (64-Pin LFQFP with High-Voltage Input Pins) (2/2)

Pin No. 64-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
39		PE4	MTIOC3A/MTCLKB/ TMO3	TXD5/SMOSI5/SSDA5/ SSLA2		IRQ7
40		PE3	MTIOC3C/MTCLKA/ TMCI3	RXD5/SMISO5/SSCL5		IRQ6
41		PE2	MTIOC3B/MTCLKD/ TMRI3	CTS5#/RTS5#/SS5#		IRQ5
42		PE1	MTIOC3D/MTCLKC	SCK5		IRQ4
43		PE0	MTCLKA/CACREF	SSLA3		
44	AVCC0					
45	AVSS0					
46					REFOUT	
47	VREFL0				AIN2/IEXC0/VBIAS	
48	VREFH0				AIN3/IEXC1	
49					LSW	
50					REF0N	
51					REF0P	
52					AIN4/AN002	
53					AIN5/AN003	
54					AIN10/AN004/VBIAS	
55					AIN11/AN005	
56					HVCOM	
57					HVAIN0	
58					HVAIN1	
59					HVAIN2	
60					HVAIN3	
61					AIN12/AN006/REF1N	
62					AIN13/AN007/REF1P	
63	VREFH					
64	VREFL					

1.6.7 64-Pin LFQFP without High-Voltage Input Pins

Table 1.11 List of Pins and Pin Functions (64-Pin LFQFP without High-Voltage Input Pins) (1/2)

Pin No. 64-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1					DA0	
2	AVSS0					
3	AVCC0					
4	MD					FINED
5	XCIN					
6	XCOUT					
7	RES#					
8	XTAL	P37				
9	VSS					
10	EXTAL	P36				
11	VCC					
12	VCL					
13		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6		
14		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6		
15		P65	MTIOC4B/MTCLKD/ TMO2/POE0#	CTS6#/RTS6#/SS6#		
16		P64	MTIOC4D/MTCLKC/ RTCOUT	SCK6	ADTRG0#	
17		P35				NMI
18		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA		IRQ1
19		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5		IRQ0
20		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#		IRQ3
21		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12		IRQ2
22		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA		IRQ7
23		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	ADTRG0#	IRQ6
24		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0		IRQ5
25		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	CLKOUT	IRQ4
26		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#		
27		P54	MTIC5V/TMRI0	SCK6/SSLA3		
28		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1		IRQ7
29		PC6	MTIOC4A/POE1#	RXD1/SMISO1/SSCL1		IRQ6
30		PC5	MTIOC4C/POE2#	TXD8/SMOSI8/SSDA8		IRQ5
31		PC4	MTIOC4B/POE3#	RXD8/SMISO8/SSCL8		IRQ4
32		PC3	MTIOC4D/POE8#	CTS8#/RTS8#/SS8#		IRQ3
33		PC1	TMO0	SCK1/SCK8/CRXD0		IRQ1
34		PC0	MTIOC4A/MTIC5U/ TMCI0	TXD1/SMOSI1/SSDA1/ CTXD0		IRQ0
35		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2		
36	VCC					
37		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	CMPA2	
38	VSS					
39		PE1	MTIOC3D/MTCLKC	SCK5		IRQ4

Table 1.11 List of Pins and Pin Functions (64-Pin LFQFP without High-Voltage Input Pins) (2/2)

Pin No. 64-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
40		PE0	MTCLKA/CACREF	SSLA3		
41	AVCC0					
42	AVSS0					
43					REFOUT	
44					AIN0/AN000	
45					AIN1/AN001	
46	VREFL0				AIN2/IEXC0/VBIAS	
47	VREFH0				AIN3/IEXC1	
48					LSW	
49					REF0N	
50					REF0P	
51					AIN4/AN002	
52					AIN5/AN003	
53					AIN6	
54					AIN7	
55					AIN8/IEXC0	
56					AIN9/IEXC1	
57					AIN10/AN004/VBIAS	
58					AIN11/AN005	
59					AIN12/AN006/REF1N	
60					AIN13/AN007/REF1P	
61					AIN14	
62					AIN15	
63	VREFH					
64	VREFL					

1.6.8 48-Pin LFQFP

Table 1.12 List of Pins and Pin Functions (48-Pin LFQFP) (1/2)

Pin No. 48-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1					DA0	
2	AVSS0					
3	AVCC0					
4	MD					FINED
5	RES#					
6	XTAL	P37				
7	VSS					
8	EXTAL	P36				
9	VCC					
10	VCL					
11		P67	MTIOC4A/TMRI2	TXD6/SMOSI6/SSDA6		
12		P66	MTIOC4C/TMCI2	RXD6/SMISO6/SSCL6		
13		P35				NMI
14		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA		IRQ1
15		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5		IRQ0
16		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#		IRQ3
17		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12		IRQ2
18		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA		IRQ7
19		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	ADTRG0#	IRQ6
20		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0		IRQ5
21		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	CLKOUT	IRQ4
22		P55	MTIC5W/TMO0	CTS6#/RTS6#/SS6#		
23		P54	MTIC5V/TMRI0	SCK6/SSLA3		
24		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1		IRQ7
25		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2		
26	VCC					
27		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	CMPA2	
28	VSS					
29	AVCC0					
30	AVSS0					
31					REFOUT	
32					AIN0/AN000	
33					AIN1/AN001	
34	VREFL0				AIN2/IEXC0/VBIAS	
35	VREFH0				AIN3/IEXC1	
36					LSW	
37					REF0N	
38					REF0P	
39					AIN4/AN002	
40					AIN5/AN003	
41					AIN8/IEXC0	

Table 1.12 List of Pins and Pin Functions (48-Pin LFQFP) (2/2)

Pin No. 48-Pin LFQFP	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
42					AIN9/IEXC1	
43					AIN10/AN004/VBIAS	
44					AIN11/AN005	
45					AIN12/AN006/REF1N	
46					AIN13/AN007/REF1P	
47	VREFH					
48	VREFL					

1.6.9 40-Pin HWQFN with High-Voltage Input Pins

Table 1.13 List of Pins and Pin Functions (40-Pin HWQFN with High-Voltage Input Pins)

Pin No. 40-Pin HWQFN	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1					DA0	
2	AVSS0					
3	AVCC0					
4	MD					FINED
5	RES#					
6	XTAL	P37				
7	VSS					
8	EXTAL	P36				
9	VCC					
10	VCL					
11		P35				NMI
12		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA		IRQ1
13		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5		IRQ0
14		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#		IRQ3
15		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12		IRQ2
16		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA		IRQ7
17		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	ADTRG0#	IRQ6
18		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0		IRQ5
19		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	CLKOUT	IRQ4
20		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1		IRQ7
21		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2		
22	VCC					
23		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	CMPA2	
24	VSS					
25	AVCC0					
26	AVSS0					
27					REFOUT	
28					AIN0/AN000	
29					AIN1/AN001	
30	VREFL0				AIN2/IEXC0/VBIAS	
31	VREFH0				AIN3/IEXC1	
32					REF0N	
33					REF0P	
34					HVCOM	
35					HVAIN0	
36					HVAIN1	
37					HVAIN2	
38					HVAIN3	
39	VREFH					
40	VREFL					

1.6.10 40-Pin HWQFN without High-Voltage Input Pins

Table 1.14 List of Pins and Pin Functions (40-Pin HWQFN without High-Voltage Input Pins)

Pin No. 40-Pin HWQFN	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN)	Analog (S12AD, R16DA, VREF, IEXC, DSAD, AMUX)	Others
1					DA0	
2	AVSS0					
3	AVCC0					
4	MD					FINED
5	RES#					
6	XTAL	P37				
7	VSS					
8	EXTAL	P36				
9	VCC					
10	VCL					
11		P35				NMI
12		P31	MTIOC1A/MTIOC4D/ MTCLKB/TMO3/CACREF	TXD5/SMOSI5/SSDA5/ RSPCKA		IRQ1
13		P30	MTIOC2A/MTIOC4B/ MTCLKD/TMCI3/POE8#	RXD1/SMISO1/SSCL1/ RXD5/SMISO5/SSCL5		IRQ0
14		P27	MTIOC2B/MTIOC4A/ TMRI3/POE2#	SCK5/CTS12#/RTS12#/ SS12#		IRQ3
15		P26	MTIOC0A/MTIOC4C/ MTCLKC/TMO0	TXD1/SMOSI1/SSDA1/ CTS5#/RTS5#/SS5#/ SCK12		IRQ2
16		P17	MTIOC0D/MTIOC3A/ MTIOC3B/TMO1	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MISOA/SDA		IRQ7
17		P16	MTIOC3C/MTIOC3D/ TMO2	RXD12/SMISO12/ SSCL12/RXDX12/ MOSIA/SCL	ADTRG0#	IRQ6
18		P15	MTIOC0C/MTIOC4D/ MTCLKB/TMCI2	CTS1#/RTS1#/SS1#/ SSLA0/CRXD0		IRQ5
19		P14	MTIOC0B/MTIOC3B/ MTCLKA/TMRI2	SCK1/CTXD0	CLKOUT	IRQ4
20		PC7	MTIOC4B/MTIOC3D/ MTIC5U/TMCI0/POE0#	TXD1/SMOSI1/SSDA1/ SSLA1		IRQ7
21		PB1	MTIOC4C/MTIOC3A/ MTIC5V/TMRI0/TMCI1/ POE1#	RXD1/SMISO1/SSCL1/ SSLA2		
22	VCC					
23		PB0	MTIOC1B/MTIOC3C/ MTIC5W/TMRI1/POE3#	RSPCKA	CMPA2	
24	VSS					
25		PE0	MTCLKA/CACREF	SSLA3		
26	AVCC0					
27	AVSS0					
28					REFOUT	
29	VREFL0				AIN2/IEXC0/VBIAS	
30	VREFH0				AIN3/IEXC1	
31					REF0N	
32					REF0P	
33					AIN4/AN002	
34					AIN5/AN003	
35					AIN10/AN004/VBIAS	
36					AIN11/AN005	
37					AIN12/AN006/REF1N	
38					AIN13/AN007/REF1P	
39	VREFH					
40	VREFL					

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL = HVCOM = 0 V

Item			Symbol	Value	Unit
Power supply voltage			VCC	–0.3 to +6.5	V
Input voltage	P16, P17, P60, P61, P73, P74 (5-V tolerant)		V_{in}	–0.3 to +6.5	V
	Ports other than above			–0.3 to VCC + 0.3	
Reference power supply voltage			VREFH0	–0.3 to AVCC0 + 0.3	V
			VREFH		
Analog power supply voltage			AVCC0	–0.3 to +6.5	V
Analog input voltage	HVAIN0 to HVAIN3		V_{HVAN}	–15 to +15	V
	Ports other than above		V_{AN}	–0.3 to AVCC0 + 0.3	
Reference voltage for 24-bit delta-sigma A/D converter			REF0P, REF1P	–0.3 to AVCC0 + 0.3	V
			REF0N, REF1N	–0.3 to AVCC0 + 0.3	
LCD voltage	V_{L1} voltage		V_{L1}	–0.3 to +6.5	V
	V_{L2} voltage		V_{L2}	–0.3 to +6.5	
	V_{L3} voltage		V_{L3}	–0.3 to +6.5	
	V_{L4} voltage		V_{L4}	–0.3 to +6.5	
Junction temperature		D version	T_j	–40 to +105	°C
		G version		–40 to +112	
Storage temperature			T_{stg}	–55 to +125	°C

Caution: Exceeding absolute maximum ratings may permanently damage the MCU.

To preclude malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors with values of about 0.1 µF as close as possible to every power supply pin and use the shortest and widest possible traces.

Connect the VCL pin to a VSS pin via a 4.7-µF capacitor. The capacitor must be placed close to the pin. For details, refer to section 2.15.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals to ports other than 5-V tolerant ports while power is not being supplied to the MCU.

The current injection that results from the input of such a signal may lead to malfunctions and the abnormal current that passes through the MCU at such times may cause degradation of internal elements.

However, even if –0.3 to +6.5 V is input to a 5-V tolerant port, this will not cause problems such as damage to the MCU.

2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltages		VCC*1, *2	1.8	—	5.5	V
		VSS	—	0	—	
Analog power supply voltages		AVCC0*1, *2	1.8	—	5.5	V
		AVSS0	—	0	—	
		VREFH0	1.8	—	5.5	
		VREFL0	—	0	—	
		VREFH	2.5	—	AVCC0	
		VREFL	—	0	—	
Input voltage	Ports for 5 V tolerant: P16, P17, P60, P61, P73, P74	V_{in}	–0.3	—	5.8	V
	AIN0 to AIN15, REF0N, REF0P, REF1N, REF1P		–0.3	—	AVCC0 + 0.3	
	HVCOM		—	0	—	
	HVAIN0 to HVAIN3		–10	—	10	
	Ports other than above		–0.3	—	VCC + 0.3	
Operating temperature	D version	T_{opr}	–40	—	85	°C
	G version		–40	—	105	

Note 1. Use AVCC0 and VCC under the following conditions:
While VCC > 2.4 V: AVCC0 and VCC can be set independently when AVCC0 ≥ 2.4 V
While VCC ≤ 2.4 V: AVCC0 and VCC can be set independently when AVCC0 ≥ VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance for stabilizing the internal voltage	C_{VCL}	4.7 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 4.7 µF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—	V	
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	IRQ input pin, MTU2 input pin, POE2 input pin, TMR input pin, SCI input pin, RSPI input pin, CAC input pin, CAN input pin, ADTRG0# input pin, RES#, NMI	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.1 × VCC	—	—		
Input level voltage (except for schmitt trigger input pins)	MD	V_{IH}	0.9 × VCC	—	—	V	
		V_{IL}	—	—	0.1 × VCC		
	EXTAL (external clock input)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	RIIC input pin (SMBus)	V_{IH}	2.1	—	—		
		V_{IL}	—	—	0.8		
	P12 to P17, P20 to P27, P30, P31, P35 to P37, P54, P55, P60 to P67, P70 to P74, PA0 to PA4, PB0, PB1, PC0 to PC7, PD0 to PD4, PE0 to PE4	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		

Table 2.5 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC ≤ 2.7 V, 1.8 V ≤ AVCC0 ≤ 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin, MTU2 input pin, POE2 input pin, TMR input pin, SCI input pin, RSPI input pin, CAC input pin, CAN input pin, ADTRG0# input pin, RES#, NMI	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.01 × VCC	—	—		
Input level voltage (except for schmitt trigger input pins)	MD	V_{IH}	0.9 × VCC	—	—	V	
		V_{IL}	—	—	0.1 × VCC		
	EXTAL (external clock input)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	P12 to P17, P20 to P27, P30, P31, P35 to P37, P54, P55, P60 to P67, P70 to P74, PA0 to PA4, PB0, PB1, PC0 to PC7, PD0 to PD4, PE0 to PE4	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		

Table 2.6 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, and P35	$\|I_{in}\|$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	P16, P17, P60, P61, P73, P74	$\|I_{TSI}\|$	—	—	1.0	μA	V_{in} = 0 V, 5.8V
	Ports other than P16, P17, P60, P61, P73, P74		—	—	0.2		V_{in} = 0 V, VCC
Input capacitance	P12 to P17, P20 to P27, P30, P31, P36, P37, P54, P55, P60 to P67, P70 to P74, PA0 to PA4, PB0, PB1, PC0 to PC7, PD0 to PD4, PE0 to PE4, MD, and RES#	C_{in}	—	—	15	pF	V_{in} = 20 mV, f = 1 MHz, T_a = 25°C
	P35		—	—	30		
Output voltage of the VCL pin		V_{CL}	—	2.12	—	V	

Table 2.7 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for P35)	R_U	10	20	50	kΩ	V_{in} = 0 V

Table 2.8 DC Characteristics (5) (1/2)
Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

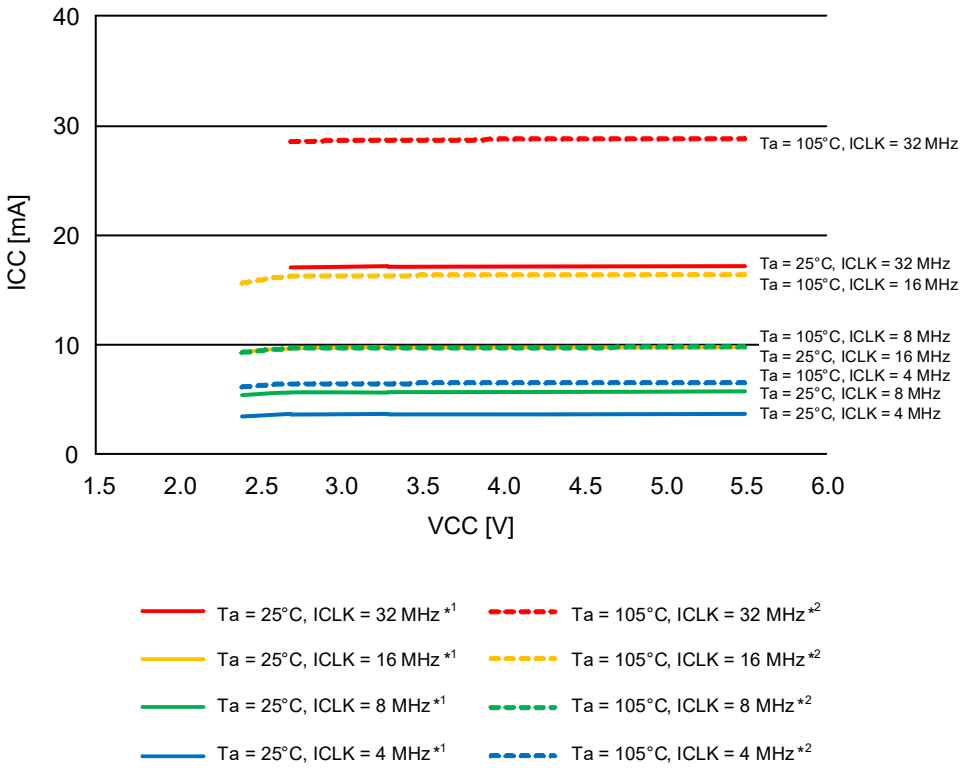
Item					Symbol	Typ.*4	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral modules are operating.*2	ICLK = 32 MHz	I_{CC}	3.7	—	mA	
				ICLK = 16 MHz		2.6	—		
				ICLK = 8 MHz		2.0	—		
				ICLK = 4 MHz		1.7	—		
			All peripheral modules are in normal operation.	ICLK = 32 MHz*3		17.1	—		
				ICLK = 16 MHz*3		9.7	—		
				ICLK = 8 MHz*3		5.7	—		
				ICLK = 4 MHz*3		3.6	—		
			All peripheral modules are in full operation.	ICLK = 32 MHz		—	30.9		
		Sleep mode	No peripheral modules are operating.*2	ICLK = 32 MHz		2.2	—		
				ICLK = 16 MHz		1.7	—		
				ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.3	—		
			All peripheral modules are in normal operation.	ICLK = 32 MHz*3		10.0	—		
				ICLK = 16 MHz*3		6.0	—		
				ICLK = 8 MHz*3		3.7	—		
				ICLK = 4 MHz*3		2.5	—		
		Deep sleep mode	No peripheral modules are operating.*2	ICLK = 32 MHz		1.4	—		
				ICLK = 16 MHz		1.2	—		
				ICLK = 8 MHz		1.1	—		
				ICLK = 4 MHz		1.0	—		
			All peripheral modules are in normal operation.	ICLK = 32 MHz*3		8.4	—		
				ICLK = 16 MHz*3		5.1	—		
				ICLK = 8 MHz*3		3.1	—		
				ICLK = 4 MHz*3		2.1	—		
		Increase during BGO operation*5				2.5	—		

Table 2.8 DC Characteristics (5) (2/2)
Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.*4	Max.	Unit	Test Conditions
Supply current *1	Middle-speed operating mode	Normal operating mode	No peripheral modules are operating.*6	ICLK = 12 MHz	I_{CC}	1.9	—	mA	
				ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.2	—		
				ICLK = 1 MHz		0.9	—		
			All peripheral modules are in normal operation.*7	ICLK = 12 MHz		7.2	—		
				ICLK = 8 MHz		5.1	—		
				ICLK = 4 MHz		3.1	—		
				ICLK = 1 MHz		1.4	—		
			All peripheral modules are in full operation.*7	ICLK = 12 MHz		—	13.8		
		Sleep mode	No peripheral modules are operating.*6	ICLK = 12 MHz		1.3	—		
				ICLK = 8 MHz		1.0	—		
				ICLK = 4 MHz		0.9	—		
				ICLK = 1 MHz		0.8	—		
			All peripheral modules are in normal operation.*7	ICLK = 12 MHz		4.5	—		
				ICLK = 8 MHz		3.2	—		
				ICLK = 4 MHz		2.1	—		
				ICLK = 1 MHz		1.2	—		
		Deep sleep mode	No peripheral modules are operating.*6	ICLK = 12 MHz		0.9	—		
				ICLK = 8 MHz		0.8	—		
				ICLK = 4 MHz		0.7	—		
				ICLK = 1 MHz		0.7	—		
			All peripheral modules are in normal operation.*7	ICLK = 12 MHz		3.8	—		
				ICLK = 8 MHz		2.8	—		
				ICLK = 4 MHz		1.8	—		
				ICLK = 1 MHz		1.0	—		
		Increase during BGO operation*5				2.5	—		
	Low-speed operating mode	Normal operating mode	No peripheral modules are operating.*8	ICLK = 32 kHz		4.3	—	μA	
			All peripheral modules are in normal operation.*9, *10	ICLK = 32 kHz		16.1	—		
			All peripheral modules are in full operation. *9, *10	ICLK = 32 kHz		—	78.5		
		Sleep mode	No peripheral modules are operating.*8	ICLK = 32 kHz		2.6	—		
			All peripheral modules are in normal operation.*9	ICLK = 32 kHz		9.1	—		
		Deep sleep mode	No peripheral modules are operating.*8	ICLK = 32 kHz		2.0	—		
			All peripheral modules are in normal operation.*9	ICLK = 32 kHz		7.8	—		

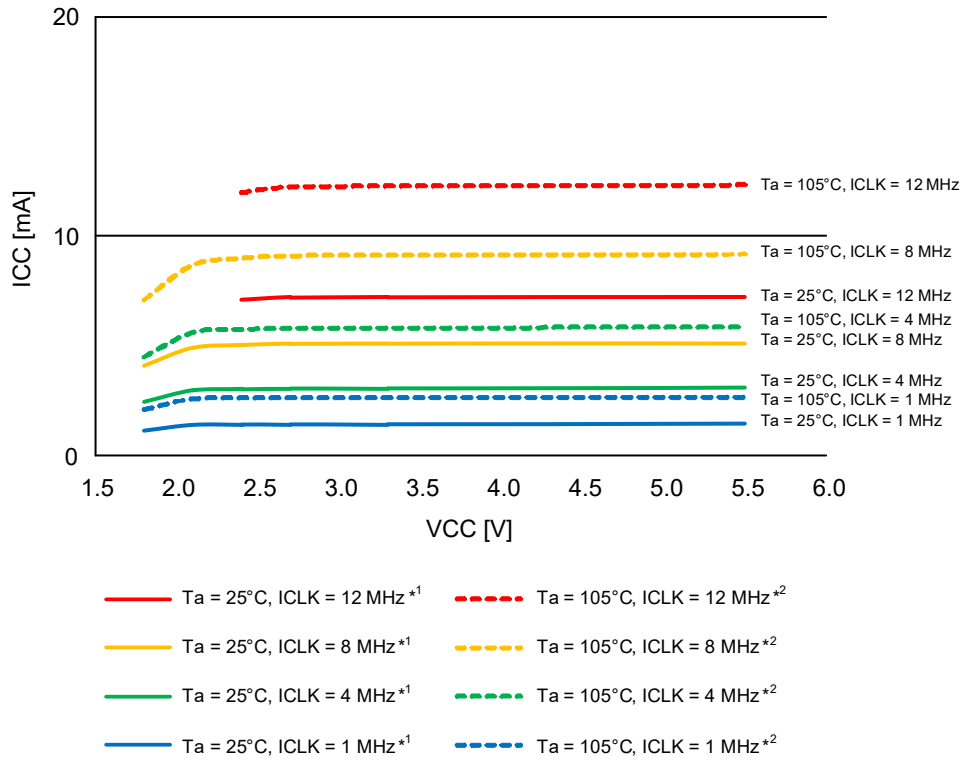
Note 1. Supply current values do not include the output charge/discharge current from all pins. The values apply when internal pull-up resistors are disabled.
Note 2. Peripheral module clocks are stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Peripheral module clocks are supplied. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are the same frequency as that of ICLK.
Note 4. Conditions for typical values are at VCC = 3.3 V and T_a = 25°C.
Note 5. The increase is caused by program/erase operation to the ROM or E2 DataFlash during the execution of a user program.
Note 6. Peripheral module clocks are stopped. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK and PCLK are set to divided by 64.
Note 7. Peripheral module clocks are supplied. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK and PCLK are the same frequency of that of the ICLK.
Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 10. The MSTPCRA.MSTPA17 (12-bit A/D converter module stop setting) and MSTPCRA.MSTPA25 (24-bit delta-sigma A/D converter module stop setting) bits are set for the module stop state.



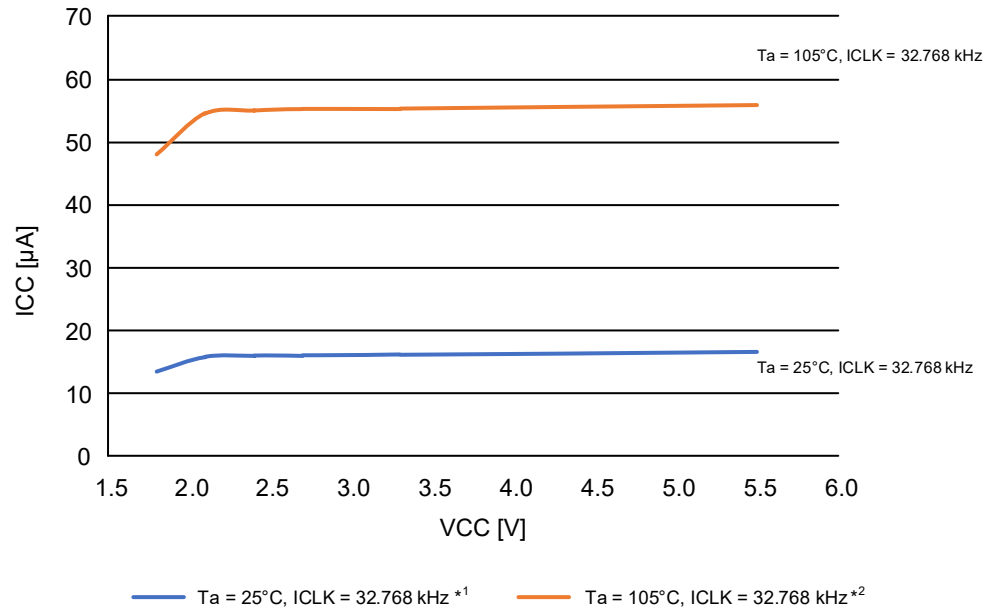
Note 1. This result applies when all peripheral modules are in normal operation but BGO is not in use. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. This result applies when all peripheral modules are in full operation but BGO is not in use. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 2.1 Voltage Dependence in High-Speed Operating Mode (Reference Data)



Note 1. This result applies when all peripheral modules are in normal operation but BGO is not in use. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. This result applies when all peripheral modules are in full operation but BGO is not in use. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 2.2 Voltage Dependence in Middle-Speed Operating Mode (Reference Data)



Note 1. This result applies when all peripheral modules are in normal operation but BGO is not in use. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. This result applies when all peripheral modules are in full operation but BGO is not in use. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

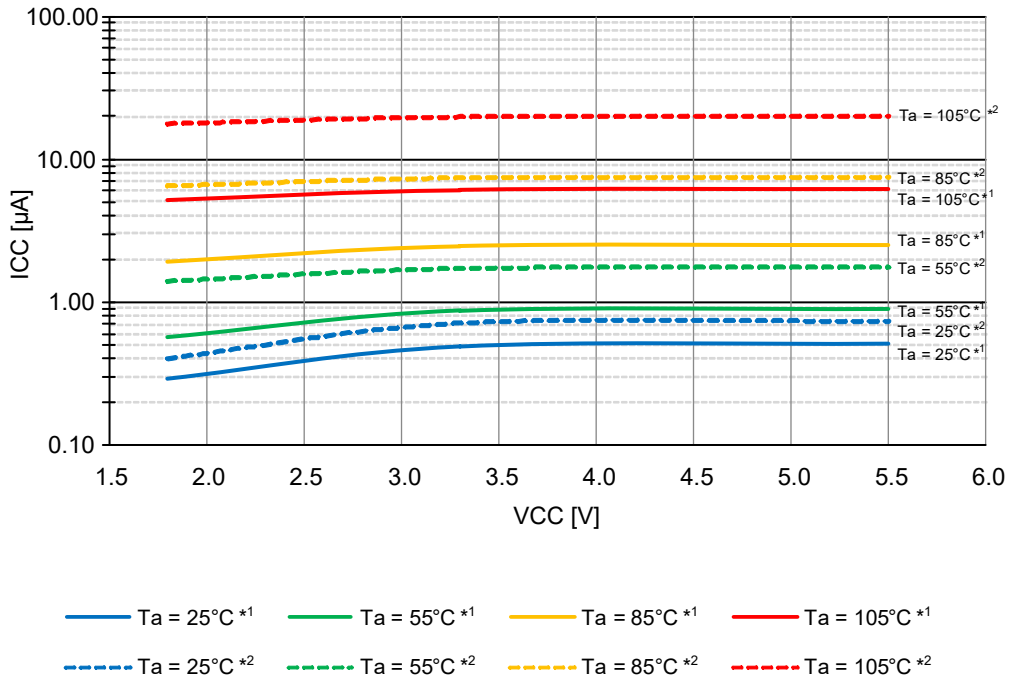
Figure 2.3 Voltage Dependence in Low-Speed Operating Mode (Reference Data)

Table 2.9 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.5	1.2	μA	
		T_a = 55°C		0.9	3.1		
		T_a = 85°C		2.5	13.7		
		T_a = 105°C		6.1	36.7		
	Increment for IWDT operation			0.4	—		
	Increment for LPT operation			0.4	—		Use IWDT-Dedicated On-Chip Oscillator for clock source
	Increment for RTC operation*4			0.4	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.2	—		RCR3.RTCDV[2:0] set to normal drive capacity

Note 1. Supply current values were obtained with no load on any output pin and all internal pull-up resistors disabled.
Note 2. The IWDT and LVD are stopped.
Note 3. Conditions for typical values are at VCC = 3.3 V.
Note 4. This increment includes the oscillation circuit.



Note 1. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 2.4 Voltage Dependence in Software Standby Mode (Reference Data)

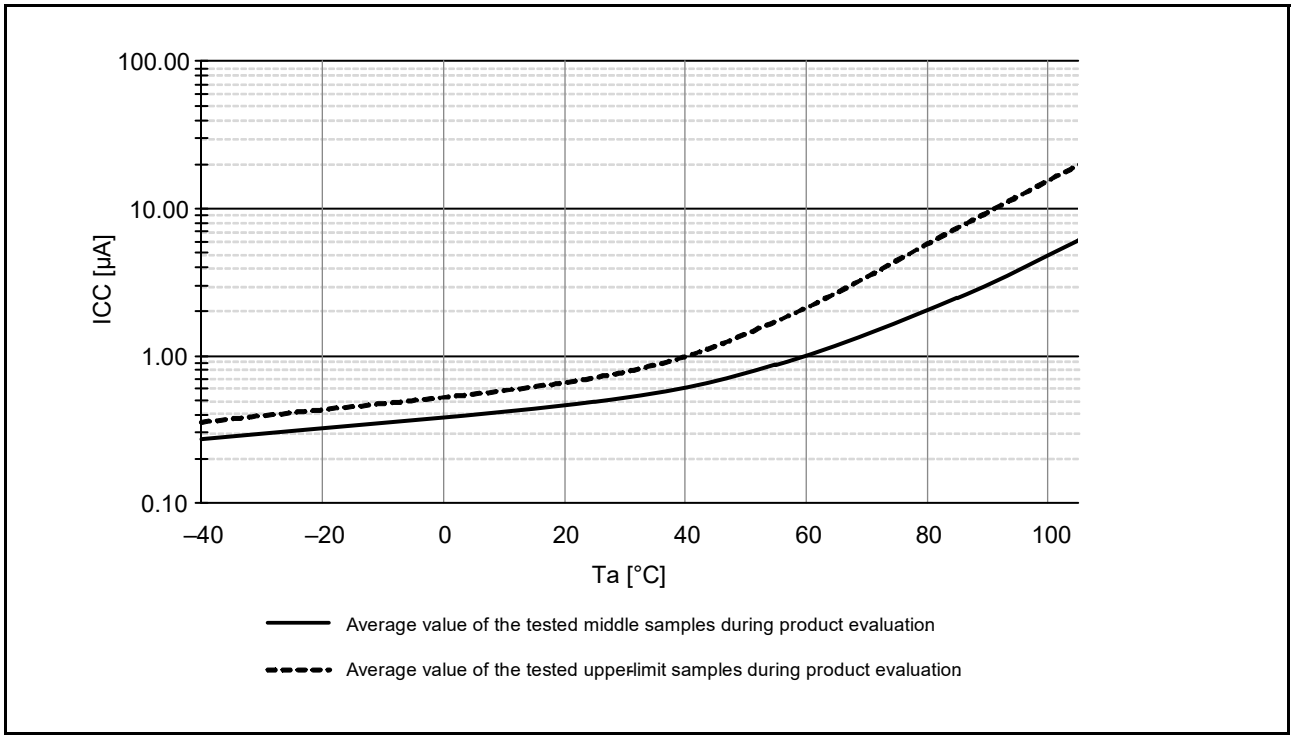


Figure 2.5 Temperature Dependence in Software Standby Mode (Reference Data)

Table 2.10 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
LVD	LVD0	I_{LVD}	—	0.10	—	µA	
	LVD1		—	0.10	—		
	LVD2		—	0.20	—		

Note 1. Conditions for typical values are at VCC = AVCC0 = 3.3 V and T_a = 25°C.

Table 2.11 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 2.12 DC Characteristics (9)

Conditions: 0 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC ramp-up rate at power-on	At normal startup*1	SrVCC	0.02	—	20.00	ms/V	
	During fast startup time*2		0.02	—	2.00		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When the OFS1.LVDAS and OFS1.FASTSTUP bits are 1
Note 2. When the OFS1.LVDAS bit is 1 and the OFS1.FASTSTUP bit is 0
Note 3. When the OFS1.LVDAS bit is 0
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the settings in the OFS1 register are not read in boot mode.

Table 2.13 DC Characteristics (10)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

The result of any ripple must be within the limit on allowable ripple frequency $f_{r\,(VCC)}$ where the ripple voltage is within the range between the VCC upper limit and lower limit. The result of any ripple must be within the limit on the allowable VCC ramp rate in power fluctuation (dt/dVCC) where the change in VCC exceeds VCC ±10%.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 2.6 $V_{r\,(VCC)} \leq 0.2 \times VCC$
		—	—	1	MHz	Figure 2.6 $V_{r\,(VCC)} \leq 0.08 \times VCC$
		—	—	10	MHz	Figure 2.6 $V_{r\,(VCC)} \leq 0.06 \times VCC$
Allowable VCC ramp rate at power fluctuation	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

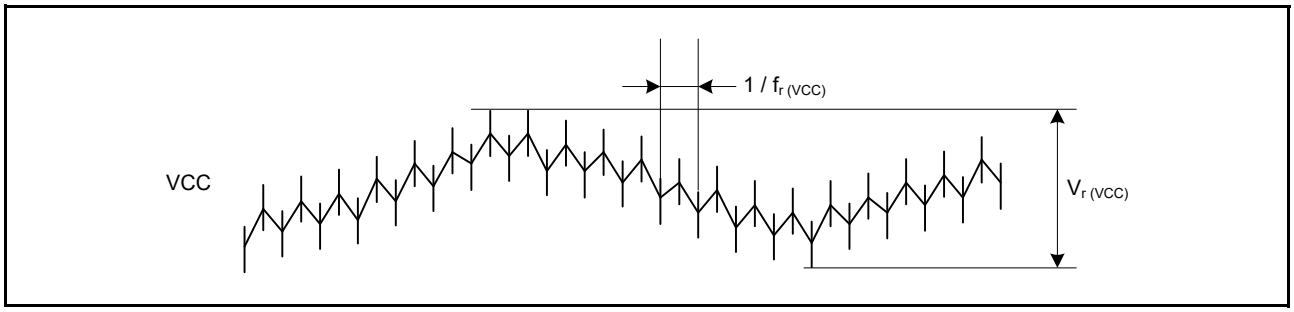


Figure 2.6 Ripple Waveform

Table 2.14 DC Characteristics (11)

Conditions: 1.8 V ≤ VCC = AVCC ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*3	Max.	Unit
LCD operating current*2	External resistive divider method*4 $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 1/4 duty	I_{LCD1}*1	—	0.04	—	µA
	Internal voltage boost method (VLCD.VLCD = 04) $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 1/4 duty	I_{LCD2}*1	—	0.85	—	µA
	Internal voltage boost method (VLCD.VLCD = 12) $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 1/4 duty	I_{LCD2}*1	—	1.55	—	µA
	Capacitive divider method $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 1/4 duty	I_{LCD3}*1	—	0.20	—	µA

Note 1. Current consumed only by the LCD module. Current when the LCD panel is not connected.
Note 2. Current consumed by the power supply (VCC).
Note 3. When VCC = AVCC0 = 3.3 V and T_a = 25°C.
Note 4. It does not include the current that flows through external divider resistors.

Table 2.15 DC Characteristics (12)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating current of 24-bit delta-sigma A/D converter	Gain = 1 (PGA disabled, BUF disabled)	I_{AVCC0} (DSAD)	—	7.5	9.1	mA	Figure 2.7, Figure 2.8 1 unit, external reference in use, reference buffer disabled VCC ≥ 2.4 V
	Gain = 1 to 128 (PGA enabled)		—	17.1	20.2		
Operating current of voltage reference		I_{AVCC0} (VREF)	—	45	75	µA	Figure 2.9
Operating current of temperature sensor		I_{AVCC0} (TEMPS)	—	15	40	µA	Figure 2.10
Operating current of bias voltage generator		I_{AVCC0} (VBIAS)	—	15	25	µA	Figure 2.11
Operating current of excitation current source		I_{AVCC0} (IEXC)	—	30	50	µA	Figure 2.12
Operating current of analog input buffer		I_{AVCC0} (BUF)	—	2.6	4.5	mA	Figure 2.13, 1 unit VCC ≥ 2.4 V
Operating current of reference buffer		I_{AVCC0} (REFBUF)	—	2.8	4.6	mA	Figure 2.14, 1 unit VCC ≥ 2.4 V
Operating current of voltage detector	Low voltage detector for power supply	I_{AVCC0} (LVDET)	—	5	9	µA	1 unit
	Excitation current source disconnect detector	I_{AVCC0} (IEXCDET)	—	2	4		
	DSAD input voltage fault detector	I_{AVCC0} (DSIDET)	—	5	7		
	DSAD reference voltage fault detector	I_{AVCC0} (DSRDET)	—	10	15		
	High voltage analog common input disconnect detector	I_{AVCC0} (HVCOMDET)	—	10	15		
Operating current of 16-bit D/A converter		I_{v5dc}	—	200	300	µA	Figure 2.15 AVCC0 pin and VREFH pin current

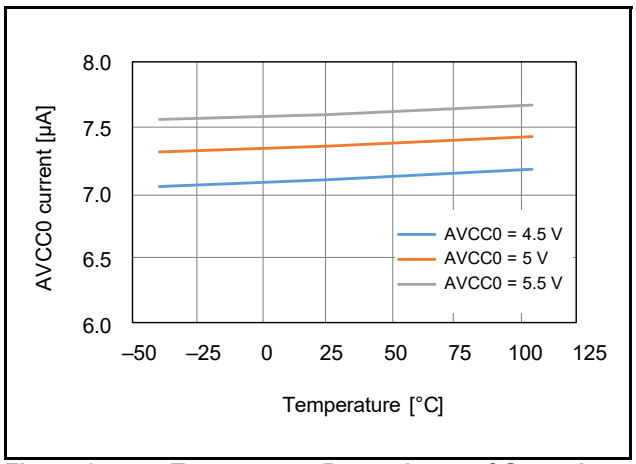


Figure 2.7 Temperature Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (PGA Disabled, BUF Disabled)

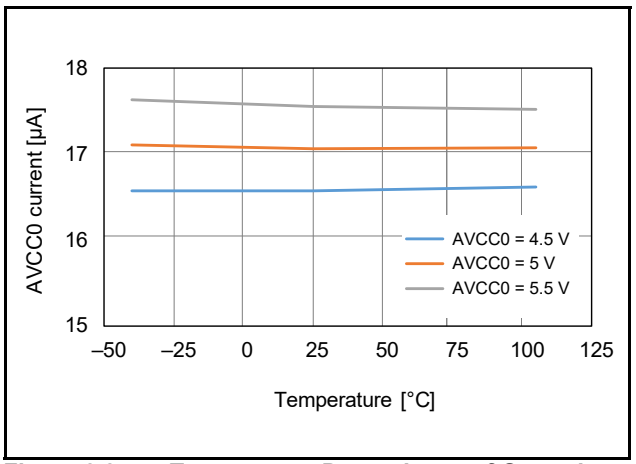


Figure 2.8 Temperature Dependence of Operating Current of 24-Bit Delta-Sigma A/D Converter (PGA Enabled)

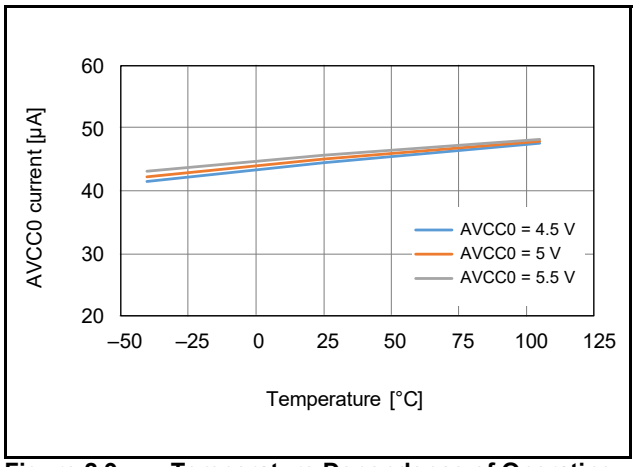


Figure 2.9 Temperature Dependence of Operating Current of Voltage Reference

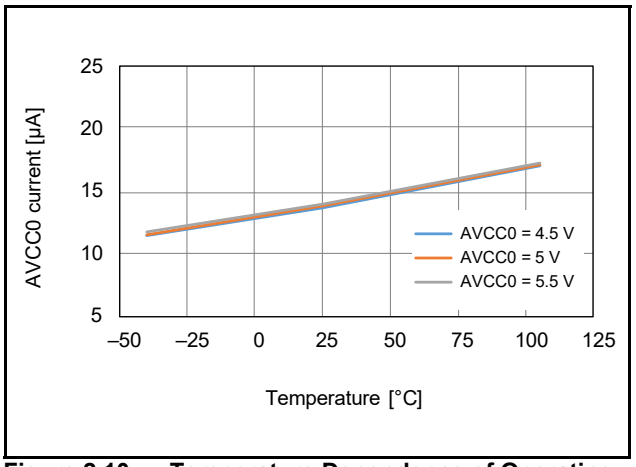


Figure 2.10 Temperature Dependence of Operating Current of Temperature Sensor

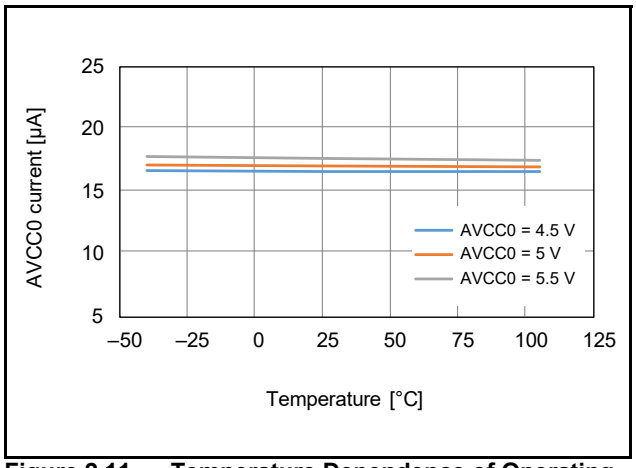


Figure 2.11 Temperature Dependence of Operating Current of Bias Voltage Generator

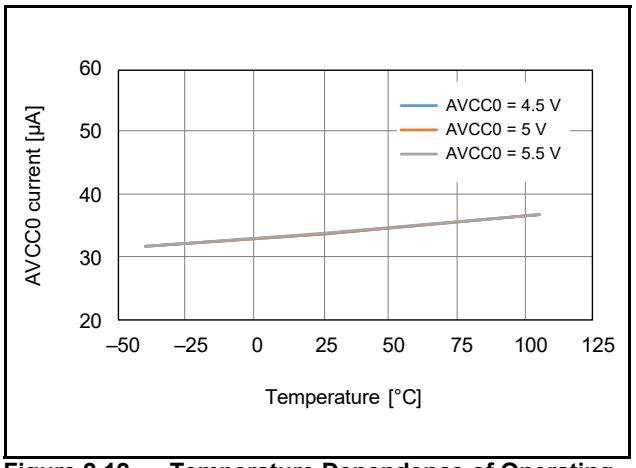


Figure 2.12 Temperature Dependence of Operating Current of Excitation Current Source

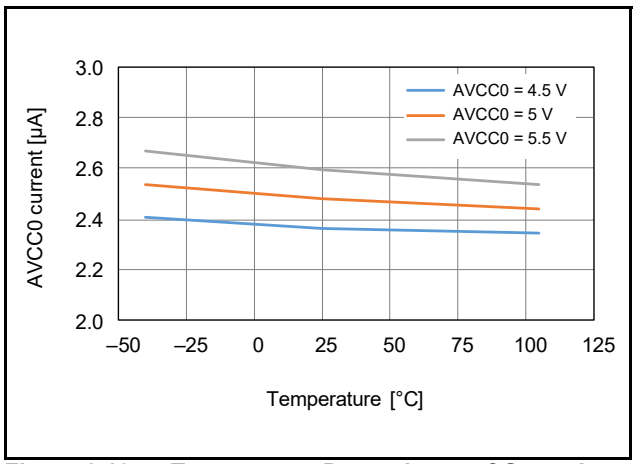


Figure 2.13 Temperature Dependence of Operating Current of Analog Input Buffer

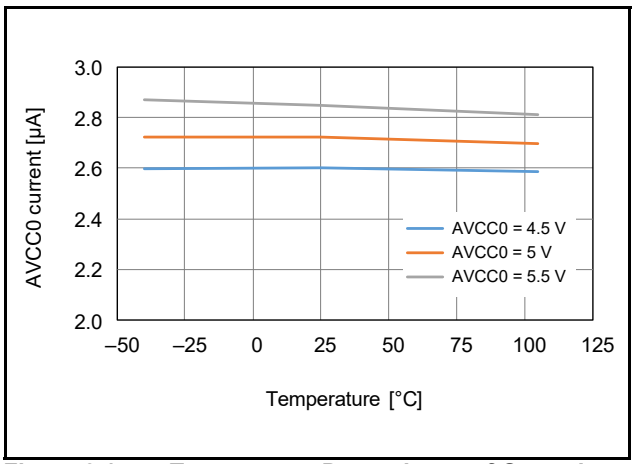


Figure 2.14 Temperature Dependence of Operating Current of Reference Buffer

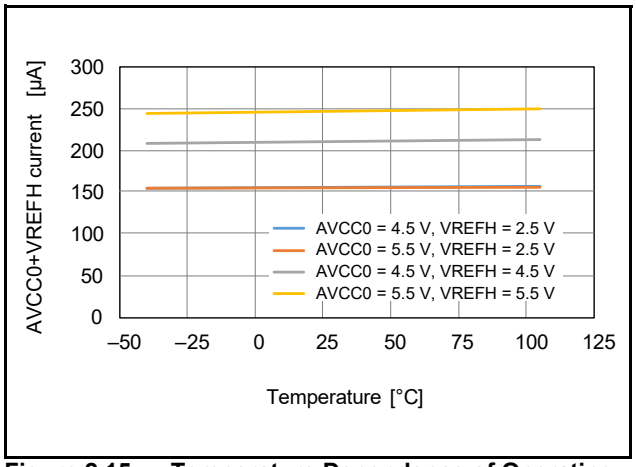


Figure 2.15 Temperature Dependence of Operating Current of 16-Bit D/A Converter

Table 2.16 DC Characteristics (13)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
12-bit A/D converter operating current	During A/D conversion (in high-speed conversion)	I_{AVCC0} (S12AD)	—	1.1	1.8	mA	
	During A/D conversion (in low-current mode)		—	0.6	1.1		
Reference power supply current	During A/D conversion (in high-speed conversion)	I_{REFH0}	—	74	122	µA	
	Current while waiting for A/D conversion (all units)		—	—	60	nA	
AVCC0 power down current		I_{STBY}	—	—	2.4	µA	

Note 1. Conditions for typical values are at AVCC0 = 5.0 V and T_a = 25°C.

Table 2.17 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible low-level output current (average value per pin)	P36 and P37		I_{OL}	4.0	mA
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current (maximum value per pin)	P36 and P37			4.0	
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current	Total of PD0 to PD4, PE0 to PE4		ΣI_{OL}	40	
	Total of P12 to P17, PA0 to PA4, PB0, PB1, PC0 to PC7			40	
	Total of P20 to P27, P30, P31, P36, P37, P60 to P67			40	
	Total of P70 to P74			40	
	Total of all output pins			80	
Permissible high-level output current (average value per pin)	P36 and P37		I_{OH}	–4.0	
	P16, P17, P60, P61, P70 to P74, PD0	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
	Ports other than above*1			–4.0	
Permissible high-level output current (maximum value per pin)	P36 and P37			–4.0	
	P16, P17, P60, P61, P70 to P74, PD0	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
	Ports other than above*1			–4.0	
Permissible high-level output current	Total of PD0 to PD4, PE0 to PE4		ΣI_{OH}	–40	
	Total of P12 to P17, PA0 to PA4, PB0, PB1, PC0 to PC7			–40	
	Total of P20 to P27, P30, P31, P36, P37, P60 to P67			–40	
	Total of P70 to P74			–40	
	Total of all output pins			–80	

Note 1. Drive capacities of port pins that are not 5-V tolerant and those to which the LCD functions are assigned are also switchable. Note that switching of drive capacities does not affect the I_{OH} characteristics in either the normal drive output mode or the high-drive output mode.

Table 2.18 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible low-level output current (average value per pin)	P36 and P37		I_{OL}	4.0	mA
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current (maximum value per pin)	P36 and P37			4.0	
	Ports other than above	Normal drive output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current	Total of PD0 to PD4, PE0 to PE4		ΣI_{OL}	30	
	Total of P12 to P17, PA0 to PA4, PB0, PB1, PC0 to PC7			30	
	Total of P20 to P27, P30, P31, P36, P37, P60 to P67			30	
	Total of P70 to P74			30	
	Total of all output pins			60	
Permissible high-level output current (average value per pin)	P36 and P37		I_{OH}	–4.0	
	P16, P17, P60, P61, P70 to P74, PD0	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
	Ports other than above*1			–4.0	
Permissible high-level output current (maximum value per pin)	P36 and P37			–4.0	
	P16, P17, P60, P61, P70 to P74, PD0	Normal drive output mode		–4.0	
		High-drive output mode		–8.0	
	Ports other than above*1			–4.0	
Permissible high-level output current	Total of PD0 to PD4, PE0 to PE4		ΣI_{OH}	–30	
	Total of P12 to P17, PA0 to PA4, PB0, PB1, PC0 to PC7			–30	
	Total of P20 to P27, P30, P31, P36, P37, P60 to P67			–30	
	Total of P70 to P74			–30	
	Total of all output pins			–60	

Note 1. Drive capacities of port pins that are not 5-V tolerant and those to which the LCD functions are assigned are also switchable. Note that switching of drive capacities does not affect the I_{OH} characteristics in either the normal drive output mode or the high-drive output mode.

Table 2.19 Output Voltage (1)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports	Normal drive output mode	V_{OL}	—	0.3	V	I_{OL} = 0.5 mA
		High-drive output mode		—	0.3		I_{OL} = 1.0 mA
High-level output voltage	P16, P17, P60, P61, P70 to P74, PD0	Normal drive output mode	V_{OH}	VCC – 0.3	—	V	I_{OH} = –0.5 mA
		High-drive output mode		VCC – 0.3	—		I_{OH} = –1.0 mA
	Other output pins*1			VCC – 0.3	—		I_{OH} = –0.5 mA

Note 1. Drive capacities of port pins that are not 5-V tolerant and those to which the LCD functions are assigned are also switchable. Note that switching of drive capacities does not affect the V_{OH} characteristics in either the normal drive output mode or the high-drive output mode.

Table 2.20 Output Voltage (2)

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 4.0 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for RIIC pins)	Normal drive output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins	Normal drive output mode		—	0.4		I_{OL} = 3.0 mA
		High-drive output mode		—	0.6		I_{OL} = 6.0 mA
High-level output voltage	P16, P17, P60, P61, P70 to P74, PD0	Normal drive output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA
	Other output pins*1			VCC – 0.5	—		I_{OH} = –1.0 mA

Note 1. Drive capacities of port pins that are not 5-V tolerant and those to which the LCD functions are assigned are also switchable. Note that switching of drive capacities does not affect the V_{OH} characteristics in either the normal drive output mode or the high-drive output mode.

Table 2.21 Output Voltage (3)

Conditions: 4.0 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for RIIC pins)	Normal drive output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins	Normal drive output mode		—	0.4		I_{OL} = 3.0 mA
		High-drive output mode		—	0.6		I_{OL} = 6.0 mA
High-level output voltage	P16, P17, P60, P61, P70 to P74, PD0	Normal drive output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA
	Other output pins*1			VCC – 0.8	—		I_{OH} = –2.0 mA

Note 1. Drive capacities of port pins that are not 5-V tolerant and those to which the LCD functions are assigned are also switchable. Note that switching of drive capacities does not affect the V_{OH} characteristics in either the normal drive output mode or the high-drive output mode.

Table 2.22 Thermal Resistance Value (Reference)

Item	Package	Symbol	Min.		Max.	Unit	Test Conditions
Thermal resistance	100-pin TFBGA (PTBG0100KD-A)	θ_{ja}	—	—	26.0	°C/W	JESD51-2 and JESD51-9 compliant
	100-pin LFQFP (PLQP0100KB-B)		—	—	40.2		JESD51-2 and JESD51-7 compliant
	80-pin LFQFP (PLQP0080KB-B)		—	—	40.0		
	64-pin LFQFP (PLQP0064KB-C)		—	—	41.4		
	48-pin LFQFP (PLQP0048KB-B)		—	—	49.0		
	40-pin HWQFN (PWQN0040KD-A)		—	—	19.8*1		
	100-pin TFBGA (PTBG0100KD-A)	Ψ_{jt}	—	—	0.24	°C/W	JESD51-2 and JESD51-9 compliant
	100-pin LFQFP (PLQP0100KB-B)		—	—	0.59		JESD51-2 and JESD51-7 compliant
	80-pin LFQFP (PLQP0080KB-B)		—	—	0.59		
	64-pin LFQFP (PLQP0064KB-C)		—	—	0.59		
	48-pin LFQFP (PLQP0048KB-B)		—	—	1.08		
	40-pin HWQFN (PWQN0040KD-A)		—	—	0.07*1		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

Note 1. This value applies when the exposed die pad for this purpose is connected to VSS.

2.4 Typical I/O Pin Output Characteristics

Table 2.23 Typical I/O Pin Normal Output V_{OH} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC–0.05	—	V	I_{OH} = –0.5 mA
			—	VCC–0.11	—		I_{OH} = –1.0 mA
			—	VCC–0.23	—		I_{OH} = –2.0 mA
			—	VCC–0.55	—		I_{OH} = –4.0 mA

Table 2.24 Typical I/O Pin Normal Output V_{OH} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC–0.03	—	V	I_{OH} = –0.5 mA
			—	VCC–0.07	—		I_{OH} = –1.0 mA
			—	VCC–0.13	—		I_{OH} = –2.0 mA
			—	VCC–0.27	—		I_{OH} = –4.0 mA

Table 2.25 Typical I/O Pin Normal Output V_{OH} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC–0.03	—	V	I_{OH} = –0.5 mA
			—	VCC–0.05	—		I_{OH} = –1.0 mA
			—	VCC–0.10	—		I_{OH} = –2.0 mA
			—	VCC–0.20	—		I_{OH} = –4.0 mA

Table 2.26 Typical I/O Pin Normal Output V_{OL} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.05	—	V	I_{OL} = 0.5 mA
			—	0.11	—		I_{OL} = 1.0 mA
			—	0.24	—		I_{OL} = 2.0 mA
			—	0.70	—		I_{OL} = 4.0 mA

Table 2.27 Typical I/O Pin Normal Output V_{OL} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.03	—	V	I_{OL} = 0.5 mA
			—	0.06	—		I_{OL} = 1.0 mA
			—	0.12	—		I_{OL} = 2.0 mA
			—	0.25	—		I_{OL} = 4.0 mA

Table 2.28 Typical I/O Pin Normal Output V_{OL} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
			—	0.04	—		I_{OL} = 1.0 mA
			—	0.09	—		I_{OL} = 2.0 mA
			—	0.18	—		I_{OL} = 4.0 mA

Table 2.29 Typical I/O Pin High-Drive Output V_{OH} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	P16, P17, P60, P61, P70 to P74, PD0	V_{OH}	—	VCC–0.03	—	V	I_{OH} = –0.5 mA
			—	VCC–0.05	—		I_{OH} = –1.0 mA
			—	VCC–0.10	—		I_{OH} = –2.0 mA
			—	VCC–0.22	—		I_{OH} = –4.0 mA
			—	VCC–0.48	—		I_{OH} = –8.0 mA
	Other output pins	V_{OH}	—	VCC–0.05	—	V	I_{OH} = –0.5 mA
			—	VCC–0.10	—		I_{OH} = –1.0 mA
			—	VCC–0.20	—		I_{OH} = –2.0 mA
			—	VCC–0.45	—		I_{OH} = –4.0 mA

Table 2.30 Typical I/O Pin High-Drive Output V_{OH} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	P16, P17, P60, P61, P70 to P74, PD0	V_{OH}	—	VCC–0.02	—	V	I_{OH} = –0.5 mA
			—	VCC–0.04	—		I_{OH} = –1.0 mA
			—	VCC–0.07	—		I_{OH} = –2.0 mA
			—	VCC–0.14	—		I_{OH} = –4.0 mA
			—	VCC–0.28	—		I_{OH} = –8.0 mA
	Other output pins	V_{OH}	—	VCC–0.03	—	V	I_{OH} = –0.5 mA
			—	VCC–0.06	—		I_{OH} = –1.0 mA
			—	VCC–0.12	—		I_{OH} = –2.0 mA
			—	VCC–0.24	—		I_{OH} = –4.0 mA

Table 2.31 Typical I/O Pin High-Drive Output V_{OH} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	P16, P17, P60, P61, P70 to P74, PD0	V_{OH}	—	VCC–0.02	—	V	I_{OH} = –0.5 mA
			—	VCC–0.03	—		I_{OH} = –1.0 mA
			—	VCC–0.06	—		I_{OH} = –2.0 mA
			—	VCC–0.11	—		I_{OH} = –4.0 mA
			—	VCC–0.23	—		I_{OH} = –8.0 mA
	Other output pins	V_{OH}	—	VCC–0.02	—	V	I_{OH} = –0.5 mA
			—	VCC–0.05	—		I_{OH} = –1.0 mA
			—	VCC–0.09	—		I_{OH} = –2.0 mA
			—	VCC–0.18	—		I_{OH} = –4.0 mA

Table 2.32 Typical I/O Pin High-Drive Output V_{OL} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
			—	0.05	—		I_{OL} = 1.0 mA
			—	0.10	—		I_{OL} = 2.0 mA
			—	0.21	—		I_{OL} = 4.0 mA
			—	0.49	—		I_{OL} = 8.0 mA

Table 2.33 Typical I/O Pin High-Drive Output V_{OL} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.03	—		I_{OL} = 1.0 mA
			—	0.06	—		I_{OL} = 2.0 mA
			—	0.12	—		I_{OL} = 4.0 mA
			—	0.25	—		I_{OL} = 8.0 mA

Table 2.34 Typical I/O Pin High-Drive Output V_{OL} Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.05	—		I_{OL} = 2.0 mA
			—	0.10	—		I_{OL} = 4.0 mA
			—	0.20	—		I_{OL} = 8.0 mA

2.5 AC Characteristics

2.5.1 Clock Timing

Table 2.35 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*3	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	
	Peripheral module clock (PCLKA)		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKC)		8	16	32	
	Peripheral module clock (PCLKD)		8	16	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 2.38, Clock Timing.

Table 2.36 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*3	System clock (ICLK)	f_{max}	8	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	
	Peripheral module clock (PCLKA)		8	12	12	
	Peripheral module clock (PCLKB)		8	12	12	
	Peripheral module clock (PCLKC)		8	12	12	
	Peripheral module clock (PCLKD)		8	12	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 2.38, Clock Timing.

Table 2.37 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKA)		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKC)*2		32.768			
	Peripheral module clock (PCLKD)*3		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The 24-bit Δ-Σ A/D converter cannot be used.
Note 3. The 12-bit A/D converter cannot be used.
Note 4. The maximum operating frequency listed above does not include errors of the external oscillator. For details on the range for the guaranteed operation, see Table 2.38, Clock Timing.

Table 2.38 Clock Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 2.16
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 2.17
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.00	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 2.18
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15.00	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 2.19
HOCO clock oscillation frequency		f_{HOCO}	31.52	32.00	32.48	MHz	T_a = –40 to +85°C
			31.68	32.00	32.32		T_a = –20 to +85°C
			31.36	32.00	32.64		T_a = –40 to +105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	41.3	μs	Figure 2.21
PLL input frequency*3		f_{PLLIN}	4	—	8	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	32	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	74.4	μs	Figure 2.22
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
Sub-clock oscillator oscillation frequency*4		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	—	0.5	—	s	Figure 2.23

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Only 32.768 kHz can be used.

Note 5. Reference values when a 32.768-kHz resonator is used.
After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

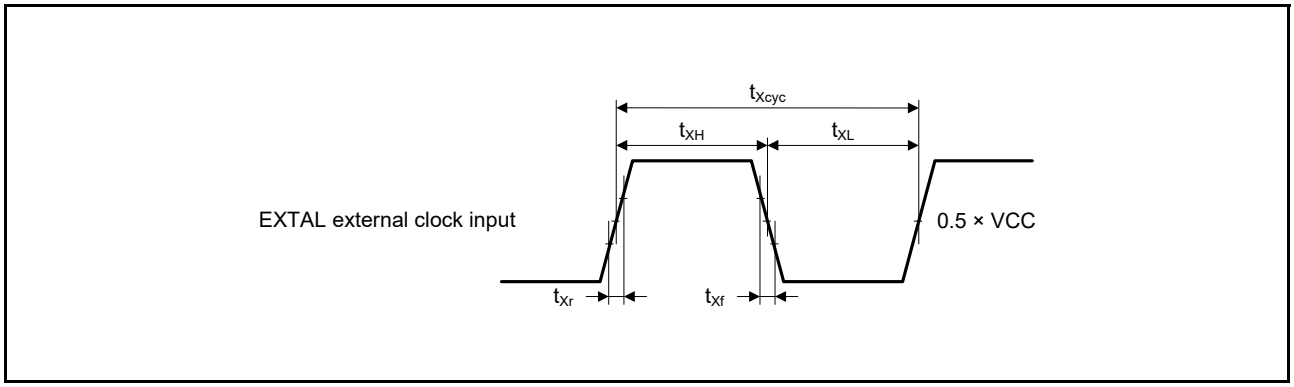


Figure 2.16 EXTAL External Clock Input Timing

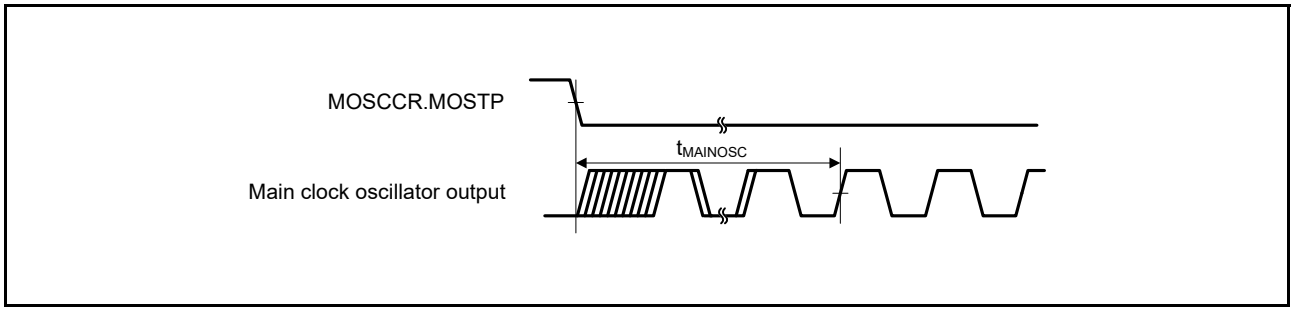


Figure 2.17 Main Clock Oscillation Start Timing

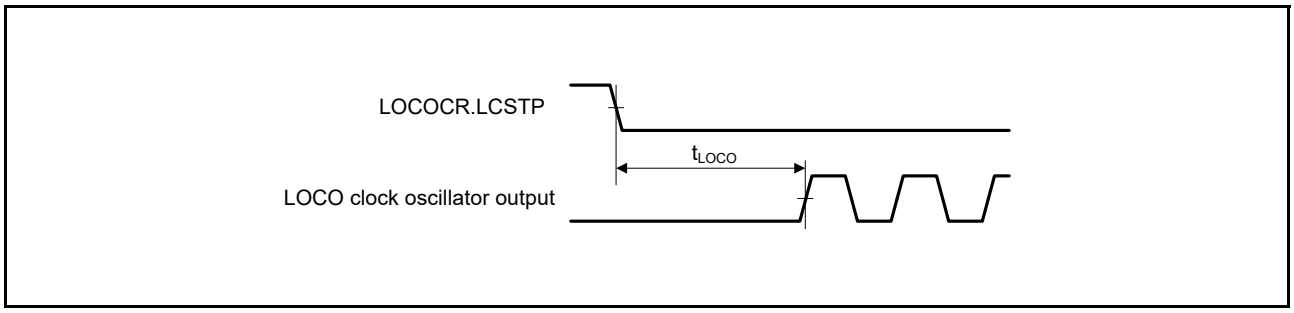


Figure 2.18 LOCO Clock Oscillation Start Timing

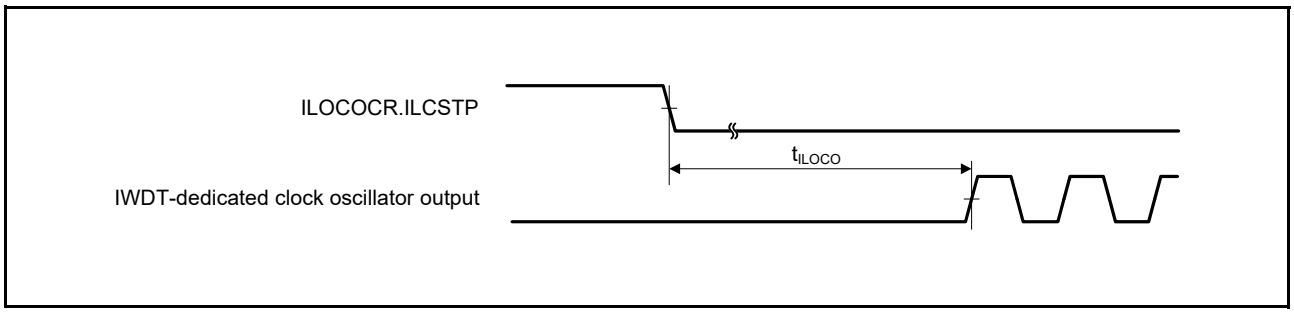


Figure 2.19 IWDT-Dedicated Clock Oscillation Start Timing

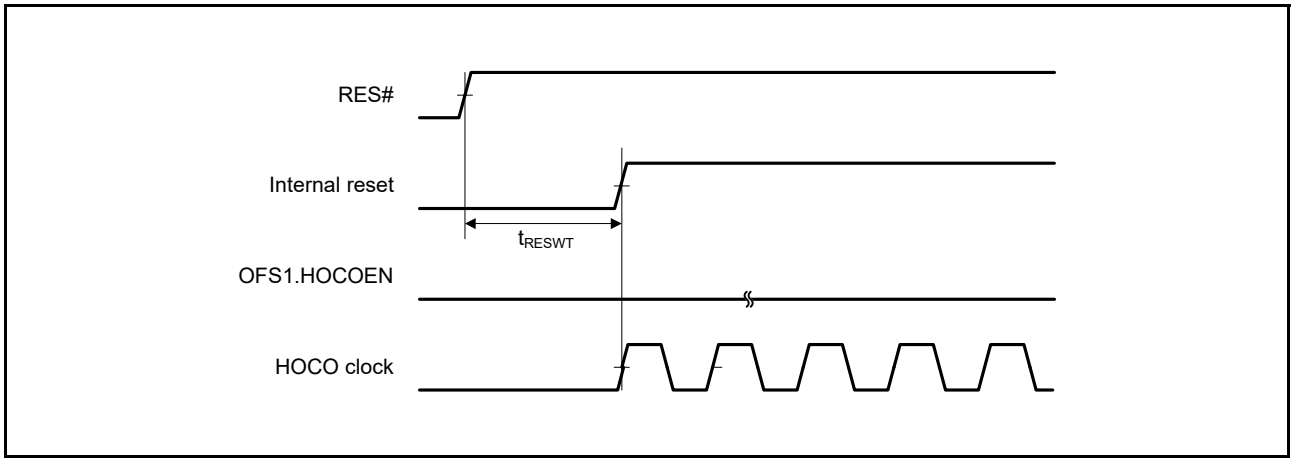


Figure 2.20 HOCO Clock Oscillation Start Timing (After Release from a Reset by Setting OFS1.HOCOEN Bit to 0)

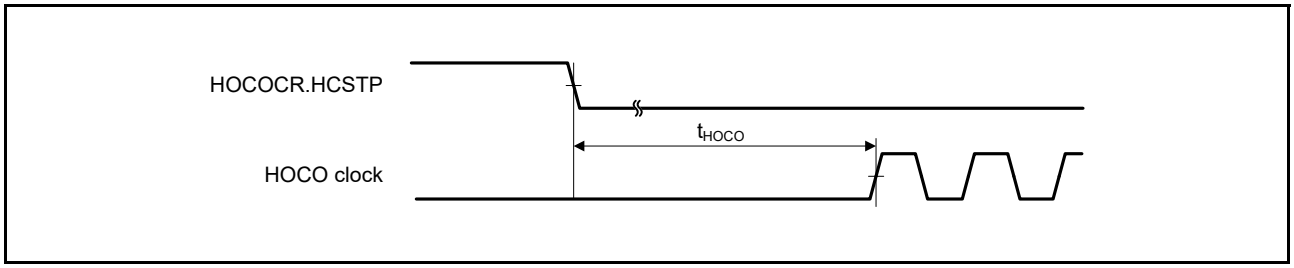


Figure 2.21 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

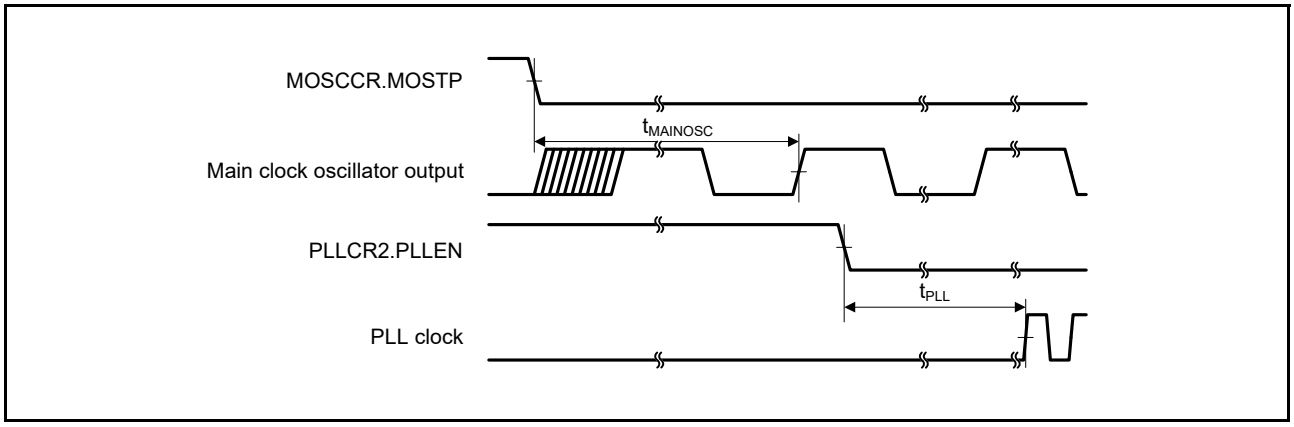


Figure 2.22 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Been Stabled)

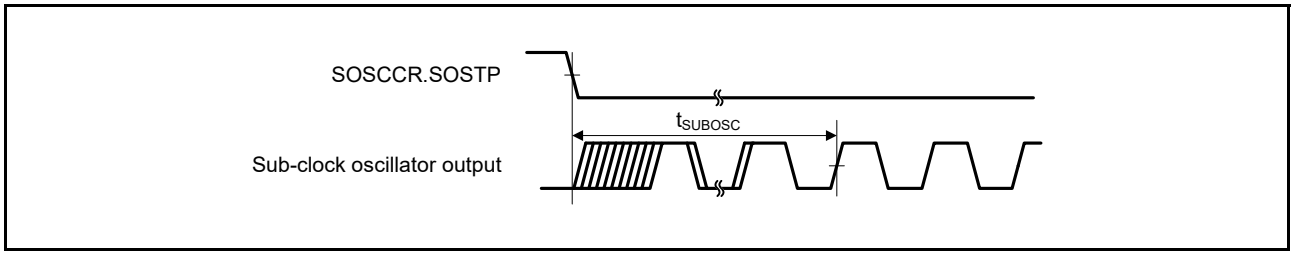


Figure 2.23 Sub-Clock Oscillation Start Timing

2.5.2 Reset Timing

Table 2.39 Reset Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 2.24
	Other than above	t_{RESW}	30	—	—	µs	Figure 2.25
Wait time after release from the RES# pin reset (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 2.24
	During fast startup time*2	t_{RESWT}	—	650	—	µs	
Wait time after release from the RES# pin reset (from a warm start)		t_{RESWT}	—	310	—	µs	Figure 2.25
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 2.26
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after release from the independent watchdog timer reset*3		t_{RESWT2}	—	350	—	µs	
Wait time after release from the software reset		t_{RESWT2}	—	220	—	µs	

Note 1. When the OFS1.LVDAS and OFS1.FASTSTUP bits are 1
Note 2. When the OFS1.LVDAS and/or OFS1.FASTSTUP bits are 0
Note 3. When the IWDTCR.CKS[3:0] bits are 0000b

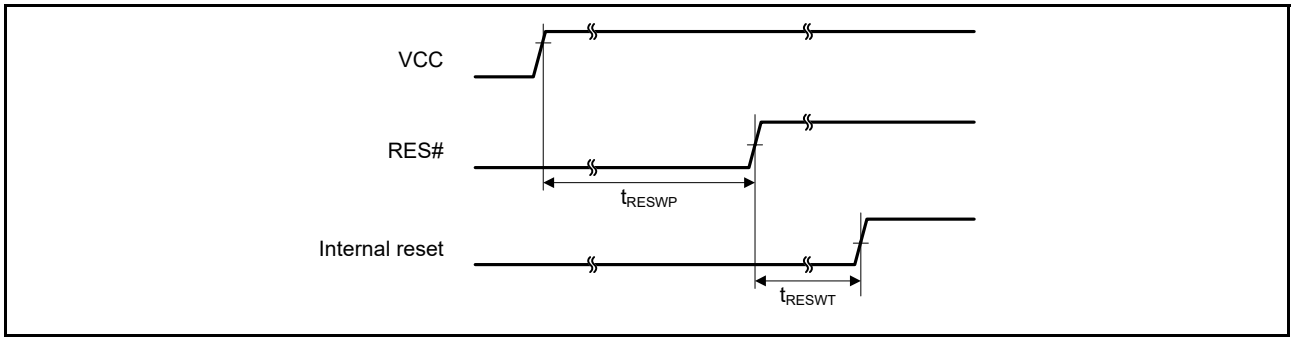


Figure 2.24 Reset Input Timing at Power-On

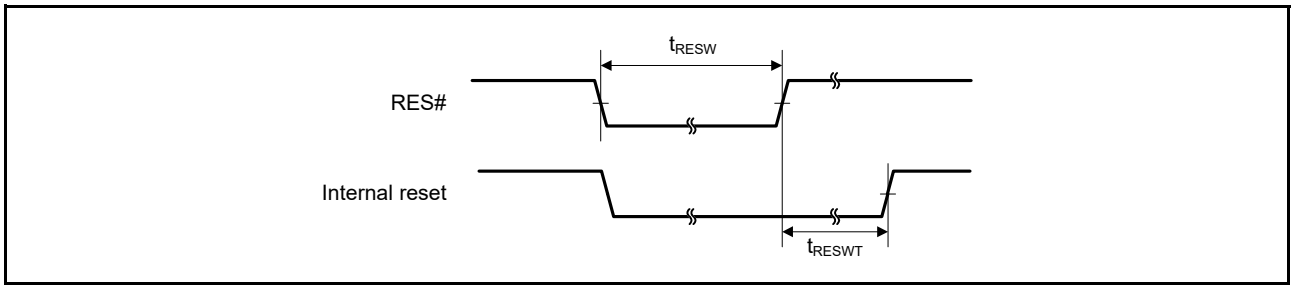


Figure 2.25 Reset Input Timing (1)

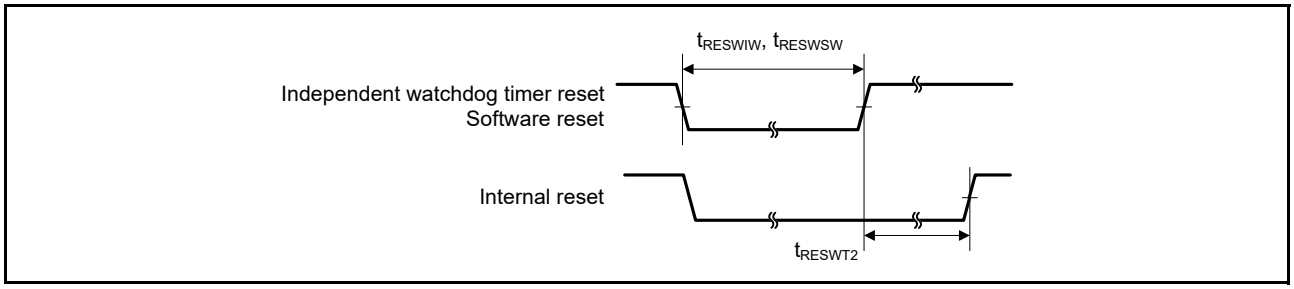


Figure 2.26 Reset Input Timing (2)

2.5.3 Timing of Recovery from Low Power Consumption Modes

Table 2.40 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 2.27
		External clock input to main clock oscillator	Main clock oscillator operating*3	t_{SBYEX}	—	35	50	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	650	800	µs	
		HOCO clock oscillator operating		t_{SBYHO}	—	40	55	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 20 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h
Note 3. When the frequency of the external clock is 20 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h

Table 2.41 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 2.27
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	600	750	µs	
		HOCO clock oscillator operating*6		t_{SBYHO}	—	40	50	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 12 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h
Note 3. This is the case when PLL is selected as the system clock and its frequency division is set to be 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h
Note 4. When the frequency of the external clock is 12 MHz
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h
Note 5. This is the case when PLL is selected as the system clock and its frequency division is set to be 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h
Note 6. This is the case when HOCO is selected as the system clock and its frequency division is set to be 8 MHz.

Table 2.42 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 2.27

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

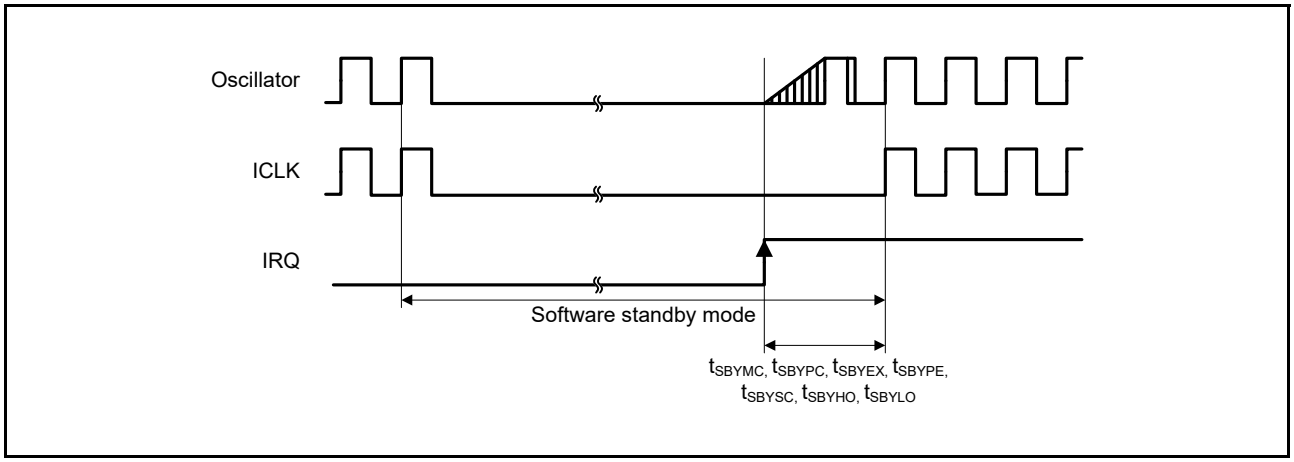


Figure 2.27 Software Standby Mode Recovery Timing

Table 2.43 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2.0	3.5	µs	Figure 2.28
	Middle-speed mode*3	t_{DSLP}	—	3.0	4.0	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz
Note 3. When the frequency of the system clock is 12 MHz
Note 4. When the frequency of the system clock is 32 kHz.

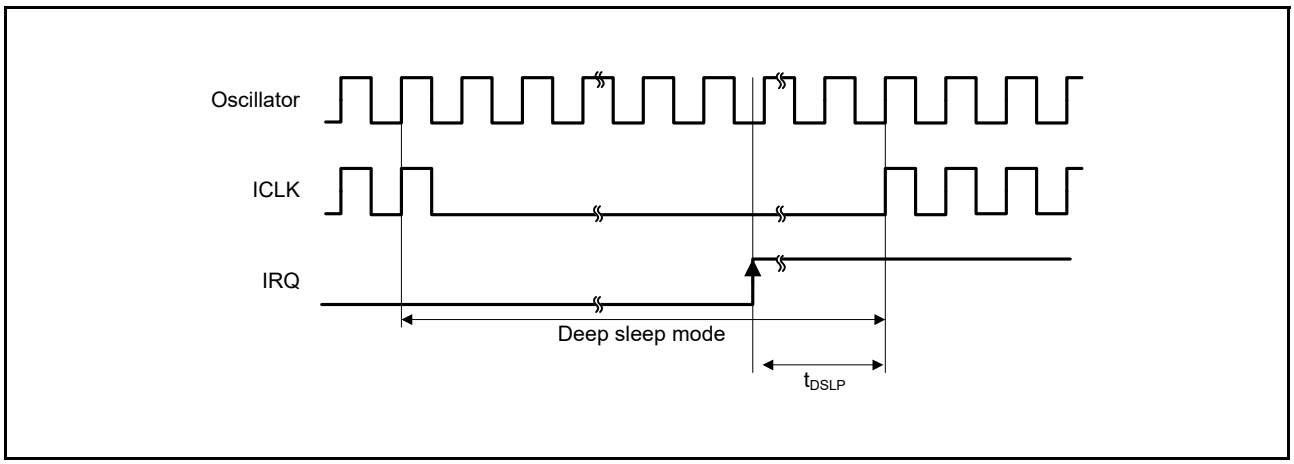


Figure 2.28 Deep Sleep Mode Recovery Timing

Table 2.44 Operating Mode Transition Time

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10.0	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	215	—	µs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	185	—	µs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK are not divided.

2.5.4 Control Signal Timing

Table 2.45 Control Signal Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	2 × t_{Pcyc} ≤ 200 ns
		2 × t_{Pcyc}*1	—	—			2 × t_{Pcyc} > 200 ns
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	3 × t_{NMICK} ≤ 200 ns
		3.5 × t_{NMICK}*2	—	—			3 × t_{NMICK} > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	2 × t_{Pcyc} ≤ 200 ns
		2 × t_{Pcyc}*1	—	—			2 × t_{Pcyc} > 200 ns
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	3 × t_{IRQCK} ≤ 200 ns
		3.5 × t_{IRQCK}*3	—	—			3 × t_{IRQCK} > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

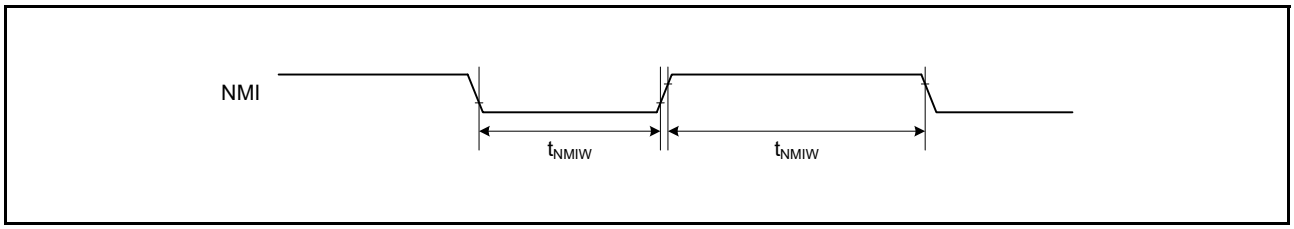


Figure 2.29 NMI Interrupt Input Timing

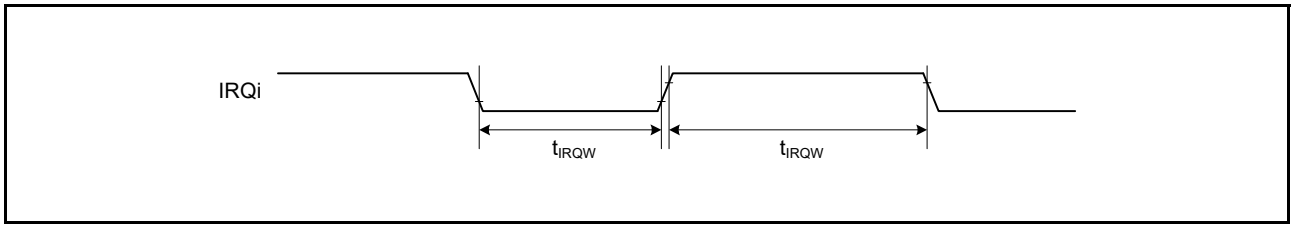


Figure 2.30 IRQ Interrupt Input Timing

2.5.5 Timing of On-Chip Peripheral Modules

2.5.5.1 I/O ports

Table 2.46 Timing of I/O ports

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	—	t_{Pcyc}	Figure 2.31

Note 1. t_{Pcyc}: PCLK cycle

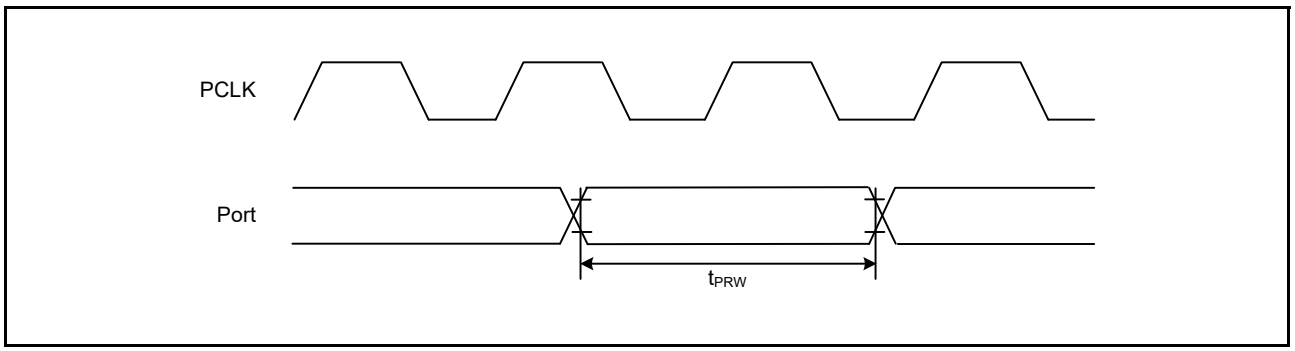


Figure 2.31 I/O Port Input Timing

2.5.5.2 MTU

Table 2.47 Timing of MTU

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	—	t_{Pcyc}	Figure 2.32
		Both-edge setting		2.5	—	—		
	Input capture input rise/fall time		t_{TICr}, t_{TICf}	—	—	0.1	µs/V	
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	—	t_{Pcyc}	Figure 2.33
		Both-edge setting		2.5	—	—		
		Phase counting mode		2.5	—	—		
	Timer clock rise/fall time		t_{TCKr}, t_{TCKf}	—	—	0.1	µs/V	

Note 1. t_{Pcyc}: PCLK cycle

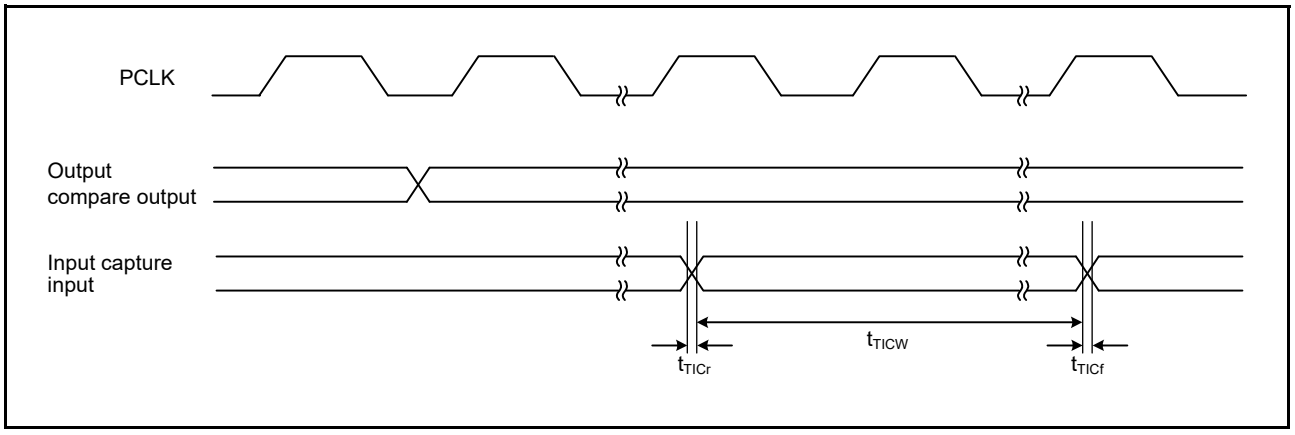


Figure 2.32 MTU Input/Output Timing

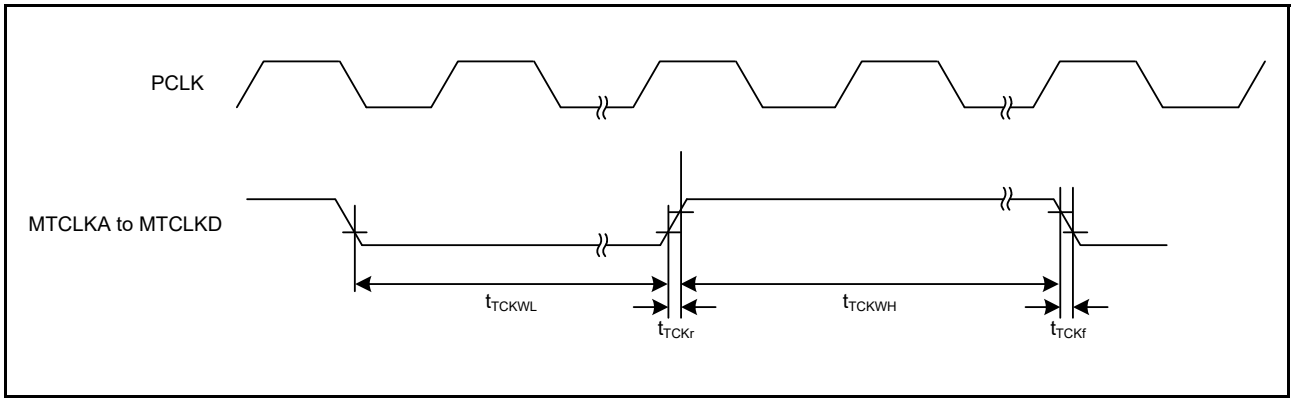


Figure 2.33 MTU Clock Input Timing

2.5.5.3 POE

Table 2.48 Timing of POE

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POE# input pulse width		t_{POEW}	1.5	—	—	t_{Pcyc}	Figure 2.34
	POE# input rise/fall time		t_{POEr}, t_{POEf}	—	—	0.1	µs/V	
	Output disable time	Transition of the POE# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	µs	Figure 2.35 When detecting falling edges (ICSRm.POEnM[1:0] = 00 (m = 1, 2; n = 0 to 3, 8))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	µs	Figure 2.36
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	µs	Figure 2.37 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	µs	Figure 2.38

Note 1. t_{Pcyc}: PCLK cycle

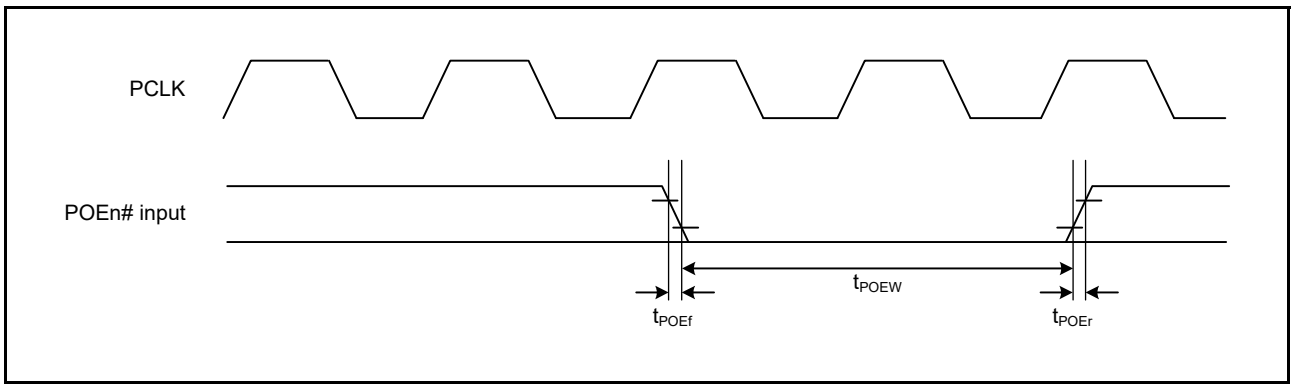


Figure 2.34 POE Input Timing (n = 0 to 3, 8)

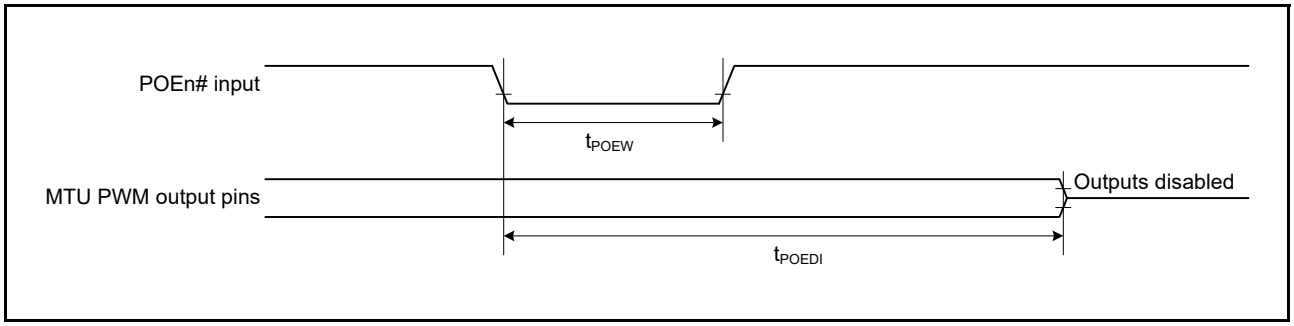
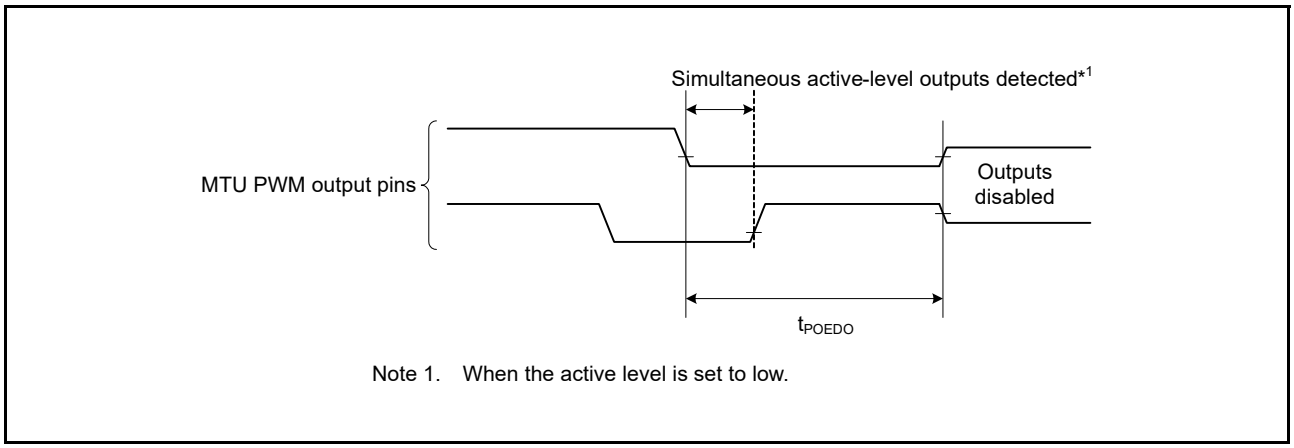


Figure 2.35 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.36 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

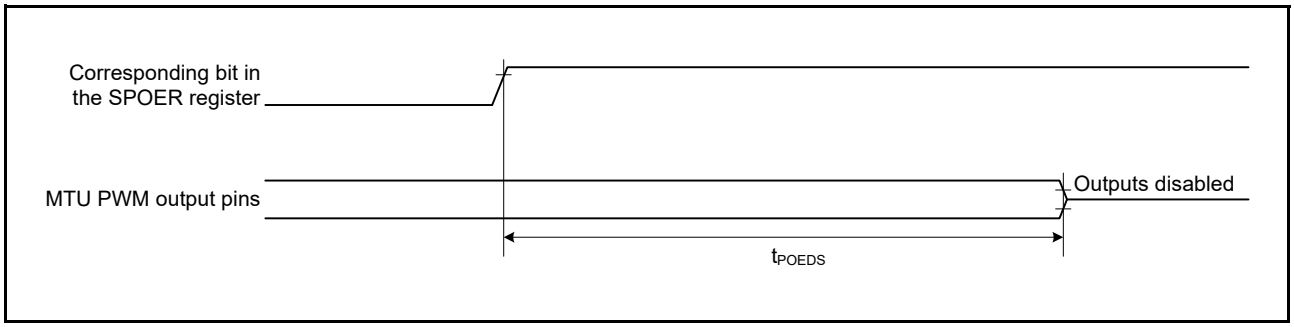


Figure 2.37 Output Disable Time for POE in Response to the Register Setting

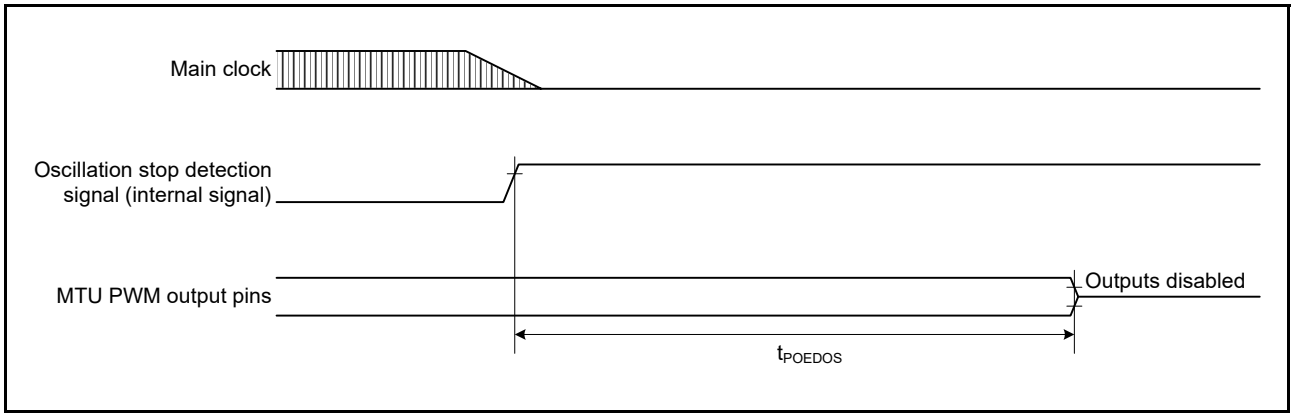


Figure 2.38 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.5.5.4 TMR

Table 2.49 Timing of TMR

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	—	t_{Pcyc}	Figure 2.39
		Both-edge setting		2.5	—	—		
	Timer clock rise/fall time		t_{TMCr}, t_{TMCf}	—	—	0.1	μs/V	

Note 1. t_{Pcyc}: PCLK cycle

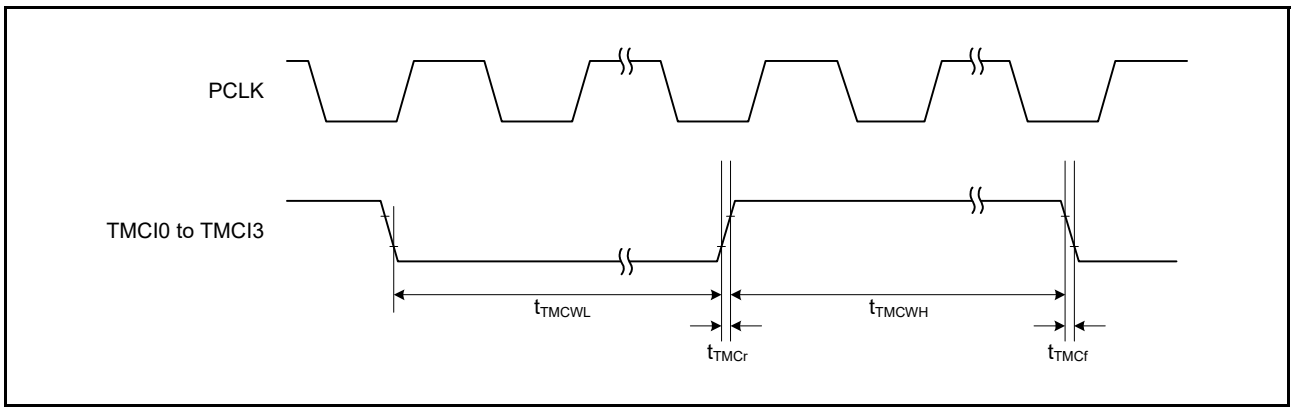


Figure 2.39 TMR Clock Input Timing

2.5.5.5 SCI

Table 2.50 Timing of SCI

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle time		Asynchronous	t_{Scyc}	4	—	—	t_{Pcyc}	Figure 2.40
			Clock synchronous		6	—	—		
	Input clock pulse width			t_{SCKW}	0.4	—	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	—	20	ns	
	Input clock fall time			t_{SCKf}	—	—	20	ns	
	Output clock cycle time		Asynchronous	t_{Scyc}	16	—	—	t_{Pcyc}	
			Clock synchronous		4	—	—		
	Output clock pulse width			t_{SCKW}	0.4	—	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	—	20	ns	
	Output clock fall time			t_{SCKf}	—	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	—	40	ns	Figure 2.41
	Transmit data delay time (slave)	Clock synchronous	VCC ≥ 2.7 V		—	—	65	ns	
			VCC < 2.7 V		—	—	100	ns	
	Receive data setup time (master)	Clock synchronous	VCC ≥ 2.7 V	t_{RXS}	65	—	—	ns	
			VCC < 2.7 V		90	—	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	—	ns	

Note 1. t_{Pcyc}: PCLK cycle

Table 2.51 Timing of Simple I²C

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I²C (Standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 2.42
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple I²C (Fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 2.42
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{Pcyc}: PCLK cycle
Note 1. C_b is the total capacitance of the bus lines.

Table 2.52 Timing of Simple SPI

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.43
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC ≥ 2.7 V	t_{SU}	65	—	ns	Figure 2.44, Figure 2.45
		VCC < 2.7 V		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC ≥ 2.7 V		—	65		
		VCC < 2.7 V		—	100		
	Data output hold time (master)	VCC ≥ 2.7 V	t_{OH}	–10	—	ns	
		VCC < 2.7 V		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 2.46, Figure 2.47
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

2.5.5.6 RIIC

Table 2.53 Timing of RIIC

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.42
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.42
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

2.5.5.7 RSPI

Table 2.54 Timing of RSPI

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF, when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.43
		Slave			4	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC ≥ 2.7 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			VCC < 2.7 V		—	15		
		Input			—	0.1	µs/V	
	Data input setup time	Master	VCC ≥ 2.7 V	t_{SU}	10	—	ns	Figure 2.44 to Figure 2.47
			VCC < 2.7 V		30	—		
		Slave			10	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	20	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC ≥ 2.7 V	t_{OD}	—	14	ns	
			VCC < 2.7 V		—	30		
		Slave	VCC ≥ 2.7 V		—	50		
			VCC < 2.7 V		—	85		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	VCC ≥ 2.7 V	t_{Dr}, t_{Df}	—	10	ns	
			VCC < 2.7 V		—	15		
		Input			—	1	µs	
	SSL rise/fall time	Output	VCC ≥ 2.7 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			VCC < 2.7 V		—	15	ns	
		Input			—	1	µs	
RSPI	Slave access time		VCC ≥ 2.7 V	t_{SA}	—	6	t_{Pcyc}	Figure 2.46, Figure 2.47
			VCC < 2.7 V		—	7		
	Slave output release time		VCC ≥ 2.7 V	t_{REL}	—	5	t_{Pcyc}	
			VCC < 2.7 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)

Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

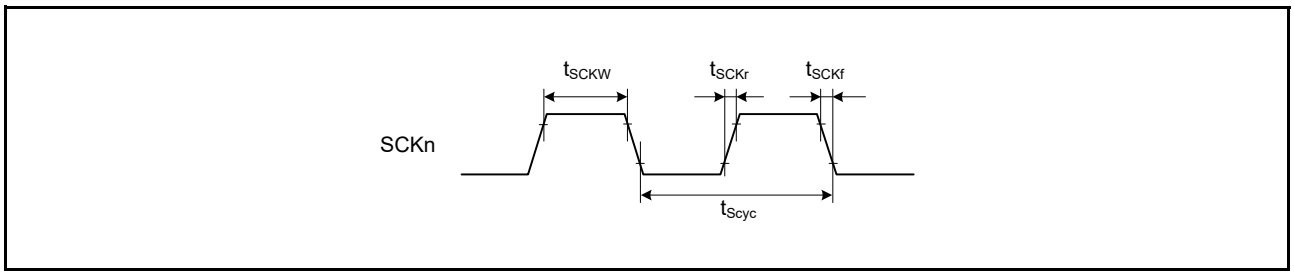


Figure 2.40 SCK Clock Input Timing (n = 0, 1, 5, 6, 8, 9, 12)

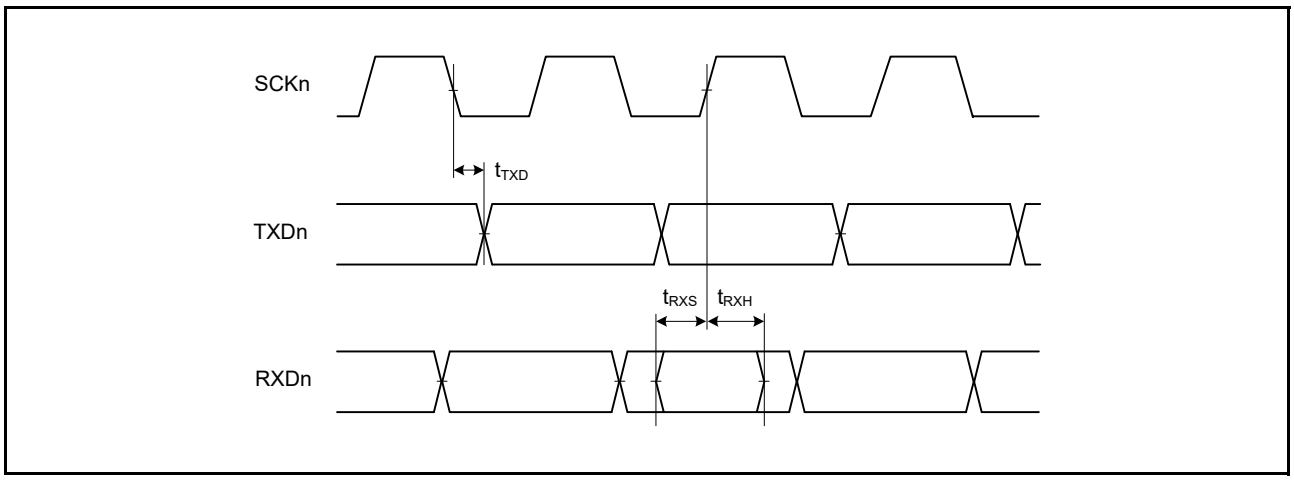
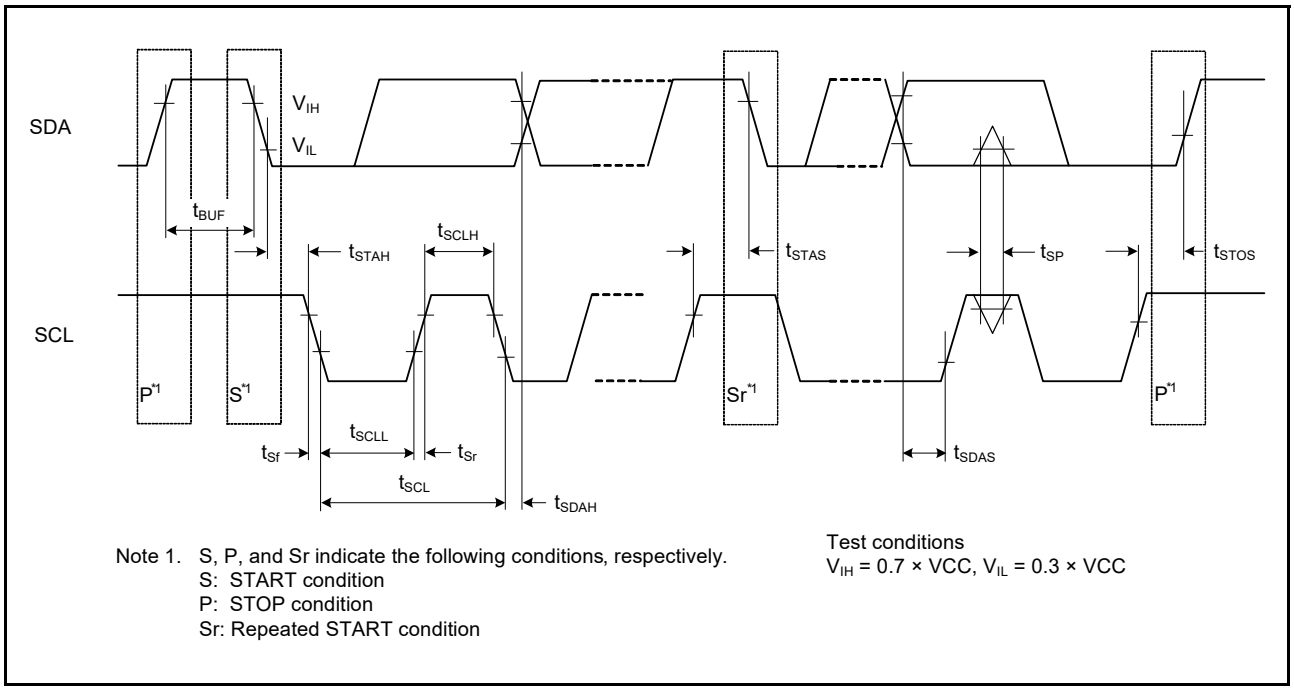


Figure 2.41 SCI Input/Output Timing: Clock Synchronous Mode (n = 0, 1, 5, 6, 8, 9, 12)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.42 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

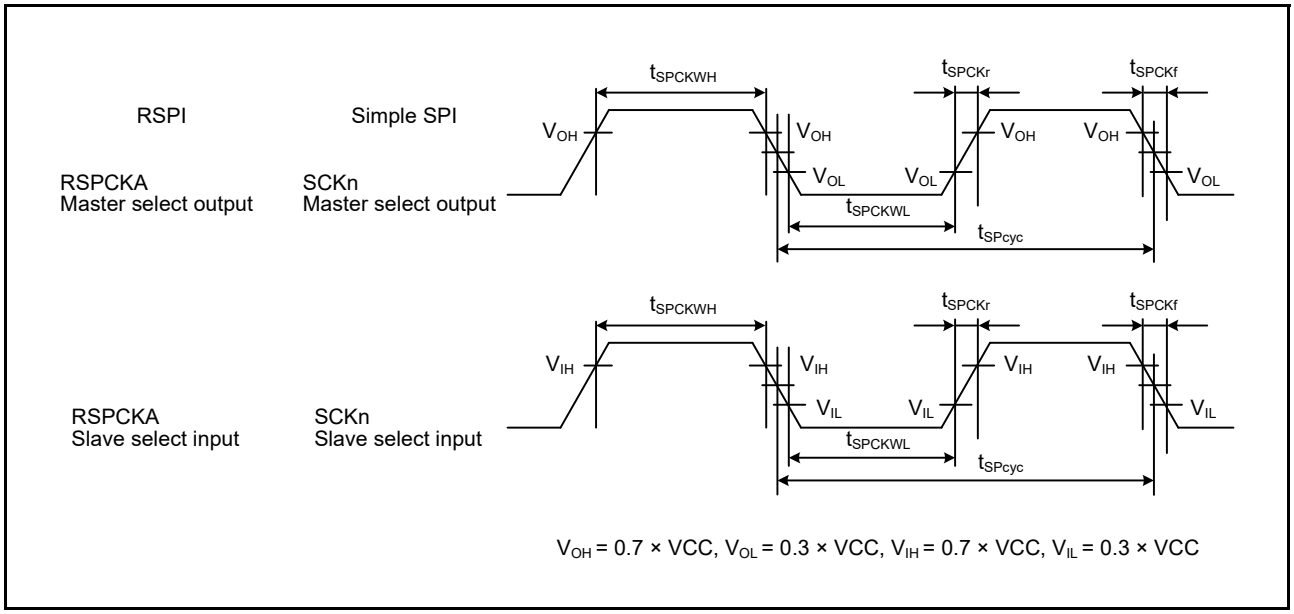


Figure 2.43 RSPI Clock Timing and Simple SPI Clock Timing (n = 0, 1, 5, 6, 8, 9, 12)

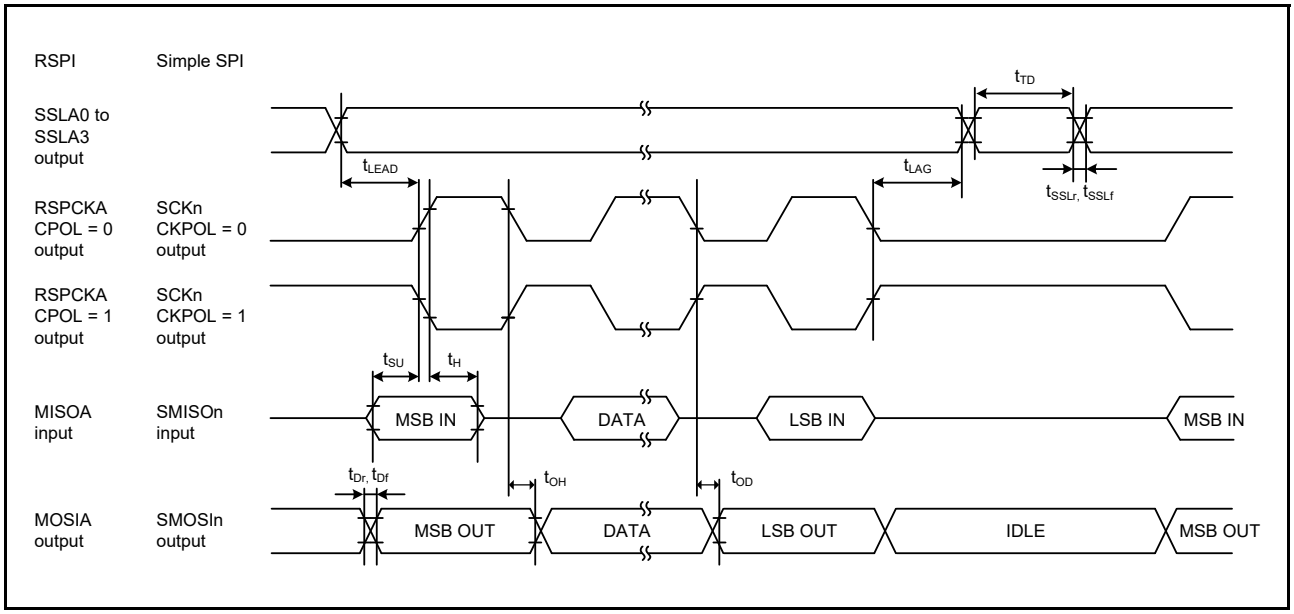


Figure 2.44 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1) (n = 0, 1, 5, 6, 8, 9, 12)

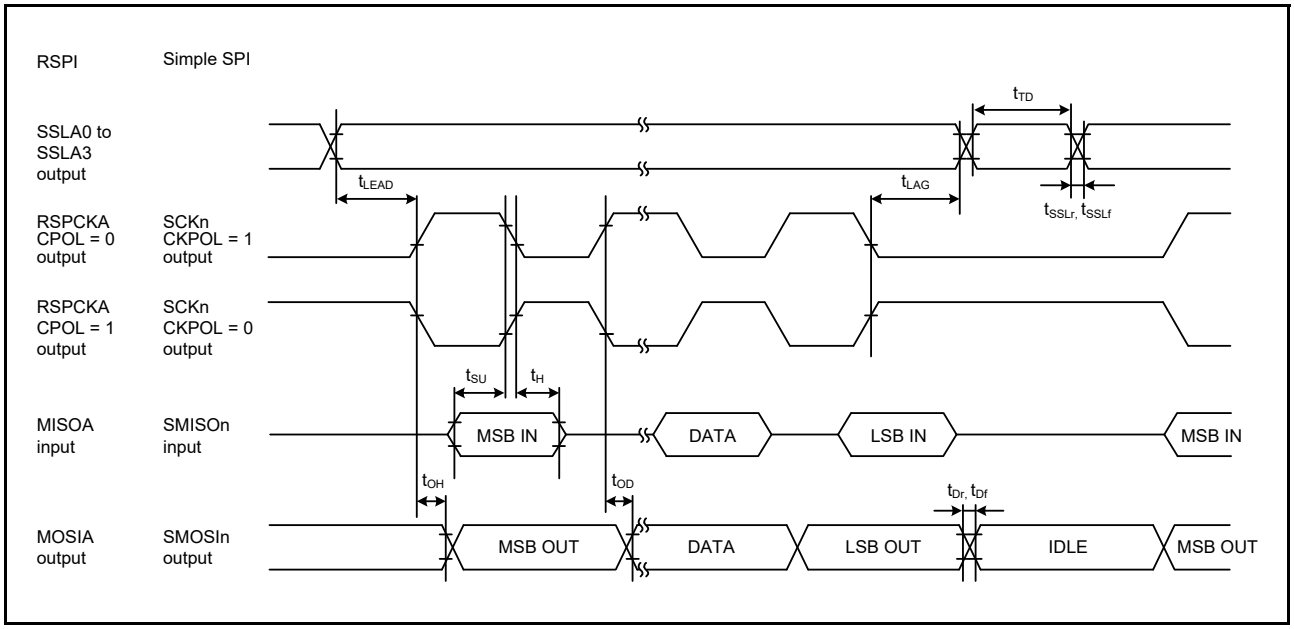


Figure 2.45 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0) (n = 0, 1, 5, 6, 8, 9, 12)

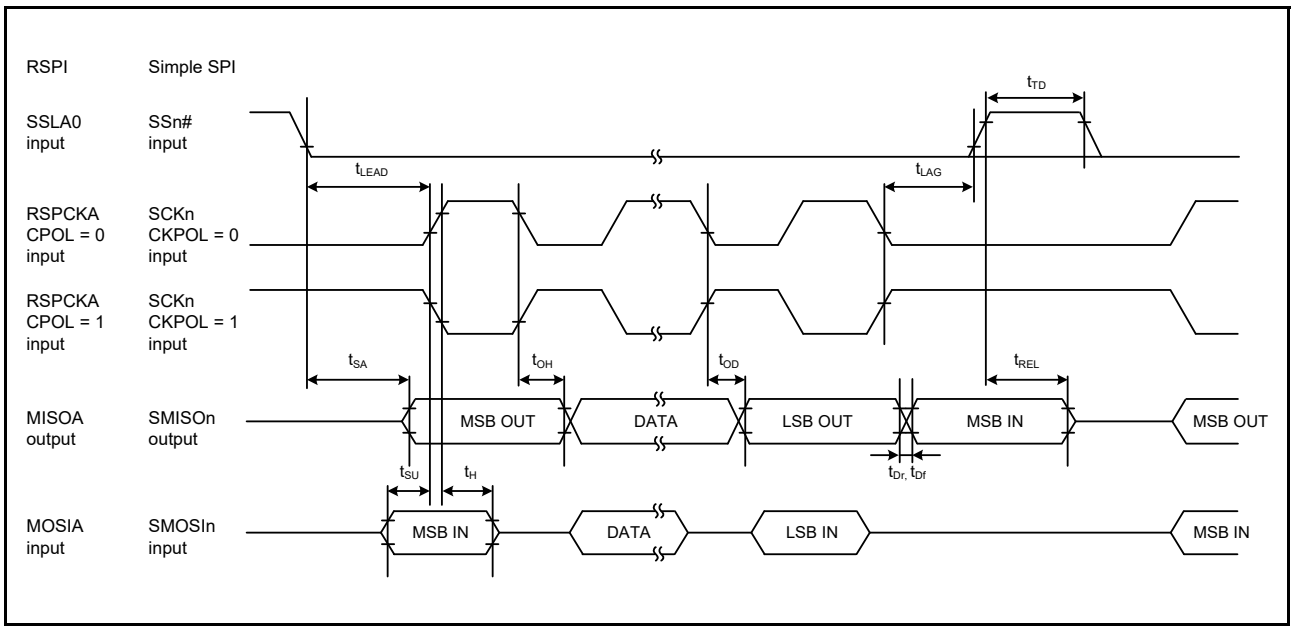


Figure 2.46 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1) (n = 0, 1, 5, 6, 8, 9, 12)

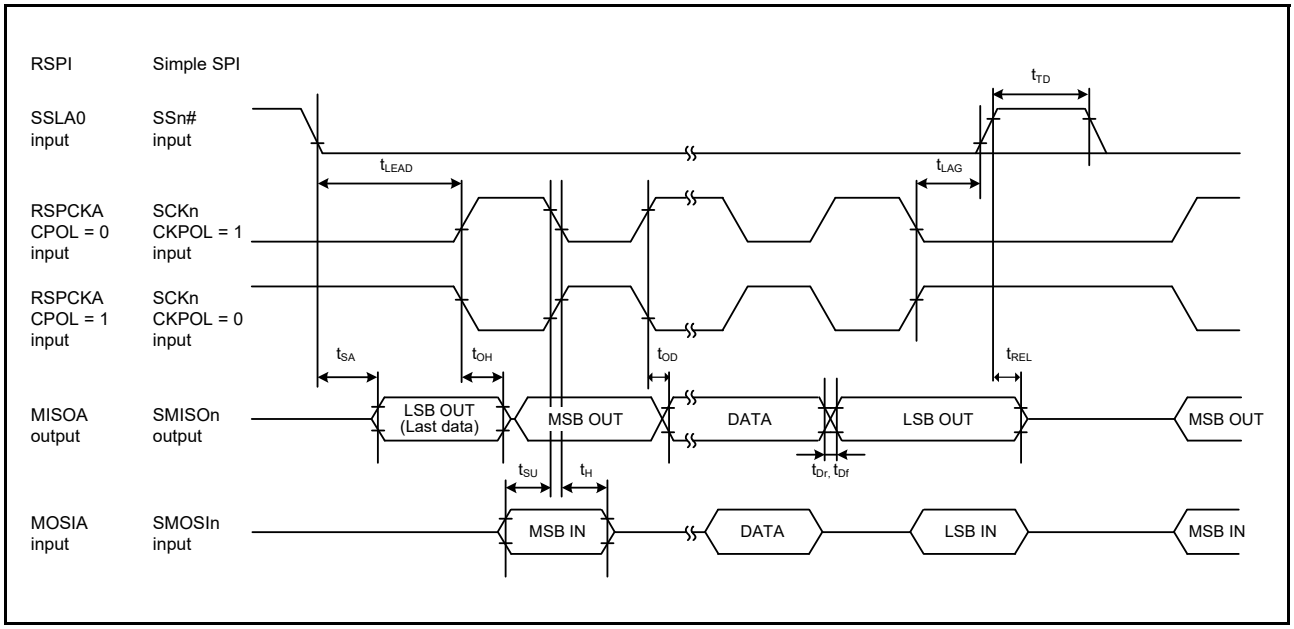


Figure 2.47 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0) (n = 0, 1, 5, 6, 8, 9, 12)

2.5.5.8 A/D converter Trigger

Table 2.55 Timing of A/D converter Trigger)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
A/D converter	Trigger input pulse width	t_{TRGW}	1.5	—	—	t_{Pcyc}	Figure 2.48

Note 1. t_{Pcyc}: PCLK cycle

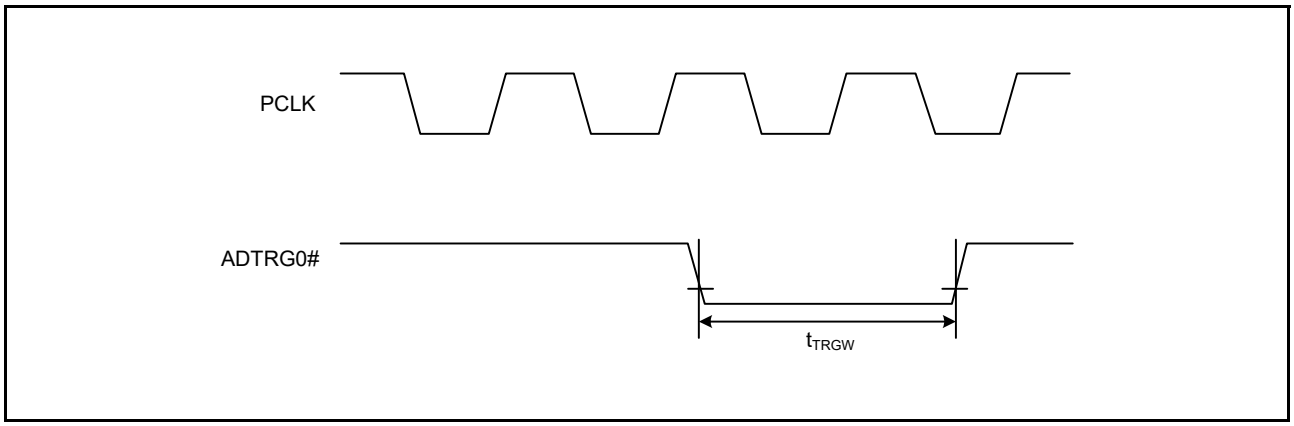


Figure 2.48 A/D Converter External Trigger Input Timing

2.5.5.9 CAC

Table 2.56 Timing of CAC

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
CAC	CACREF input pulse width	$t_{Pcyc} \leq t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}	—			
	CACREF input rise/fall time		$t_{CACREFr}$, $t_{CACREFf}$	—	—	0.1	µs/V	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle

2.5.5.10 CLKOUT

Table 2.57 Timing of CLKOUT

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
CLKOUT	CLKOUT pin output cycle*3	VCC ≥ 2.7 V	t_{Ccyc}	62.5	—	—	ns	Figure 2.49
		VCC < 2.7 V		125	—			
	CLKOUT pin high pulse width*2	VCC ≥ 2.7 V	t_{CH}	15	—	—	ns	
		VCC < 2.7 V		30	—			
	CLKOUT pin low pulse width*2	VCC ≥ 2.7 V	t_{CL}	15	—	—	ns	
		VCC < 2.7 V		30	—			
	CLKOUT pin output rise time	VCC ≥ 2.7 V	t_{Cr}	—	—	12	ns	
		VCC < 2.7 V			—	25		
	CLKOUT pin output fall time	VCC ≥ 2.7 V	t_{Cf}	—	—	12	ns	
		VCC < 2.7 V			—	25		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. When the LOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 000b), set the clock output division ratio selection to divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).
Note 3. When the EXTAL external clock input or an oscillator is used with divided by 1 (the CKOCR.CKOSEL[2:0] bits are 010b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

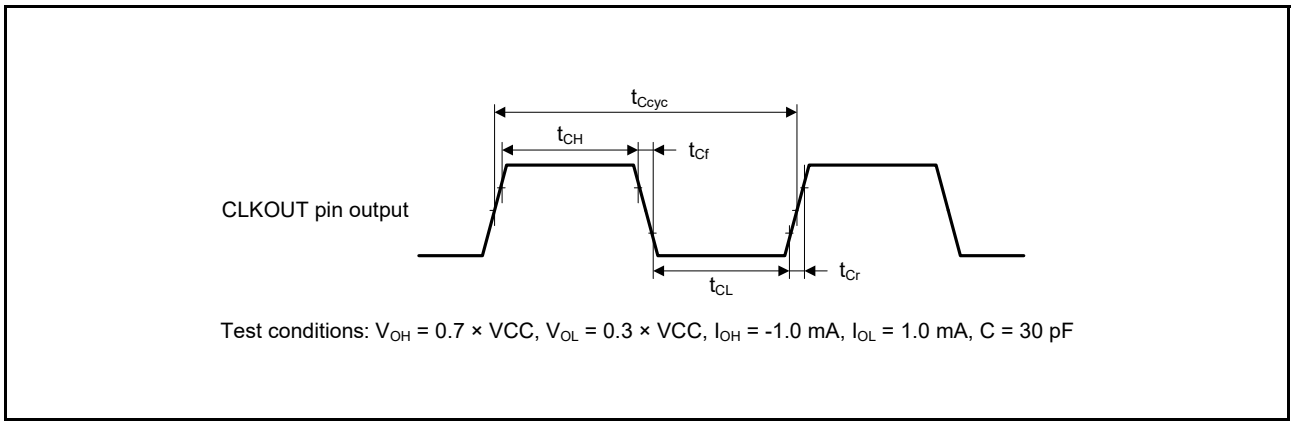


Figure 2.49 CLKOUT Output Timing

2.6 LCD Characteristics

2.6.1 External Resistance Division Method

(1) Static Display Mode

Table 2.58 LCD Characteristics

Conditions: 2.0 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.0	—	VCC	V	

(2) 1/2 Bias Method, 1/4 Bias Method

Table 2.59 LCD Characteristics

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.7	—	VCC	V	

(3) 1/3 Bias Method

Table 2.60 LCD Characteristics

Conditions: 2.5 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.5	—	VCC	V	

2.6.2 Internal Voltage Boosting Method

Table 2.61 Internal Voltage Boosting Method

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Value	Test Conditions
External capacitance connected between CAPH and CAPL pins	0.47 µF ±30%	
External capacitance connected to V_{L1} to V_{L4} pins	0.47 µF ±30%	

(1) 1/3 Bias Method

Table 2.62 Internal Voltage Boosting Method LCD Characteristics

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD output voltage variation range	V_{L1}	0.9	1.0	1.08	V	VLCD = 04h
		0.95	1.05	1.13	V	VLCD = 05h
		1	1.1	1.18	V	VLCD = 06h
		1.05	1.15	1.23	V	VLCD = 07h
		1.1	1.2	1.28	V	VLCD = 08h
		1.15	1.25	1.33	V	VLCD = 09h
		1.2	1.3	1.38	V	VLCD = 0Ah
		1.25	1.35	1.43	V	VLCD = 0Bh
		1.3	1.4	1.48	V	VLCD = 0Ch
		1.35	1.45	1.53	V	VLCD = 0Dh
		1.4	1.5	1.58	V	VLCD = 0Eh
		1.45	1.55	1.63	V	VLCD = 0Fh
		1.5	1.6	1.68	V	VLCD = 10h
		1.55	1.65	1.73	V	VLCD = 11h
		1.6	1.70	1.78	V	VLCD = 12h
		1.65	1.75	1.83	V	VLCD = 13h
Doubler output voltage	V_{L2}	$2V_{L1}$ – 0.10	$2V_{L1}$	$2V_{L1}$	V	
Tripler output voltage	V_{L4}	$3V_{L1}$ – 0.15	$3V_{L1}$	$3V_{L1}$	V	
Reference voltage setup time*1	t_{VL1S}	5	—	—	ms	
Voltage boost wait time*2	t_{VLWT}	500	—	—	ms	

Note 1. This is the required wait time from when the reference voltage is specified by the VLCD register (or when the internal voltage boosting method is selected (LCDM0.MDSET1 and MDSET0 = 01b) if the default reference voltage value is used) until voltage boosting starts (VLCON = 1).

Note 2. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 Bias Method

Table 2.63 Internal Voltage Boosting Method LCD Characteristics

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD output voltage variation range	V_{L1}	0.9	1.0	1.08	V	VLCD = 04h
		0.95	1.05	1.13	V	VLCD = 05h
		1	1.1	1.18	V	VLCD = 06h
		1.05	1.15	1.23	V	VLCD = 07h
		1.1	1.2	1.28	V	VLCD = 08h
		1.15	1.25	1.33	V	VLCD = 09h
		1.2	1.3	1.38	V	VLCD = 0Ah
Doubler output voltage	V_{L2}	$2V_{L1}$ – 0.08	$2V_{L1}$	$2V_{L1}$	V	
Tripler output voltage	V_{L3}	$3V_{L1}$ – 0.12	$3V_{L1}$	$3V_{L1}$	V	
Quadruply output voltage	V_{L4}	$4V_{L1}$ – 0.16	$4V_{L1}$	$4V_{L1}$	V	
Reference voltage setup time*1	t_{VL1S}	5	—	—	ms	
Voltage boost wait time*2	t_{VLWT}	500	—	—	ms	

Note 1. This is the required wait time from when the reference voltage is specified by the VLCD register (or when the internal voltage boosting method is selected (LCDM0.MDSET1 and MDSET0 = 01b) if the default reference voltage value is used) until voltage boosting starts (VLCON = 1).

Note 2. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.6.3 Capacitor Split Method

Table 2.64 Capacitive Divider Method

Conditions: 2.2 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Value	Test Conditions
External capacitance connected between CAPH and CAPL pins	0.47 µF ±30%	
External capacitor connected to V_{L1} pin	0.47 µF ±30%	
External capacitor connected to V_{L2} pin	0.47 µF ±30%	
External capacitor connected to V_{L4} pin	0.47 µF ±30%	

(1) 1/3 Bias Method

Table 2.65 Capacitive Divider Method LCD Characteristics

Conditions: 2.2 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{L4} voltage	V_{L4}	—	VCC	—	V	
V_{L2} voltage	V_{L2}	$2/3V_{L4}$ – 0.07	$2/3V_{L4}$	$2/3V_{L4}$ + 0.07	V	
V_{L1} voltage	V_{L1}	$1/3V_{L4}$ – 0.08	$2/3V_{L4}$	$2/3V_{L4}$ + 0.08	V	
Capacitor split wait time*1	t_{WAIT}	100	—	—	ms	

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

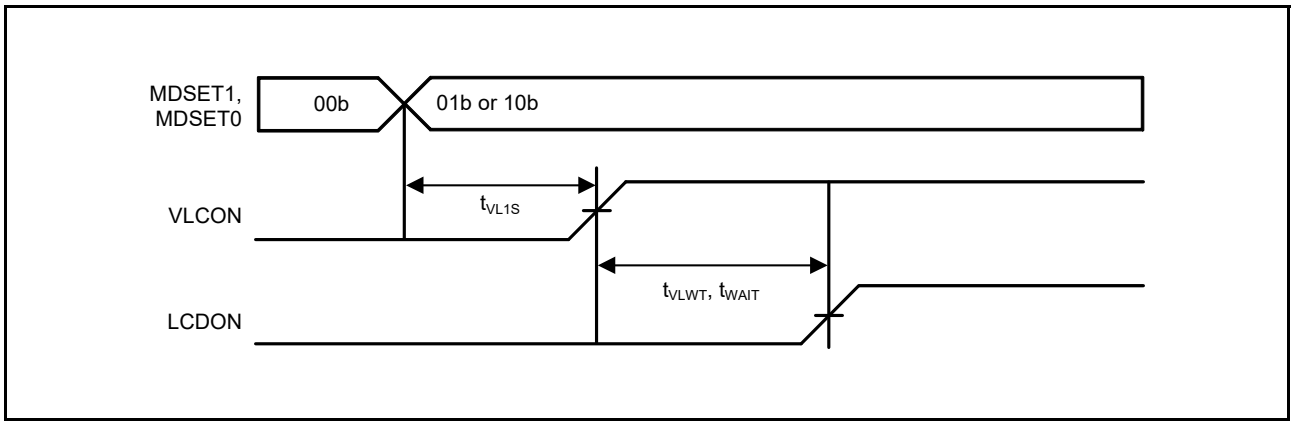


Figure 2.50 LCD Reference Voltage Setup Time, Voltage Boosting Wait Time, and Capacitor Split Wait Time

2.7 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 2.66 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 2.51, Figure 2.52
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	Figure 2.53 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 2.54 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.58	2.67		
		V_{det1_A}	2.37	2.48	2.57		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.86	1.96	2.06		
		V_{det1_D}	1.80	1.86	1.96		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48	V	Figure 2.55 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet0_n denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

Table 2.67 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after release from the power-on reset	At normal startup	t_{POR}	—	9.1	—	ms	Figure 2.52
	During fast startup time	t_{POR}	—	1.6	—		
Wait time after release from voltage monitoring 0 reset		t_{LVD0}	—	600	—	µs	Figure 2.53
Wait time after release from voltage monitoring 1 reset		t_{LVD1}	—	150	—	µs	Figure 2.54
Wait time after release from voltage monitoring 2 reset		t_{LVD2}	—	150	—	µs	Figure 2.55
Response delay time		t_{det}	—	—	350	µs	Figure 2.51
Minimum VCC down time*1		t_{VOFF}	350	—	—	µs	Figure 2.51, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 2.52, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 2.54, Figure 2.55
Hysteresis width (power-on rest (POR))		V_{PORH}	—	110	—	mV	
Hysteresis width (voltage detection circuit: LVD0, LVD1 and LVD2)		V_{LVH}	—	70	—	mV	When Vdet1_0 to Vdet1_4 is selected
			—	60	—		When Vdet1_5 to Vdet1_9 is selected
			—	50	—		When Vdet1_A or Vdet1_B is selected
			—	40	—		When Vdet1_C or Vdet1_D is selected
			—	60	—		When LVD0 or LVD2 is selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

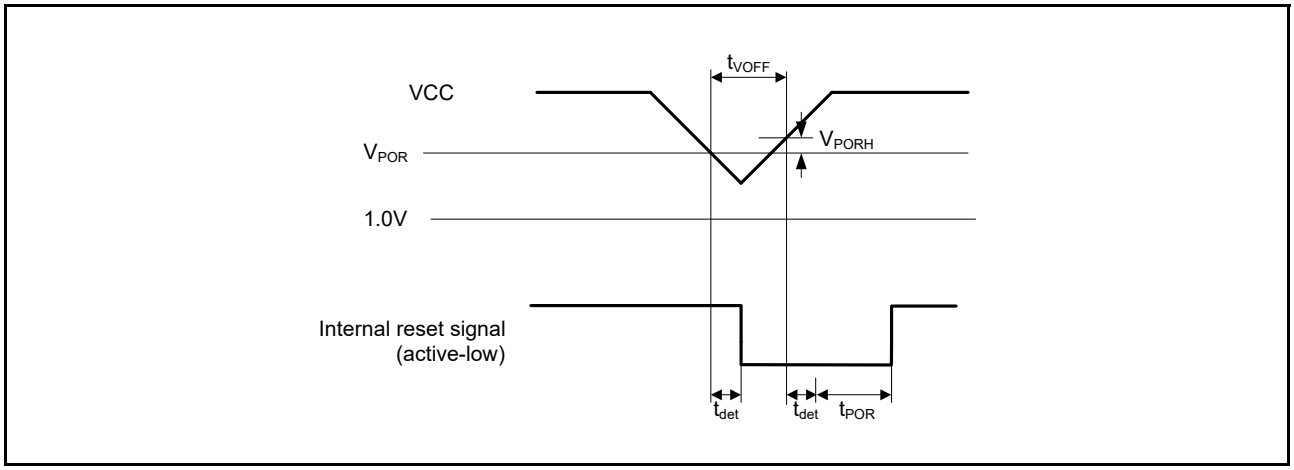
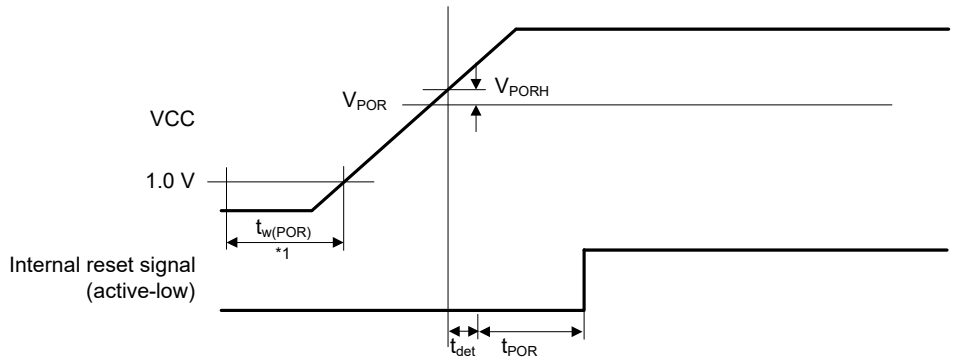


Figure 2.51 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When turning the VCC on, maintain a voltage below 1.0V for at least 1.0ms.

Figure 2.52 Power-On Reset Timing

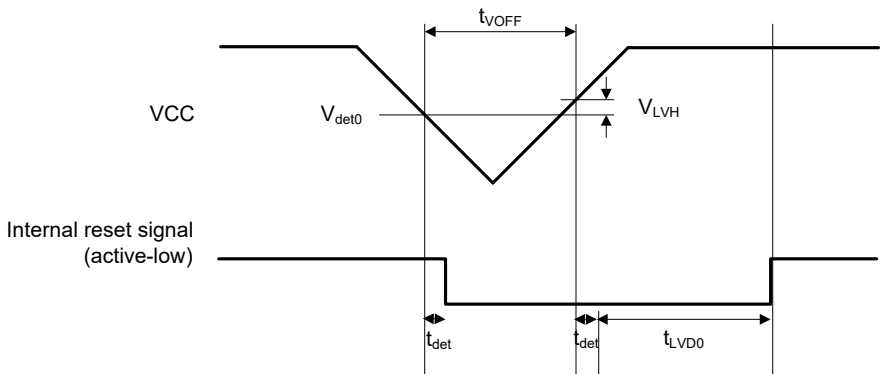


Figure 2.53 Voltage Detection Circuit Timing (Vdet0)

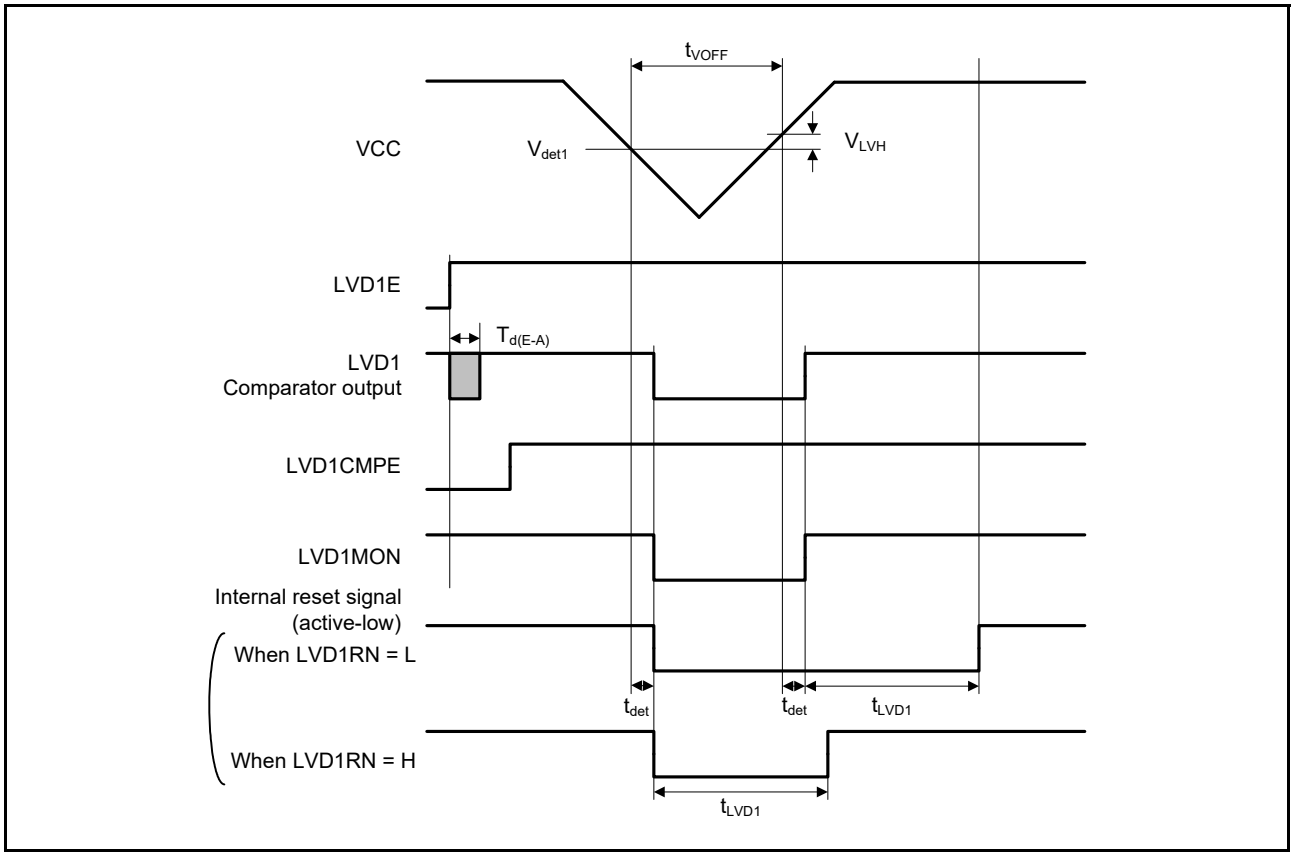


Figure 2.54 Voltage Detection Circuit Timing (V_{det1})

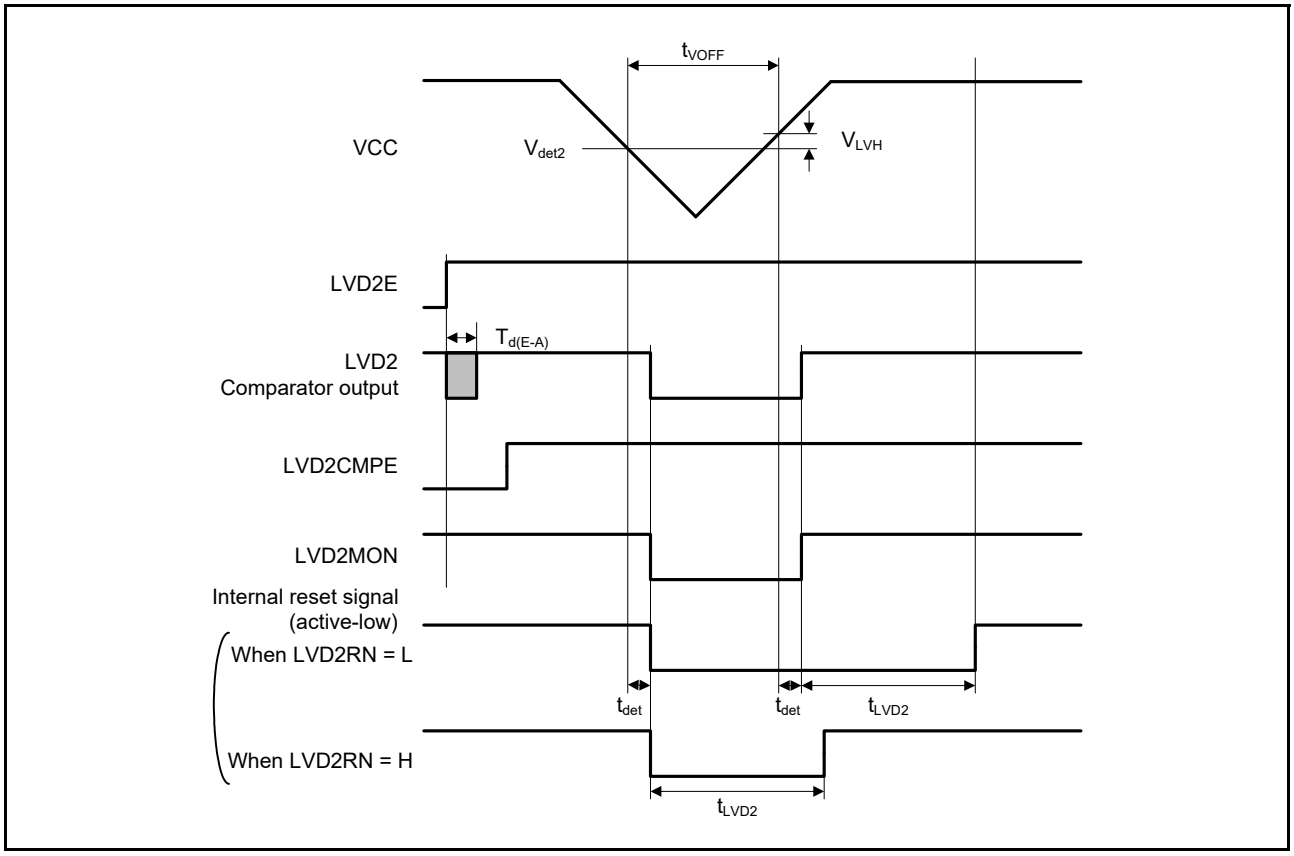


Figure 2.55 Voltage Detection Circuit Timing (V_{det2})

2.8 Oscillation Stop Detection Timing

Table 2.68 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.56

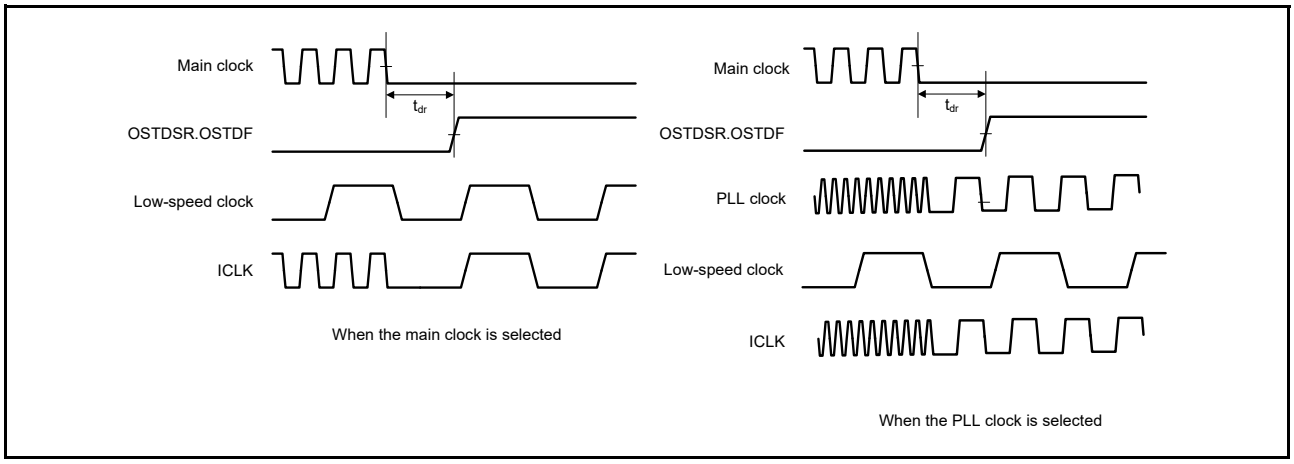


Figure 2.56 Oscillation Stop Detection Timing

2.9 ROM (Code Flash Memory) Characteristics

Table 2.69 ROM (Code Flash Memory) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{PEC}	1000	—	—	Times	
Data retention	After 1000 times of erase	t_{DRP}	20*2, *3	—	—	Year	T_a = 85°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 256 times for different addresses in a 1-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.70 ROM (Code Flash Memory) Characteristics (2) (High-Speed Operating Mode)

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	8-byte	t_{P8}	—	112.0	967.0	—	52.3	490.5	µs
Erase time	2-Kbyte	t_{E2K}	—	8.7	278.1	—	5.5	214.6	ms
	256-Kbyte (when block erase command is used)	t_{E256K}	—	469.1	9813.6	—	41.2	1049.2	ms
	256-Kbyte (when all-block erase command is used)	t_{EA256K}	—	463.9	9609.0	—	36.0	839.5	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	µs
	2-Kbyte	t_{BC2K}	—	—	1840.0	—	—	135.7	µs
Erase operation forced stop time		t_{SED}	—	—	18.0	—	—	10.7	µs
Start-up area switching time		t_{SAS}	—	12.3	566.5	—	6.2	433.5	ms
Access window setting time		t_{AWS}	—	12.3	566.5	—	6.2	433.5	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

Table 2.71 ROM (Code Flash Memory) Characteristics (3) (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	8-byte	t_{P8}	—	152.0	1367.0	—	97.9	936.0	µs
Erase time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	220.8	ms
	256-Kbyte (when block erase command is used)	t_{E256K}	—	469.2	9816.9	—	100.5	2260.1	ms
	256-Kbyte (when all-block erase command is used)	t_{EA256K}	—	464.0	9610.7	—	95.3	2053.7	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.9	µs
	2-Kbyte	t_{BC2K}	—	—	1870.0	—	—	401.5	µs
Erase operation forced stop time		t_{SED}	—	—	28.0	—	—	21.3	µs
Start-up area switching time		t_{SAS}	—	13.0	573.3	—	7.7	450.1	ms
Access window setting time		t_{AWS}	—	13.0	573.3	—	7.7	450.1	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.

2.10 E2 DataFlash (Data Flash Memory) Characteristics

Table 2.72 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{DPEC}	100000	1000000	—	Times	
Data retention	After 10000 times of erase	t_{DDRP}	20*2, *3	—	—	Year	T_a = 85°C
	After 100000 times of erase		5*2, *3	—	—	Year	
	After 1000000 times of erase		—	1*2, *3	—	Year	T_a = 25°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycle is n, each block can be erased n times. For instance, when 1-byte program is performed 1000 times for different addresses in a 1-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when the flash programmer is used and the self-programming library is provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 2.73 E2 DataFlash Characteristics (2) (High-Speed Operating Mode)

Conditions: 2.7 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	1 byte	t_{DP1}	—	95.0	797.0	—	40.8	375.5	µs
Erase time	1 Kbyte	t_{DE1K}	—	19.5	498.5	—	6.2	229.4	ms
	8 Kbyte	t_{DE8K}	—	119.8	2555.7	—	12.9	367.2	ms
Blank check time	1 byte	t_{DBC1}	—	—	55.0	—	—	16.1	µs
	1 Kbyte	t_{DBC1K}	—	—	7216.0	—	—	495.7	µs
Erase operation forced stop time		t_{DSED}	—	—	16.0	—	—	10.7	µs
DataFlash STOP recovery time		t_{DSTOP}	5.0	—	—	5.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

Table 2.74 E2 DataFlash Characteristics (3) (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{DP1}	—	135.0	1197.0	—	86.5	822.5	µs
Erasure time	1 Kbyte	t_{DE1K}	—	19.6	500.1	—	8.0	264.1	ms
	8 Kbyte	t_{DE8K}	—	119.9	2557.4	—	27.7	668.2	ms
Blank check time	1 byte	t_{DBC1}	—	—	85.0	—	—	50.9	µs
	1 Kbyte	t_{DBC1K}	—	—	7246.0	—	—	1457.5	µs
Erase operation forced stop time		t_{DSED}	—	—	28.0	—	—	21.3	µs
DataFlash STOP recovery time		t_{DSTOP}	0.72	—	—	0.72	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

2.11 24-Bit Delta-Sigma A/D Converter Characteristics

Table 2.75 24-Bit Delta-Sigma A/D Converter Characteristics (1)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gain		Gain	1, 2, 4, 8, 16, 32, 64, 128			—	
Output data rate		f_{DR}	3.8	—	125000	SPS	f_{MOD} = 4 MHz
Resolution (no missing codes)		—	24	—	—	Bits	
RMS noise		V_N	—	Table 2.83, Table 2.85	—	—	Figure 2.57 to Figure 2.68
Normal mode rejection ratio	External clock, 50 Hz, 60 Hz	NMRR	120	—	—	dB	10 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
			75	—	—		54 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
	External clock, 50 Hz		120	—	—		50 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz
	External clock, 60 Hz		120	—	—		60 SPS, $Sinc^4$+$Sinc^4$ 60 ± 1 Hz
	Internal clock (HOCO), 50 Hz, 60 Hz		110	—	—		10 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
			70	—	—		54 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
	Internal clock (HOCO), 50 Hz		110	—	—		50 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz
	Internal clock (HOCO), 60 Hz		110	—	—		60 SPS, $Sinc^4$+$Sinc^4$ 60 ± 1 Hz
Disconnect detection assist currents		—		0.5, 2, 4, 20		µA	
Modulator clock		f_{MOD}	100	4000	4100	kHz	

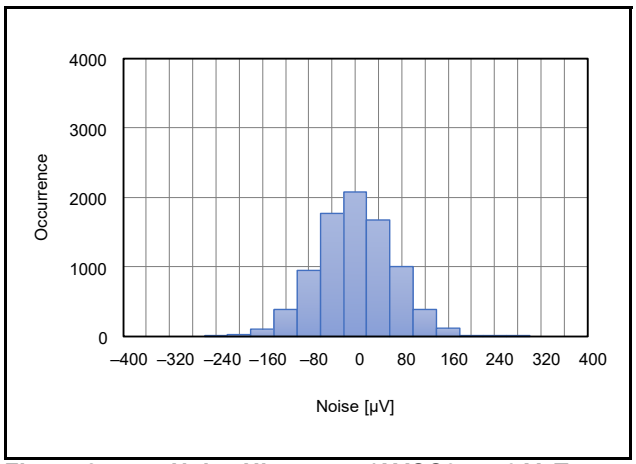


Figure 2.57 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA disabled, BUF disabled), f_{MOD} = 4 MHz, f_{DR} = 125k SPS, Sinc^5 Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

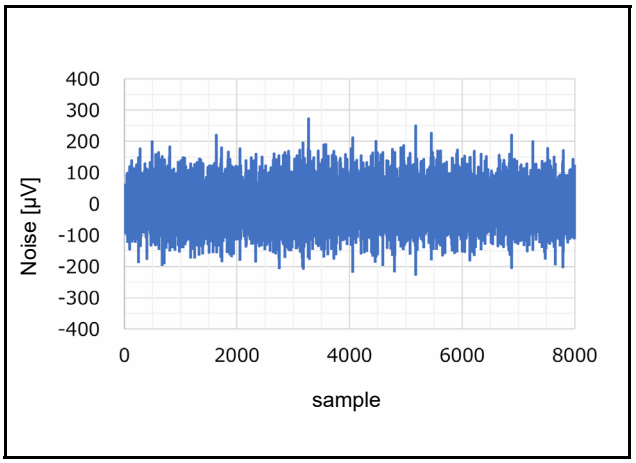


Figure 2.58 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA disabled, BUF disabled), f_{MOD} = 4 MHz, f_{DR} = 125k SPS, Sinc^5 Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

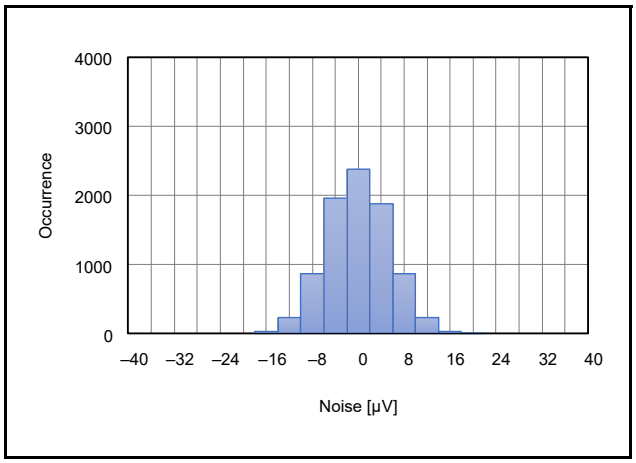


Figure 2.59 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Gain = 64, f_{MOD} = 4 MHz, f_{DR} = 125k SPS, Sinc^5 Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

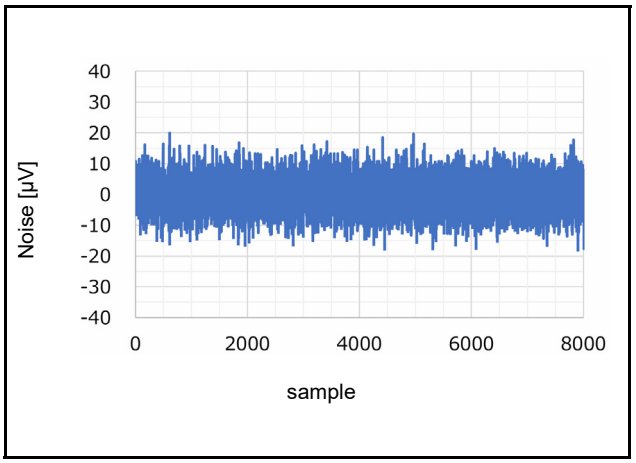


Figure 2.60 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Gain = 64, f_{MOD} = 4 MHz, f_{DR} = 125k SPS, Sinc^5 Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

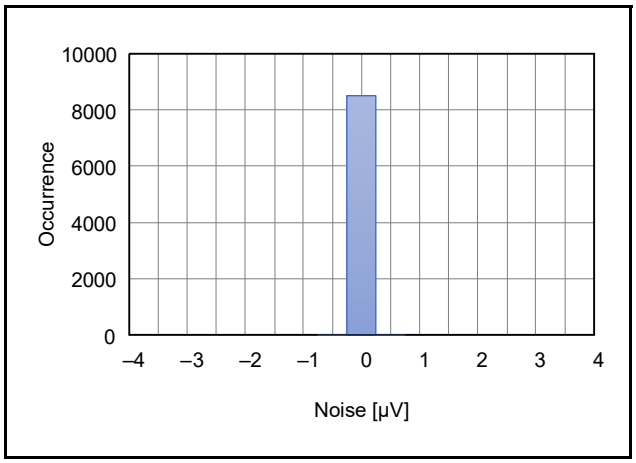


Figure 2.61 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA disabled, BUF disabled), f_{MOD} = 4 MHz, f_{DR} = 3.8 SPS, $Sinc^4$+$Sinc^4$ Filter. V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

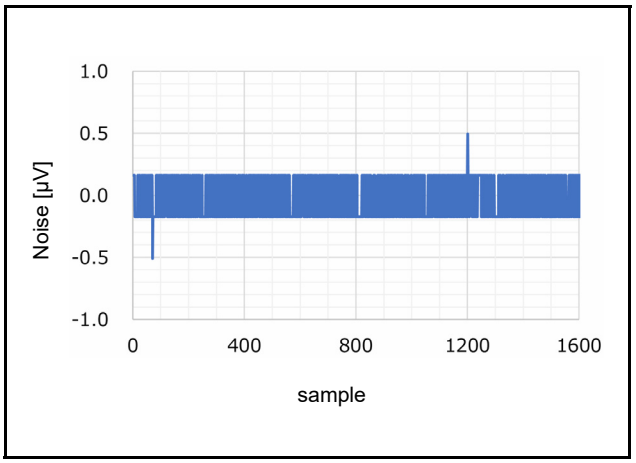


Figure 2.62 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA disabled, BUF disabled). f_{MOD} = 4 MHz, f_{DR} = 3.8 SPS, $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

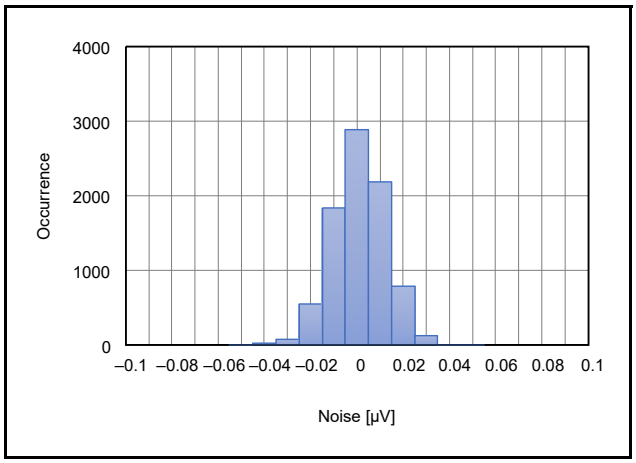


Figure 2.63 Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Gain = 64, f_{MOD} = 4 MHz, f_{DR} = 3.8 SPS, $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

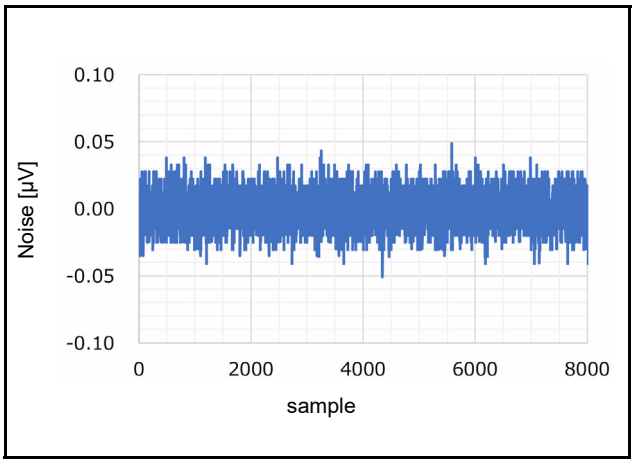


Figure 2.64 Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Gain = 64, f_{MOD} = 4 MHz, f_{DR} = 3.8 SPS, $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

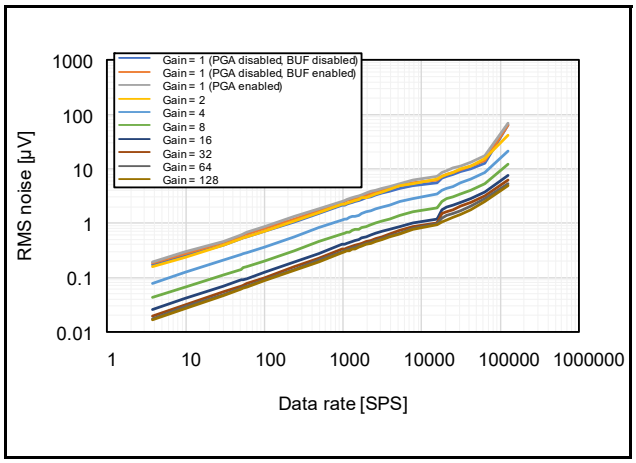


Figure 2.65 Data Rate Dependence of RMS Noise (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, $Sinc^5$ Filter or $Sinc^5$+$Sinc^1$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

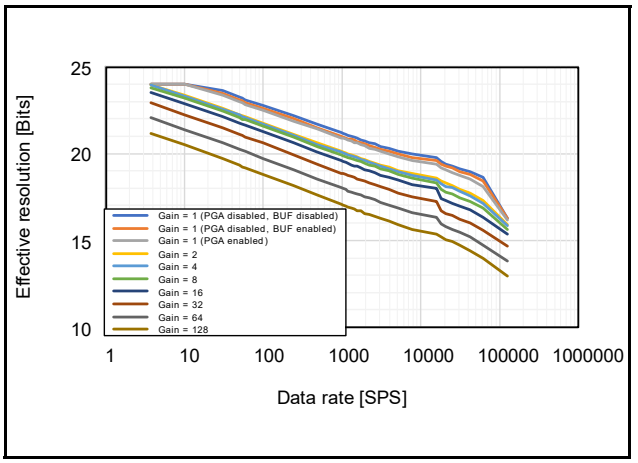


Figure 2.66 Data Rate Dependence of Effective Resolution (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, $Sinc^5$ Filter or $Sinc^5$+$Sinc^1$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

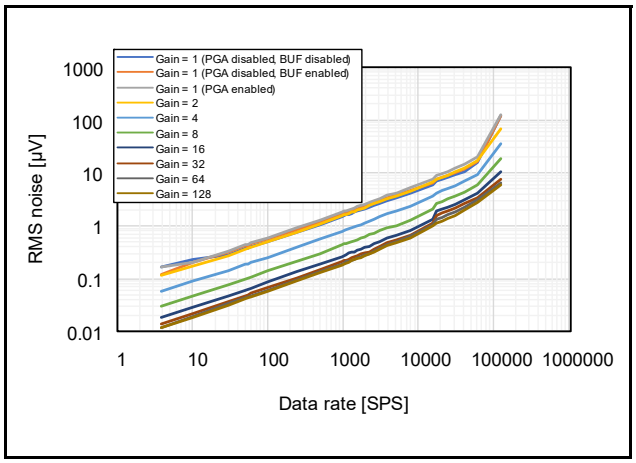


Figure 2.67 Data Rate Dependence of RMS Noise (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, $Sinc^4$ Filter or $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

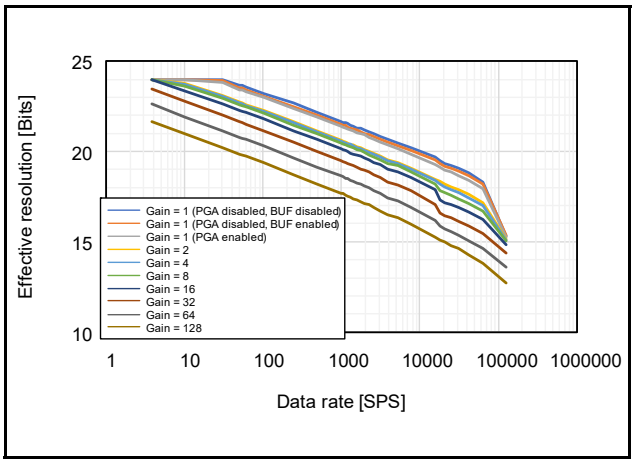


Figure 2.68 Data Rate Dependence of Effective Resolution (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, $Sinc^4$ Filter or $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)

Table 2.76 24-Bit Delta-Sigma A/D Converter Characteristics (2) (1/2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≥ 1024 ($Sinc^4$+$Sinc^4$), OSR ≥ 8192 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Integral non-linearity	Gain = 1 to 64 (PGA enabled)	INL	—	±10	±18	ppmFSR	Figure 2.69
	Gain = 128 (PGA enabled)		—	±12	±20		
	Gain = 1 (PGA disabled, BUF disabled)		—	±6	±8		
	Gain = 1 (PGA disabled, BUF enabled)		—	±5	±8		
Offset error	Before calibration	E_O	—	—	±70	µV	Figure 2.70 AVCC0 = 5.0 V, T_a = 25°C, Gain = 2
	After calibration		—	On the level of the noise	—		
Offset drift	Gain = 1, 2 (PGA enabled)	dE_O	—	70	335	nV/°C	Figure 2.70 V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 4 to 8		—	33	150		
	Gain = 16 to 32		—	7	36		
	Gain = 64 to 128		—	4	15		
	Gain = 1 (PGA disabled, BUF disabled)		—	25	130		
	Gain = 1 (PGA disabled, BUF enabled)		—	50	215		
Gain error	Gain = 1 to 64 (PGA enabled)	E_G	—	±0.030	±0.060	%	Figure 2.71 AVCC0 = 5.0 V, T_a = 25°C, V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 128		—	±0.030	±0.075		
	Gain = 1 (PGA disabled, BUF disabled)		—	±0.010	±0.022		
	Gain = 1 (PGA disabled, BUF enabled)		—	±0.010	±0.020		
	After calibration of gain errors		—	On the level of the noise	—		
Gain drift	Gain = 1 to 16 (PGA enabled)	dE_G	—	1.0	3.0	ppm/°C	Figure 2.71 V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 32 to 128 (PGA enabled)		—	1.2	4.0		
	Gain = 1 (PGA disabled, BUF disabled)		—	0.8	1.8		
	Gain = 1 (PGA disabled, BUF enabled)		—	0.8	2.2		
Power supply rejection ratio	Gain = 1 to 8 (PGA enabled)	PSRR	72	85	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 16 to 64		90	100	—		
	Gain = 128		—	105	—		
	Gain = 1 (PGA disabled, BUF disabled)		75	92	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		75	92	—		
Common mode rejection ratio	Gain = 1 to 8 (PGA enabled)	CMRR	88	95	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 16 to 32		105	115	—		
	Gain = 64 to 128		105	120	—		
	Gain = 1 (PGA disabled, BUF disabled)		84	95	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		84	95	—		

Table 2.76 24-Bit Delta-Sigma A/D Converter Characteristics (2) (2/2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≥ 1024 ($Sinc^4$+$Sinc^4$), OSR ≥ 8192 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Signal to noise ratio*1	Gain = 1 (PGA disabled, BUF disabled)	SNR	—	120	—	dB	$Sinc^4$+$Sinc^4$, f_{DR} = 977 SPS
	Gain = 64		—	100	—		
Total harmonic distortion	Gain = 1 (PGA disabled, BUF disabled)	THD	—	100	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 977 SPS
	Gain = 64		—	95	—		
Signal to noise and distortion	Gain = 1 (PGA disabled, BUF disabled)	SINAD	—	100	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 977 SPS
	Gain = 64		—	95	—		
Spurious free dynamic range	Gain = 1 (PGA disabled, BUF disabled)	SFDR	—	100	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 977 SPS
	Gain = 64		—	100	—		

Note 1. Ratio of Noise at 0 input and signal at FullScale input.

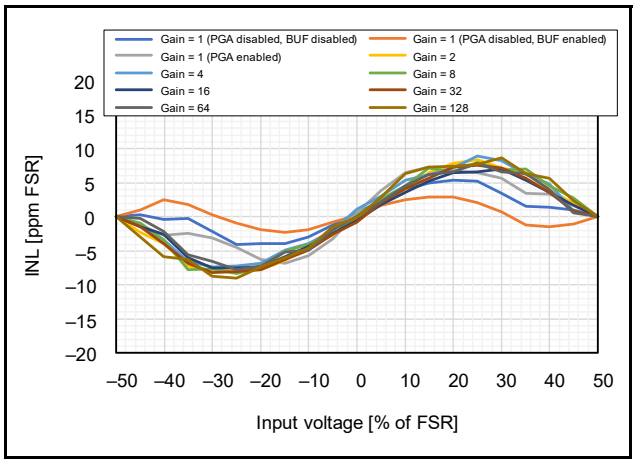


Figure 2.69 Input Voltage Dependence of Integral Non-Linearity (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, Total oversampling ratio = 4096, V_{REF} = 2.5 V)

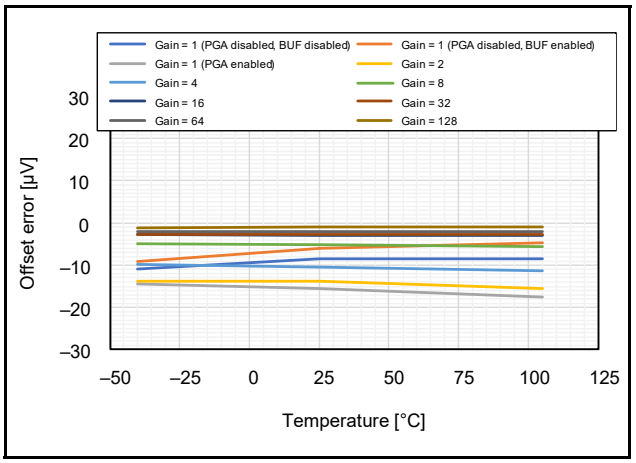


Figure 2.70 Temperature Dependence of Offset Error (AVCC0 = 5.0 V, V_{ID} = 0 V, f_{MOD} = 4 MHz, Total oversampling ratio = 4096, V_{REF} = 2.5 V)

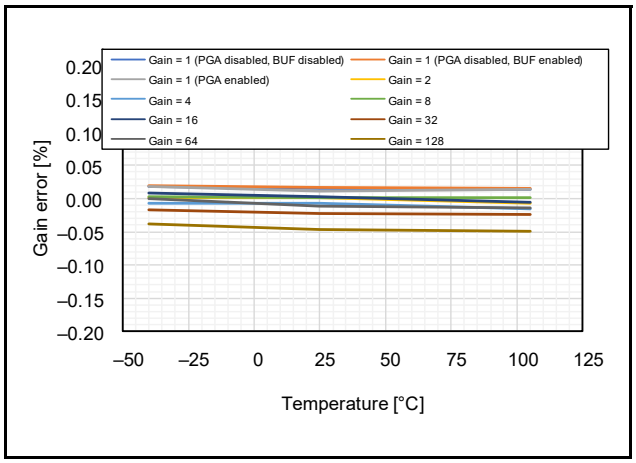


Figure 2.71 Temperature Dependence of Gain Error (AVCC0 = 5.0 V, f_{MOD} = 4 MHz, Total oversampling ratio = 4096, V_{REF} = 2.5 V)

Table 2.77 24-Bit Delta-Sigma A/D Converter Characteristics (3) (1/2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, 256 ≤ OSR ≤ 768 ($Sinc^4$+$Sinc^4$), 256 ≤ OSR ≤ 7936 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Integral non-linearity	Gain = 1 to 64 (PGA enabled)	INL	—	±15	±25	ppmFSR	
	Gain = 128 (PGA enabled)		—	±15	±30		
	Gain = 1 (PGA disabled, BUF disabled)		—	±6	±8		
	Gain = 1 (PGA disabled, BUF enabled)		—	±5	±8		
Offset error	Before calibration	E_O	—	—	±90	µV	AVCC0 = 5.0 V, T_a = 25°C, Gain = 2
	After calibration		—	On the level of the noise	—		
Offset drift	Gain = 1, 2 (PGA enabled)	dE_O	—	95	385	nV/°C	V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 4, 8		—	40	170		
	Gain = 16, 32		—	9	40		
	Gain = 64, 128		—	4	15		
	Gain = 1 (PGA disabled, BUF disabled)		—	37	165		
	Gain = 1 (PGA disabled, BUF enabled)		—	37	205		
Gain error	Gain = 1 to 64 (PGA enabled)	E_G	—	±0.030	±0.060	%	AVCC0 = 5.0 V, T_a = 25°C, V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 128		—	±0.040	±0.080		
	Gain = 1 (PGA disabled, BUF disabled)		—	±0.010	±0.022		
	Gain = 1 (PGA disabled, BUF enabled)		—	±0.010	±0.020		
	After calibration of gain errors		—	On the level of the noise	—		
Gain drift	Gain = 1 to 16 (PGA enabled)	dE_G	—	1.0	3.0	ppm/°C	V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 32 to 128 (PGA enabled)		—	1.2	4.0		
	Gain = 1 (PGA disabled, BUF disabled)		—	0.8	1.8		
	Gain = 1 (PGA disabled, BUF enabled)		—	0.8	2.2		
Power supply rejection ratio	Gain = 1 to 8 (PGA enabled)	PSRR	72	82	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 16 to 64		90	100	—		
	Gain = 128		—	100	—		
	Gain = 1 (PGA disabled, BUF disabled)		75	92	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		75	92	—		
Common mode rejection ratio	Gain = 1 to 8 (PGA enabled)	CMRR	88	95	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 16 to 32		105	115	—		
	Gain = 64 to 128		105	120	—		
	Gain = 1 (PGA disabled, BUF disabled)		84	95	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		84	95	—		

Table 2.77 24-Bit Delta-Sigma A/D Converter Characteristics (3) (2/2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, 256 ≤ OSR ≤ 768 ($Sinc^4$+$Sinc^4$), 256 ≤ OSR ≤ 7936 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Signal to noise ratio*1	Gain = 1 (PGA disabled, BUF disabled)	SNR	—	110	—	dB	$Sinc^4$+$Sinc^4$, f_{DR} = 15.6k SPS
	Gain = 64		—	85	—		
Total harmonic distortion	Gain = 1 (PGA disabled, BUF disabled)	THD	—	100	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 15.6k SPS
	Gain = 64		—	95	—		
Signal to noise and distortion	Gain = 1 (PGA disabled, BUF disabled)	SINAD	—	95	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 15.6k SPS
	Gain = 64		—	85	—		
Spurious free dynamic range	Gain = 1 (PGA disabled, BUF disabled)	SFDR	—	100	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 15.6k SPS
	Gain = 64		—	95	—		

Note 1. Ratio of Noise at 0 input and signal at FullScale input.

Table 2.78 24-Bit Delta-Sigma A/D Converter Characteristics (4) (1/2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≤ 224 ($Sinc^4$+$Sinc^4$, $Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Integral non-linearity	Gain = 1 to 64 (PGA enabled)	INL	—	±10	±18	ppmFSR	
	Gain = 128 (PGA enabled)		—	±10	±20		
	Gain = 1 (PGA disabled, BUF disabled)		—	±6	±8		
	Gain = 1 (PGA disabled, BUF enabled)		—	±5	±8		
Offset error	Before calibration	E_O	—	—	±110	µV	AVCC0 = 5.0 V, T_a = 25°C, Gain = 2
	After calibration		—	On the level of the noise	—		
Offset drift	Gain = 1, 2 (PGA enabled)	dE_O	—	80	415	nV/°C	V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 4, 8		—	40	196		
	Gain = 16, 32		—	12	48		
	Gain = 64, 128		—	6	18		
	Gain = 1 (PGA disabled, BUF disabled)		—	80	305		
	Gain = 1 (PGA disabled, BUF enabled)		—	90	340		
Gain error	Gain = 1 to 64 (PGA enabled)	E_G	—	±0.030	±0.060	%	AVCC0 = 5.0 V, T_a = 25°C, V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 128		—	±0.030	±0.070		
	Gain = 1 (PGA disabled, BUF disabled)		—	±0.010	±0.022		
	Gain = 1 (PGA disabled, BUF enabled)		—	±0.010	±0.020		
	After calibration of gain errors		—	On the level of the noise	—		
Gain drift	Gain = 1 to 16 (PGA enabled)	dE_G	—	1.0	3.0	ppm/°C	V_{IC} = 2.5 V, V (VR0P) = 2.5 V, V (VR0N) = 0 V
	Gain = 32 to 128 (PGA enabled)		—	1.2	4.0		
	Gain = 1 (PGA disabled, BUF disabled)		—	0.8	1.8		
	Gain = 1 (PGA disabled, BUF enabled)		—	0.8	2.2		
Power supply rejection ratio	Gain = 1 to 8 (PGA enabled)	PSRR	72	82	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 16 to 64		90	100	—		
	Gain = 128		—	100	—		
	Gain = 1 (PGA disabled, BUF disabled)		72	92	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		72	90	—		
Common mode rejection ratio	Gain = 1 to 8 (PGA enabled)	CMRR	88	95	—	dB	V_{ID} = 1 V/Gain (DC)
	Gain = 16 to 32		105	115	—		
	Gain = 64 to 128		110	120	—		
	Gain = 1 (PGA disabled, BUF disabled)		84	95	—		V_{ID} = 1 V (DC)
	Gain = 1 (PGA disabled, BUF enabled)		84	95	—		

Table 2.78 24-Bit Delta-Sigma A/D Converter Characteristics (4) (2/2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≤ 224 ($Sinc^4$+$Sinc^4$, $Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Signal to noise ratio*1	Gain = 1 (PGA disabled, BUF disabled)	SNR	—	105	—	dB	$Sinc^4$+$Sinc^4$, f_{DR} = 17.9 SPS
	Gain = 64		—	85	—		
Total harmonic distortion	Gain = 1 (PGA disabled, BUF disabled)	THD	—	100	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 17.9 SPS
	Gain = 64		—	95	—		
Signal to noise and distortion	Gain = 1 (PGA disabled, BUF disabled)	SINAD	—	95	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 17.9 SPS
	Gain = 64		—	80	—		
Spurious free dynamic range	Gain = 1 (PGA disabled, BUF disabled)	SFDR	—	100	—	dB	fin = 50 Hz, V_{ID} = -0.5 dBFS, $Sinc^4$+$Sinc^4$, f_{DR} = 17.9 SPS
	Gain = 64		—	95	—		

Note 1. Ratio of Noise at 0 input and signal at FullScale input.

Table 2.79 24-Bit Delta-Sigma A/D Converter Analog Input Characteristics (1)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Differential input voltage range	Gain = 1 (PGA disabled)	V_{ID}	$-V_{REF}$	—	$+V_{REF}$	V	V_{REF} = $V_{(VR0P)}$ – $V_{(VR0N)}$
	Gain = 1 (PGA enabled)		Whichever is greater of the values of $-V_{REF}$ and –(AVCC0 – AVSS0 – 0.5V)	—	Whichever is smaller of the values of $+V_{REF}$ and +(AVCC0 – AVSS0 – 0.5V)		
	Gain ≥ 2		$-V_{REF}$/ Gain	—	$+V_{REF}$ / Gain		
Absolute input voltage range	Gain = 1 (PGA disabled, BUF disabled)	V_I	AVSS0 + 0.2	—	AVCC0 – 0.2	V	Specified Performance
			AVSS0 – 0.05	—	AVCC0 + 0.05		Functional
	Gain = 1 (PGA disabled, BUF enabled)		AVSS0 + 0.2	—	AVCC0 – 0.2		
	Gain = 1 to 128 (PGA enabled)		AVSS0 + 0.2	—	AVCC0 – 0.2		Specified Performance
			AVSS0 – 0.05	—	AVCC0 + 0.05		Functional

Table 2.80 24-Bit Delta-Sigma A/D Converter Analog Input Characteristics (2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≥ 1024 ($Sinc^4$+$Sinc^4$), OSR ≥ 8192 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input bias current	Gain = 1 to 128 (PGA enabled)	I_{IB}	—	±8	±35	nA	Figure 2.72 T_a = 25°C, V_{ID} = 0 V
	Gain = 1 (PGA disabled, BUF enabled)		—	±9	±40		
	Gain = 1 (PGA disabled, BUF disabled)		—	±3	±15		
Input offset current	Gain = 1 to 128 (PGA enabled)	I_{IO}	—	±30	±150	nA	Figure 2.73 T_a = 25°C, V_{ID} = 2.5 V/ Gain
	Gain = 1 (PGA disabled, BUF enabled)		—	±20	±80		
	Gain = 1 (PGA disabled, BUF disabled)		—	55	75	µA/V	
Input bias current drift	Gain = 1 to 16 (PGA enabled)	dI_{IB}	—	250	800	pA/°C	Figure 2.72
	Gain = 32 to 128		—	250	850		
	Gain = 1 (PGA disabled, BUF enabled)		—	200	600		
	Gain = 1 (PGA disabled, BUF disabled)		—	200	700		
Input offset current drift	Gain = 1 (PGA enabled)	dI_{IO}	—	1000	3500	pA/°C	Figure 2.73
	Gain = 2 to 16 (PGA enabled)		—	600	2500		
	Gain = 32 to 128 (PGA enabled)		—	300	1500		
	Gain = 1 (PGA disabled, BUF enabled)		—	750	3000		
	Gain = 1 (PGA disabled, BUF disabled)		—	1500	3000	pA/V/°C	

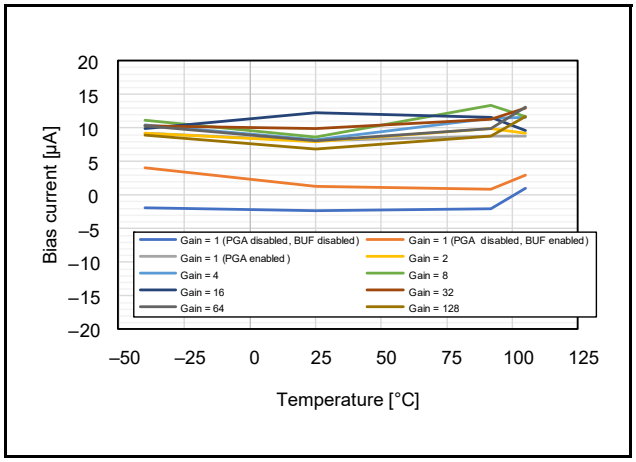


Figure 2.72 Temperature Dependence of Analog Input Bias Current (AVCC0 = 5.0 V, f_{MOD} = 4 MHz, Total oversampling ratio = 4096)

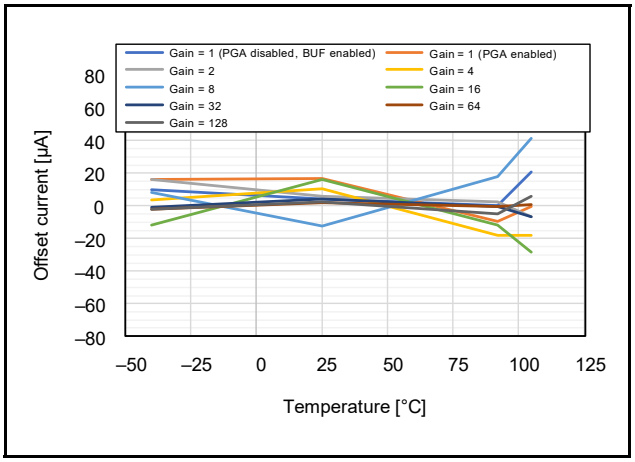


Figure 2.73 Temperature Dependence of Analog Input Offset Current (AVCC0 = 5.0 V, f_{MOD} = 4 MHz, Total oversampling ratio = 4096)

Table 2.81 24-Bit Delta-Sigma A/D Converter Analog Input Characteristics (3)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, 256 ≤ OSR ≤ 768 ($Sinc^4$+$Sinc^4$), 256 ≤ OSR ≤ 7936 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input bias current	Gain = 1 to 128 (PGA enabled)	I_{IB}	—	±8	±35	nA	T_a = 25°C, V_{ID} = 0 V
	Gain = 1 (PGA disabled, BUF enabled)		—	±9	±40		
	Gain = 1 (PGA disabled, BUF disabled)		—	±3	±15		
Input offset current	Gain = 1 to 128 (PGA enabled)	I_{IO}	—	±30	±150	nA	T_a = 25°C, V_{ID} = 2.5 V/ Gain
	Gain = 1 (PGA disabled, BUF enabled)		—	±20	±80		
	Gain = 1 (PGA disabled, BUF disabled)		—	55	80	µA/V	
Input bias current drift	Gain = 1 to 16 (PGA enabled)	dI_{IB}	—	250	800	pA/°C	
	Gain = 32 to 128		—	250	850		
	Gain = 1 (PGA disabled, BUF enabled)		—	200	600		
	Gain = 1 (PGA disabled, BUF disabled)		—	200	700		
Input offset current drift	Gain = 1 (PGA enabled)	dI_{IO}	—	1000	3500	pA/°C	
	Gain = 2 to 16 (PGA enabled)		—	600	2500		
	Gain = 32 to 128 (PGA enabled)		—	300	1500		
	Gain = 1 (PGA disabled, BUF enabled)		—	750	3000		
	Gain = 1 (PGA disabled, BUF disabled)		—	1500	3000	pA/V/°C	

Table 2.82 24-Bit Delta-Sigma A/D Converter Analog Input Characteristics (4)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≤ 224 ($Sinc^4$+$Sinc^4$, $Sinc^5$+$Sinc^1$), T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input bias current	Gain = 1 to 128 (PGA enabled)	I_{IB}	—	±25	±65	nA	T_a = 25°C, V_{ID} = 0 V
	Gain = 1 (PGA disabled, BUF enabled)		—	±8.5	±40		
	Gain = 1 (PGA disabled, BUF disabled)		—	±4	±15		
Input offset current	Gain = 1 to 128 (PGA enabled)	I_{IO}	—	±75	±350	nA	T_a = 25°C, V_{ID} = 2.5 V/ Gain
	Gain = 1 (PGA disabled, BUF enabled)		—	±35	±150		
	Gain = 1 (PGA disabled, BUF disabled)		—	55	75	µA/V	
Input bias current drift	Gain = 1 to 16 (PGA enabled)	dI_{IB}	—	300	1500	pA/°C	
	Gain = 32 to 128		—	250	950		
	Gain = 1 (PGA disabled, BUF enabled)		—	150	600		
	Gain = 1 (PGA disabled, BUF disabled)		—	200	650		
Input offset current drift	Gain = 1 (PGA enabled)	dI_{IO}	—	2500	8000	pA/°C	
	Gain = 2 to 16 (PGA enabled)		—	2000	6500		
	Gain = 32 to 128 (PGA enabled)		—	500	2000		
	Gain = 1 (PGA disabled, BUF enabled)		—	600	3000		
	Gain = 1 PGA disabled, BUF disabled)		—	1500	3000	pA/V/°C	

Table 2.83 Typical Noise Characteristics

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^4$+$Sinc^4$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
3.814	1048576	0.160	0.168	0.179	0.141	0.061	0.031	0.019	0.014	0.012	0.011
		(0.50)	(1.00)	(1.00)	(0.92)	(0.42)	(0.23)	(0.14)	(0.10)	(0.09)	(0.09)
10.003	399872	0.192	0.252	0.236	0.177	0.094	0.047	0.030	0.022	0.019	0.018
		(1.24)	(1.48)	(1.48)	(1.24)	(0.62)	(0.31)	(0.20)	(0.16)	(0.14)	(0.14)
50.1	79872	0.359	0.406	0.431	0.352	0.178	0.096	0.059	0.046	0.042	0.041
		(2.43)	(2.73)	(3.03)	(2.58)	(1.29)	(0.72)	(0.42)	(0.34)	(0.30)	(0.31)
54	73728	0.346	0.390	0.421	0.352	0.182	0.098	0.062	0.048	0.044	0.042
		(2.51)	(2.72)	(3.34)	(2.51)	(1.41)	(0.71)	(0.46)	(0.35)	(0.33)	(0.32)
60	66560	0.387	0.427	0.463	0.374	0.193	0.106	0.065	0.051	0.046	0.044
		(2.52)	(3.15)	(3.15)	(2.67)	(1.34)	(0.75)	(0.47)	(0.37)	(0.34)	(0.33)
100	39936	0.470	0.523	0.572	0.469	0.242	0.133	0.083	0.065	0.059	0.057
		(3.34)	(3.64)	(4.55)	(3.49)	(1.74)	(0.95)	(0.66)	(0.47)	(0.46)	(0.46)
977	4096	1.407	1.562	1.691	1.442	0.748	0.408	0.256	0.207	0.190	0.181
		(10.9)	(12.9)	(12.4)	(11.1)	(5.90)	(3.10)	(1.98)	(1.54)	(1.40)	(1.43)
1953	2048	1.959	2.217	2.406	2.021	1.065	0.591	0.374	0.298	0.272	0.265
		(15.9)	(16.7)	(17.2)	(17.0)	(7.99)	(4.56)	(3.00)	(2.12)	(2.09)	(2.06)
3906	1024	2.760	3.114	3.519	3.057	1.592	0.897	0.561	0.462	0.427	0.414
		(21.4)	(22.9)	(27.1)	(22.1)	(11.6)	(6.78)	(4.19)	(3.92)	(3.18)	(3.21)
15625	256	5.579	6.185	7.339	6.490	3.422	1.930	1.250	1.070	1.001	0.971
		(43.7)	(45.2)	(58.1)	(50.6)	(25.5)	(14.1)	(9.74)	(7.57)	(7.56)	(7.80)
17857	224	6.393	7.098	8.323	7.108	3.909	2.516	1.835	1.507	1.286	1.053
		(46.8)	(52.2)	(63.1)	(52.0)	(30.1)	(19.5)	(13.9)	(11.7)	(9.67)	(7.86)
31250	128	8.509	9.342	11.25	9.657	5.429	3.435	2.502	2.084	1.778	1.511
		(63.4)	(71.1)	(81.2)	(70.7)	(40.3)	(25.4)	(20.1)	(16.7)	(13.8)	(11.4)
41667	96	9.997	10.97	13.29	11.71	6.542	4.074	2.973	2.471	2.151	1.819
		(80.7)	(81.7)	(98.6)	(85.9)	(49.6)	(30.6)	(23.3)	(18.7)	(16.2)	(14.0)
62500	64	14.59	15.73	19.50	16.09	8.891	5.504	3.850	3.277	2.968	2.613
		(114)	(128)	(143)	(129)	(64.6)	(46.8)	(29.5)	(24.5)	(23.7)	(21.2)
125000	32	122.6	122.1	122.1	65.91	34.11	17.67	10.10	7.107	5.844	5.301
		(851)	(904)	(909)	(489)	(264)	(126)	(72.7)	(53.2)	(44.9)	(40.1)

Note: "Bypass" indicates the state where both PGA and BUF are disabled, "BUF" indicates the state where PGA is disabled and BUF is enabled, and "PGA" indicates the state where PGA is enabled.

Note: The upper rows indicate RMS noise (μV_{RMS}) and the lower rows (in parentheses) indicate peak-to-peak noise (μV_{PP}).

Table 2.84 Effective Resolution

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^4$+$Sinc^4$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
3.814	1048576	24.0	24.0	24.0	24.0	24.0	24.0	23.9	23.4	22.6	21.7
		(23.2)	(22.2)	(22.2)	(21.4)	(21.5)	(21.4)	(21.1)	(20.5)	(19.7)	(18.8)
10.003	399872	24.0	24.0	24.0	23.8	23.7	23.6	23.3	22.8	22.0	21.0
		(21.9)	(21.7)	(21.7)	(20.9)	(20.9)	(20.9)	(20.6)	(19.9)	(19.1)	(18.1)
50.1	79872	23.7	23.6	23.5	22.8	22.7	22.6	22.3	21.7	20.8	19.9
		(21.0)	(20.8)	(20.7)	(19.9)	(19.9)	(19.7)	(19.5)	(18.8)	(18.0)	(16.9)
54	73728	23.8	23.6	23.5	22.8	22.7	22.6	22.3	21.6	20.8	19.8
		(20.9)	(20.8)	(20.5)	(19.9)	(19.8)	(19.8)	(19.4)	(18.8)	(17.9)	(16.9)
60	66560	23.6	23.5	23.4	22.7	22.6	22.5	22.2	21.5	20.7	19.8
		(20.9)	(20.6)	(20.6)	(19.8)	(19.8)	(19.7)	(19.3)	(18.7)	(17.8)	(16.9)
100	39936	23.3	23.2	23.1	22.3	22.3	22.2	21.8	21.2	20.3	19.4
		(20.5)	(20.4)	(20.1)	(19.5)	(19.5)	(19.3)	(18.8)	(18.3)	(17.4)	(16.4)
977	4096	21.8	21.6	21.5	20.7	20.7	20.5	20.2	19.5	18.7	17.7
		(18.8)	(18.6)	(18.6)	(17.8)	(17.7)	(17.6)	(17.3)	(16.6)	(15.8)	(14.7)
1953	2048	21.3	21.1	21.0	20.2	20.2	20.0	19.7	19.0	18.1	17.2
		(18.3)	(18.2)	(18.1)	(17.2)	(17.3)	(17.1)	(16.7)	(16.2)	(15.2)	(14.2)
3906	1024	20.8	20.6	20.4	19.6	19.6	19.4	19.1	18.4	17.5	16.5
		(17.8)	(17.7)	(17.5)	(16.8)	(16.7)	(16.5)	(16.2)	(15.3)	(14.6)	(13.6)
15625	256	19.8	19.6	19.4	18.6	18.5	18.3	17.9	17.2	16.3	15.3
		(16.8)	(16.8)	(16.4)	(15.6)	(15.6)	(15.4)	(15.0)	(14.3)	(13.3)	(12.3)
17857	224	19.6	19.4	19.2	18.4	18.3	17.9	17.4	16.7	15.9	15.2
		(16.7)	(16.5)	(16.3)	(15.6)	(15.3)	(15.0)	(14.5)	(13.7)	(13.0)	(12.3)
31250	128	19.2	19.0	18.8	18.0	17.8	17.5	16.9	16.2	15.4	14.7
		(16.3)	(16.1)	(15.9)	(15.1)	(14.9)	(14.6)	(13.9)	(13.2)	(12.5)	(11.7)
41667	96	18.9	18.8	18.5	17.7	17.5	17.2	16.7	15.9	15.1	14.4
		(15.9)	(15.9)	(15.6)	(14.8)	(14.6)	(14.3)	(13.7)	(13.0)	(12.2)	(11.4)
62500	64	18.4	18.3	18.0	17.2	17.1	16.8	16.3	15.5	14.7	13.9
		(15.4)	(15.3)	(15.1)	(14.2)	(14.2)	(13.7)	(13.4)	(12.6)	(11.7)	(10.8)
125000	32	15.3	15.3	15.3	15.2	15.2	15.1	14.9	14.4	13.7	12.8
		(12.5)	(12.4)	(12.4)	(12.3)	(12.2)	(12.3)	(12.1)	(11.5)	(10.8)	(9.9)

Effective resolution = $\log_2$(full-scale voltage/RMS noise)

Noise-free resolution = $\log_2$(full-scale voltage/peak-to-peak noise)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate effective resolution (bits) and the lower rows (in parentheses) indicate noise-free resolution (bits).

Table 2.85 Typical Noise Characteristics

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^5$+$Sinc^1$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
3.814	1048576	0.165	0.194	0.203	0.174	0.093	0.042	0.027	0.020	0.017	0.017
		(1.00)	(1.34)	(1.34)	(1.17)	(0.67)	(0.33)	(0.19)	(0.15)	(0.13)	(0.13)
10.003	399872	0.243	0.268	0.284	0.234	0.121	0.067	0.040	0.030	0.027	0.027
		(1.32)	(1.76)	(1.97)	(1.76)	(0.88)	(0.47)	(0.27)	(0.23)	(0.21)	(0.19)
50.1	79872	0.481	0.534	0.573	0.481	0.249	0.137	0.085	0.068	0.062	0.060
		(3.29)	(3.84)	(3.84)	(3.71)	(1.79)	(1.10)	(0.62)	(0.47)	(0.46)	(0.44)
54	73728	0.502	0.561	0.597	0.500	0.263	0.141	0.089	0.070	0.064	0.062
		(3.87)	(4.46)	(4.76)	(3.87)	(1.93)	(1.12)	(0.69)	(0.50)	(0.48)	(0.50)
60	66560	0.529	0.594	0.637	0.529	0.271	0.151	0.094	0.074	0.067	0.064
		(3.95)	(3.95)	(4.61)	(3.95)	(2.14)	(1.11)	(0.72)	(0.55)	(0.51)	(0.48)
100	39936	0.663	0.732	0.788	0.675	0.348	0.191	0.120	0.094	0.087	0.084
		(4.67)	(5.22)	(6.04)	(5.08)	(2.61)	(1.41)	(0.94)	(0.70)	(0.65)	(0.65)
977	4096	1.931	2.216	2.403	2.067	1.078	0.599	0.384	0.316	0.293	0.277
		(14.1)	(15.9)	(18.7)	(15.5)	(8.33)	(4.50)	(2.89)	(2.51)	(2.22)	(2.06)
1953	2048	2.697	3.050	3.325	2.896	1.489	0.832	0.535	0.442	0.402	0.390
		(20.1)	(23.1)	(27.6)	(22.9)	(10.7)	(6.59)	(4.00)	(3.27)	(2.89)	(2.98)
3906	1024	3.636	4.098	4.507	3.938	2.052	1.145	0.740	0.602	0.563	0.537
		(27.9)	(31.8)	(31.6)	(30.7)	(15.4)	(8.83)	(5.53)	(4.63)	(4.03)	(4.26)
15625	256	5.226	5.936	6.801	5.927	3.170	1.791	1.154	0.988	0.921	0.884
		(40.2)	(48.0)	(50.5)	(47.4)	(24.2)	(13.3)	(8.68)	(7.57)	(6.94)	(6.67)
17857	224	6.076	6.764	7.896	6.624	3.771	2.376	1.721	1.417	1.205	1.012
		(45.4)	(48.9)	(59.1)	(47.8)	(28.9)	(17.4)	(12.8)	(11.3)	(9.54)	(7.93)
31250	128	8.214	8.876	10.65	9.046	5.059	3.158	2.311	1.936	1.661	1.399
		(60.2)	(66.4)	(78.2)	(67.3)	(39.4)	(22.8)	(19.9)	(13.8)	(12.9)	(10.8)
41667	96	9.363	10.27	12.50	10.84	6.065	3.816	2.743	2.314	2.002	1.699
		(67.5)	(78.1)	(95.7)	(83.0)	(45.2)	(28.4)	(20.7)	(16.7)	(15.5)	(13.5)
62500	64	11.76	13.09	16.36	14.50	8.139	4.996	3.531	3.071	2.638	2.364
		(87.5)	(95.4)	(126)	(106)	(57.6)	(37.5)	(27.1)	(22.7)	(21.0)	(16.9)
125000	32	63.20	64.38	66.39	39.73	21.06	11.65	7.214	5.870	5.167	4.829
		(468)	(472)	(495)	(320)	(156)	(88.4)	(58.2)	(48.2)	(40.5)	(39.9)

Note: "Bypass" indicates the state where both PGA and BUF are disabled, "BUF" indicates the state where PGA is disabled and BUF is enabled, and "PGA" indicates the state where PGA is enabled.

Note: The upper rows indicate RMS noise (μV_{RMS}) and the lower rows (in parentheses) indicate peak-to-peak noise (μV_{PP}).

Table 2.86 Effective Resolution

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^5$+$Sinc^1$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 1 (Bypass)	Gain = 1 (BUF)	Gain = 1 (PGA)	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
3.814	1048576	24.0	24.0	24.0	23.8	23.7	23.8	23.4	22.9	22.1	21.2
		(22.2)	(21.8)	(21.8)	(21.0)	(20.8)	(20.8)	(20.7)	(20.0)	(19.2)	(18.2)
10.003	399872	24.0	24.0	24.0	23.3	23.3	23.2	22.9	22.3	21.4	20.5
		(21.9)	(21.4)	(21.3)	(20.4)	(20.4)	(20.4)	(20.1)	(19.4)	(18.5)	(17.7)
50.1	79872	23.3	23.2	23.1	22.3	22.3	22.1	21.8	21.1	20.3	19.3
		(20.5)	(20.3)	(20.3)	(19.4)	(19.4)	(19.1)	(18.9)	(18.3)	(17.4)	(16.4)
54	73728	23.2	23.1	23.0	22.3	22.2	22.1	21.7	21.1	20.2	19.3
		(20.3)	(20.1)	(20.0)	(19.3)	(19.3)	(19.1)	(18.8)	(18.2)	(17.3)	(16.3)
60	66560	23.2	23.0	22.9	22.2	22.1	22.0	21.7	21.0	20.1	19.2
		(20.3)	(20.3)	(20.0)	(19.3)	(19.2)	(19.1)	(18.7)	(18.1)	(17.2)	(16.3)
100	39936	22.8	22.7	22.6	21.8	21.8	21.6	21.3	20.7	19.8	18.8
		(20.0)	(19.9)	(19.7)	(18.9)	(18.9)	(18.8)	(18.3)	(17.8)	(16.9)	(15.9)
977	4096	21.3	21.1	21.0	20.2	20.1	20.0	19.6	18.9	18.0	17.1
		(18.4)	(18.3)	(18.0)	(17.3)	(17.2)	(17.1)	(16.7)	(15.9)	(15.1)	(14.2)
1953	2048	20.8	20.6	20.5	19.7	19.7	19.5	19.2	18.4	17.6	16.6
		(17.9)	(17.7)	(17.5)	(16.7)	(16.8)	(16.5)	(16.3)	(15.5)	(14.7)	(13.7)
3906	1024	20.4	20.2	20.1	19.3	19.2	19.1	18.7	18.0	17.1	16.1
		(17.4)	(17.3)	(17.3)	(16.3)	(16.3)	(16.1)	(15.8)	(15.0)	(14.2)	(13.2)
15625	256	19.9	19.7	19.5	18.7	18.6	18.4	18.0	17.3	16.4	15.4
		(16.9)	(16.7)	(16.6)	(15.7)	(15.7)	(15.5)	(15.1)	(14.3)	(13.5)	(12.5)
17857	224	19.7	19.5	19.3	18.5	18.3	18.0	17.5	16.8	16.0	15.2
		(16.8)	(16.6)	(16.4)	(15.7)	(15.4)	(15.1)	(14.6)	(13.8)	(13.0)	(12.3)
31250	128	19.2	19.1	18.8	18.1	17.9	17.6	17.0	16.3	15.5	14.8
		(16.3)	(16.2)	(16.0)	(15.2)	(15.0)	(14.7)	(13.9)	(13.5)	(12.6)	(11.8)
41667	96	19.0	18.9	18.6	17.8	17.7	17.3	16.8	16.0	15.3	14.5
		(16.2)	(16.0)	(15.7)	(14.9)	(14.8)	(14.4)	(13.9)	(13.2)	(12.3)	(11.5)
62500	64	18.7	18.5	18.2	17.4	17.2	16.9	16.4	15.6	14.9	14.0
		(15.8)	(15.7)	(15.3)	(14.5)	(14.4)	(14.0)	(13.5)	(12.8)	(11.9)	(11.2)
125000	32	16.3	16.2	16.2	15.9	15.9	15.7	15.4	14.7	13.9	13.0
		(13.4)	(13.4)	(13.3)	(12.9)	(13.0)	(12.8)	(12.4)	(11.7)	(10.9)	(9.9)

Effective resolution = $\log_2$(full-scale voltage/RMS noise)

Noise-free resolution = $\log_2$(full-scale voltage/peak-to-peak noise)

Note: "Bypass" indicates the state where both PGA and BUF are disabled, "BUF" indicates the state where PGA is disabled and BUF is enabled, and "PGA" indicates the state where PGA is enabled.

Note: The upper rows indicate effective resolution (bits) and the lower rows (in parentheses) indicate noise-free resolution (bits).

Table 2.87 24-Bit Delta-Sigma A/D Converter Characteristics (High-Voltage Inputs) (1)
Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = HVCOM =0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gain		Gain		0.1		—	Gain = $Gain_{Voltage-divider}$ × $Gain_{PGA}$ $Gain_{Voltage-divider}$: Gain of the voltage divider $Gain_{PGA}$: Gain of the PGA
Output data rate		f_{DR}	3.8	—	125000	SPS	f_{MOD} = 4 MHz
Resolution (no missing codes)		—	24	—	—	Bits	
RMS noise		V_N	—	Table 2.92 to Table 2.94	—	—	Figure 2.74 to Figure 2.79
Normal mode rejection ratio	External clock, 50 Hz, 60 Hz	NMRR	120	—	—	dB	10 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
			75	—	—		54 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
	External clock, 50 Hz		120	—	—		50 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz
	External clock, 60 Hz		120	—	—		60 SPS, $Sinc^4$+$Sinc^4$ 60 ± 1 Hz
	Internal clock (HOCO), 50 Hz, 60 Hz		110	—	—		10 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
			70	—	—		54 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz, 60 ± 1 Hz
	Internal clock (HOCO), 50 Hz		110	—	—		50 SPS, $Sinc^4$+$Sinc^4$ 50 ± 1 Hz
	Internal clock (HOCO), 60 Hz		110	—	—		60 SPS, $Sinc^4$+$Sinc^4$ 60 ± 1 Hz
Disconnect detection assist currents		—		0.5, 2, 4, 20		µA	
Modulator clock		f_{MOD}	100	4000	4100	kHz	

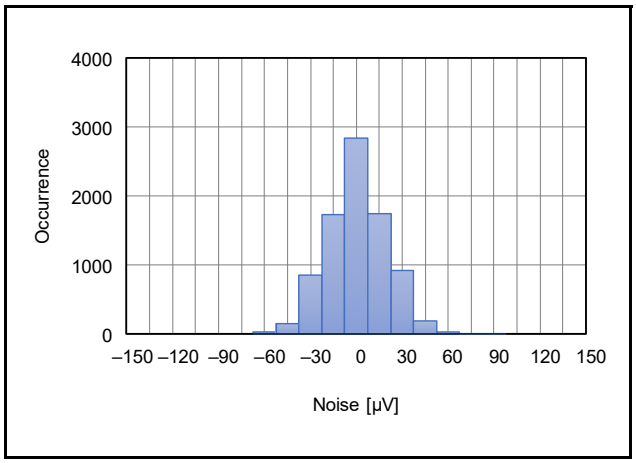


Figure 2.74 **Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA disabled, BUF enabled), f_{MOD} = 4 MHz, f_{DR} = 976.6 SPS, $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V)**

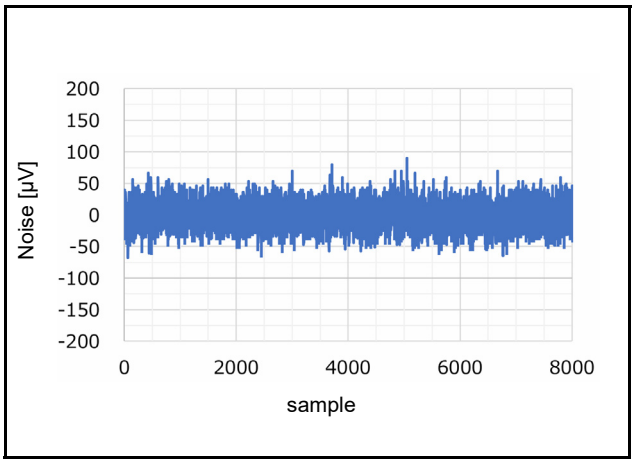


Figure 2.75 **Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA disabled, BUF enabled), f_{MOD} = 4 MHz, f_{DR} = 976.6 SPS, $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V)**

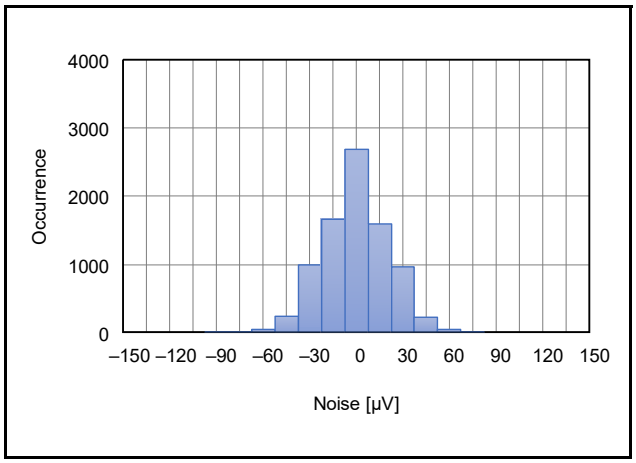


Figure 2.76 **Noise Histogram (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA enabled, BUF enabled), f_{MOD} = 4 MHz, f_{DR} = 976.6 SPS, $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V)**

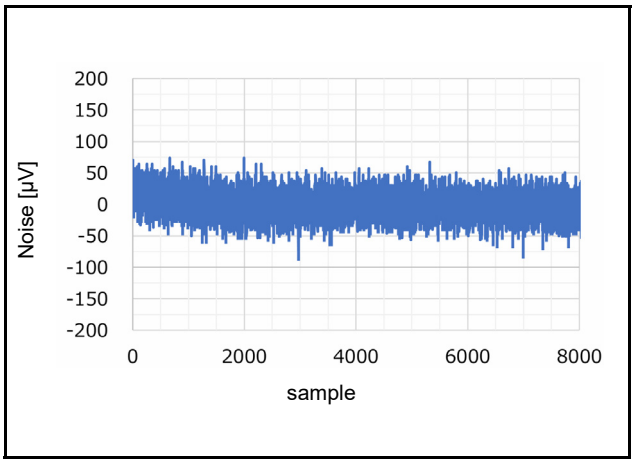


Figure 2.77 **Plot of Noise (AVCC0 = 5.0 V, T_a = 25°C, Gain = 1 (PGA enabled, BUF enabled), f_{MOD} = 4 MHz, f_{DR} = 976.6 SPS, $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V)**

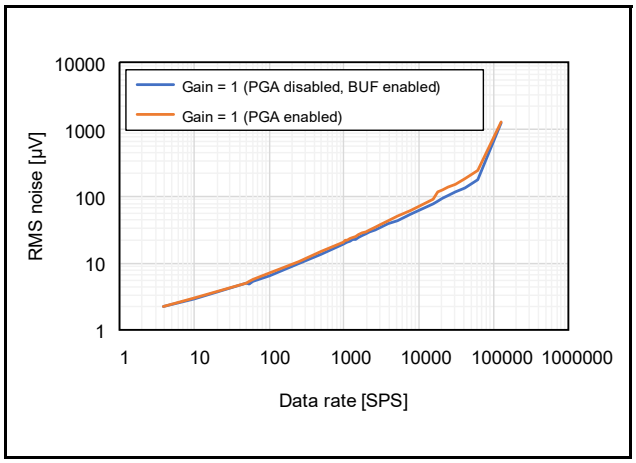


Figure 2.78 **Data Rate Dependence of RMS Noise (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, $Sinc^4$ Filter or $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)**

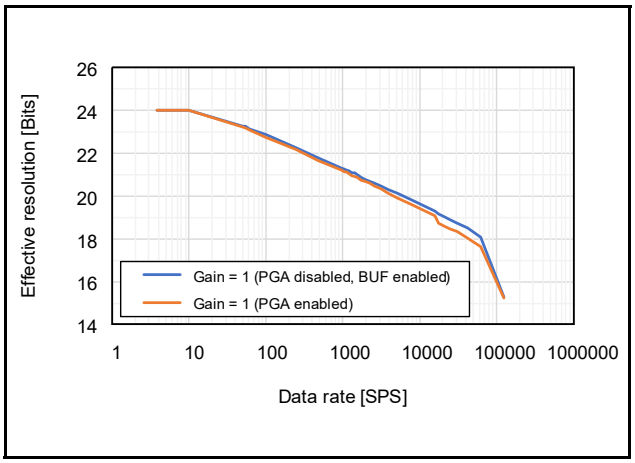


Figure 2.79 **Data Rate Dependence of Effective Resolution (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, $Sinc^4$ Filter or $Sinc^4$+$Sinc^4$ Filter, V_{ID} = 0 V, V_{REF} = 2.5 V, Reference buffer disabled)**

Table 2.88 24-Bit Delta-Sigma A/D Converter Characteristics (High-Voltage Inputs) (2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = HVCOM =0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≥ 1024 ($Sinc^4$+$Sinc^4$), OSR ≥ 8192 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Integral non-linearity	PGA enabled, BUF enabled	INL	—	±20	—	ppmFSR	Figure 2.80
	PGA disabled, BUF enabled		—	±20	±80		
Offset error	Before calibration	E_O	—	—	±50	mV	AVCC0 = 5.0 V, T_a = 25°C
	After calibration		—	On the level of the noise	—		
Offset drift	PGA enabled, BUF enabled	dE_O	—	15	45	nV/°C	
	PGA disabled, BUF enabled		—	15	55		
Gain error	Before calibration of gain errors	E_G	—	±0.8	±2.0	%	AVCC0 = 5.0 V, T_a = 25°C
	After calibration of gain errors		—	On the level of the noise	—		
Gain drift	PGA enabled, BUF enabled	dE_G	—	3	15	ppm/°C	
	PGA disabled, BUF enabled		—	3	17		
Power supply rejection ratio	PGA enabled, BUF enabled	PSRR	—	50	—	dB	V_{ID} = 10 V (DC)
	PGA disabled, BUF enabled		—	50	—		
Common mode rejection ratio	PGA enabled, BUF enabled	CMRR	60	70	—	dB	V_{ID} = 10 V (DC)
	PGA disabled, BUF enabled		55	65	—		

Table 2.89 24-Bit Delta-Sigma A/D Converter Characteristics (High-Voltage Inputs) (3)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = HVCOM = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, 256 ≤ OSR ≤ 768 ($Sinc^4$+$Sinc^4$), 256 ≤ OSR ≤ 7936 ($Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Integral non-linearity	PGA enabled, BUF enabled	INL	—	±30	—	ppmFSR	
	PGA disabled, BUF enabled		—	±20	±80		
Offset error	Before calibration	E_O	—	—	±50	mV	AVCC0 = 5.0 V, T_a = 25°C
	After calibration		—	On the level of the noise	—		
Offset drift	PGA enabled, BUF enabled	dE_O	—	15	45	nV/°C	
	PGA disabled, BUF enabled		—	15	55		
Gain error	Before calibration of gain errors	E_G	—	±0.8	±2.0	%	AVCC0 = 5.0 V, T_a = 25°C
	After calibration of gain errors		—	On the level of the noise	—		
Gain drift	PGA enabled, BUF enabled	dE_G	—	6	25	ppm/°C	
	PGA disabled, BUF enabled		—	3	17		
Power supply rejection ratio	PGA enabled, BUF enabled	PSRR	—	50	—	dB	V_{ID} = 10 V (DC)
	PGA disabled, BUF enabled		—	50	—		
Common mode rejection ratio	PGA enabled, BUF enabled	CMRR	—	70	—	dB	V_{ID} = 10 V (DC)
	PGA disabled, BUF enabled		55	65	—		

Table 2.90 24-Bit Delta-Sigma A/D Converter Characteristics (High-Voltage Inputs) (4)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = HVCOM = 0 V, V_{REF} = 2.5 V, f_{MOD} = 4 MHz, OSR ≤ 224 ($Sinc^4$+$Sinc^4$, $Sinc^5$+$Sinc^1$), T_a = –40 to +105°C, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Integral non-linearity	PGA enabled, BUF enabled	INL	—	±70	—	ppmFSR	
	PGA disabled, BUF enabled		—	±20	±80		
Offset error	Before calibration	E_O	—	—	±50	mV	AVCC0 = 5.0 V, T_a = 25°C
	After calibration		—	On the level of the noise	—		
Offset drift	PGA enabled, BUF enabled	dE_O	—	15	45	nV/°C	
	PGA disabled, BUF enabled		—	15	55		
Gain error	Before calibration of gain errors	E_G	—	±0.8	±2.0	%	AVCC0 = 5.0 V, T_a = 25°C
	After calibration of gain errors		—	On the level of the noise	—		
Gain drift	PGA enabled, BUF enabled	dE_G	—	15	75	ppm/°C	
	PGA disabled, BUF enabled		—	3	17		
Power supply rejection ratio	PGA enabled, BUF enabled	PSRR	—	45	—	dB	V_{ID} = 10 V (DC)
	PGA disabled, BUF enabled		—	50	—		
Common mode rejection ratio	PGA enabled, BUF enabled	CMRR	—	65	—	dB	V_{ID} = 10 V (DC)
	PGA disabled, BUF enabled		55	65	—		

Table 2.91 24-Bit Delta-Sigma A/D Converter Analog Input Characteristics (High-Voltage Inputs) (5)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = HVCOM = 0 V, V_{REF} = 2.5 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Differential input voltage range	Gain = 0.1	V_{IDR}	−10	—	10	V	Specified Performance
			Whichever is greater of the values of $-V_{REF}$/ Gain and −20	—	Whichever is smaller of the values of $+V_{REF}$ / Gain and +20	V	Functional $V_{REF} = V_{(VR0P)} - V_{(VR0N)}$
Absolute input voltage range		V_I	−10	—	10	V	
Input bias current		I_{IB}	5	7	11	μA	Figure 2.81 V_I = +10 V
			−17	−11	−8		V_I = −10 V
Input bias current drift		dI_{IB}	—	0.7	2.3	pA/°C	
Impedance		—	0.9	1.4	2	MΩ	V_I = +10 V
			0.6	0.9	1.25	MΩ	V_I = −10 V

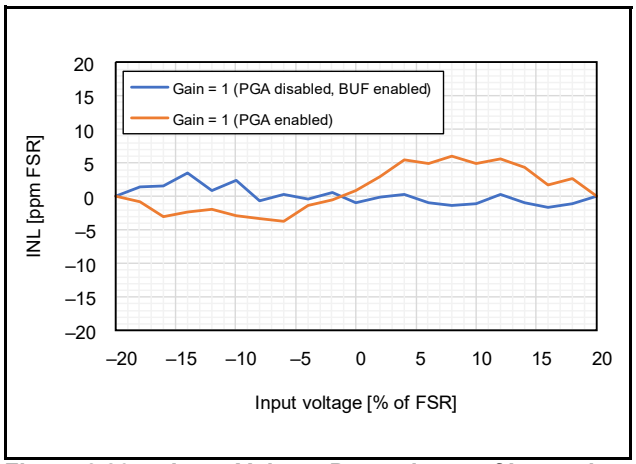


Figure 2.80 Input Voltage Dependence of Integral Non-Linearity (AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, Total oversampling ratio = 4096, V_{REF} = 2.5 V)

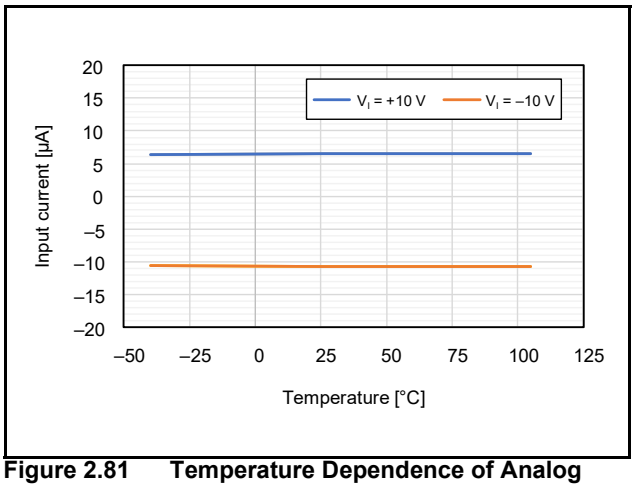


Figure 2.81 Temperature Dependence of Analog Input Current (AVCC0 = 5.0 V, f_{MOD} = 4 MHz, Total oversampling ratio = 4096)

Table 2.92 Typical Noise Characteristics (High-Voltage Inputs)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^4$+$Sinc^4$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 0.1 (BUF)	Gain = 0.1 (PGA)
3.814	1048576	2.285	2.173
		(13.39)	(13.39)
10.003	399872	2.871	2.929
		(19.78)	(17.31)
50.1	79872	4.815	5.029
		(33.37)	(36.40)
54	73728	4.795	4.950
		(35.52)	(35.52)
60	66560	5.151	5.404
		(37.74)	(37.74)
100	39936	6.322	6.759
		(48.54)	(48.54)
977	4096	18.29	19.53
		(143.9)	(157.3)
1953	2048	25.45	27.80
		(189.1)	(195.8)
3906	1024	36.36	40.47
		(269.4)	(311.2)
15625	256	72.33	87.76
		(547.2)	(676.0)
17857	224	81.57	110.7
		(588.1)	(856.4)
31250	128	108.4	147.3
		(809.9)	(1029)
41667	96	124.6	173.6
		(909.7)	(1285)
62500	64	175.3	233.3
		(1322)	(1760)
125000	32	1274	1285
		(8976)	(9287)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate RMS noise (μV_{RMS}) and the lower rows (in parentheses) indicate peak-to-peak noise (μV_{PP}).

Table 2.93 Effective Resolution (High-Voltage Inputs)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^4$+$Sinc^4$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 0.1 (BUF)	Gain = 0.1 (PGA)
3.814	1048576	24.0	24.0
		(18.5)	(18.5)
10.003	399872	24.0	24.0
		(17.9)	(18.1)
50.1	79872	23.3	23.2
		(17.2)	(17.1)
54	73728	23.3	23.3
		(17.1)	(17.1)
60	66560	23.2	23.1
		(17.0)	(17.0)
100	39936	22.9	22.8
		(16.7)	(16.7)
977	4096	21.4	21.3
		(15.1)	(15.0)
1953	2048	20.9	20.8
		(14.7)	(14.6)
3906	1024	20.4	20.2
		(14.2)	(14.0)
15625	256	19.4	19.1
		(13.2)	(12.9)
17857	224	19.2	18.8
		(13.1)	(12.5)
31250	128	18.8	18.4
		(12.6)	(12.2)
41667	96	18.6	18.1
		(12.4)	(11.9)
62500	64	18.1	17.7
		(11.9)	(11.5)
125000	32	15.3	15.2
		(9.1)	(9.1)

Effective resolution = $\log_2$(full-scale voltage/RMS noise)

Noise-free resolution = $\log_2$(full-scale voltage/peak-to-peak noise)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate effective resolution (bits) and the lower rows (in parentheses) indicate noise-free resolution (bits).

Table 2.94 Typical Noise Characteristics (High-Voltage Inputs)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^5$+$Sinc^1$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 0.1 (BUF)	Gain = 0.1 (PGA)
3.814	1048576	2.656	2.791
		(18.41)	(20.08)
10.003	399872	3.379	3.519
		(24.13)	(24.13)
50.1	79872	6.349	6.763
		(43.93)	(52.18)
54	73728	6.578	7.087
		(50.57)	(47.59)
60	66560	7.099	7.519
		(52.72)	(56.02)
100	39936	8.744	9.389
		(63.15)	(68.66)
977	4096	25.69	29.47
		(192.4)	(225.9)
1953	2048	35.69	40.31
		(289.5)	(297.9)
3906	1024	47.88	55.15
		(339.7)	(431.7)
15625	256	69.04	81.43
		(513.7)	(622.5)
17857	224	77.43	103.7
		(574.2)	(769.9)
31250	128	102.1	138.9
		(801.6)	(1006)
41667	96	117.6	163.3
		(914.9)	(1208)
62500	64	148.6	208.7
		(1131)	(1504)
125000	32	648	701
		(4767)	(5335)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate RMS noise (μV_{RMS}) and the lower rows (in parentheses) indicate peak-to-peak noise (μV_{PP}).

Table 2.95 Effective Resolution (High-Voltage Inputs)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, AVCC0 = 5.0 V, T_a = 25°C, f_{MOD} = 4 MHz, V_{ID} = 0 V, V_{REF} = 2.5 V, $Sinc^5$+$Sinc^1$, DS0mISR.RSEL[1:0] = 00b (m = 0 to 7)

f_{DR} (SPS)	OSR	Gain = 0.1 (BUF)	Gain = 0.1 (PGA)
3.814	1048576	24.0	24.0
		(18.1)	(17.9)
10.003	399872	23.8	23.8
		(17.7)	(17.7)
50.1	79872	22.9	22.8
		(16.8)	(16.5)
54	73728	22.9	22.8
		(16.6)	(16.7)
60	66560	22.7	22.7
		(16.5)	(16.4)
100	39936	22.4	22.3
		(16.3)	(16.2)
977	4096	20.9	20.7
		(14.7)	(14.4)
1953	2048	20.4	20.2
		(14.1)	(14.0)
3906	1024	20.0	19.8
		(13.8)	(13.5)
15625	256	19.5	19.2
		(13.2)	(13.0)
17857	224	19.3	18.9
		(13.1)	(12.7)
31250	128	18.9	18.5
		(12.6)	(12.3)
41667	96	18.7	18.2
		(12.4)	(12.0)
62500	64	18.4	17.9
		(12.1)	(11.7)
125000	32	16.2	16.1
		(10.0)	(9.9)

Effective resolution = $\log_2$(full-scale voltage/RMS noise)

Noise-free resolution = $\log_2$(full-scale voltage/peak-to-peak noise)

Note: “Bypass” indicates the state where both PGA and BUF are disabled, “BUF” indicates the state where PGA is disabled and BUF is enabled, and “PGA” indicates the state where PGA is enabled.

Note: The upper rows indicate effective resolution (bits) and the lower rows (in parentheses) indicate noise-free resolution (bits).

2.12 Analog Front End Characteristics

Table 2.96 Voltage Reference Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage	V_{REFOUT}	—	2.5	—	V	Figure 2.82
Initial accuracy	—	—	±0.04	±0.2	%	Figure 2.83 T_a = 25°C
Temperature drift	—	—	8	30	ppm/°C	Figure 2.82, Figure 2.84 T_a = –40 to +85°C
		—	10	30		T_a = –40 to +105°C
Load current	I_L	—	—	±10	mA	
Load regulation (40-pin HWQFN, 48-pin LFQFP)	—	—	–35	–50	µV/mA	Figure 2.85 I_L= 0 to +10 mA
		—	350	500		I_L = –10 to 0 mA T_a = –40 to +85°C
		—	350	550		I_L = –10 to 0 mA T_a = –40 to +105°C
Load regulation (64-pin LFQFP, 80-pin LFQFP, 100-pin LFQFP, 100-pin TFBGA)	—	—	–55	–70	µV/mA	Figure 2.85 I_L= 0 to +10 mA
		—	350	500		I_L = –10 to 0 mA T_a = –40 to +85°C
		—	350	550		I_L = –10 to 0 mA T_a = –40 to +105°C
Power supply rejection ratio	PSRR	70	80	—	dB	DC

Table 2.97 Bias Voltage Generator Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage	V_{BIAS}	(AVCC0 + AVSS0)/2 – 0.02	(AVCC0 + AVSS0)/2	(AVCC0 + AVSS0)/2 + 0.02	V	
Startup time	t_{START}	—	—	20	µs/nF	

Table 2.98 Temperature Sensor Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Accuracy		—	—	—	±5	°C	Figure 2.86
Voltage sensitivity coefficient	Second-order	TC_{SNS}	—	$–6.37 \times 10^{–13}$	—	°C/LSB^2	
	First-order		—	$7.60 \times 10^{–5}$	—	°C/LSB	
	Zeroth-order		—	–275.65	—	°C	
Output code		—	—	3E9464 (4101221)	—	—	

Table 2.99 Excitation Current Source Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output current	IEXC	50, 100, 250, 500, 750, 1000			µA	Figure 2.87
Initial accuracy	—	—	±1	±5	%	Figure 2.88 T_a = 25°C
Temperature drift	—	—	25	60	ppm/°C	
Current matching	—	—	±0.2	±2.0	%	Figure 2.89, Figure 2.90 T_a = 25°C
Drift matching	—	—	5	30	ppm/°C	Matching between IEXC0 and IEXC1
Line regulation	—	—	0.05	0.30	%/V	
Load regulation	—	—	0.1	0.5	%/V	
Compliance voltage	V_{COMP}	AVSS0 – 0.05	—	AVCC0 – 0.9	V	Figure 2.91 Output current error = –2.0%

Table 2.100 External Reference Input Characteristics

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Differential input voltage range		V_{REF}	1	2.5	AVCC0	V	$V_{REF} = V_{(VR0P)} - V_{(VR0N)}$
Absolute input voltage range	Reference buffer disabled	$V_{(REF0P)}$, $V_{(REF1P)}$, $V_{(REF0N)}$, $V_{(REF1N)}$	AVSS0	—	AVCC0	V	Specified Performance
			AVSS0 – 0.05	—	AVCC0 + 0.05		Functional
	Reference buffer enabled		AVSS0 + 0.2	—	AVCC0 – 0.2		
Input current	Reference buffer disabled, PGA Gain = 1	I_b	—	65	90	µA/V	Figure 2.92 T_a = 25°C
	Reference buffer disabled, PGA Gain ≥ 2		—	40	50	µA/V	
	Reference buffer enabled		—	±15	±40	nA	Figure 2.93 T_a = 25°C
Input current drift	Reference buffer disabled, PGA Gain = 1	dI_b	—	9	30	nA/V/°C	T_a = –40 to +105°C
	Reference buffer disabled, PGA Gain ≥ 2		—	5.5	20	nA/V/°C	T_a = –40 to +105°C
	Reference buffer enabled		—	150	550	pA/°C	T_a = –40 to +105°C
Common mode rejection ratio	Reference buffer disabled	CMRR	85	95	—	dB	V_{ID} = 1 V (DC)
	Reference buffer enabled		75	90	—		

Table 2.101 Low Side Switch Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
On-state resistance	R_{ON}	—	—	10	Ω	
Off-state leakage current	I_{lkg}	—	—	0.1	μA	
Allowable current	I_{LIMIT}	—	—	30	mA	

Table 2.102 Low Power-Supply Voltage Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage (LVDET0)	DET0LVL = 0	V_{DET0}	1.83	2.00	2.17	V	Negative-going AVCC0
	DET0LVL = 1		1.70	1.86	2.02		
Non-responsive period (LVDET0)		t_{DET0}	—	—	20	μs	
Detection voltage (LVDET1)	DET1LVL[1:0] = 00b	V_{DET1}	3.50	3.80	4.10	V	Negative-going AVCC0
Non-responsive period (LVDET1)		t_{DET1}	—	—	20	μs	

Table 2.103 Input Voltage Fault Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Upper detection level for the analog input voltage	V_{IDETH}	AVCC0 + 0.05	AVCC0 + 0.2	—	V	
Lower detection level for the analog input voltage	V_{IDETL}	—	AVSS0 – 0.2	AVSS0 – 0.05	V	
Non-responsive period	t_{IDET}	—	—	20	μs	

Table 2.104 Reference Voltage Fault Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection level for external reference voltage differential	V_{RDET}	0.65	0.85	1.05	V	
Upper detection level for the external reference voltage	V_{RDETH}	AVCC0 – 0.7	AVCC0 – 0.4	—	V	
Lower detection level for the external reference voltage	V_{RDETL}	—	AVSS0 + 0.4	AVSS0 + 0.7	V	
Non-responsive period	t_{RDET}	—	—	20	μs	

Table 2.105 Excitation Current Source Disconnect Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection level for disconnection of the excitation current source	$V_{IEXCDET}$	AVCC0 – 0.35	AVCC0 – 0.06	—	V	
Non-responsive period	$t_{IEXCDET}$	—	—	20	μs	

Table 2.106 High Voltage Analog Common Input Disconnect Detector Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = HVCOM =0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Upper detection voltage for high voltage analog common inputs	$V_{HVCOMDETH}$	AVSS0 +0.05	AVSS0 +0.2	AVSS0 +0.4	V	
Lower detection voltage for high voltage analog common inputs	$V_{HVCOMDETL}$	AVSS0 –0.4	AVSS0 –0.2	AVSS0 –0.05	V	
Non-responsive period	$t_{HVCOMDET}$	—	—	20	µs	

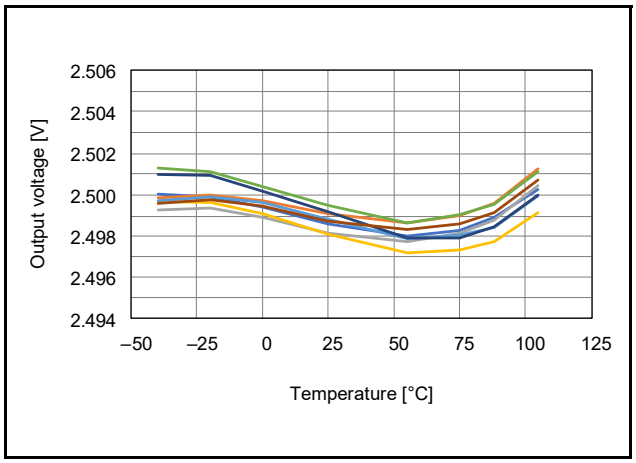


Figure 2.82 Temperature Dependence of Output Voltage of Voltage Reference (AVCC0 = 5.0 V)

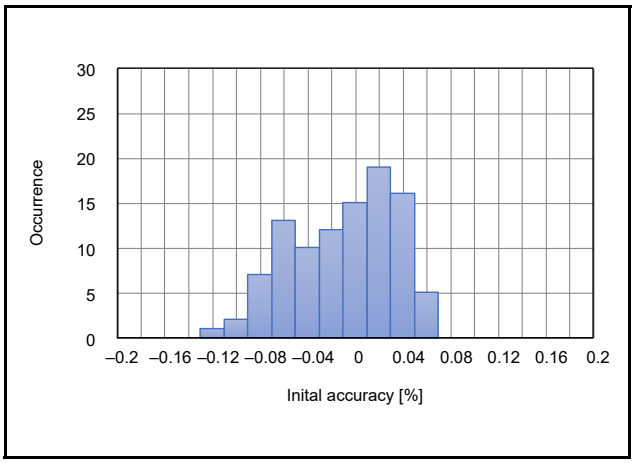


Figure 2.83 Initial Accuracy of Voltage Reference (AVCC0 = 5.0 V)

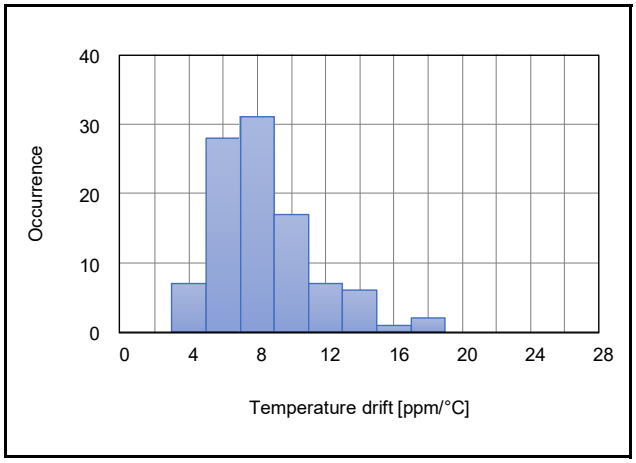


Figure 2.84 Reference Voltage Source Temperature Drift (AVCC0 = 5.0 V)

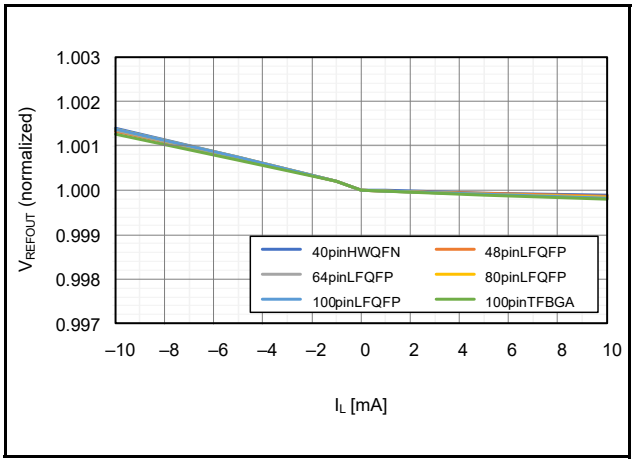


Figure 2.85 Load Regulation of Voltage Reference (AVCC0 = 5V, T_a = 25°C)

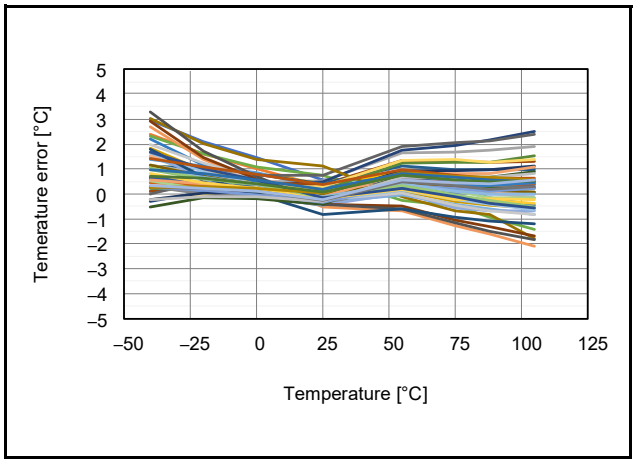


Figure 2.86 Accuracy of Temperature Sensor (AVCC0 = 5.0 V)

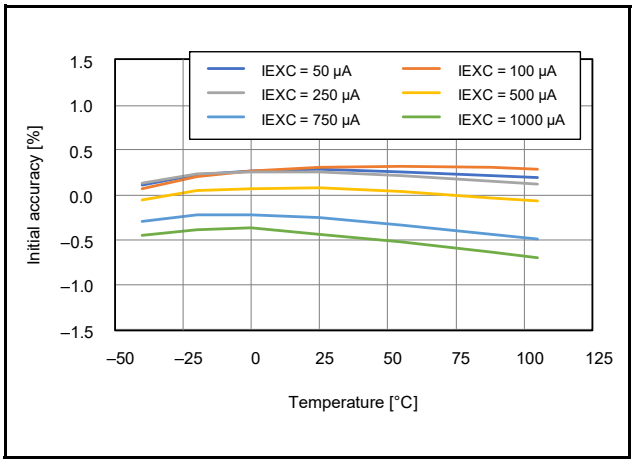


Figure 2.87 Temperature Dependence of Output Current of Excitation Current Source (AVCC0 = 5.0 V)

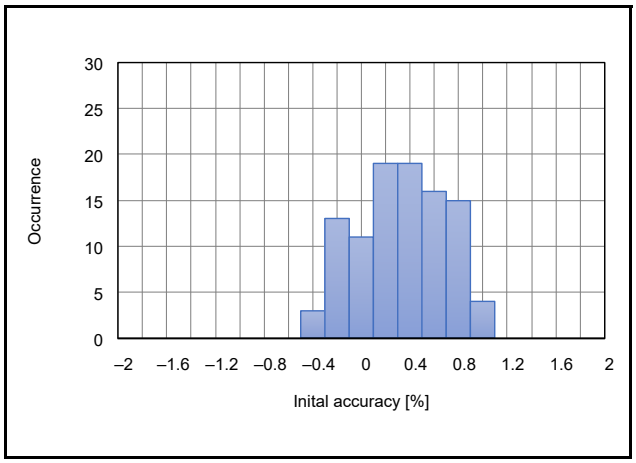


Figure 2.88 Initial Accuracy of Output Current of Excitation Current Source (AVCC0 = 5.0 V)

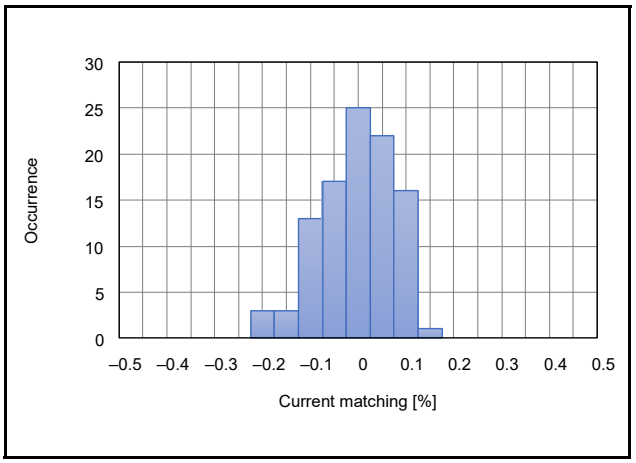


Figure 2.89 Matching of Output Current of Excitation Current Source (AVCC0 = 5.0 V, IEXC = 250 µA)

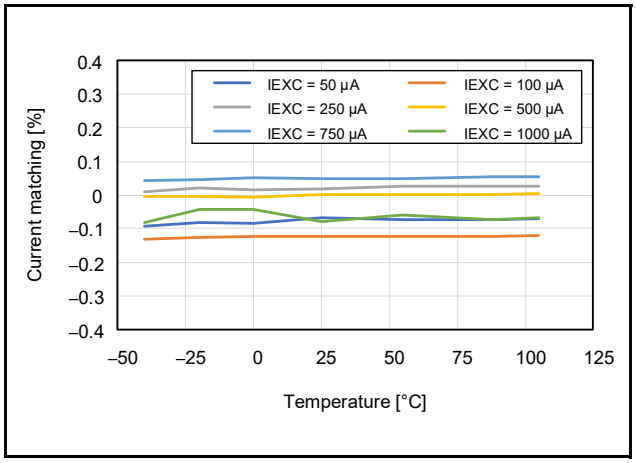


Figure 2.90 Temperature Dependence of Matching of Output Current of Excitation Current Source (AVCC0 = 5.0 V)

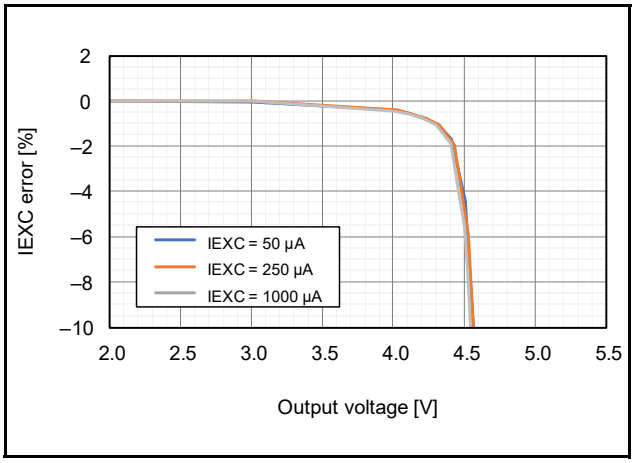


Figure 2.91 IEXC Accuracy vs Compliance Voltage (AVCC0 = 5.0 V, T_a = 25°C)

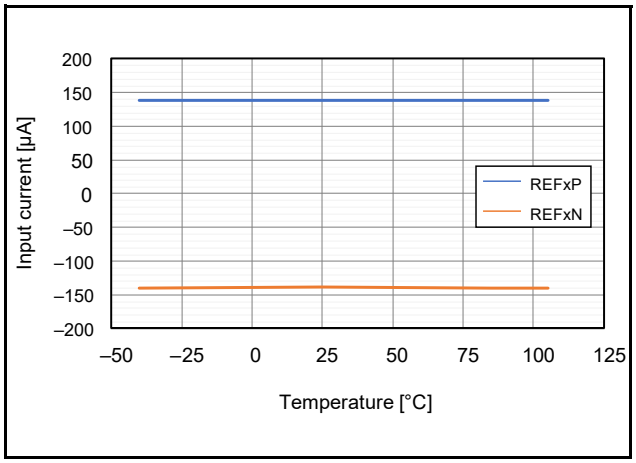


Figure 2.92 Temperature Dependence of External Reference Input Current (AVCC0 = 5.0 V, V_{REF} = 2.5 V, Reference Buffer Disabled)

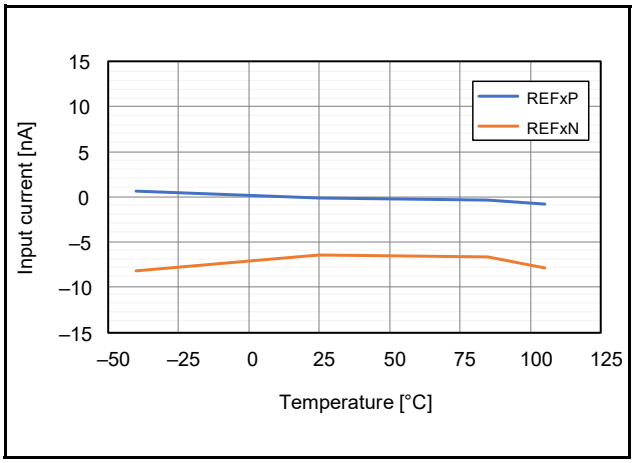


Figure 2.93 Temperature Dependence of External Reference Input Current (AVCC0 = 5.0 V, Reference Buffer Enabled)

2.13 12-Bit A/D Conversion Characteristics

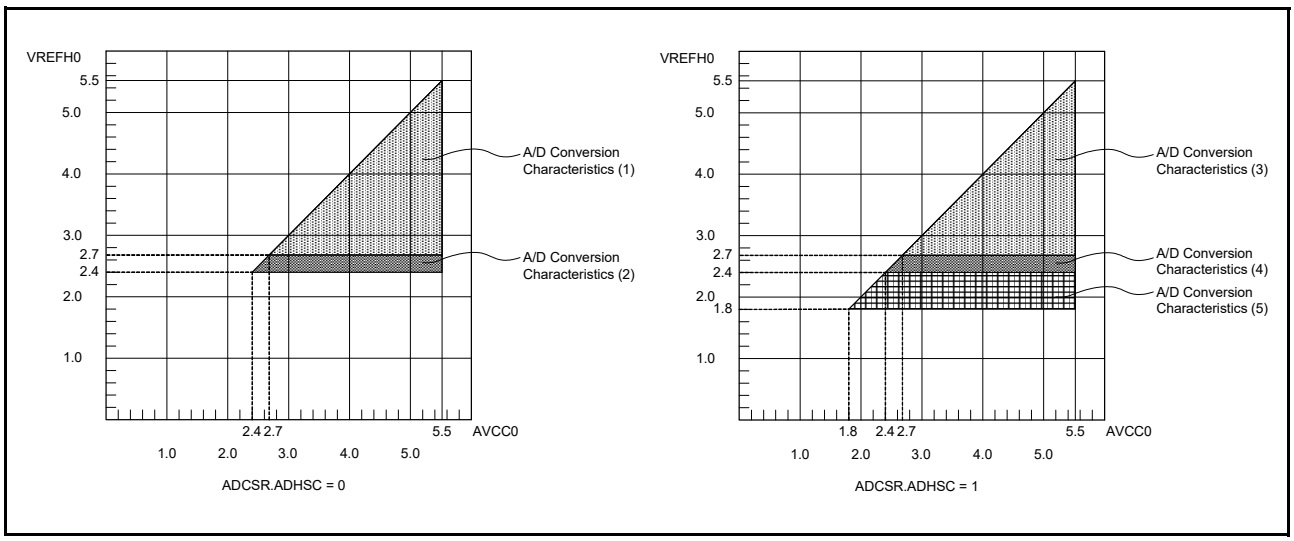


Figure 2.94 AVCC0 to VREFH0 Voltage Range

Table 2.107 12-Bit A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, Source impedance = 0.3 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)		1.41 (0.406)*2	—	—	µs	ADCSR.ADHSC bit = 0 ADSSTRn = 0Dh
Analog input capacitance	Cs	—	—	9*3	pF	
Analog input resistance	Rs	—	—	4.5*3	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. Reference values

Table 2.108 12-Bit A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, 2.4 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, Source impedance = 1.3 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)		2.82 (0.813)*2	—	—	µs	ADCSR.ADHSC bit = 0 ADSSTRn = 0Dh
Analog input capacitance	Cs	—	—	9*3	pF	
Analog input resistance	Rs	—	—	4.5*3	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±4.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. Reference values

Table 2.109 12-Bit A/D Conversion Characteristics (3)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, Source impedance = 1.1 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)		3 (1.481)*2	—	—	µs	ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	9*3	pF	
Analog input resistance	Rs	—	—	4.5*3	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. Reference values

Table 2.110 12-Bit A/D Conversion Characteristics (4)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, 2.4 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, Source impedance = 2.2 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)		5.06 (2.5)*2	—	—	µs	ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	9*3	pF	
Analog input resistance	Rs	—	—	4.5*3	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.50	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.00	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. Reference values

Table 2.111 12-Bit A/D Conversion Characteristics (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, 1.8 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, Source impedance = 5 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)		10.13 (5.0)*2	—	—	µs	ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	9*3	pF	
Analog input resistance	Rs	—	—	6*3	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±3.00	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. Reference values

Table 2.112 12-Bit A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
Analog input channel	AN000 to AN007	AVCC0 = 1.8 to 5.5 V	

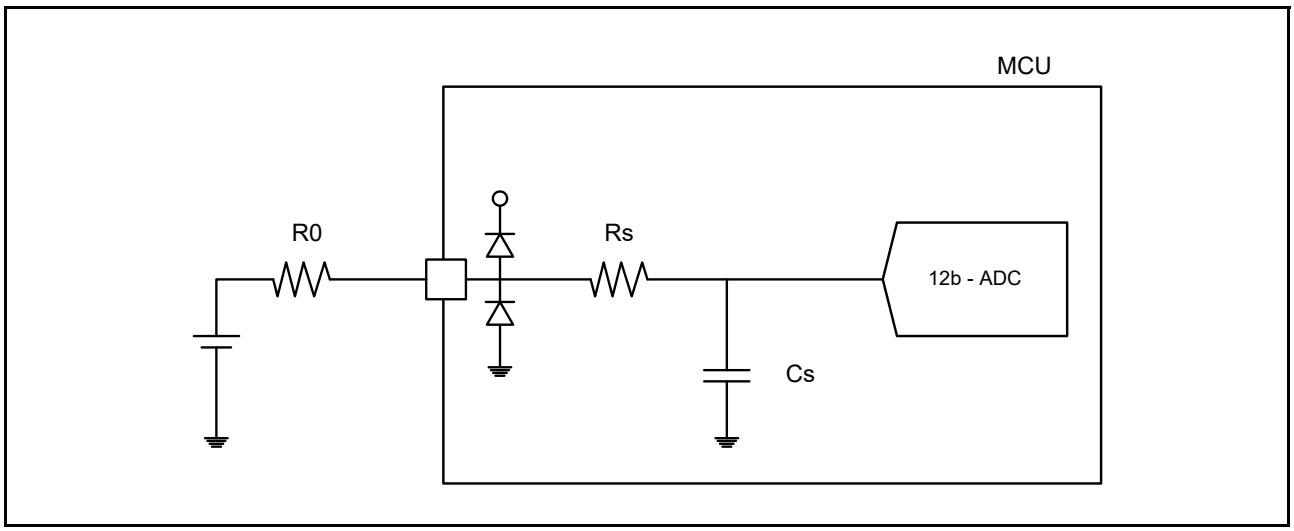


Figure 2.95 Equivalent Circuit

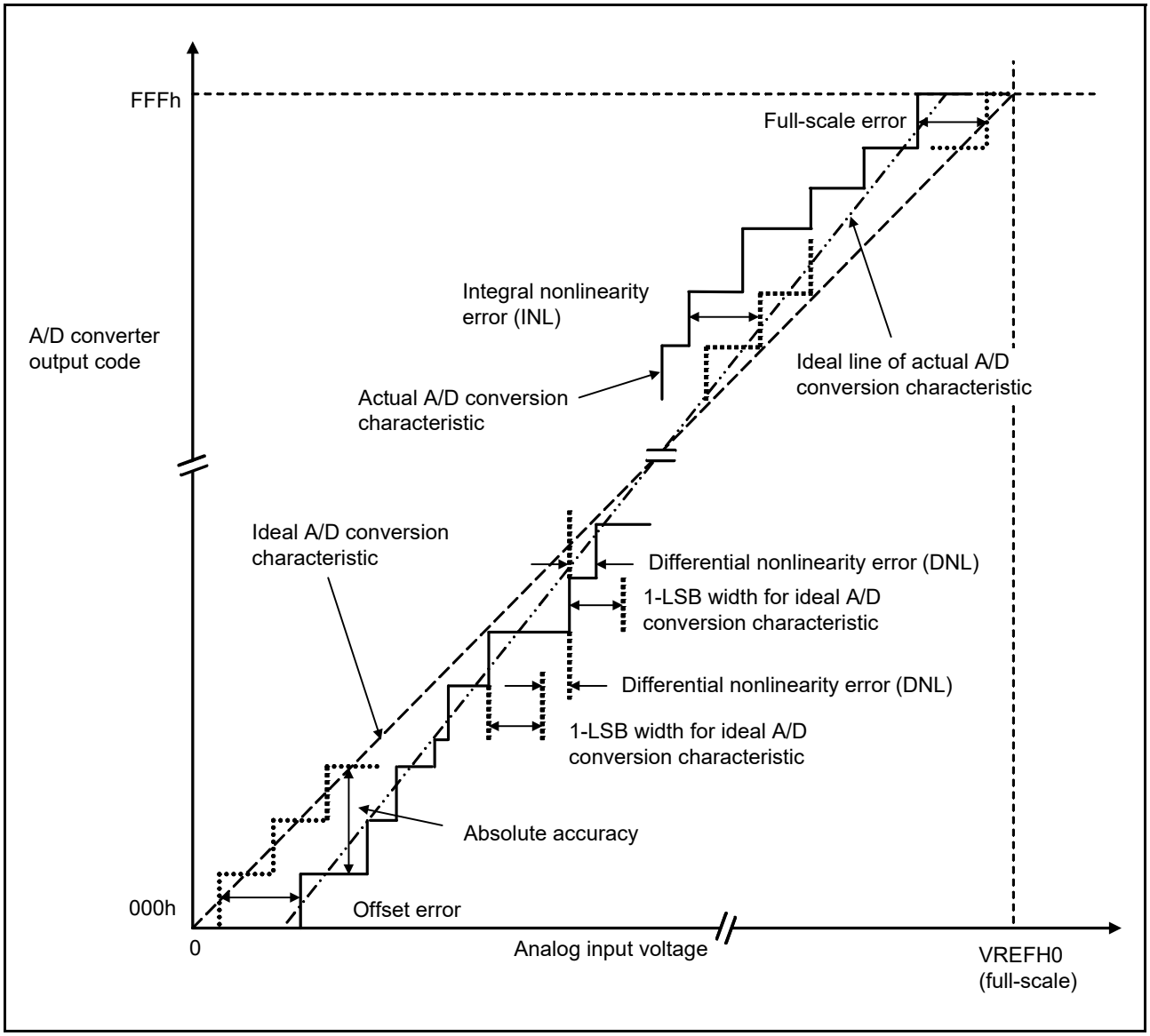


Figure 2.96 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

2.14 16-Bit D/A Conversion Characteristics

Table 2.113 D/A Conversion Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS = 0 V, VREFH ≥ 2.5 V, VREFL = 0 V, T_a = –40 to +105°C

Item		Symbol	min	typ	max	Unit	Test Conditions
Resolution		—	—	—	16	Bits	
Integral nonlinearity error*1		INL	—	±2	±5	LSB	Figure 2.97 VREFH ≥ 4.5 V
			—	±4	±8		2.5 V ≤ VREFH < 4.5 V
Differential nonlinearity error*1		DNL	—	±0.5	±1	LSB	Figure 2.98 VREFH ≥ 4.5 V
			—	±1	±2		2.5 V ≤ VREFH < 4.5 V
Offset error	Center code	E_O	—	±1	±7	mV	Figure 2.99 VREFH ≥ 4.5 V
			—	±2	±7		2.5 V ≤ VREFH < 4.5 V
Offset error drift	Center code	dE_O	—	3	12	µV/°C	Figure 2.99
Gain error*1		E_G	—	±0.5	±1	%FSR	Figure 2.100
Gain error drift*1		dE_G	—	1	5	ppm/°C	Figure 2.100 VREFH ≥ 4.5 V
			—	2	10		2.5 V ≤ VREFH < 4.5 V
Power supply rejection ratio	Center code	PSRR	—	–70	–60	dB	DC
Output voltage range		V_O	0	—	AVCC0	V	
Capacitive load		CL	—	—	90	pF	
Resistive load		RL	10	—	—	kΩ	
Settling time		t_{DCCONV}	—	10 + 1 CLKB	15.5 + 1 CLKB	µs	Transitions between 1/4 and 3/4 codes, ±2 LSB
Slew rate		—	0.25	0.5	—	V/µs	V_O: Change of voltage per unit of time measured in the range from 10% to 90% of output in transitions between 0.2 V and AVCC0 – 0.2 V
Buffer preparation time		$t_{startup}$	24	—	—	µs	
Output noise density	Center code	—	—	85	125	nV√Hz	10 kHz
Output noise voltage	Center code	—	—	15	25	µVpp	0.1 Hz–10 Hz
Output impedance	Center code	—	—	0.5	—	Ω	
Reference voltage range	Characteristic guaranteed range	VREF	2.5	—	AVCC0	V	VREF = VREFH–VREFL
	Function guaranteed range		2.4	—	AVCC0		
Reference input impedance		—	30	50	—	kΩ	

Note 1. The characteristic guaranteed range of the output voltage is 0.2 V ≤ V_O ≤ AVCC – 0.2 V.

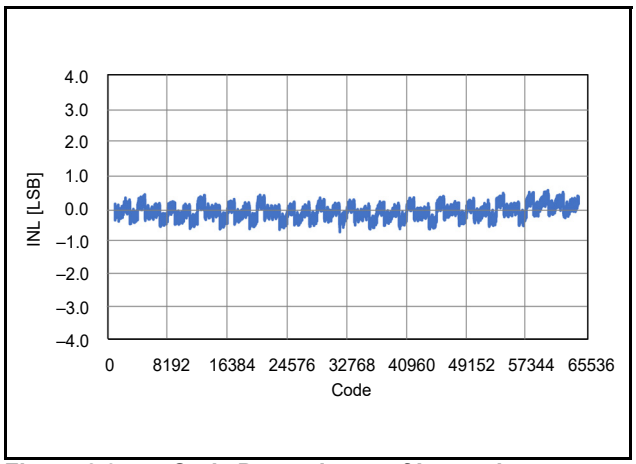


Figure 2.97 Code Dependence of Integral Nonlinearity Error (AVCC0 = 5V, VREFH = 5V, T_a = 25°C)

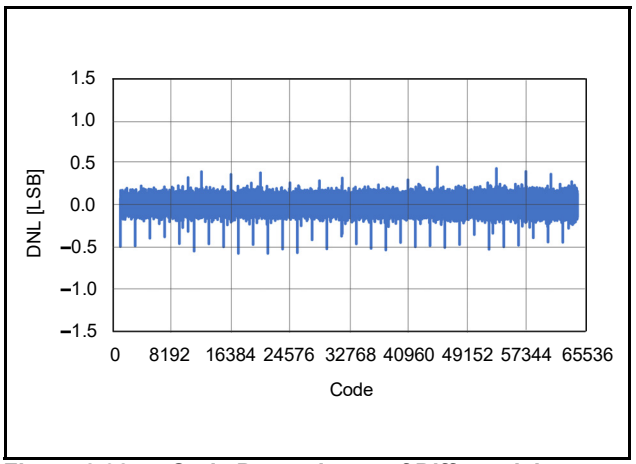


Figure 2.98 Code Dependence of Differential Nonlinearity Error (AVCC0 = 5V, VREFH = 5V, T_a = 25°C)

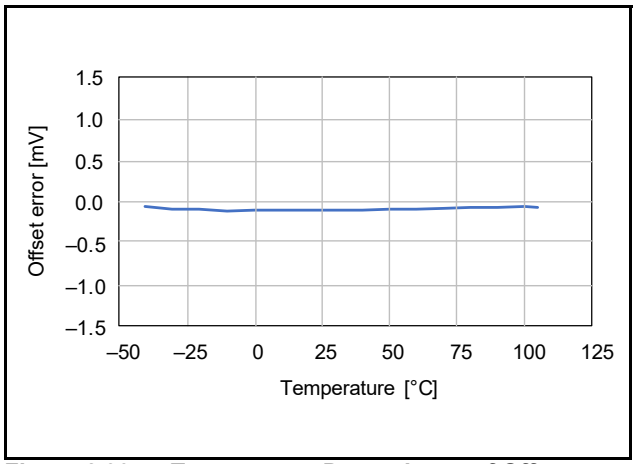


Figure 2.99 Temperature Dependence of Offset Error (AVCC0 = 5V, VREFH = 5V)

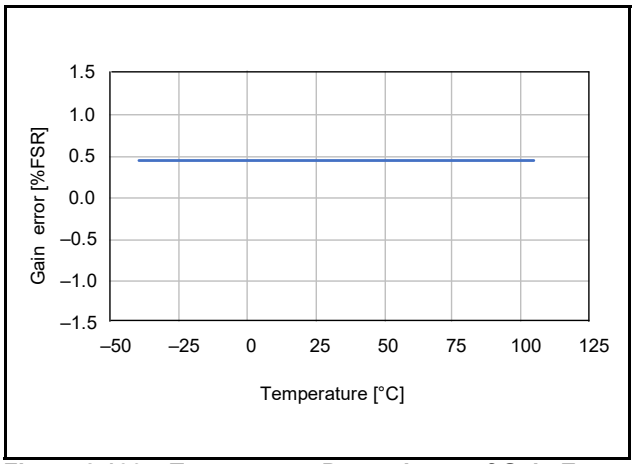
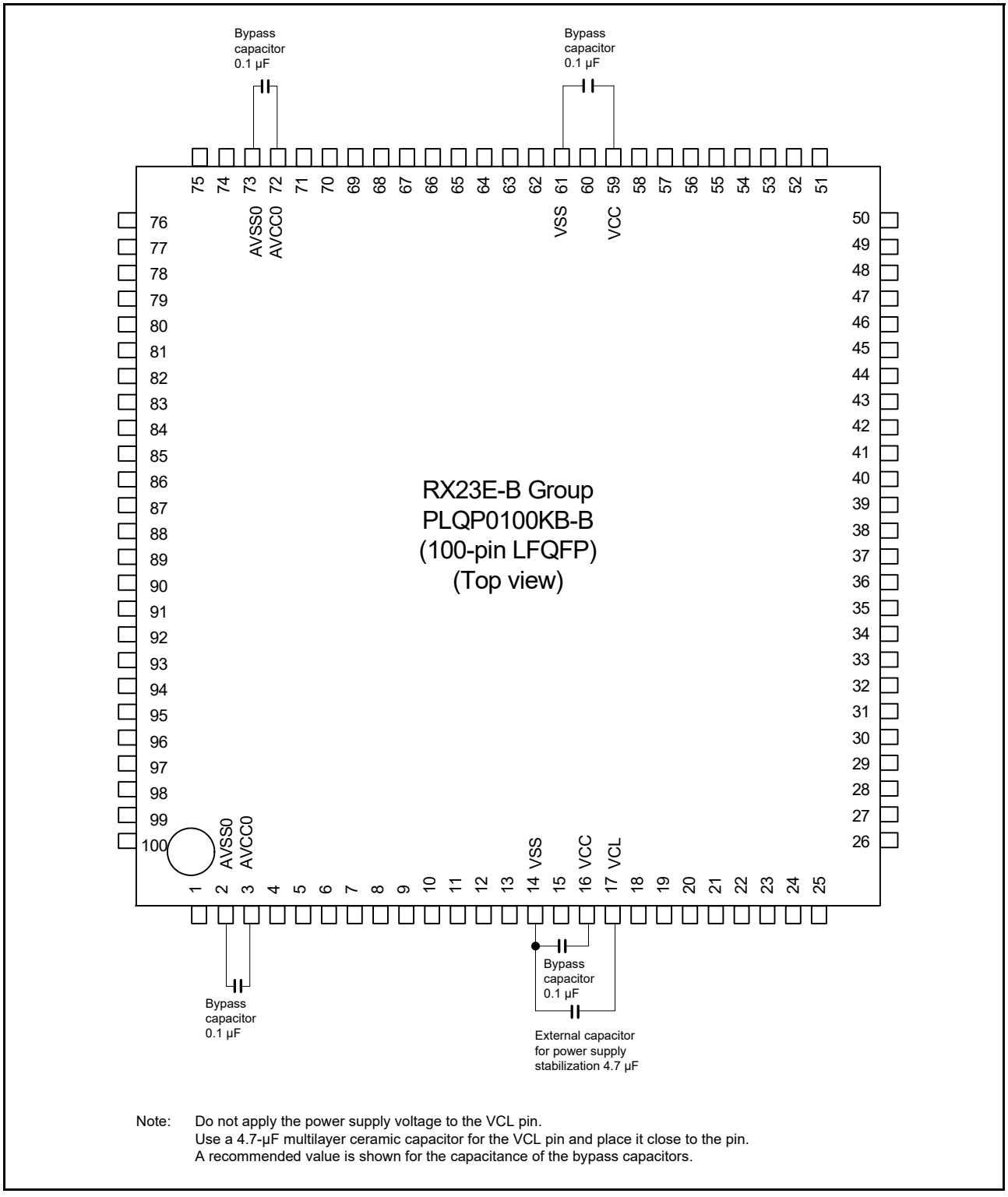


Figure 2.100 Temperature Dependence of Gain Error (AVCC0 = 5V, VREFH = 5V)

2.15 Usage Notes

2.15.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and the VSS pin. Figure 2.101 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin.
Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor as closer to the MCU power supply pins as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 35, Analog Front End (AFEA), and section 37, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note, the Hardware Design Guide (R01AN1411EJ). The latest version can be downloaded from the Renesas Electronics website.



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

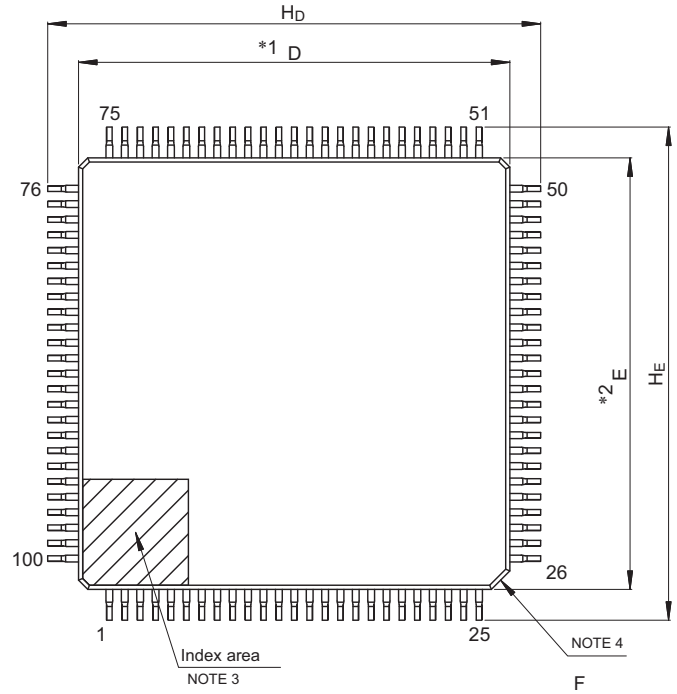
Figure 2.101 Connecting Capacitors (100 Pins)

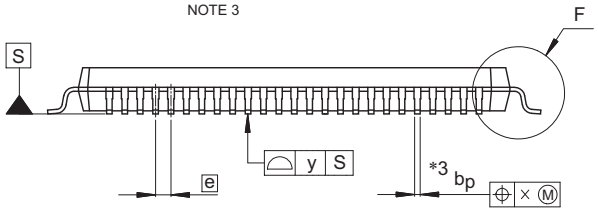
Appendix 1. Package Dimensions

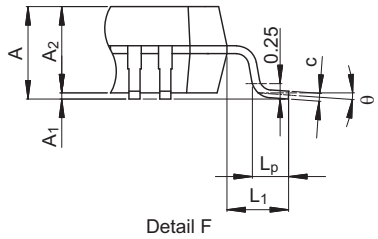
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm





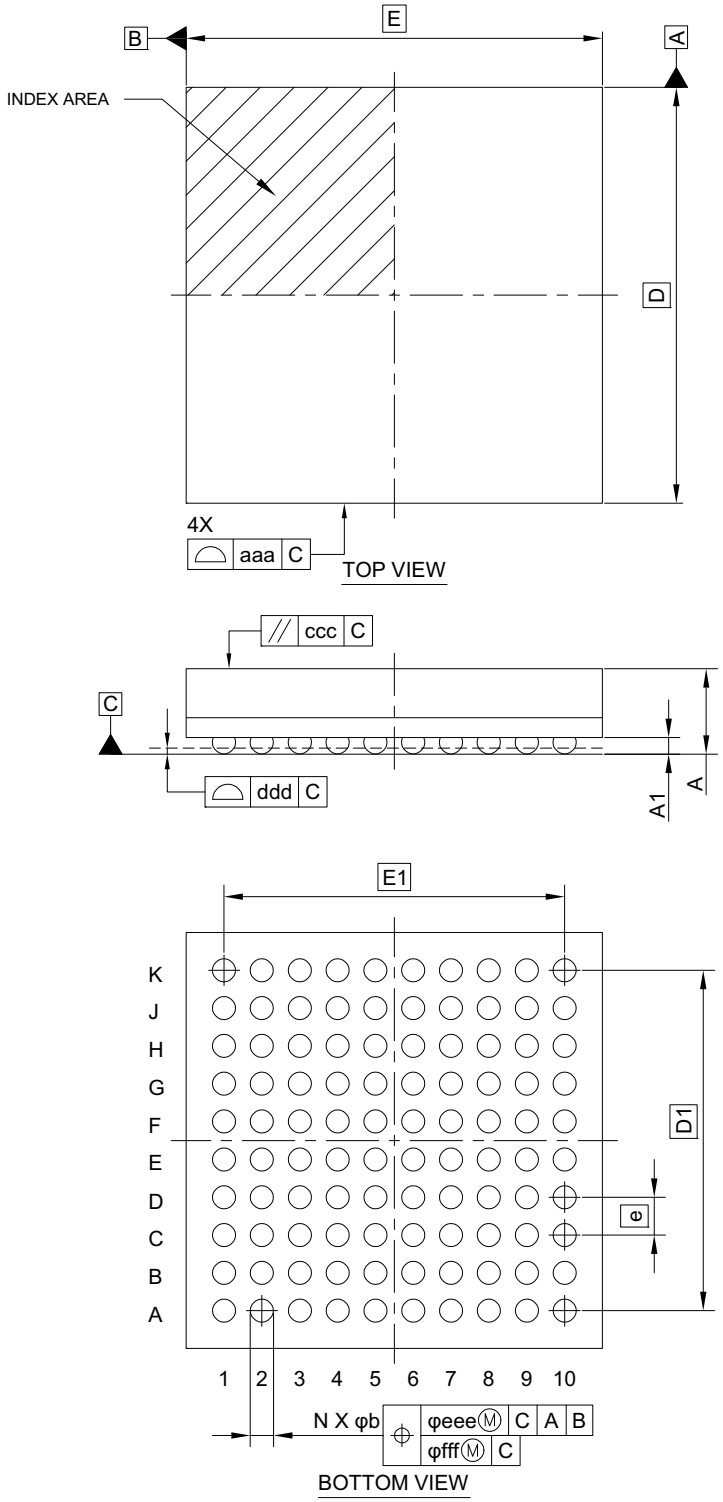


NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFBGA100-5.5x5.5-0.50	PTBG0100KD-A	0.07

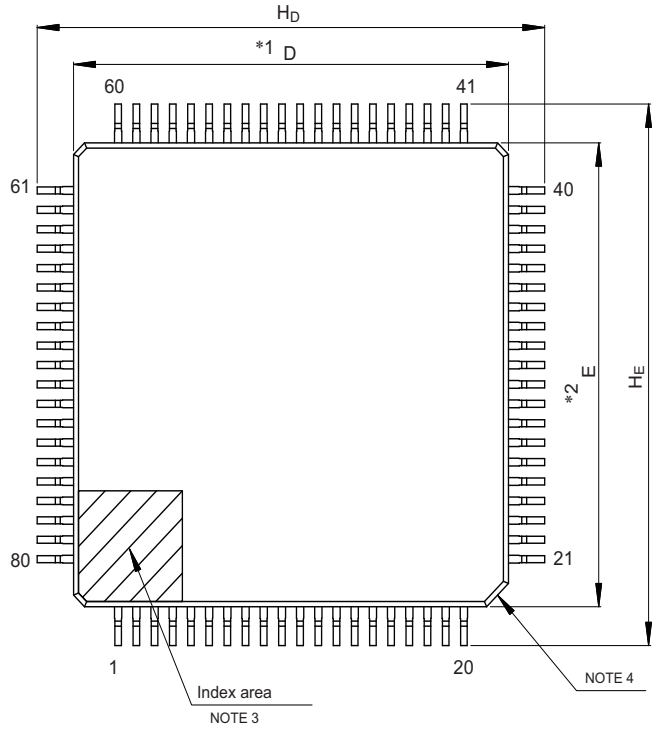


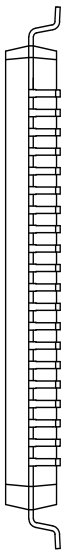
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	5.50	—
E	—	5.50	—
D1	—	4.50	—
E1	—	4.50	—
A	—	—	1.20
A1	0.17	—	—
b	0.26	0.31	0.36
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.05
N	—	100	—

Figure B 100-Pin TFBGA (PTBG0100KD-A)

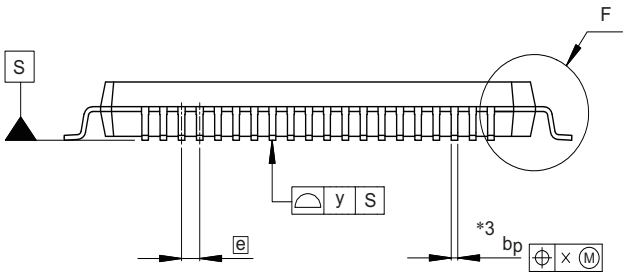
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

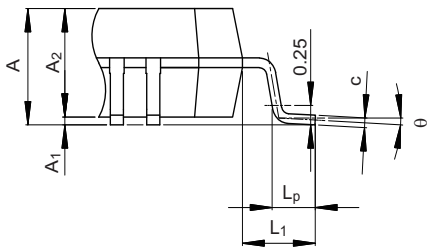
Unit: mm





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





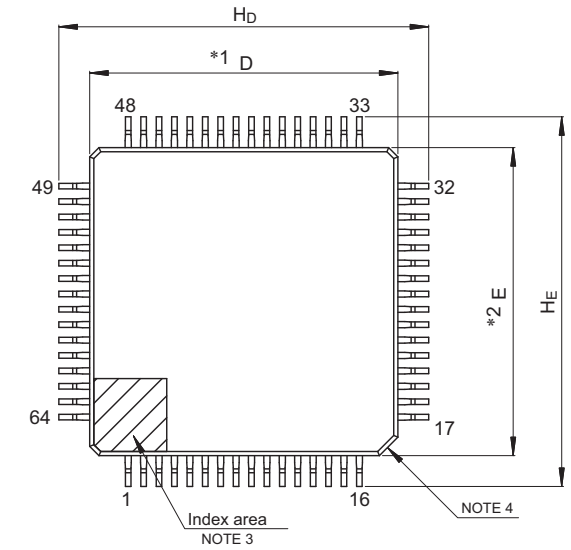
Detail F

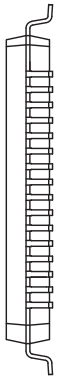
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

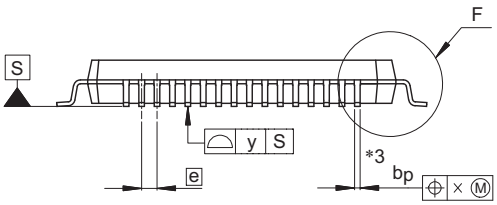
Figure C 80-Pin LFQFP (PLQP0080KB-B)

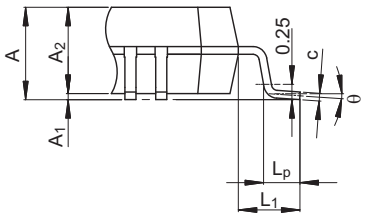
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm









Detail F

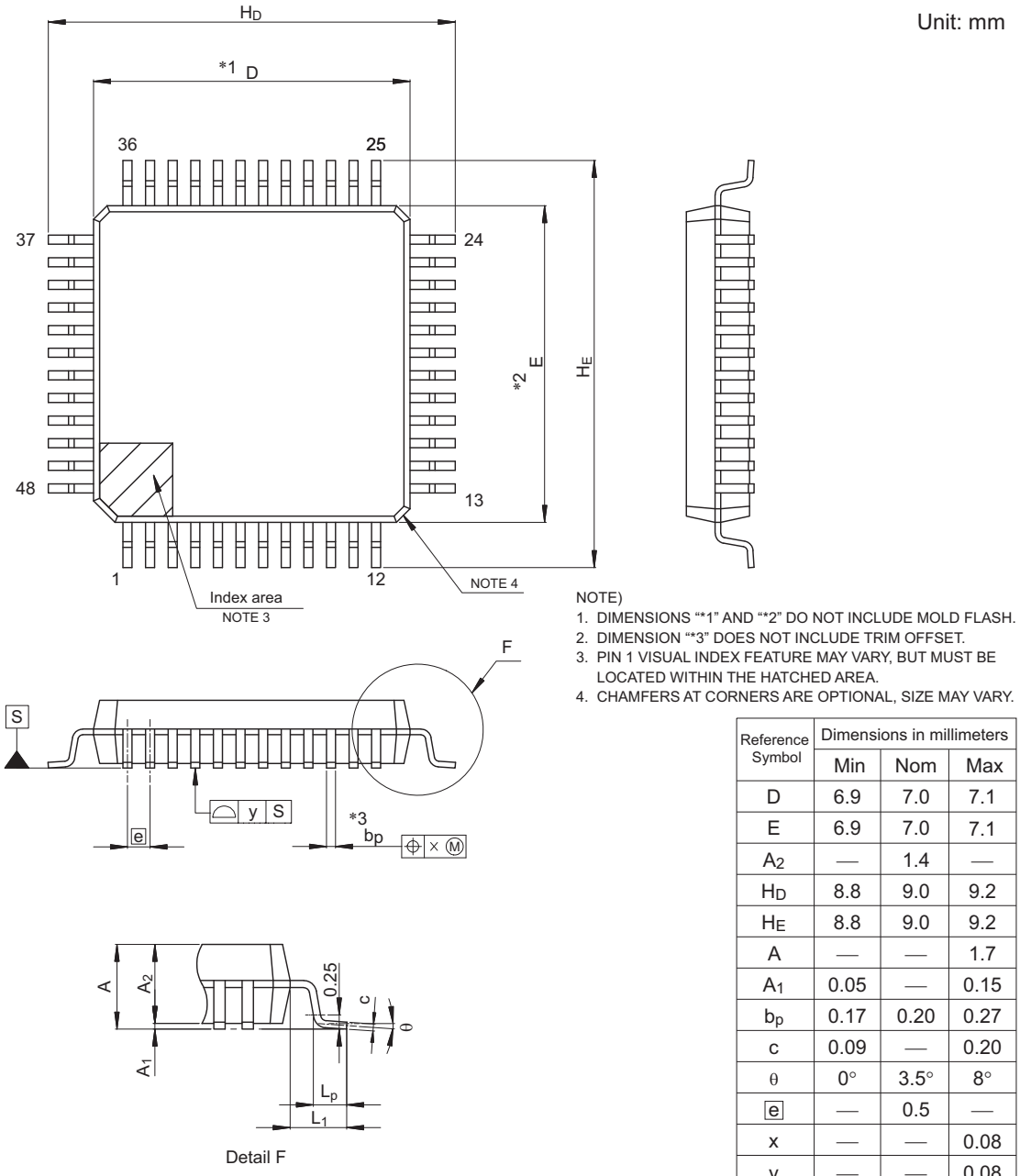
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure D 64-Pin LFQFP (PLQP0064KB-C)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm

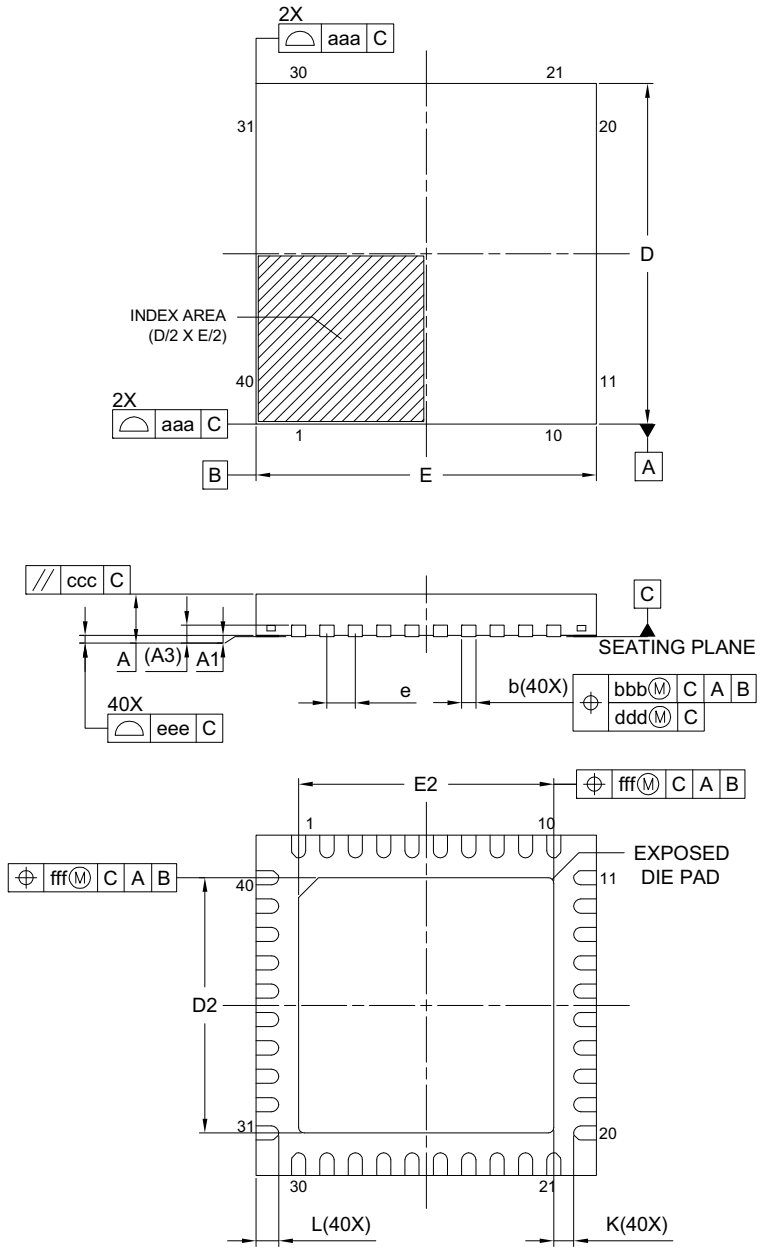


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure E 48-Pin LFQFP (PLQP0048KB-B)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN040-6x6-0.50	PWQN0040KD-A	0.08



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	4.45	4.50	4.55
E_2	4.45	4.50	4.55
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure F 40-Pin HWQFN (PWQN0040KD-A)

REVISION HISTORY	RX23E-B Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Aug 31, 2023	—	First edition, issued	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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