

RTP100E1P8G1FL-DSC

100V E-Mode GaN FET in FCLGA 3.3 × 3.3 mm Package

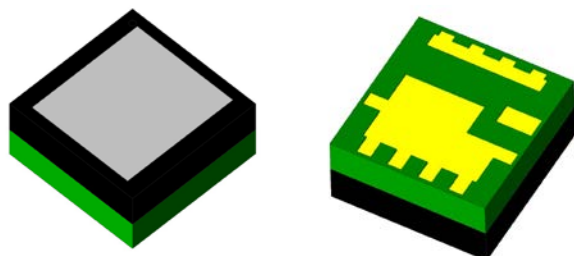
Description

The RTP100E1P8G1FL-DSC 100V, 1.8mΩ is an enhancement mode Gallium Nitride (GaN) FET in a 3.3 × 3.3 mm FCLGA dual-side cooled (DSC) package using Renesas' Gen 1 REXGAN® platform. Utilizing advanced packaging technology, these devices deliver high-speed switching and enhanced thermal performance. Designed with footprint compatibility to standard silicon counterparts, these devices simplify the transition to GaN technology.

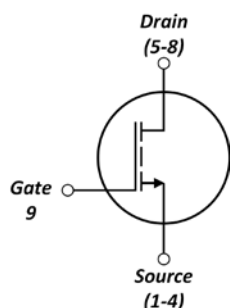
Benefits

- Facilitates cost-effective GaN adoption in Si compatible footprint reducing development time, and system size
- Enables high-efficiency, high power density, and reliable power conversion
- Enhanced thermal conductivity through larger contact area for improved heat spreading

Product Diagrams



RTP100E1P8G1FL-DSC



Symbol

Features

- Ultra-fast switching E-mode GaN HEMT
- JEDEC-qualified GaN technology
- Package footprint compatible to Si counterpart
- Dual-side cooled package simplifying thermal design
- Simplified thermal design
- Zero reverse recovery charge
- Low gate charge and output charge

Applications

- 48V IBC in telecom and AI datacenter
- Synchronous rectification and DC-DC converters
- Battery operated tools
- Class-D audio amplifier
- Energy storage systems
- 48V Servo drive
- Robotic systems

Specifications

V_{DS} (V)	100
$R_{DS(on)}$ (mΩ)	1.8
Q_{OSS} (nC)	50
Q_G (nC)	16.3
Q_{rr} (nC)	0

Contents

1. Pin Information	3
1.1 Pin Assignments	3
1.2 Pin Descriptions	3
2. Specifications	4
2.1 Absolute Maximum Ratings	4
2.2 Thermal Specifications	4
2.3 Electrical Specifications – Forward Device	5
2.4 Electrical Specifications – Reverse Conduction	5
3. Typical Performance Graphs	6
4. Package Outline Drawings	9
5. Packaging Specification	9
6. Related Information	10
7. Ordering Information	10
8. Revision History	10

Figures

Figure 1. Pin Assignments - Bottom View	3
Figure 2. Typical Output Characteristics, Parameter V_{GS}	6
Figure 3. Typical Transfer Characteristics, Parameter T_J	6
Figure 4. $R_{DS(on)}$ vs V_g , Parameter I_{DS}	6
Figure 5. $R_{DS(on)}$ vs V_g , Parameter T_J	6
Figure 6. Typical Capacitance Characteristics	7
Figure 7. Normalized $R_{DS(on)}$, Parameter T_J	7
Figure 8. Typical C_{oss} Stored Energy	7
Figure 9. Typical Q_{oss}	7
Figure 10. Gate Charge	8
Figure 11. Reverse Conduction Characteristics, Parameter T_J	8
Figure 12. Junction-Case Transient Thermal Response, Parameter $D=t_1/T$	8
Figure 13. Safe Operating Area (Single Pulse), Parameter $T_J = \text{Max Rated}$	8

1. Pin Information

1.1 Pin Assignments

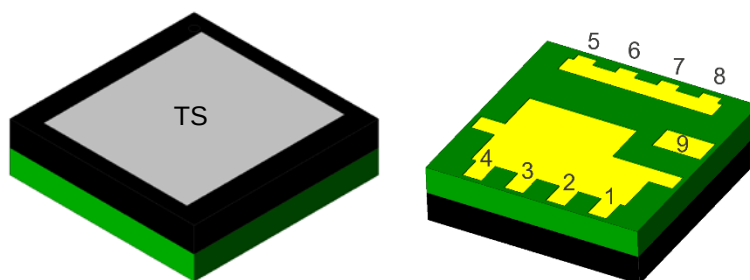


Figure 1. Pin Assignments - Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4	S	Source
5, 6, 7, 8	D	Drain
9	G	Gate
TS ^[1]	S	Source

1. TS Pin is the exposed die and is the silicon substrate that is internally connected to the source. It is not recommended to use it as an electrical connection

2. Specifications

2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DS}	Drain to source voltage	-	100	V
$V_{DS(TR), \text{repetitive}}$	Transient drain to source voltage, repetitive ^[1]	-	120	
$V_{GS(TR), \text{repetitive}}$	Transient gate to source voltage, repetitive ^[1]	-	+7	
V_{GS}	Gate to source voltage	-4	+6	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$	-	28	W
	Maximum power dissipation at $T_A = 25^\circ\text{C}$ [at $R_{\theta JA} = 25.7^\circ\text{C/W}$]	-	4.86	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$	-	101	A
	Continuous drain current at $T_A = 25^\circ\text{C}$ [at $R_{\theta JA} = 25.7^\circ\text{C/W}$]	-	38.7	A
I_{DM}	Pulsed drain current (pulse width: 10 μs) ^[2]	-	410	A
T_J	Junction operating temperature	-40	+150	$^\circ\text{C}$
T_S	Storage temperature	-40	+150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature	-	260	$^\circ\text{C}$

1. Pulsed repetitively, at Duty cycle factor (DC_{Factor}) $\leq 1\%$.
2. Defined by design. Not subject to production test.

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC(top)}$	Junction-to-case, Top	0.4	$^\circ\text{C/W}$
$R_{\theta JC(bottom)}$	Junction-to-case, Bottom	4.2	
$R_{\theta JA}$	Junction-to-ambient, 2s2p ^[1]	25.7	

1. $R_{\theta JA}$ determined with device on 4-layer PCB (with vias), under natural convection.

2.3 Electrical Specifications – Forward Device

$T_J = 25^\circ\text{C}$ unless otherwise stated ^[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Drain-Source Voltage Blocking	$V_{GS} = 0V$	100	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 10mA$	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-source on-resistance	$V_{GS} = 5V$, $I_D = 30A$, $T_J = 25^\circ\text{C}$	-	1.8	2.4	m Ω
I_{DSS}	Drain-to-source leakage current	$V_{DS} = 80V$, $V_{GS} = 0V$, $T_J = 25^\circ\text{C}$	-	10	200	μA
I_{GSS}	Gate-to-source forward leakage current	$V_{GS} = 5V$	-	30	2900	μA
	Gate-to-source reverse leakage current	$V_{GS} = -4V$	-	0.2	-	
C_{ISS}	Input capacitance	$V_{GS} = 0V$, $V_{DS} = 50V$, $f = 100kHz$	-	2147	-	pF
C_{OSS}	Output capacitance		-	606	-	
C_{RSS}	Reverse transfer capacitance		-	12	-	
$C_{O(er)}$	Output capacitance, energy related ^[2]	$V_{GS} = 0V$, $V_{DS} = 0V$ to $50V$	-	872	-	pF
$C_{O(tr)}$	Output capacitance, time related ^[3]		-	1000	-	
Q_G	Total gate charge	$V_{DS} = 50V$, $V_{GS} = 0V$ to $5V$, $I_D = 30A$	-	16.3	-	nC
Q_{GS}	Gate-source charge		-	4.9	-	
Q_{GD}	Gate-drain charge		-	2.4	-	
$Q_{G(th)}$	Gate Charge at threshold		-	3.8	-	
Q_{OSS}	Output charge	$V_{GS} = 0V$, $V_{DS} = 0V$ to $50V$	-	50	-	nC

- Parameters for which only a typical value is provided are defined by design and may not be subject to production test.
- Equivalent capacitance to give same stored energy from 0V to 50V.
- Equivalent capacitance to give same charging time from 0V to 50V.

2.4 Electrical Specifications – Reverse Conduction

$T_J = 25^\circ\text{C}$ unless otherwise stated ^[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{SD}	Reverse voltage	$V_{GS} = 0V$, $I_{SD} = 0.5A$	-	1.4	-	V
Q_{RR}	Source-Drain Recovery Charge	-	-	0	-	nC

- Parameters for which only a typical value is provided are defined by design and may not be subject to production test.

3. Typical Performance Graphs

$T_J = 25^\circ\text{C}$ unless otherwise stated.

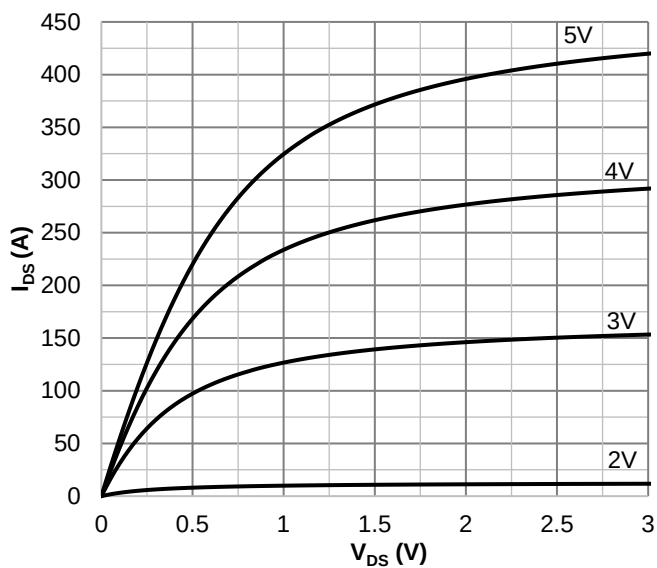


Figure 2. Typical Output Characteristics, Parameter V_{GS}

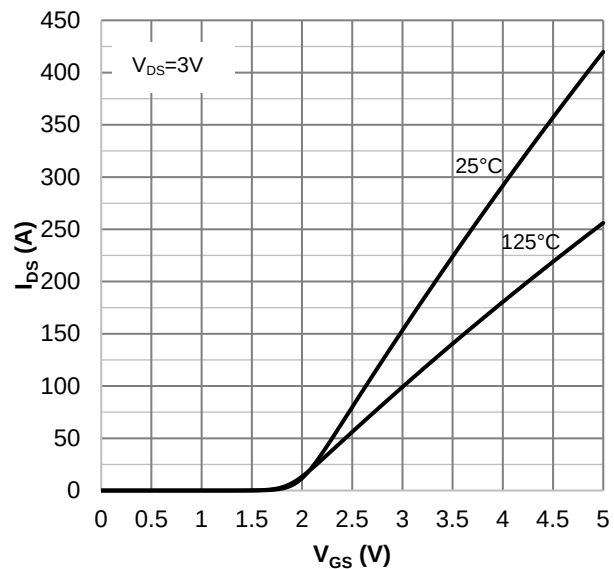


Figure 3. Typical Transfer Characteristics, Parameter T_J

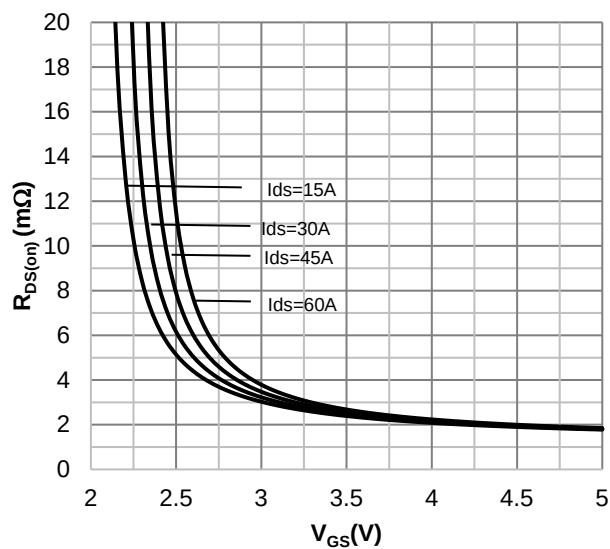


Figure 4. $R_{DS(on)}$ vs V_G , Parameter I_{DS}

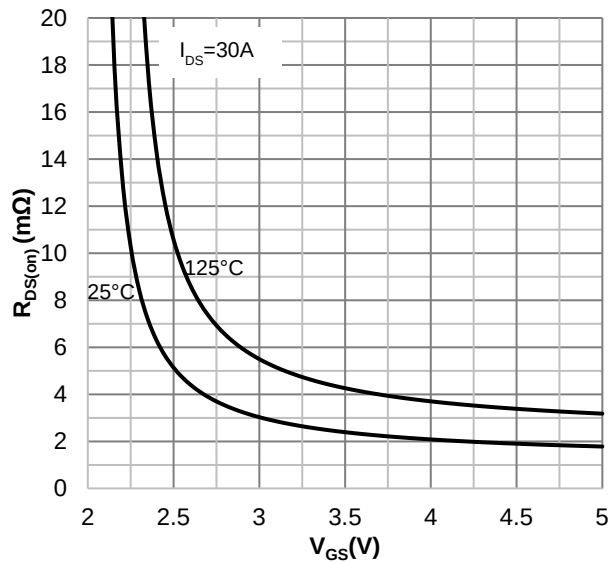


Figure 5. $R_{DS(on)}$ vs V_G , Parameter T_J

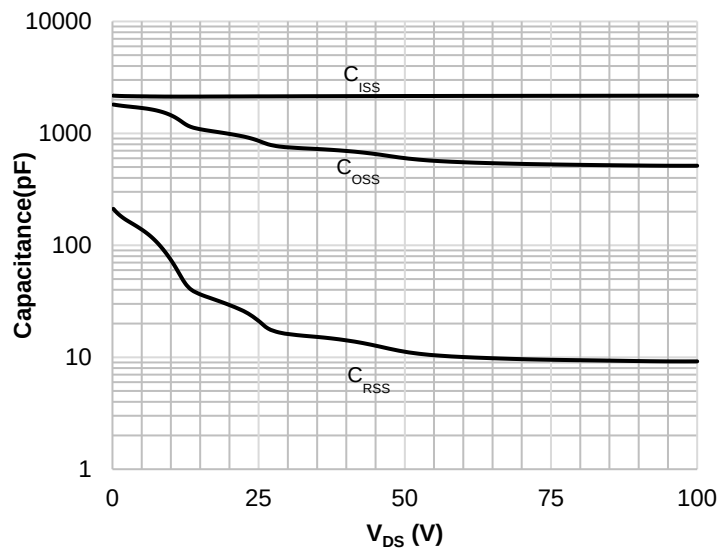
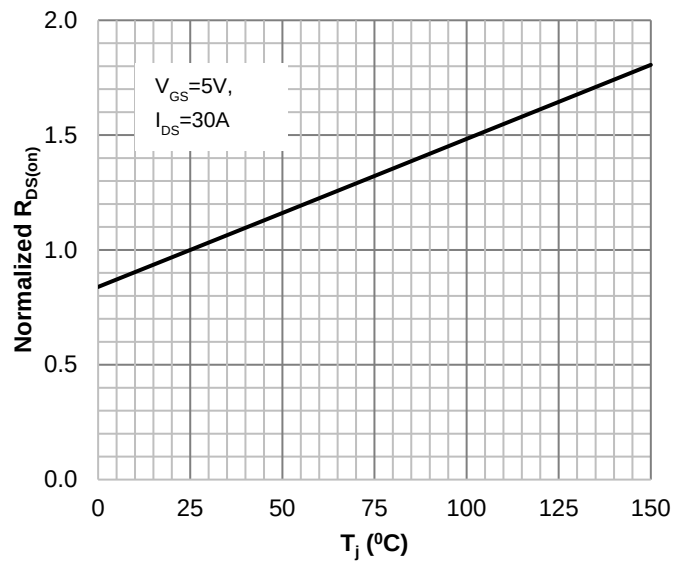
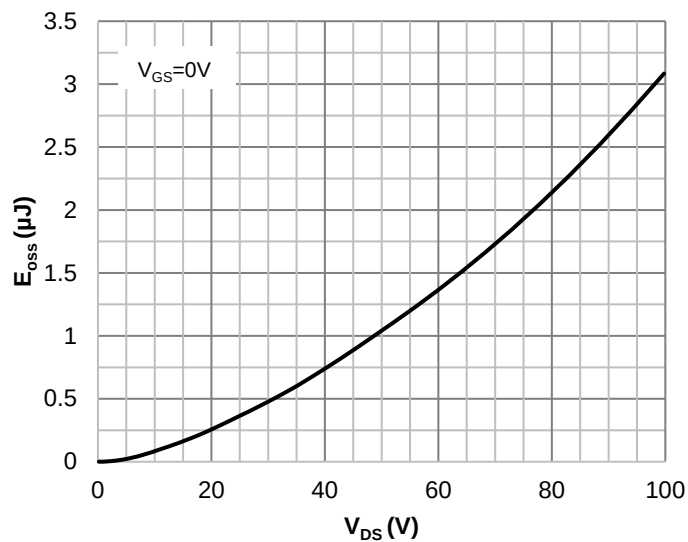
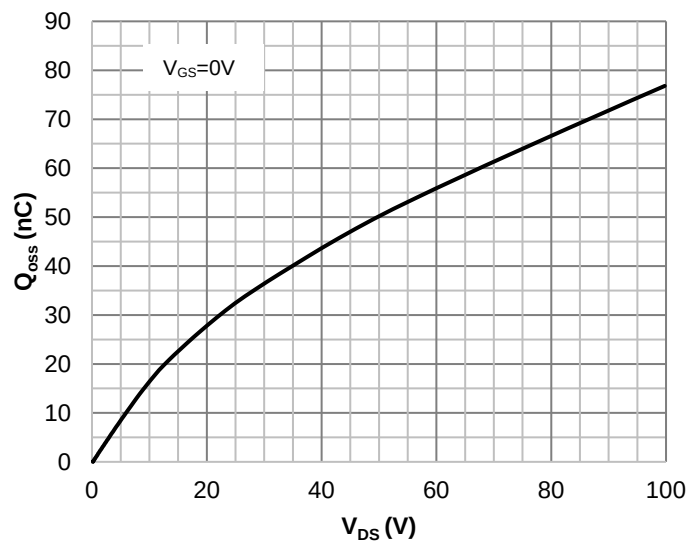


Figure 6. Typical Capacitance Characteristics


Figure 7. Normalized $R_{DS(on)}$, Parameter T_J

Figure 8. Typical C_{OSS} Stored Energy

Figure 9. Typical Q_{OSS}

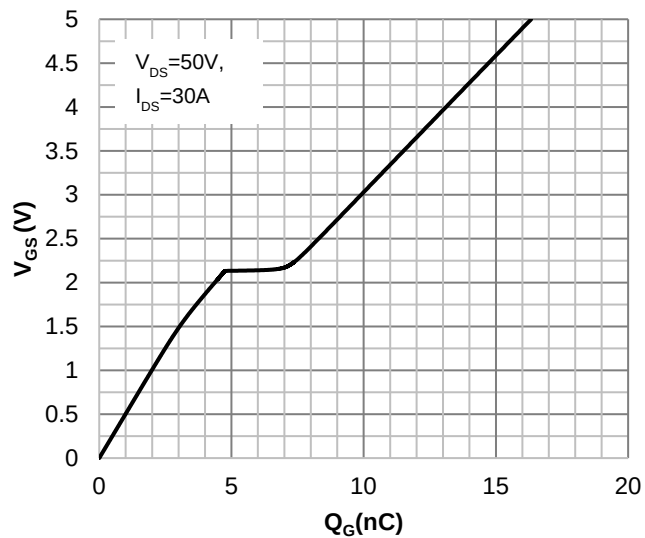
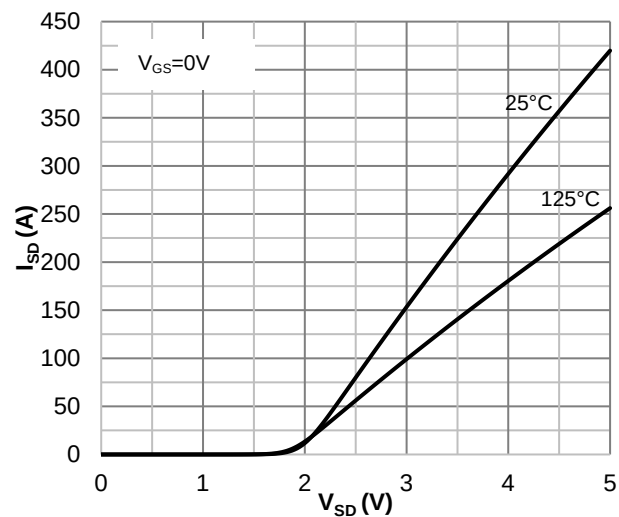
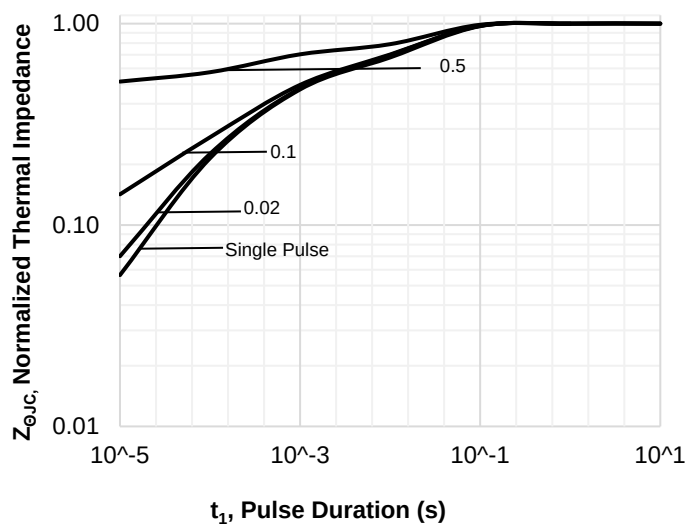
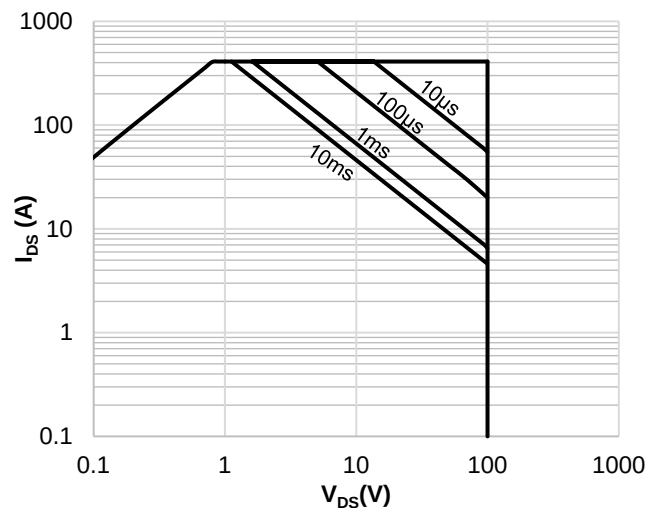


Figure 10. Gate Charge

Figure 11. Reverse Conduction Characteristics,
Parameter T_J Figure 12. Junction-Case Transient Thermal Response,
Parameter $D=t_1/T$ Figure 13. Safe Operating Area (Single Pulse),
Parameter $T_J = \text{Max Rated}$

4. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

5. Packaging Specification



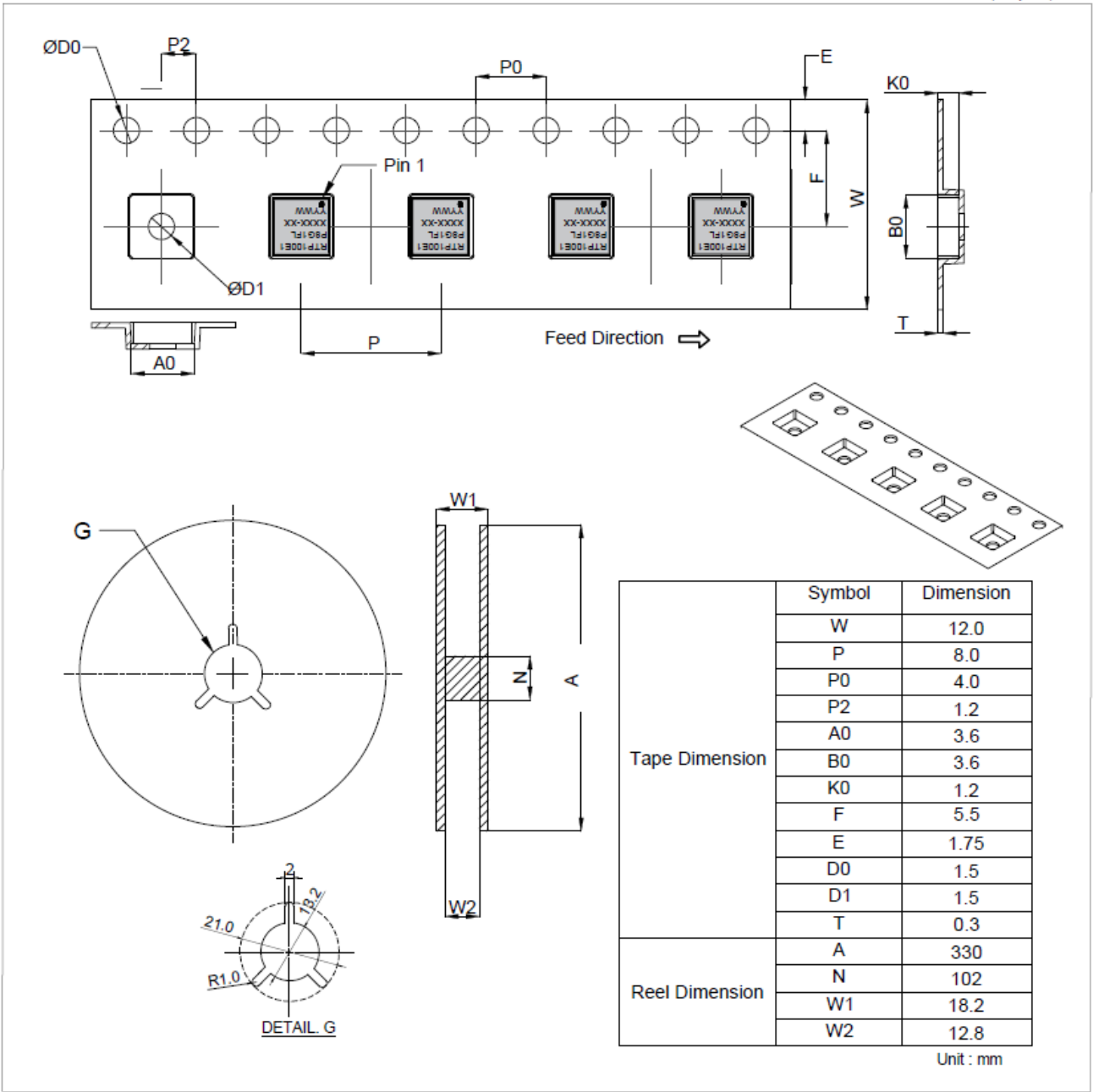
Package Specification

PSC-5170-01

FL0009AA

9-FLIP CHIP 3.3x 3.3 x 0.902 mm Body, 0.650mm Pitch (ePad: 1.975 x 3.750 mm)

Rev00, Sep 21, 2026



© Renesas Electronics Corporation

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the [GaN Power Solutions](#) page.

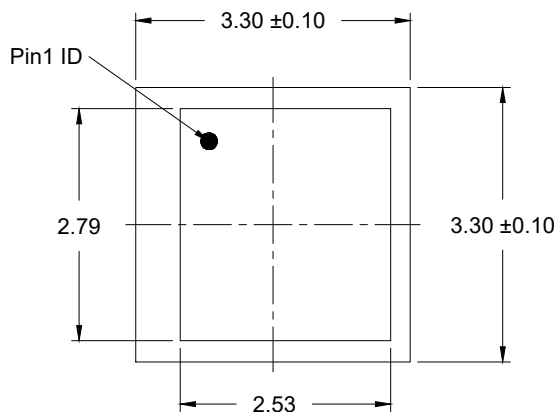
- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

7. Ordering Information

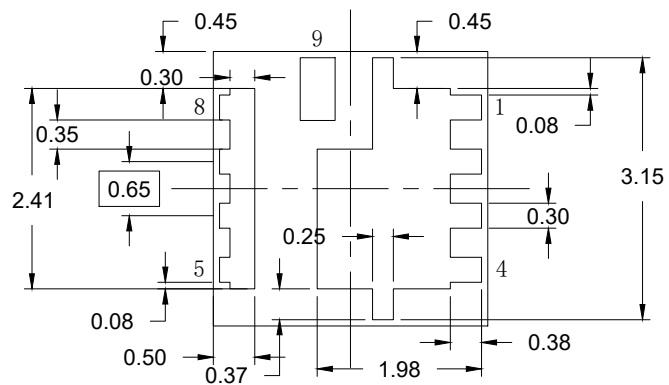
Part Number	Package Description	Carrier Type	Package Configuration
RTP100E1P8G1FL-DSC-TR	9-Flip Chip , 3.3 × 3.3 × 0.902 mm Body	Taping	3000pcs/reel

8. Revision History

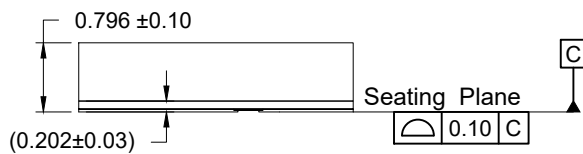
Revision	Date	Description
1.00	Sep 29, 2026	Initial Release



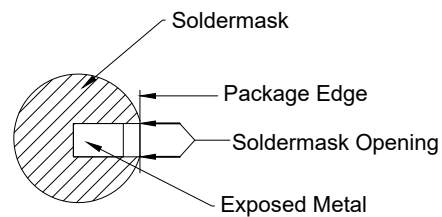
TOP VIEW



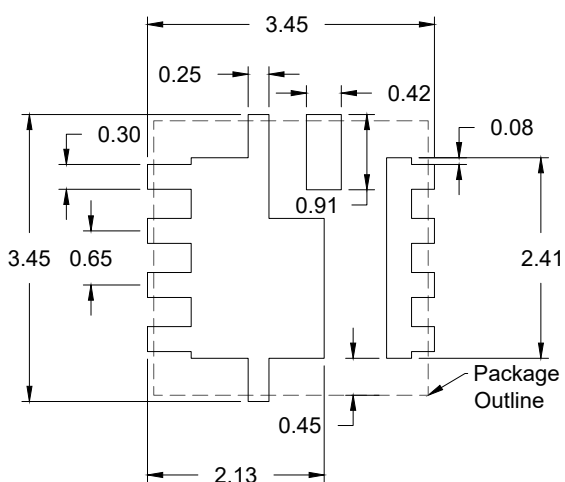
BOTTOM VIEW



SIDE VIEW



Detail A



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.