

RTP100E1P2G1FL-DSC

100V E-Mode GaN FET in FCLGA 5 × 6 mm Package

Description

The RTP100E1P2G1FL-DSC 100V, 1.2mΩ is an enhancement mode Gallium Nitride (GaN) FET in a 5 × 6 mm FCLGA dual-side cooled (DSC) package using Renesas' Gen 1 REXGAN® platform. Utilizing advanced packaging technology, these devices deliver high-speed switching and enhanced thermal performance. Designed with footprint compatibility to standard silicon counterparts, these devices simplify the transition to GaN technology.

Benefits

- Facilitates cost-effective GaN adoption in Si compatible footprint reducing development time, and system size
- Enables high-efficiency, high power density, and reliable power conversion
- Enhanced thermal conductivity through larger contact area for improved heat spreading

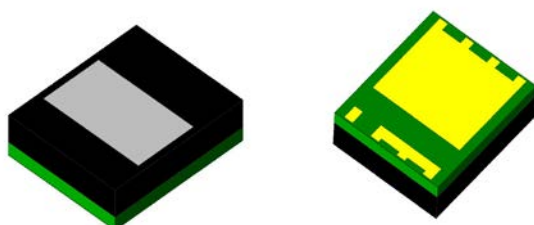
Features

- Ultra-fast switching E-mode GaN HEMT
- JEDEC-qualified GaN technology
- Package footprint compatible to Si counterpart
- Dual-side cooled package simplifying thermal design
- Zero reverse recovery charge
- Low gate charge and output charge

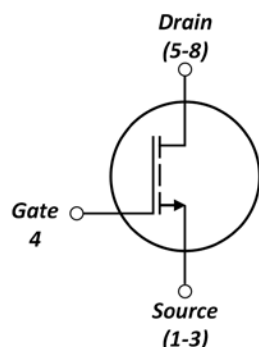
Applications

- 48V IBC in telecom and AI datacenter
- Synchronous rectification and DC-DC converters
- Battery operated tools
- Class-D audio amplifier
- Energy storage systems
- 48V Servo drive
- Robotic systems

Product Diagrams



RTP100E1P2G1FL-DSC



Symbol

Specifications

V_{DS} (V)	100
$R_{DS(on)}$ (mΩ)	1.2
Q_{OSS} (nC)	86
Q_G (nC)	27
Q_{rr} (nC)	0

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1. Pin Information

1.1 Pin Assignments

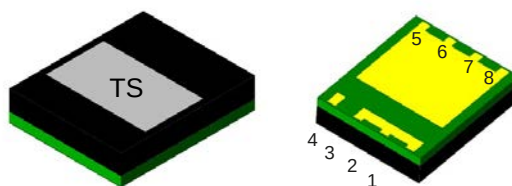


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3	S	Source
5, 6, 7, 8	D	Drain
4	G	Gate
TS ^[1]	S	Source

1. TS Pin is the exposed die and is the silicon substrate that is internally connected to the source. It is not recommended to use it as an electrical connection.

2. Specifications

2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage	-	100	V
$V_{DSS(TR), \text{repetitive}}$	Transient drain to source voltage, repetitive ^[1]	-	120	
$V_{GSS(TR), \text{repetitive}}$	Transient gate to source voltage, repetitive ^[1]	-	+7	
V_{GSS}	Gate to source voltage	-4	+6	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$	-	50	W
	Maximum power dissipation at $T_A = 25^\circ\text{C}$ [at $R_{\theta JA} = 20.7^\circ\text{C/W}$]	-	6.03	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$	-	133	A
	Continuous drain current at $T_A = 25^\circ\text{C}$ [at $R_{\theta JA} = 20.7^\circ\text{C/W}$]	-	52	A
I_{DM}	Pulsed drain current (pulse width: 10 μs) ^[2]	-	697	A
T_J	Junction operating temperature	-40	+150	$^\circ\text{C}$
T_S	Storage temperature	-40	+150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature	-	260	$^\circ\text{C}$

1. Pulsed repetitively, at Duty cycle factor (DCFactor) < 1%.
2. Defined by design. Not subject to production test.

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC(top)}$	Junction-to-case, Top	0.28	$^\circ\text{C/W}$
$R_{\theta JC(bottom)}$	Junction-to-case, Bottom	2.5	
$R_{\theta JA}$	Junction-to-ambient, 2s2p ^[1]	20.7	

1. $R_{\theta JA}$ determined with device on 4-layer PCB (with vias), under natural convection.

2.3 Electrical Specifications – Forward Device

$T_J = 25^\circ\text{C}$ unless otherwise stated ^[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Drain-source Voltage Blocking	$V_{GS} = 0V$	100	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 18mA$	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-source on-resistance	$V_{GS} = 5V, I_D = 50A,$ $T_J = 25^\circ\text{C}$	-	1.2	1.6	m Ω
I_{DSS}	Drain-to-source leakage current	$V_{DS} = 80V, V_{GS} = 0V,$ $T_J = 25^\circ\text{C}$	-	15	150	μA
I_{GSS}	Gate-to-source forward leakage current	$V_{GS} = 5V$	-	40	4000	μA
	Gate-to-source reverse leakage current	$V_{GS} = -4V$	-	3	-	
C_{ISS}	Input capacitance	$V_{GS} = 0V, V_{DS} = 50V,$ $f = 100kHz$	-	3666	-	pF
C_{OSS}	Output capacitance		-	950	-	
C_{RSS}	Reverse transfer capacitance		-	9.5	-	
$C_{O(er)}$	Output capacitance, energy related ^[2]	$V_{GS} = 0V,$ $V_{DS} = 0V \text{ to } 50V$	-	1368	-	pF
$C_{O(tr)}$	Output capacitance, time related ^[3]		-	1720	-	
Q_G	Total gate charge	$V_{DS} = 50V, V_{GS} = 0V \text{ to } 5V,$ $I_D = 50A$	-	27	-	nC
Q_{GS}	Gate-source charge		-	8.2	-	
Q_{GD}	Gate-drain charge		-	3.7	-	
$Q_{G(th)}$	Gate charge at threshold		-	5.8	-	
Q_{OSS}	Output charge	$V_{GS} = 0V,$ $V_{DS} = 0V \text{ to } 50V$	-	86	-	nC

- Parameters for which only a typical value is provided are defined by design. Not subject to production test.
- Equivalent capacitance to give same stored energy from 0V to 50V.
- Equivalent capacitance to give same charging time from 0V to 50V.

2.4 Electrical Specifications – Reverse Conduction

$T_J = 25^\circ\text{C}$ unless otherwise stated ^[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{SD}	Reverse voltage	$V_{GS} = 0V, I_{SD} = 0.5A$	-	1.6	-	V
Q_{RR}	Source-Drain Recovery Charge	-	-	0	-	nC

- Parameters for which only a typical value is provided are defined by design. Not subject to production test.

3. Typical Performance Graphs

$T_J = 25^\circ\text{C}$ unless otherwise stated.

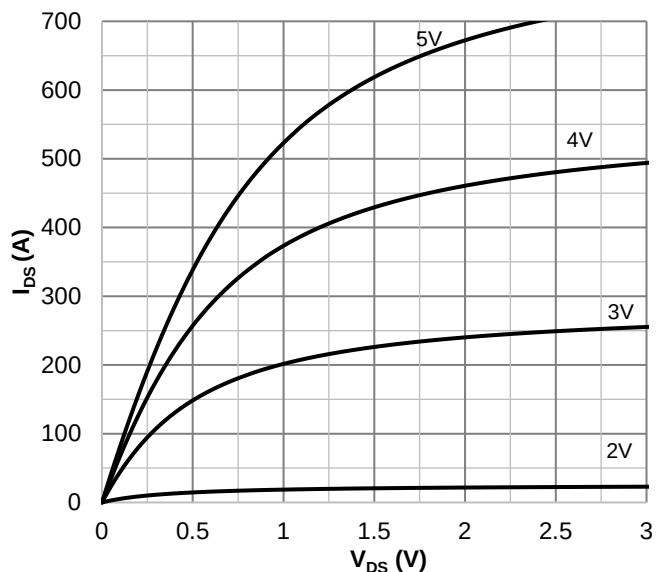


Figure 2. Typical Output Characteristics, Parameter V_{GS}

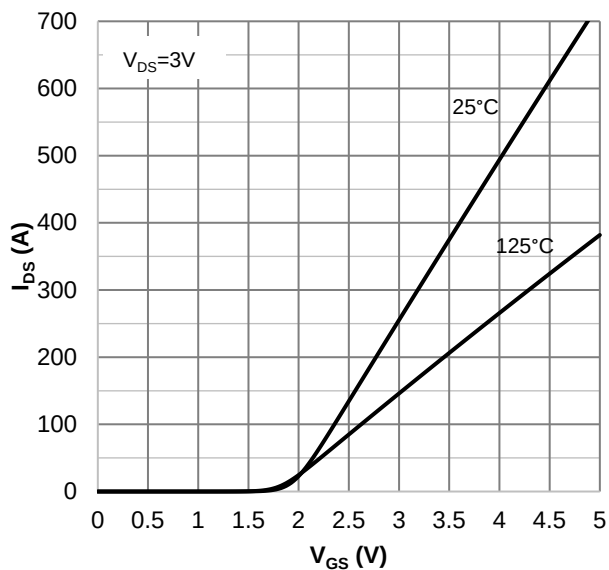


Figure 3. Typical Output Characteristics, Parameter T_J

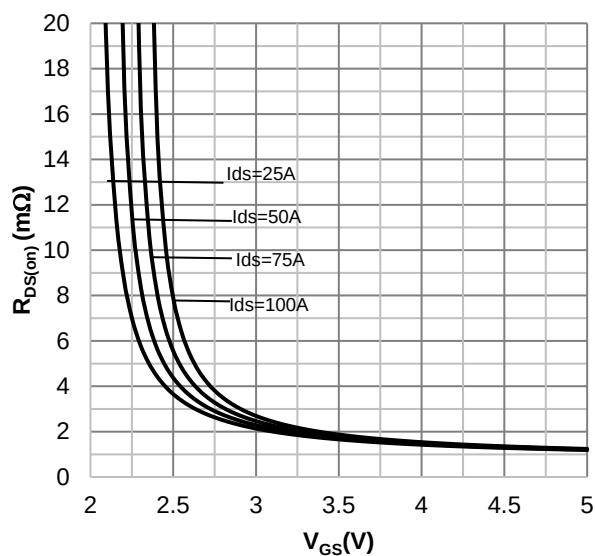


Figure 4. $R_{DS(on)}$ vs V_G , Parameter I_{DS}

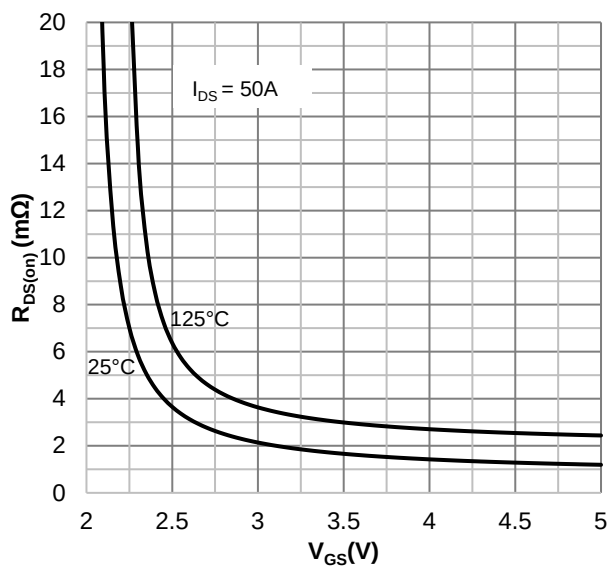


Figure 5. $R_{DS(on)}$ vs V_G , Parameter T_J

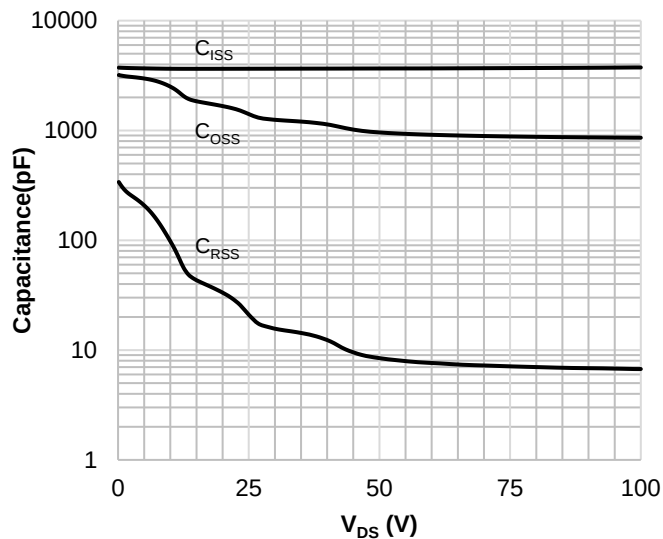
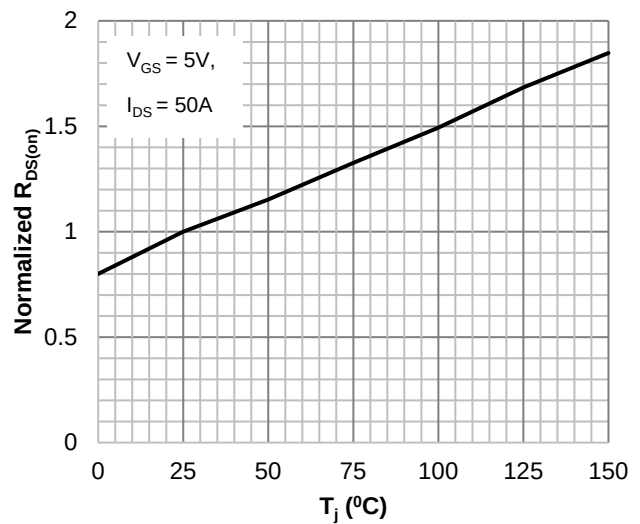
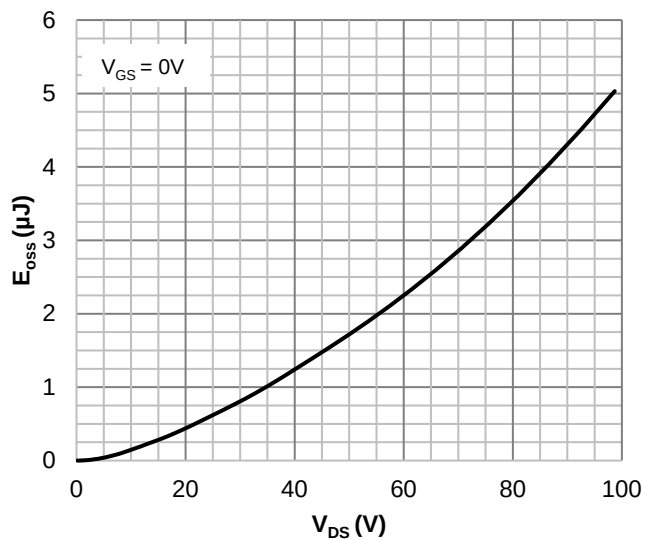
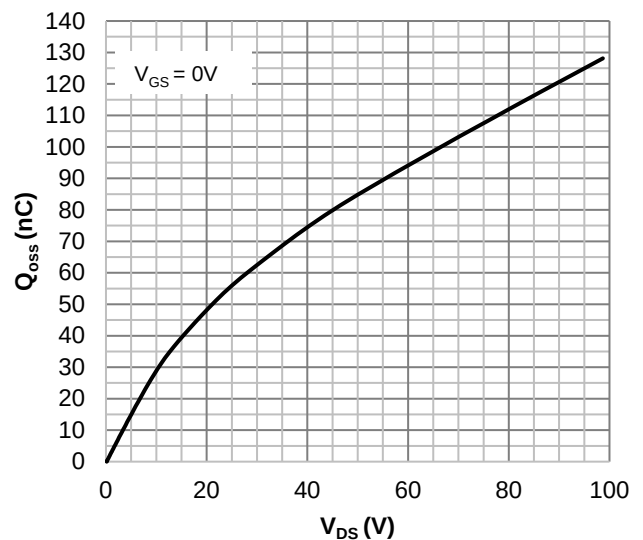


Figure 6. Typical Capacitance Characteristics

Figure 7. Normalized $R_{DS(on)}$, Parameter T_J Figure 8. Typical C_{oss} Stored EnergyFigure 9. Typical Q_{oss}

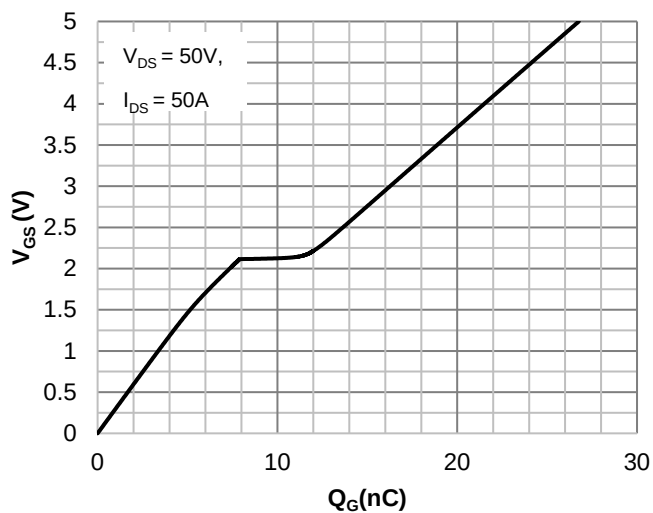


Figure 10. Gate Charge

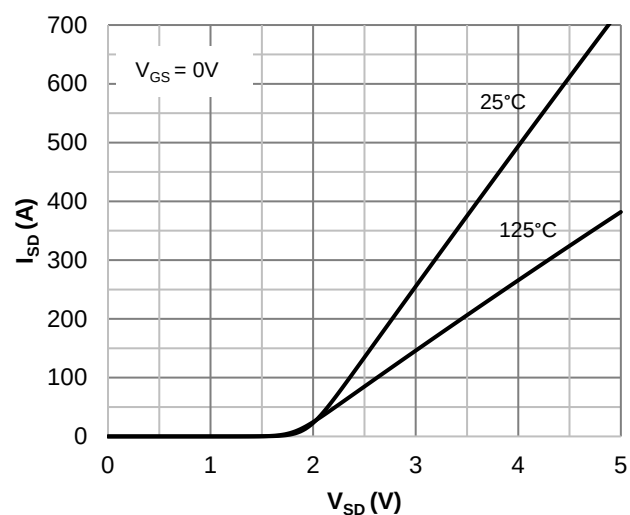
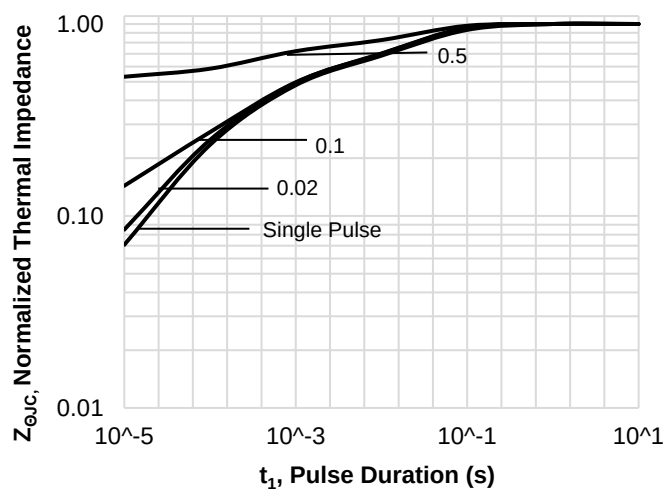
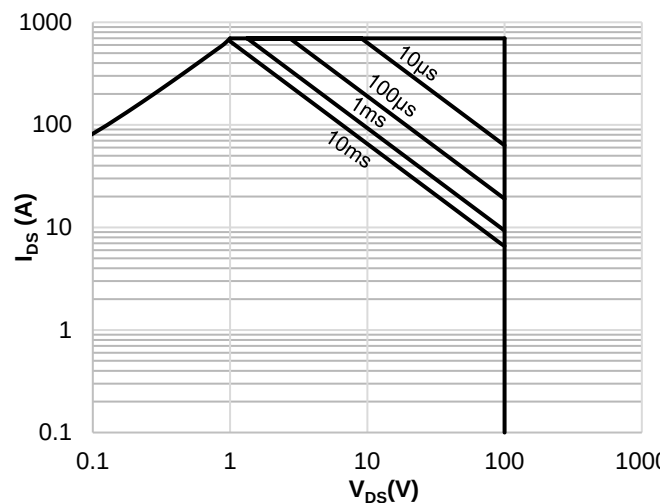
Figure 11. Reverse Conduction Characteristics, Parameter T_J Figure 12. Junction-Case Transient Thermal Response, Parameter $D = t_1/T$ 

Figure 13. Transient Thermal Resistance

4. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

5. Packaging Specification



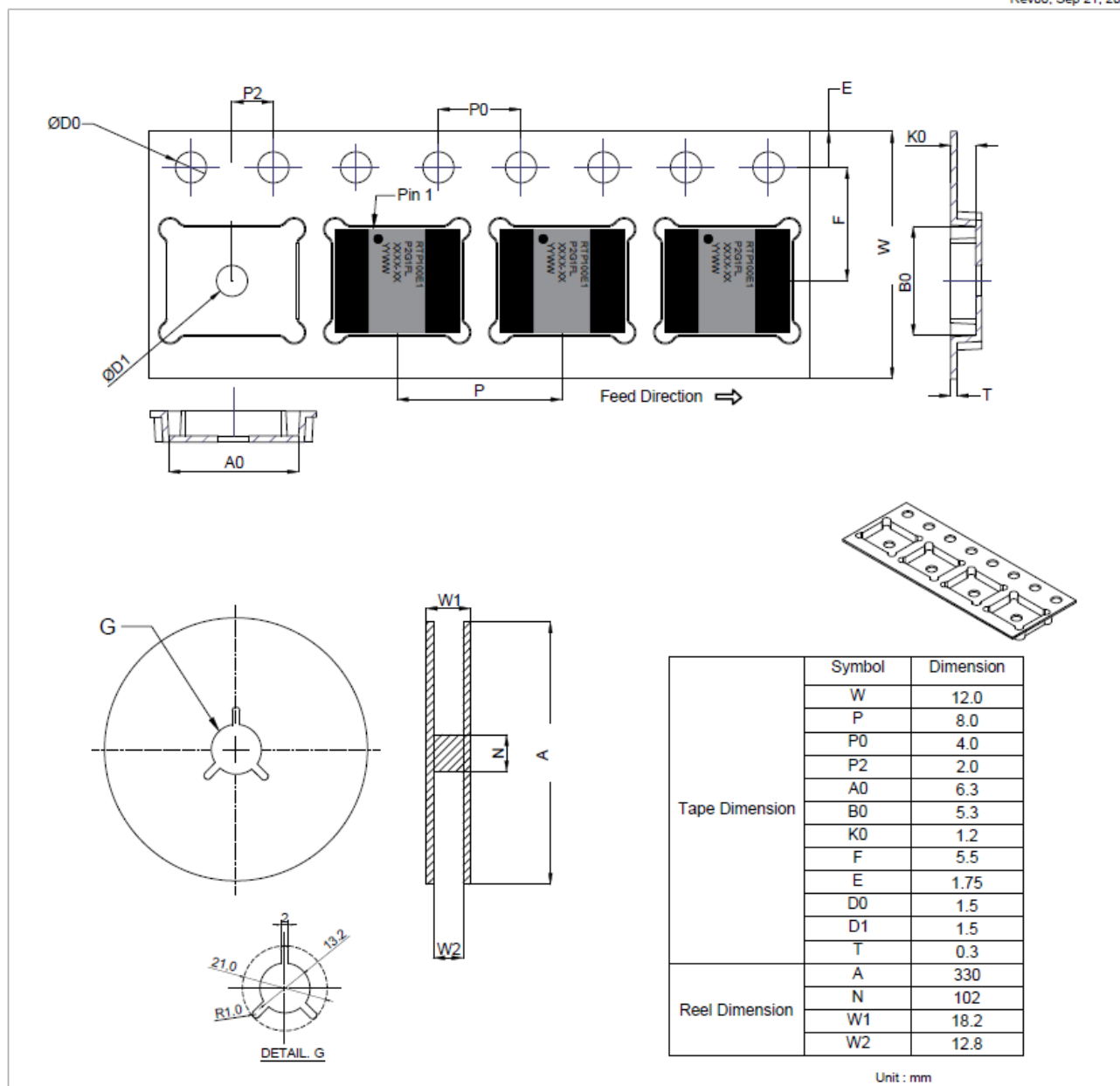
Packaging Specification

PSC-XXXX-01

FL000XAA

8-FLIP CHIP 5.0 x 6.0 x 0.702 mm Body, 1.270mm Pitch (ePad: 4.105 x 4.210 mm)

Rev00, Sep 21, 2026



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6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the [GaN Power Solutions](#) page.

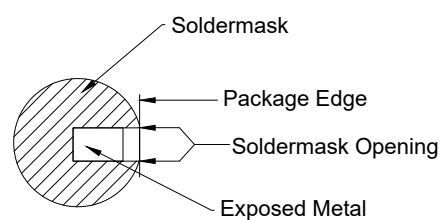
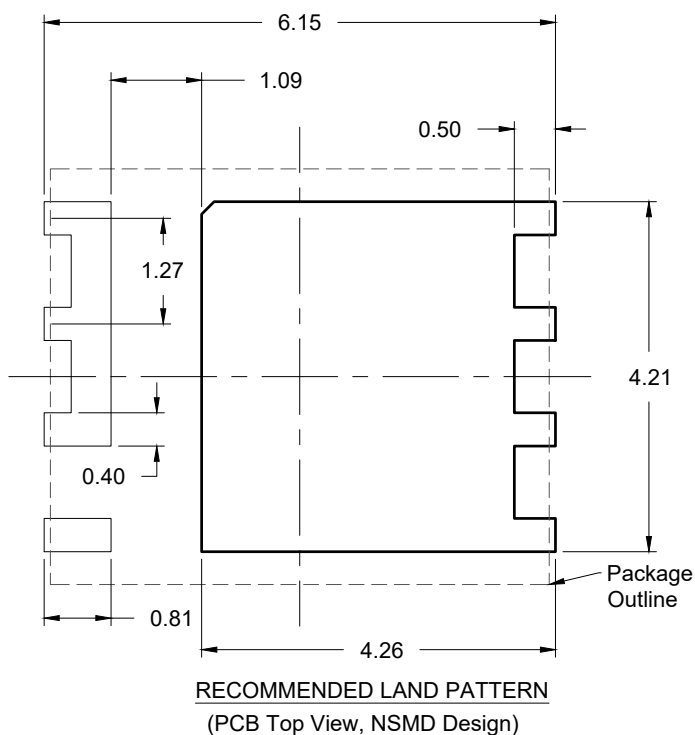
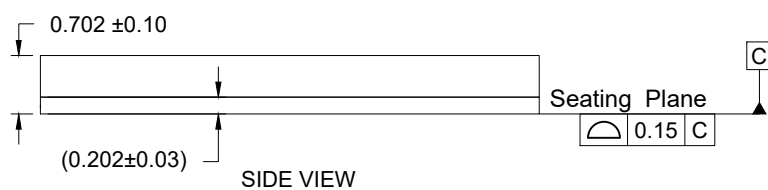
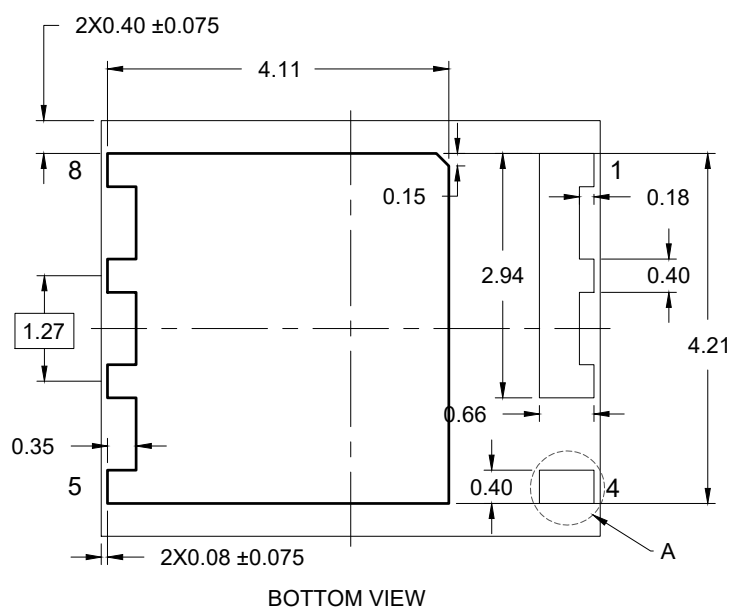
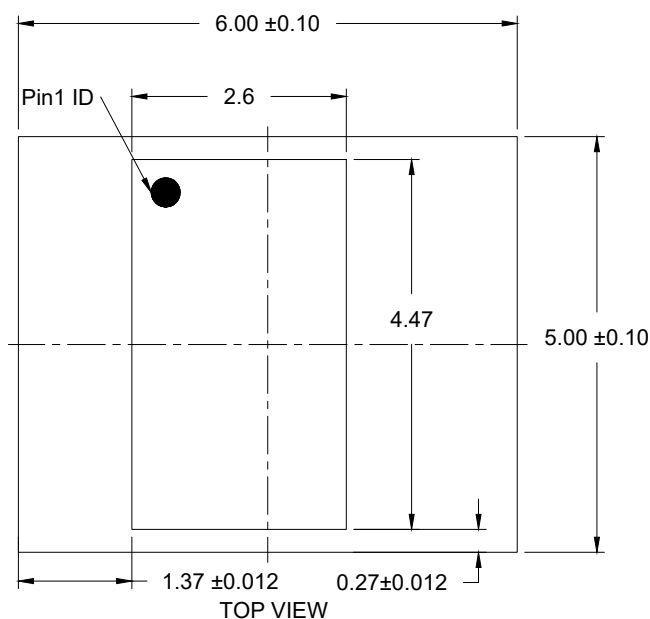
- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

7. Ordering Information

Part Number	Package Description	Carrier Type	Package Configuration
RTP100E1P2G1FL-DSC-TR	8-Flip Chip , 5.0 × 6.0 × 0.902 mm Body	Taping	3000pcs/reel

8. Revision History

Revision	Date	Description
1.00	Sep 29, 2026	Initial release.



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

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