RRP63175

5V, 7.2A Source, 5.3A Sink, High Frequency GaN/MOSFET Single Low-Side Driver

Description

The RRP63175 is a 5V, 7.2A source, 5.3A sink high frequency enhance mode GaN or logic level gate MOSFET single low-side driver. The RRP63175 accepts 3.3V/5V logic level PWM inputs.

The driver features a fast 5ns typical propagation delay, making it optimal for high-frequency switching applications. The RRP63175 can operate up to 30MHz.

The RRP63175 has split-gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently.

The driver features VDD UVLO that protects against undervoltage operation and over-temperature protection (OTP) in the event of overload and fault condition.

The RRP63175 is offered in a SCTDFN-6L (2mm×2mm) package with wettable flanks.

Features

- Accepts 3.3V/5V logic level PWM inputs
- 7.2A source and 5.3A sink driver for GaN/MOSFET
- Separately adjusts turn-on and turn-off speed
- Supports positive, negative PWM or EN input logic
- Fast propagation delay: 5ns typical delay
- 7ns minimum input pulse width
- 4ns typical rise and fall time
- 5V power supply
- V_{DD} undervoltage lockout (UVLO) and over-temperature protection (OTP)
- Small package with low parasitic inductance supporting up to 30MHz switching frequency application
- Low power consumption
- 2mm×2mm SCTDFN package

Applications

- GaN/MOSFET synchronous rectifier
- Power modules
- DC/DC converter

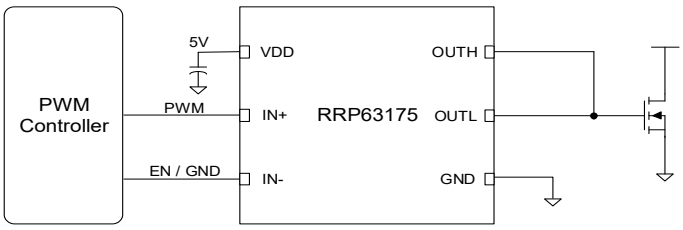


Figure 1. Low-Side Driver Typical Application

Contents

1. Overview

1.1 Block Diagram

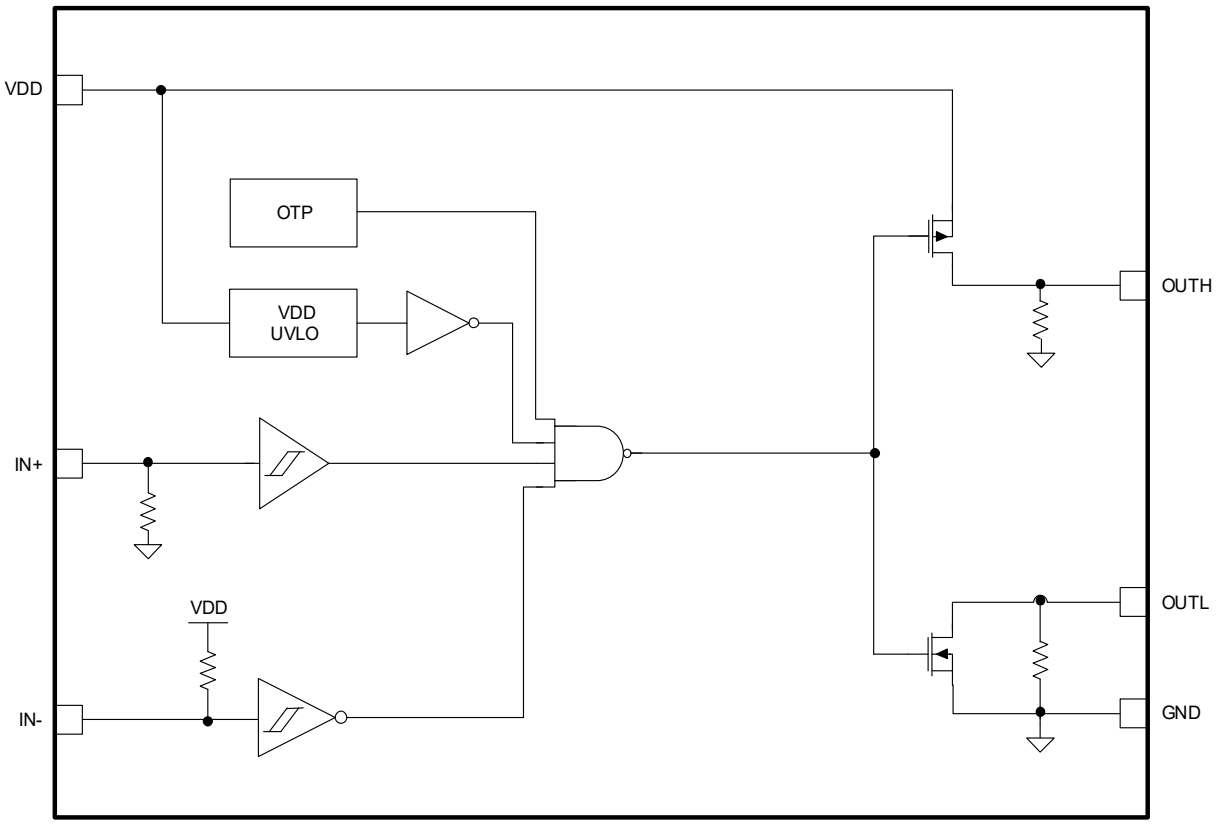


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

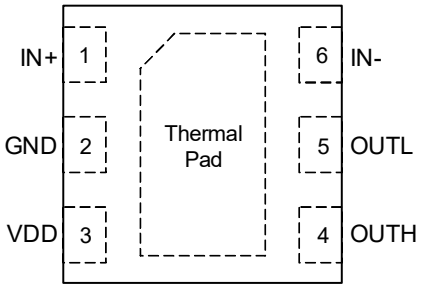


Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Name	Pin Number	Description
VDD	3	Supply voltage is 5V. Decouple through a small size, low inductance capacitor to GND.
OUTH	4	Pull-up gate drive output. Connect through an optional resistor to the gate of the target transistor.
GND	2	Analog ground. Provides the ground return path for driver circuitry and internal reference.
OUTL	5	Pull-down gate drive output. Connect through an optional resistor to the gate of the target transistor.
IN+	1	Positive logic-level input
IN-	6	Negative logic-level input. The pin could be used as negative logic EN function.
Thermal Pad	-	Internally connected to the ground plane through substrate.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, VDD	-0.3	6.0	V
Output Voltage, OUTH, OUTL	-0.3	6.0	V
Input voltage, IN+, IN-	-0.3	6.0	V
Maximum Junction Temperature	-40	150	°C
Maximum Storage Temperature Range	-65	150	°C
Human Body Model (Tested per JS-001-2023)	-2000	2000	V
Charged Device Model (Tested per JS-002-2022)	-750	750	V
Latch-Up (Tested per JESD78F; Class 2, Level A)	-100	100	mA

1. All voltages referenced to GND (AGND and PGND are connected together as GND) unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter[1][2]	Minimum	Typical	Maximum	Units
Supply Voltage, VDD	4.5	5.0	5.5	V
Output Voltage, OUTH, OUTL	0.0	-	5.5	V
Input Voltage, IN+, IN-	0.0	3.3/5	5.5	V
Operating Temperature	-40	-	125	°C

1. All voltages referenced to GND (AGND and PGND are connected together as GND) unless otherwise specified.
2. Assured by design.

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	6 Ld SCTDFN	θ_{JA}[1]	Junction to ambient (on JEDEC high effective thermal conductivity test board with direct attach features)	68	°C/W
		θ_{JC}[2]	Junction to case (at bottom)	11	
		θ_{JB}	Junction to board	31	
Max Power Dissipation		P_D	For T_J(MAX) of 150°C in free air at 25°C	1.83	W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board with direct attach features in free air. See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

3.4 Electrical Specifications

Typical Values at 25°C, V_{DD} = 5V; GND = 0V. Limits apply across the operating temperature range, -40°C to +125°C.

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Power Supply						
V_{DD} Quiescent Current	I_Q	V_{DD} = 5V; IN+ = IN- = 0V	-	48	-	µA
V_{DD} Operating Current	I_O	V_{DD} = 5V; f_{SW} = 1000kHz PWMx = 50% square wave, EN = V_{DD}, C_{LOAD} = 1000pF	-	5.9	-	mA
VDD UV Rising Threshold	VIN_{UV_Rise}	-	3.9	4.2	4.5	V
VDD UV Threshold Hysteresis	-	-	-	0.2	-	V
PWMx INPUT						
Low Level Input Voltage Threshold	VIN_{x_L}	-	1.0	1.4	1.8	V
High Level Input Voltage Threshold	VIN_{x_H}	-	1.6	2.1	2.7	V
Input Voltage Hysteresis	VHys	-	-	0.7	-	V
Input Pull-Down IN+	RIN+	PWMx = V_{DD}. Measure I.Calculate R. Pull down	100	200	300	kΩ
Input Pull-UP IN-	RIN-	-	100	200	300	kΩ
Minimum Input Pulse Width for Response at Output to Reach 90% Value	T_{MIN}	C_{LOAD} = 1nF	-	7.0[2]	-	ns
Output						
Peak Source Current	ISRC	V_{DD} = 5V, CV_{DD} = 20.1µF, CL = 0.256µF, f = 10Hz	-	7.2[2]	-	A
Pull-Up Resistance	ROH	V_{DD} = 5V, IOUT = 100mA	-	0.30[2]	-	Ω
Peak Sink Current	ISNK	V_{DD} = 5V, CV_{DD}= 20.1µF, CL = 0.256µF, f = 10Hz	-	5.3[2]	-	A
Pull-Down Resistance	ROL	V_{DD} = 5V, IOUT = 100mA	-	0.25[2]	-	Ω
OUTH, OUTL Pull Down Resistance	$Rout_L$, $Rout_H$	-	-	400	-	kΩ
Thermal Shutdown						
Thermal Shutdown	OT	-	-	160	-	°C
Thermal Hysteresis	-	-	-	20	-	°C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Characterized by engineering samples, not fully tested.

3.5 Switching Specifications

Typical Values at 25°C, V_{DD} = 5V; GND = 0V. Limits apply across the operating temperature range, -40°C to +125°C.

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn ON Propagation Delay (50% IN to 50% OUT)	TDON	C_{LOAD} = 1nF, 50% of the input rise to 50% of output rise, V_{DD} = 5V, f_{SW} = 1MHz, 50% duty cycle	-	5[1]	-	ns
Turn OFF Propagation Delay (50% IN to 50% OUT)	TDOFF	C_{LOAD} = 1nF, 50% of the input fall to 50% of output fall, V_{CC} = 5V, f_{SW} = 1MHz, 50% duty cycle	-	5[1]	-	ns
Pulse Positive Distortion (Δtpd)	-	C_{LOAD} = 1000pF	-	150[1]	-	ps
Output Rise Time (10% to 90%)	TRx	C_{LOAD} = 1nF, V_{DD} = 5V, f_{SW} = 1MHz, 50% duty cycle	-	4[1]	-	ns
Output Fall Time (90% to 10%)	TFx	C_{LOAD} = 1nF, V_{DD} = 5V, f_{SW} = 1MHz, 50% duty cycle	-	4[1]	-	ns

1. Characterized by engineering samples, not fully tested.

3.6 Timing Diagrams

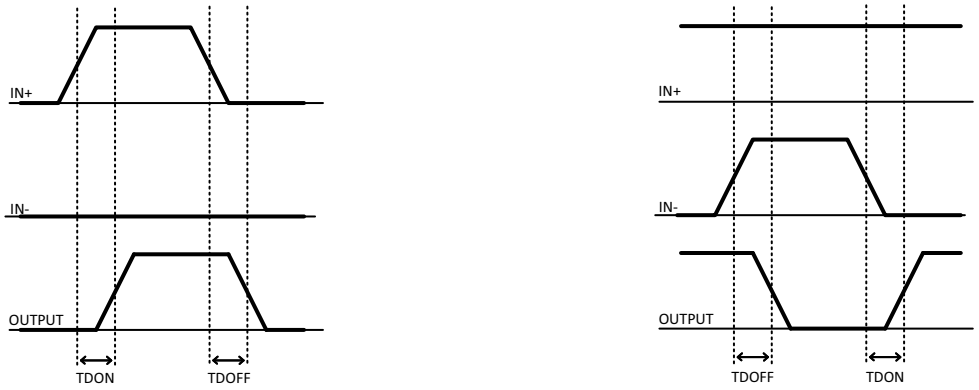


Figure 4. Propagation Delay Timing Diagram

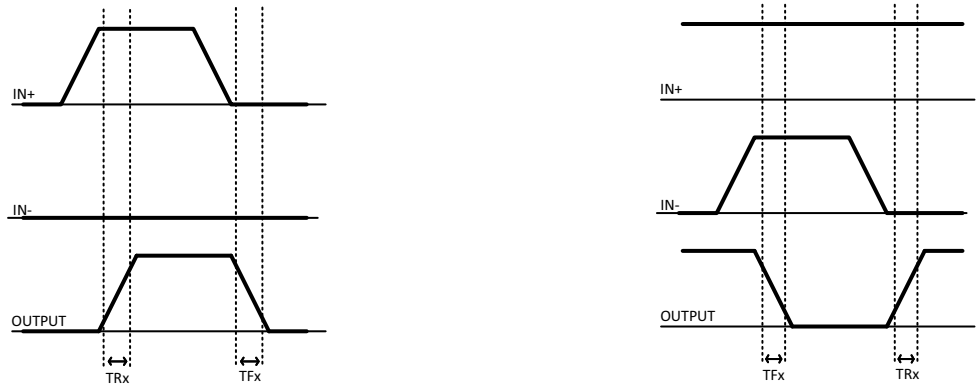


Figure 5. Output Rise and Fall Time

4. Typical Performance Curves

Unless otherwise specified, operating conditions at: T = +25°C; V_{DD} 5V;

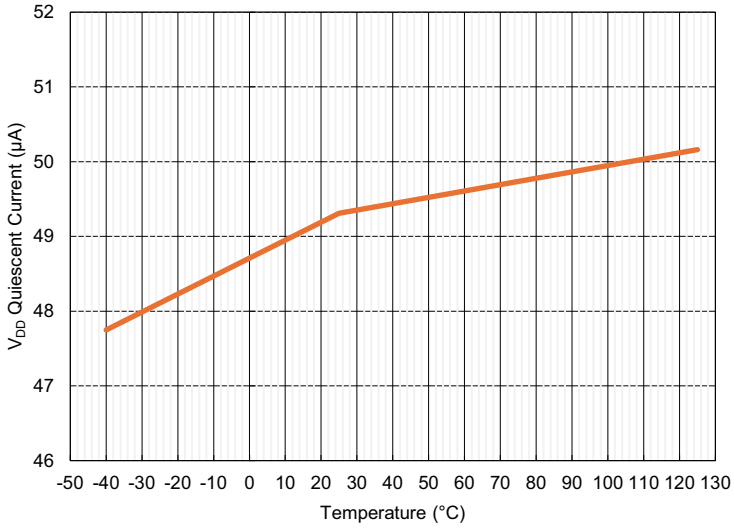


Figure 6. Quiescent Current vs Temperature

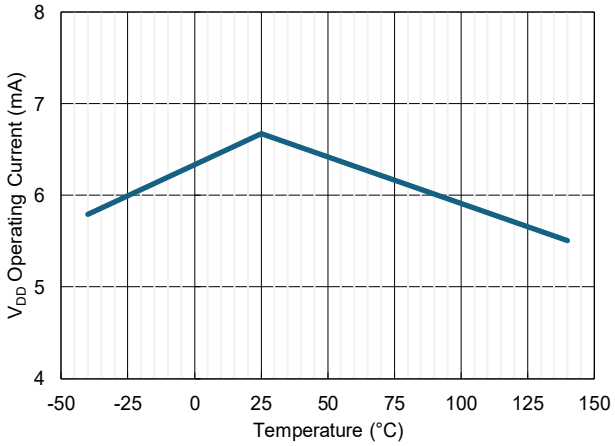


Figure 7. Operating Current vs Temperature, 1nF Load, 1MHz Frequency

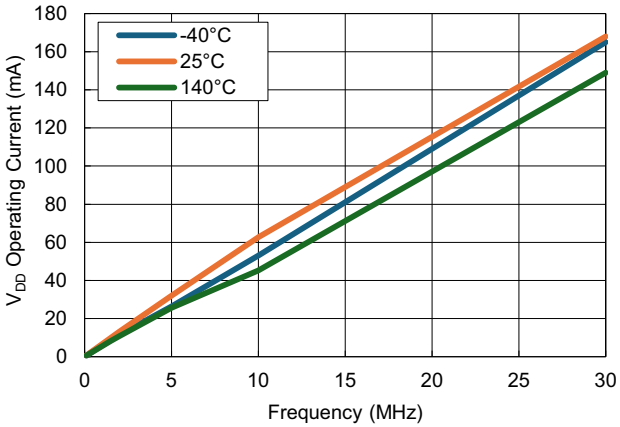


Figure 8. Operating Current vs Frequency, 1nF Load

Unless otherwise specified, operating conditions at: T = +25°C; V_{DD} 5V;

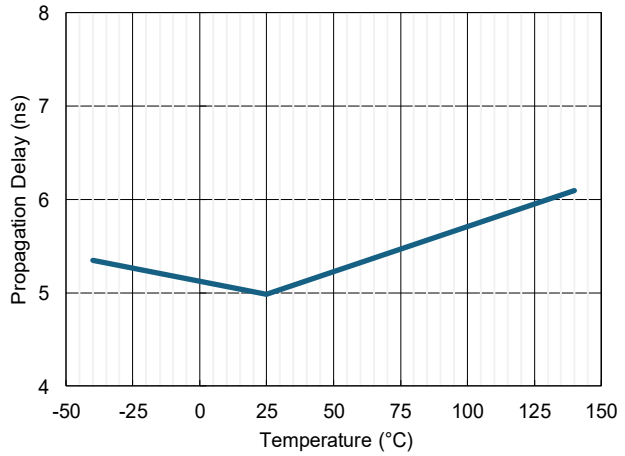


Figure 9. Propagation Delay vs Temperature, 1nF Load, Rising Edge

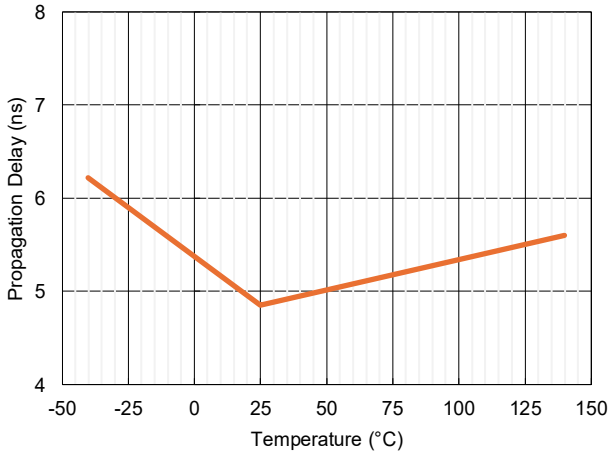


Figure 10. Propagation Delay vs Temperature, 1nF Load, Falling Edge

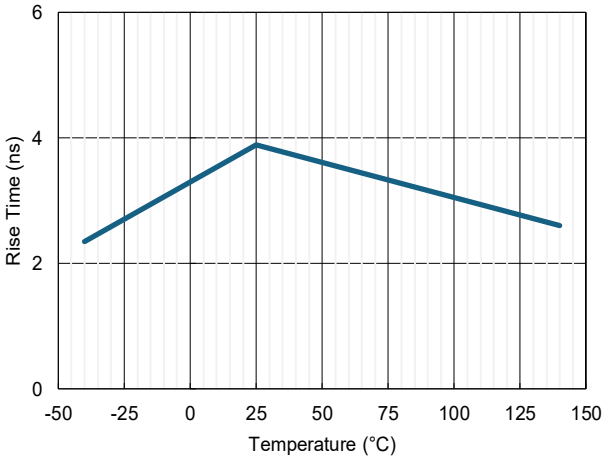


Figure 11. Rise Time vs Temperature, 1nF Load

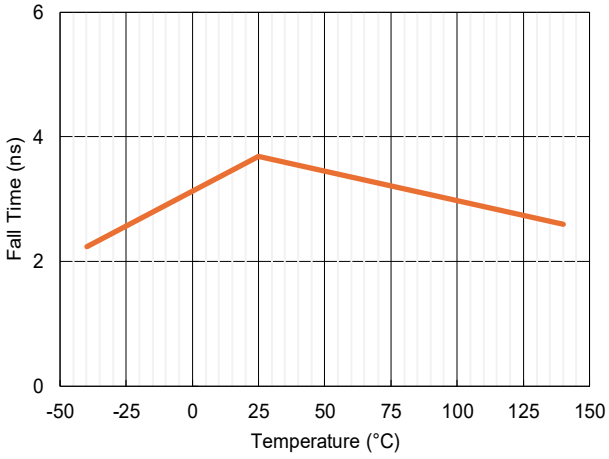


Figure 12. Fall Time vs Temperature, 1nF Load

5. Functional Description

5.1 Overview

The RRP63175 is an advanced gate driver engineered for GaN and silicon FETs in low-side configurations. This driver accommodates both 3.3V and 5V logic level PWM inputs and offers adjustable turn-on and turn-off strengths. The RRP63175 is optimized to deliver high peak current to the power transistor. Housed in a compact 2mm×2mm SCTDFN package with wettable flanks, this design is intended for high-density applications and mitigates the influence of parasitic inductance, which improves ringing performance across various conditions.

5.2 Input Stage

The input stage's IN+ and IN– pins are connected to an AND gate. When the IN+ signal exceeds the high-level input voltage threshold while the IN– signal remains below the low-level input voltage threshold, the output registers a high state. Conversely, the output transitions to a low state when both IN+ and IN– exceed the high-level input voltage threshold. Additional conditions resulting in a low output are detailed in the truth table (see Table 1). IN+ is connected to a pull-down resistor, and IN– is connected to a pull-up resistor to reduce the risk of erroneous behavior. The input pins are connected with two Schmitt triggers to minimize noise and mitigate the

impact of parasitic inductance on the performance of RRP63175. The IN- pin can be used as a negative logic EN pin.

Table 1. Functional Mode Table

IN-	IN+	OUTH	OUTL
Low	Low	Open	Low
Low	High	High	Open
High	Low	Open	Low
High	High	Open	Low

5.3 Output Stage

The output stage, comprising OUTH and OUTL, is designed with a split configuration, allowing for independent resistor connections to the gate. The output ringing and slew rate can be adjusted by using these two resistors. The RRP63175 features a peak drive current capability of 7.2 A for sourcing and 5.3 A for sinking. This current drive capability allows the driver to drive a 256nF load with a 1V output voltage difference time of 39ns for sourcing and 54ns for sinking.

5.4 Undervoltage Lockout (UVLO)

RRP63175 is equipped with an internal undervoltage lockout (UVLO) mechanism to protect against fault conditions. The UVLO threshold is set between 3.9V and 4.5V, with a large hysteresis of 0.2V. During UVLO conditions, the OUTL pin is pulled down to ground.

5.5 Over-Temperature Protection (OTP)

The RRP63175 over-temperature protection feature activates with a rising edge trigger point at approximately 160°C of junction temperature. The device exhibits a hysteresis of 20°C, allowing it to resume operation when the junction temperature falls below 140°C.

6. Applications Information

6.1 Output Damping

High-speed applications often encounter ringing issues. Reducing parasitic inductance by shortening printed circuit board traces is crucial. Additionally, adding a gate resistor in series with the output helps mitigate ringing, though it might slightly increase the rise and fall times. Employing bypassing techniques is also effective in preventing ringing.

6.2 VDD

Controlling overshoot voltage during switching is important to prevent the voltage from exceeding the absolute maximum limit. The RRP63175 supports typical supply voltages of 5V and a maximum of 6V. Reducing parasitic inductance in the layout is essential to mitigate ringing, which can contribute to VDD overshoot voltage.

6.3 Application Curves

The waveforms were recorded using an RRP63175 IC evaluation board. Figure 13 through Figure 16 illustrate the short propagation delays observed on both the IN+ and IN– pins with no load on the output. This propagation delay performance is critical for high-frequency applications.

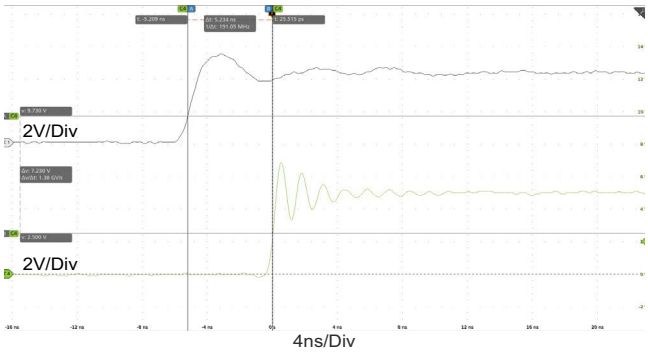


Figure 13. Propagation Delay (IN+ Rising Edge)

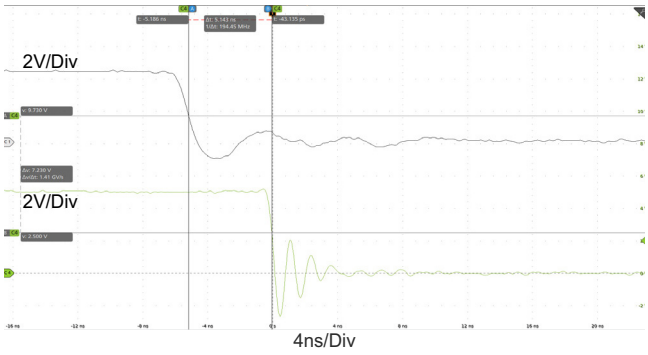


Figure 14. Propagation Delay (IN+ Falling Edge)

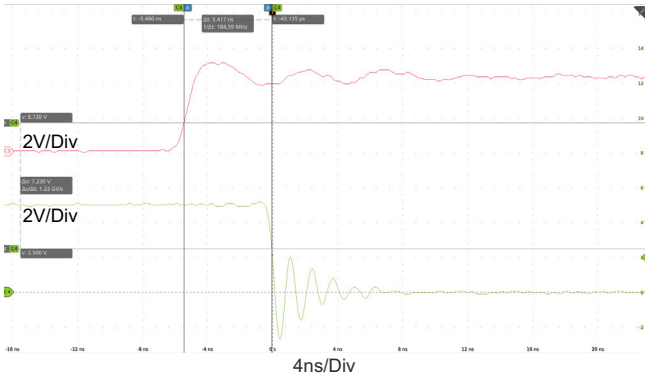


Figure 15. Propagation Delay (IN- Rising Edge)

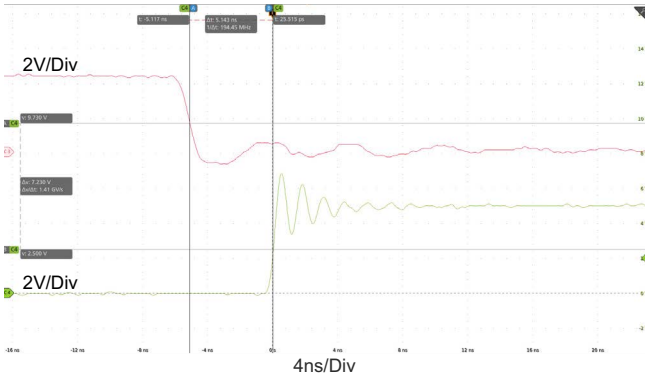


Figure 16. Propagation Delay (IN- Falling Edge)

7. PCB Layout Guidelines

The AC performance of the RRP63175 depends significantly on the design of the PCB. The following layout design guidelines are recommended to achieve optimum switching performance:

- Connect the driver thermal pad to a low thermal impedance ground plane.
- Use as many vias as possible to connect the top layer PCB thermal land to the ground planes on other PCB layers.
- Place the driver as close as possible to the driven power FET.
- Keep power loops as short as possible by routing the source and return traces on adjacent layers, directly above and beneath each other.
- It might be necessary to add resistance to dampen resonating parasitic circuits. PCB designs with long trace lengths on the outputs may require series gate resistors on the FETs to dampen the oscillations.
- Use low inductance components such as SMD chip resistors and chip capacitors with low Equivalent Series Inductance (ESL). The 0201 package is highly recommended.
- Bypass capacitors are strongly recommended for the VDD power terminal. It is essential to ensure the shortest possible lead lengths to the IC. Additionally, capacitors with a temperature coefficient of X7R or better are advisable.
- Use planes where practical; they are usually more effective than parallel traces. A four or more layer PCB design is recommended.
- Understand where the switching power currents flow. The high-amplitude di/dt currents of the driven power FET induce significant voltage transients on the associated traces.

- Avoid having a signal ground plane under a high-amplitude dv/dt circuit, which injects di/dt currents into the signal ground paths.
- Complete the power dissipation and voltage drop calculations for the power traces. Many PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (such as power FETs, Electrolytic caps, power resistors) have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If simulating the circuits is required, consider including parasitic components.

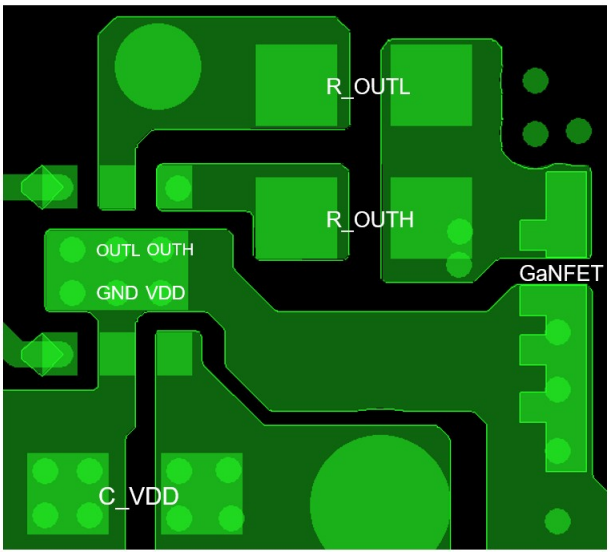


Figure 17. Typical RRP63175 Layout with GaN FET

8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number[1] [2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
RRP63175-NH0	175	6LD SC-TDFN	L6.2x2A	Reel, 6k	-40 to +125°C
RRP63175-NM0				Reel, 1k	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), refer to the RRP63175 product information pages. For more information about MSL, refer to TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. Refer to TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.02	Apr 21, 2025	Updated POD. Added ECAD Design Information.
1.01	Jan 17, 2025	Updated Features. Updated Figures 7 and 9-12. Updated section 5.1.
1.00	Nov 21, 2024	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRP63175-NH0	6	SCTDFN	L6.2x2A
RRP63175-NM0	6	SCTDFN	L6.2x2A

A.2 Symbol Pin Information

A.2.1 6-SCTDFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	IN+	Input	-
2	GND	Power	-
3	VDD	Power	-
4	OUTH	Output	-
5	OUTL	Output	-
6	IN-	Input	-
EPAD7	GND	Power	-

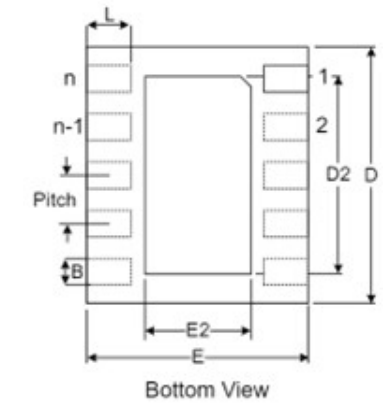
A.3 Symbol Parameters

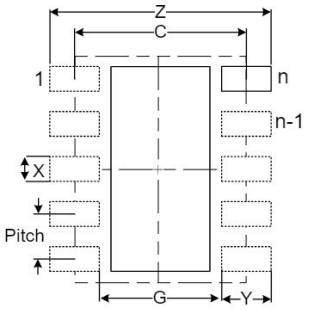
Orderable Part Number	Qualification	Mounting Type	Peak Source Current	Peak Sink Current	Min Supply Voltage	Max Supply Voltage	RoHS	Min Operating Temperature	Max Operating Temperature	Max Switching Frequency
RRP63175-NH0	Industrial	SMD	7.2 A	5.3 A	4.5 V	5.5 V	Compliant	-40 °C	125 °C	30 MHz
RRP63175-NM0	Industrial	SMD	7.2 A	5.3 A	4.5 V	5.5 V	Compliant	-40 °C	125 °C	30 MHz

A.4 Footprint Design Information

A.4.1 6-SCTDFN

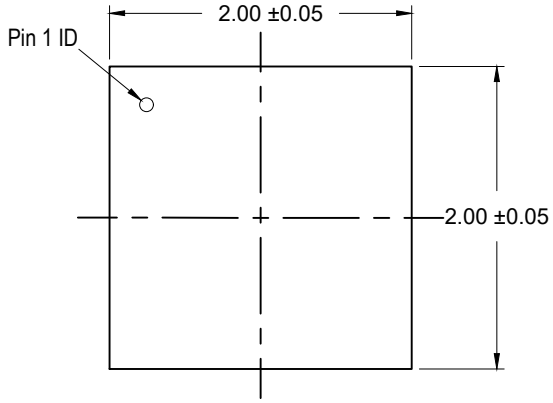
IPC Footprint Type	Package Code/ POD Number	Number of Pins
DFN	L6.2x2A/DW0006AA	6

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	1.95	 Bottom View
Maximum body span (vertical side)	Dmax	2.05	
Minimum body span (horizontal side)	Emin	1.95	
Maximum body span (horizontal side)	Emax	2.05	
Minimum Lead Width	Bmin	0.35	
Maximum Lead Width	Bmax	0.45	
Minimum Lead Width	Lmin	0.25	
Maximum Lead Width	Lmax	0.35	
Maximum Height	Amax	0.80	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.153	
Maximum Lead Thickness	cmax	0.253	
Number of pins	PinCount	6	 Side View
Distance between the center of any two adjacent pins	Pitch	0.65	
Minimum thermal pad size (vertical side)	D2min	1.50	
Maximum thermal pad size (vertical side)	D2max	1.70	
Minimum thermal pad size (vertical side)	E2min	0.80	
Maximum thermal pad size (vertical side)	E2max	1.00	

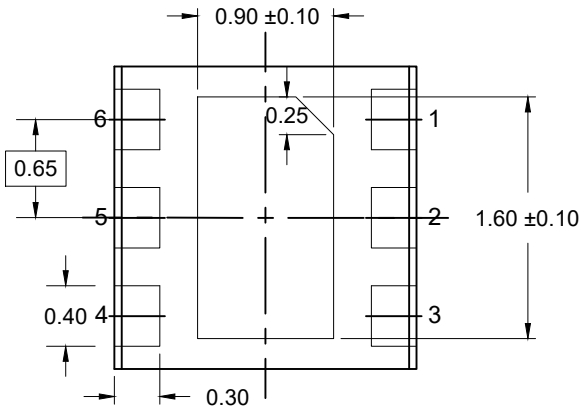
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Row spacing. Distance between pad centers.	C	1.85	 PCB Top View
Distance between pads. Measured from outside edges.	Z	2.30	
Distance between pads. Measured from inside edges.	G	1.40	
Pad Width	X	0.40	
Pad Length	Y	0.45	

Package Outline Drawing

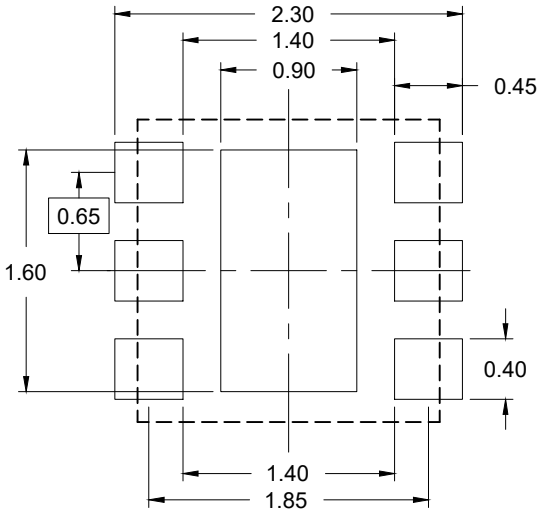
L6.2x2A
DW0006AA
6-SCTDFN 2.0 x 2.0 x 0.8 mm Body, 0.65 mm Pitch
Rev 02, Feb 18, 2025



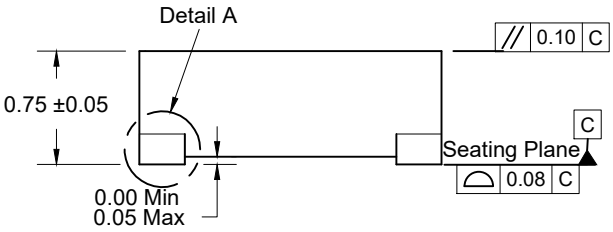
Top View



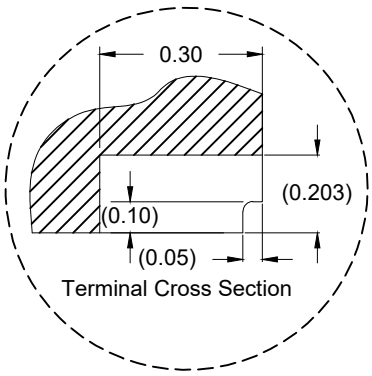
Bottom View



Recommended Land Pattern



Side View



Terminal Cross Section

Detail A: Wettable Flank

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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