RRP52999

-500mA, -20V Wide Input Voltage Range Negative LDO Linear Regulator

Description

The RRP52999 is a negative low-dropout linear voltage regulator that operates from -2.5V to -20V and provides up to 500mA of output current with a typical dropout of 269mV. The output voltage is adjustable with external feedback resistors anywhere from -1.2V to -18V.

The ground current is typically 98µA at no-load and drops to 10µA typical when in shutdown.

The LDO features excellent line and load regulation, input UVLO with hysteresis, enable control, short-circuit current limit with foldback, and over-temperature shutdown protection with hysteresis.

The LDO is stable with a minimum 2.2µF MLCC output capacitor and is available in 8 Ld 3mm×3mm DFN package.

Features

- Wide input voltage range: -2.5V to -20V
- Maximum output current: 500mA
- Low dropout voltage: 269mV typical at 500mA
- Low ground current
- Output voltage adjustable: -1.2V to -18V
- Excellent line and load regulation
- Stable with at least 2.2µF MLCC output capacitor
- Short-circuit current limit with foldback
- Over-temperature shutdown protection
- 8 Ld DFN (3mm×3mm) package

Applications

- Supply to analog-to-digital converter (ADC), digital-to-analog converter (DAC) circuits, and precision amplifiers
- Medical and healthcare
- Communication and infrastructure
- Industrial and instrumentation

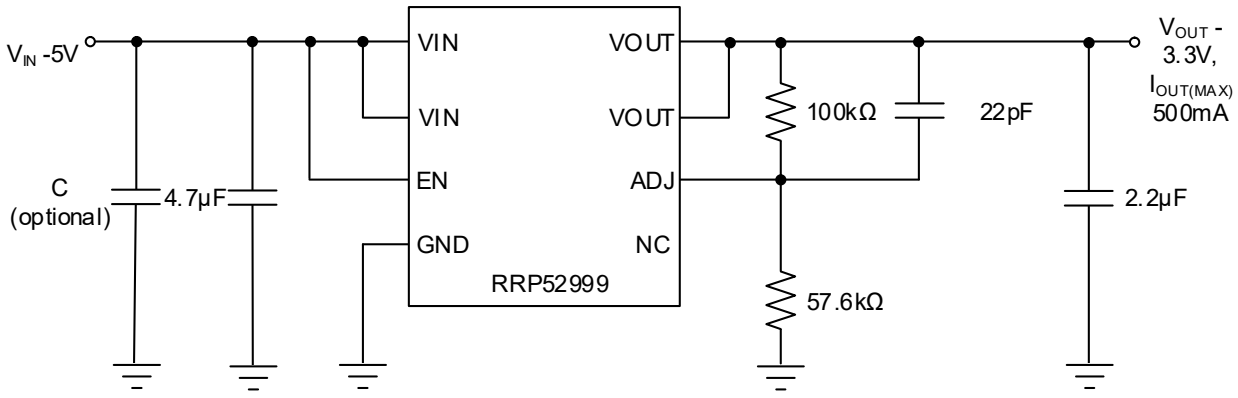


Figure 1. Typical Application Circuit

Contents

1. Overview

1.1 Block Diagram

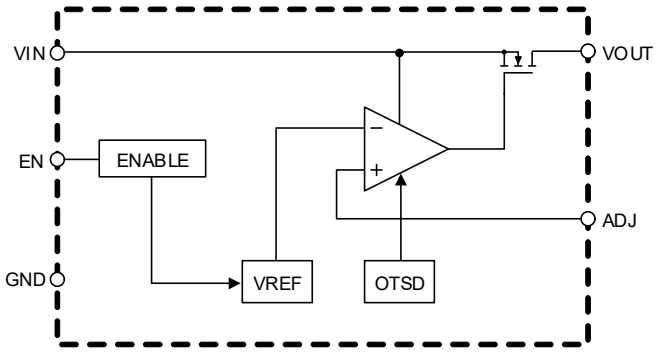


Figure 2. RRP52999 Block Diagram

2. Pin Information

2.1 Pin Assignments

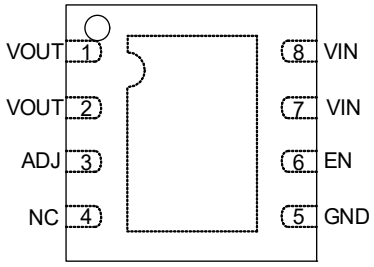


Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2	VOUT	VOUT are the regulated output voltage pins that supply power to the load. For stable operation across the full temperature range, input range, output range, and load extremes, a minimum 2.2µF X5R/X7R output capacitor is required between this pin and GND.
3	ADJ	ADJ is the adjustable pin. The ADJ pin is internally set to 1.2V using the band-gap circuitry. The external voltage divider formed around this pin sets the LDO output voltage. When the pin is shorted to VOUT, the output voltage is set to the minimum -1.2V. See Programming the Output Voltage for more information on setting the output voltage.
4	NC	No Connect
5	GND	GND is the ground pin. This pin must be tied to GND.
6	EN	EN is the ENABLE input and can be driven by either positive or negative logic. If VEN ≥ VEN_Rising or VEN ≤ VEN_Falling, the regulator is enabled, otherwise, the regulator is disabled. ***Important:*** This pin should not be left floating. Instead tie it to the VIN pins for automatic enabling. It is required that VEN ≥ VIN to avoid the leakage current because of the ESD diode between them.
7, 8	VIN	VIN are the input voltage pins that supply power to the LDO. Renesas recommends placing a 10µF and 1µF input capacitor from this pin to GND. Place the 1µF as close as possible to the VIN pins.
-	EPAD	EPAD is the exposed pad on the bottom of the package. To ensure proper electrical and thermal performance, solder the exposed pad to the PCB VIN plane and tie it directly to the VIN Pin 1. See Layout Guidelines for more layout guidelines for this pin.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, V_{IN}	-22	0.3	V
Enable Input Voltage, EN	-22	6	V
Output Voltage, V_{OUT}	-22	0.3	V
Adjustable Pin Voltage, ADJ	-6	0.3	V
Output Current, I_{OUT}	0	500	mA
Maximum Junction Temperature	-40	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	±1	kV
Charged Device Model (Tested per JS-002-2022)	-	±500	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. All voltages referenced to VSS unless otherwise specified.

3.2 Thermal Information

Parameter[1]	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld DFN 3×3	θ_{JA}[2]	Junction to ambient	56	°C/W
		θ_{JC}[3]	Junction to case	16	°C/W

1. Specified at published junction to ambient thermal resistance for a junction temperature of +150°C. See [2] for test conditions to establish junction to ambient thermal resistance.
2. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.3 Recommended Operating Conditions

Parameter[1]	Minimum	Maximum	Units
Supply Voltage (V_{IN})	-20	-2.5	V
Enable Input Voltage (EN)	VIN - 0.3	5	V
Output Voltage (V_{OUT})	-18	-1.2	V
Output Current (I_{OUT})	0	500	mA
Output Capacitor (C_{OUT})	2.2	200	µF
Junction Temperature (T_J)	-40	+125	°C

1. All voltages referenced to VSS unless otherwise specified.

3.4 Electrical Specifications

I_{OUT} = 1mA, C_{OUT} = 2.2µF, C_{IN} = 1µF, V_{IN} = -5V, V_{OUT} = V_{ADJ}, V_{EN} = 5V unless otherwise specified. Typical values are at T_A = 25C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage	V_{OUT}	-	**-18**	-	**-1.2**	V
Input Voltage	V_{IN}	-	**-20**	-	**-2.5**	V
Output Voltage Accuracy	-	I_{OUT} = 10mA, V_{OUT} = -3.3V, V_{IN} = -5V	**-2**	-	**2**	%
Reference Voltage	V_{REF}	-	-	-1.2	-	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{OUT} - 1V to -20V, I_{OUT} = 1mA	-	0.03	**0.05**	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = -5V, I_{OUT} = 100µA to 500mA, V_{OUT} = VADJ	-	0.0236	-	%/mA
Dropout Voltage[2]	V_{DO}	I_{OUT} = 10mA, V_{OUT} = -3.3V	-	4.5	-	mV
		I_{OUT} = 50mA, V_{OUT} = -3.3V	-	22	-	mV
		I_{OUT} = 500mA, V_{OUT} = -3.3V	-	220	**380**	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0, V_{IN} = -5V	-	10	-	µA
		V_{EN} = 0, V_{IN} = -20V	-	12	-	µA
Ground Current	I_{GND}	I_{OUT} = 0mA, V_{IN} = -5V, V_{EN} = ±5V	-	98	-	µA
		I_{OUT} = 10mA, V_{IN} = -5V, V_{EN} = ±5V	-	225	-	µA
		I_{OUT} = 50mA, V_{IN} = -5V, V_{EN} = ±5V	-	280	-	µA
		I_{OUT} = 500mA, V_{IN} = -5V, V_{EN} = ±5V	-	620	-	µA
Power Supply Rejection Ratio	PSRR	FREQ = 100Hz, I_{OUT} = 500mA, V_{IN} = -6.5V, V_{OUT} = -5V	-	66	-	dB
Output Voltage Noise	-	BW = 10Hz to 100kHz, I_{OUT} = 50mA, C_{OUT} = 2.2µF, V_{OUT} = VADJ	-	230	-	μV_{RMS}
EN Positive Threshold	-	-	-	1.2	**1.5**	V
EN Negative Threshold	-	-	-1.6	-1.2	-	V
EN Hysteresis for Positive Threshold	-	-	-	200	-	mV
EN Hysteresis for Negative Threshold	-	-	-	200	-	mV
EN Leakage Current	-	V_{EN} = -5V	-	0.132	-	µA
VIN UVLO Rising Threshold	-	-	-	-2.1	-	V
VIN UVLO Hysteresis	-	-	-	200	-	mV
Short Circuit Current Limit	-	No Foldback	**550**	-	-	mA
		With Foldback, V_{IN} - V_{OUT} = -10V	**550**	-	-	mA
		With Foldback, V_{IN} - V_{OUT} = -18V	-	-	**650**	mA
Thermal Shutdown	-	-	-	150	-	°C
Hysteresis	-	-	-	20	-	°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its normal value.

4. Typical Performance Graphs

Operating conditions unless otherwise noted: T_A = 25°C, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 2.2µF.

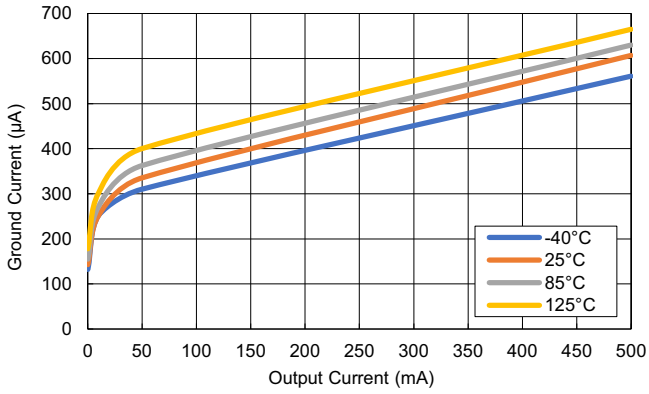


Figure 4. Ground Current vs Output Current (V_{IN} = -5V, V_{OUT} = -3.3V)

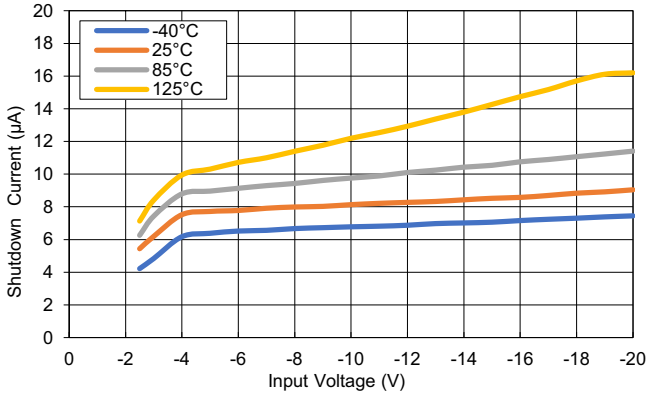


Figure 5. Shutdown Current vs Input Voltage

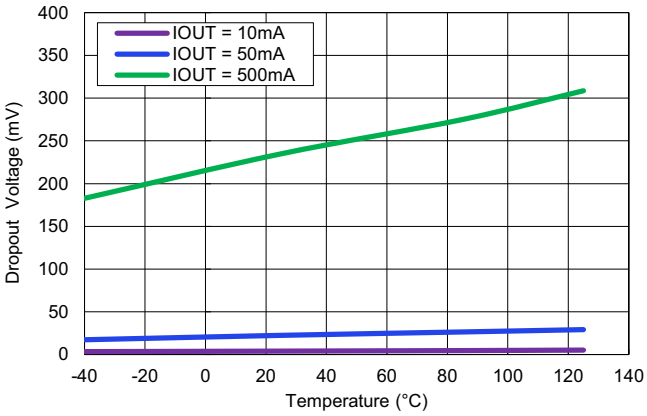


Figure 6. Dropout Voltage vs Temperature (V_{OUT} = -3.3V)

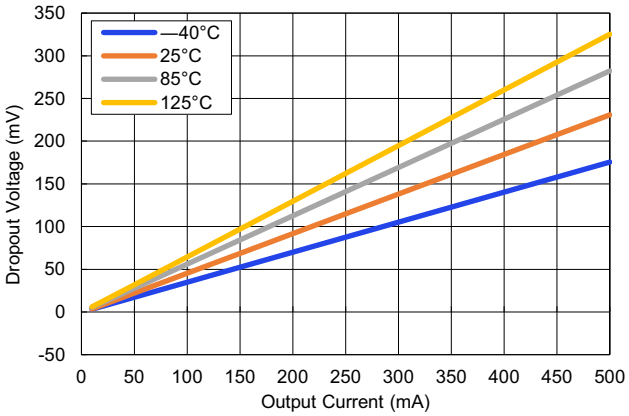


Figure 7. Dropout Voltage vs Output Current (V_{OUT} = -3.3V)

Operating conditions unless otherwise noted: T_A = 25°C, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 2.2µF.

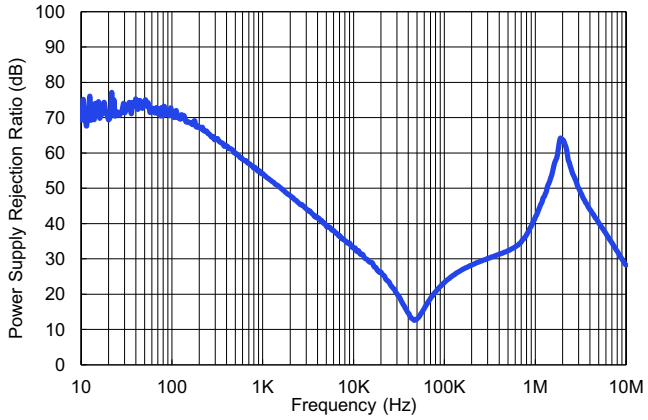


Figure 8. Power Supply Rejection Ratio (V_{IN} = -5V, V_{OUT} = -3.3V, I_{OUT} = 0.5A, C_{IN} = 10nF, C_{OUT} = 2.2µF)

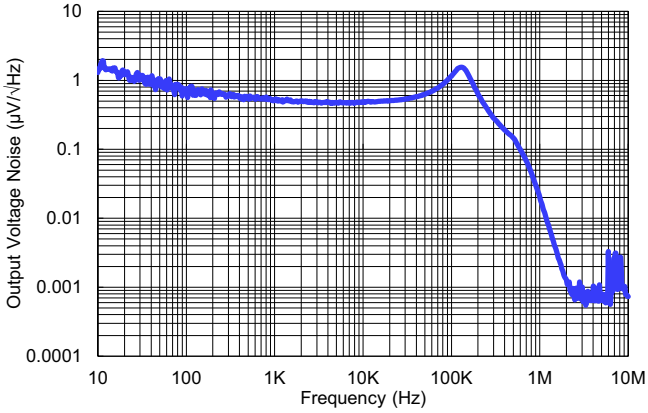


Figure 9. Output Voltage Noise (V_{IN} = -5V, V_{OUT} = -1.2V, I_{OUT} = 50mA, C_{OUT} = 2.2µF)

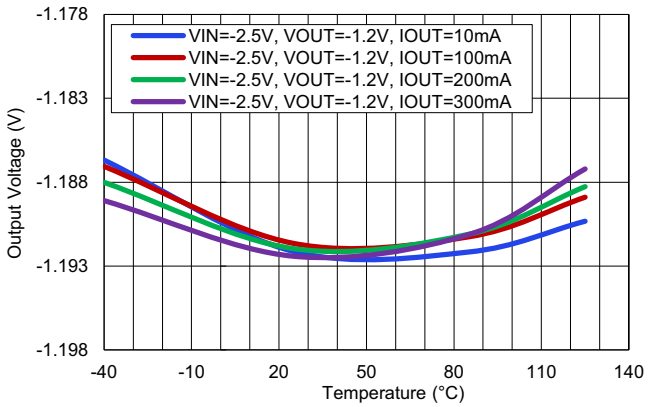


Figure 10. Output Voltage vs Temperature (V_{IN} = -2.5V, V_{OUT} = -1.2V)

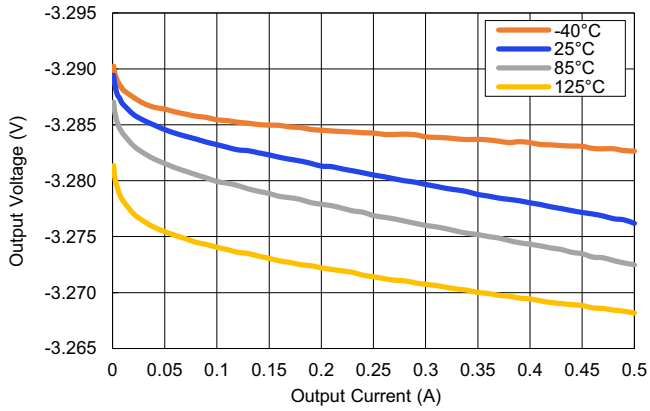


Figure 11. Load Regulation vs Output Current (V_{OUT} = -3.3V)

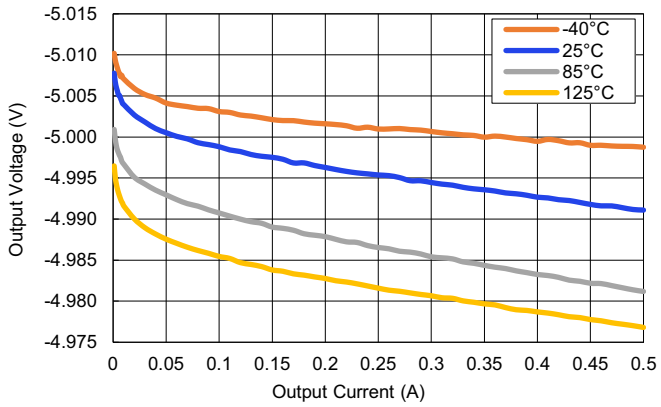


Figure 12. Load Regulation vs Output Current (V_{OUT} = -5V)

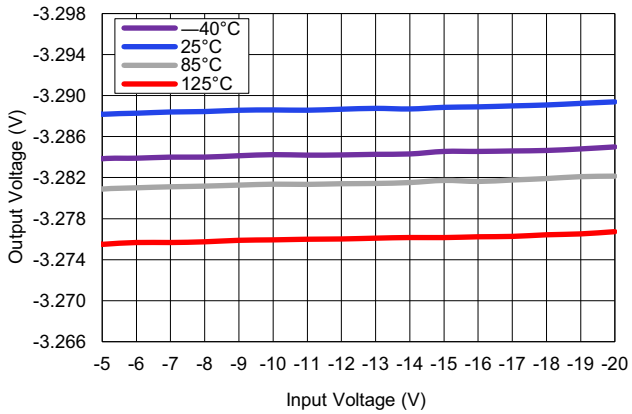


Figure 13. Line Regulation vs Input Voltage (V_{OUT} = -3.3V, I_{OUT} = 1mA)

Operating conditions unless otherwise noted: T_A = 25°C, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 2.2µF.

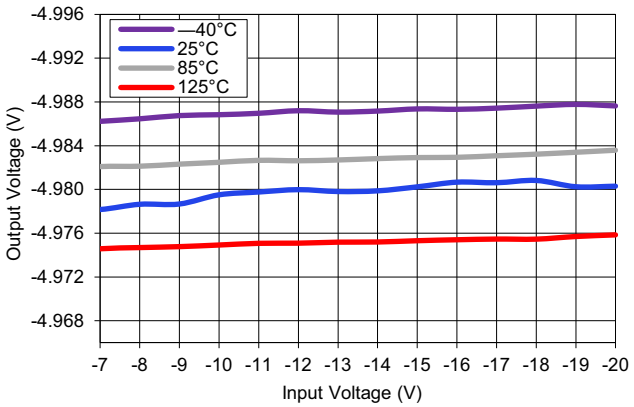


Figure 14. Line Regulation vs Input Voltage (V_{OUT} = -5V, I_{OUT} = 1mA)

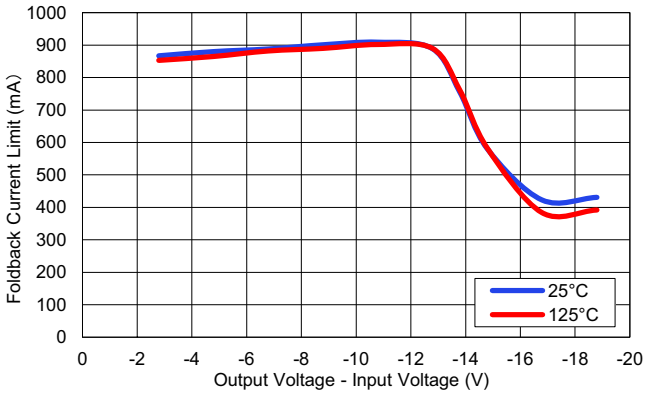


Figure 15. Foldback Current Limit vs Output Voltage - Input Voltage

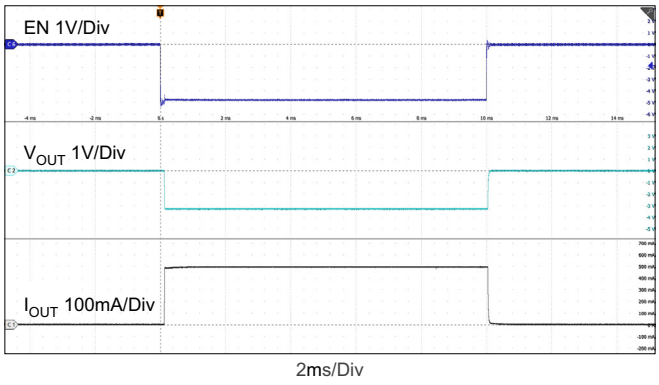


Figure 16. Enable Turn-on Response (V_{OUT} = -3.3V, I_{OUT} = 500mA, EN = -5V)

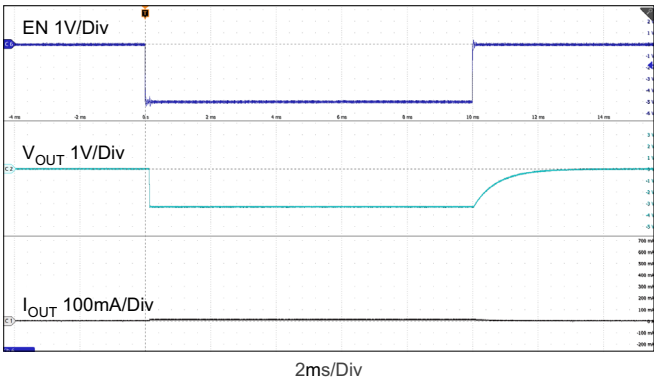


Figure 17. Enable Turn-on Response (V_{OUT} = -3.3V, I_{OUT} = 10mA, EN = -5V)

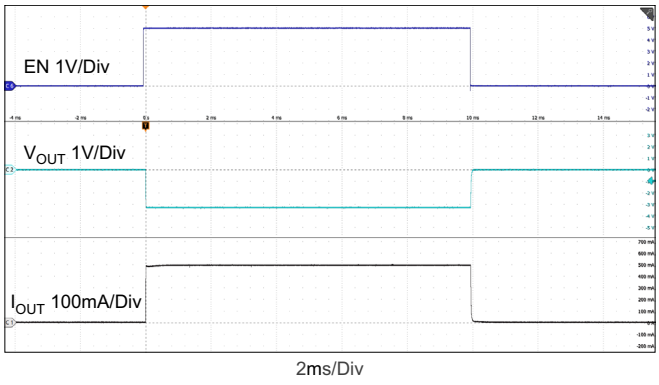


Figure 18. Enable Turn-on Response (V_{OUT} = -3.3V, I_{OUT} = 500mA, EN = 5V)

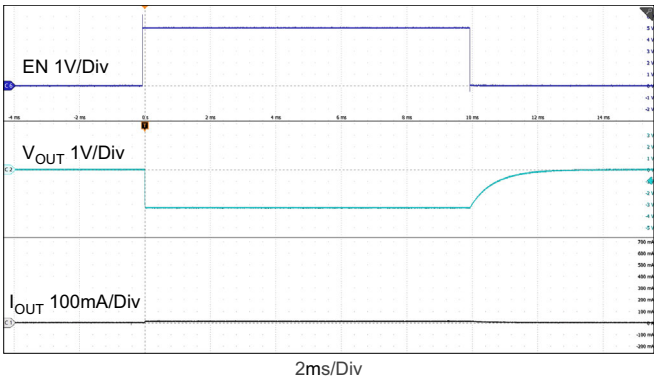


Figure 19. Enable Turn-on Response (V_{OUT} = -3.3V, I_{OUT} = 10mA, EN = 5V)

Operating conditions unless otherwise noted: T_A = 25°C, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 2.2µF.

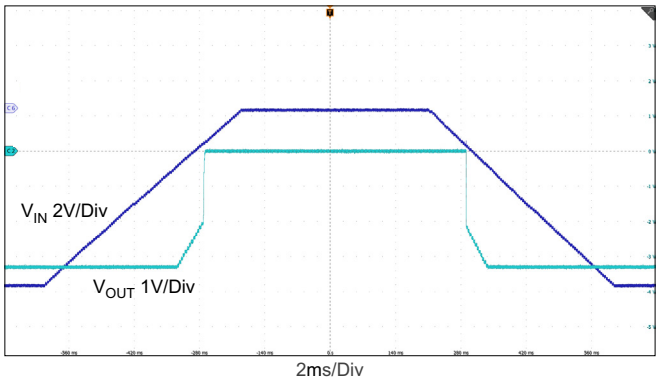


Figure 20. Turn-on/off Response from Slow Rising/Falling V_{IN} (V_{OUT} = -3.3V, I_{OUT} = 10mA, EN = V_{IN})

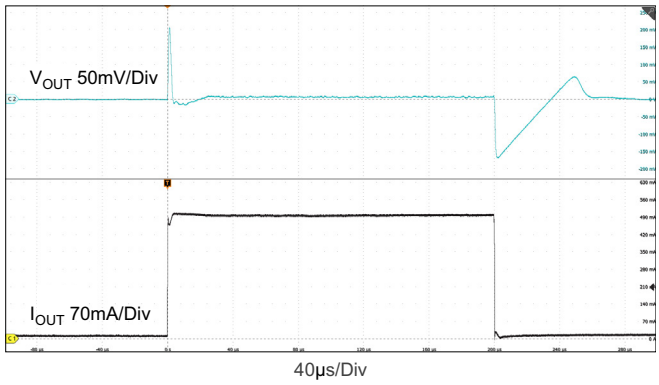


Figure 21. Load Transient Response (V_{IN} = -6V, V_{OUT} = -3.3V, ΔIOUT = 10mA to 500mA, C_{OUT} = 2.2µF)

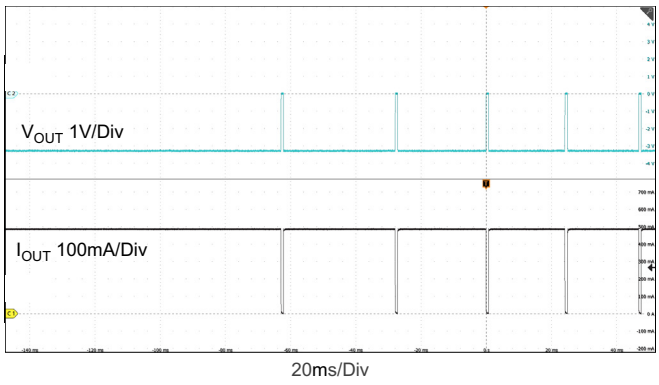


Figure 22. Thermal Shutdown and Recovery (V_{IN} = -12V, V_{OUT} = -3.3V)

5. Application Information

5.1 Overview

The RRP52999 is a low-dropout (LDO) linear voltage regulator that operates from an input voltage of -2.5V to -20V while sourcing a maximum 500mA load. The output voltage is adjustable with external feedback resistors from -1.2V to -18V. It typically draws 98µA of ground current at no-load which drops to 10µA during shutdown.

The RRP52999 is designed and tested with a 2.2µF minimum output capacitor, and a 1µF input capacitor. The LDO is available in a 3×3mm 8 Ld DFN package.

The RRP52999 integrates the following additional features:

- Undervoltage Lockout (UVLO)
- Enable Control
- Short-Circuit Current Limit with Foldback
- Thermal Shutdown Protection

5.2 Theory of Operation of NMOS LDOs

Like the majority of LDOs with a NMOS pass transistor, the RRP52999 DC output voltage (V_{OUT}) regulation can be a modeled with a voltage reference (V_{REF}), NMOS pass-transistor, error amplifier and feedback (FB) resistors as shown in Figure 23.

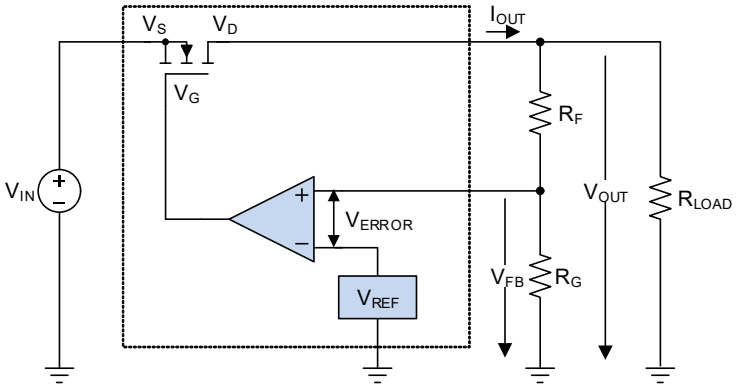


Figure 23. Simple NMOS LDO Regulator Block Diagram

The NMOS pass transistor can be modeled as a variable resistor ($r_{DS(ON)}$) that is controlled by the error amplifier to maintain a constant DC output voltage for changes in load current (I_{OUT}). Assuming the input voltage (V_{IN}) remains constant, the $r_{DS(ON)}$ is adjusted for a given I_{OUT} to set V_{OUT}. This relationship is summarized in Equation 1.

(EQ. 1) $$V_{OUT} = V_{IN} - I_{OUT} \times R_{DS(ON)}$$

V_{OUT} is set using the FB resistor divider, which sets V_{OUT} to a value that corresponds to Equation 2.

(EQ. 2) $$V_{OUT} = V_{FB} \times \left(\frac{R_F}{R_G} + 1 \right)$$

The error amplifier compares V_{FB} with the fixed V_{REF} voltage and works to minimize the difference or error voltage between V_{FB} and V_{REF} by changing the gate voltage of the NMOS pass transistor and therefore the $r_{DS(ON)}$.

If the I_{OUT} suddenly increases because of decreased load resistance, V_{OUT} increases because the regulator has not responded to the change and the $r_{DS(ON)}$ is set too high. V_{FB} correspondingly increases and is above the V_{REF} voltage therefore, increasing the error voltage. The error amplifier senses and minimizes the error by driving the NMOS gate voltage more positive relative to the FET source to decrease the $r_{DS(ON)}$, which decreases the output voltage bringing it back into regulation.

By similar logic, a sudden decrease in I_{OUT} because of increased load resistance causes V_{OUT} to decrease because the $r_{DS(ON)}$ is set too low. V_{FB} is then lower than the fixed V_{REF} voltage increasing the error. The error amplifier senses and minimizes the error by driving the NMOS gate voltage more negative relative to the FET source to increase the $r_{DS(ON)}$, which increases the output voltage bringing it back into regulation.

6. Functional Description

6.1 UVLO

The RRP52999 integrates an internal UVLO circuit to keep the device safely disabled if the input voltage is above the UVLO threshold. This prevents the part from turning on in an unpredictable state.

When the input voltage is below the UVLO threshold, the part is enabled and the output voltage ramps up. The UVLO hysteresis prevents input voltage noise from causing the output to oscillate as well as prevents input voltage droops because of long input traces and wires from turning off the LDO when it turns on and draws current. Figure 24 illustrates the UVLO operation.

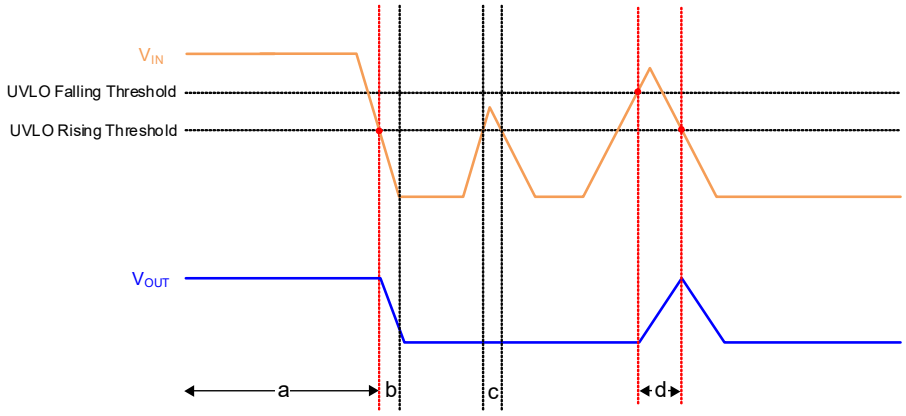


Figure 24. UVLO Operation

a, d The LDO is disabled.

b The LDO is enabled and the output starts to rise.

c The LDO remains enabled.

6.2 Enable Control

RRP52999 uses the bipolar EN voltage (VEN) to enable or disable the LDO. If VEN ≥ VEN_Rising or VEN ≤ VEN_Falling, the regulator is enabled, otherwise, the regulator is disabled. ***Important***: This pin should not be left floating. Instead tie it to the VIN pins for automatic enabling. It is required that VEN ≥ VIN to avoid the leakage current because of the ESD diode between them. The VEN hysteresis prevents enable voltage noise from causing the output to oscillate. When the LDO is disabled, the shutdown current is typically 10μA.

The EN pin can be directly connected to the input voltage for automatic start-up or connected to a logic controller such as an MCU of FPGA. To ensure proper Enable control operation, the V_{EN} signal source should be capable of swinging above and below the threshold values. The device also has a very accurate and stable Enable threshold, which allows the user to program the Enable voltage through a resistor divider.

6.3 Short-Circuit Current Limit Protection and Foldback

The Short-Circuit Protection circuitry (ILIM) limits the maximum output current the LDO can source during fault conditions such as short-circuits or start-up inrush current. During a short-circuit fault, the LDO becomes a constant current source and as a result any decrease in load resistance causes a decrease in the output voltage. This relationship is summarized in Equation 3.

(EQ. 3) $$V_{OUT} = ILIM \times R_{FAULT}$$

The RRP52999 also incorporates fold-back, which reduces the constant current limit to reduce the amount of power dissipation caused during short-circuit events.

When the short or overcurrent condition is removed, the LDO returns to normal output voltage regulation. Because of the high power dissipation caused by overcurrent faults, the LDO might begin to cycle ON and OFF because the die junction temperature (T_J) is exceeding thermal fault conditions (+150°C) and subsequently cooling down to +130°C when the LDO is disabled.

6.4 Over-Temperature Shutdown (OTSD) Protection

The RRP52999 is protected against thermal overloads caused by current limit protection or high ambient temperature (T_A). When the die junction temperature (T_J) exceeds +150°C, the thermal shutdown circuit disables the LDO by reducing the output current (I_{OUT}) to 0A and therefore reducing the output voltage (V_{OUT}) to 0V, allowing the LDO to cool. A 20°C hysteresis is included to prevent the LDO from uncontrollably heating and cooling.

Prolonged exposure to a T_J exceeding +125°C reduces the long-term stability and life of the LDO. Therefore, it is important that the design considers the T_A the LDO works in, the thermal resistance between T_J and T_A (θ_{JA}), and any fault conditions that can cause the T_J to exceed the recommended operating range. In some applications, implementing a heat sink can be required.

6.5 Voltage Requirements

6.5.1 Input Voltage

The RRP52999 operates with an input voltage of -2.5V to -20V on the VIN pin. The input supply must be able to supply enough current to keep the input voltage from drooping during load steps or high load currents.

For proper voltage regulation the input voltage must be chosen so that it is higher than the sum of the output voltage and the maximum dropout voltage expected for a given application as expressed in Equation 4.

(EQ. 4) $$|V_{IN}| > |V_{OUT}| + V_{DROPOUT(MAX)}$$

The difference between V_{IN} and V_{OUT} required for proper regulation is commonly called the headroom voltage ($V_{HEADROOM}$).

6.5.2 Programming the Output Voltage

The RRP52999 output voltage can be programmed down to -1.2V and up to -18V using external resistors, RF and RG shown in Figure 25.

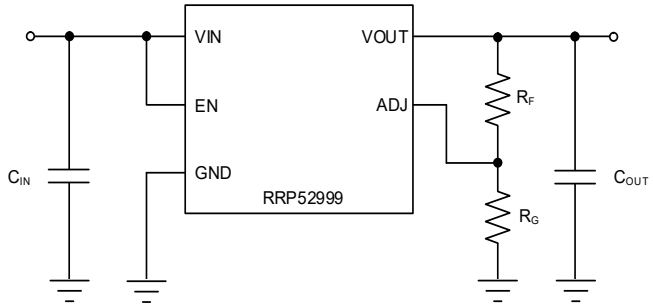


Figure 25. Setting the Output Voltage

V_{OUT} is calculated using Equation 5, where V_{REF} is the reference voltage.

(EQ. 5) $$V_{OUT} = V_{REF} \times \left(1 + \frac{R_F}{R_G}\right)$$

Similarly, the R_F and R_G resistors are calculated for any target output voltage by rearranging Equation 5 to get Equation 6 and solving for R_F.

(EQ. 6) $$R_F = R_G \times \left(\frac{V_{OUT(TARGET)}}{(-1.2V)} - 1\right)$$

The voltage divider resistors with commercially available in 0.1% tolerances are recommended to obtain the high accuracy of the output voltage.

6.6 External Capacitor Selection

The RRP52999 is stable with C_{IN} C_{OUT} and bypass capacitors. For improved load transient, line transient, PSRR and output noise performance a feed-forward capacitor (C_{FF}) is recommended though it is not required.

Multilayer ceramic capacitors (MLCC) are an excellent choice for bypass capacitors because of their small size, low ESR, low ESL, and wide operating temperature. They are not without their problems though. Ceramic capacitor values can vary with the DC bias voltage, temperature, and tolerance. Therefore, Renesas recommends using de-rated capacitors.

X5R, X7R, and C0G capacitors are recommended.To ensure the performance of the RRP52999, it is important that the effects of DC bias voltage, temperature, and tolerances for a chosen capacitor are evaluated. The X7R type is recommended because it has lower capacitance variation over temperature.

Place the bypass capacitors as close as is practical to their respective pins to minimize trace inductance.

6.6.1 Input Capacitor

The minimum input capacitor that is recommended is 1µF to reduce the negative effects of large input impedances because of long input traces of high source impedances. This capacitor should be connected between VIN and GND. Adding a larger bulk capacitor such as a 10µF might be required to minimize input voltage droops during large changes in load currents, such as during load transients or during start-up, which does not affect stability. Larger input capacitors also improve the line transient response.

6.6.2 Output Capacitor

The RRP52999 is stable with a minimum 2.2µF output ceramic capacitor.

A large value output capacitor can help minimize the overshoot and undershoot transient response because of large changes in load current. Larger output capacitors or multiple output capacitors can also be used to improve high-frequency PSRR.

6.6.3 Feed Forward Capacitor

A Feed-Forward Capacitor (C_{FF}) in parallel with the RF resistor as shown in Figure 26 can be used to improve the transient, noise, start-up and PSRR performance. However, it is not necessary to use one to achieve stability.

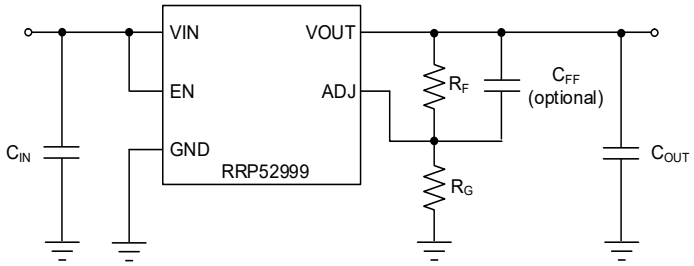


Figure 26. The Feed-Forward Capacitor

6.7 Power Dissipation and Thermals

To ensure reliable operation, the die junction temperature (T_J) of the RRP52999 must not exceed +125°C. In applications with high ambient temperature (T_A), large headroom voltages ($V_{HEADROOM}$), and large load currents (I_{OUT}), the heat dissipated in the package can become large enough to cause the T_J to exceed the maximum operating temperature of +125°C.

6.7.1 Power Dissipation

The Power Dissipation (PD) is calculated using Equation 7.

(EQ. 7) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times IQ(V_{IN})$$

Because the power dissipation contribution from the quiescent (or ground current) is typically small compared to the current the LDO needs to supply to a load, it can be ignored and Equation 7 simplifies to Equation 8.

(EQ. 8) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, to lower the power dissipated inside the die, the $V_{HEADROOM}$ and/or the I_{OUT} can be decreased.

6.7.2 The Junction Temperature and Thermal Resistance

The junction temperature (T_J) is the sum of the environmental ambient temperature (T_A) and the temperature rise in the T_J because of power dissipation, which is calculated using Equation 9 if the ambient temperature, Power Dissipation, and θ_{JA} are known.

(EQ. 9) $$T_J = T_A + \theta_{JA} \times PD$$

The θ_{JA} is the thermal resistance between the junction temperature and ambient temperature and is largely dependent on the device package and the PCB design. The θ_{JA} includes the thermal resistance of the junction to the bottom thermal pad ($\theta_{JC(BOTTOM)}$) and the resistance of the junction to the top of the package ($\theta_{JC(TOP)}$). These two thermal resistances are determined by the package features, dimensions, areas, thicknesses, and materials and therefore are fixed.

The remaining thermal resistance that makes up θ_{JA} largely depends on the total PCB copper area, copper weight, location of the thermal planes, and location of the IC on the PCB, amongst other things. Therefore, to compare the θ_{JA} of different products it is important to ensure the PCB layouts are similar, which is why the JEDEC standard exists.

7. Layout Guidelines

The following are recommendations for the RRP52999 to achieve optimal performance:

- Place all the required components for the RRP52999 on the same layer as the IC.
- Place a minimum capacitance of 1µF ceramic input capacitor to the VIN and GND pins of the LDO as close as practical.
- Place a minimum capacitance of 2.2µF ceramic output capacitor to the VOUT and GND pins of the LDO as close as practical.
- The feedback trace should be short, direct, and away from other noisy traces. Place the feedback resistors as close as possible to the IC.
- The package thermal EPAD is the largest heat conduction path for the package. It should be soldered to a copper pad on the PCB underneath the part. The PCB thermal pad should have as many plated vias to increase the heat flow from the package thermal EPAD to the inner PCB areas and/or the bottom PCB area. If possible, adding thermal vias around the PCB package helps improve heat spread from the package to other layers of the board.
- Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow. For efficient heat transfer, it is important that the vias have low thermal resistance. Do not use thermal relief patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane. The top copper VIN layer, that the EPAD is connected to is the least thermally resistant path for heat flow. To this end, minimize the components and traces that cut this layer.

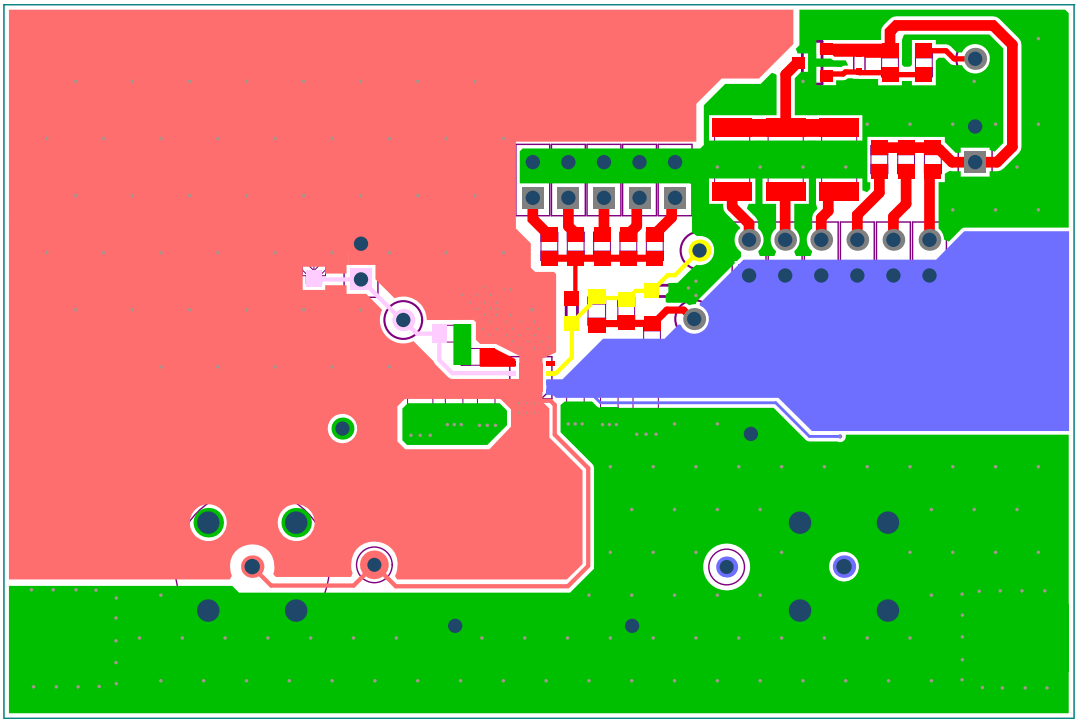


Figure 27. Layout Scheme - DFN

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
RRP52999-NH0	52999	8Ld DFN3×3	L8.3x3M	Reel, 3k	-40°C to 125°C
RTKP52999DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. The Moisture Sensitivity Level (MSL) is 1. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.03	Apr 24, 2026	Updated the typical values for the Load Regulation, Dropout Voltage, Ground Current, and EN Leakage Current specs.
1.02	Apr 10, 2026	In Electrical Specifications, updated the parameter Short Circuit Current Limit.
1.01	Mar 20, 2026	Added ECAD Information.
1.00	Jan 8, 2026	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRP52999-NH0	8	DFN	L8.3x3M / DV0008AF

A.2 Symbol Pin Information

A.2.1 8-DFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	VOUT	Power	-
2	VOUT	Power	-
3	ADJ	Input	-
4	NC	Passive	-
5	GND	Power	-
6	EN	Input	-
7	VIN	Power	-
8	VIN	Power	-
EPAD9	GND	Power	-

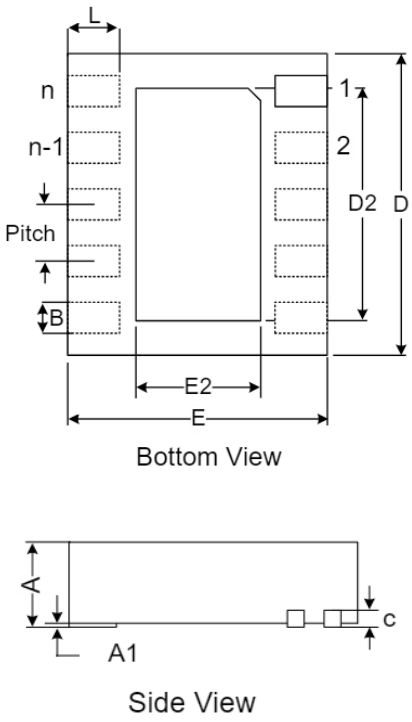
A.3 Symbol Parameters

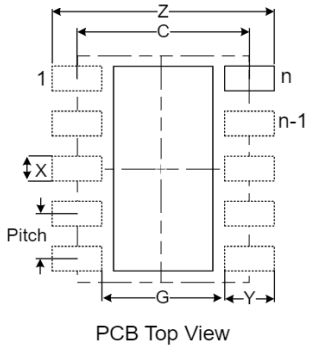
Orderable Part Number	Qualification	Mounting Type	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Min Output Voltage	Max Output Voltage	RoHS
RRP52999-NH0	Industrial	SMD	-40 °C	125 °C	- 20 V	-2.5 V	-18 V	-1.2 V	Compliant

A.4 Footprint Design Information

A.4.1 8-DFN

IPC Footprint Type	Package Code/ POD Number	Number of Pins
DFN	L8.3x3M / DV0008AF	8

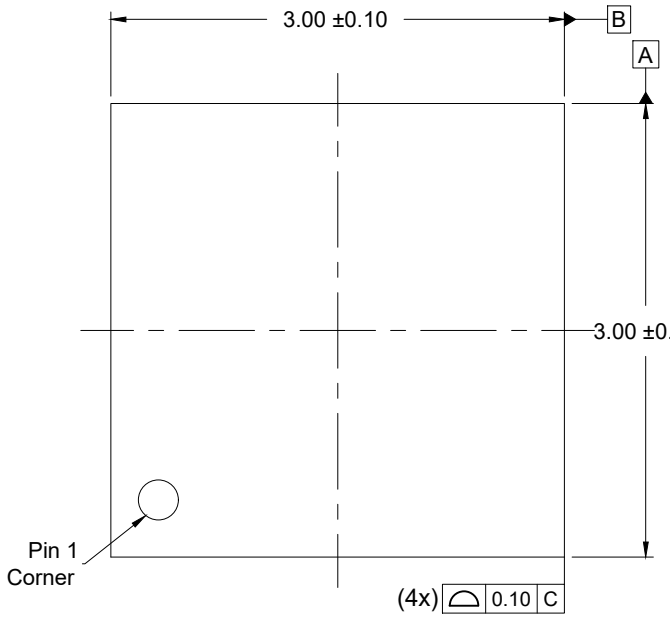
Description	Dimension	Value (mm)	Diagram[1]
Minimum body span (vertical side)	Dmin	2.90	
Maximum body span (vertical side)	Dmax	3.10	
Minimum body span (horizontal side)	Emin	2.90	
Maximum body span (horizontal side)	Emax	3.10	
Minimum Lead Width	Bmin	0.25	
Maximum Lead Width	Bmax	0.35	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.45	
Number of pins	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.65	
Minimum thermal pad size (vertical side)	D2min	1.95	
Maximum thermal pad size (vertical side)	D2max	2.05	
Minimum thermal pad size (horizontal side)	E2min	1.60	
Maximum thermal pad size (horizontal side)	E2max	1.70	
Comma separated list showing absent pins. Example: 1,2,5. If blank all pins present.	AbsentPins	-	
Comma-separated pin order. If blank, defaults to sequential (1 to PinCount). Example: 8,7,6,5,4,3,2,1 reverses an 8-pin package.	PinOrder	1,2,3,4,5,6,7,8	
Maximum Height	Amax	1.00	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.153	
Maximum Lead Thickness	cmax	0.253	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram[1]**
Row spacing. Distance between pad centres	C	2.80	
Distance between pads. Measured from outside edges	Z	3.40	
Distance between pads. Measured from inside edges	G	2.20	
Pad Width	X	0.30	
Pad Length	Y	0.60	

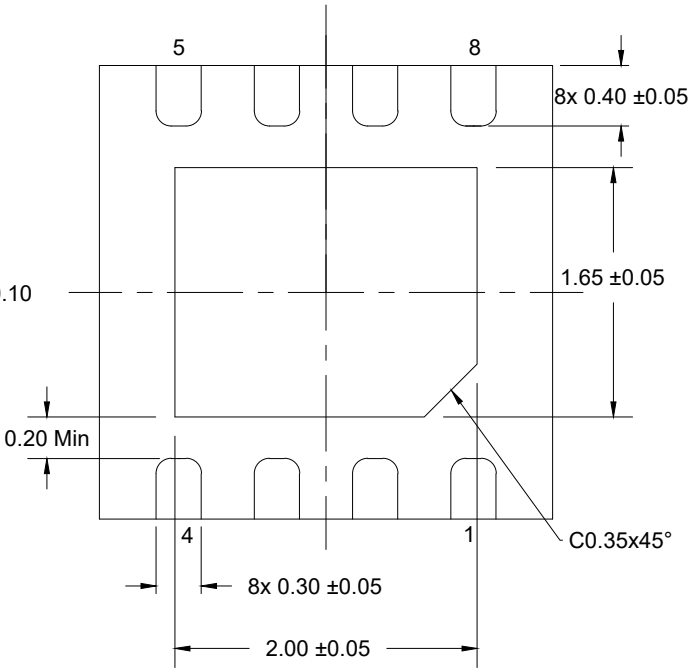
1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

Package Outline Drawing

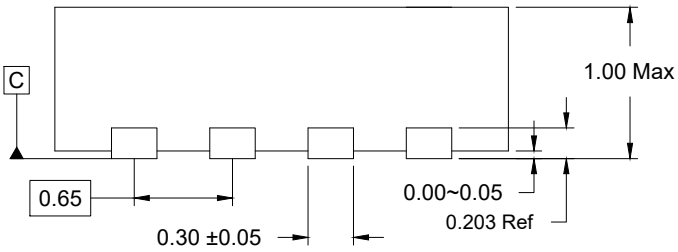
L8.3x3M
DV0008AF
8-DFN 3.0 x 3.0 x 1.00 mm Body, 0.65 mm Pitch Epad 2.0 x .65 mm
Rev.02, Apr 10, 2026



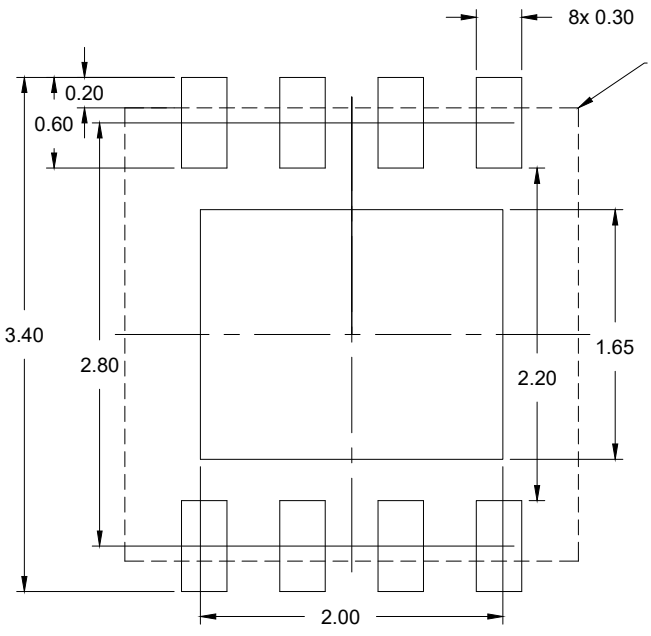
Top View



Bottom View



Side View



Recommended Land Pattern

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm tolerance for all other dimensions.
4. Numbers in ( ) are for reference only.

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