RRA79001, RRA79002, RRA79004

Low-Power, RRIO, 1MHz Operational Amplifiers

Description

The RRA79001, RRA79002, and RRA79004 represent the single, dual, and quad-channel lineup of low-power operational amplifiers designed for modern, space-conscious electronics. With rail-to-rail input and output swing, these op amps deliver exceptional performance in tight quarters, making them ideal for smoke detectors, wearable tech, and compact appliances where low-voltage operation and robust capacitive-load driving are essential.

Built on a rugged, streamlined architecture, the RRA7900x family simplifies circuit design without compromising performance. Each device features:

- Unity-gain stability for dependable operation
- Integrated RFI/EMI rejection filters to shield against interference
- Consistent phase integrity, even under overdrive conditions

These op amps are rated for a wide temperature range of -40°C to +125°C, making them suitable for demanding industrial and consumer applications. Packaging options include a variety of formats, with the standout being the ultra-compact 2.00mm×2.00mm DFN-8, which is perfect for designs where every millimeter counts.

Part	Package	Body Size (nom)
RRA79001	SC70-5	1.25mm×2.00mm
	SOT-23-5	1.60mm×2.90mm
RRA79002	MSOP-8	3.00mm×4.90mm
	SOICN-8	3.90mm×4.90mm
	DFN-8	2.00mm×2.00mm
RRA79004	SOICN-14	3.90mm×8.65mm
	TSSOP-14	4.40mm×5.00mm

Features

- Single-supply operation: 1.8V to 5.5V
- Rail-to-rail input and output
- Low input offset voltage: ±0.4mV
- Gain bandwidth product: 1MHz
- Low broadband noise: 38nV/√Hz
- Low input bias current: 5pA
- Low supply current: 60µA/Ch
- Unity-gain stable
- Internal EMI filter
- Temperature range: -40°C to 125°C

Applications

- Sensor signal conditioning
- Power modules
- Active filters
- Low-side current sensing
- Smoke detectors
- Motion detectors
- Wearable devices
- Appliances
- EPOS systems
- Barcode scanners
- HVAC (heating, ventilation and air condition)
- Motor control

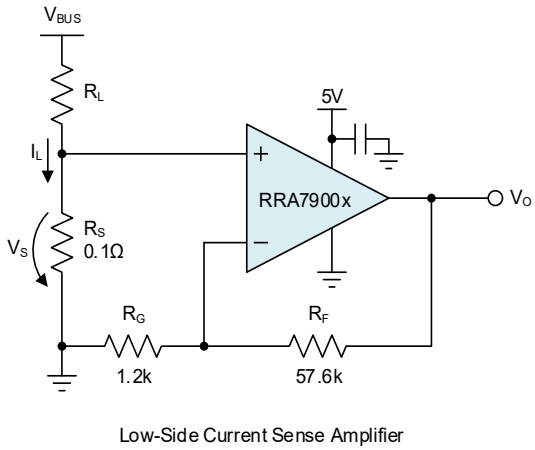


Figure 1. Typical Application Circuit

Contents

1. Pin Information

1.1 5-Pin SOT-23 Package

1.1.1 Pin Assignments

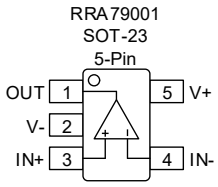


Figure 2. Pin Assignments – Top View

1.1.2 Pin Descriptions

Pin Name	Pin Number	Function
IN+	3	Non-Inverting Signal Input
IN-	4	Inverting Signal Input
OUT	1	Signal Output
V+	5	Positive Supply Voltage
V-	2	Negative Supply Voltage

1.2 5-Pin SC70 Package

1.2.1 Pin Assignments

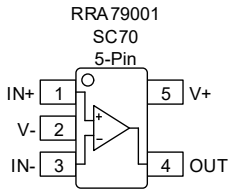


Figure 3. Pin Assignments – Top View

1.2.2 Pin Descriptions

Pin Name	Pin Number	Function
IN+	1	Non-Inverting Signal Input
IN-	3	Inverting Signal Input
OUT	4	Signal Output
V+	5	Positive Supply Voltage
V-	2	Negative Supply Voltage

1.3 8-Pin SOICN, DFN, MSOP Packages

1.3.1 Pin Assignments

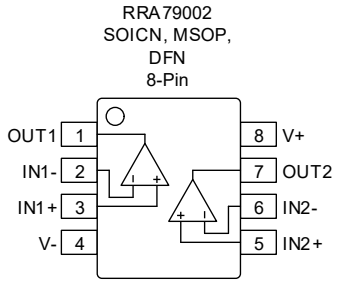


Figure 4. Pin Assignments – Top View

1.3.2 Pin Descriptions

Pin Name	Pin Number	Function
IN1+	3	Non-Inverting Signal Input
IN2+	5	
IN1-	2	Inverting Signal Input
IN2-	6	
OUT1	1	Signal Output
OUT2	7	
V+	8	Positive Supply Voltage
V-	4	Negative Supply Voltage
EPAD	-	Connect the EPAD to ground for temperature dissipation. (DFN Package Only)

1.4 14-Pin SOICN, TSSOP Packages

1.4.1 Pin Assignments

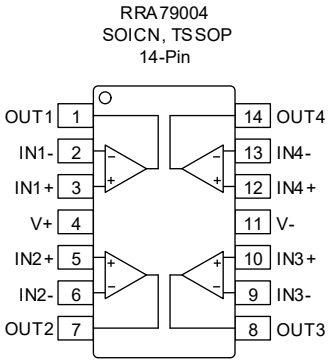


Figure 5. Pin Assignments – Top View

1.4.2 Pin Definitions

Pin Name	Pin Number	Function
IN1+	3	Non-Inverting Signal Input
IN2+	5	
IN3+	10	
IN4+	12	
IN1-	2	Inverting Signal Input
IN2-	6	
IN3-	9	
IN4-	13	
OUT1	1	Signal Output
OUT2	7	
OUT3	8	
OUT4	14	
V+	4	Positive Supply Voltage
V-	11	Negative Supply Voltage

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage, V+ to V-	-	6.0	V
Input Voltage, IN± to V-	(V-) – 0.5	(V+) + 0.5	V
Input Voltage, IN+ to IN-	-	6.0	V
Input Current	-	10	mA
Output Short-Circuit Current	Continuous		
Maximum Junction Temperature, T_J	-	150	°C
Storage Temperature, Tstg	-65	150	°C
RRA79001 ESD Ratings			
Human Body Model (Tested per JS-001-2024)	-	±3	kV
Charged-Device Model (CDM) (Tested per JS-002-2022)	-	±2	kV
Latch-Up (Tested per JESD78F), T_A = 125°C	-	100	mA
RRA79002 ESD Ratings			
Human Body Model (HBM) (Tested per JS-001-2023)	-	±2	kV
Charged-Device Model (CDM) (Tested per JS-002-2018)	-	±2	kV
Latch-Up (Tested per JESD78F), T_A = 125°C	-	100	mA
RRA79004 ESD Ratings			
Human Body Model (Tested per JS-001-2024)	-	±6	kV
Charged-Device Model (CDM) (Tested per JS-002-2022)	-	±1.5	kV
Latch-Up (Tested per JESD78F), T_A = 125°C	-	100	mA

2.2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage [(V+) - (V-)]	V_S	1.8	5.5	V
Input Voltage Range	V_I	(V-) – 0.1	(V+) + 0.1	V
Output Voltage Range	V_O	V-	V+	V
Ambient Temperature	T_A	-40	+125	°C

2.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	5 Ld SOT-23 Package	θ_{JA}[1]	Junction to ambient	209	°C/W
		θ_{JC}[2]	Junction to case	159	°C/W
Thermal Resistance	5 Ld SC70 Package	θ_{JA}[1]	Junction to ambient	243	°C/W
		θ_{JC}[2]	Junction to case	157	°C/W
Thermal Resistance	8 Ld SOICN Package	θ_{JA}[1]	Junction to ambient	140	°C/W
		θ_{JC}[2]	Junction to case	85	°C/W
Thermal Resistance	8 Ld MSOP Package	θ_{JA}[1]	Junction to ambient	170	°C/W
		θ_{JC}[2]	Junction to case	93	°C/W
Thermal Resistance	8 Ld 2x2 DFN Package	θ_{JA}[3]	Junction to ambient	87	°C/W
		θ_{JC}[4]	Junction to case	27	°C/W
Thermal Resistance	14 Ld SOICN Package	θ_{JA}[1]	Junction to ambient	92	°C/W
		θ_{JC}[2]	Junction to case	60	°C/W
Thermal Resistance	14 Ld TSSOP Package	θ_{JA}[1]	Junction to ambient	125	°C/W
		θ_{JC}[2]	Junction to case	58	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.
3. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
4. For θ_{JC}, is measured at the center of the exposed metal pad on the package underside.

2.4 Electrical Specifications

V_S = (V+) - (V-) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S/2, VCM = V_S/2 (unless otherwise noted)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
DC Parameters						
Input Offset Voltage	V_{OS}	V_S = 5V, V_{CM} = 2.5V	-	±0.4	±1.6	mV
		T_A = -40°C to 125°C	-	-	±2	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}	T_A = -40°C to 125°C	-	±0.6	-	µV/°C
Input Bias Current	I_B	-	-	±5	-	pA
Input Offset Current	I_{OS}	-	-	±2	-	pA
Common-Mode Input Range	V_{ICM}	V_S = 1.8V to 5.5V	(V_S-) - 0.1		(V_S+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_S = 5.5V, T_A = -40°C to 125°C (V-) - 0.1V < V_{CM} < (V+) +0.1V	65	100	-	dB
Power Supply Rejection Ratio	PSRR	V_S = 1.8V to 5.5V, V_{CM} = (V-)	80	100	-	dB
Open Loop Gain	A_{OL}	(V-) + 50mV < V_O < (V+) – 50mV, R_L = 10kΩ	105	120	-	dB
Output Voltage Swing from Rails	V_{OFR+}	V_S = ±2.75V, R_L = 10kΩ	-	-	20	mV
	V_{OFR-}		-	-	20	mV
Sourcing Short-Circuit Current	I_{SC+}	V_{OUT} connected to V-	-	40	-	mA
Sinking Short-Circuit Current	I_{SC-}	V_{OUT} connected to V+	-	-40	-	mA
Supply Current per Amplifier	I_Q	R_L = ∞	-	60	78	µA
AC Parameters						
Differential Input Capacitance	C_D	-	-	1.4	-	pF
Common-mode Input Capacitance	C_{CM}	-	-	3	-	pF
Open-Loop Output Impedance	Z_O	f = 1MHz	-	1400	-	Ω

V_S = (V+) - (V-) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S/2, VCM = V_S/2 (unless otherwise noted) (Cont.)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Input Noise Voltage	E_n	f = 0.1 to 10Hz	-	5	-	μV_{P-P}
Voltage Noise Density	e_n	f = 1kHz	-	38	-	nV/√Hz
Current Noise Density	i_n	f = 1kHz	-	7	-	fA/√Hz
Total Harmonic Distortion	THD	V_S = 5.5V, V_{CM} = V_S/2, V_{OUT} = $1V_{RMS}$, G = 1, f = 1kHz	-	0.0029	-	%
Gain Bandwidth Product	GBW	R_L = 10kΩ	-	1	-	MHz
Phase Margin	Φ_m	R_L = 10kΩ	-	60	-	deg
Transient Response						
Slew Rate	SR	G = 1, V_{OUT} = 1V to 4V	-	2.5	-	V/µs
Settling Time to 0.1% V_O	t_S	V_S = ±2.5V, G = 1, 2V-Step, C_L = 100pF	-	2.5	-	µs
Overload Recovery Time	t_{OR}	V_S = 5V, V_{IN} x G > V_S	-	1	-	µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Typical Characteristics

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted)

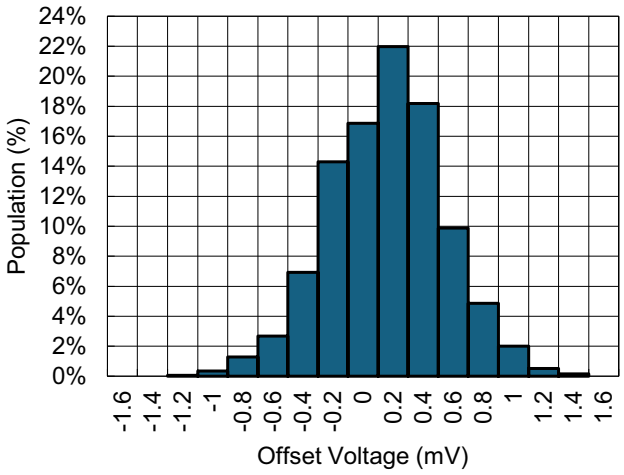


Figure 6. Offset Voltage Distribution Histogram

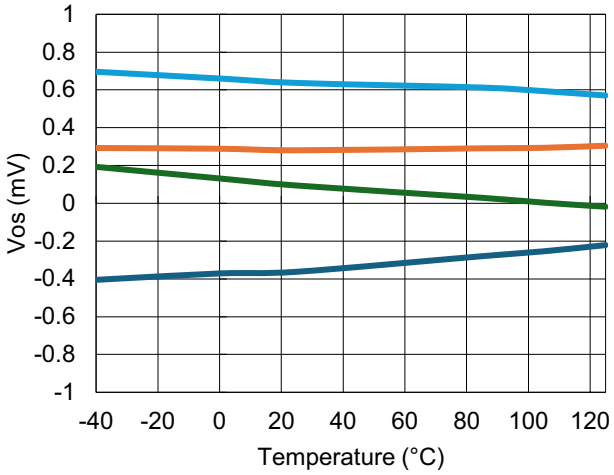


Figure 7. Offset Voltage vs Temperature

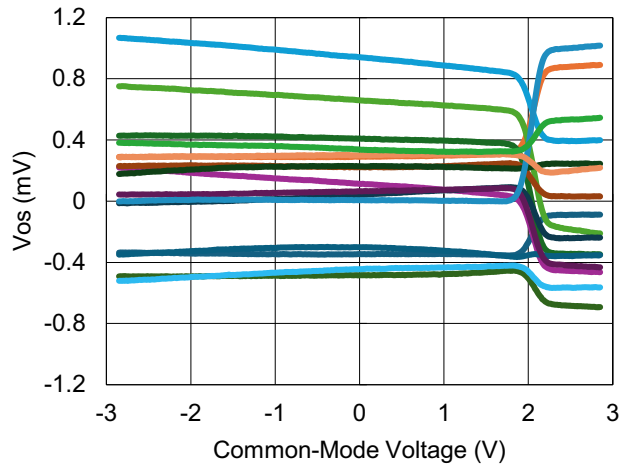


Figure 8. Offset Voltage vs Common-Mode Voltage

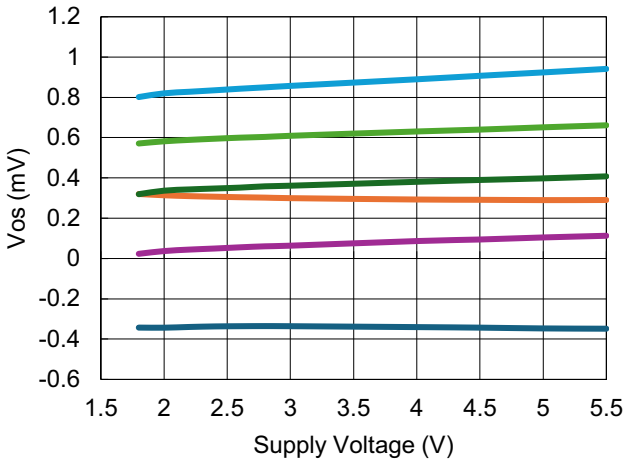


Figure 9. Offset Voltage vs Supply Voltage

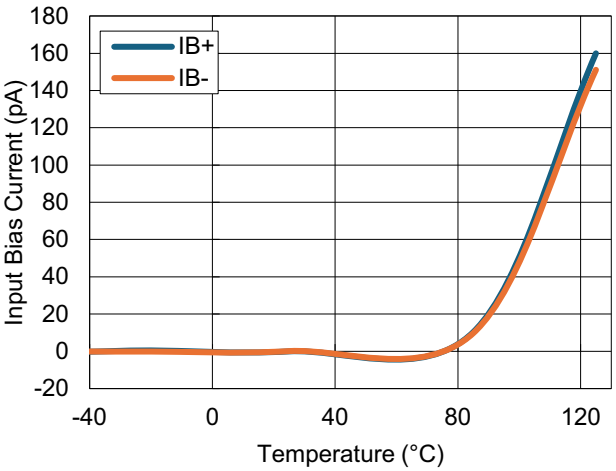


Figure 10. Input Bias Current vs Temperature

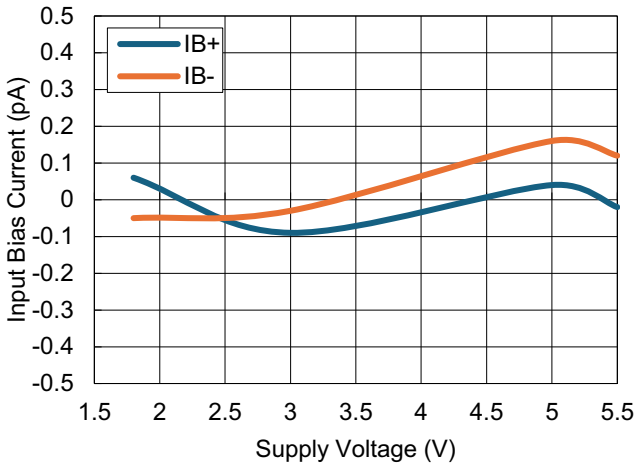


Figure 11. Input Bias Current vs Supply Voltage

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted) (Cont.)

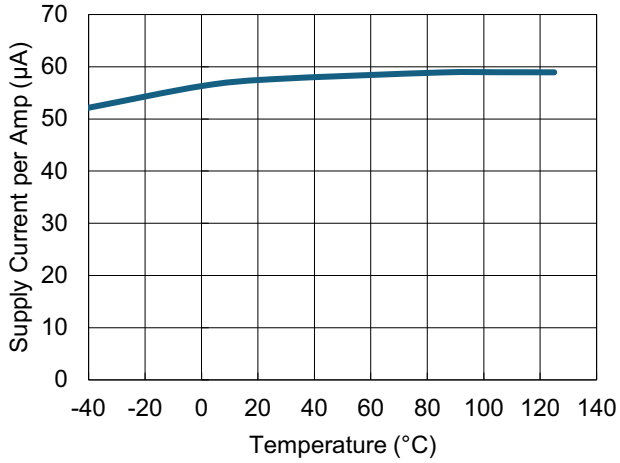


Figure 12. Quiescent Current vs Temperature

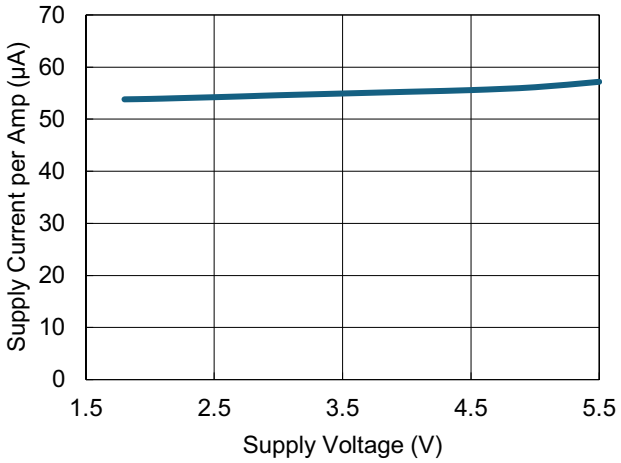


Figure 13. Quiescent Current vs Supply Voltage

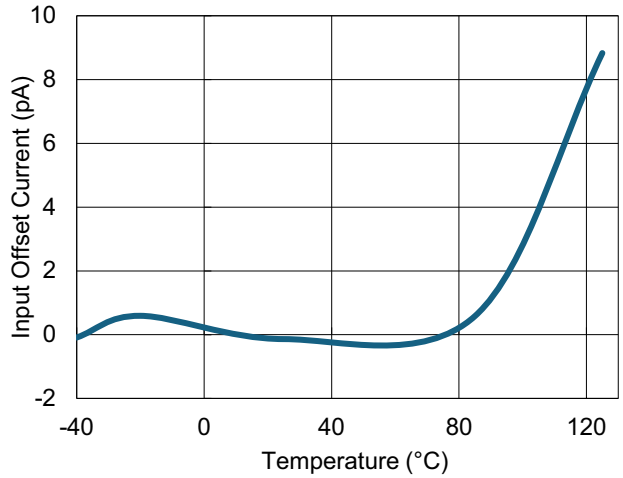


Figure 14. Input Offset Current vs Temperature

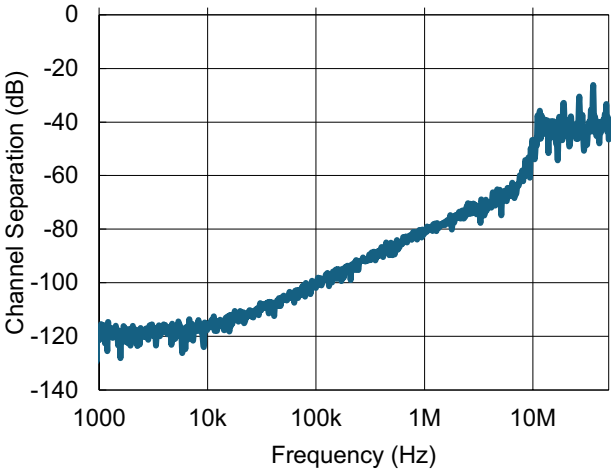


Figure 15. Channel Separation

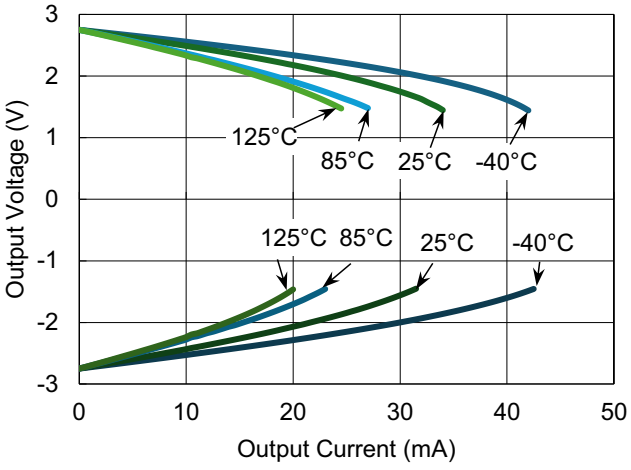


Figure 16. Output Voltage Swing vs Output Current

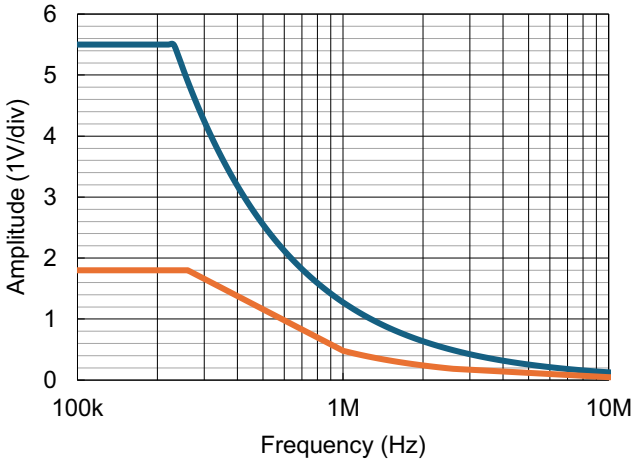


Figure 17. Maximum Output Voltage vs Frequency

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted) (Cont.)

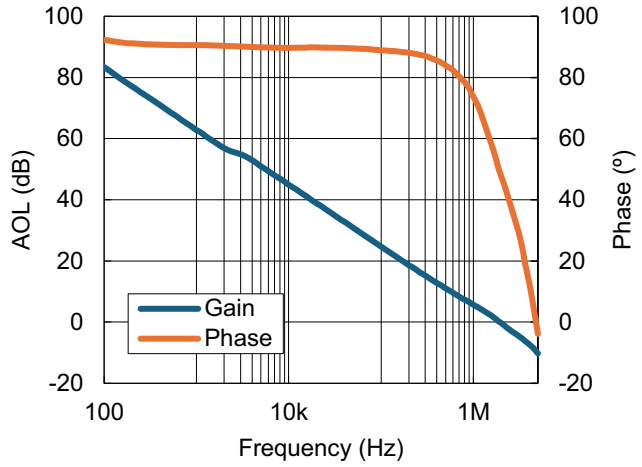


Figure 18. Open-Loop Gain and Phase vs Frequency

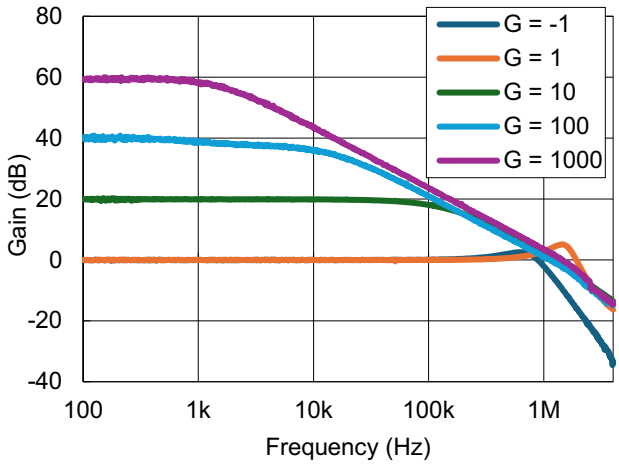


Figure 19. Closed-Loop Gain vs Frequency

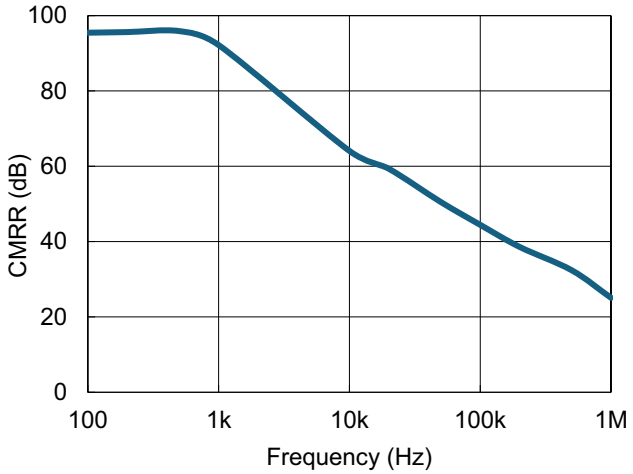


Figure 20. Common-Mode Rejection Ratio (CMRR) vs Frequency

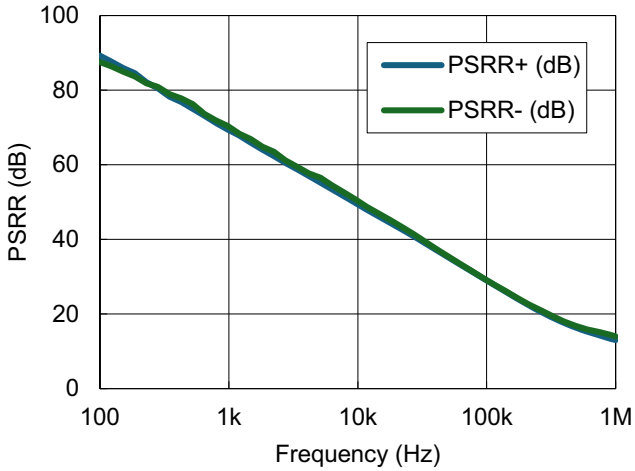


Figure 21. Power Supply Rejection Ratio (PSRR) vs Frequency

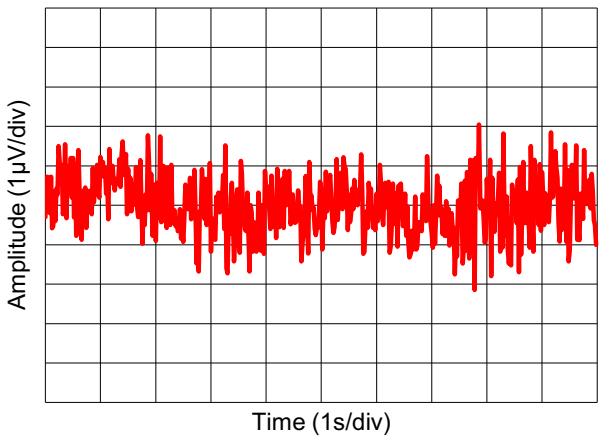


Figure 22. 0.1Hz to 10Hz Voltage Noise

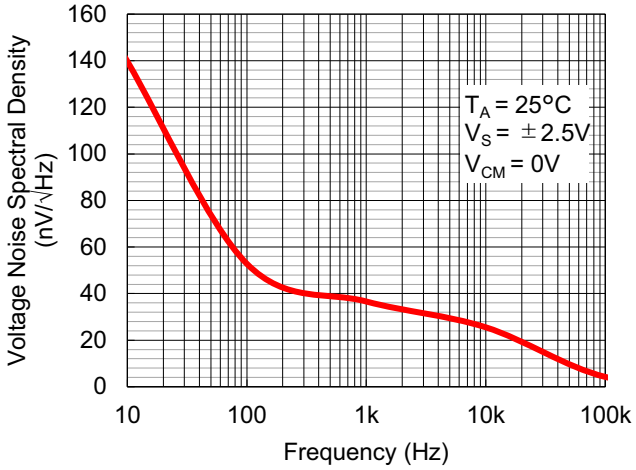


Figure 23. Voltage Noise Spectral Density vs Frequency

V_S = 5.5V (±2.75V) at T_A = 25°C, R_L =10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted) (Cont.)

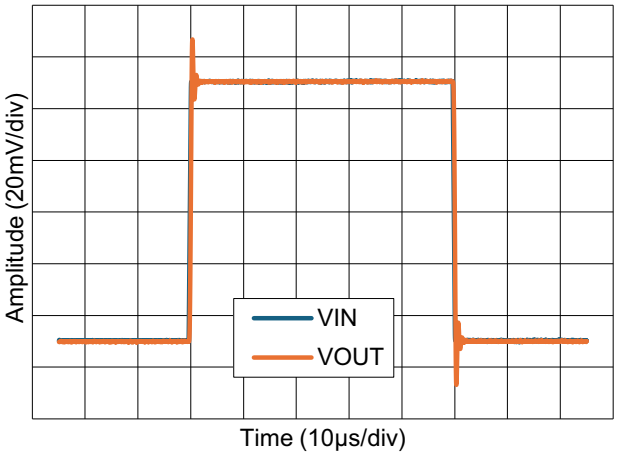


Figure 24. Small Signal Step Response

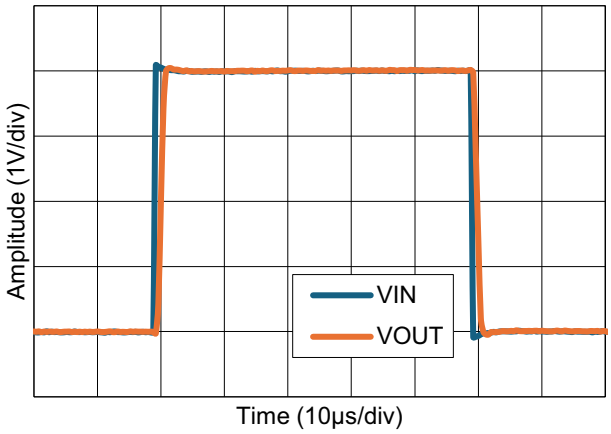


Figure 25. Large Signal Step Response

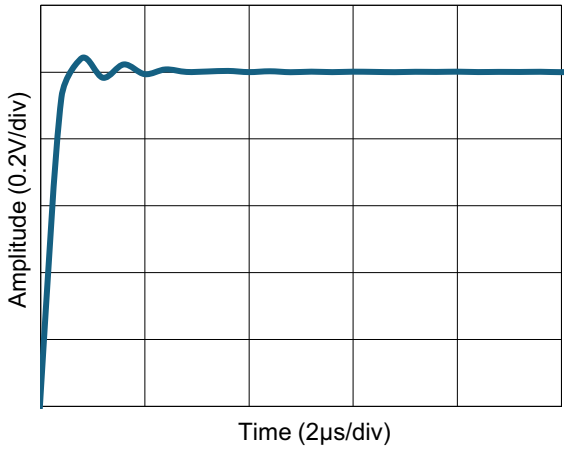


Figure 26. Settling Time Positive

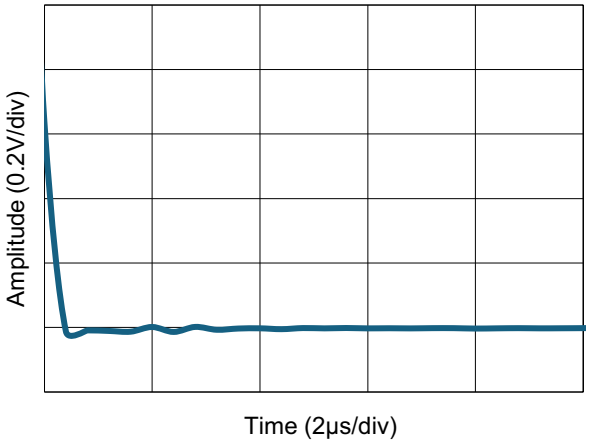


Figure 27. Figure 23. Settling Time Negative

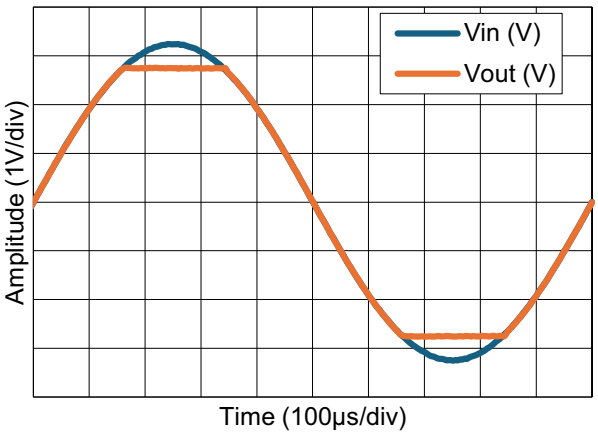


Figure 28. No Phase Reversal

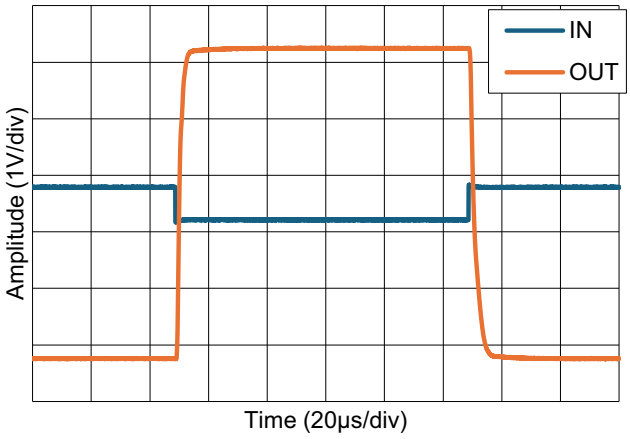


Figure 29. Overload Recovery

4. Detailed Description

4.1 Overview

The RRA7900x family of operational amplifiers are low-power devices with rail-to-rail input and outputs. These op amps operate from supply voltages as low as 1.8V up to 5.5V. The devices are unity-gain stable and designed for a wide range of general-purpose applications.

Their input common-mode voltage range extends 100mV above and below the power supply voltage rails, which allows the devices to be used in any single-supply application. The output stage can swing to within 20mV of the supply rails with a 10kΩ load.

The rail-to-rail input and output swing capability increases the signal dynamic range, which is highly beneficial in low-supply applications.

4.2 Feature Description

4.2.1 Rail-To-Rail Input

The input common-mode voltage range of the RRA7900x family extends 100mV beyond both supply rails for the full supply voltage range of 1.8V to 5.5V. This performance is accomplished with complementary input stages, consisting of an N-channel input differential pair in parallel with a P-channel differential input pair (Figure 30).

Figure 30 shows the N-channel pair being active for input voltages close to the positive rail, typically (V+) – 1V to (V+) + 0.1V, while the P-channel pair is active for inputs from (V-) - 0.1V to about (V+) – 0.8V. Within the small transition region of 0.2V, where both pairs are active, PSRR, CMRR, VOS, and THD can slightly degrade from their values outside this region.

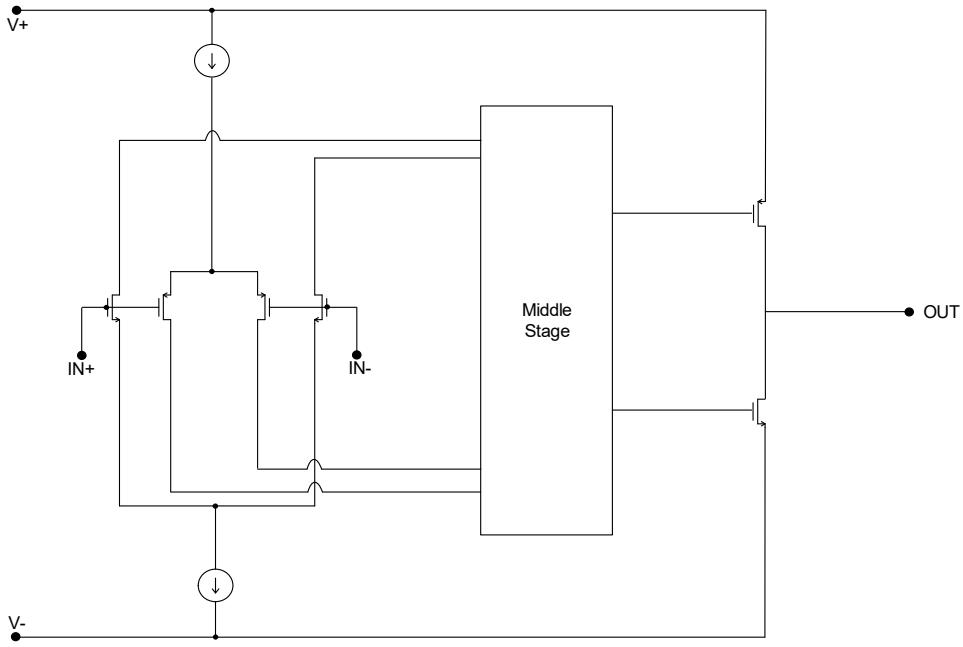


Figure 30. Block Diagram of a Single Amplifier Stage

4.2.2 Rail-To-Rail Output

The RRA7900x family delivers robust output drive capability. A class AB output stage with common-source transistors provides full rail-to-rail output swing capability. For resistive loads of 10kΩ, the output swings to within 20mV of either supply rail, regardless of the applied supply voltage. Heavier load conditions, however, cause the amplifier to swing less close to the supply rails.

4.2.3 EMI Filter

The RRA7900x possess internal electromagnetic interference (EMI) filtering to reduce the effects of EMI from external sources such as wireless communications and densely populated circuit boards with a mix of analog and digital components. EMI immunity can be improved with circuit design techniques; RRA7900x has been quantified for the immunity over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 31 shows the results of this test on RRA7900x.

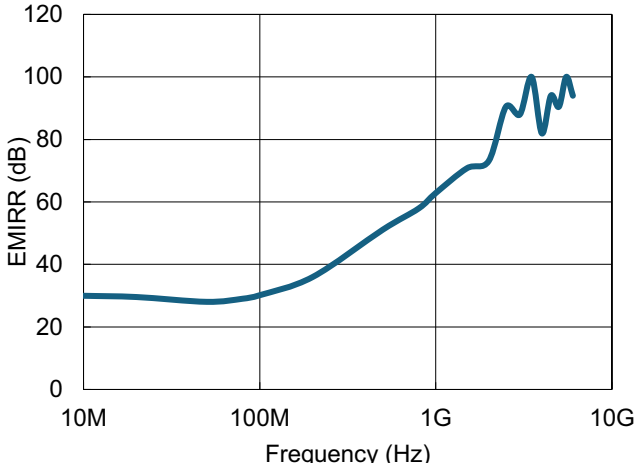


Figure 31. EMIRR vs Frequency

4.2.4 Overload Recovery

Overload recovery is defined as the time required for the op amp output to return from a saturated state to the linear state. The op amp output saturates when the output voltage exceeds the applied supply voltage because of a high input voltage or a high gain setting. After entering saturation, charge carriers in the output stage require time to return to the linear operating region. Only then does the device begin to slew at the specified slew rate.

Therefore, the propagation delay during an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the RRA7900x family is less than 1µs.

4.2.5 Input and Output ESD Protection

The RRA7900x family incorporates internal ESD protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes that are connected between the input and output pins and the power-supply pins. If the input voltage is expected to exceed the specified value in the absolute maximum ratings, insert a series resistor, R_S, which limits the input current to about 1 to 10mA (Figure 32).

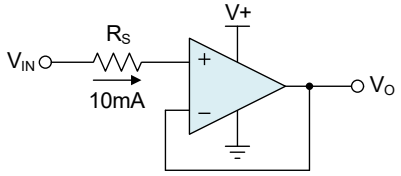


Figure 32. Input Current Protection

5. Application Information

The RRA7900x family of low-power, rail-to-rail input and output operational amplifiers are specifically designed for portable applications. The devices operate from 1.8V to 5.5V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10kΩ loads connected to any point between V+ and V–. The input common-mode voltage range includes both rails and allows the devices to be used in any single-supply application.

5.1 Typical Applications

5.1.1 High Gain, Precision DC-Coupled Amplifier

Figure 33 shows one channel of the RRA7900x configured in a low-side current sensing application.

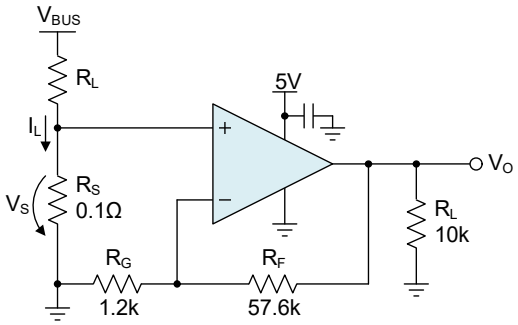


Figure 33. RRA79001 in a Low-Side, Current-Sensing Application

5.1.2 Design Procedure

The following are the design requirements for this design.

- Maximum Load current: I_L = 0 to 1A
- Output range: V_O = 4.9V
- Maximum sense voltage: $V_{S\text{-}max}$ = 100mV

To ensure that at maximum input current, the maximum sense or input voltage is present, use Equation 1 to calculate the sense resistor value.

(EQ. 1) $$R_S = \frac{V_{IN\text{-}max}}{I_{L\text{-}max}} = \frac{0.1V}{1A} = 0.1\Omega$$

To ensure that at the maximum sense voltage, the maximum output voltage is reached, use Equation 2 to calculate the circuit gain.

(EQ. 2) $$G = \frac{V_O}{V_{IN}} = \frac{4.9V}{0.1V} = 49V/V$$

The circuit gain is set by the feedback and gain resistors using $G = 1 + R_F/R_G$, therefore, solving for the resistor ratio gives:

(EQ. 3) $$\frac{R_F}{R_G} = G - 1 = 48V/V$$

Making R_F = 57.6kΩ and R_G = 1.2kΩ yields a gain of 49.

Figure 34 shows the V-I characteristic of the above circuit.

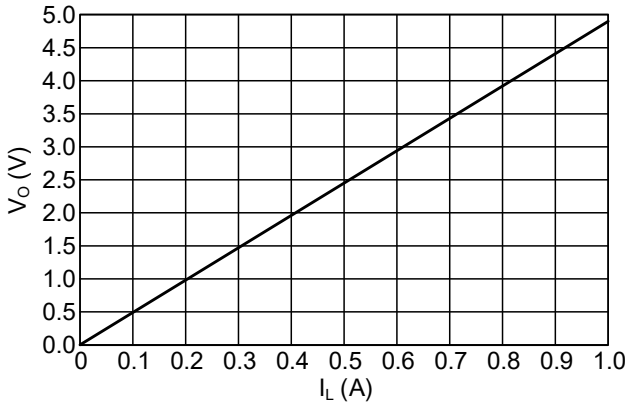


Figure 34. Output Voltage vs Load Current Characteristic

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

Part Number[1]	# Channels	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	MSL Rating[2]	Carrier Type[3]	Temp. Range
RRA79001-QAJ	1	901[4]	5 Ld SC70	P5.049	1	Reel, 3k units	-40 to 125°C
RRA79001-P3J	1	7901[4]	5 Ld SOT-23	P5.064	1	Reel, 3k units	-40 to 125°C
RRA79002-SPH	2	79002 SPH	8 Ld SOICN	M8.15	3	Reel, 2.5k units	-40 to 125°C
RRA79002-SNH	2	79002	8 Ld MSOP	M8.118D	1	Reel, 2.5k units	-40 to 125°C
RRA79002-NSH	2	902	8 Ld 2x2 DFN	L8.2x2F	1	Reel, 1k units	-40 to 125°C
RRA79004-SLH	4	79004 SLH	14 Ld SOICN	M14.15	3	Reel, 2.5k units	-40 to 125°C
RRA79004-SKH	4	79004 SKH	14 Ld TSSOP	M14.173	1	Reel, 2.5k units	-40 to 125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For more information about Moisture Sensitivity Level (MSL), see TB363.
3. See TB347 for details about reel specifications.
4. The part marking is located on the bottom of the part.

8. Revision History

Revision	Date	Description
1.03	Dec 18, 2025	Added RAA79004 information throughout.
1.02	Oct 7, 2025	Updated Figure 1. Corrected units on feature bullet. Updated EPAD pin description. Updated EPAD pin name in ECAD section.
1.01	Sep 17, 2025	Added RAA79001 information throughout. Added more package options for RAA79002. Updated test condition for Gain Bandwidth Product. Updated Rail-To-Rail Input section. Updated ordering information.
1.00	Jul 21, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRA79001-QAJ	5	SC70	P5.049
RRA79001-P3J	5	SOT-23	P5.064
RRA79002-SPH	8	SOICN	M8.15
RRA79002-SNH	8	MSOP	M8.118D
RRA79002-NSH	8	DFN	L8.2x2F
RRA79004-SLH	14	SOICN	M14.15
RRA79004-SKH	14	TSSOP	M14.173

A.2 Symbol Pin Information

A.2.1 5-SC70

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	IN+	Input	-
2	V-	Power	-
3	IN-	Input	-
4	OUT	Output	-
5	V+	Power	-

A.2.2 5-SOT-23

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT	Output	-
2	V-	Power	-
3	IN+	Input	-
4	IN-	Input	-
5	V+	Power	-

A.2.3 8-SOICN/MSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Output	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V-	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Output	-
8	V+	Power	-

A.2.4 8-DFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Output	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V-	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Output	-
8	V+	Power	-
EPAD9	V-	Power	

A.2.5 14-SOICN/TSSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Output	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V+	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Output	-
8	OUT3	Output	-
9	IN3-	Input	-
10	IN3+	Input	-
11	V-	Power	-
12	IN4+	Input	-
13	IN4-	Input	-
14	OUT4	Output	-

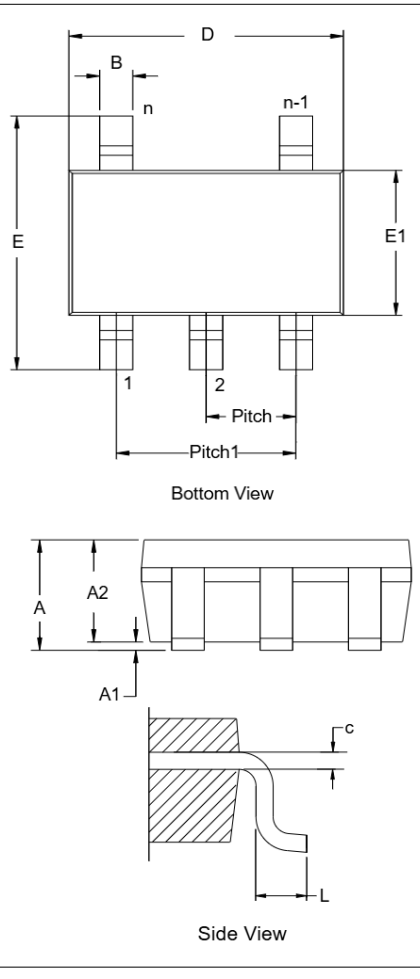
A.3 Symbol Parameters

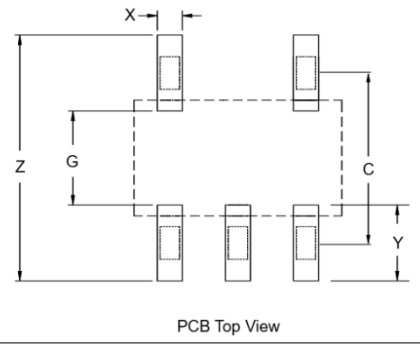
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Supply Voltage	Max Supply Voltage	Number of Channels	Slew Rate	Operating Supply Current	Input Offset Voltage (V_{OS})
RRA79001-QAJ	Industrial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	1	2.5 V/µs	60 µA	±0.4 mV
RRA79001-P3J	Industrial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	1	2.5 V/µs	60 µA	±0.4 mV
RRA79002-SPH	Industrial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	2	2.5 V/µs	60 µA	±0.4 mV
RRA79002-SNH	Industrial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	2	2.5 V/µs	60 µA	±0.4 mV
RRA79002-NSH	Industrial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	2	2.5 V/µs	60 µA	±0.4 mV
RRA79004-SLH	Industrial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	4	2.5 V/µs	60 µA	±0.4 mV
RRA79004-SKH	Industrial	SMD	Compliant	-40 °C	125 °C	1.8 V	5.5 V	4	2.5 V/µs	60 µA	±0.4 mV

A.4 Footprint Design Information

A.4.1 5-SC70

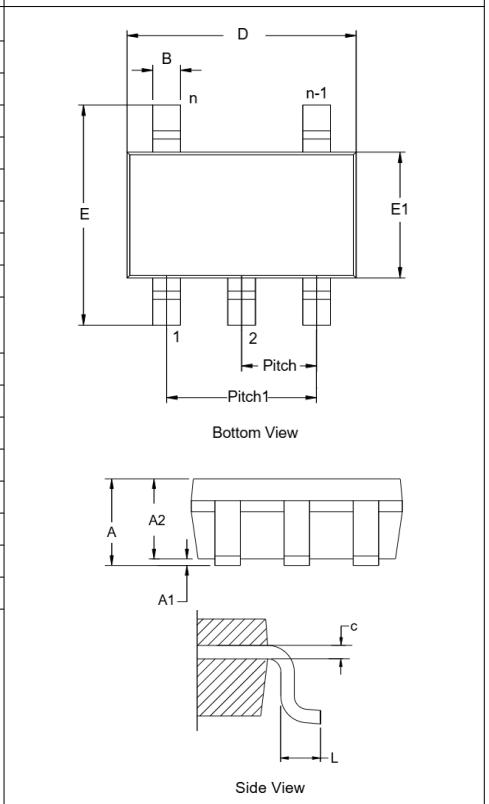
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SC70	P5.049/KA0005AA	5

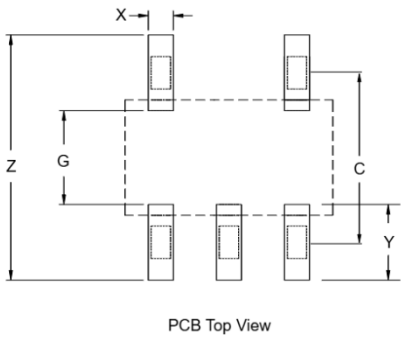
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	1.85	
Maximum body span (vertical side)	Dmax	2.15	
Minimum lead span (horizontal side)	Emin	1.80	
Maximum lead span (horizontal side)	Emax	2.40	
Minimum lead width	Bmin	0.15	
Maximum lead width	Bmax	0.30	
Minimum body width (horizontal side)	E1min	1.15	
Maximum body width (horizontal side)	E1max	1.35	
Number of leads: 3, 4, 5 or 6	PinCount	5	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5	
Distance between the center of any two adjacent pins	Pitch	0.65	
Overall pitch (e1)	Pitch1	1.30	
Maximum Height	Amax	1.10	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.00	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.22	
Minimum Lead Length	Lmin	0.26	
Maximum Lead Length	Lmax	0.46	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between pads. Measured from outside edges	Z	2.85	
Distance between pads. Measured from inside edges	G	1.35	
Pad width	X	0.40	
Pad length	Y	0.75	
Row spacing. Distance between pad centers	C	2.10	

A.4.2 5-SOT23

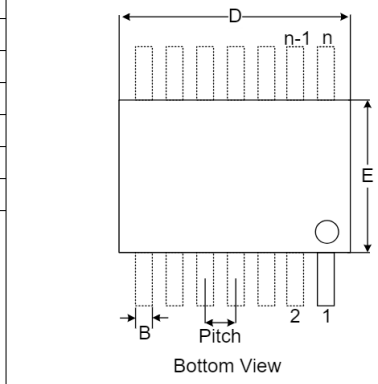
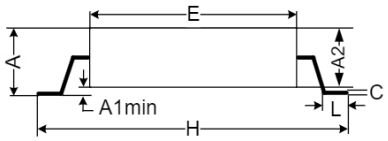
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOT23	P5.064/KA0005AB	5

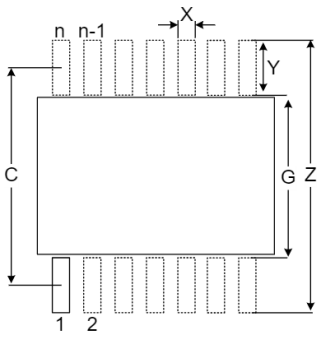
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	2.80	
Maximum body span (vertical side)	Dmax	3.00	
Minimum lead span (horizontal side)	Emin	2.60	
Maximum lead span (horizontal side)	Emax	3.00	
Minimum lead width	Bmin	0.30	
Maximum lead width	Bmax	0.50	
Minimum body width (horizontal side)	E1min	1.50	
Maximum body width (horizontal side)	E1max	1.70	
Number of leads: 3, 4, 5 or 6	PinCount	5	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5	
Distance between the center of any two adjacent pins	Pitch	0.95	
Overall pitch (e1)	Pitch1	1.90	
Maximum Height	Amax	1.45	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.30	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	022	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.55	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between pads. Measured from outside edges	Z	3.60	
Distance between pads. Measured from inside edges	G	1.20	
Pad width	X	0.60	
Pad length	Y	1.20	
Row spacing. Distance between pad centers	C	2.40	

A.4.3 8-SOICN

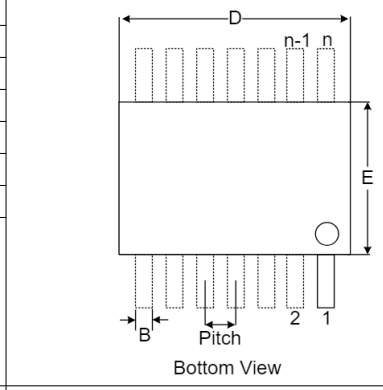
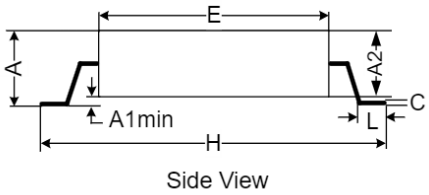
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOIC	M8.15/GS0008AC	8

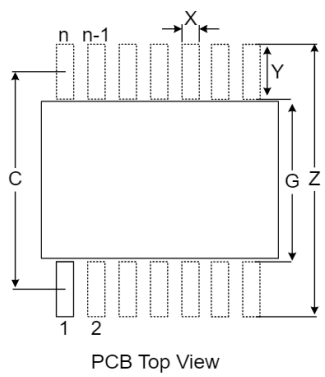
Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	5.80	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.20	
Minimum body span (horizontal side)	Dmin	4.80	
Maximum body span (horizontal side)	Dmax	5.00	
Minimum body span (vertical side)	Emin	3.80	
Maximum body span (vertical side)	Emax	4.00	
Minimum Lead Width	Bmin	0.33	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	 Side View
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	1.27	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.40	 PCB Top View
Distance between left pad heel to right pad heel.	G	3.00	
Row spacing. Distance between pad centers	C	5.20	
Pad Width	X	0.60	
Pad Length	Y	2.20	

A.4.4 8-MSOP

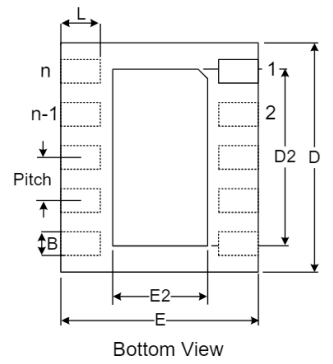
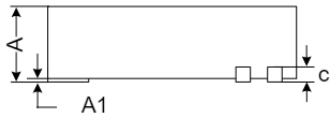
IPC Footprint Type	Package Code/ POD number	Number of Pins
SOP	M8.118D/HV0008AC	8

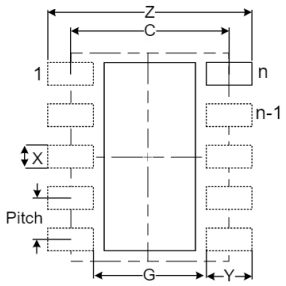
Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	4.70	
Maximum lead span (horizontal side)	Hmax	5.10	
Minimum body span (horizontal side)	Dmin	2.90	
Maximum body span (horizontal side)	Dmax	3.10	
Minimum body span (vertical side)	Emin	2.90	
Maximum body span (vertical side)	Emax	3.10	
Minimum Lead Width	Bmin	0.22	
Maximum Lead Width	Bmax	0.40	
Minimum Lead Length	Lmin	0.40	
Maximum Lead Length	Lmax	0.80	
Maximum Height	Amax	1.10	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.23	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.65	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	5.50	
Distance between left pad heel to right pad heel.	G	3.10	
Row spacing. Distance between pad centers	C	4.30	
Pad Width	X	0.32	
Pad Length	Y	1.20	

A.4.5 8-DFN

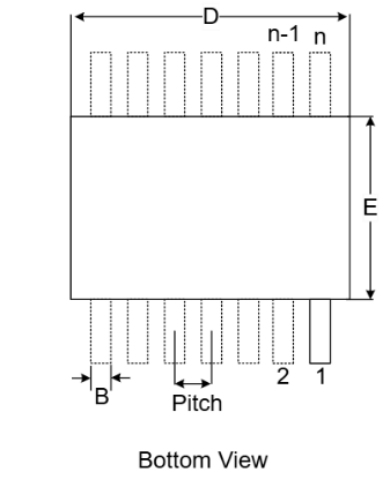
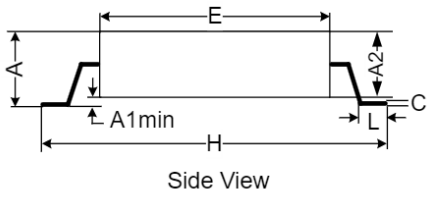
IPC Footprint Type	Package Code/ POD Number	Number of Pins
DFN	L8.2x2F	8

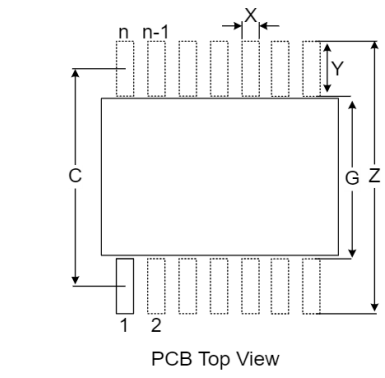
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	1.90	 Bottom View
Maximum body span (vertical side)	Dmax	2.10	
Minimum body span (horizontal side)	Emin	1.90	
Maximum body span (horizontal side)	Emax	2.10	
Minimum Lead Width	Bmin	0.20	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.25	
Maximum Lead Length	Lmax	0.35	
Maximum Height	Amax	0.80	
Minimum Standoff Height	A1min	0.00	 Side View
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	
Number of pins	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.50	
Minimum thermal pad size (vertical side)	D2min	1.50	
Maximum thermal pad size (vertical side)	D2max	1.70	
Minimum thermal pad size (horizontal side)	E2min	0.80	
Maximum thermal pad size (horizontal side)	E2max	1.00	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Row spacing. Distance between pad centres	C	1.85	 PCB Top View
Distance between pads. Measured from outside edges	Z	2.30	
Distance between pads. Measured from inside edges	G	1.40	
Pad Width	X	0.25	
Pad Length	Y	0.45	

A.4.6 14-SOICN

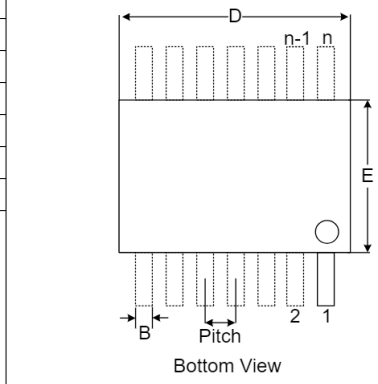
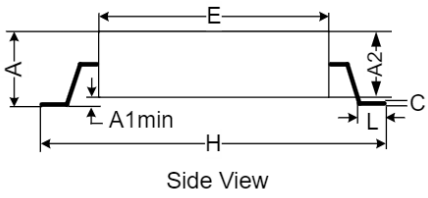
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOIC	M14.15	14

Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	5.95	
Maximum lead span (horizontal side)	Hmax	6.05	
Minimum body span (pin1 side)	Dmin	8.55	
Maximum body span (pin1 side)	Dmax	8.75	
Minimum body span	Emin	3.80	
Maximum body span	Emax	4.00	
Minimum Lead Width	Bmin	0.31	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	1.27	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	6.60	
Distance between left pad heel to right pad heel.	G	4.20	
Row spacing. Distance between pad centers	C	5.40	
Pad Width	X	0.41	
Pad Length	Y	1.20	

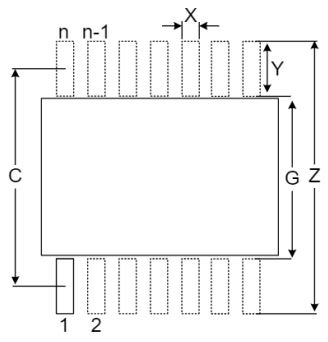
A.4.7 14-TSSOP

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M14.173	14

Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	6.30	
Maximum lead span (horizontal side)	Hmax	6.50	
Minimum body span (horizontal side)	Dmin	4.90	
Maximum body span (horizontal side)	Dmax	5.10	
Minimum body span (vertical side)	Emin	4.30	
Maximum body span (vertical side)	Emax	4.50	
Minimum Lead Width	Bmin	0.20	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	0.65	

Bottom View

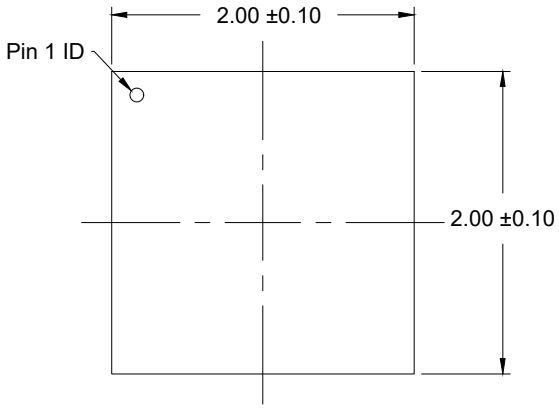
Side View

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.0	
Distance between left pad heel to right pad heel.	G	4.60	
Row spacing. Distance between pad centers	C	5.80	
Pad Width	X	0.25	
Pad Length	Y	1.20	

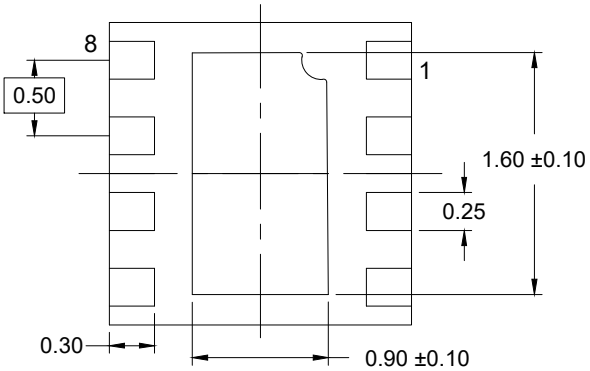
PCB Top View

Package Outline Drawing

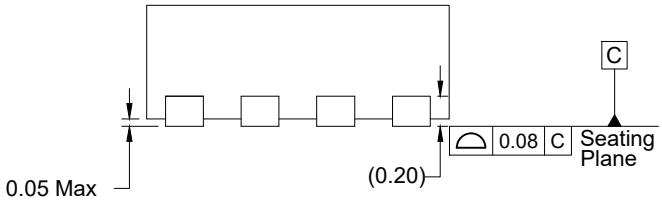
L8.2x2F
DW0008AA
8-DFN 2.0 x2.0 x 0.8 mm Body, 0.50mm Pitch
Rev 00, Jan 21, 2025



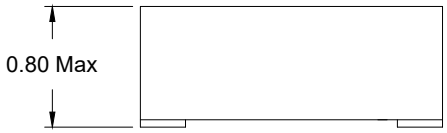
Top View



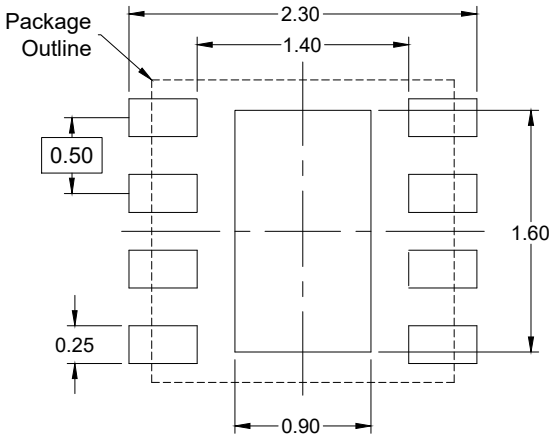
Bottom View



Side View (Rotated 90°)



Side View



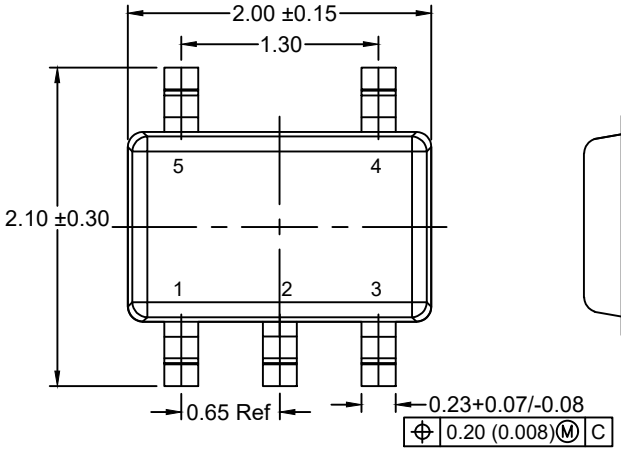
Recommende Land Pattern

Notes:

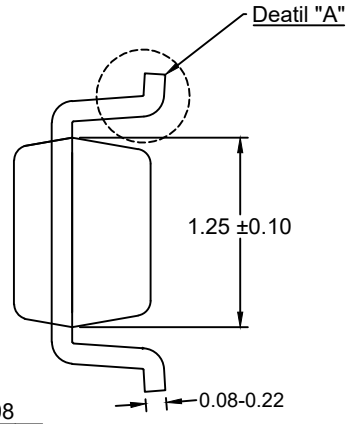
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

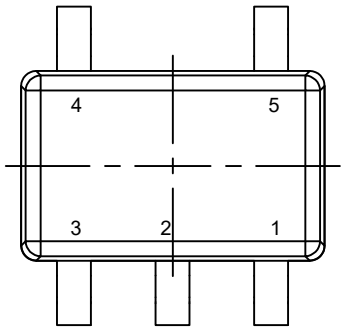
P5.049
KA0005AA
5-SC70 2.0 x 1.25 x 0.95 mm Body, 0.65mm Pitch Lead Small Outlibe Transistor Plastic Package
Rev04, Jul 16, 2025



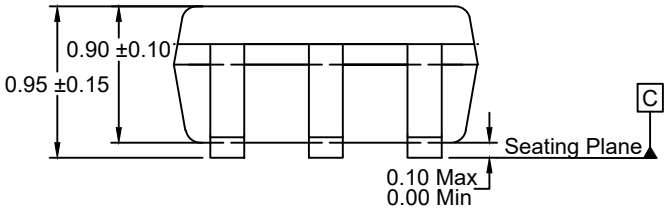
Top View



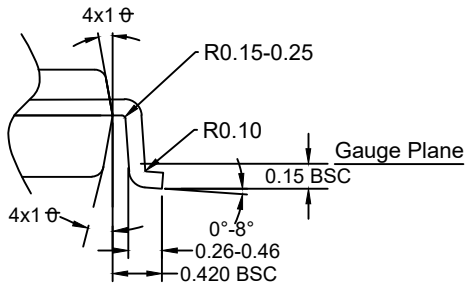
Side View



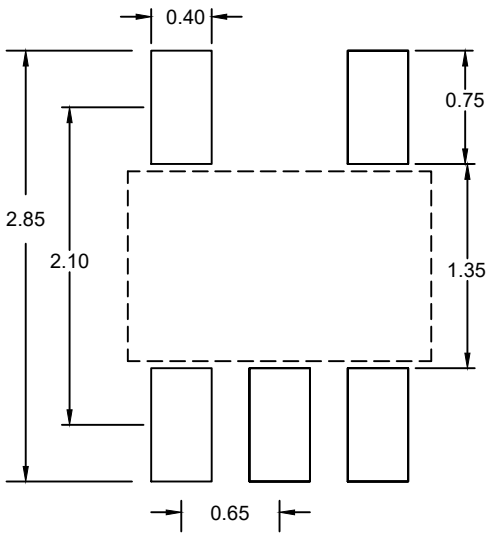
Bottom View



Side View



Detail"A"

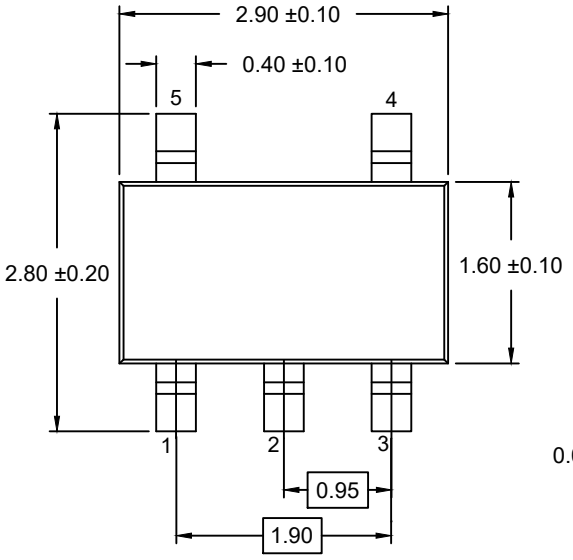


Recommended Land Pattern

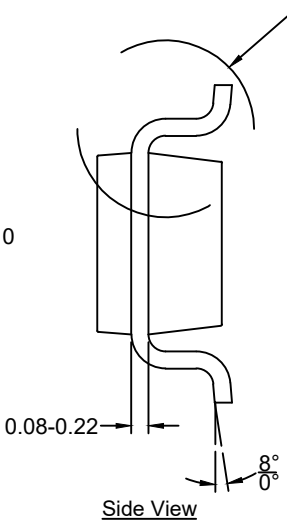
Notes:
1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions body x and y are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Converted inch dimen

Package Outline Drawing

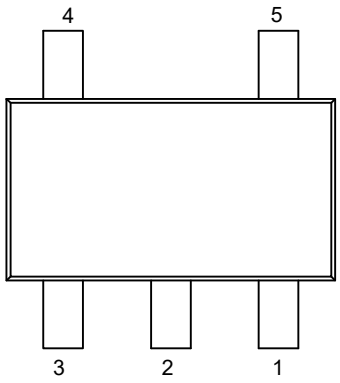
P5.064
KA0005AB
5-SOT 2.90 x 1.60 x 1.45 mm Body, 0.95mm Pitch Lead Small Outline Transistor Plastic Package
Rev04, Jul 22, 2025



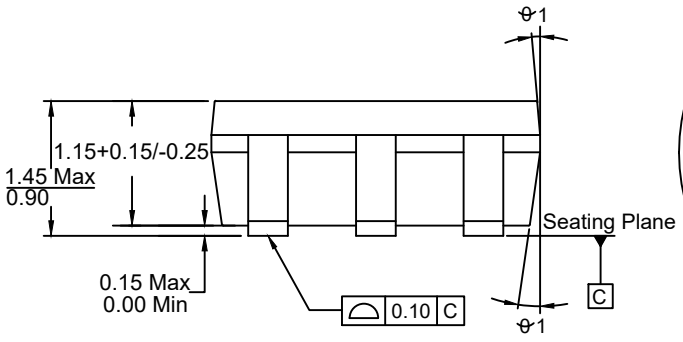
Top View



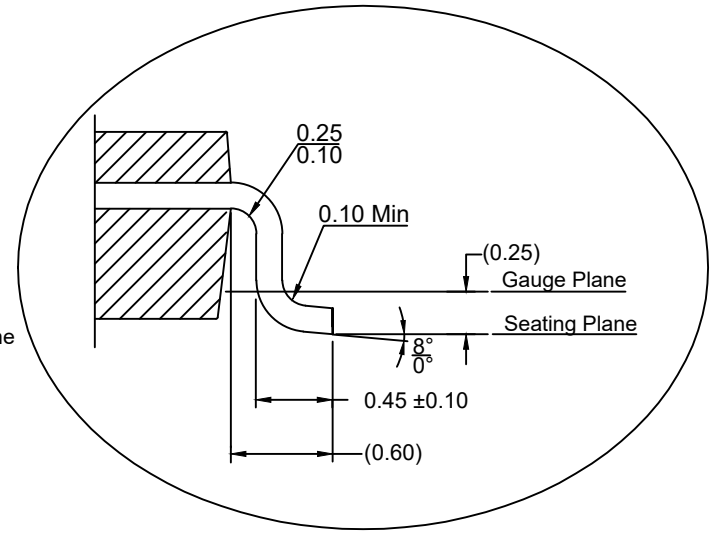
Side View



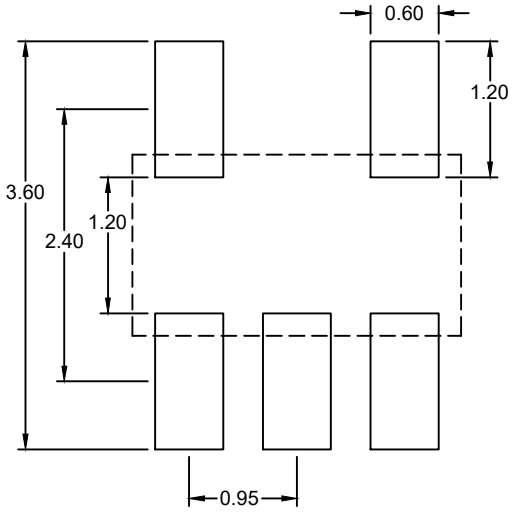
Bottom View



Side View



Detail "A"



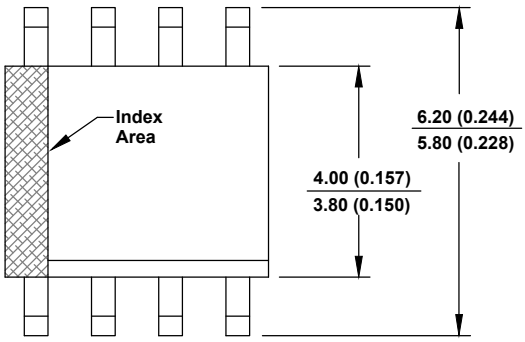
Recommended Land Pattern

Notes:

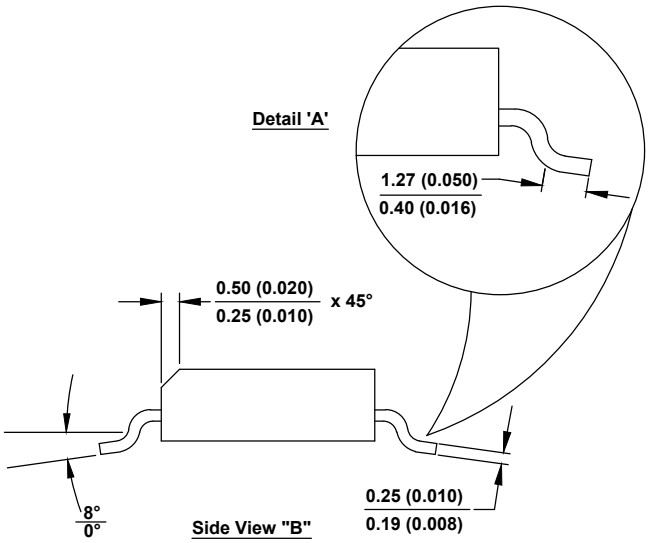
1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA
3. Package length and width are exclusive of mold flash, protrusions or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: Millimeter.

Package Outline Drawing

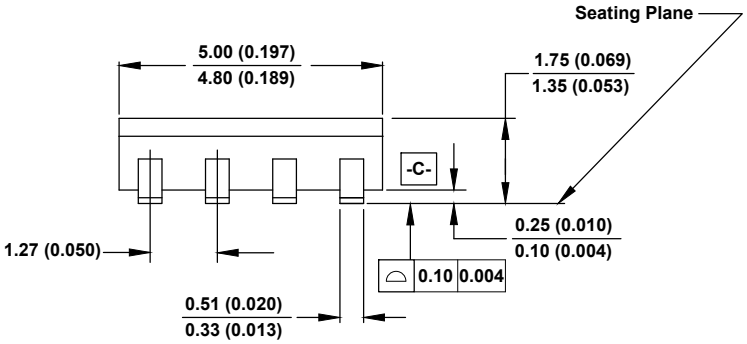
M8.15
GS0008AC
8-Lead Narrow Body Small Outline Plastic Package 4.90 x 3.90 x 1.43 mm Body, 1.27 mm Pitch
Rev08, Jul 7, 2025



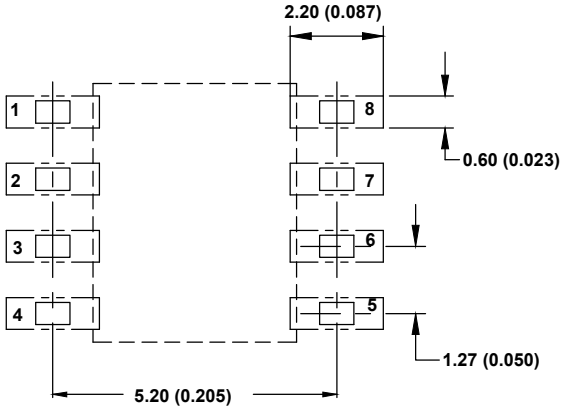
Top View



Side View "B"



Side View "A"



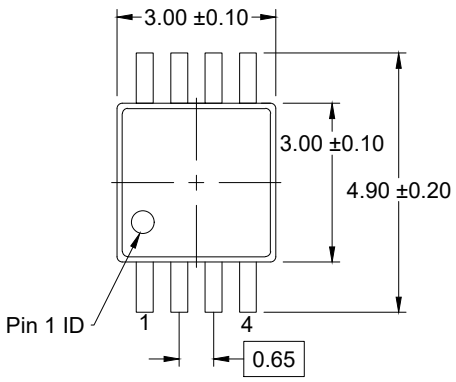
Typical Recommended Land Pattern

Notes:

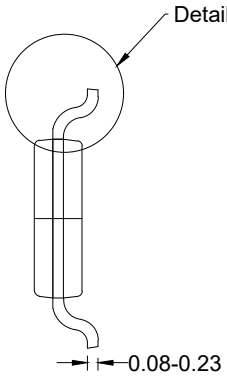
1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

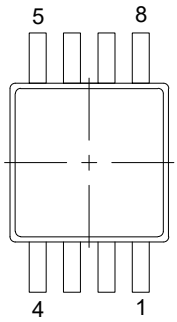
M8.118D
HV0008AC
8-MSOP 3.00 x4.90 x 1.10 mm Body, 0.65 mm Pitch
Rev03, Jul 11, 2025



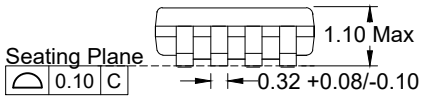
Top View



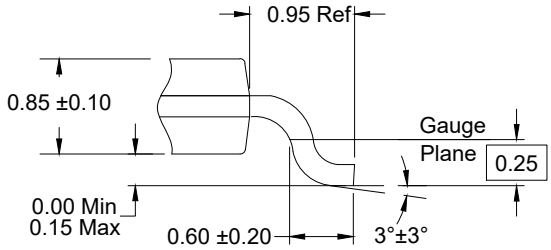
Side View



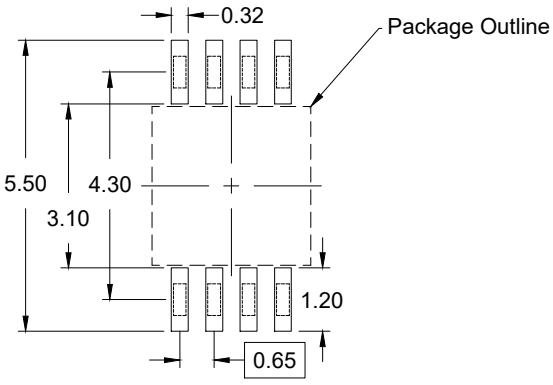
Bottom View



Side View



Detail "X"



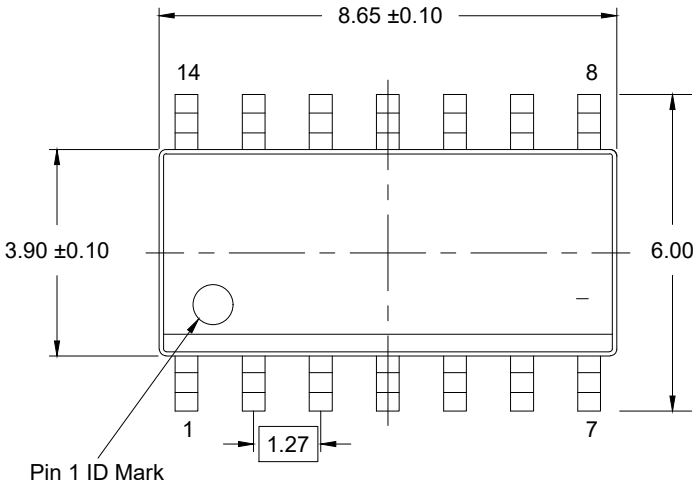
Typical Recommended Land Pattern

Notes:

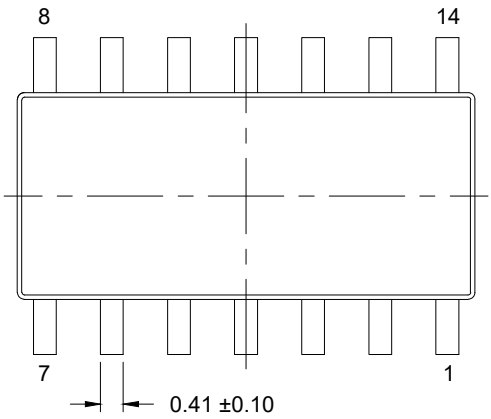
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Package Outline Drawing

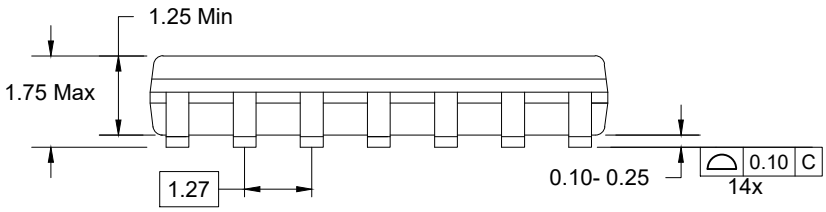
M14.15
GS0014AB
14-SOICN 8.65 x 3.90 x 1.75 mm Body, 1.27 mm Pitch
Rev03, Jun 26, 2025



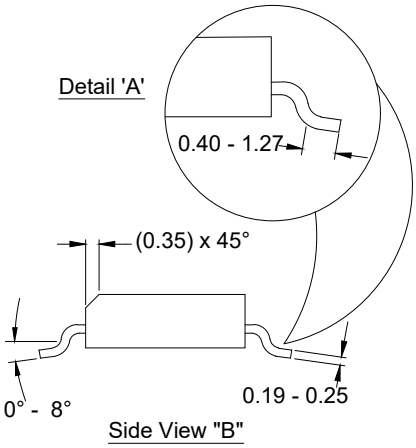
Top View



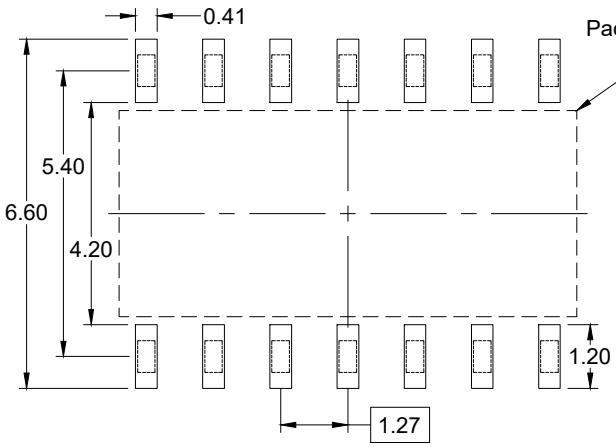
Bottom View



Side View



Side View "B"



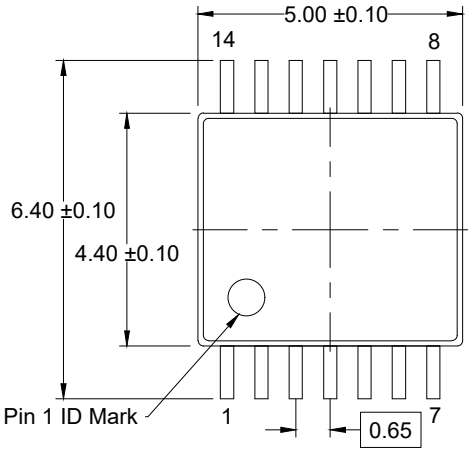
Typical Recommended Land Pattern

Notes:

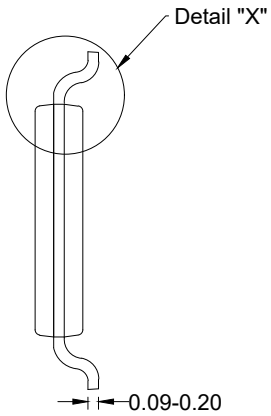
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Package Outline Drawing

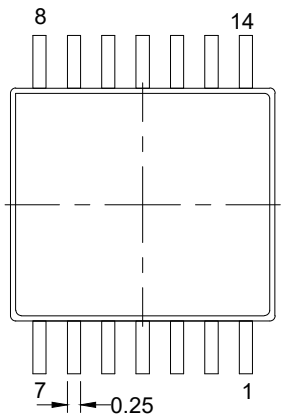
M14.173
HV0014AA
14-Lead Thin Shrink Small Outline package (TSSOP) 5.00 x 4.40 x 1.20 mm Body, 0.65 mm Pitch
Rev04, Jun 26, 2025



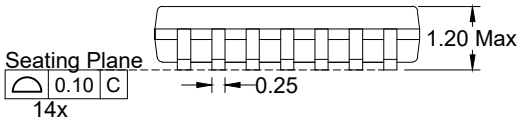
Top View



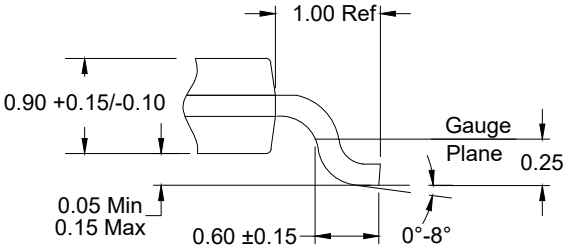
Side View



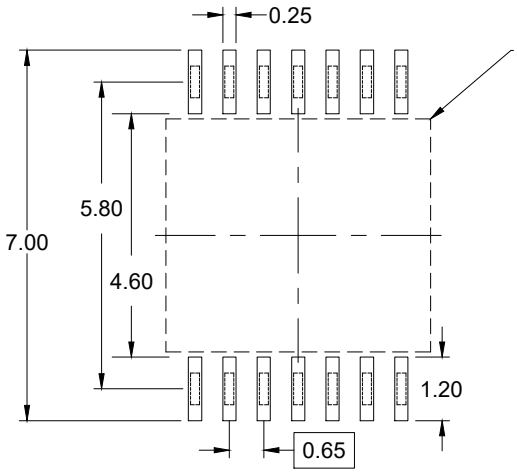
Bottom View



Side View



Detail "X"



Typical Recommended Land Pattern

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

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