RRA70180, RRA71180

Low-Side and High-Side Voltage Output, Current-Sense Amplifiers

Description

The RRA70180 and RRA71180 deliver high-accuracy current sensing in a compact, cost-effective package. These voltage-output current-sense amplifiers precisely measure the differential voltage across an external shunt resistor and convert it into a ground-referenced signal for easy system integration.

With a wide common-mode input range from -0.2V to +26V, these devices simplify both high-side and low-side current measurements in 12V and 24V systems, regardless of the supply voltage. The integrated, precision-matched resistor network offers four fixed-gain options (20V/V, 50V/V, 100V/V, and 200V/V), ensuring exceptional accuracy with minimal gain error and temperature drift.

Designed for robust performance, the devices operate from a 2.7V to 5.5V supply and maintain accuracy across a -40°C to +125°C temperature range. With a low supply current of only 260µA, the RRA70180 and RRA71180 are perfectly suited for always-on power and energy monitoring.

Available in a space-saving 5-pin SOT-23 package with two pinout options (A and B), this amplifier family easily fits into existing designs while streamlining layout compatibility and production efficiency.

Part	Package	Body Size (Nominal)
RRA70180	5-pin SOT-23	1.60mm×2.90mm
RRA71180	5-pin SOT-23	1.60mm×2.90mm

Features

- Wide common-mode range: -0.2V to +26V (supports high-side and low-side sensing)
- High bandwidth: 350kHz small signal (20V/V devices)
- Low offset: ≤±150µV (VCM = 0V), ≤±500µV (VCM = 12V)
- Fast response: 2V/µs output slew rate
- High accuracy: ≤±1% gain error (max); ≤1µV/°C offset drift (max)
- Fixed-gain options: 20 / 50 / 100 / 200V/V
- Low power: ≤260µA quiescent current (per channel)

Applications

- Motor drives and phase-current sensing
- Battery pack/BMS charge-discharge monitoring
- DC power-rail management: DC/DC, hot-swap, e-fuse, OR-ing
- LED and lighting control (constant-current regulation, fault detect)
- Fast over-current/short-circuit detection and load diagnostics
- Solar/PV inverters and charge controllers (MPPT current sensing)

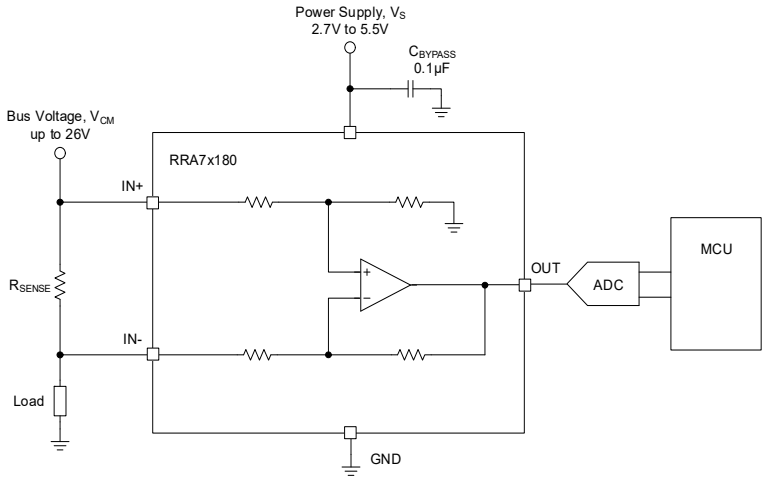


Figure 1. Typical Application Circuit

Contents

1. Overview

1.1 Functional Block Diagram

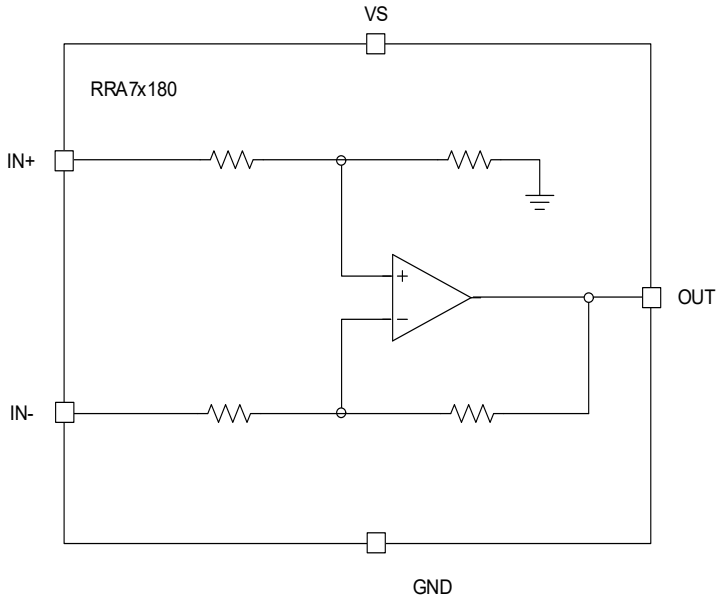


Figure 2. Block Diagram

2. Pin Information

2.1 5-pin SOT-23 (RRA70180)

2.1.1 Pin Assignments

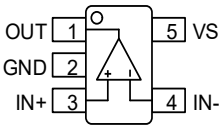


Figure 3. Pin Assignments – Top View

2.1.2 Pin Descriptions

Pin Number	Pin Name	Function
1	OUT	Signal Output
2	GND	Ground
3	IN+	Non-Inverting Signal Input
4	IN-	Inverting Signal Input
5	VS	Supply Voltage

2.2 5-pin SOT-23 (RRA71180)

2.2.1 Pin Assignments

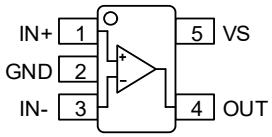


Figure 4. Pin Assignments – Top View

2.2.2 Pin Descriptions

Pin Number	Pin Name	Function
1	IN+	Non-Inverting Signal Input
2	GND	Ground
3	IN-	Inverting Signal Input
4	OUT	Signal Output
5	VS	Supply Voltage

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage, VS	-	6.0	V
Input Voltage, IN to GND (Differential (V_{IN+}) – (V_{IN-}))	-28	28	V
Input Voltage, IN+ to IN- (Common mode)	(GND) – 0.3	28.0	V
Output Voltage	(GND) – 0.3	(VS) + 0.3	V
Output Current	-	±8	mA
Output Short-Circuit	Continuous		mA
Ambient Temperature, T_A	-55	150	°C
Junction Temperature, T_J	-	150	°C
Storage Temperature, T_{stg}	-65	150	°C
Human Body Model (Tested per JS-001)	-	6	kV
Charged Device Model (Tested per JS-002)	-	1.5	kV
Latch-Up (Tested per JESD78; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage, V_S	2.7	5	5.5	V
Common-mode Input Voltage (IN+ and IN-), V_{CM}	-0.2	12	26	V
Ambient Temperature, T_A	-40	-	+125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	5-pin SOT-23 Package	θ_{JA}[1]	Junction to ambient	180	°C/W
		θ_{JC}[2]	Junction to case	130	°C/W

1. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

V_S = 5V, V_{IN+} = 12V, and V_{SENSE} = V_{IN+} – V_{IN-} at T_A = 25°C, (unless otherwise noted)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Input						
Common-Mode Rejection Ratio	CMRR	V_{IN+} = 0V to 26V, V_{SENSE} = 10mV, T_A = -40°C to 125°C	90	100	-	dB
Input Offset Voltage	V_{OS}	V_{SENSE} = 0mV, V_{IN+} = 0V[2]	-	±25	±150	µV
		V_{SENSE} = 0mV[2]	-	±100	±500	µV
Input Offset Voltage Temperature Coefficient	TCV_{OS}	T_A = -40°C to 125°C	-	±0.2	1	µV/°C

V_S = 5V, V_{IN+} = 12V, and V_{SENSE} = V_{IN+} – V_{IN-} at T_A = 25°C, (unless otherwise noted) (Cont.) (Cont.)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Power Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5V, V_{IN+} = 12V, V_{SENSE} = 10mV	-	±8	±40	µV/V
Input Bias Current	I_B	V_{IN+} = 0V, V_{SENSE} = 0mV	-	0.1	-	µA
		V_{SENSE} = 0mV	-	80	-	µA
Input Offset Current	I_{OS}	V_{SENSE} = 0mV	-	±0.05	-	µA
Quiescent Current	I_Q	V_{SENSE} = 10mV	-	197	260	µA
		V_{SENSE} = 10mV, T_A = -40°C to 125°C	-	-	300	µA
Output						
Gain	G	RRA7x180-2xx	-	20	-	V/V
		RRA7x180-5xx	-	50	-	V/V
		RRA7x180-8xx	-	100	-	V/V
		RRA7x180-9xx	-	200	-	V/V
Gain Error	E_G	V_{OUT} = 0.5V to V_S – 0.5V, T_A = -40°C to 125°C	-	±0.1	±1	%
Gain Error vs Temperature	-	T_A = -40°C to 125°C	-	1.5	20	ppm/℃
Nonlinearity Error	-	V_{OUT} = 0.5V to V_S – 0.5V	-	±0.01		%
Maximum Capacitive Load	-	No sustained oscillation	-	1		nF
Output Voltage Swing	V_{SP}	Swing to V_S, R_L = 10kΩ to GND, T_A = -40°C to 125°C	-	V_S – 0.02	V_S – 0.03	V
	V_{SN}	Swing to GND, R_L = 10kΩ to GND, T_A = -40°C to 125°C	-	V_{GND} + 0.0005	V_{GND} + 0.005	V
AC Parameters						
Bandwidth	BW	RRA7x180-2xx, C_L = 10pF	-	350	-	kHz
		RRA7x180-5xx, C_L = 10pF	-	210	-	kHz
		RRA7x180-8xx, C_L = 10pF	-	150	-	kHz
		RRA7x180-9xx, C_L = 10pF	-	105	-	kHz
Slew Rate	SR	-	-	2	-	V/µs
Noise						
Voltage Noise Density, RTI	e_n	-	-	40	-	nV/√Hz

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Offset voltage is obtained by linear extrapolation to V_{SENSE} = 0V with V_{SENSE} = 10% to 90% of full-scale-range.

4. Typical Performance Graphs

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V (unless otherwise specified)

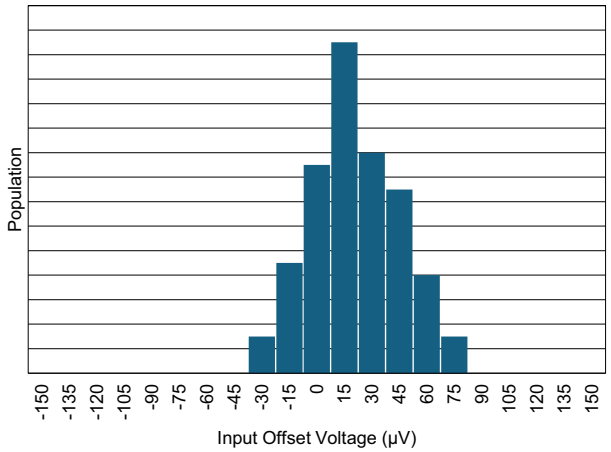


Figure 5. VOS Production Distribution Gain = 20, V_{IN+} = 0V

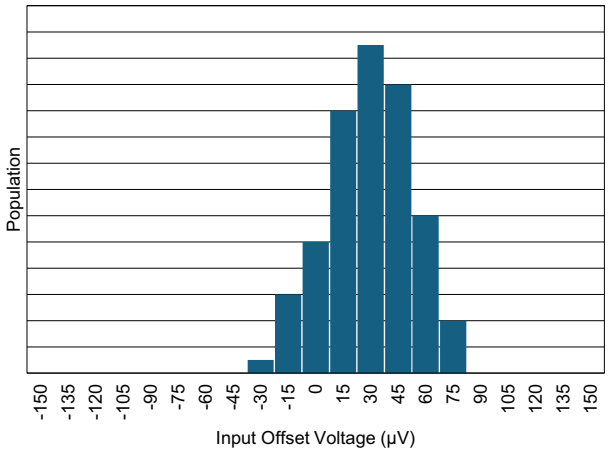


Figure 6. VOS Production Distribution Gain = 50, V_{IN+} = 0V

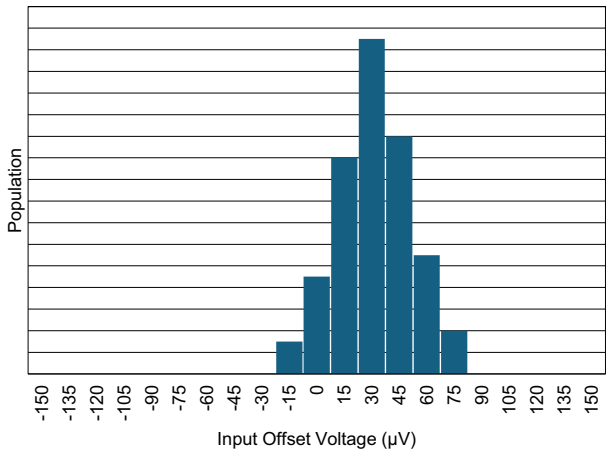


Figure 7. VOS Production Distribution Gain = 100, V_{IN+} = 0V

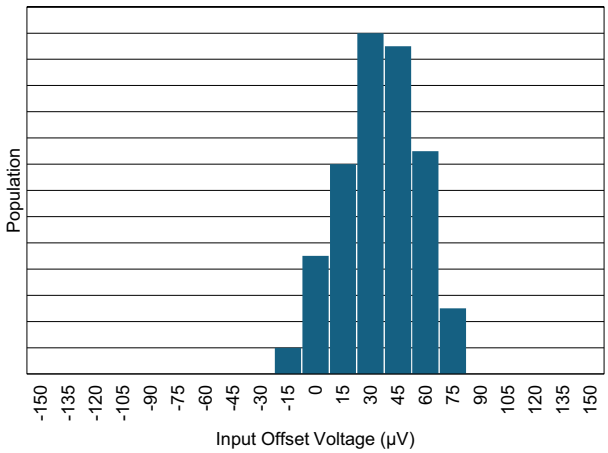


Figure 8. VOS Production Distribution Gain = 200, V_{IN+} = 0V

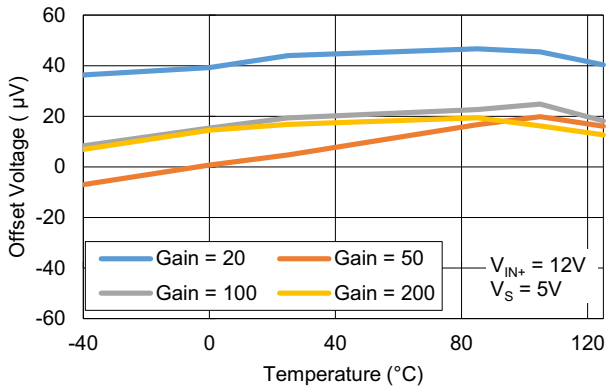


Figure 9. Offset Voltage vs Temperature

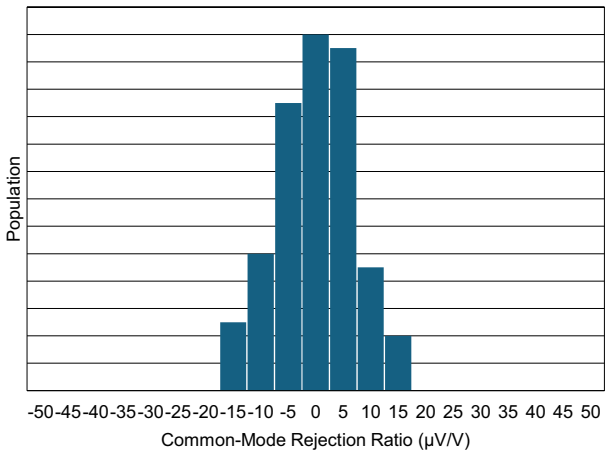


Figure 10. CMRR Production Distribution Gain = 20

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V (unless otherwise specified) (Cont.)

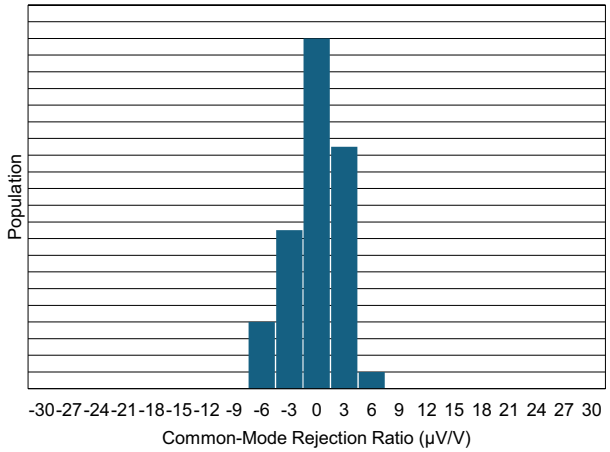


Figure 11. CMRR Production Distribution Gain = 50

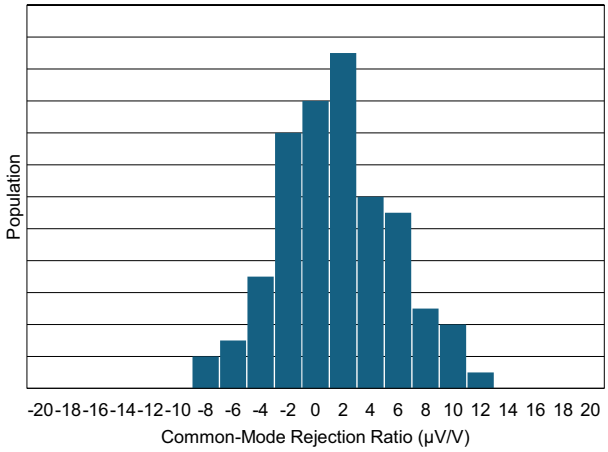


Figure 12. CMRR Production Distribution Gain = 100

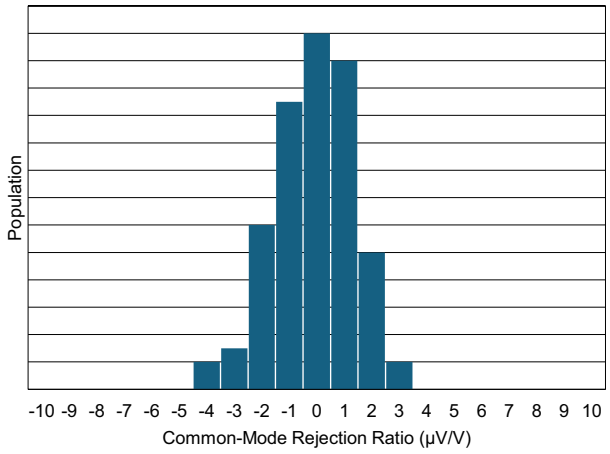


Figure 13. CMRR Production Distribution Gain = 200

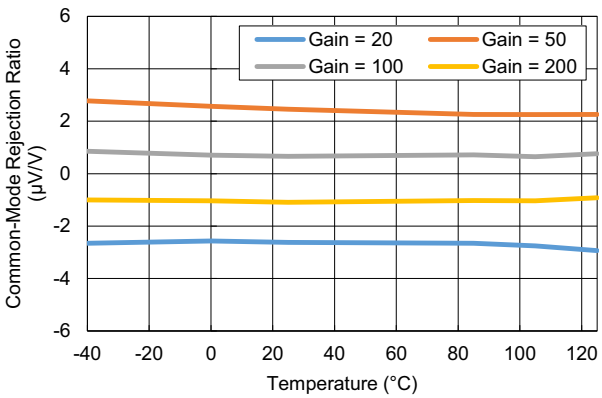


Figure 14. CMRR vs Temperature

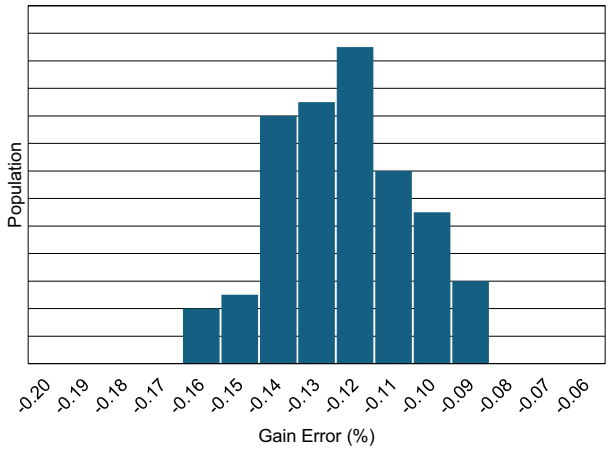


Figure 15. Gain Error Production Distribution Gain = 20

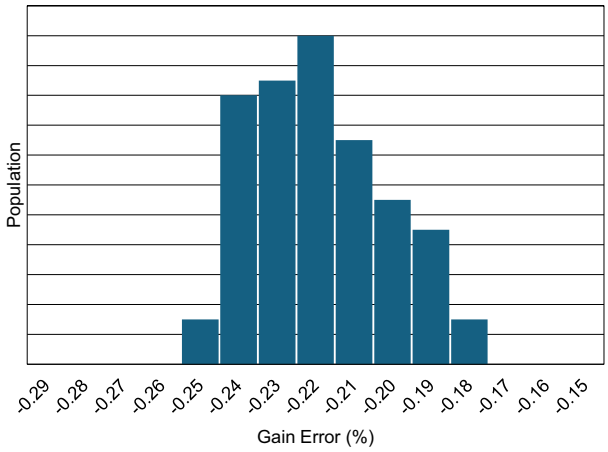


Figure 16. Gain Error Production Distribution Gain = 50

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V (unless otherwise specified) (Cont.)

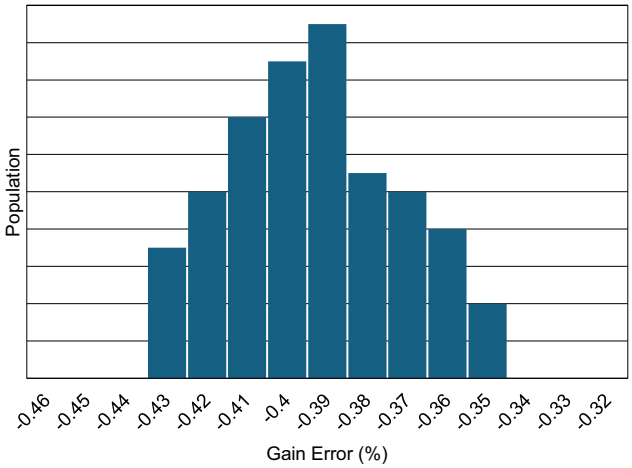


Figure 17. Gain Error Production Distribution Gain = 100

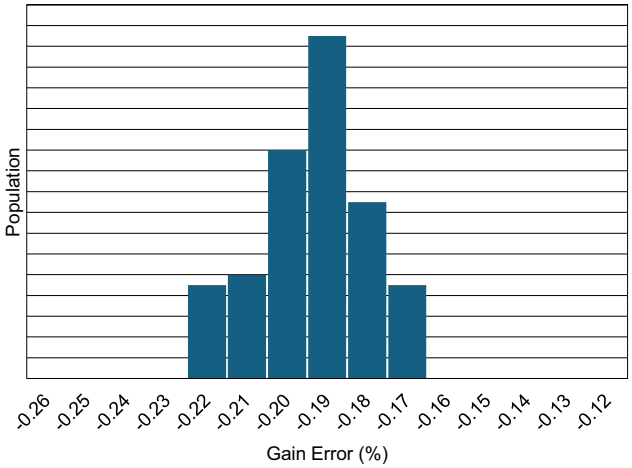


Figure 18. Gain Error Production Distribution Gain = 200

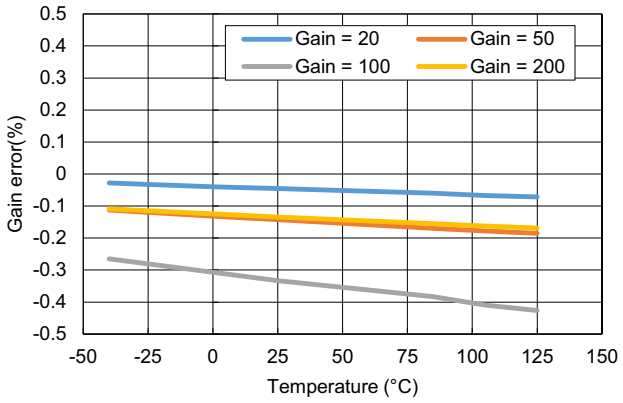


Figure 19. Gain Error vs Temperature

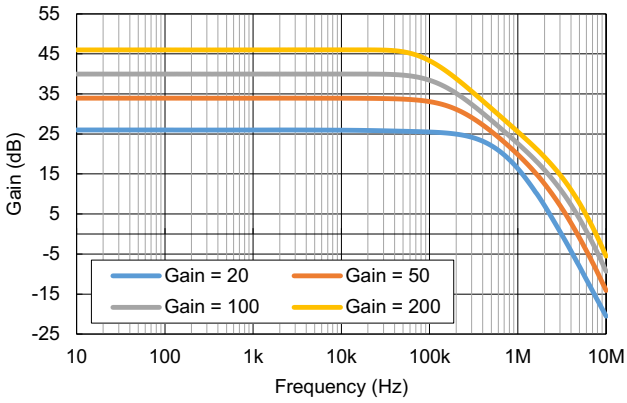


Figure 20. Gain vs Frequency

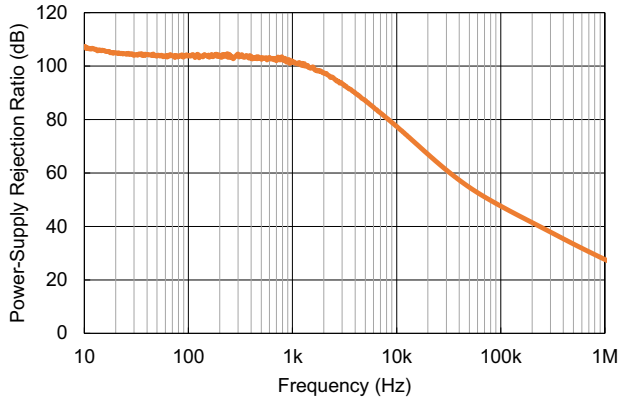


Figure 21. PSRR vs Frequency

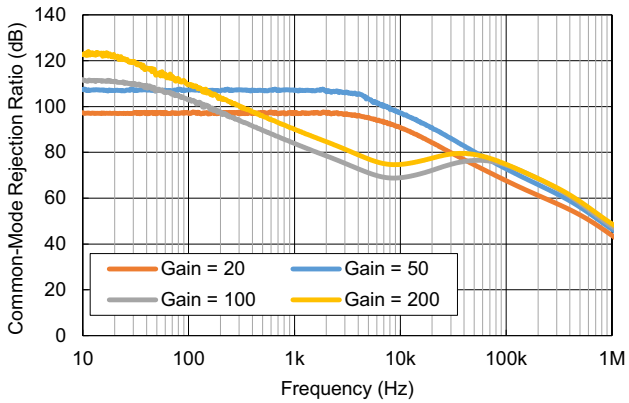


Figure 22. CMRR vs Frequency

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V (unless otherwise specified) (Cont.)

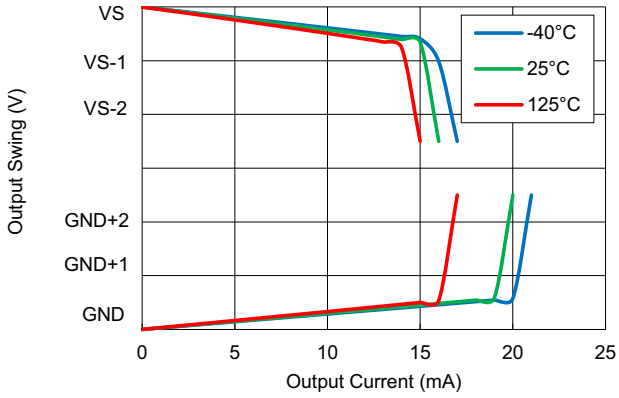


Figure 23. Output Voltage Swing vs Output Current

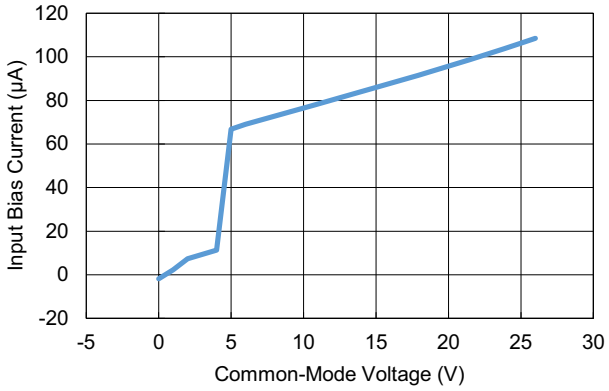


Figure 24. Input Bias Current vs Common-Mode Voltage

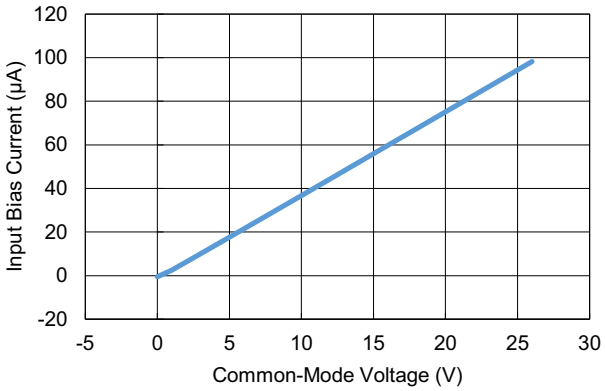


Figure 25. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

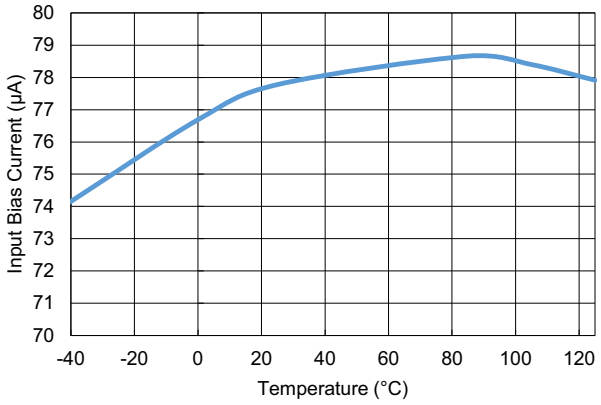


Figure 26. Input Bias Current vs Temperature

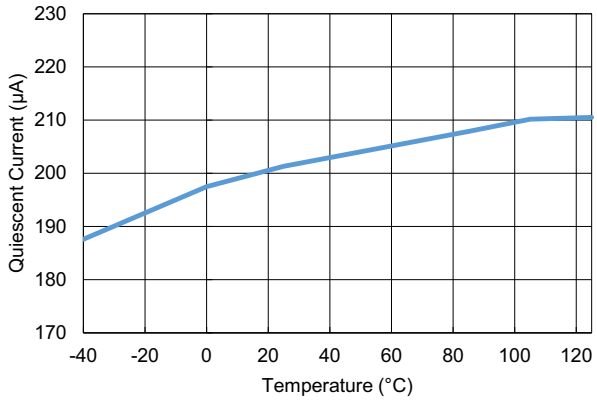


Figure 27. Quiescent Current vs Temperature

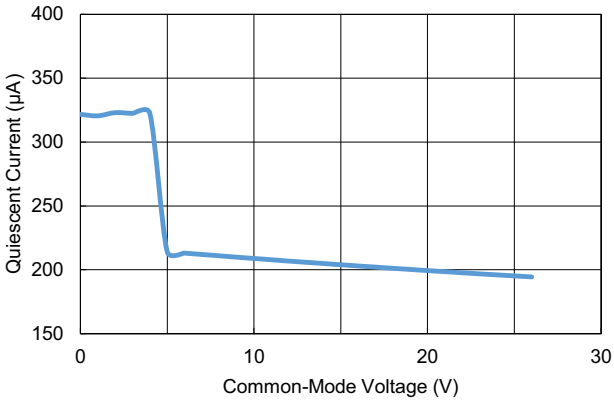


Figure 28. Quiescent Current vs Common-Mode Voltage

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V (unless otherwise specified) (Cont.)

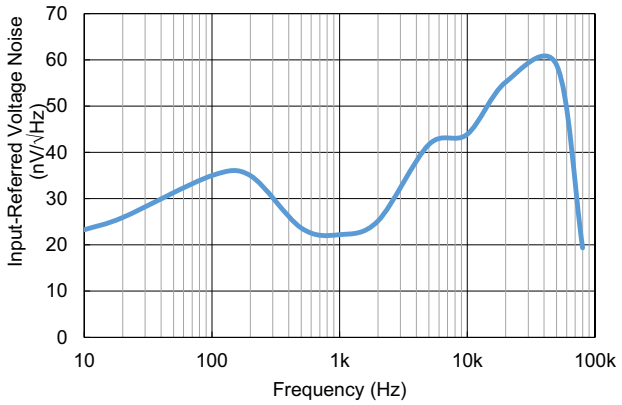


Figure 29. Input Refereed Voltage Noise vs Frequency (G = 100)

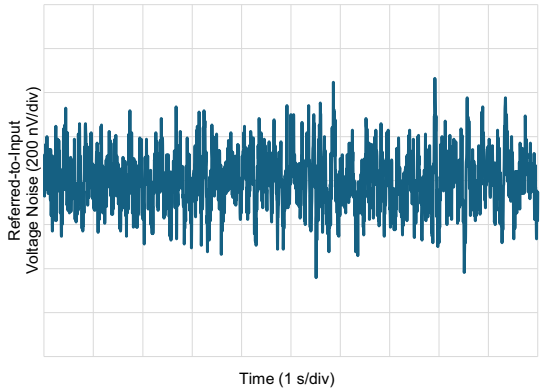


Figure 30. 0.1Hz to 10Hz Voltage Noise (Referred-to-Input)

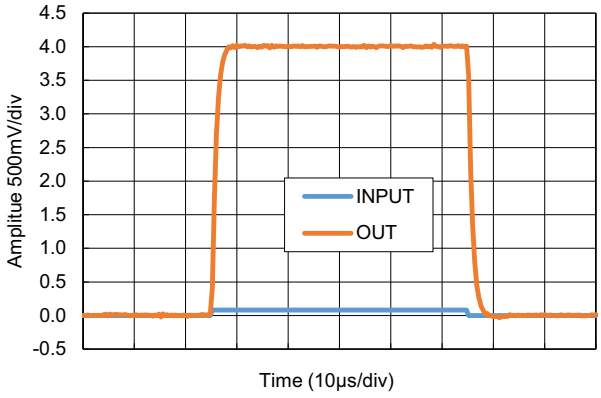


Figure 31. Step Response

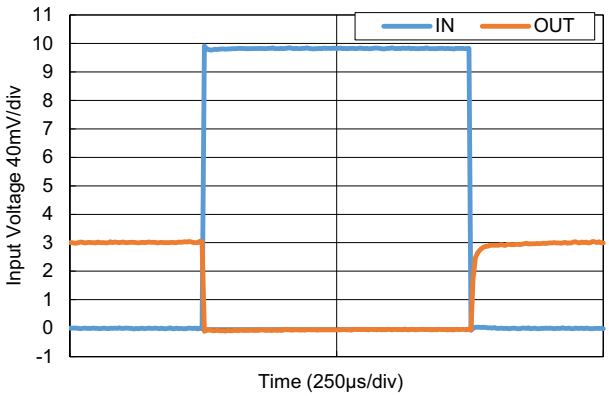


Figure 32. Inverting Differential Input Overload

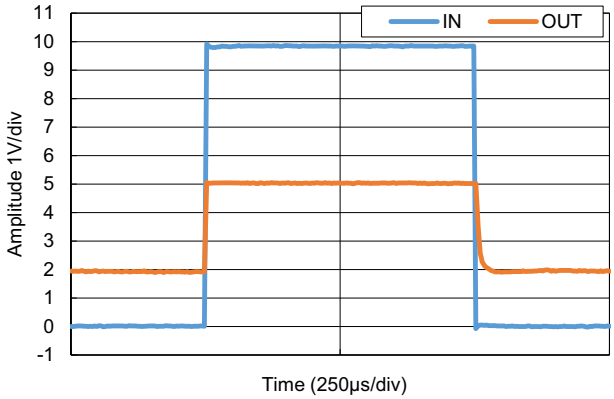


Figure 33. Non-inverting Differential Input Overload

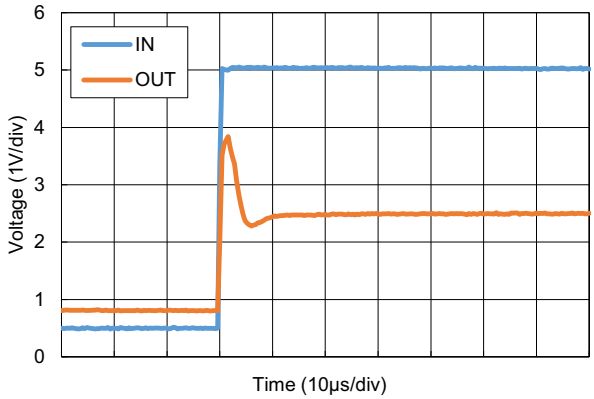


Figure 34. Startup Response

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V (unless otherwise specified) (Cont.)

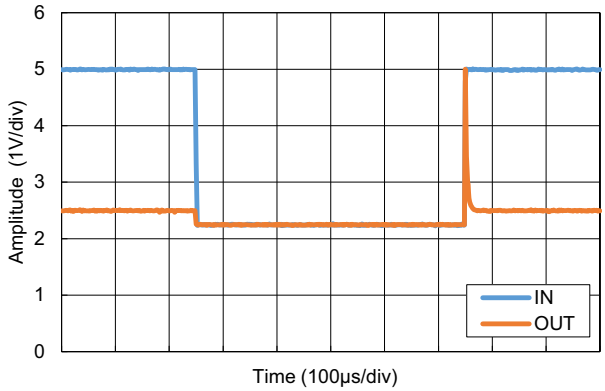


Figure 35. Brownout Recovery

5. Functional Description

5.1 Overview

The RRA7x180 is a fixed-gain, single-channel current-sense amplifier designed for cost-sensitive, high-volume applications, including motor control, battery monitoring, power management, lighting control, and overcurrent detection. The device measures the small differential voltage developed across an external shunt resistor and produces a single-ended output voltage proportional to the sensed current.

A defining characteristic of this device family is that its common-mode input range (-0.2V to +26V) is independent of its supply voltage range (2.7V to 5.5V). This feature allows the device to sense current on rails well above its own supply voltage, enabling use in both low-side (device referenced near ground) and high-side (device referenced to the bus voltage) configurations without altering the surrounding circuit topology.

The gain is factory-trimmed using an internal matched-resistor network rather than external gain-setting resistors. This architecture minimizes gain error and temperature drift and requires no user calibration.

5.2 High-Side Versus Low-Side Current Sensing

Because its input common-mode range is independent of the supply pin, the RRA7x180 operates in either sensing topology without modification. In low-side sensing, the shunt resistor is placed between the load and ground, so the input common-mode voltage remains near 0V and is isolated from bus-voltage transients. In high-side sensing, the shunt resistor is placed between the supply rail and the load, so the input common-mode voltage tracks the bus voltage. High-side sensing is preferred when the load's return path must remain continuously grounded, such as in fault-detection or ground-continuity-sensitive systems.

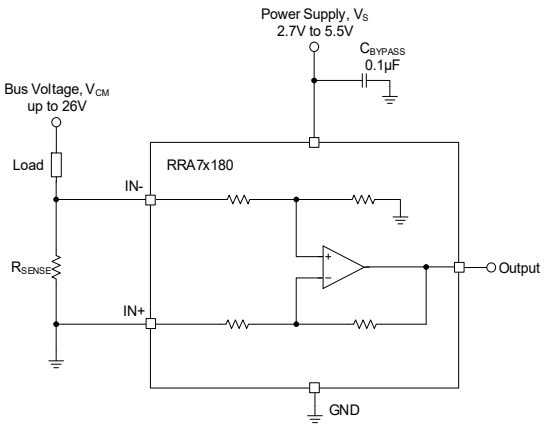


Figure 36. Low-Side Sensing

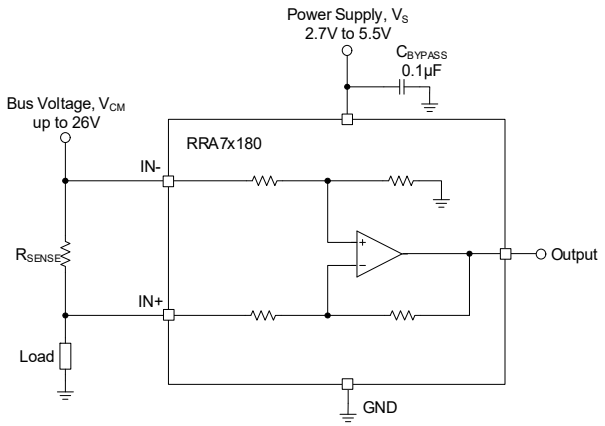


Figure 37. High-Side Sensing

5.3 Bandwidth

Bandwidth scales inversely with gain: the lowest-gain device (Gain = 20V/V) provides the widest bandwidth, 350kHz, while the highest-gain device (Gain = 200V/V) is limited to approximately 105kHz. Applications that must track fast-changing currents, such as PWM motor drives or fast overcurrent comparators, should consider this bandwidth-versus-gain trade-off together with the shunt-resistor sizing procedure described under Selecting Shunt Resistor and Gain.

5.4 Slew Rate

The device specifies an output slew rate of 2V/µs, which determines how quickly the output can respond to a step change in current sensing. This specification is most significant during fault recovery: after a differential-input overload condition clears, the output must slew back to its correct value quickly enough that a downstream comparator or ADC does not miss or mistime the recovery. A higher slew rate also ensures the amplifier does not become the limiting factor when paired with a fast external comparator for overcurrent protection.

5.5 Output Swing

The output swings close to both supply rails; however, because the current-sense amplifier is a closed-loop system, its minimum achievable swing to GND at zero current is limited by whichever is greater: the specified minimum swing or the input offset voltage multiplied by the device gain. At the highest gain grade (Gain = 200V/V), even a small input offset is multiplied into a non-negligible zero-current output voltage, an important consideration when digitizing very low currents.

5.6 No Shutdown Pin

The device does not include a dedicated enable or shutdown pin. However, its low quiescent current allows an external logic gate or small transistor switch to control its supply current directly. Designers using this approach should account for the approximately 500kΩ impedance path between each input and the OUT and GND pins, which can source a small current back into the shunt circuit even while the device is unpowered.

6. Application Information

6.1 Basic Connection

The minimum required external components are a 0.1µF supply bypass capacitor, placed close to the VS and GND pins, and a Kelvin (four-wire) connection from IN+ and IN− directly to the shunt-resistor pads. Noisy or high-impedance supply rails may require an additional bulk decoupling capacitor.

6.2 Selecting Shunt Resistor and Gain

Selecting the shunt-resistor value and gain grade requires evaluating three constraints together, rather than in isolation:

- Power dissipation: $R_{SENSE(max)} = P_{D(max)} \div I_{MAX}^2$, where P_D(max) is the maximum power the design can dissipate in the shunt at full-scale current.
- Positive output-swing headroom: Gain × I_{MAX} × R_{SENSE} must remain below V_{SP}; otherwise, the output clips before reaching full-scale current.
- Negative output-swing / resolution floor: Gain × I_{MIN} × R_{SENSE} must exceed the minimum specified swing-to-GND; otherwise, low-end currents will be indistinguishable from the zero-current floor.

In practice, the design process is as follows:

1. Select the largest R_{SENSE} that the power budget allows, since a larger shunt improves the signal-to-offset ratio.
2. Select the lowest gain grade that fully uses the amplifier's output range without clipping. Higher gain improves resolution at low currents but reduces bandwidth and available rail headroom at high currents.

6.3 Sample Calculation

The design target is V_S = 5V, low-side sensing, unidirectional current measurement, I_{MAX} = 40A, shunt power-loss budget < 900mW, target accuracy better than 1.5% at full scale, and small-signal bandwidth greater than 80kHz.

- Power-limited shunt size: $R_{SENSE(max)} \leq 900mW \div (40A)^2 \approx 0.56m\Omega$. The nearest standard value, 0.5mΩ, is selected.
- Gain check against positive swing: the maximum usable gain is approximately 248V/V; the 200V/V grade fits comfortably and maximizes output range.
- Offset contribution at full scale: with a maximum offset of 150µV at V_S = 5V and VCM = 0V, the offset error is approximately 150µV ÷ (40A × 0.5mΩ) = 0.75%.
- Total error (root-sum-square of gain error and offset error): $\sqrt{(1\%^2 + 0.75\%^2)} \approx 1.25\%$, which is within the 1.5% budget.
- Bandwidth check: the device with Gain = 200V/V has a typical bandwidth of 105kHz, which comfortably exceeds the 80kHz requirement.

This sizing procedure applies to any of the four gain grades; only the numeric values in each step change.

6.4 Signal Filtering

The current-sense amplifier's signal path can be filtered at either the input or the output, depending on the type of noise the design needs to reject. Both locations work, but they behave very differently: one is tightly constrained by the device's internal architecture, and the other is not.

6.4.1 Input Filtering

A simple RC filter can be placed directly at IN+ and IN-: a small series resistor (R_P) on each line, with a differential capacitor (C_P) across the two inputs.

The one hard rule here is resistor size. Keep R_P to 10Ω or less per side. If RP exceeds this value, it begins interacting with the amplifier's internal input circuitry, which adds gain error rather than simply filtering the signal. Because R_P is capped so low, a practically sized capacitor only pushes the filter's corner frequency into the tens-of-megahertz range (for example, 10Ω with 1nF gives a corner frequency near 16MHz). This is far above where most switching noise actually occurs, so input filtering is best reserved for one specific purpose: suppressing high-frequency EMI picked up directly at the sense leads, not general noise cleanup.

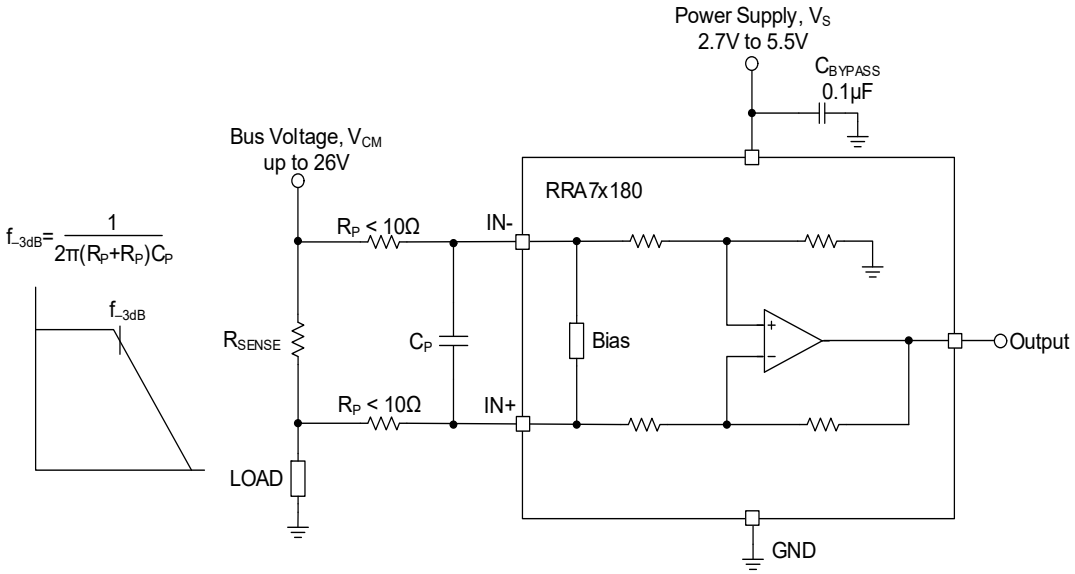


Figure 38. Input Filtering

6.4.2 Output Filtering

Filtering at the output, ahead of a high-impedance ADC input, is the more flexible option and the default choice for most designs. Because it sits after the amplifier's gain stage, there is no resistor-size constraint: R_P and C_P can be chosen freely to set whatever corner frequency the application requires, without affecting measurement accuracy.

6.5 Power Supply Recommendations

6.5.1 Overview

The device operates from a single 2.7V to 5.5V supply and draws very little quiescent current. However, it is typically installed alongside noisier components motor drivers, switching converters, digital logic, so supply design deserves more attention than the low quiescent-current spec might suggest. Decoupling, ripple, sequencing, and layout are addressed together below, since each affects the others.

6.5.2 Decoupling

Connect the 0.1µF bypass capacitor with short, direct traces to VS and GND. Any additional trace length adds inductance that reduces the capacitor's effectiveness at the frequencies it is meant to filter. Add the bulk capacitor whenever this rail is shared with a switching regulator or similar load, the two capacitors filter different frequency ranges, and one does not replace the other.

6.5.3 Supply Ripple (PSRR)

Supply ripple couples into the output through the device's power-supply rejection ratio (PSRR) typically, ±8µV/V, up to ±40µV/V worst-case, referred to the input. This should be treated as a real term in the overall accuracy budget rather than ignored.

Example: on a 5V rail with 50mV of ripple (1%, a reasonable figure near a switching converter), worst-case PSRR contributes 50mV × 40µV/V = 2µV of input-referred error. At 200V/V gain, this becomes a 0.4mV output error, small individually, but it adds to offset and gain error in the total accuracy calculation. On a noisier rail (200mV to 500mV ripple, common directly off an unfiltered switching supply), this error becomes significant enough to require explicit budgeting.

6.5.4 Quiescent Current

For designs with a strict power budget (battery-powered or duty-cycled systems in particular) use the 300µA maximum figure to account for worst-case operating temperature.

6.5.5 Supply Sequencing

The device has no dedicated shutdown or enable pin. If a design requires powering the device down between measurements, gate VS externally using a logic-level switch rather than relying on an internal low-power mode.

Two considerations apply:

- An internal impedance of approximately 500kΩ remains between the inputs and OUT/GND even when VS is removed. Include this leakage path when budgeting ultra-low sleep currents.
- Allow the device to complete its normal turn-on settling time after VS rises before sampling the output.

6.5.6 Shared Supply Rails

When this device shares a supply rail with other analog or mixed-signal components, route its 0.1µF bypass capacitor independently rather than connecting it to a shared decoupling point. A shared connection allows switching noise from one component to couple into another through the common trace. Feeding each device's decoupling separately avoids this risk, at the cost of a small number of additional capacitors.

6.6 Transient Protection Circuits

Two circuit topologies protect against common-mode transients that exceed the 26V input rating conditions such as automotive load dump, hot-plug events, or similar bus disturbances. Both work the same way: a series resistor limits the transient current, and a clamping diode redirects it to ground before it reaches the amplifier's input stage.

6.6.1 Dual-Zener Protection

This circuit uses an independent Zener diode on each input line, referenced to ground, with its own 10Ω series resistor. Because each line is clamped separately, this topology is well suited to designs where IN+ and IN- may experience different fault conditions. For example, an asymmetric cable fault or a line with its own local noise source. Select a Zener voltage below the device's absolute maximum rating but above its normal operating range, so the diode clamps only during a fault and remains inactive during normal operation (see Figure 39).

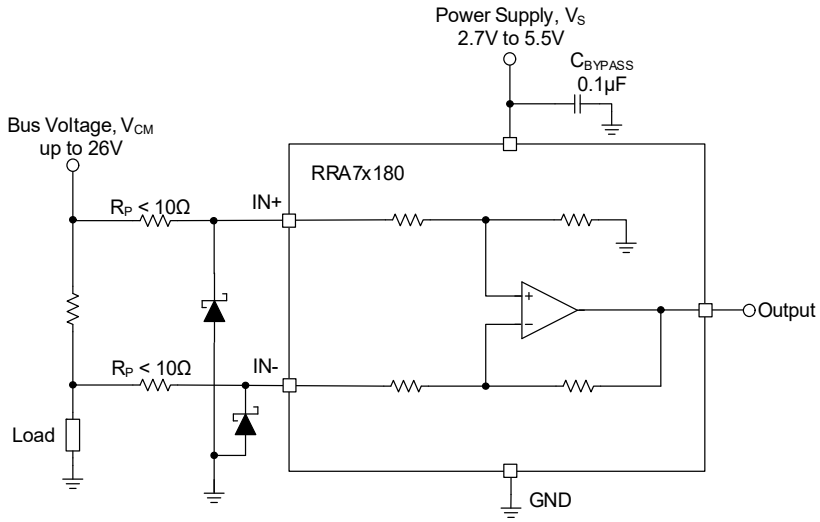


Figure 39. Transient Protection Using Dual-Zener Diodes

6.6.2 TVS Diode with Input Clamps

This circuit uses a single bidirectional transient-voltage-suppressor (TVS) diode connected across both input lines, along with the same 10Ω series resistors. Because one component protects both lines simultaneously, this approach requires one fewer part than the dual-Zener design and generally responds faster, since TVS diodes are built specifically for transient suppression. It is the preferred choice when the expected fault is common-mode such as ESD or hot-plug events rather than specific to one line.

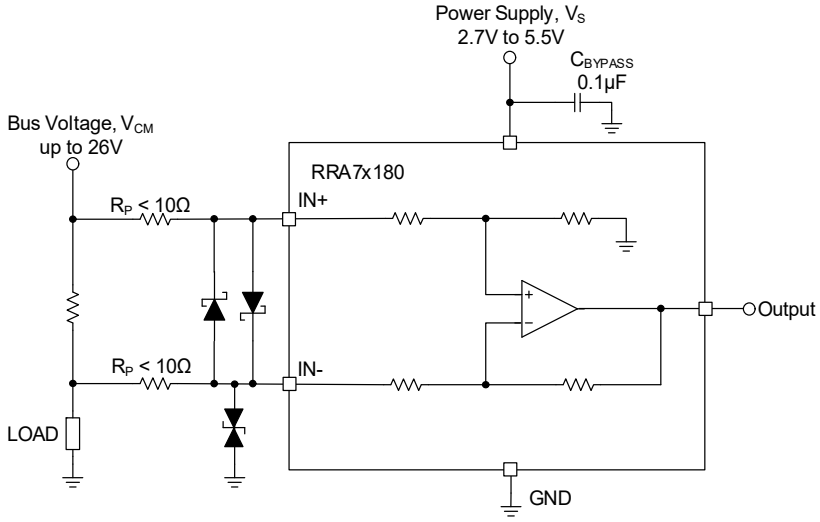


Figure 40. Transient Protection Using a Single Bidirectional TVS Diode and Input Clamps

6.7 Layout Guidelines

Board layout has a direct impact on measurement accuracy. Connect IN+ and IN− as a short, matched Kelvin pair straight to the shunt resistor's dedicated sense pads, keeping them away from switching nodes and routed over a solid, unbroken ground plane. Place the 0.1µF bypass capacitor within a few millimeters of the VS pin with short, direct connections, and position the shunt resistor close to the device with symmetric current flow to avoid introducing offset. Size power traces to the shunt independently from the low-current sense traces, and keep in mind that the shunt resistor is typically the larger heat source on the board, not the amplifier itself.

7. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1][2]	Part Marking	Gain (V/V)	# Channels	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
RRA70180-2P3	0182[5]	20	1	5-Pin SOT-23	P5.064	Reel, 3k units	-40 to 125°C
RRA70180-5P3	0185[5]	50					
RRA70180-8P3	0188[5]	100					
RRA70180-9P3	0189[5]	200					
RRA71180-2P3	1182[5]	20	1	5-Pin SOT-23	P5.064	Reel, 3k units	-40 to 125°C
RRA71180-5P3	1185[5]	50					
RRA71180-8P3	1188[5]	100					
RRA71180-9P3	1189[5]	200					

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. The Moisture Sensitivity Level (MSL) rating is 1. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.
5. The part marking is located on the bottom of the part.

9. Revision History

Revision	Date	Description
1.00	Aug 5, 2026	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRA70180-2P3	5	SOT-23	P5.064/KA0005AB
RRA70180-5P3	5	SOT-23	P5.064/KA0005AB
RRA70180-8P3	5	SOT-23	P5.064/KA0005AB
RRA70180-9P3	5	SOT-23	P5.064/KA0005AB
RRA71180-2P3	5	SOT-23	P5.064/KA0005AB
RRA71180-5P3	5	SOT-23	P5.064/KA0005AB
RRA71180-8P3	5	SOT-23	P5.064/KA0005AB
RRA71180-9P3	5	SOT-23	P5.064/KA0005AB

A.2 Symbol Pin Information

A.2.1 SOT-23 (RRA70180)

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT	Output	-
2	GND	Power	-
3	IN+	Input	-
4	IN-	Input	-
5	VS	Power	-

A.2.2 SOT-23 (RRA71180)

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	IN+	Input	-
2	GND	Power	-
3	IN-	Input	-
4	OUT	Output	-
5	VS	Power	-

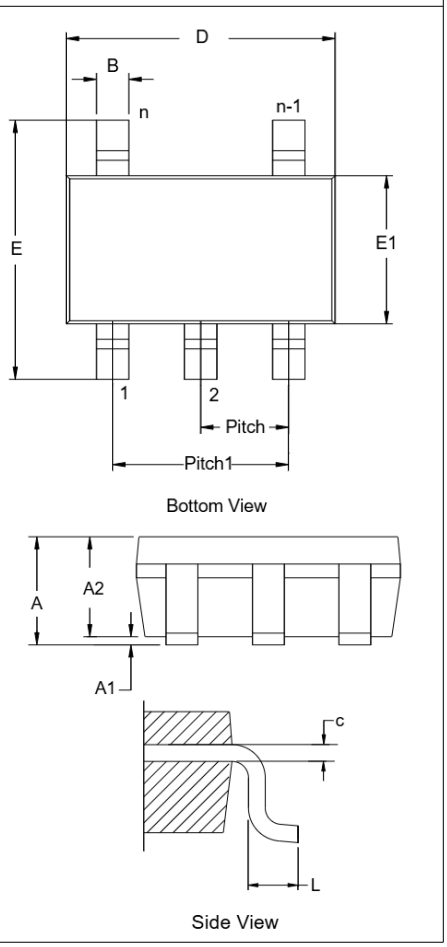
A.3 Symbol Parameters

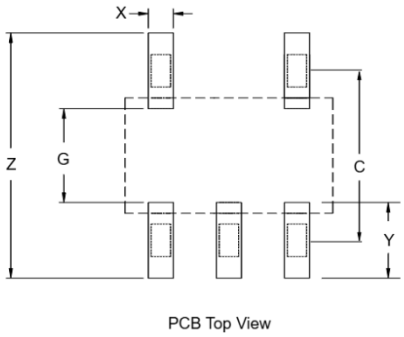
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Supply Voltage	Max Supply Voltage	Output Slew Rate	Gain
RRA70180-2P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	20V/V
RRA70180-5P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	50V/V
RRA70180-8P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	100V/V
RRA70180-9P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	200V/V
RRA71180-2P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	20V/V
RRA71180-5P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	50V/V
RRA71180-8P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	100V/V
RRA71180-9P3	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs	200V/V

A.4 Footprint Design Information

A.4.1 5-SOT-23

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOT23	P5.064/KA0005AB	5

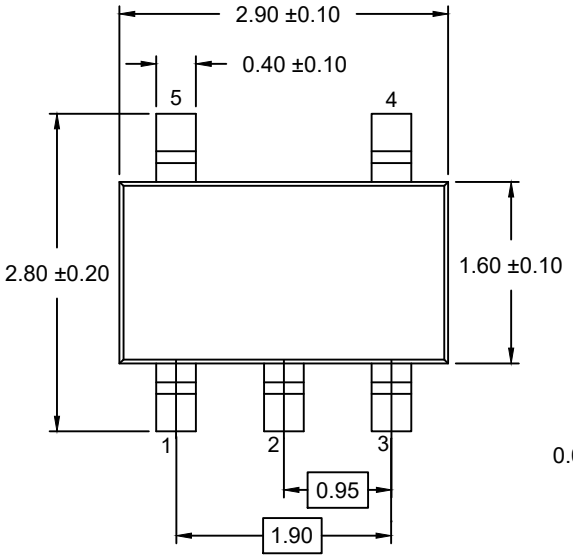
Description	Dimension	Value (mm)	Diagram[1]
Minimum body span (vertical side)	Dmin	2.80	
Maximum body span (vertical side)	Dmax	3.00	
Minimum lead span (horizontal side)	Emin	2.60	
Maximum lead span (horizontal side)	Emax	3.00	
Minimum lead width	Bmin	0.30	
Maximum lead width	Bmax	0.50	
Minimum body width (horizontal side)	E1min	1.50	
Maximum body width (horizontal side)	E1max	1.70	
Number of leads: 3, 4, 5 or 6	PinCount	5	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5	
Distance between the center of any two adjacent pins	Pitch	0.95	
Overall pitch (e1)	Pitch1	1.90	
Maximum Height	Amax	1.45	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.30	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	022	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.55	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram[1]**
Distance between pads. Measured from outside edges	Z	3.60	
Distance between pads. Measured from inside edges	G	1.20	
Pad width	X	0.60	
Pad length	Y	1.20	
Row spacing. Distance between pad centers	C	2.40	

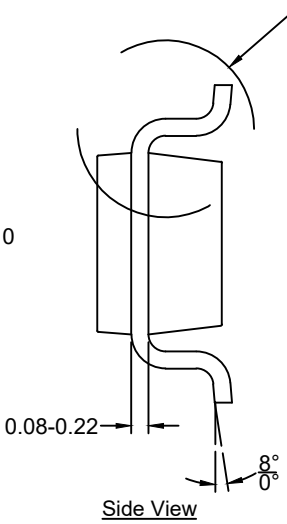
1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

Package Outline Drawing

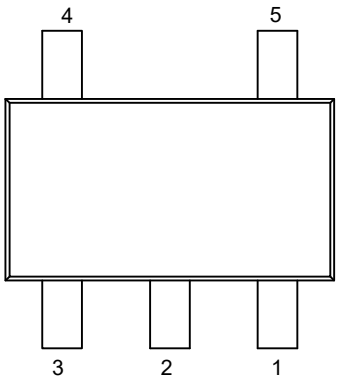
P5.064
KA0005AB
5-SOT 2.90 x 1.60 x 1.45 mm Body, 0.95mm Pitch Lead Small Outline Transistor Plastic Package
Rev04, Jul 22, 2025



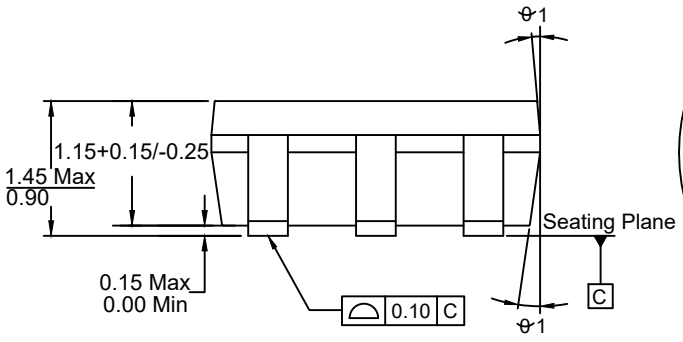
Top View



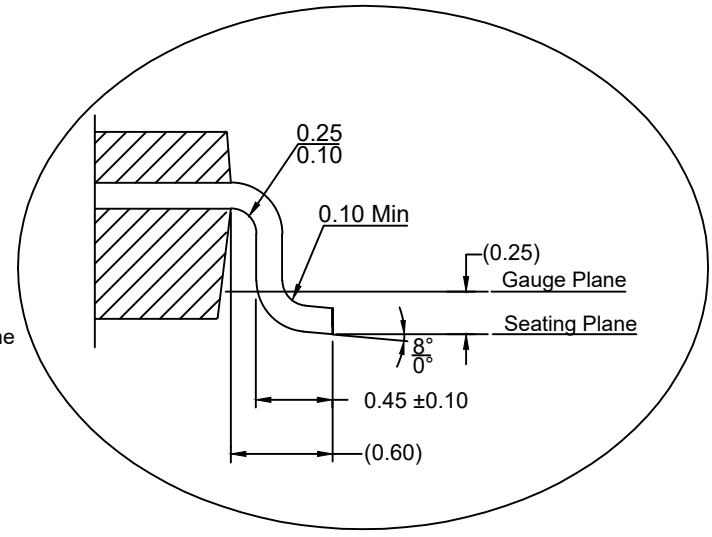
Side View



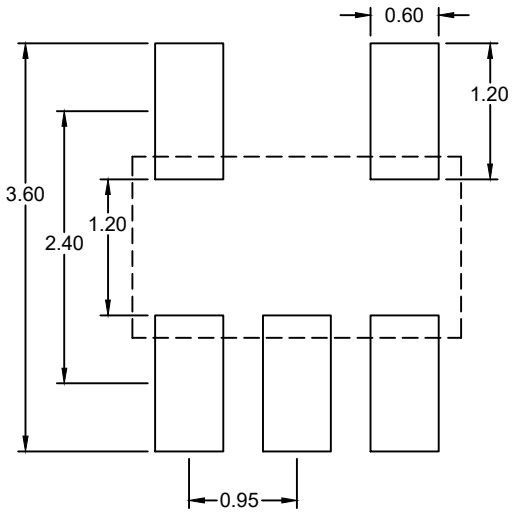
Bottom View



Side View



Detail "A"



Recommended Land Pattern

Notes:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA
3. Package length and width are exclusive of mold flash, protrusions or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: Millimeter.

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