To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RQM2201DNS

Silicon N Channel MOS FET
Power Switching

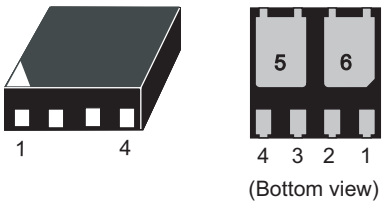
REJ03G1492-0200
Rev.2.00
Apr 16, 2007

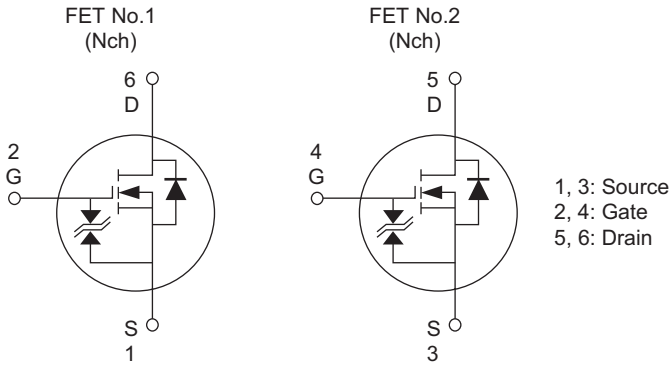
Features

- Small, thin and leadless type package (3 × 3 mm, t = 0.8 mm max.)
- Two FET chips are mounted in one package
- High density mounting
- High speed switching. (Ciss = 200 pF typ)
- V_{DSS} ≥ 60 V and capable of 2.5 V gate drive

Outline

RENESAS Package code: PWSN0006ZA-A
(Package name: WSON0303-6 <HWSON-6>)





Notes: 1. Marking is “M2201“.
2. The following maximum ratings and electric characteristics are applied to both FET1 and FET2.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±12	V
Drain current	I_D	2	A
Drain peak current	$I_{D(pulse)}$ Note1	8	A
Body - drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch Note2	1	W
Channel dissipation	Pch Note3	1.5	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, Duty cycle ≤ 1%
2. 1 Drive operation: When using the glass epoxy board (FR-4 40 × 40 × 1 mm)
3. 2 Drive operation: When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

Electrical Characteristics

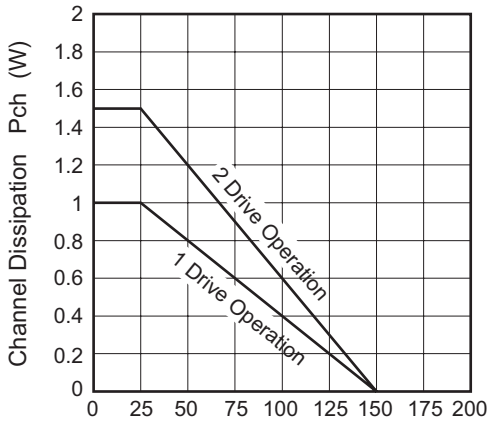
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	+12	—	—	V	I_G = +100 µA, V_{DS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	–12	—	—	V	I_G = –100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	+10	µA	V_{GS} = +10 V, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	–10	µA	V_{GS} = –10 V, V_{DS} = 0
Drain to source leak current	I_{DSS}	—	—	1	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	V_{DS} = 10 V, I_D = 1 mA
Drain to source on state resistance	$R_{DS(on)}$	—	173	225	mΩ	I_D = 1 A, V_{GS} = 4.5 V [Note4]
Drain to source on state resistance	$R_{DS(on)}$	—	207	290	mΩ	I_D = 1 A, V_{GS} = 2.5 V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	2.3	3.5	—	S	I_D = 1 A, V_{DS} = 10 V [Note4]
Input capacitance	Ciss	—	200	—	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	25	—	pF	
Reverse transfer capacitance	Crss	—	13	—	pF	
Turn - on delay time	$t_{d(on)}$	—	7	—	ns	I_D = 1 A V_{GS} = 10 V R_L = 10 Ω Rg = 4.7 Ω
Rise time	t_r	—	28	—	ns	
Turn - off delay time	$t_{d(off)}$	—	30	—	ns	
Fall time	t_f	—	4	—	ns	
Total gate charge	Qg	—	2.4	—	nC	V_{DD} = 10 V V_{GS} = 4.5 V I_D = 2 A
Gate to Source charge	Qgs	—	0.4	—	nC	
Gate to drain charge	Qgd	—	0.4	—	nC	
Body - drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 2 A, V_{GS} = 0 [Note4]

Notes: 4. Pulse test

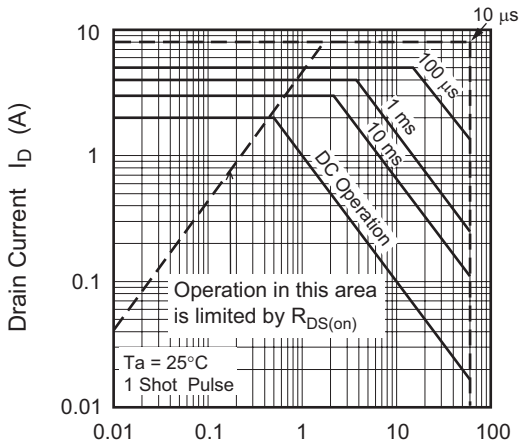
Main Characteristics

Maximum Channel Power Dissipation Curve

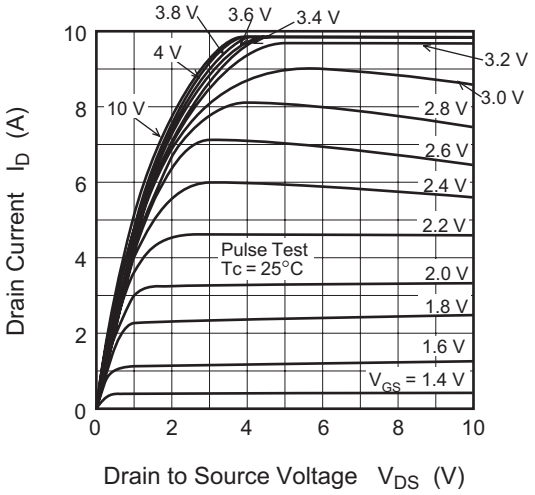


*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

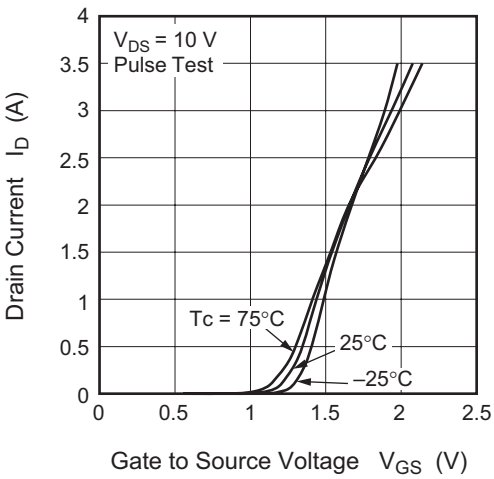
Maximum Safe Operation Area



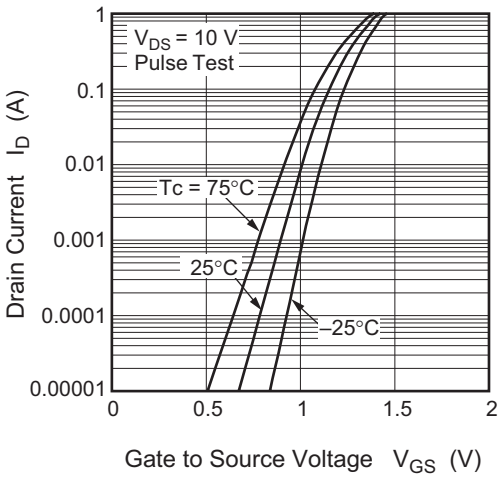
Typical Output Characteristics



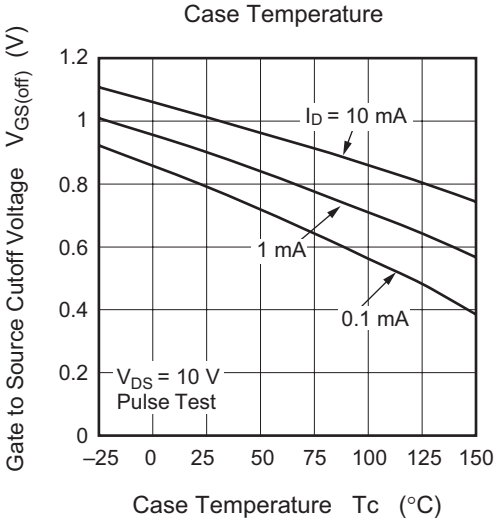
Typical Transfer Characteristics (1)



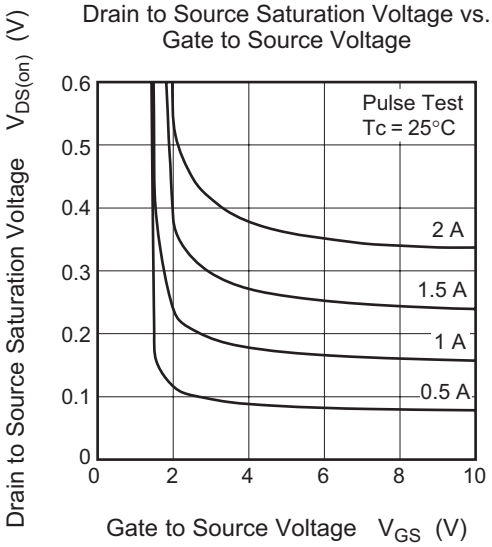
Typical Transfer Characteristics (2)



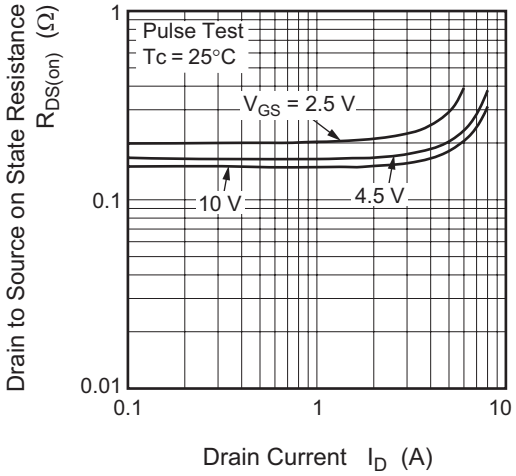
Gate to Source Cutoff Voltage vs. Case Temperature



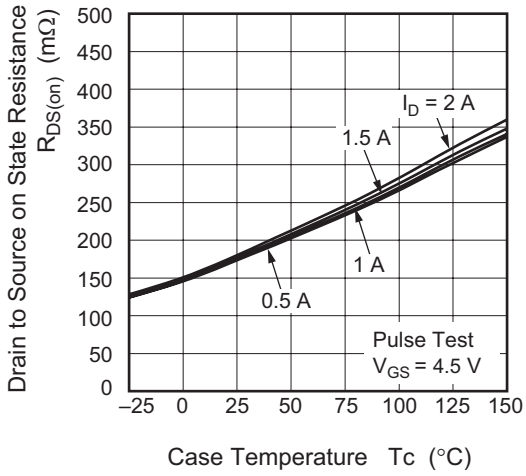
Drain to Source Saturation Voltage vs. Gate to Source Voltage



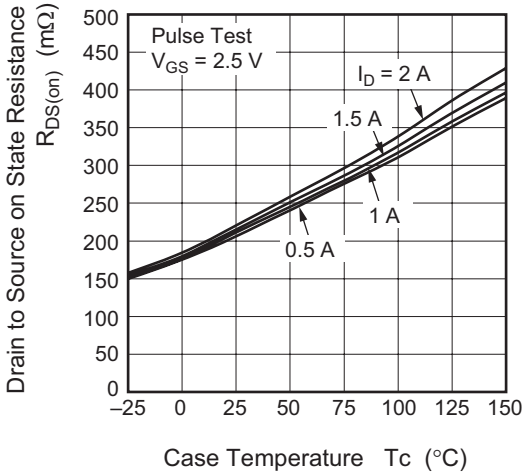
Static Drain to Source on State Resistance vs. Drain Current



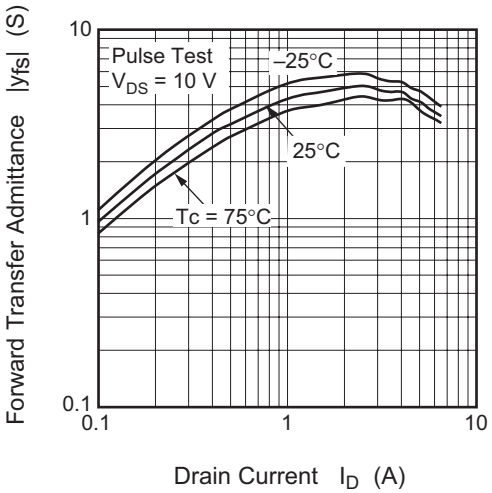
Static Drain to Source on State Resistance vs. Case Temperature



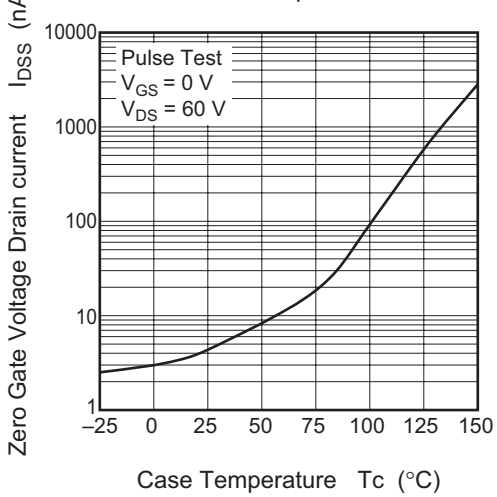
Static Drain to Source on State Resistance vs. Case Temperature



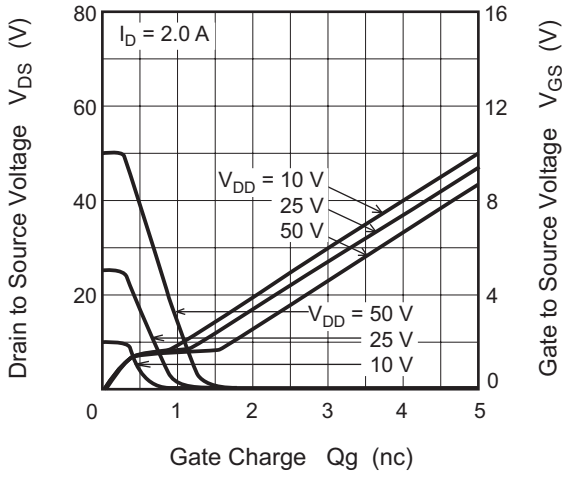
Forward Transfer Admittance vs. Drain Current



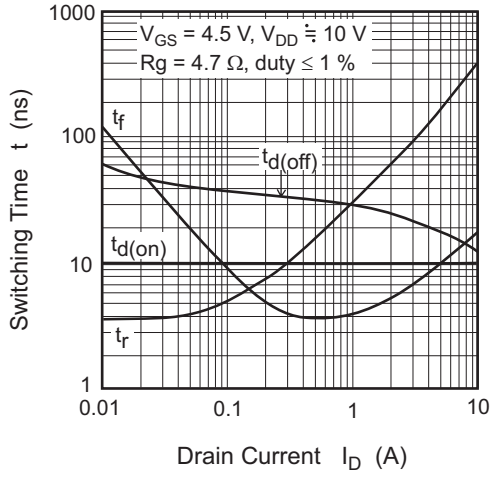
Zero Gate Voltage Drain current vs. Case Temperature



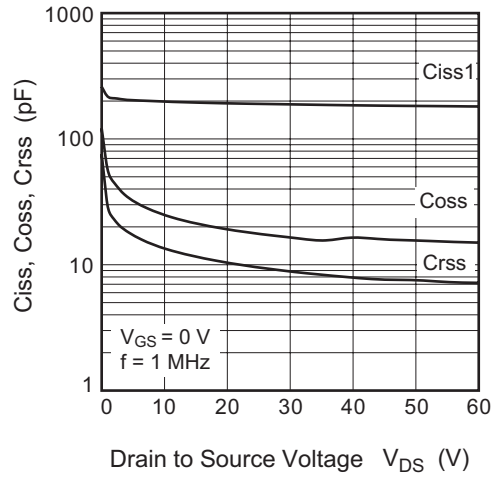
Dynamic Input Characteristics



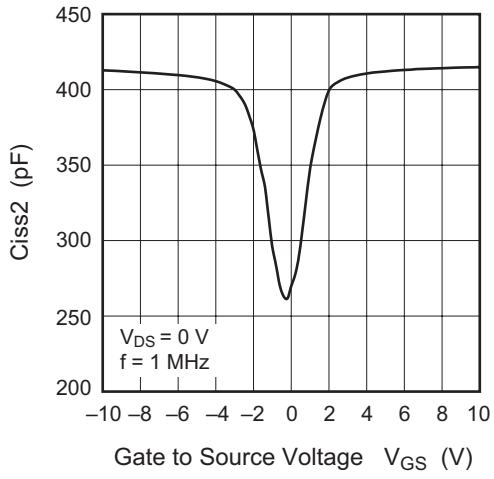
Switching Characteristics



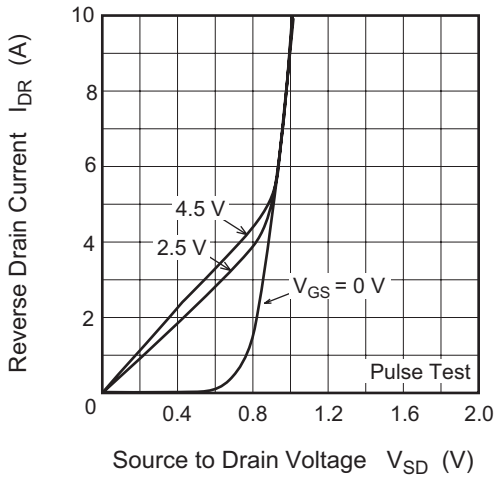
Typical Capacitance vs.
Drain to Source Voltage



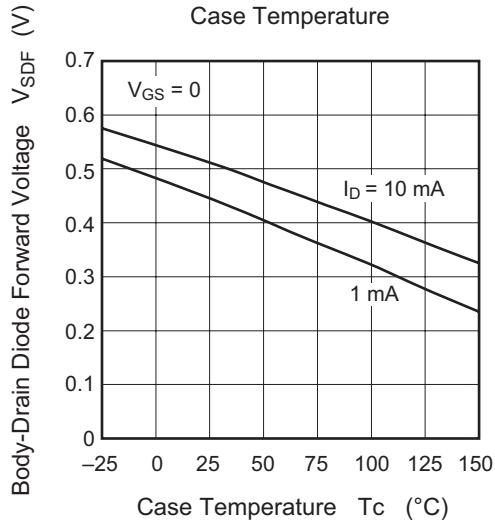
Input Capacitance vs.
Gate to Source Voltage



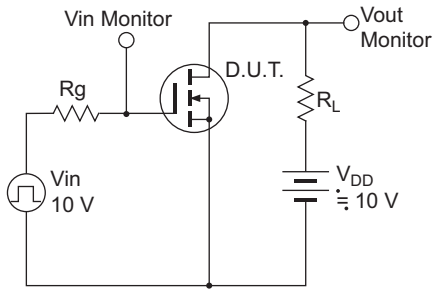
Reverse Drain Current vs.
Source to Drain Voltage



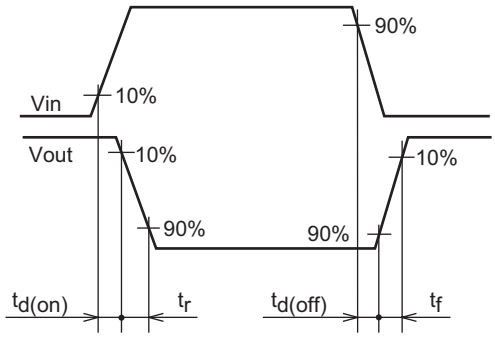
Body-Drain Diode Forward Voltage vs.
Case Temperature



Switching Time Test Circuit

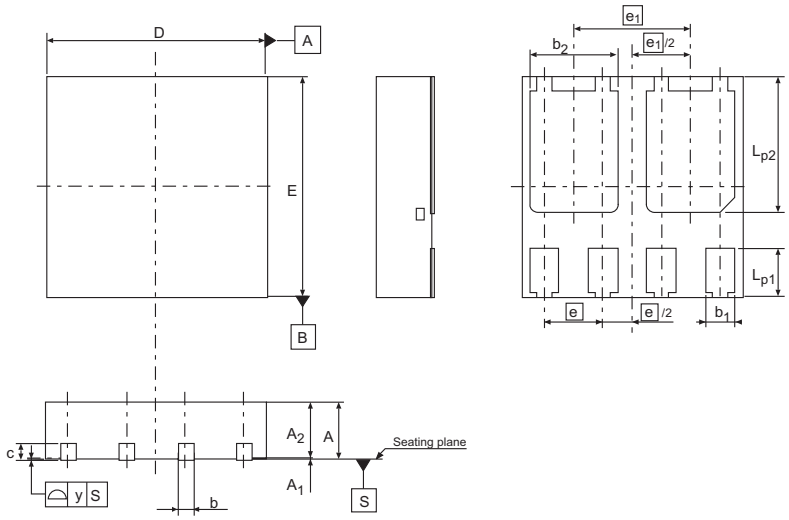


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
HWSON-6	P-HWSON6-3x3-0.80	PWSN0006ZA-A	—	0.022 g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.70	—	0.80
A_1	0	—	0.05
A_2	0.70	—	0.75
b	—	0.20	—
b_1	0.35	0.40	0.45
b_2	1.10	1.15	1.20
c	—	0.20	—
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	—	0.80	—
e_1	—	1.60	—
L_{p1}	0.55	—	0.75
L_{p2}	1.75	—	1.95
y	—	—	0.05

Ordering Information

Part No.	Quantity	Shipping Container
RQM2201DNSTL-E	2000 pcs.	ϕ178 mm reel, 8 mm Emboss taping
RQM2201DNSTR-E	2000 pcs.	ϕ178 mm reel, 8 mm Emboss taping

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http://www.renesas.com

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