RNA50C27A

CMOS System-Reset IC

R03DS0064EJ0100
Rev.1.00
Aug 03, 2012

Description

This IC facilitates complicated power-on and power-monitoring resets of microcomputers that require the 3.3-V and 1.8-V dual power supplies. It also facilitates change of delay time of reset signal by externally setting resistance and capacity for delay time. By employing complementary open-drain output, desired output such as open-drain output and CMOS output can be obtained.

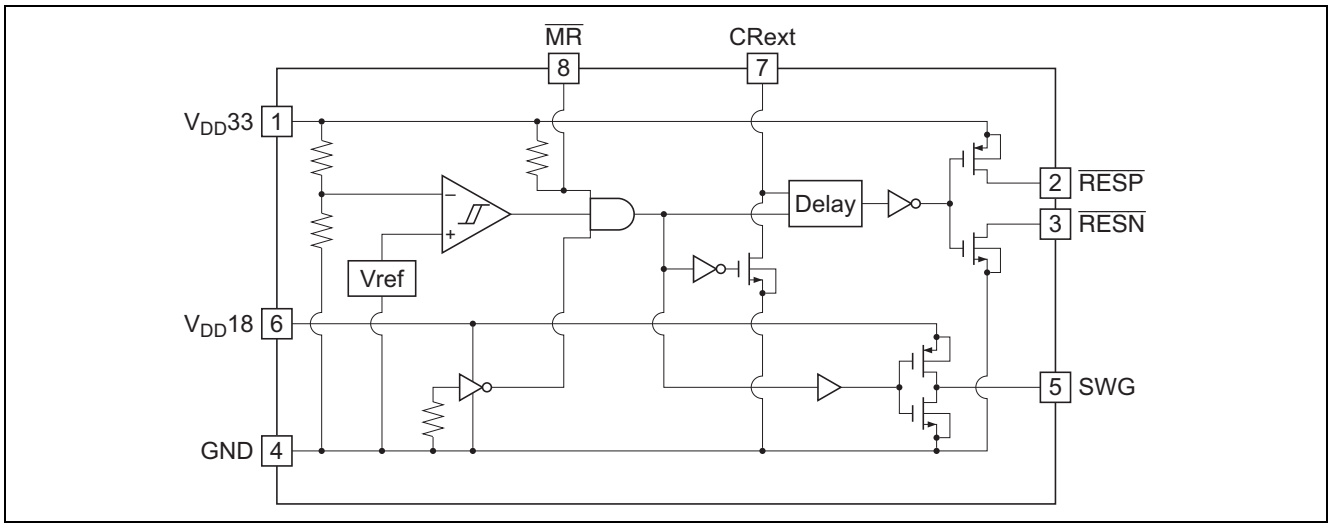
Functions

- 3.3-V detection voltage : 2.7 V
- Accuracy of 3.3-V detection voltage : ±1.0%
- Hysteresis of 3.3-V detection voltage : 5% Typ.
- 1.8-V detection voltage : 0.9 V Typ.
- Open-drain/CMOS output
- 1.8-V PMOS drive output
- Package : 8-pin SSOP-8/MMPAK-8
- Operating temperature : –40 to +85°C

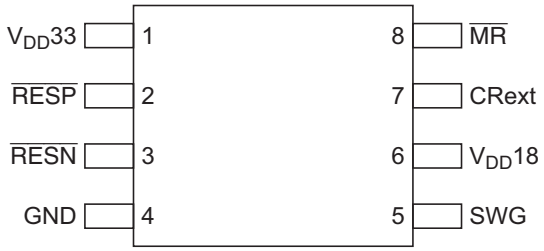
Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA50C27AUSEL-E	SSOP-8	PVSP0008KA-A	US	EL (3,000 pcs / Reel)	E (Sn-Bi)
RNA50C27AMMEL-E	MMPACK-8	PLSP0008JC-A	MM	EL (3,000 pcs / Reel)	E (Sn-Bi)

Block Diagram



Pin Arrangement



(Top view)

Pin Description

Pin No.	Pin Name	Function
1	V_{DD}33	Input power supply pin for 3.3 V voltage. Recommended operating range is V_{TH}33 to 3.6 V. Set input voltage to 0.033 V/μs or less when starting up. If input voltage terminal V_{DD}33 was momentary (V_{DD}33 pin input voltage is lower than detection voltage state period of short), for discharge of external capacitance becomes insufficient, delay time will be very short. Please check if there is any problem as a system.
2	$\overline{RESP}$	Pull-down when reset signal output pin. By connecting to $\overline{RESN}$ pin, CMOS output can be used.
3	$\overline{RESN}$	Pull-up when reset signal output pin. By connecting to $\overline{RESP}$ pin, CMOS output can be used.
4	GND	GND pin
5	SWG	To be installed between 1.8 V power supply and 1.8 V voltage input of microcomputer, gate of PMOS is external control signal. It has been designed with load capacity of 2200 pF Typ., will change size of rise time/fall time of SWG capacity.
6	V_{DD}18	Input power supply pin for 1.8 V voltage. Recommended operating range is 1.65 V to V_{DD}33. When terminal voltage is below 0.9 V Typ, and outputs high-level signal SWG.
7	CRext	Terminal is for determining Rext resistance and Cext capacitance of reset signal delay time. Resistance is recommended for more than 3.3 kΩ. Delay time is given by tDLY = Cext × Rext [s] Does not output reset signal when this pin is not high-level. Connect external resistor for V_{DD}33 necessarily.
8	$\overline{MR}$	This terminal outputs a reset signal manually. Has been pull-up internally 2 MΩ. If behavior is unstable, behavior is stabilized by connecting 220 pF to this pin to GND. In addition, or when connected to potential, such as V_{DD}33 to force this pin to external, pulse width input to the $\overline{MR}$ be shorter than discharge time of CRext is, please note for delay normal can not be obtained.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Terminal	Ratings	Unit	Remarks
Supply voltage	$V_{DD}33$	$V_{DD}33$	4.6	V	
	$V_{DD}18$	$V_{DD}18$	4.6		
Input voltage	V_I	$\overline{MR}$, CRext	–0.3 to $V_{DD}33$	V	
Output voltage	V_O	$\overline{RESP}$, $\overline{RESN}$	–0.3 to $V_{DD}33$	V	
		SWG	–0.3 to $V_{DD}18$		
Input current	I_I	$\overline{MR}$, CRext	20	mA	
Output current	I_O	$\overline{RESP}$, $\overline{RESN}$, SWG	20	mA	
Supply current	I_{DD}	$V_{DD}33$, $V_{DD}18$	25	mA	
Power dissipation	P_T	—	160	mW	SSOP-8
			145		MMPAK-8
Storage temperature	Tstg	—	–55 to +125	°C	

Recommended Operating Conditions

(Ta = 25°C)

Item	Symbol	Terminal	Min	Typ	Max	Unit	Remarks
Supply voltage	$V_{DD}33$	$V_{DD}33$	$V_{TH}33$	—	3.6	V	
	$V_{DD}18$	$V_{DD}18$	1.65	—	$V_{DD}33$		
Input voltage	V_I	$\overline{MR}$, CRext	0	—	$V_{DD}33$	V	
Output voltage	V_O	$\overline{RESP}$	0	—	$V_{DD}33$	V	
		$\overline{RESN}$	0	—	$V_{DD}33$		
		SWG	0	—	$V_{DD}18$		
External resistor	Rext	CRext	3.3	—	—	kΩ	$V_{DD}33$ = 3.3V
External capacitor	Cext	CRext	—	Nolimit	—	F	
MR pin capacitor	$C_{\overline{MR}}$	$\overline{MR}$	—	220	—	pF	
Drivable capacitor	C_L	SWG	—	2200	—	pF	SWG output
Operating temperature	Ta	—	–40	—	85	°C	

Electrical Characteristics

DC Characteristics

($V_{DD}33$ = 3.3V, $V_{DD}18$ = 1.8V, Ta = 25°C, Rext = 10kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Quiescent supply current		$I_{DD}33$	0.6	2.0	8.0	μA	
		$I_{DD}18$	0.3	1.0	3.0		
Detection voltage		$V_{TH}33$	2.673	2.700	2.727	V	
		$V_{TH}18H$	1.2	—	—		
		$V_{TH}18L$	—	—	0.6		
Detection voltage temperature dependency		$\frac{\Delta V_{TH}33}{V_{TH}33 \cdot \Delta Ta}$	—	(±100)	—	ppm/°C	
Detection voltage hysteresis		V_{HYS}	$V_{TH}33\times1.03$	$V_{TH}33\times1.05$	$V_{TH}33\times1.08$	V	
$\overline{MR}$	Low-level input voltage	V_{IL}	—	—	0.495	V	
	High-level input voltage	V_{IH}	2.805	—	—	V	
	Internal pull-up resistance	RMR	—	(2.0)	—	MΩ	
CMOS	Low-level output current	I_{OL}	5	15	20	mA	V_O = 0.5V
	High-level output current	I_{OH}	5	10	13		V_O = 2.8V
$\overline{RESP}$	Output leakage current	I_{OLEAK}	—	(0.1)	—	μA	V_O = 0.5V
	High-level output current	I_{OH}	5	10	13	mA	V_O = 2.8V
$\overline{RESN}$	Low-level output current	I_{OL}	5	15	20	mA	V_O = 0.5V
	Output leakage current	I_{OLEAK}	—	(0.1)	—	μA	V_O = 2.8V
SWG	Low-level output current	I_{OL}	0.2	0.35	0.6	mA	V_O = 0.5V
	High-level output current	I_{OH}	1.0	3.0	6.0		V_O = 1.3V
	Low-level output voltage	V_{OL}	—	—	0.1	V	SWG = OPEN
	High-level output voltage	V_{OH}	1.7	—	—		

Note: When the voltage within $V_{IL} < V_{IN} < V_{IH}$ is applied to $\overline{MR}$ and $V_{DD}18$ input by DC, oscillation may occur.
When $\overline{RESP}$ output and $\overline{RESN}$ short out and CMOS output is used.

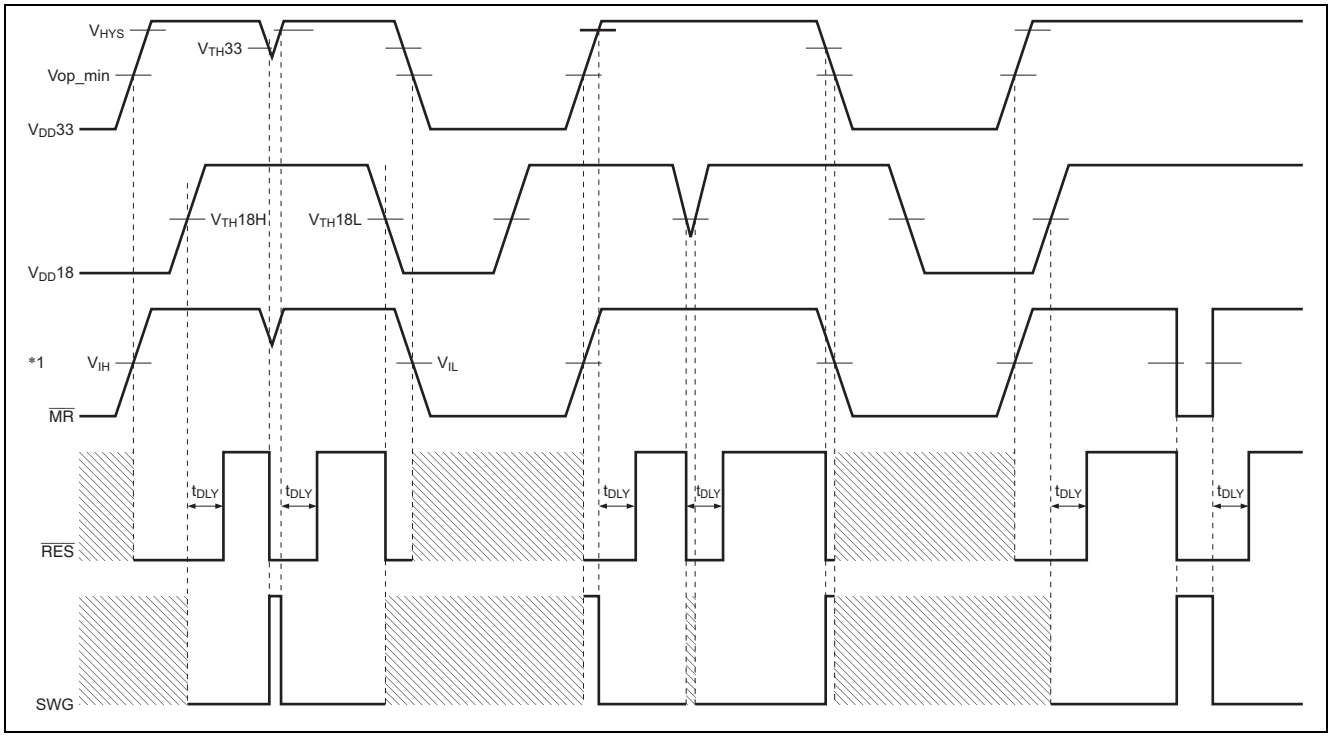
AC Characteristics

($V_{DD}33$ = 3.3V, $V_{DD}18$ = 1.8V, Ta = 25°C, Rext = 10kΩ, R_L = 100kΩ, C_L = 15pF)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
CMOS	Propagation delay time	tpLH	—	—	(500) *1	μs	
		tpHL	—	—	(100) *1		
	Response time	tr	—	—	(100) *1	ns	
		tf	—	—	(100) *1		
$\overline{RESP}$	Propagation delay time	tpLH	—	—	500 *2	μs	
		tpHL	—	—	(100) *3		
	Response time	tr	—	—	(100) *3	ns	
		tf	—	—	(100) *3	μs	
$\overline{RESN}$	Propagation delay time	tpLH	—	—	500 *2	μs	
		tpHL	—	—	(100) *3		
	Response time	tr	—	—	(100) *3	μs	
		tf	—	—	(100) *3	ns	
SWG	Propagation delay time	tpHL	—	—	500 *2	μs	C_L = 2200pF
		tpLH	—	—	100 *2		
	Response time	tf	—	(10) *3	—	μs	C_L = 2200pF
		tr	—	(5) *3	—		
Delay time		tDLY	—	(93) *2	—	ms	Cext = 0.1μF, Rext = 1MΩ

Notes: ( ) is a design reference value.
*1 Estimated from measured value of $\overline{RESP}$, $\overline{RESN}$ (Will vary considerably depending on conditions).
*2 Edge is triggered 0 V→3.3 V, 3.3 V→0 V when change of maximum delay path $V_{DD}33$.
*3 Signal to trigger $\overline{MR}$.

Timing Chart



Note: $\overline{MR}$ has been pulled up to V_{CC} by the internal resistance. Timing diagram is in phase with signal of $V_{DD}33$.

Table of Graphs

DC Characteristics

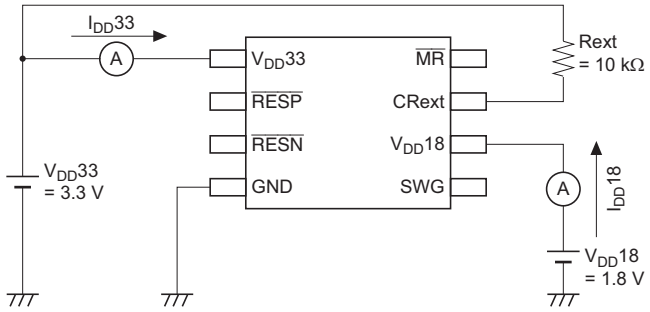
Item		Symbol	vs. $V_{DD}33$	vs. $V_{DD}18$	vs. Ta	Other	Test Circuit
Quiescent supply current		$I_{DD}33$	Fig. 1-1	—	Fig. 3-1	—	1
		$I_{DD}18$	—	Fig. 2-1	Fig. 3-2	—	1
Detection voltage		$V_{TH}33$	—	—	Fig. 3-3	—	2
		$V_{TH}18H$	—	—	Fig. 3-5	—	3
		$V_{TH}18L$	—	—	Fig. 3-5	—	3
Detection voltage temperature dependency			—	—	—	—	2
Detection voltage hysteresis		V_{HYS}	—	—	Fig. 3-4	—	2
$\overline{MR}$	Input voltage	V_{IL}	Fig. 1-2, 3	—	Fig. 3-6	—	4
		V_{IH}	Fig. 1-2, 3	—	Fig. 3-6	—	4
	Internal pulled-up resistor	RMR	—	—	Fig. 3-7	—	5
$\overline{RESP}$	Output current	I_{OLEAK}	Fig. 1-4	—	Fig. 3-8	—	8
		I_{OH}	Fig. 1-5	—	Fig. 3-9	—	7
$\overline{RESN}$	Output current	I_{OL}	Fig. 1-6	—	Fig. 3-10	—	6
		I_{OLEAK}	Fig. 1-7	—	Fig. 3-11	—	9
SWG	Output current	I_{OL}	—	Fig. 2-2	Fig. 3-12	—	13
		I_{OH}	—	Fig. 2-3	Fig. 3-13	—	11

AC Characteristics

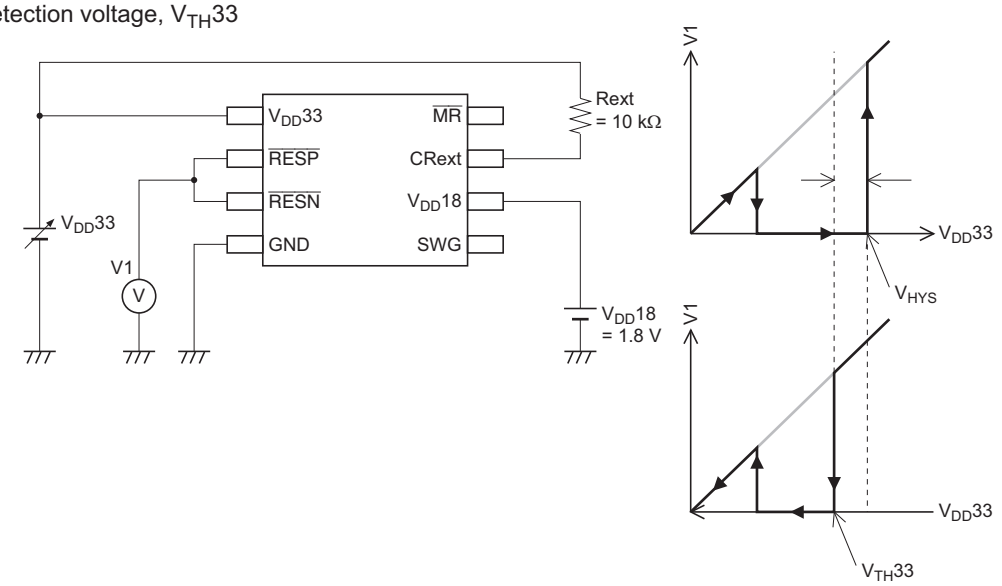
Item		Symbol	vs. $V_{DD}33$	vs. $V_{DD}18$	vs. Ta	Other	Test Circuit
$\overline{RESP}$	Propagation delay time	tpLH	Fig. 1-8	—	Fig. 3-14	—	14
		tpHL	Fig. 1-9	—	Fig. 3-15	—	17
	Response time	tr	Fig. 1-10	—	Fig. 3-16	—	20
		tf	Fig. 1-11	—	Fig. 3-17	—	23
$\overline{RESN}$	Propagation delay time	tpLH	Fig. 1-12	—	Fig. 3-18	—	15
		tpHL	Fig. 1-13	—	Fig. 3-19	—	18
	Response time	tr	Fig. 1-14	—	Fig. 3-20	—	21
		tf	Fig. 1-15	—	Fig. 3-21	—	24
SWG	Propagation delay time	tpHL	Fig. 1-16	—	Fig. 3-22	—	16
		tpLH	Fig. 1-17	—	Fig. 3-23	—	19
	Response time	tf	Fig. 1-18	—	Fig. 3-24	—	22
		tr	Fig. 1-19	—	Fig. 3-25	—	25
Delay time		tDLY	Fig. 1-20	Fig. 2-4	Fig. 3-26	Fig. 4-1	26

Test Circuits

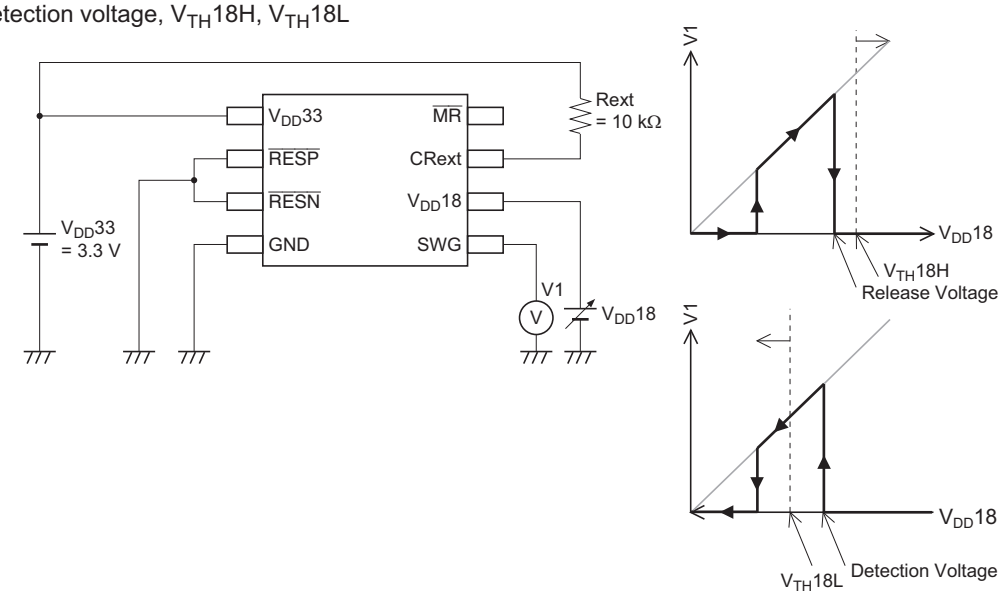
1. Quiescent supply curren, $I_{DD}33$, $I_{DD}18$



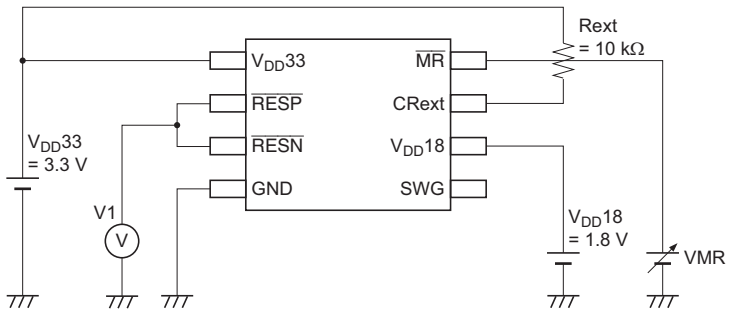
2. Detection voltage, $V_{TH}33$

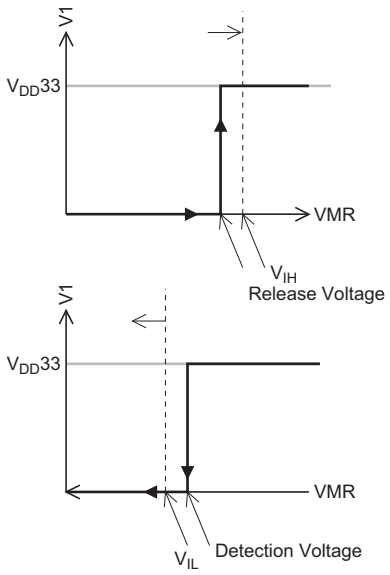


3. Detection voltage, $V_{TH}18H$, $V_{TH}18L$

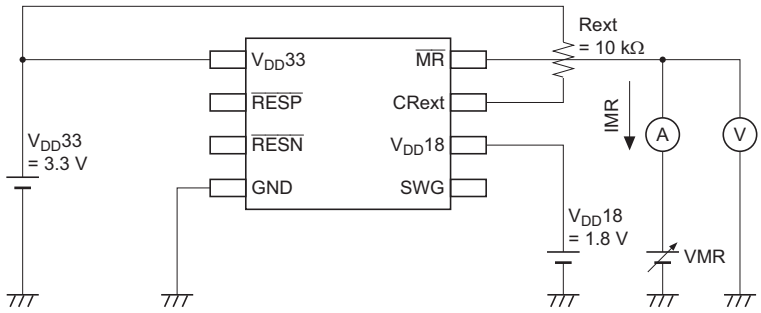


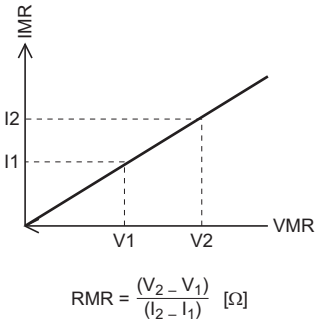
4. $\overline{MR}$ pin Input voltage Low-level / High-level, V_{IL}/V_{IH}



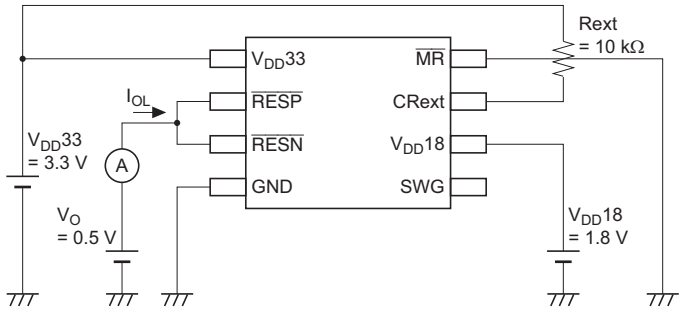


5. $\overline{MR}$ pin Internal pulled-up resistor, RMR

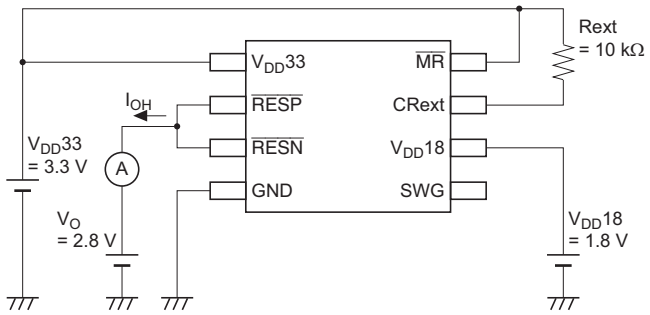




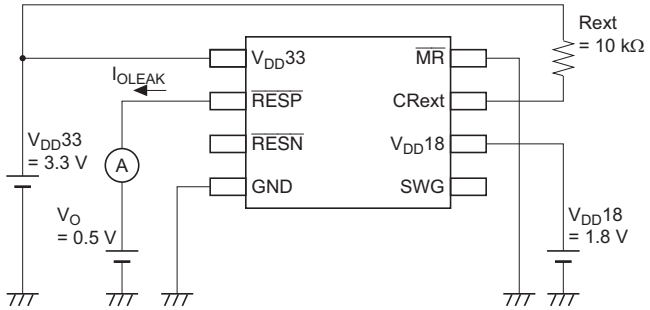
6. CMOS($\overline{RESN}$) Output current Low-level, I_{OL}



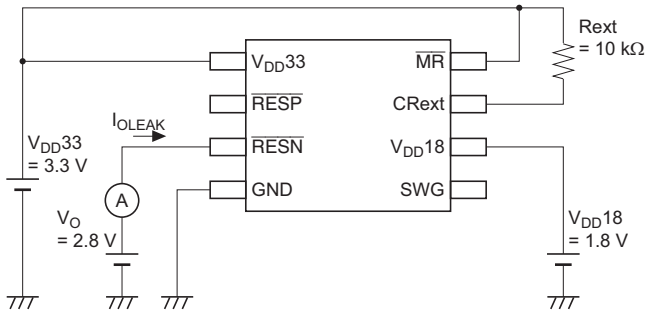
7. CMOS($\overline{\text{RESP}}$) Output current High-level, I_{OH}



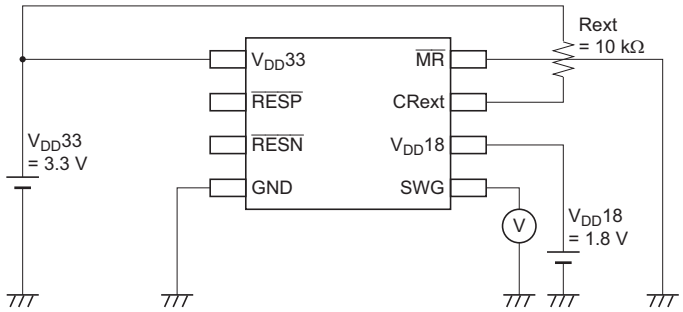
8. $\overline{\text{RESP}}$ pin Output leakage current, I_{OLEAK}



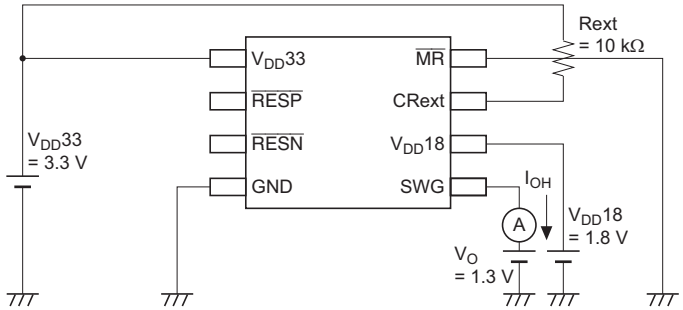
9. $\overline{\text{RESN}}$ pin Output leakage current, I_{OLEAK}



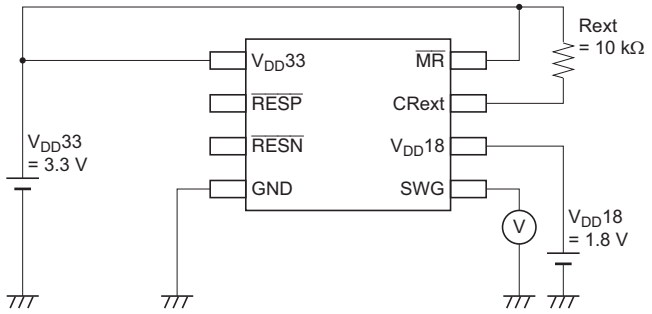
10. SWG Output voltage High-level, V_{OH}



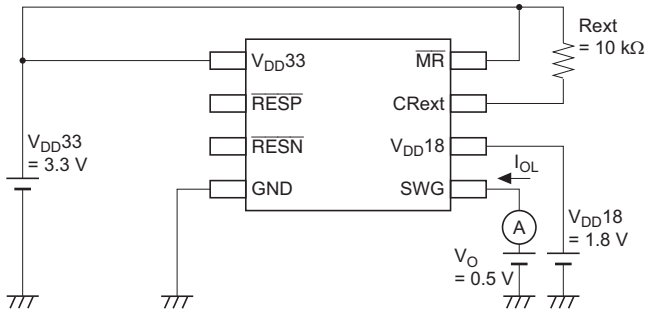
11. SWG pin Output current High-level, I_{OH}



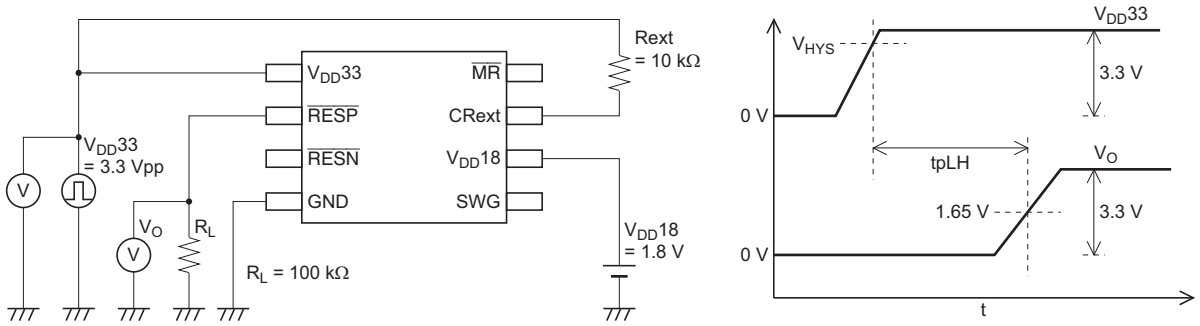
12. SWG Output voltage Low-level, V_{OL}



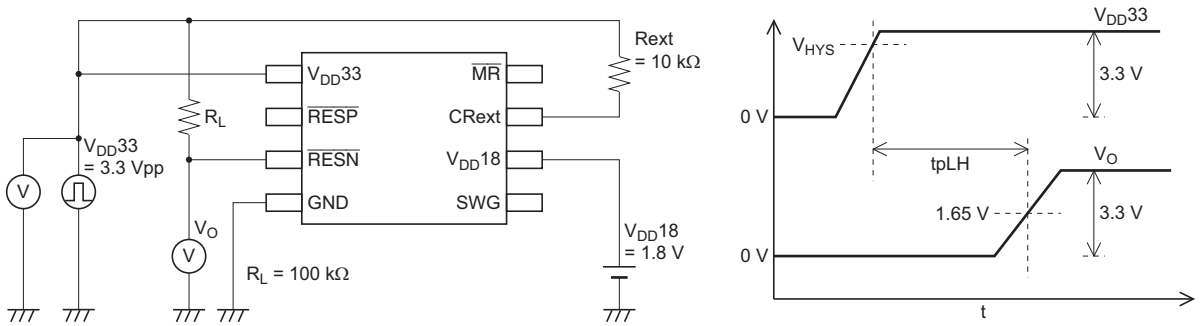
13. SWG pin Output current Low-level, I_{OL}



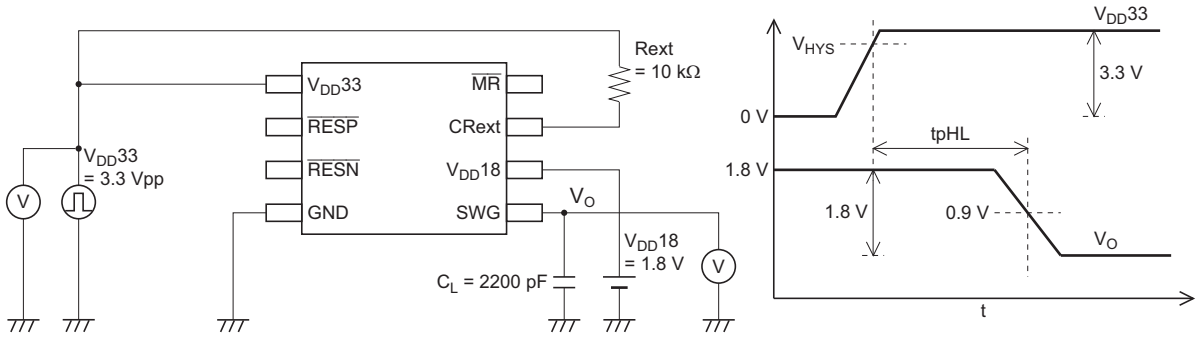
14. Propagation delay time $\overline{RESP}$, tpLH



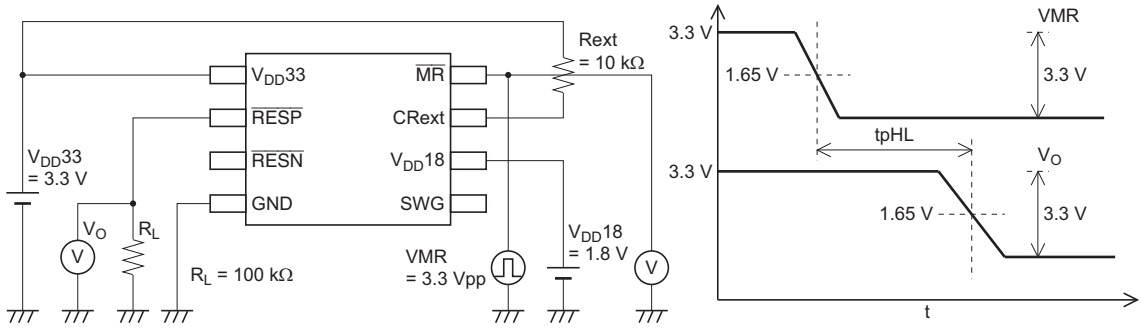
15. Propagation delay time $\overline{RESN}$, tpLH



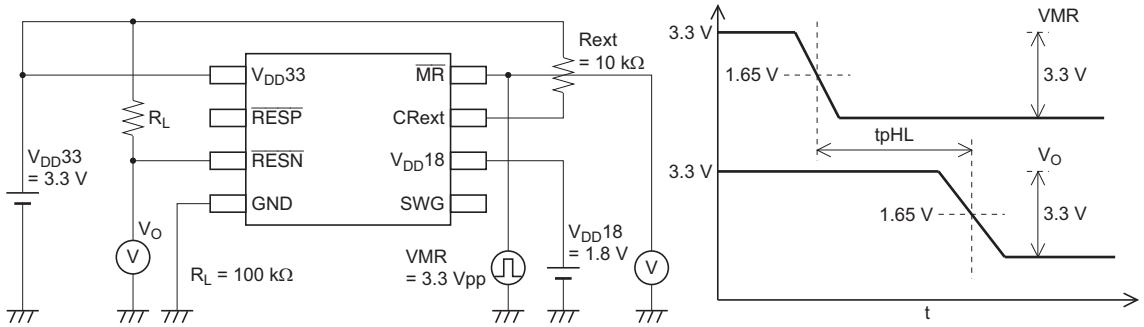
16. Propagation delay time SWG, tpHL



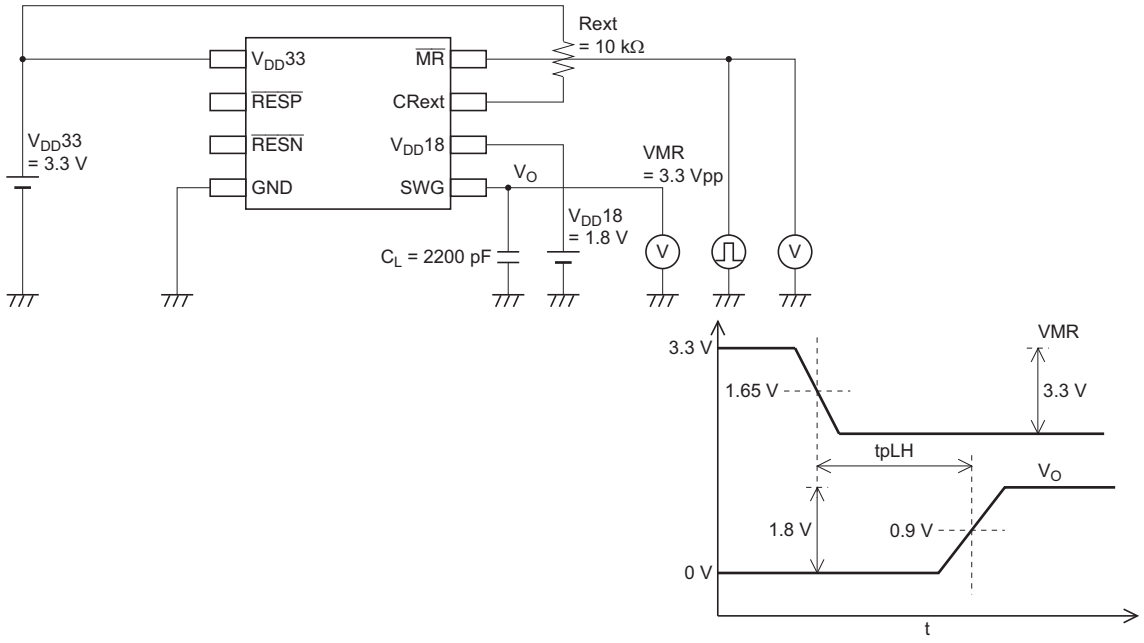
17. Propagation delay time $\overline{RESP}$, tpHL



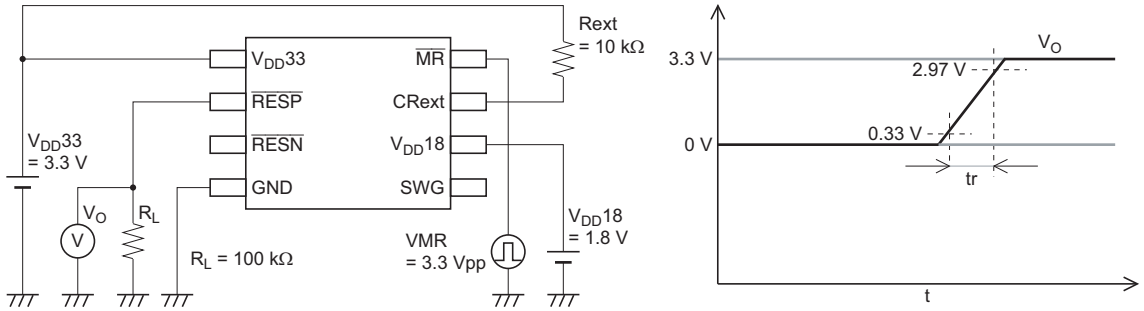
18. Propagation delay time $\overline{RESN}$, tpHL



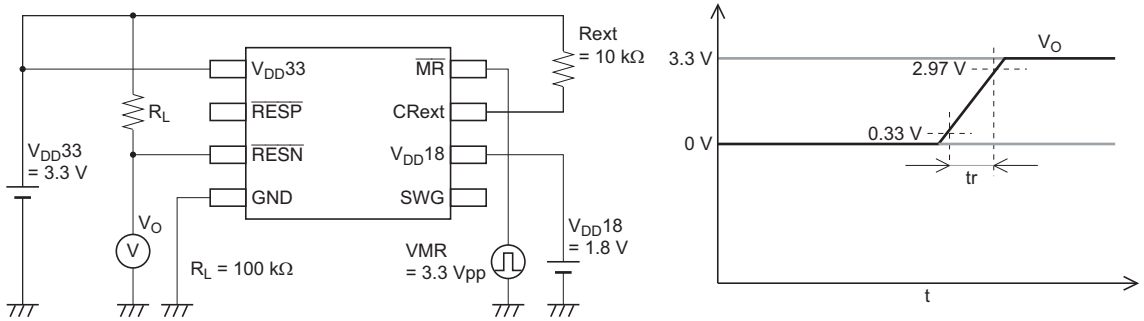
19. Propagation delay time SWG, tpLH



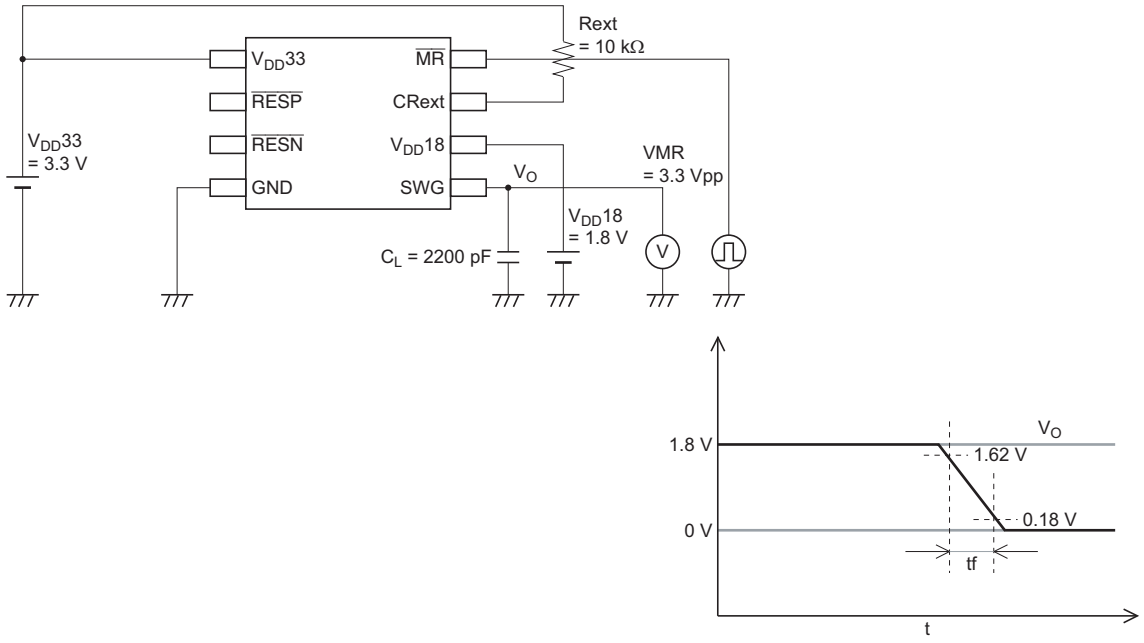
20. Rising Response time $\overline{RESP}$, tr



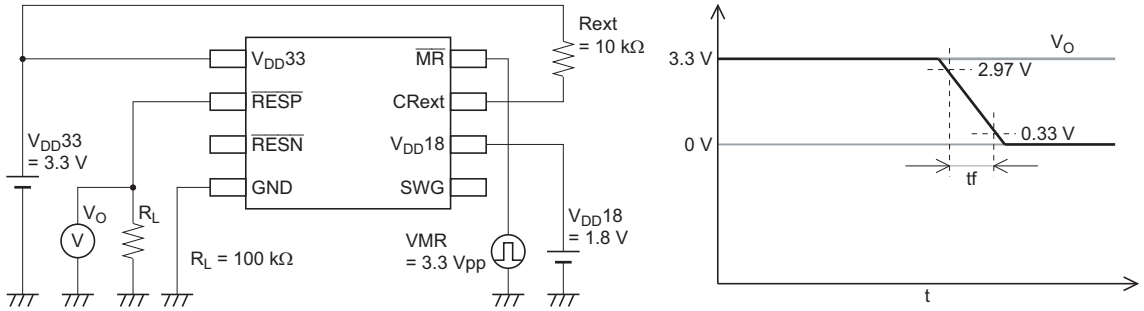
21. Rising Response time $\overline{RESN}$, tr



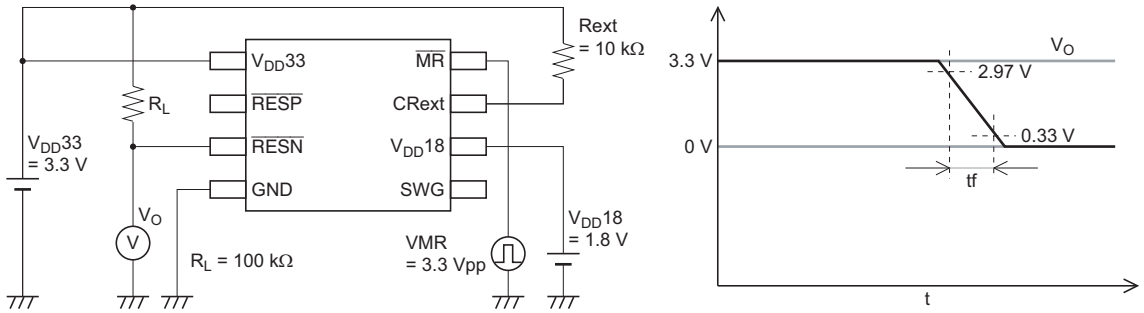
22. Falling Response time SWG, tf



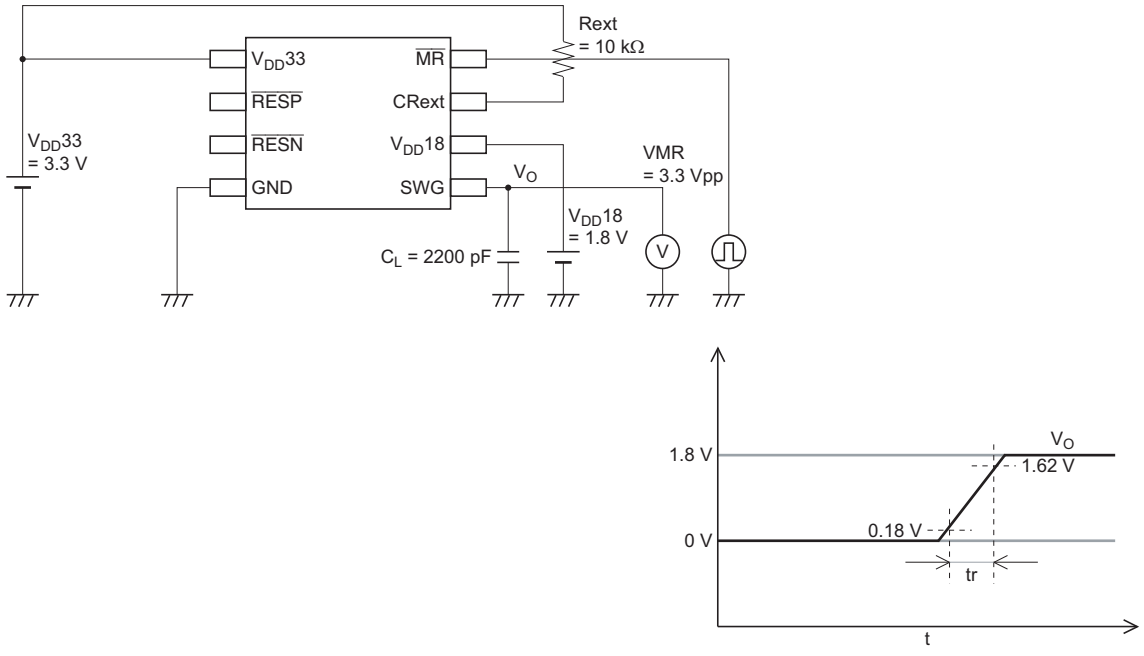
23. Falling Response time $\overline{RESP}$, tf



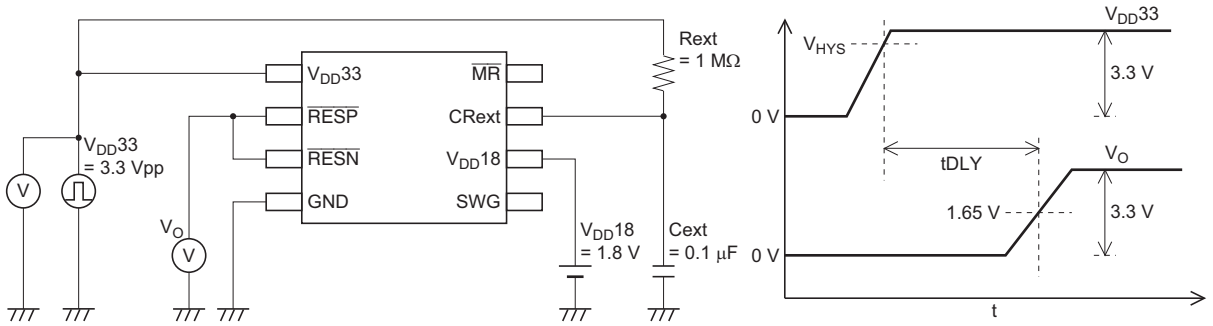
24. Falling Response time $\overline{RESN}$, tf



25. Falling Response time SWG, tr



26. Delay time, tDLY



Main Characteristics

Figure 1-1.
Supply Current vs. Supply Voltage

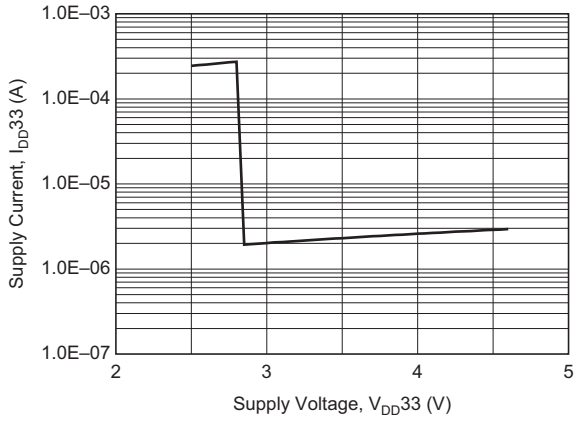


Figure 1-2.
Manual Reset Threshold Voltage of Reset Output vs. Supply Voltage

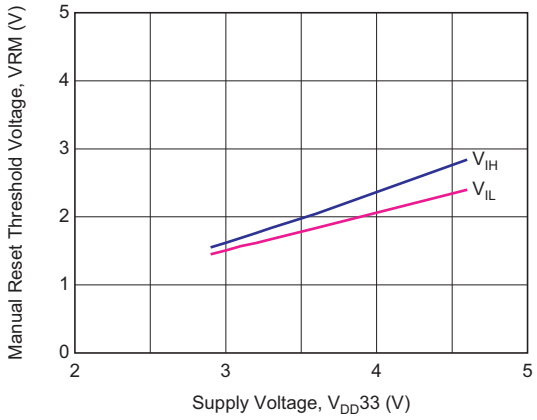


Figure 1-3.
Manual Reset of Output Threshold Voltage SWG vs. Supply Voltage

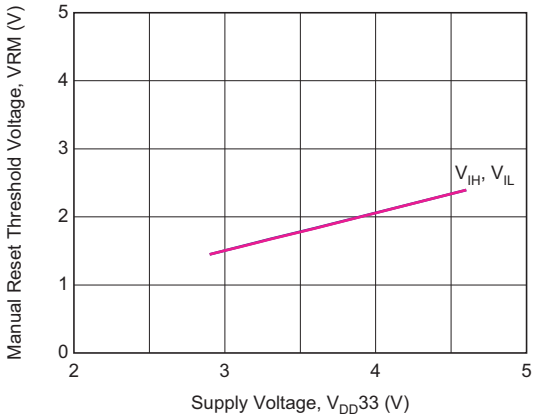


Figure 1-4.
$\overline{\text{RESP}}$ Output Leakage Current vs. Output Voltage

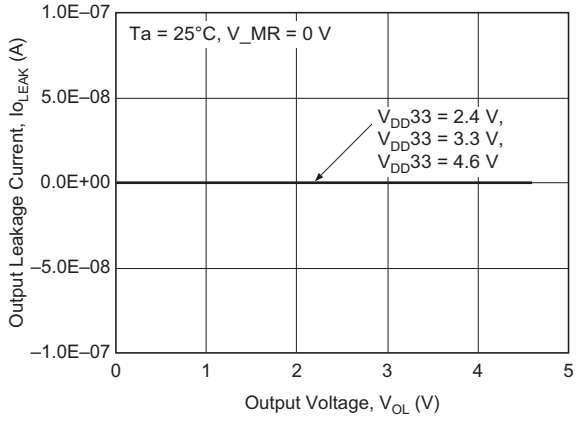


Figure 1-5.
$\overline{\text{RESP}}$ Output Current vs. Output Voltage

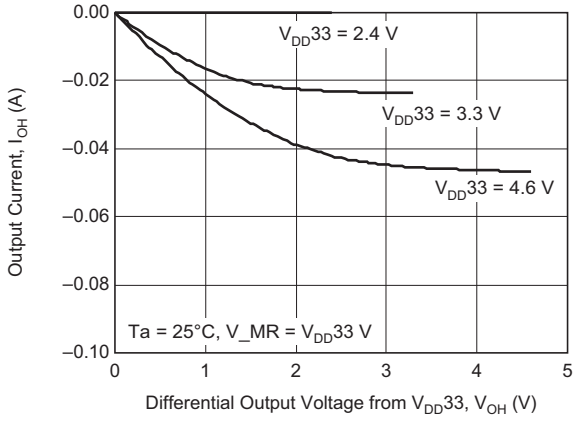


Figure 1-6.
$\overline{\text{RESN}}$ Output Current vs. Output Voltage

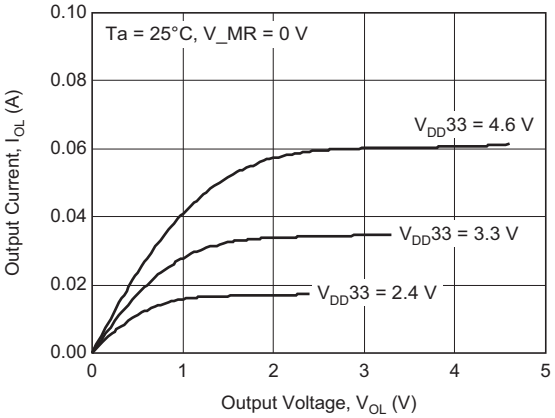


Figure 1-7.
$\overline{\text{RESN}}$ Output Leakage Current vs. Output Voltage

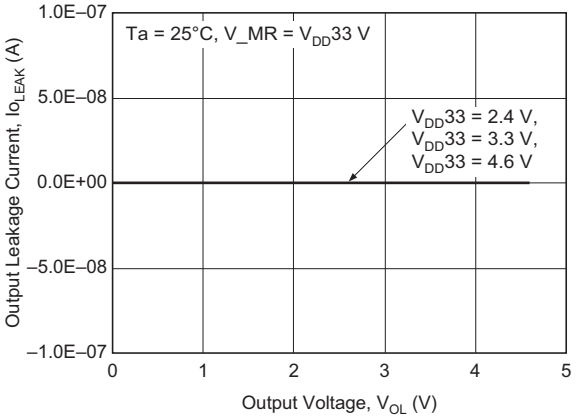


Figure 1-8.
$\overline{\text{RESP}}$ Output Rising Propagation Delay Time vs. Supply Voltage

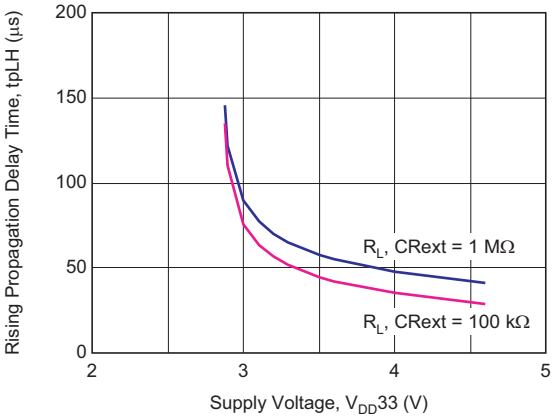


Figure 1-9.
$\overline{\text{RESP}}$ Output Falling Propagation Delay Time vs. Supply Voltage

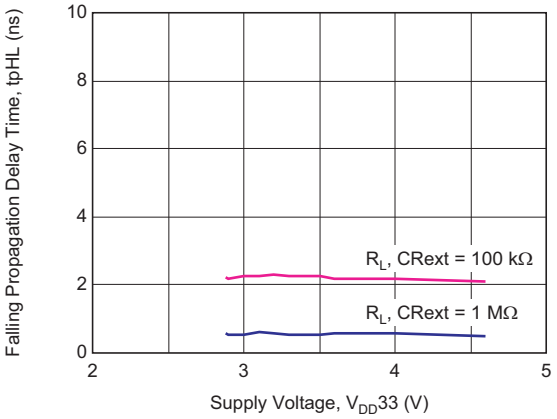


Figure 1-10.
$\overline{\text{RESP}}$ Output Rising Response Time vs. Supply Voltage

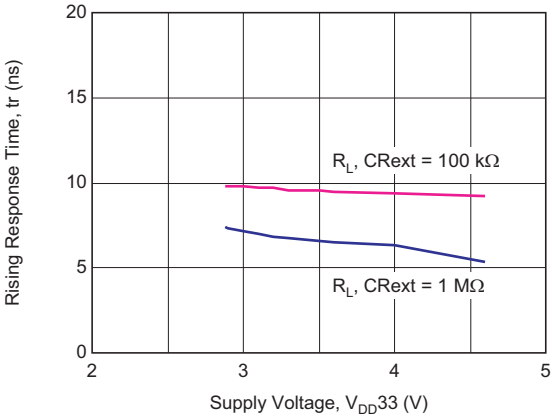


Figure 1-11.
$\overline{\text{RESP}}$ Output Falling Response Time vs. Supply Voltage

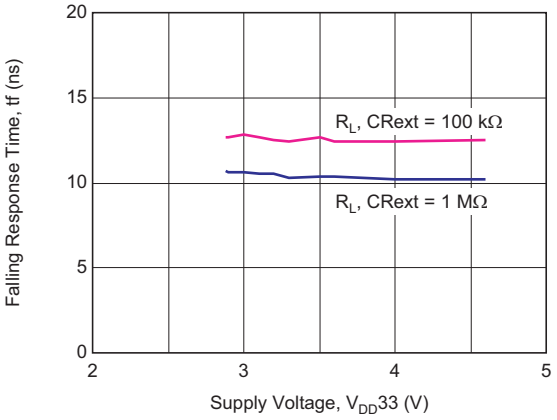


Figure 1-12.
$\overline{\text{RESN}}$ Output Rising Propagation Delay Time vs. Supply Voltage

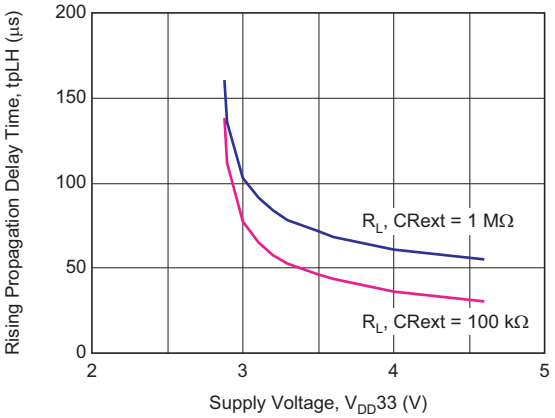


Figure 1-13.
$\overline{\text{RESN}}$ Output Falling Propagation Delay Time vs. Supply Voltage

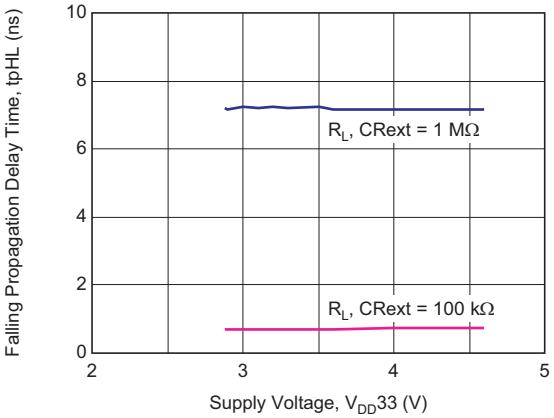


Figure 1-14.
$\overline{\text{RESN}}$ Output Rising Response Time vs. Supply Voltage

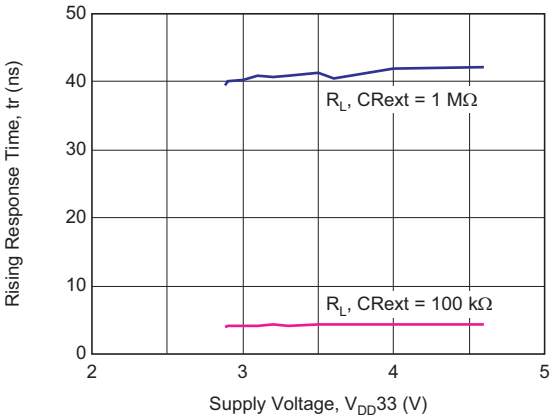


Figure 1-15.
$\overline{\text{RESN}}$ Output Falling Response Time vs. Supply Voltage

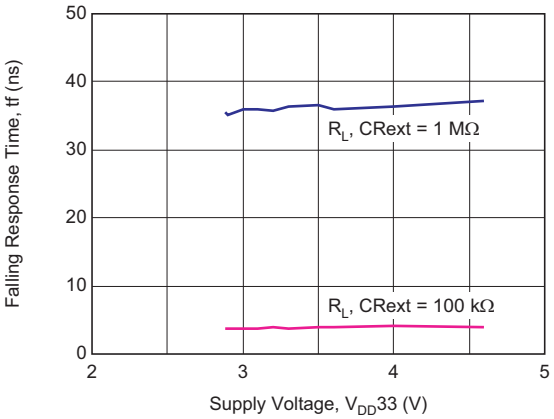


Figure 1-16.
SWG Output Rising Propagation Delay Time vs. Supply Voltage

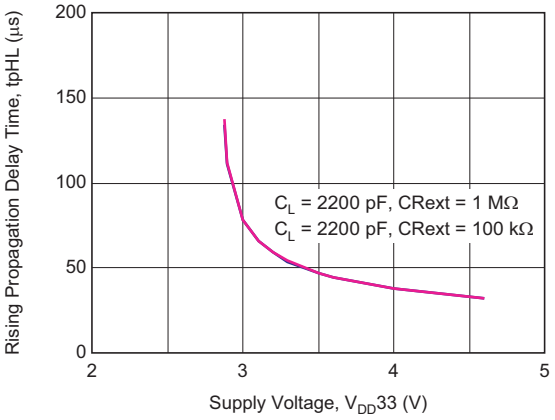


Figure 1-17.
SWG Output Falling Propagation Delay Time vs. Supply Voltage

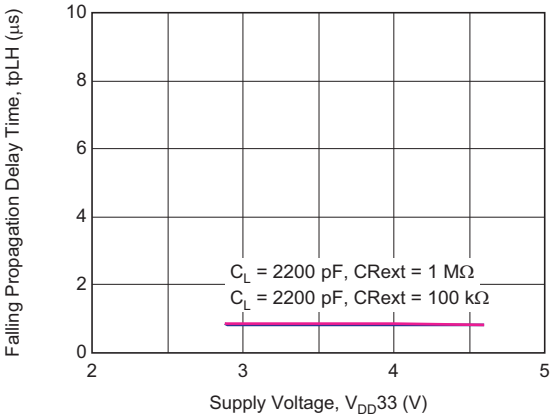


Figure 1-18.
SWG Output Rising Response Time vs. Supply Voltage

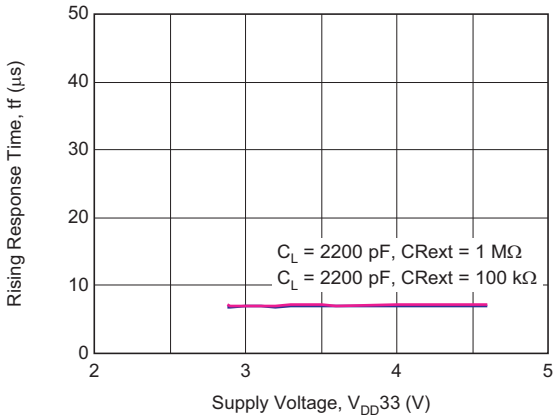


Figure 1-19.
SWG Output Falling Response Time vs. Supply Voltage

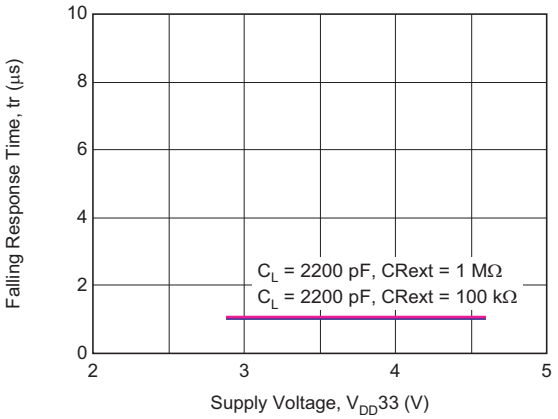


Figure 1-20.
Reset Output Delay Time vs. Supply Voltage

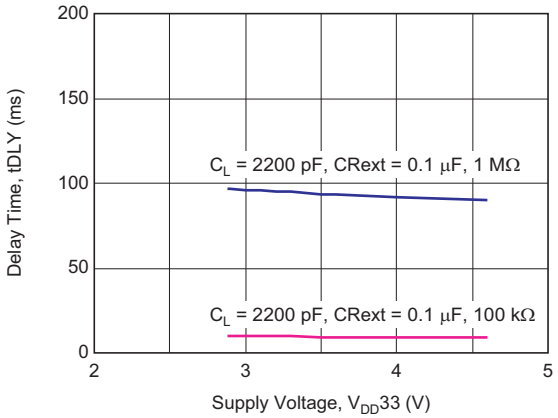


Figure 2-1.
Supply Current vs. Supply Voltage

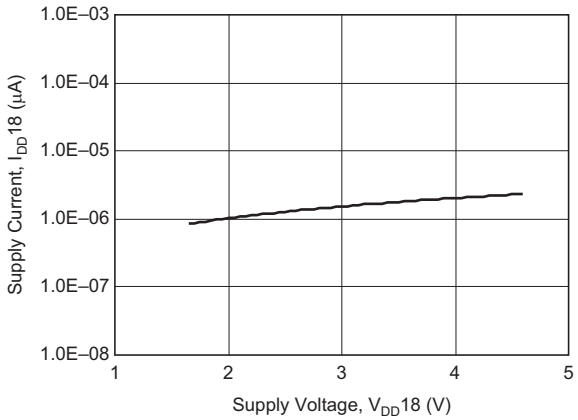


Figure 2-2.
SWG Output Current vs. Output Voltage

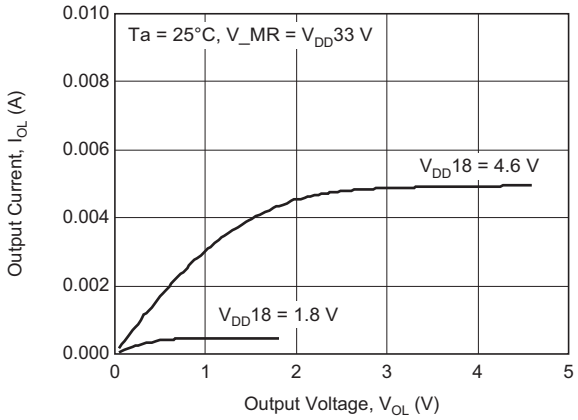


Figure 2-3.
SWG Output Current vs. Output Voltage

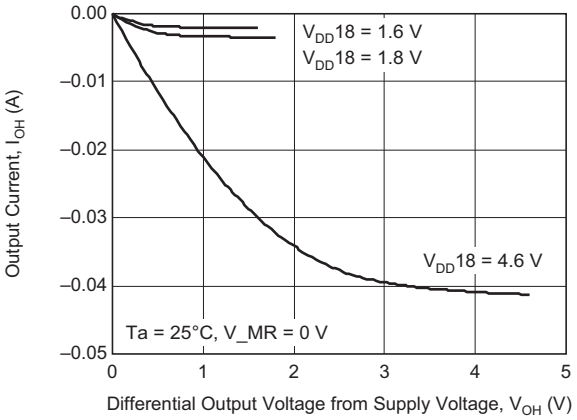


Figure 2-4.
Reset Output Delay Time vs. Supply Voltage

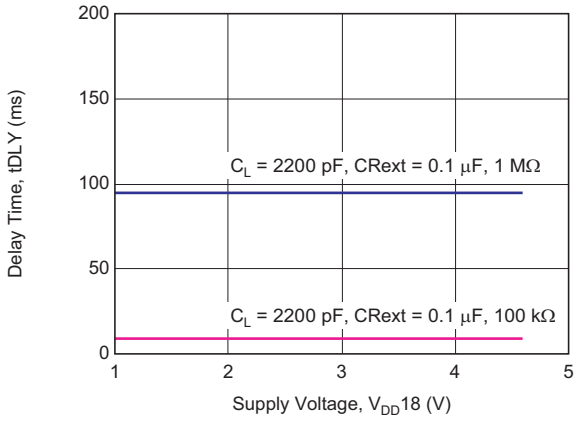


Figure 3-1.
Supply Current vs. Ambient Temperature

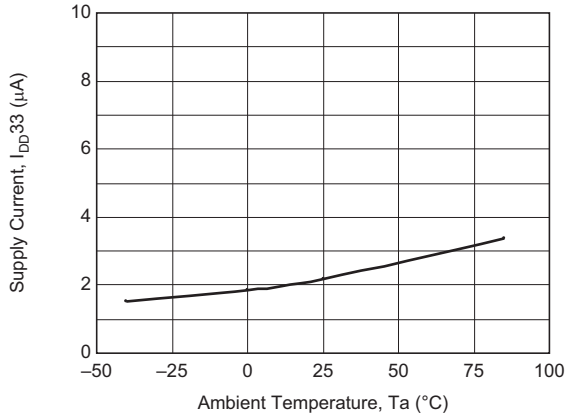


Figure 3-2.
Supply Current vs. Ambient Temperature

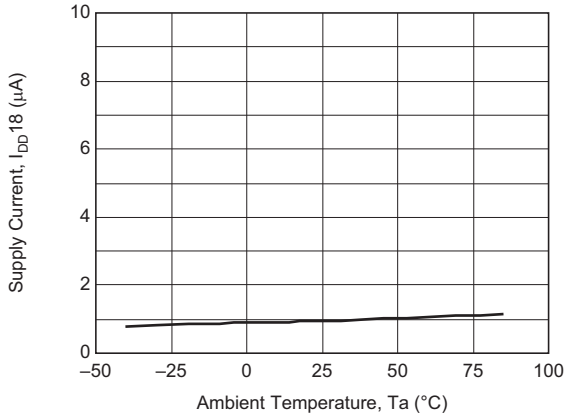


Figure 3-3.
Detection Voltage vs. Ambient Temperature

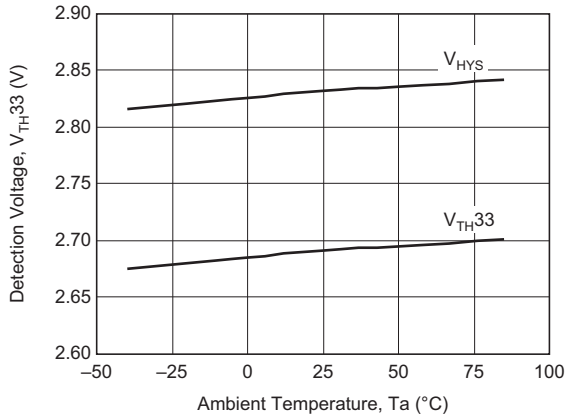


Figure 3-4.
Detection Voltage Hysteresis vs. Ambient Temperature

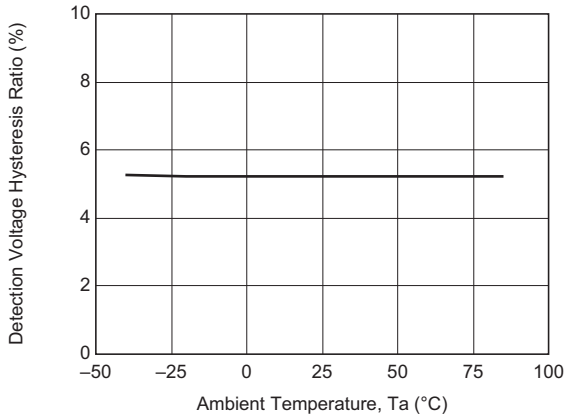


Figure 3-5.
Detection Voltage vs. Ambient Temperature

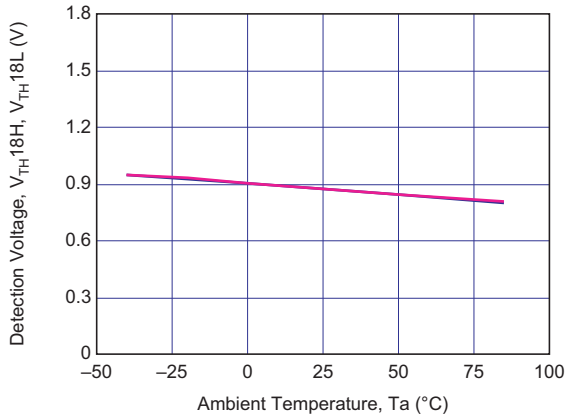


Figure 3-6.
Manual Reset Threshold Voltage vs. Ambient Temperature

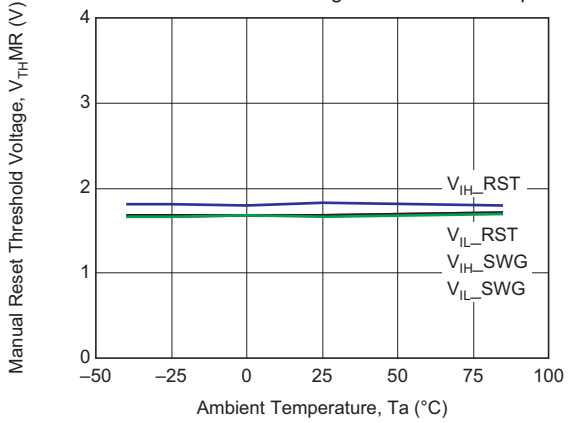


Figure 3-7.
Internal Pulled-up Resistor vs. Ambient Temperature

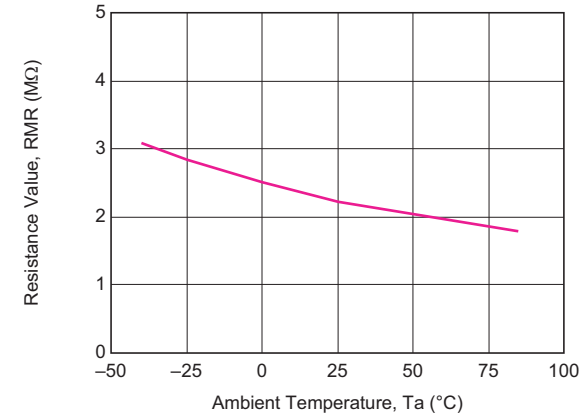


Figure 3-8.
$\overline{RESP}$ Output Leakage Current vs. Ambient Temperature

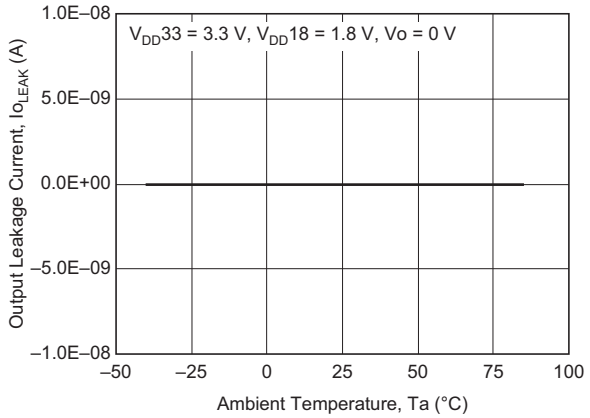


Figure 3-9.
$\overline{RESP}$ Output Current vs. Ambient Temperature

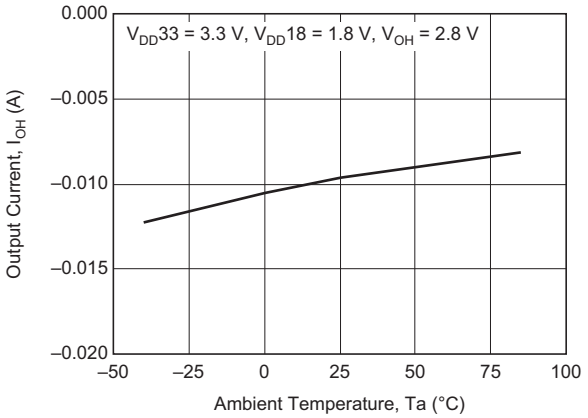


Figure 3-10.
$\overline{RESN}$ Output Current vs. Ambient Temperature

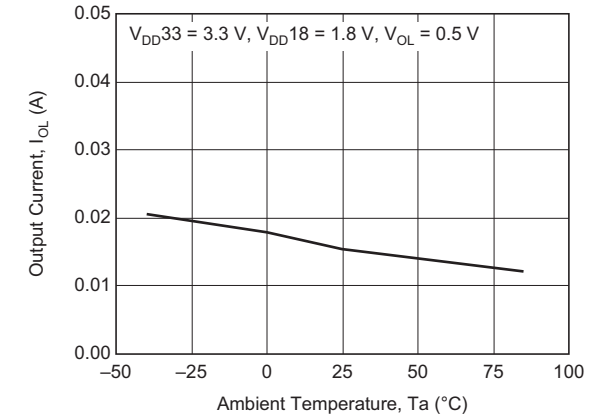


Figure 3-11.
$\overline{RESN}$ Output Leakage Current vs. Ambient Temperature

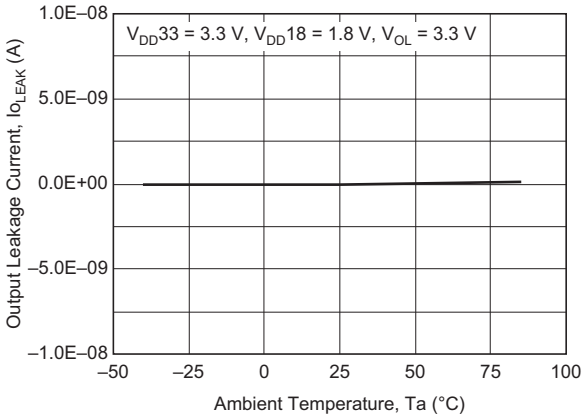


Figure 3-12.
SWG Output Current vs. Ambient Temperature

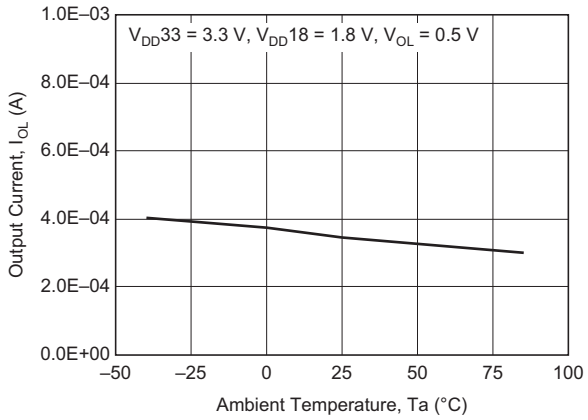


Figure 3-13.
SWG Output Current vs. Ambient Temperature

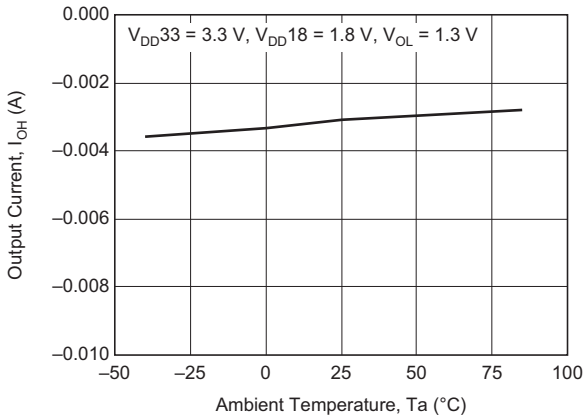


Figure 3-14.
$\overline{RESP}$ Output Rising Propagation Delay Time
vs. Ambient Temperature

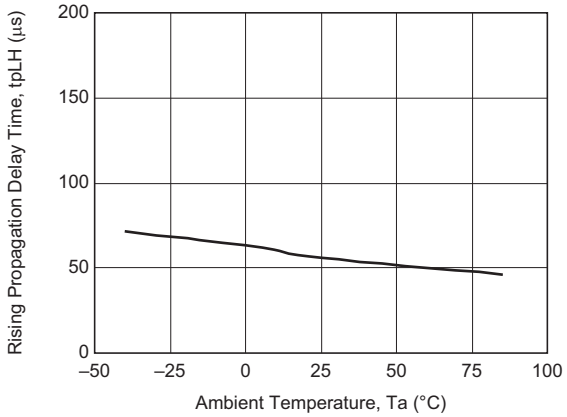


Figure 3-15.
$\overline{RESP}$ Output Falling Propagation Delay Time
vs. Ambient Temperature

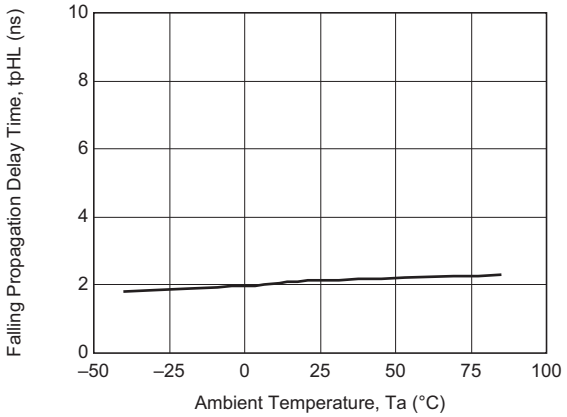


Figure 3-16.
$\overline{RESP}$ Output Rising Response Time
vs. Ambient Temperature

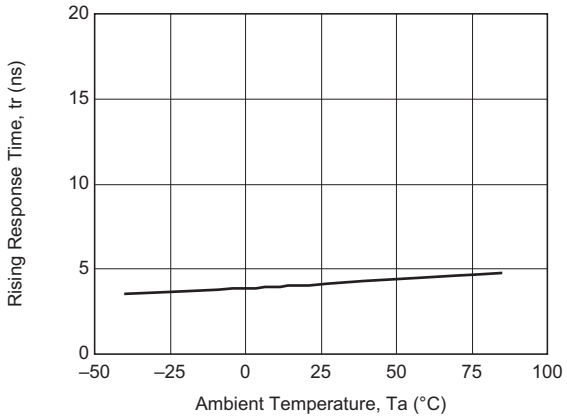


Figure 3-17.
$\overline{RESP}$ Output Falling Response Time
vs. Ambient Temperature

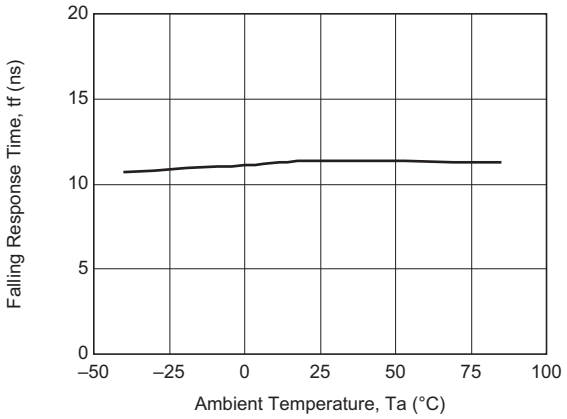


Figure 3-18.
$\overline{\text{RESN}}$ Output Rising Propagation Delay Time
vs. Ambient Temperature

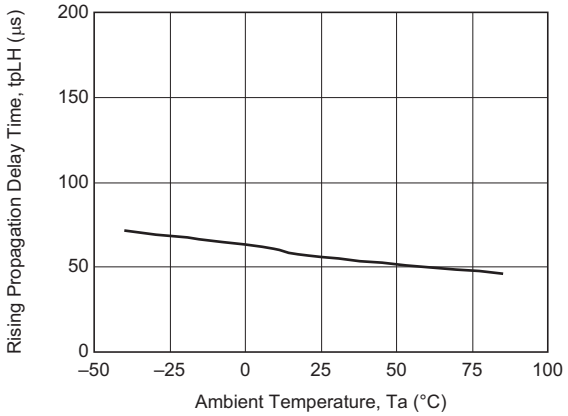


Figure 3-19.
$\overline{\text{RESN}}$ Output Falling Propagation Delay Time
vs. Ambient Temperature

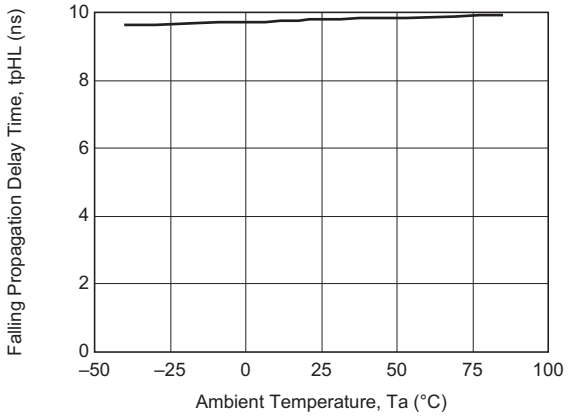


Figure 3-20.
$\overline{\text{RESN}}$ Output Rising Response Time
vs. Ambient Temperature

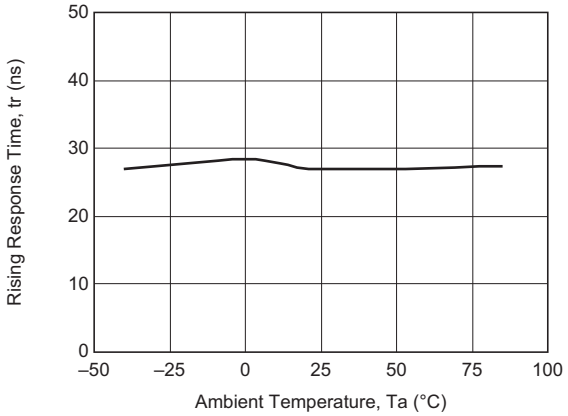


Figure 3-21.
$\overline{\text{RESN}}$ Output Falling Response Time
vs. Ambient Temperature

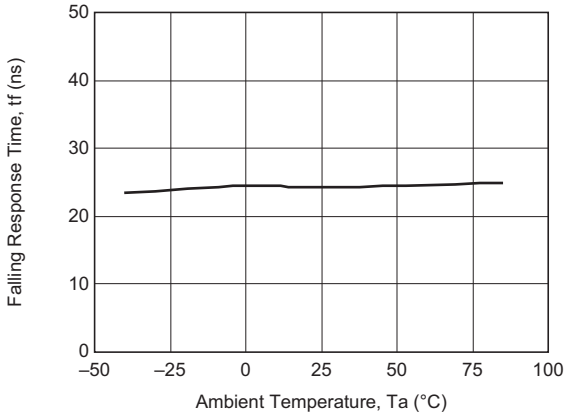


Figure 3-22.
SWG Output Falling Propagation Delay Time
vs. Ambient Temperature

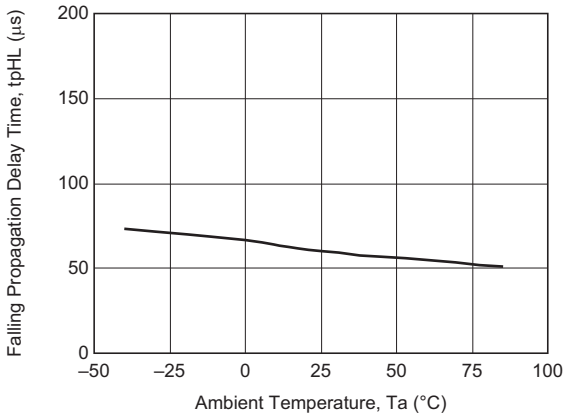


Figure 3-23.
SWG Output Rising Propagation Delay Time
vs. Ambient Temperature

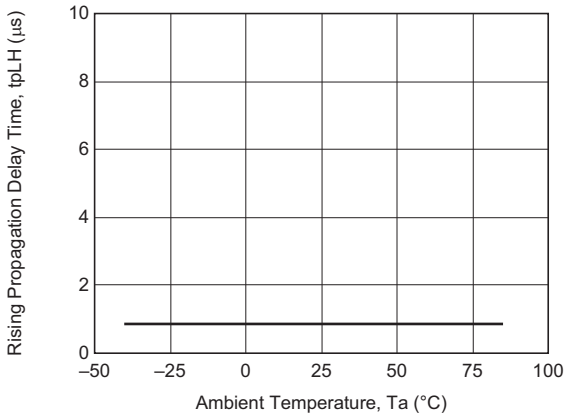


Figure 3-24.
SWG Output Falling Response Time
vs. Ambient Temperature

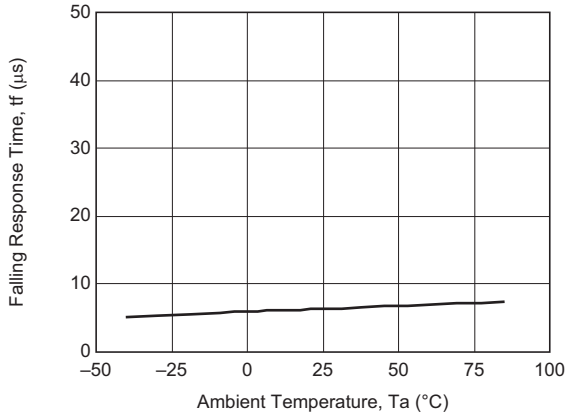


Figure 3-25.
SWG Output Rising Response Time
vs. Ambient Temperature

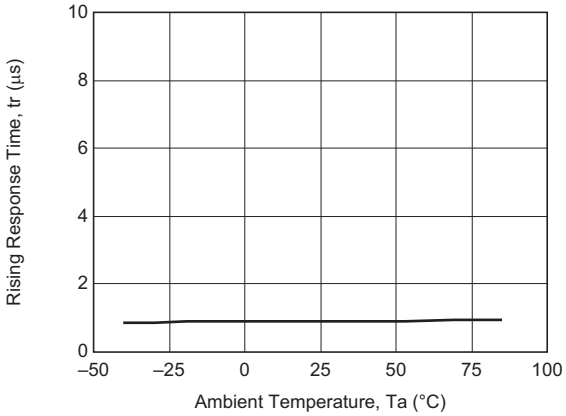


Figure 3-26.
Reset Output Delay Time vs. Ambient Temperature

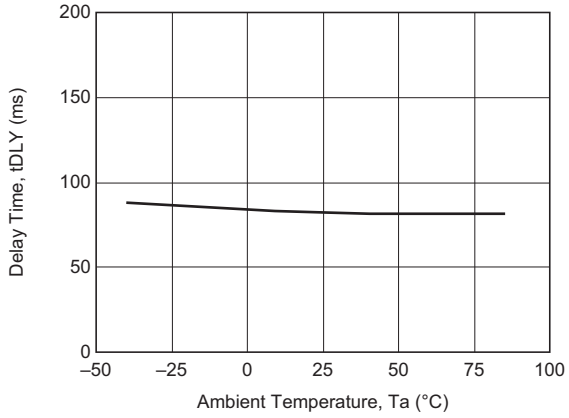


Figure 4-1.
Reset Output Delay Time vs. External Resistor

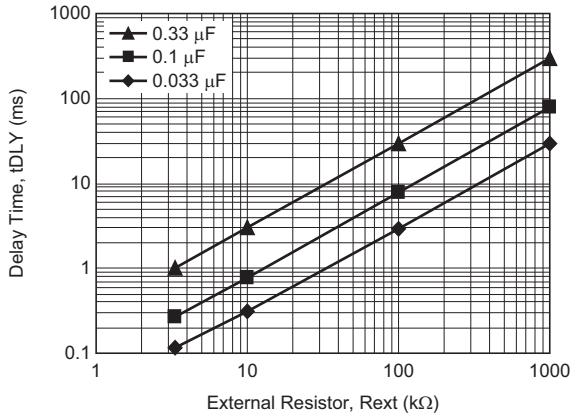
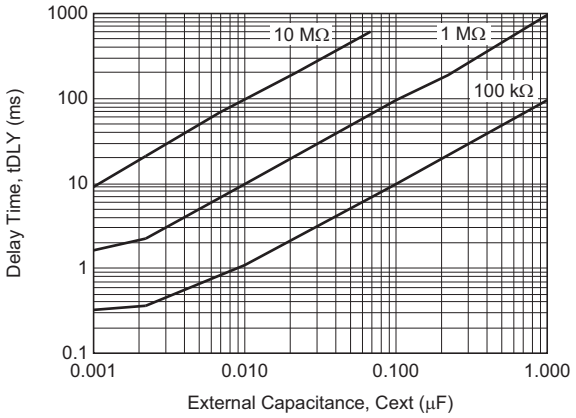


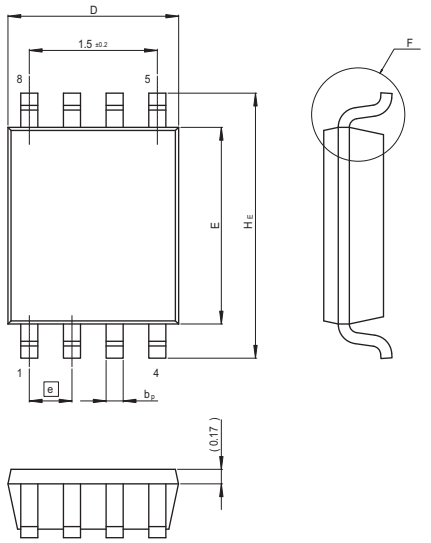
Figure 4-2.
Reset Output Delay Time vs. External Capacitance

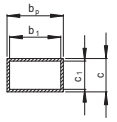


Package Dimensions

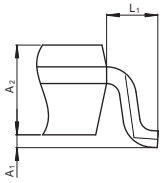
RNA50C27AUS

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VSSOP8-2.3x2-0.50	PVSP0008KA-A	TTP-8DB/TTP-8DBV	0.010g





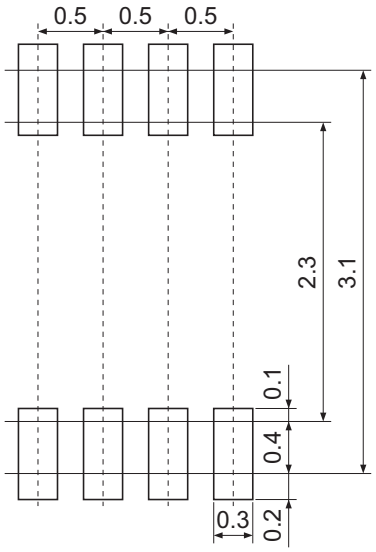
Terminal cross section



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	1.8	2.0	2.2
E	2.2	2.3	2.4
A_2	0.6	0.7	0.8
A_1	0	—	0.1
A	—	—	—
b_p	0.15	0.22	0.3
b_1	—	0.20	—
c	0.08	0.13	0.23
c_1	—	0.11	—
θ	—	—	—
H_E	2.8	3.1	3.4
e	—	(0.5)	—
x	—	—	—
y	—	—	—
Z	—	—	—
L	—	—	—
L_1	—	(0.4)	—

Unit: mm



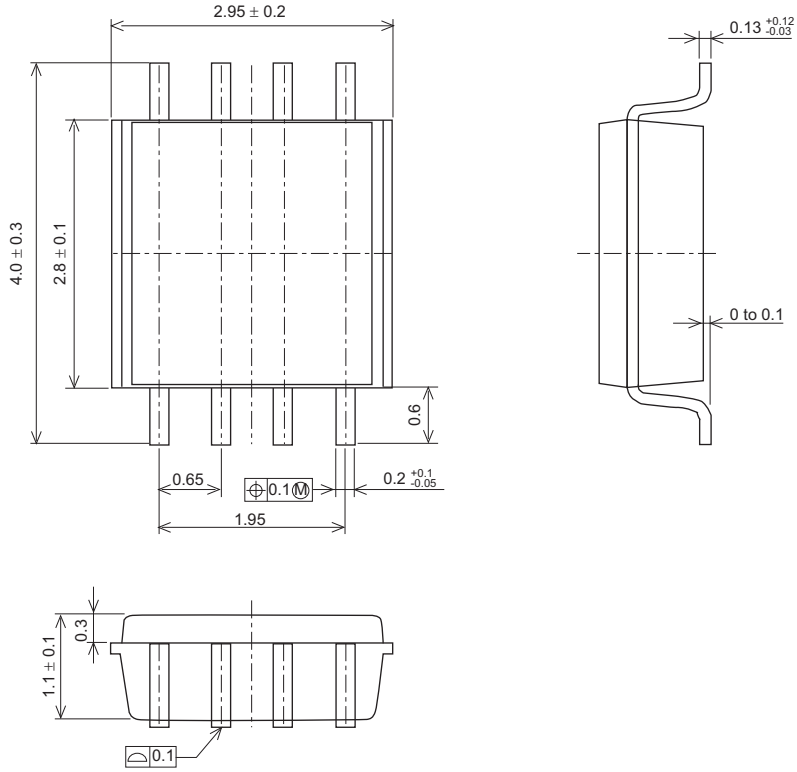
SSOP-8 Footprint Example

Note: These numbers on the diagram are reference values.
Please adjust size, space, and other area of footprint as needed.

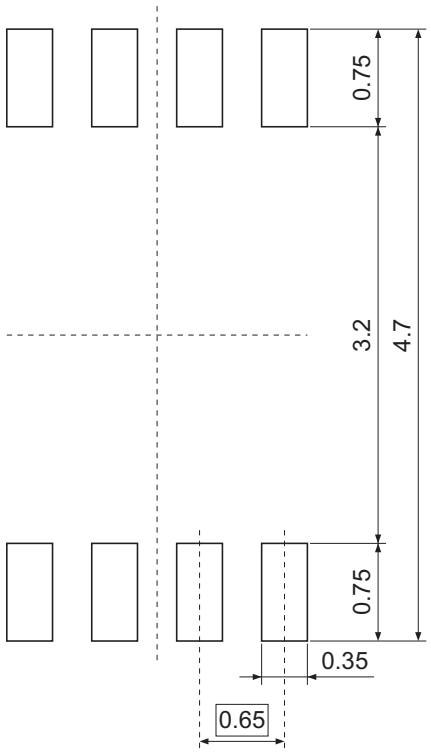
RNA50C27AMM

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
MMPAK-8	P-LSOP8-2.8 x 2.95 - 0.65	PLSP0008JC-A	—	0.02 g

Unit: mm



Unit: mm

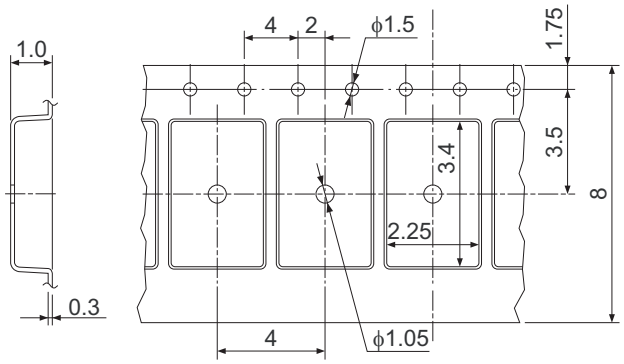


MMPAK-8 Footprint Example

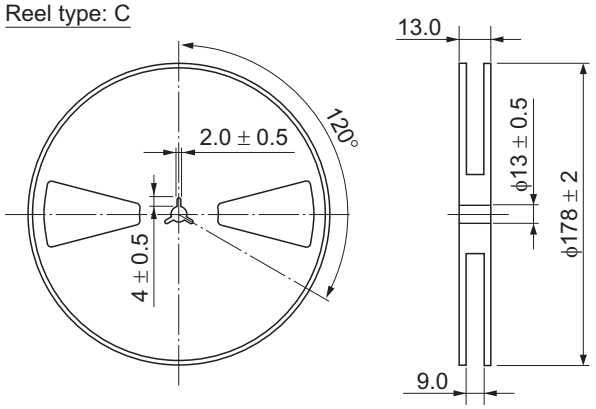
Taping and Reel Specifications

SSOP-8

Unit: mm



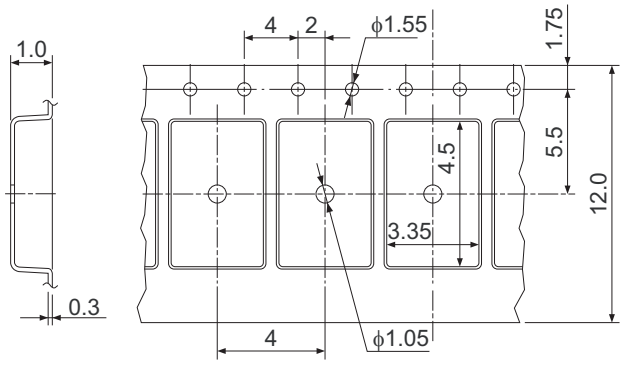
Reel type: C



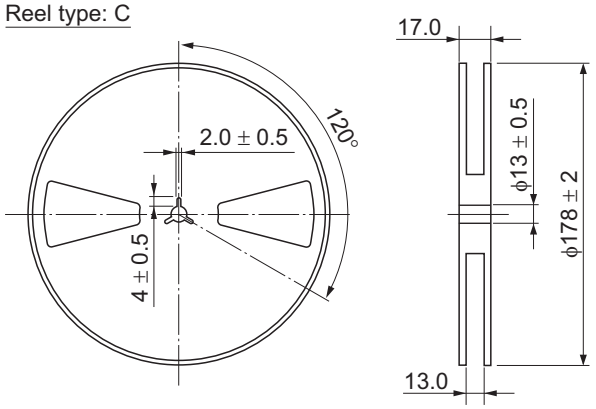
Maximum storage No.:
3000 pcs./Reel

MMPAK-8

Unit: mm

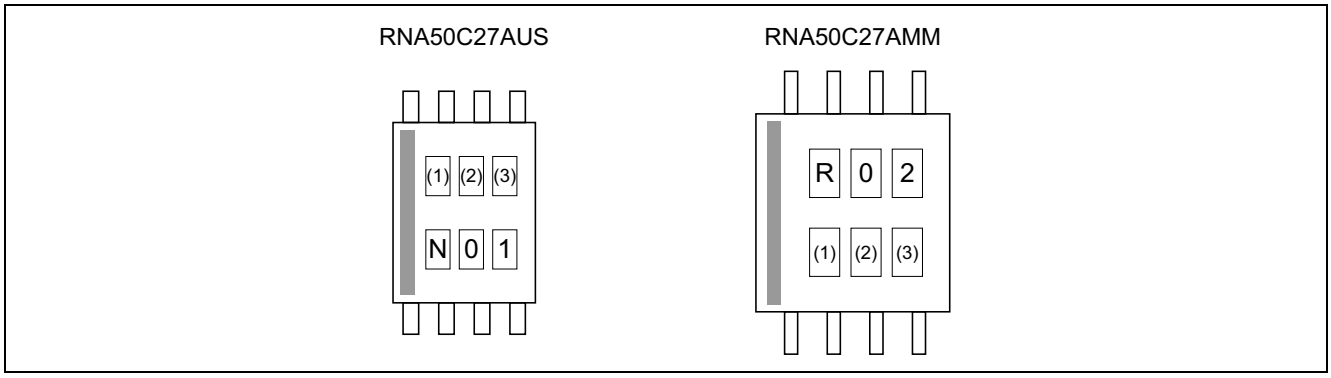


Reel type: C



Maximum storage No.:
3000 pcs./Reel

Mark Indication



(1)	Year code	The last digit of year
(2)	Month code	Starting in January "A","B","C","D","E","F","G","H","J","K","L","M"
(3)	Week code	View Week of month, 1 week → "1"

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