RMQS3A3636DGBA, RMQS3A3618DGBA

36-Mbit QDR™ II SRAM
4-word Burst

R10DS0236EJ0100
Rev.1.00
Jan. 13, 2015

Description

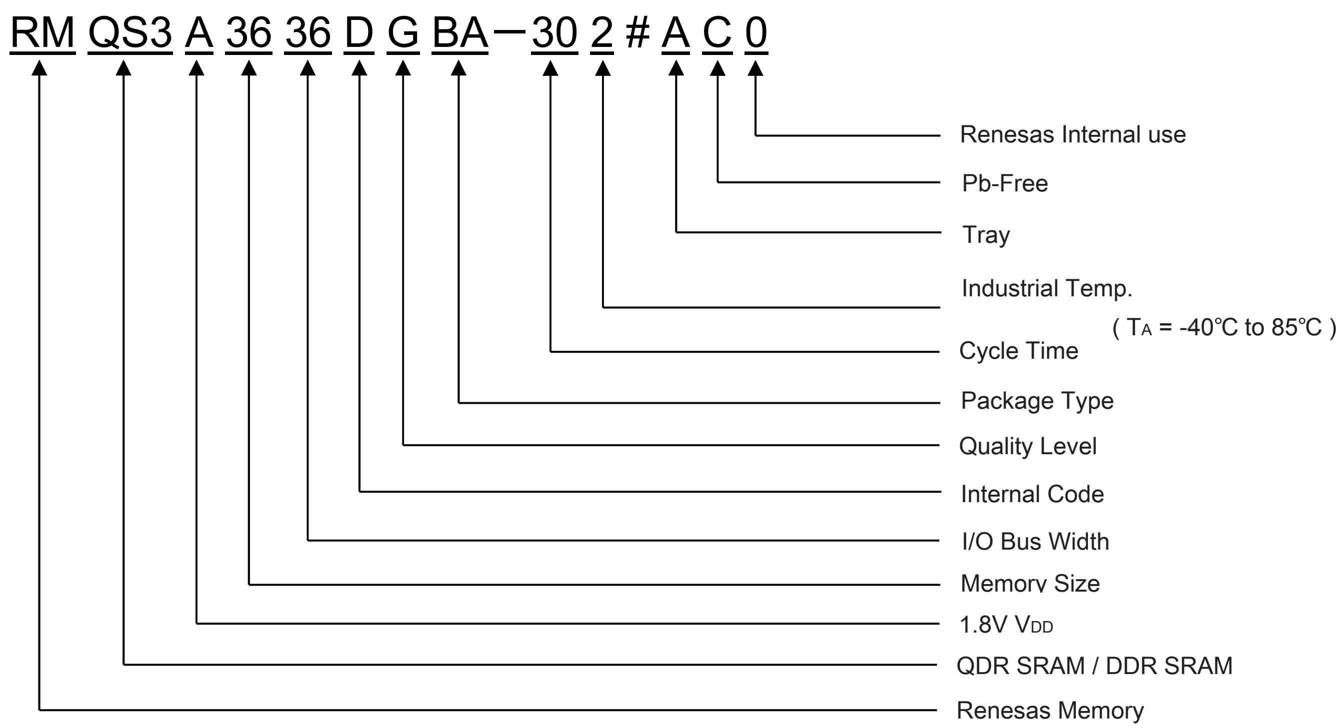
The RMQS3A3636DGBA is a 1,048,576-word by 36-bit and the RMQS3A3618DGBA is a 2,097,152-word by 18-bit synchronous quad data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell. It integrates unique synchronous peripheral circuitry and a burst counter. All input registers are controlled by an input clock pair (K and /K) and are latched on the positive edge of K and /K. These products are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration. These products are packaged in 165-pin plastic FBGA package.

Features

- Power Supply
  - 1.8 V for core (V_{DD}), 1.4 V to V_{DD} for I/O (V_{DDQ})
- Clock
  - Fast clock cycle time for high bandwidth
  - Two input clocks (K and /K) for precise DDR timing at clock rising edges only
  - Two input clocks for output data (C and /C) to minimize clock skew and flight time mismatches
  - Two output echo clocks (CQ and /CQ) simplify data capture in high-speed systems
  - Clock-stop capability with µs restart
- I/O
  - Separate independent read and write data ports with concurrent transactions
  - 100% bus utilization DDR read and write operation
  - HSTL I/O
  - User programmable output impedance
  - PLL circuitry for wide output data valid window and future frequency scaling
- Function
  - Four-tick burst for reduced address frequency
  - Internally self-timed write control
  - Simple control logic for easy depth expansion
  - JTAG 1149.1 compatible test access port
- Package
  - 165 FBGA package (13 x 15 x 1.4 mm)

Orderable Part Name Definition

Column No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Example	R	M	Q	*X*	*X*	A	*X*	*X*	*X*	*X*	D	G	B	A	-	3	0	2	#	A	C	0



Order Information

Orderable Part Name	Organization (word x bit)	Cycle time	Clock frequency	Operating Ambient Temperature	Core Supply Voltage (V)	Package
RMQS3A3636DGBA-302#AC0	1M x 36	3.00ns	333MHz	T_A = −40 to 85°C	1.8 ± 0.1	165-pin PLASTIC BGA (13 x 15) Pb-free
RMQS3A3636DGBA-332#AC0		3.30ns	300MHz			
RMQS3A3618DGBA-302#AC0	2M x 18	3.00ns	333MHz			
RMQS3A3618DGBA-332#AC0		3.30ns	300MHz			

Pin Arrangement

[RMQS3A3636DGBA]

1M x 36

(Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	NC	NC	/W	/BW2	/K	/BW1	/R	SA	NC	CQ
B	Q27	Q18	D18	SA	/BW3	K	/BW0	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	NC	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	/C	SA	SA	SA	TMS	TDI

Notes: 1. Address expansion order for future higher density SRAMs: 9A → 3A → 10A → 2A → 7A → 5B.

2. NC pins can be left floating or connected to 0V to V_{DDQ}

[RMQS3A3618DGBA]

2M x 18

(Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	NC	SA	/W	/BW1	/K	NC	/R	SA	NC	CQ
B	NC	Q9	D9	SA	NC	K	/BW0	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	NC	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	/C	SA	SA	SA	TMS	TDI

Notes: 1. Address expansion order for future higher density SRAMs: 9A → 3A → 10A → 2A → 7A → 5B.

2. NC pins can be left floating or connected to 0V to V_{DDQ}

Pin Descriptions

Name	I/O type	Descriptions	Note
SA	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K (read and write address). These inputs are ignored when device is deselected.	
/R	Input	Synchronous read: When low, this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K, and is ignored on the subsequent rising edge of K.	
/W	Input	Synchronous write: When low, this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K, and is ignored on the subsequent rising edge of K.	
$/BW_x$	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals are sampled on the same edge as the corresponding data and must meet setup and hold times around the rising edges of K and /K for each of the two rising edges comprising the WRITE cycle. See Byte Write Truth Table for signal to data relationship.	
K, /K	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of /K. /K is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain V_{REF} level.	
C, /C	Input	Output clock: This clock pair provides a user-controlled means of tuning device output data. Ideally, /C is 180 degrees out of phase with C. If C and /C are tied high, K and /K are used as the output reference clocks instead of C and /C clocks. If tied high, C and /C must remain high and not to be toggled during device operation. These balls cannot remain VREF level.	
/DOFF	Input	PLL disable: When low, this input causes the PLL to be bypassed for stable, low frequency operation.	
TMS TDI	Input	IEEE1149.1 test inputs: 1.8 V I/O levels. These balls may be left unconnected if the JTAG function is not used in the circuit.	
TCK	Input	IEEE1149.1 clock input: 1.8 V I/O levels. This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.	
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. Q and CQ output impedance are set to $0.2 \times RQ$, where RQ is a resistor from this ball to ground. This ball can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This ball cannot be connected directly to V_{SS} or left unconnected.	

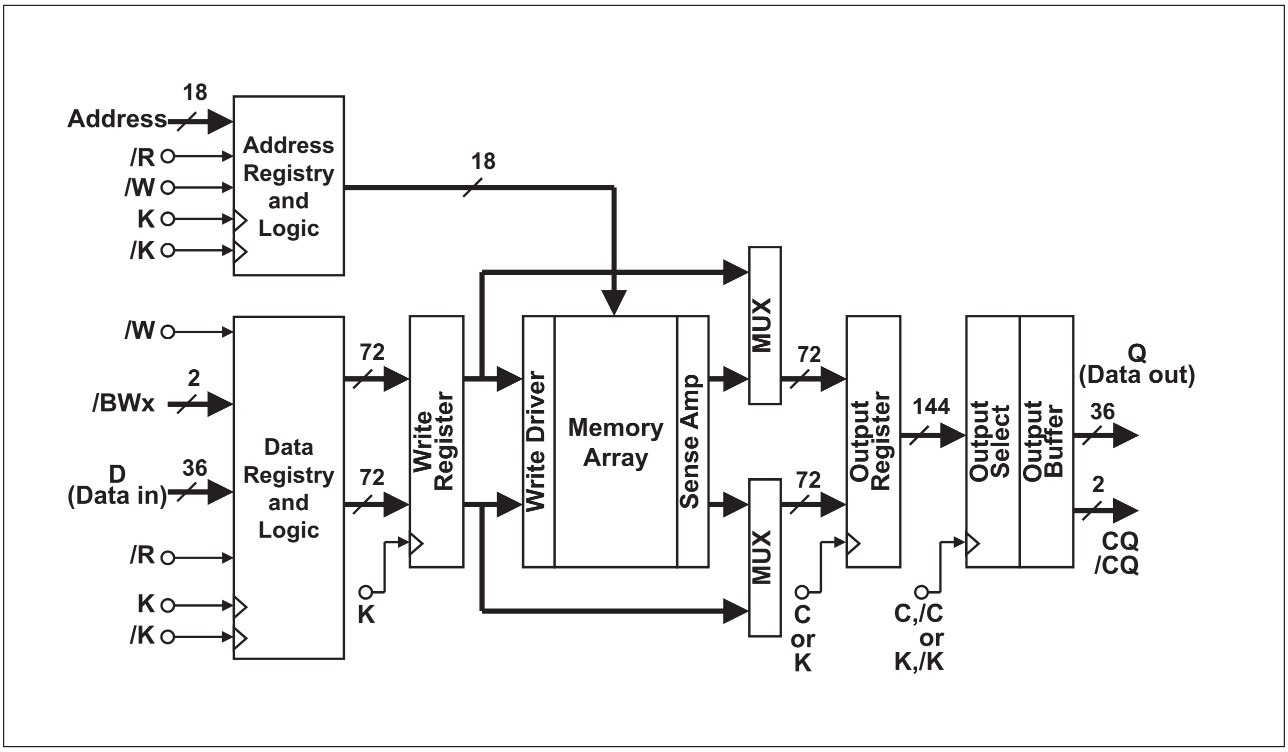
Name	I/O type	Descriptions	Note
D_0 to D_n	Input	Synchronous data inputs: Input data must meet setup and hold times around the rising edges of K and /K during WRITE operations. See Pin Arrangement figures for ball site location of individual signals. The ×18 device uses D0 to D17. D18 to D35 should be treated as NC pin. The ×36 device uses D0 to D35.	
CQ, /CQ	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tri-states.	
TDO	Output	IEEE 1149.1 test output: 1.8 V I/O level.	
Q_0 to Q_n	Output	Synchronous data outputs: Output data is synchronized to the C clock. If C and /C are tied high, Output data is synchronized to the K clock instead of C clock. This bus operates in response to /R commands. See Pin Arrangement figures for ball site location of individual signals. The ×18 device uses Q0 to Q17. Q18 to Q35 should be treated as NC pin. The ×36 device uses Q0 to Q35.	
V_{DD}	Supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.	1
V_{DDQ}	Supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. See DC Characteristics and Operating Conditions for range.	1
V_{SS}	Supply	Power supply: Ground.	1
V_{REF}	-	HSTL input reference voltage: Nominally $V_{DDQ}/2$, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.	
NC	-	No connect: These pins can be left floating or connected to 0V to V_{DDQ}.	

Notes:

1. All power supply and ground balls must be connected for proper operation of the device.

Block Diagram

[RMQS3A3636DGBA]



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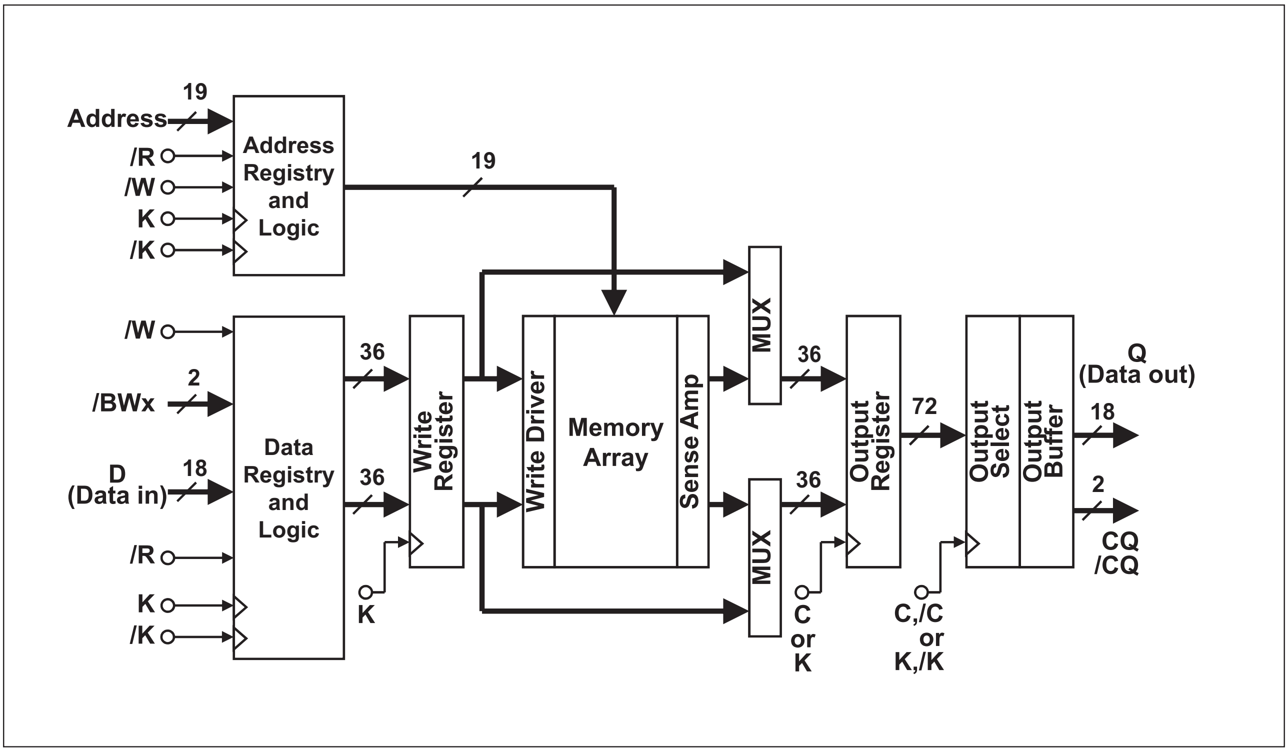
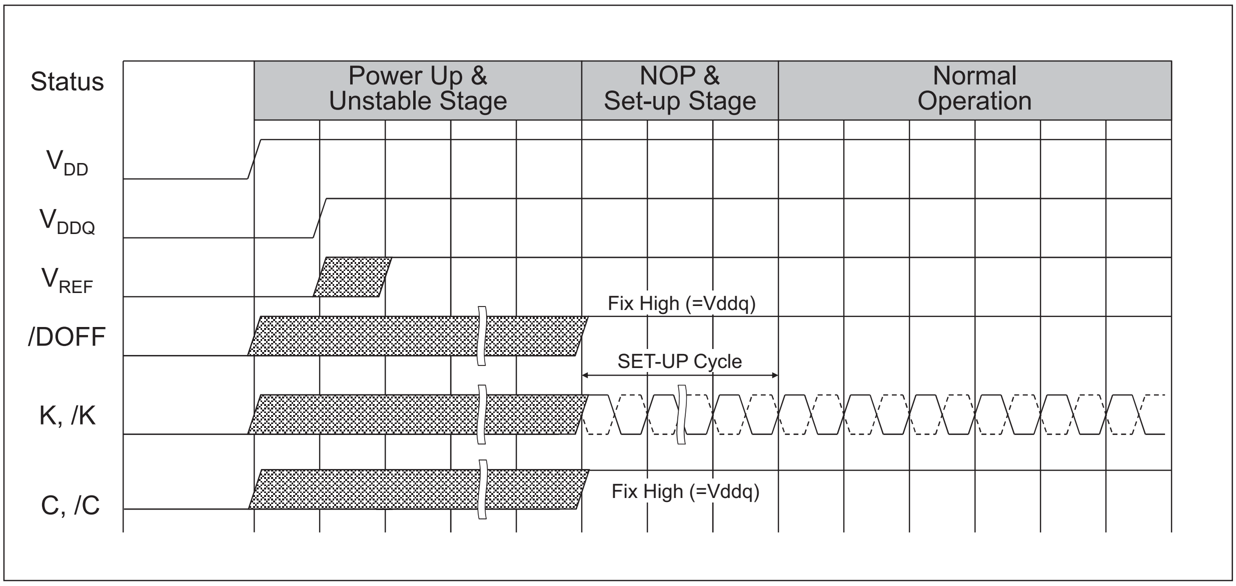


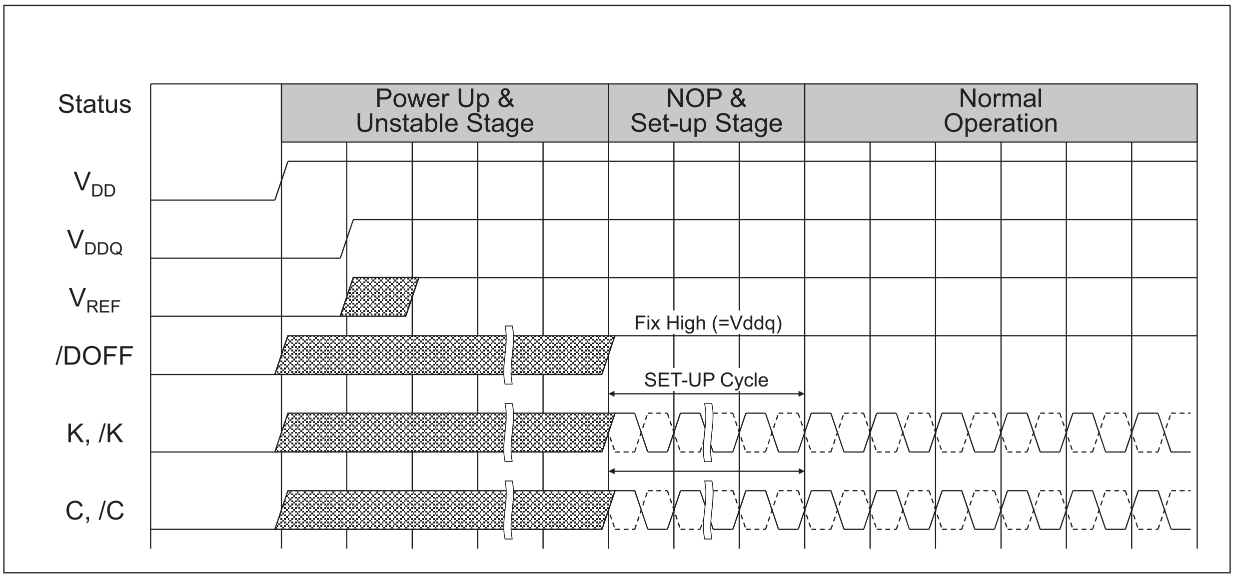
Power-up and Initialization Sequence

- V_{DD} must be stable before K, /K clocks are applied.
- Recommended voltage application sequence : $V_{SS} \rightarrow V_{DD} \rightarrow V_{DDQ}$ & $V_{REF} \rightarrow V_{IN}$. (0 V to V_{DD}, V_{DDQ} < 200 ms)
- Apply V_{REF} after V_{DDQ} or at the same time as V_{DDQ}.
- Then execute either one of the following three sequences.

1. Single Clock Mode
    - Drive /DOFF high (/DOFF can be tied high from the start).
    - Then provide stable clocks (K, /K) for at least 20 us.



2. Double Clock Mode (C and /C control outputs)
    - Drive /DOFF high (/DOFF can be tied high from the start)
    - Then provide stable clocks (K, /K , C, /C) for at least 20 us.



3. PLL Off Mode (/DOFF tied low)
    - In the "NOP and setup stage", provide stable clocks (K, /K) for at least 20 us.

PLL Constraints

1. These chips use the PLL. The clock input should have low phase jitter which is specified as tKC var.
2. The lower end of the frequency at which the PLL can operate is 120 MHz.
   (Please refer to AC Characteristics table for detail.)
3. When the operating frequency is changed or /DOFF level is changed, setup cycles are required again.

Programmable Output Impedance

1. Output buffer impedance can be programmed by terminating the ZQ ball to VSS through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 175 Ω and 350 Ω. The total external capacitance of ZQ ball must be less than 7.5 pF.

K Truth Table

Operation	K	/R	/W	D or Q				
Write Cycle: Load address, input write data on two consecutive K and /K rising edges	↑	H[*7]	L[*8]	Data in				
				Input data	D(A+0)	D(A+1)	D(A+2)	D(A+3)
				Input clock	K(t+1) ↑	/K(t+1) ↑	K(t+2) ↑	/K(t+2) ↑
Read Cycle: Load address, output read data on two consecutive C and /C rising edges	↑	L[*8]	x	Data out				
				Output data	Q(A+0)	Q(A+1)	Q(A+2)	Q(A+3)
				Input clock	/C(t+1) ↑	C(t+2) ↑	/C(t+2) ↑	C(t+3) ↑
NOP (No operation)	↑	H	H	D = x or Q = High-Z				
Standby (Clock stopped)	Stopped	x	x	Previous state				

Notes:

1. H: high level, L: low level, ×: don’t care, ↑: rising edge.
2. Data inputs are registered at K and /K rising edges. Data outputs are delivered at C clock edges, except if C and /C are high, then data outputs are delivered at K clock edges.
3. /R and /W must meet setup/hold times around the rising edges (low to high) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in high-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. When clocks are stopped, the following cases are recommended; the case of K = low, /K = high, C = low and /C = high, or the case of K = high, /K = low, C = high and /C = low. This condition is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. If this signal was low to initiate the previous cycle, this signal becomes a “don’t care” for this operation; however, it is strongly recommended that this signal be brought high, as shown in the truth table.
8. This signal was high on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.

Byte Write Truth Table (x 36)

Operation	K	/K	/BW0	/BW1	/BW2	/BW3
Write D0 to D35	↑	-	L	L	L	L
	-	↑	L	L	L	L
Write D0 to D8	↑	-	L	H	H	H
	-	↑	L	H	H	H
Write D9 to D17	↑	-	H	L	H	H
	-	↑	H	L	H	H
Write D18 to D26	↑	-	H	H	L	H
	-	↑	H	H	L	H
Write D27 to D35	↑	-	H	H	H	L
	-	↑	H	H	H	L
Write nothing	↑	-	H	H	H	H
	-	↑	H	H	H	H

Notes:

1. H: high level, L: low level, ↑: rising edge.
2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

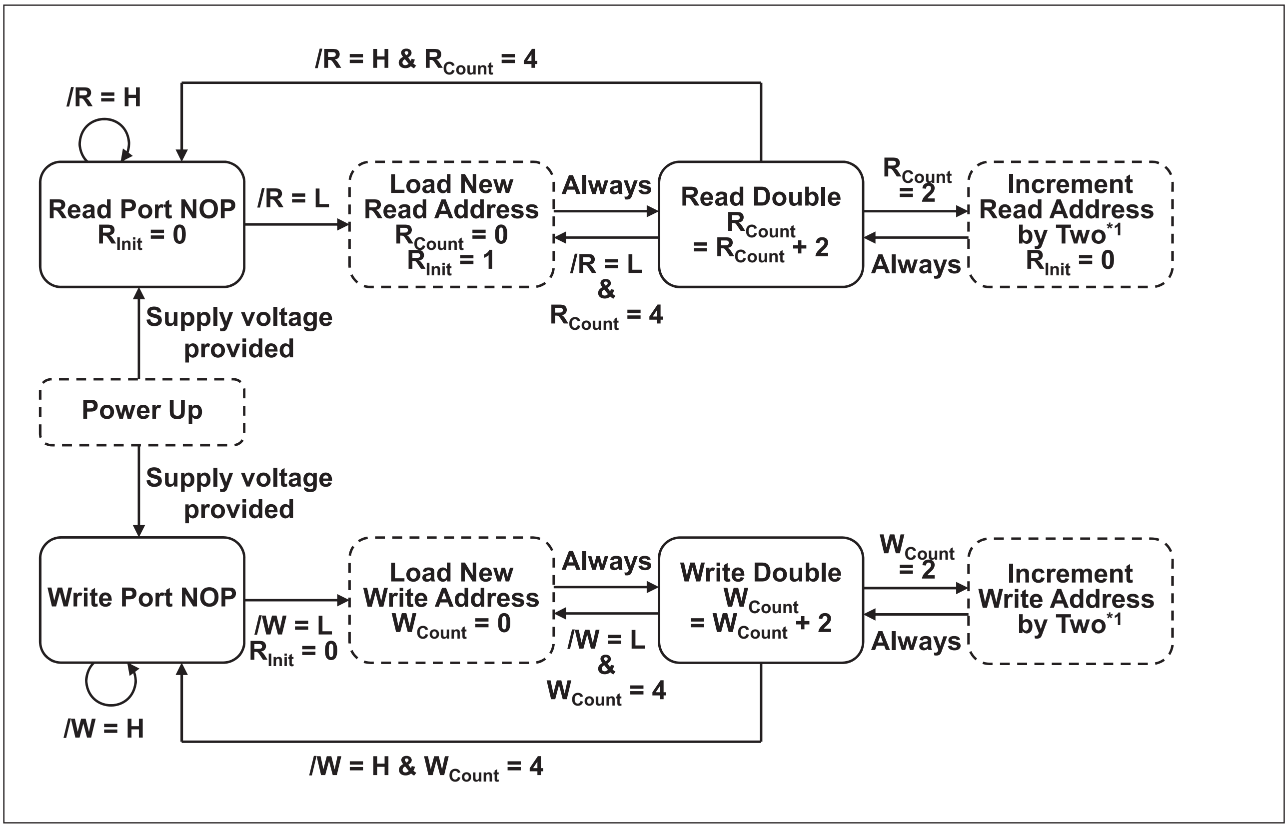
Byte Write Truth Table (x 18)

Operation	K	/K	/BW0	/BW1
Write D0 to D17	↑	-	L	L
	-	↑	L	L
Write D0 to D8	↑	-	L	H
	-	↑	L	H
Write D9 to D17	↑	-	H	L
	-	↑	H	L
Write nothing	↑	-	H	H
	-	↑	H	H

Notes:

1. H: high level, L: low level, ↑: rising edge.
2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



Notes:

1. The address is concatenated with two additional internal LSBs to facilitate burst operation. The address order is always fixed as: xxx…xxx+0, xxx…xxx+1, xxx…xxx+2, xxx…xxx+3.

   Bus cycle is terminated at the end of this sequence (burst count = 4).
2. Read and write state machines can be active simultaneously. Read and write cannot be simultaneously initiated. Read takes precedence.
3. State machine control timing sequence is controlled by K.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Input voltage on any ball	V_{IN}	–0.5 to V_{DD} + 0.5 (2.5 V max.)	V	1,4
Input/output voltage	$V_{I/O}$	–0.5 to V_{DDQ} + 0.5 (2.5 V max.)	V	1,4
Core supply voltage	V_{DD}	–0.5 to 2.5	V	1,4
Output supply voltage	V_{DDQ}	–0.5 to V_{DD}	V	1,4
Junction temperature	Tj	+125 (max)	°C	5
Storage temperature	T_{STG}	–55 to +125	°C	

Notes:

1. All voltage is referenced to V_{SS}.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 2.5 V, whatever the instantaneous value of V_{DDQ}.
5. Some method of cooling or airflow should be considered in the system.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage -- core	V_{DD}	1.7	1.8	1.9	V	1
Power supply voltage -- I/O	V_{DDQ}	1.4	1.5	V_{DD}	V	1,2
Input reference voltage -- I/O	V_{REF}	0.68	0.75	0.95	V	3
Input high voltage	$V_{IH (DC)}$	V_{REF} + 0.1	-	V_{DDQ} + 0.3	V	1,4,5
Input low voltage	$V_{IL (DC)}$	-0.3	-	V_{REF} - 0.1	V	1,4,5

Notes:

1. At power-up, V_{DD} and V_{DDQ} are assumed to be a linear ramp from 0V to V_{DD}(min.) or V_{DDQ}(min.) within 200ms. During this time, $V_{DDQ} < V_{DD}$ and $V_{IH} < V_{DDQ}$. During normal operation, V_{DDQ} must not exceed V_{DD}.
2. Please pay attention to Tj not to exceed the temperature shown in the absolute maximum ratings table due to current from V_{DDQ}.
3. Peak to peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.
4. These are DC test criteria. The AC V_{IH} / V_{IL} levels are defined separately to measure timing parameters.
5. Overshoot: $V_{IH (AC)} \le V_{DDQ} + 0.5$ V for $t \le t_{KHKH}/2$

   Undershoot: $V_{IL (AC)} \ge -0.5$ V for $t \le t_{KHKH}/2$

   During normal operation, $V_{IH(DC)}$ must not exceed V_{DDQ} and $V_{IL(DC)}$ must not be lower than V_{SS}.

DC Characteristics

(T_A = -40 to +85°C, V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.5V, V_{REF} = 0.75V)

Parameter	Symbol	Test condition	MIN.	MAX.			Unit	Notes
				333MHz	300MHz	250MHz		
Operating Supply Current (Write / Read)	I_{DD}	(x36)		590	550	500	mA	1,2,3
		(x18)		480	460	410		
Standby Supply Current (NOP)	I_{SB1}	(x36)		380	360	330	mA	2,4,5
		(x18)		360	340	310		
Input leakage current	I_{LI}		-2	2			µA	9
Output leakage current	I_{LO}		-5	5			µA	10
Output high voltage	V_{OH} (Low)	$\lvert I_{OH}\rvert \le 0.1$ mA	$V_{DDQ} - 0.2$	V_{DDQ}			V	8
	V_{OH}	Note 6	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$			V	8
Output low voltage	V_{OL} (Low)	$I_{OL} \le 0.1$ mA	V_{SS}	0.2			V	8
	V_{OL}	Note 7	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$			V	8

Notes:

1. All inputs (except ZQ, V_{REF}) are held at either V_{IH} or V_{IL}.
2. I_{OUT} = 0 mA. V_{DD} = V_{DD} max, t_{KHKH} = t_{KHKH} min.
3. Operating supply currents (I_{DD}) are measured at 100% bus utilization. I_{DD} of QDR family is current of device with 100% write and 100% read cycle.
4. All address / data inputs are static at either $V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$.
5. Reference value. (Condition = NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.)
6. Outputs are impedance-controlled. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
7. Outputs are impedance-controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
8. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
9. $0 \le V_{IN} \le V_{DDQ}$ for all input balls (except V_{REF}, ZQ, TCK, TMS, TDI ball).
10. $0 \le V_{OUT} \le V_{DDQ}$ (except TDO ball), output disabled.

Thermal Resistance

Parameter	Symbol	Airflow	Typ	Unit	Test condition	Notes
Junction to Ambient	θ_{JA}	1 m/s	13	°C/W	EIA/JEDEC JESD51	1
Junction to Case	θ_{JC}	-	6.3			

Notes:

1. These parameters are calculated under the condition. These are reference values.
2. $Tj = Ta + \theta_{JA} \times Pd$
   $Tj = Tc + \theta_{JC} \times Pd$
   where
   Tj : junction temperature when the device has achieved a steady-state after application of Pd (°C)
   Ta :ambient temperature (°C)
   Tc :temperature of external surface of the package or case (°C)
   θ_{JA} :thermal resistance from junction-to-ambient (°C/W)
   θ_{JC} :thermal resistance from junction-to-case (package) (°C/W)
   Pd :power dissipation that produced change in junction temperature (W) (cf.JESD51-2A)

Capacitance

($T_A = +25°C$, Frequency = 1.0MHz, $V_{DD} = 1.8V$, $V_{DDQ} = 1.5V$)

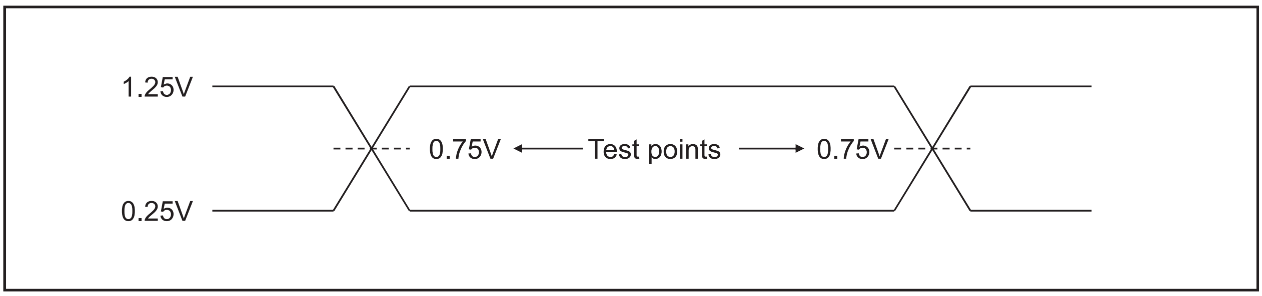
Parameter	Symbol	Min	Typ	Max	Unit	Test condition	Note
Input capacitance (SA, /R, /W, /BW)	C_{IN}	-	4	5	pF	V_{IN} = 0 V	1,2
Clock input capacitance (K, /K, C, /C)	C_{CLK}	-	4	5	pF	V_{CLK} = 0 V	1,2
Output capacitance (DQ, CQ, /CQ)	$C_{I/O}$	-	5	6	pF	$V_{I/O}$ = 0 V	1,2

Notes:

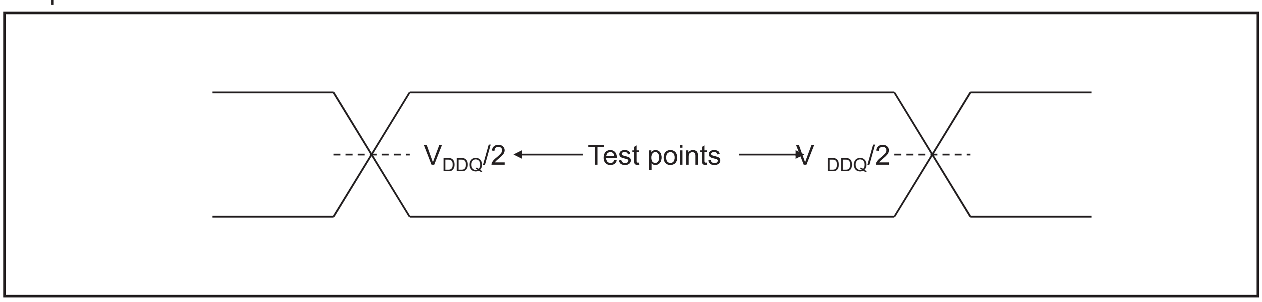
1. These parameters are sampled and not 100% tested.
2. Except JTAG (TCK, TMS, TDI, TDO) pins.

AC Test Conditions

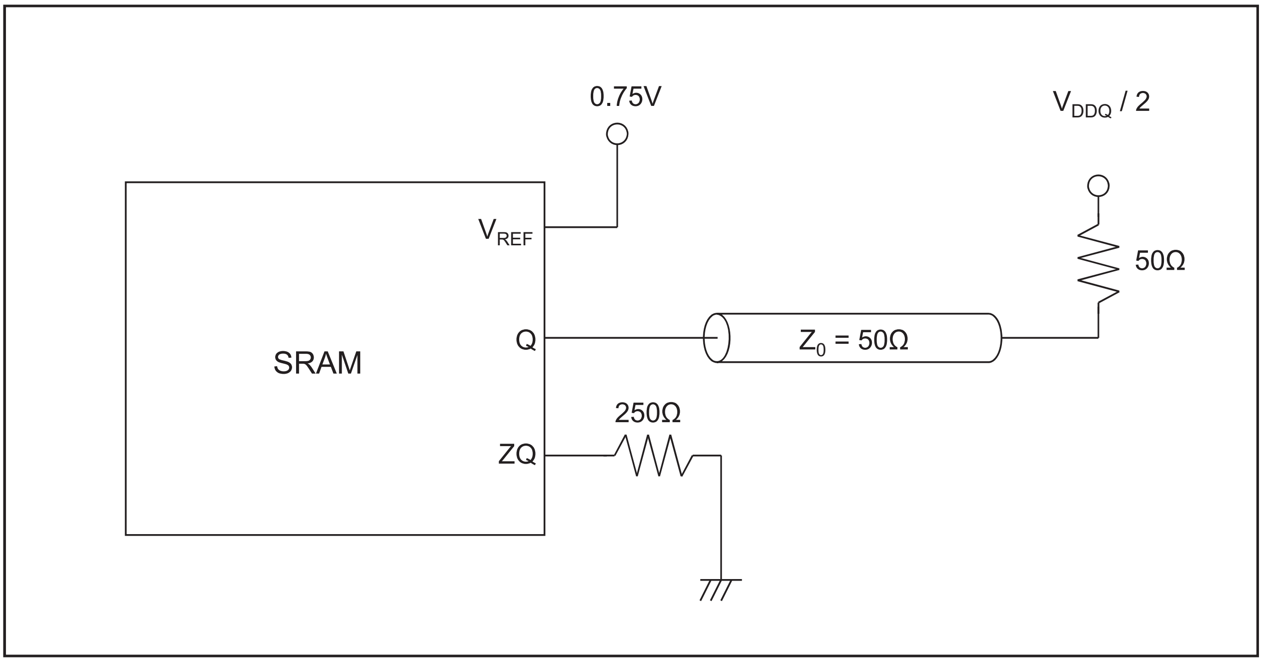
Input waveform (Rise/fall time ≤ 0.3 ns)



Output waveform



Output load conditions



AC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	$V_{IH\,(AC)}$	V_{REF} + 0.2	-	-	V	1,2,3,4
Input low voltage	$V_{IL\,(AC)}$	-	-	V_{REF} – 0.2	V	1,2,3,4

Notes:

1. All voltages referenced to V_{SS} (GND). During normal operation, V_{DDQ} must not exceed V_{DD}.
2. These conditions are for AC functions only, not for AC parameter test.
3. Overshoot: $V_{IH\,(AC)} \leq V_{DDQ} + 0.5$ V for $t \leq t_{KHKH}/2$
   Undershoot: $V_{IL\,(AC)} \geq -0.5$ V for $t \leq t_{KHKH}/2$
   Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).
4. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL\,(AC)}$ or $V_{IH\,(AC)}$.
   b. Reach at least the target AC level.
   c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL\,(DC)}$ or $V_{IH\,(DC)}$.

AC Characteristics

(T_A = -40 to +85°C, V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.5V, V_{REF} = 0.75V)

Parameter	Symbol	333MHz		300MHz		250MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock									
Average clock cycle time (K, /K, C, /C)	t_{KHKH}	3.0	8.4	3.3	8.4	4.0	8.4	ns	
Clock high time (K, /K, C, /C)	t_{KHKL}	1.20	-	1.32	-	1.60	-	ns	
Clock low time (K, /K, C, /C)	t_{KLKH}	1.20	-	1.32	-	1.60	-	ns	
Clock to /clock (K to /K, C to /C)	$t_{KH/KH}$	1.35	-	1.49	-	1.80	-	ns	
/Clock to clock (/K to K, C to /C)	$t_{/KHKH}$	1.35	-	1.49	-	1.80	-	ns	
Clock to data clock (K to C, /K, /C)	t_{KHCH}	0	1.30	0	1.45	0	1.80	ns	
PLL Timing									
Clock phase jitter (K, /K, C, /C)	t_{KC} var	-	0.20	-	0.20	-	0.20	ns	3
Lock time (K,C)	t_{KC} lock	20	-	20	-	20	-	us	2
K static to PLL reset	t_{KC} reset	30	-	30	-	30	-	ns	5
Output Times									
C, /C high to output valid	t_{CHQV}	-	0.45	-	0.45	-	0.45	ns	
C, /C high to output hold	t_{CHQX}	-0.45	-	-0.45	-	-0.45	-	ns	
C, /C high to echo clock valid	t_{CHCQV}	-	0.45	-	0.45	-	0.45	ns	
C, /C high to echo clock hold	t_{CHCQX}	-0.45	-	-0.45	-	-0.45	-	ns	
CQ, /CQ high to output valid	t_{CQHQV}	-	0.25	-	0.27	-	0.30	ns	5
CQ, /CQ high to output hold	t_{CQHQX}	-0.25		-0.27	-	-0.30	-	ns	5
Clock to /Clock (CQ to /CQ)	$t_{CQH/CQH}$	1.25	-	1.40	-	1.75	-	ns	5
/Clock to Clock (/CQ to CQ)	$t_{/CQHCQH}$	1.25	-	1.40	-	1.75	-	ns	5
C, /C high to output high-Z	t_{CHQZ}	-	0.45	-	0.45	-	0.45	ns	4
C, /C high to output low-Z	t_{CHQX1}	-0.45	-	-0.45	-	-0.45	-	ns	4
Setup Times									
Address valid to K rising edge	t_{AVKH}	0.40	-	0.40	-	0.50	-	ns	1
Control inputs valid to K rising edge	t_{IVKH}	0.40	-	0.40	-	0.50	-	ns	1
Data-in valid to K, /K rising edge	t_{DVKH}	0.30	-	0.30	-	0.35	-	ns	1
Hold Times									
K rising edge to address hold	t_{KHAX}	0.40	-	0.40	-	0.50	-	ns	1
K rising edge to control inputs hold	t_{KHIX}	0.40	-	0.40	-	0.50	-	ns	1
K, /K rising edge to data-in hold	t_{KHDX}	0.30	-	0.30	-	0.35	-	ns	1

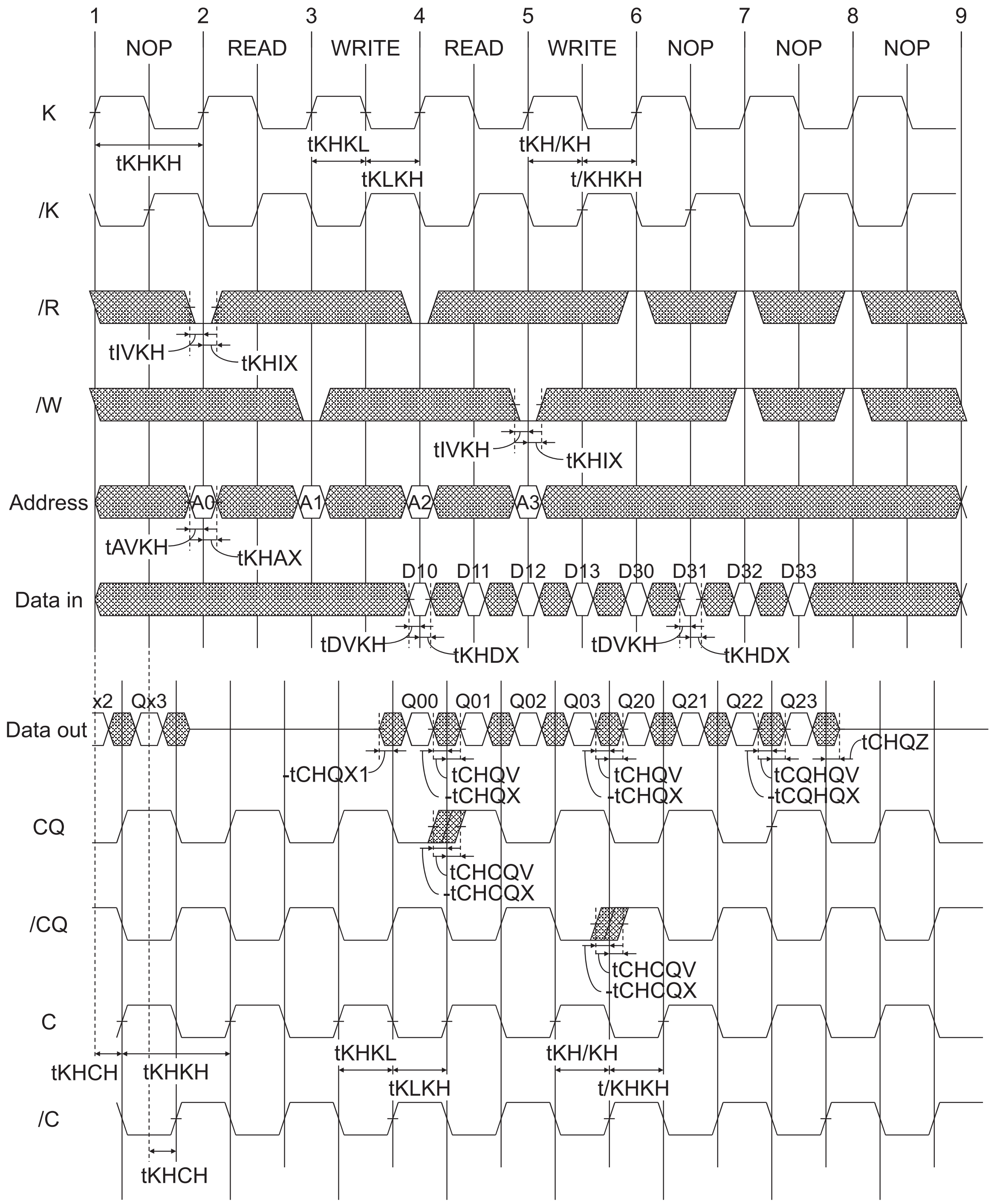
Notes:

1. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.
2. V_{DD} and V_{DDQ} slew rate must be less than 0.1 V DC per 50 ns for PLL lock retention. PLL lock time begins once V_{DD} , V_{DDQ} and input clock are stable.
   It is recommended that the device is kept inactive during these cycles.
3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
4. Transitions are measured ±100 mV from steady-state voltage.
5. These parameters are only guaranteed by design and are not tested in production.

Remarks:

1. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
2. Control input signals may not be operated with pulse widths less than t_{KHKL} (min).
3. If C, /C are tied high, K, /K become the references for C, /C timing parameters.
4. V_{DDQ} is +1.5 V DC. V_{REF} is +0.75 V DC.
5. Control signals are /R and /W.
   Setup and hold times of /BWx signals must be the same as those of Data-in signals.
6. In the case of running frequency between 250MHz and 300MHz, all the AC/DC parameters follow 300MHz.
   In the case of running frequency between 300MHz and 333MHz, all the AC/DC parameters follow 333MHz.

Read and Write Timing



Notes:

1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, i.e., A0+1.
2. In this example, if address A2 = A1, then data Q20 = D10, Q21 = D11, Q22 = D12, Q23 = D13. Write data is forwarded immediately as read results.
3. To control read and write operations, /BW signals must operate at the same timing as Data-in signals. .

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude middle level inputs.
TDI and TMS are internally pulled up and may be unconnected, or may be connected to V_{DD} through a pull up resistor.
TDO should be left unconnected.

Test Access Port (TAP) Pins

Symbol I/O	Pin assignments	Description	Notes
TCK	2R	Test clock input. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.	
TMS	10R	Test mode select. This is the command input for the TAP controller state machine.	
TDI	11R	Test data input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.	
TDO	1R	Test data output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.	

Notes:

The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on SRAM POWER-UP.

TAP DC Operating Characteristics

(T_A = -40 to +85°C , V_{DD} = 1.8V ±0.1V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	+1.3	-	V_{DD} + 0.3	V	
Input low voltage	V_{IL}	-0.3	-	+0.5	V	
Input leakage current	I_{LI}	-5.0	-	+5.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
Output leakage current	I_{LO}	-5.0	-	+5.0	µA	0 V ≤ V_{IN} ≤ V_{DD}, output disabled
Output low voltage	V_{OL1}	-	-	0.2	V	I_{OLC} = 100 µA
	V_{OL2}	-	-	0.4	V	I_{OLT} = 2 mA
Output high voltage	V_{OH1}	1.6	-	-	V	$\lvert I_{OHC}\rvert$ = 100 µA
	V_{OH2}	1.4	-	-	V	$\lvert I_{OHT}\rvert$ = 2 mA

Notes:

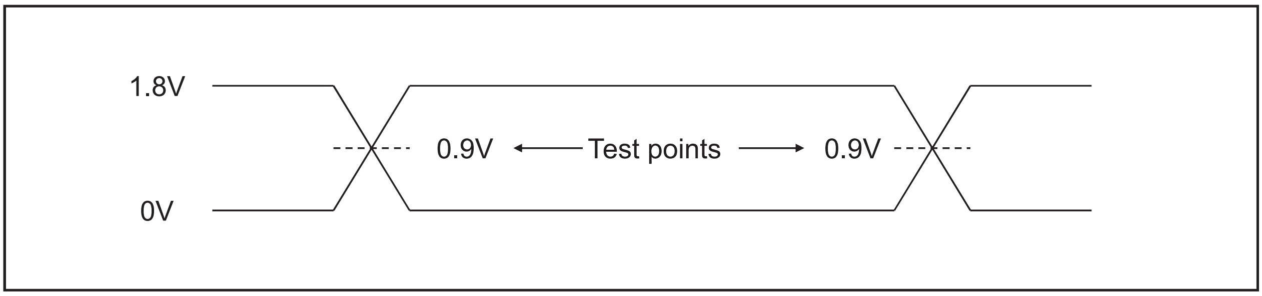
1. All voltages referenced to V_{SS} (GND).
2. At power-up, V_{DD} and V_{DDQ} are assumed to be a linear ramp from 0V to V_{DD}(min.) or V_{DDQ}(min.) within 200ms. During this time, $V_{DDQ} < V_{DD}$ and $V_{IH} < V_{DDQ}$.

   During normal operation, V_{DDQ} must not exceed V_{DD}.

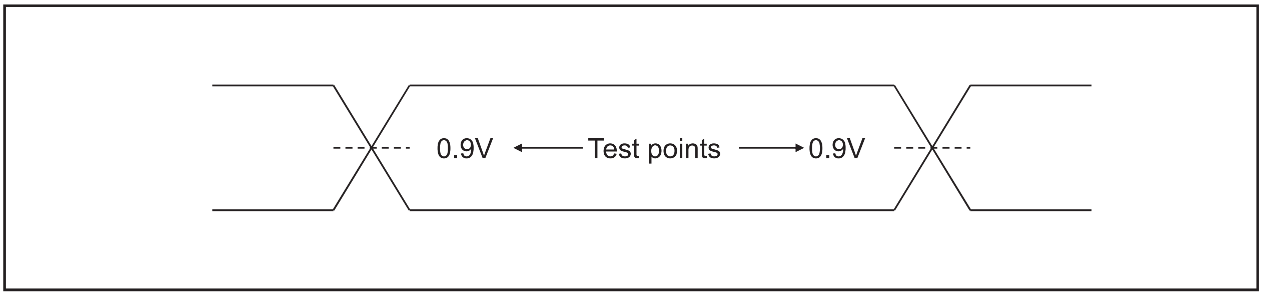
TAP AC Test Conditions

Parameter	Symbol	Conditions	Unit	Notes
Input timing measurement reference levels	V_{REF}	0.9	V	
Input pulse levels	V_{IL}, V_{IH}	0 to 1.8	V	
Input rise/fall time	tr, tf	≤ 1.0	ns	
Output timing measurement reference levels		0.9	V	
Test load termination supply voltage (V_{TT})		0.9	V	
Output load		See figures		

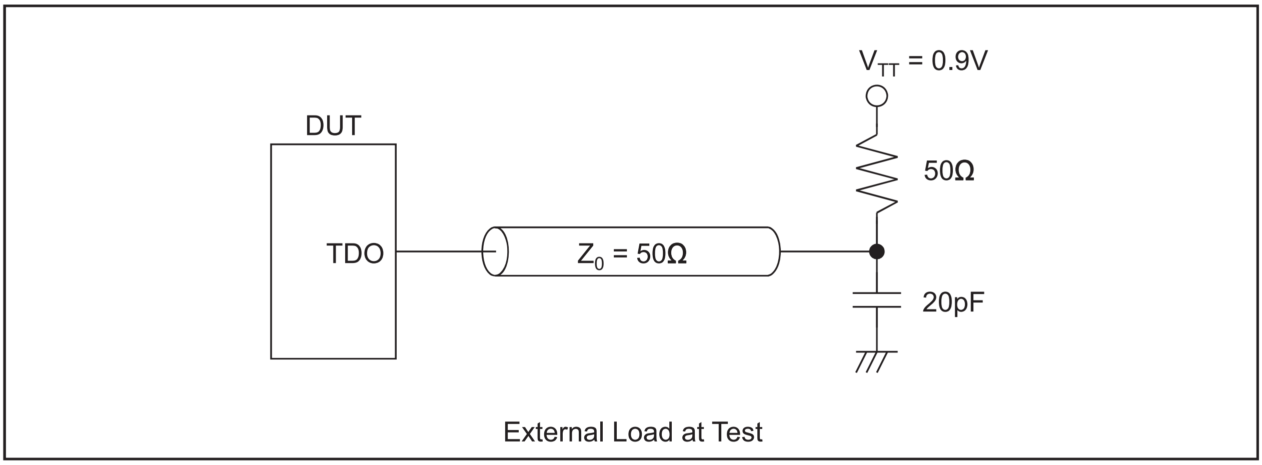
Input waveform



Output waveform



Output load condition



TAP AC Operating Characteristics

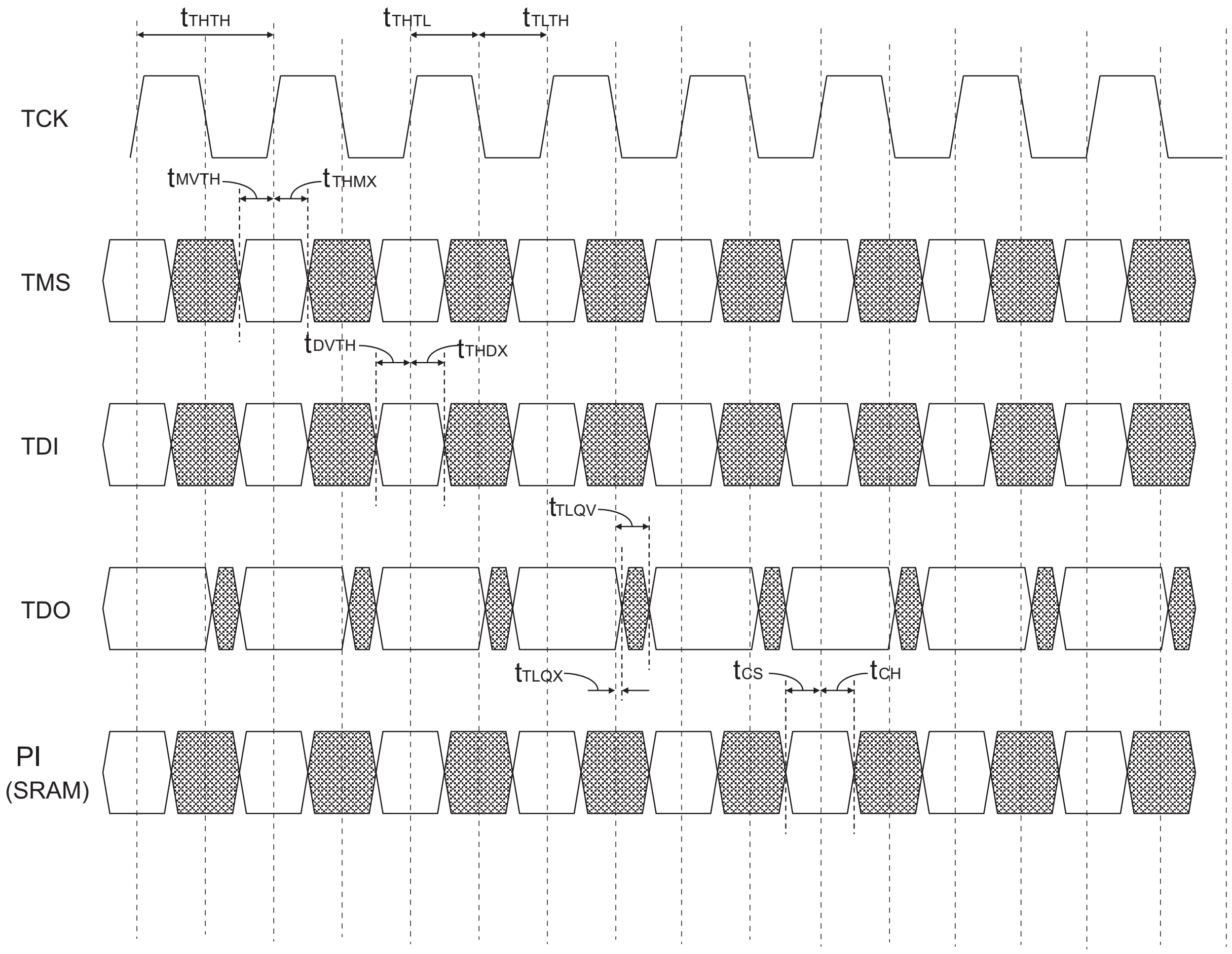
(T_A = -40 to +85°C , V_{DD} = 1.8V ±0.1V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Test clock (TCK) cycle time	t_{THTH}	50	-	-	ns	
TCK high pulse width	t_{THTL}	20	-	-	ns	
TCK low pulse width	t_{TLTH}	20	-	-	ns	
Test mode select (TMS) setup	t_{MVTH}	5	-	-	ns	
TMS hold	t_{THMX}	5	-	-	ns	
Capture setup	t_{CS}	5	-	-	ns	
Capture hold	t_{CH}	5	-	-	ns	
TDI valid to TCK high	t_{DVTH}	5	-	-	ns	
TCK high to TDI invalid	t_{THDX}	5	-	-	ns	
TCK low to TDO unknown	t_{TLQX}	0	-	-	ns	
TCK low to TDO valid	t_{TLQV}	-	-	10	ns	

Notes:

1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

TAP Controller Timing Diagram



Test Access Port Registers

Register name	Length	Symbol	Notes
Instruction register	3 bits	IR [2:0]	
Bypass register	1 bits	BP	
ID register	32 bits	ID [31:0]	
Boundary scan register	109 bit	BS [109:1]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Description	Notes
0	0	0	EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary scan register cells at output balls are used to apply test vectors, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output balls.	1,2,3,4
0	0	1	IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO balls in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.	
0	1	0	SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the RAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.	3,4
0	1	1	RESERVED	The RESERVED instruction is not implemented but is reserved for future use. Do not use this instruction.	
1	0	0	SAMPLE (/PRELOAD)	When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO balls.	3,4
1	0	1	RESERVED	The RESERVED instruction is not implemented but is reserved for future use. Do not use this instruction.	
1	1	0	RESERVED	The RESERVED instruction is not implemented but is reserved for future use. Do not use this instruction.	
1	1	1	BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.	

Notes:

1. Data in output register is not guaranteed if EXTEST instruction is loaded.
2. After performing EXTEST, power-up conditions are required in order to return part to normal operation.
3. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.
4. Clock recovery initialization cycles are required after boundary scan.

Boundary Scan Order

Bit#	Ball ID	Signal names x18	Signal names x36
1	6R	/C	/C
2	6P	C	C
3	6N	SA	SA
4	7P	SA	SA
5	7N	SA	SA
6	7R	SA	SA
7	8R	SA	SA
8	8P	SA	SA
9	9R	SA	SA
10	11P	Q0	Q0
11	10P	D0	D0
12	10N	NC	D9
13	9P	NC	Q9
14	10M	Q1	Q1
15	11N	D1	D1
16	9M	NC	D10
17	9N	NC	Q10
18	11L	Q2	Q2
19	11M	D2	D2
20	9L	NC	D11
21	10L	NC	Q11
22	11K	Q3	Q3
23	10K	D3	D3
24	9J	NC	D12
25	9K	NC	Q12
26	10J	Q4	Q4
27	11J	D4	D4
28	11H	ZQ	ZQ
29	10G	NC	D13
30	9G	NC	Q13
31	11F	Q5	Q5
32	11G	D5	D5
33	9F	NC	D14
34	10F	NC	Q14
35	11E	Q6	Q6
36	10E	D6	D6
37	10D	NC	D15

Bit#	Ball ID	Signal names x18	Signal names x36
38	9E	NC	Q15
39	10C	Q7	Q7
40	11D	D7	D7
41	9C	NC	D16
42	9D	NC	Q16
43	11B	Q8	Q8
44	11C	D8	D8
45	9B	NC	D17
46	10B	NC	Q17
47	11A	CQ	CQ
48	10A	NC	NC
49	9A	SA	SA
50	8B	SA	SA
51	7C	SA	SA
52	6C	NC	NC
53	8A	/R	/R
54	7A	NC	/BW1
55	7B	/BW0	/BW0
56	6B	K	K
57	6A	/K	/K
58	5B	NC	/BW3
59	5A	/BW1	/BW2
60	4A	/W	/W
61	5C	SA	SA
62	4B	SA	SA
63	3A	SA	NC
64	2A	NC	NC
65	1A	/CQ	/CQ
66	2B	Q9	Q18
67	3B	D9	D18
68	1C	NC	D27
69	1B	NC	Q27
70	3D	Q10	Q19
71	3C	D10	D19
72	1D	NC	D28
73	2C	NC	Q28
74	3E	Q11	Q20

Bit#	Ball ID	Signal names x18	Signal names x36
75	2D	D11	D20
76	2E	NC	D29
77	1E	NC	Q29
78	2F	Q12	Q21
79	3F	D12	D21
80	1G	NC	D30
81	1F	NC	Q30
82	3G	Q13	Q22
83	2G	D13	D22
84	1H	/DOFF	/DOFF
85	1J	NC	D31
86	2J	NC	Q31
87	3K	Q14	Q23
88	3J	D14	D23
89	2K	NC	D32
90	1K	NC	Q32
91	2L	Q15	Q24
92	3L	D15	D24
93	1M	NC	D33
94	1L	NC	Q33
95	3N	Q16	Q25
96	3M	D16	D25
97	1N	NC	D34
98	2M	NC	Q34
99	3P	Q17	Q26
100	2N	D17	D26
101	2P	NC	D35
102	1P	NC	Q35
103	3R	SA	SA
104	4R	SA	SA
105	4P	SA	SA
106	5P	SA	SA
107	5N	SA	SA
108	5R	SA	SA
109	-	Internal	Internal

Notes:

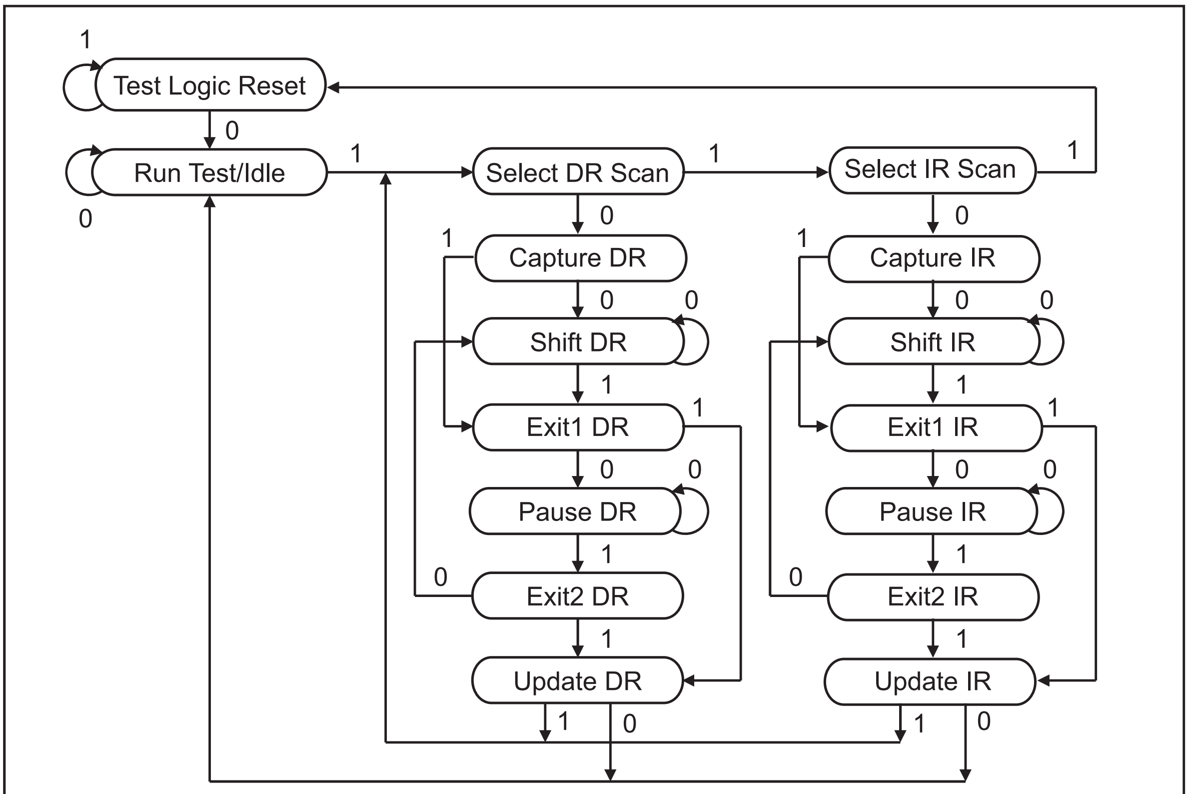
In boundary scan mode,

1. Clock balls (K, /K, C, /C) are referenced to each other and must be at opposite logic levels for reliable operation.
2. CQ and /CQ data are synchronized to the C clock (except EXTEST, SAMPLE-Z).
3. If C and /C tied high, CQ and /CQ are generated with respect to K clock instead of C clock (except EXTEST, SAMPLE-Z).

ID Register

#	Revision number (31:28)				Type number (27:12)																Vendor JEDEC code (11:1)											Start bit (0)
#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMQS3A3636DGBA	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1
RMQS3A3618DGBA	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1

TAP Controller State Diagram



Notes:

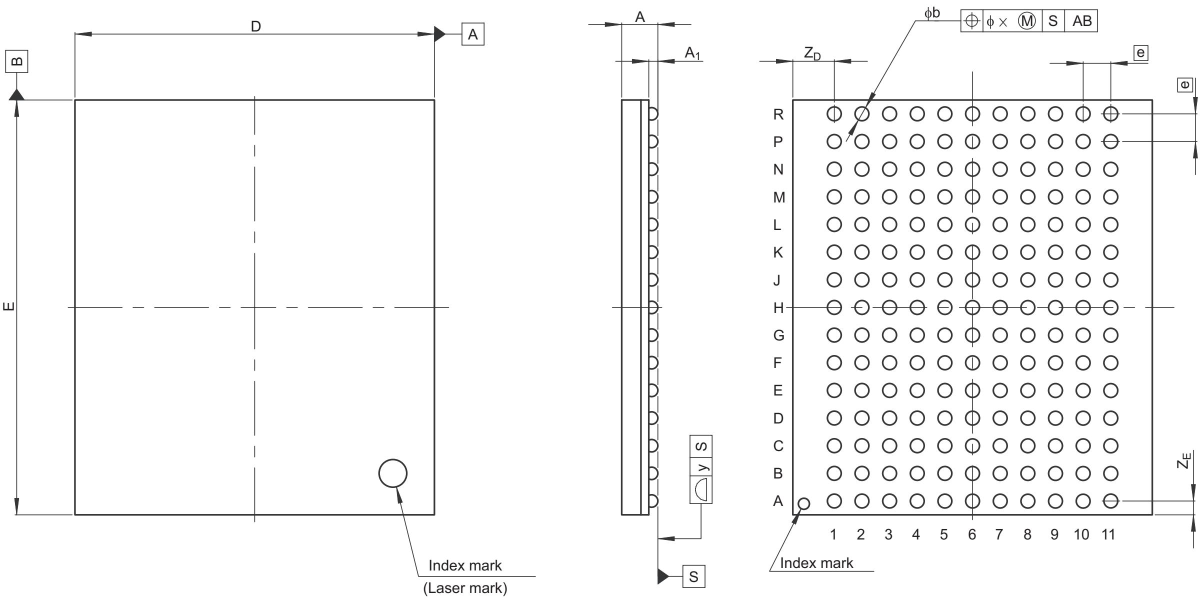
The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions

165-pin FBGA (13 x 15 x 1.4 mm)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LBGA165-13x15-1.00	PLBG0165FE-A	165FHG-A	0.5g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.9	13.0	13.1
E	14.9	15.0	15.1
A	——	——	1.4
A_1	0.31	0.36	0.41
$\boxed{e}$	——	1.0	——
b	0.45	0.5	0.6
x	——	——	0.2
y	——	——	0.15
Z_D	——	1.5	——
Z_E	——	0.5	——

Revision History	RMQS3A3636DGBA, RMQS3A3618DGBA

Rev.	Date	Description	
		Page	Summary
Rev.0.01	’14.04.25	-	New Preliminary Datasheet.
Rev.0.02	’14.12.01	P.15, 16	Modify the “Supply Current” and “Thermal Resistance”.
Rev.1.00	’15.01.13	-	New Datasheet.

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