RL78/G1H
RENESAS MCU

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1. OUTLINE

RL78/G1H is a microcontroller equipped with the low-power-consumption RF transceiver compatible with the SubGHz-band wireless communication. The wireless communication in the SubGHz band is best for the smart meter communication part, HEMS controller, wireless sensor network, etc.

1.1 Features

Ultra-low power consumption technology

- Standby function of MCU: HALT mode, STOP mode, SNOOZE mode
- <R> Standby function of RF unit: IDLE mode, SLEEP mode
  - Current drawn by the RF transceiver during transmission
    : 21 mA (typ.) with a transfer rate of 100 kbps, 2GFSK as the modulation method, +10 dBm of power, and the MCU operating at 3.0 V in STOP mode
    : 36 mA (typ.) with a transfer rate of 100 kbps, 2GFSK as the modulation method, +13 dBm of power, and the MCU operating at 3.0 V in STOP mode
  - Current drawn by the RF transceiver during reception
    : 6.9 mA (typ.) with a transfer rate of 100 kbps, 2GFSK as the modulation method, and the MCU operating at 3.0 V in STOP mode
  - Current drawn by the RF transceiver in SLEEP mode (POWER DOWN mode)
    : 0.1 μA (typ.) with the MCU operating at 3.0 V in STOP mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 μs: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 μs: @ 32.768 kHz operation with subsystem clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 24 to 48 KB

On-chip RF transceiver

- IEEE802.15.4g standard specification SubGHz-band transceiver
- RF frequency range: 863 to 928 MHz
- Modulation method: 2FSK/GFSK, 4FSK/GFSK
- Data rate: 2FSK/GFSK 10 to 300 kbps, 4FSK/GFSK 200/400 kbps
- Forward error correction (FEC) function

Code flash memory

- Code flash memory: 256 to 512 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 3.6 V

High-speed on-chip oscillator

- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz

Operating ambient temperature

- T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 10 levels)

Data transfer controller (DTC)
- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

Event link controller (ELC)
- Event signals of 13 types can be linked to the specified peripheral function.

Serial interface
- CSI: 4 channels (1 channel of 4 channels is used for the internal communication between MCU and RF transceiver.)
- UART: 2 channels
- I^2C: 2 channels

Timer
- 16-bit timer: 9 channels
- 12-bit interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter
- 10-bit resolution A/D converter (V_{DD} = 1.8 to 3.6 V)
- Analog input: 6 channels

I/O port
- I/O port: 41
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5 V device
- On-chip clock output/buzzer output controller

Cipher
- AES cipher processing (128-bit key length)
- Random number generator (true random number, complies with AIS31 standard)

Others
- On-chip BCD (binary-coded decimal) correction circuit

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G1H
256 KB	8 KB	24 KB	R5F11FLJ
384 KB	8 KB	32 KB	R5F11FLK
512 KB	8 KB	48 KB **Note**	R5F11FLL

Note This is about 47 KB when the self-programming function is used (For details, see **CHAPTER 4** in the User's Manual: Hardware).

1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1H

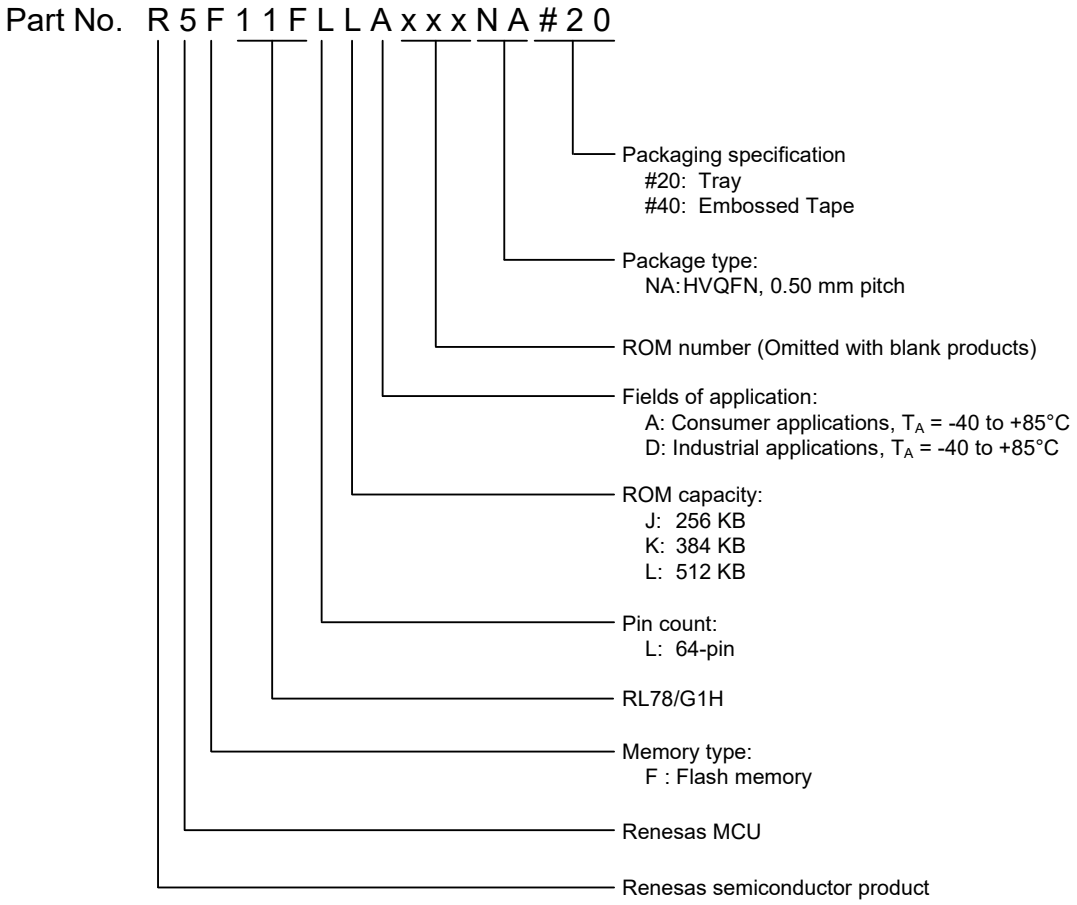


Table 1 - 1 Ordering Part Number List

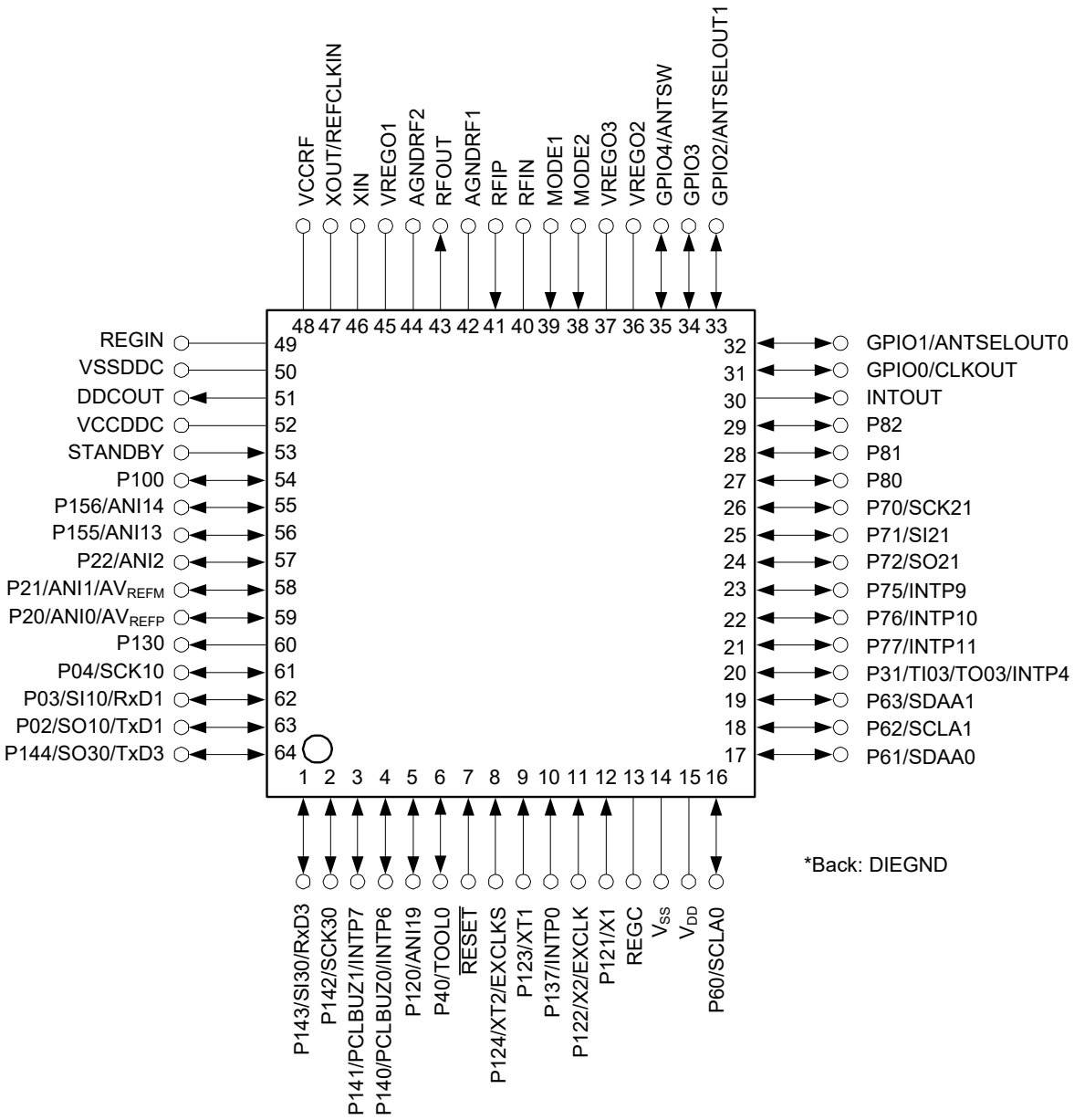
Pin count	Package	Fields of Application Note	Ordering Part Number	Code Flash Memory	Data Flash Memory
64 pins	64-pin plastic HVQFN (9 × 9)	A	R5F11FLJANA#20, R5F11FLJANA#40	256 Kbytes	8 Kbytes
		D	R5F11FLJDNA#20, R5F11FLJDNA#40		
		A	R5F11FLKANA#20, R5F11FLKANA#40	384 Kbytes	
		D	R5F11FLKDNA#20, R5F11FLKDNA#40		
		A	R5F11FLLANA#20, R5F11FLLANA#40	512 Kbytes	
		D	R5F11FLLDNA#20, R5F11FLLDNA#40		

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1H**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

• 64-pin plastic HVQFN (9 × 9)



Caution **Connect the metal pad (DIEGND) on the back of the package to GND of the board.**

Remark For pin identification, see **1.4 Pin Identification**.

1.4 Pin Identification

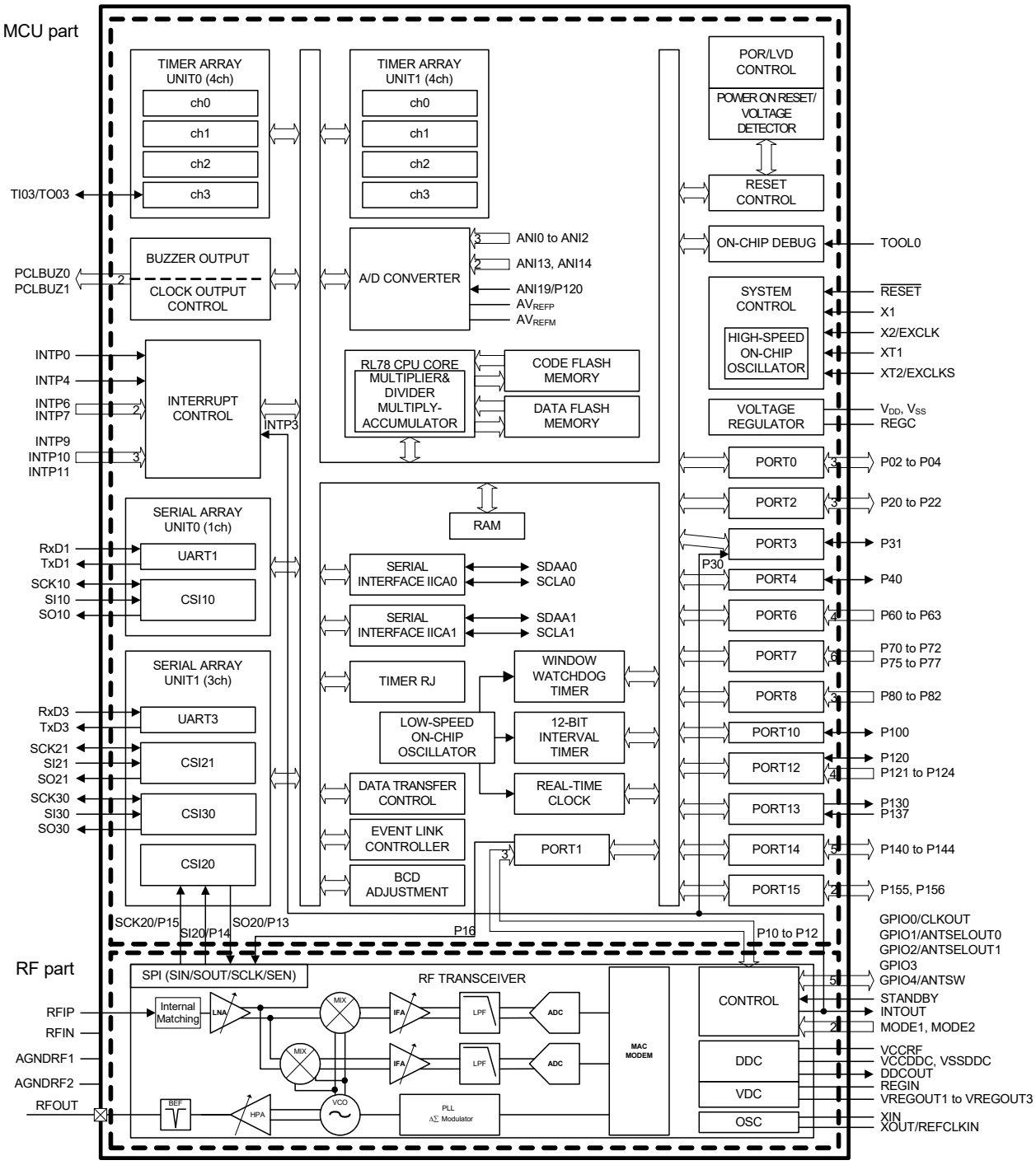
<MCU unit>

ANI0 to ANI2, ANI13:	Analog Input	P130, P137:	Port 13
ANI14, ANI19:	Analog Input	P140 to P144:	Port 14
AV_{REFM}:	Analog Reference	P155, P156:	Port 15
	Voltage Minus	PCLBUZ0, PCLBUZ1:	Programmable Clock Output/
AV_{REFP}:	Analog Reference		Buzzer Output
	Voltage Plus	REGC:	Regulator Capacitance
EXCLK:	External Clock Input	$\overline{\text{RESET}}$:	Reset
	(Main System Clock)	RxD1, RxD3:	Receive Data
EXCLKS:	External Clock Input	SCK10, SCK21,	
	(Subsystem Clock)	SCK30:	Serial Clock Input/Output
INTP0, INTP4:	External Interrupt Input	SCLA0, SCLA1:	Serial Clock Output
INTP6, INTP7:		SDAA0, SDAA1:	Serial Data Input/Output
INTP9 to INTP11:		SI10, SI21, SI30:	Serial Data Input
P02 to P04:	Port 0	SO10, SO21, SO30:	Serial Clock Output
P20 to P22:	Port 2	TI03:	Timer Input
P31:	Port 3	TO03:	Timer Output
P40:	Port 4	TOOL0:	Data Input/Output for Tool
P60 to P63:	Port 6	TxD1, TxD3:	Transmit Data
P70 to P72, P75 to P77:	Port 7	V_{DD}:	Power Supply
P80 to P82:	Port 8	V_{SS}:	Ground
P100:	Port 10	X1, X2:	Crystal Oscillator (Main System Clock)
P120 to P124:	Port 12	XT1, XT2:	Crystal Oscillator (Subsystem Clock)

<RF transceiver unit>

GPIO0-GPIO4	Transceiver I/O port	VREGO1:	Power supply stability
CLKOUT:	Clock output		capacity connection for RF
ANTSELOUT0,	Antenna select	XIN:	Buffer input for the 48 MHz
ANTSELOUT1:			X'tal oscillation
ANTSW:	Antenna switch	XOUT:	48 MHz crystal resonator output
VREGO2:	Power supply stabilization	REFCLKIN:	External clock input
	capacitor connection pin for VCO	REGIN:	Power supply input for the analog, and
VREGO3:	Power supply stability capacity		externally connect with DDCOUT
	connection for PLL	VSSDDC:	DCDC converter GND
MODE1, MODE2:	Mode switch	DDCOUT:	The DCDC converter output, to externally
RFIN:	Transceiver GND		connect with REGIN
RFIP:	RF input	VCCDDC:	DCDC converter power supply
AGNDRF1:	Transceiver GND	STANDBY:	Power down control input of the transceiver,
RFOUT:	RF output		and externally connect with P130
AGNDRF2:	Transceiver GND	INTOUT:	Interrupt output

1.5 Block Diagram



1.6 Outline of Functions

(1/2)

Item		R5F11FLJ	R5F11FLK	R5F11FLL
Code flash memory (KB)		256 KB	384 KB	512 KB
Data flash memory (KB)		8 KB	8 KB	8 KB
RAM (KB)		24 KB	32 KB	48 KB Note 1
Address space		1 MB		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillator, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 3.6 V) HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V) LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V)		
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 3.6 V), HS (high-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V),		
Subsystem clock		XT1 (crystal) oscillator, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.)		
Low-speed on-chip oscillator clock		15 kHz (TYP.)		
RF base clock		48 MHz (TYP.)		
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)		
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)		
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)		
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and boolean operation), etc.		
I/O port	Total	41 Note 2		
	CMOS I/O	26		
	CMOS input	5		
	CMOS output	1 Note 2		
	N-ch open-drain I/O (6 V tolerance)	4		
	GPIO (RF unit)	5		
SubGHz RF transceiver		• IEEE802.15.4g standard specification SubGHz-band transceiver • RF frequency range: 863 to 928 MHz • Modulation method: 2FSK/GFSK, 4FSK/GFSK		
Timer	16-bit timer	9 channels		
	Watchdog timer	1 channel		
	Real-time clock (RTC)	1 channel		
	12-bit interval timer	1 channel		
	Timer output	1 channel		

(2/2)

Item		R5F11FLJ	R5F11FLK	R5F11FLL
Clock output/buzzer output		2		
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)		
10-bit resolution A/D converter		6 channels		
Serial interface		• CSI/UART: 2 channels • CSI: 2 channels (1 channel of 2 channels is used for the internal communication between MCU and RF transceiver.)		
	I^2C bus	2 channels		
Data transfer controller (DTC)		21 sources		
Vectored interrupt sources	Internal	26		
	External	7		
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution **Note 3** • Internal reset by RAM parity error • Internal reset by illegal-memory access		
Power-on-reset circuit		• Power-on-reset: 1.51 (TYP.) • Power-down-reset: 1.50 (TYP.)		
Voltage detector		• Rising edge: 1.88 V to 3.13 V (10 stages) • Falling edge: 1.84 V to 3.06 V (10 stages)		
On-chip debug function		Provided		
Power supply voltage		V_{DD} = 1.8 to 3.6 V		
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications)		
Package		64-pin HVQFN (9 × 9), (0.5 mm pitch)		

Note 1. This is about 47 KB when the self-programming function is used (For details, see **CHAPTER 4** in the User's Manual: Hardware).

Note 2. When using the RF transceiver, pins which a user uses for external connection between the MCU and RF transceiver on the board are included.

Note 3. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

This chapter describes the electrical specifications for the following products

The target products A: Consumer applications (T_A = –40 to +85°C)
R5F11FLxANA
D: Industrial applications (T_A = –40 to +85°C)
R5F11FLxDNA

Caution The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/2)**

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	–0.5 to +3.8 **Note 1**	V
	V_{DDRF}	VCCRF, VCCDDC	–0.3 to +3.8 **Note 1**	V
	V_{SS}	V_{SS}	–0.3 to +0.3	V
	V_{SSRF}	VSSDDC, AGNDRF1, AGNDRF2, RFIN, DIEGND	–0.3 to +0.3	V
Input voltage	V_{I1}	P02 to P04, P20 to P22, P31, P40, P70 to P72, P75 to P77, P80 to P82, P120 to P124, P137, P140 to P144, P155, P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	–0.3 to V_{DD} + 0.3 **Note 2**	V
	V_{I2}	P100	–0.3 to V_{DD} + 0.3 and –0.3 to V_{DDRF} + 0.3 **Note 2**	V
	V_{I3}	P60 to P63 (N-ch open-drain)	–0.3 to +6.5	V
	V_{IRF1}	STANDBY, GPIO0 to GPIO4, MODE1, MODE2	–0.3 to V_{DDRF} + 0.3 **Note 2**	V
	V_{IRF2}	XIN, REFCLKIN	–0.3 to +1.25	V
	V_{IRF3}	RFIP	–2.0 to +2.0 **Note 3**	V
Output voltage	V_{O1}	P02 to P04, P20 to P22, P31, P40, P60 to P63, P70 to P72, P75 to P77, P80 to P82, P100, P120, P130, P140 to P144, P155, P156	–0.3 to V_{DD} + 0.3 **Note 2**	V
	V_{O2}	P100, INTOUT	–0.3 to V_{DD} + 0.3 and –0.3 to V_{DDRF} + 0.3 **Note 2**	V
	V_{O3}	P60 to P63 (N-ch open-drain)	–0.3 to +6.5	V
	V_{ORF1}	GPIO0 to GPIO4	–0.3 to V_{DDRF} + 0.3 **Note 2**	V
	V_{ORF2}	XOUT	–0.3 to +1.25	V
	V_{ORF3}	RFOUT	–2.0 to +2.0 **Note 3**	V
Analog input voltage	V_{AI}	ANI0 to ANI2, ANI13, ANI14, ANI19	–0.3 to V_{DD} + 0.3 and –0.3 to $AV_{REF}(+)$ + 0.3 **Notes 2, 4**	V

Note 1. Satisfy the relationship of $V_{DD} \geq$ VCCRF and VCCDDC upon power application.

Note 2. Must be 3.8 V or lower.

Note 3. This value is AC rating. Impression of DC voltage is prohibited to RFIP and RFOUT pins.

Note 4. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}, V_{SSRF}: Reference voltage

Absolute Maximum Ratings **(2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
REGC pin input voltage	V_{IREGC}	REGC		–0.3 to +2.8 and –0.3 to V_{DD} + 0.3 **Note**	V
RF power supply input	V_{REGIN}	REGIN		–0.3 to +3.8	V
RF power supply output	V_{RFOUT1}	DDCOUT		–0.3 to +3.8	V
	V_{RFOUT2}	VREGO1, VREGO2, VREGO3		–0.3 to +1.25	V
Output current, high	I_{OH1}	Per pin	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P130, P140 to P144	–40	mA
		Total of all pins –170 mA	P02 to P04, P40, P120, P130, P140 to P144	–70	mA
			P31, P70 to P72, P75 to P77, P80 to P82, P100	–100	mA
	I_{OH2}	Per pin	P20 to P22, P155, P156	–0.5	mA
		Total of all pins		–2	mA
	I_{OHRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4	–17	mA
Output current, low	I_{OL1}	Per pin	P02 to P04, P31, P40, P60 to P63, P70 to P72, P75 to P77, P80 to P82, P100, P120, P130, P140 to P144	40	mA
		Total of all pins 170 mA	P02 to P04, P40, P120, P130, P140 to P144	70	mA
			P31, P60 to P63, P70 to P72, P75 to P77, P80 to P82, P100	100	mA
	I_{OL2}	Per pin	P20 to P22, P155, P156	1	mA
		Total of all pins		5	mA
	I_{OLRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4	17	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150	°C

Note Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) **Note**	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
XT1 clock oscillation frequency (f_{XT}) **Note**	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, refer to **6.4 System Clock Oscillator** in the User's Manual: Hardware.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency **Notes 1, 2**	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85°C	1.8 V ≤ V_{DD} ≤ 3.6 V	–1.0		+1.0	%
		–40 to –20°C	1.8 V ≤ V_{DD} ≤ 3.6 V	–1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P130, P140 to P144				–10.0 Note 2	mA
		Total of P02 to P04, P40, P120, P130, P140 to P144 (When duty ≤ 70% Note 3)	2.7 V ≤ V_{DD} ≤ 3.6 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P31, P70 to P72, P75 to P77, P80 to P82, P100 (When duty ≤ 70% Note 3)	2.7 V ≤ V_{DD} ≤ 3.6 V			–19.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				–29.0	mA
	I_{OH2}	Per pin for P20 to P22, P155, P156				–0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)				–0.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≈ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

<R>

Caution P02 to P04, P71, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(2/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low **Note 1**	I_{OL1}	Per pin for P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P130, P140 to P144				20.0 **Note 2**	mA
		Per pin for P60 to P63				15.0 **Note 2**	mA
		Total of P02 to P04, P40, P120, P130, P140 to P144 (When duty ≤ 70% **Note 3**)	2.7 V ≤ V_{DD} ≤ 3.6 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P31, P60 to P63, P70 to P72, P75 to P77, P80 to P82, P100 (When duty ≤ 70% **Note 3**)	2.7 V ≤ V_{DD} ≤ 3.6 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% **Note 3**)				50.0	mA
	I_{OL2}	Per pin for P20 to P22, P155, P156				0.4 **Note 2**	mA
		Total of all pins (When duty ≤ 70% **Note 3**)				2.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P140 to P144	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P03, P04, P80, P81, P142, P143	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	2.0		V_{DD}	V
			TTL input buffer 1.8 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20 to P22, P155, P156		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P140 to P144	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	P03, P04, P80, P81, P142, P143	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	0		0.5	V
			TTL input buffer 1.8 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P22, P155, P156		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution The maximum value of V_{IH} of pins P02 to P04, P71, P80 to P82, and P142 to P144 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P130, P140 to P144	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH1} = –2.0 mA	V_{DD} – 0.6			V
			1.8 V ≤ V_{DD} ≤ 3.6 V, I_{OH1} = –1.5 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P22, P155, P156	1.8 V ≤ V_{DD} ≤ 3.6 V, I_{OH2} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P130, P140 to P144	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 3.6 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P22, P155, P156	1.8 V ≤ V_{DD} ≤ 3.6 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 3.6 V, I_{OL3} = 2.0 mA			0.4	V

Caution P02 to P04, P71, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(5/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P140 to P144	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P22, P137, P155, P156, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P140 to P144	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P20 to P22, P137, P155, P156, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
On-chip pull-up resistance	R_U	P02 to P04, P31, P40, P70 to P72, P75 to P77, P80 to P82, P100, P120, P140 to P144	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	HS (high-speed main) mode **Note 5**	f_{IH} = 32 MHz **Note 3**	Basic operation	V_{DD} = 3.0 V		2.5		mA
			HS (high-speed main) mode **Note 5**	f_{IH} = 32 MHz **Note 3**	Normal operation	V_{DD} = 3.0 V		5.5	10.6	mA
				f_{IH} = 24 MHz **Note 3**	Normal operation	V_{DD} = 3.0 V		4.4	8.2	
				f_{IH} = 16 MHz **Note 3**	Normal operation	V_{DD} = 3.0 V		3.3	5.9	
			LS (low-speed main) mode **Note 5**	f_{IH} = 8 MHz **Note 3**	Normal operation	V_{DD} = 3.0 V		1.5	2.5	mA
						V_{DD} = 2.0 V		1.5	2.5	
			HS (high-speed main) mode **Note 5**	f_{MX} = 20 MHz **Note 2**, V_{DD} = 3.0 V	Normal operation	Square wave input		3.7	6.8	mA
						Resonator connection		3.9	7.0	
				f_{MX} = 8 MHz **Note 2**, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	4.1	
						Resonator connection		2.0	4.2	
			LS (low-speed main) mode **Note 5**	f_{MX} = 8 MHz **Note 2**, V_{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA
						Resonator connection		1.4	2.5	
				f_{MX} = 8 MHz **Note 2**, V_{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.4	
						Resonator connection		1.4	2.5	
			Subsystem clock operation	f_{SUB} = 32.768 kHz **Note 4** T_A = –40°C	Normal operation	Square wave input		5.2		µA
						Resonator connection		5.2		
				f_{SUB} = 32.768 kHz **Note 4** T_A = +25°C	Normal operation	Square wave input		5.3	7.7	
						Resonator connection		5.3	7.7	
				f_{SUB} = 32.768 kHz **Note 4** T_A = +50°C	Normal operation	Square wave input		5.5	10.6	
						Resonator connection		5.5	10.6	
				f_{SUB} = 32.768 kHz **Note 4** T_A = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				f_{SUB} = 32.768 kHz **Note 4** T_A = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	

(Notes and Remarks are listed on the next page.)

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the RF transceiver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current **Note 1**	I_{DD2} **Note 2**	HALT mode	HS (high-speed main) mode **Note 7**	f_{IH} = 32 MHz **Note 4**	V_{DD} = 3.0 V		0.5	2.63	mA
				f_{IH} = 24 MHz **Note 4**	V_{DD} = 3.0 V		0.42	2.03	
				f_{IH} = 16 MHz **Note 4**	V_{DD} = 3.0 V		0.39	1.50	
			LS (low-speed main) mode **Note 7**	f_{IH} = 8 MHz **Note 4**	V_{DD} = 3.0 V		270	800	µA
					V_{DD} = 2.0 V		270	800	
			HS (high-speed main) mode **Note 7**	f_{MX} = 20 MHz **Note 3**, V_{DD} = 3.0 V	Square wave input		0.31	1.69	mA
					Resonator connection		0.41	1.91	
				f_{MX} = 8 MHz **Note 3**, V_{DD} = 3.0 V	Square wave input		0.16	0.94	
					Resonator connection		0.21	1.02	
			LS (low-speed main) mode **Note 7**	f_{MX} = 8 MHz **Note 3**, V_{DD} = 3.0 V	Square wave input		110	610	µA
					Resonator connection		150	660	
				f_{MX} = 8 MHz **Note 3**, V_{DD} = 2.0 V	Square wave input		110	610	
					Resonator connection		150	660	
			Subsystem clock operation	f_{SUB} = 32.768 kHz **Note 5**, T_A = –40°C	Square wave input		0.31		µA
					Resonator connection		0.50		
				f_{SUB} = 32.768 kHz **Note 5**, T_A = +25°C	Square wave input		0.38	0.76	
					Resonator connection		0.57	0.95	
				f_{SUB} = 32.768 kHz **Note 5**, T_A = +50°C	Square wave input		0.47	3.59	
					Resonator connection		0.70	3.78	
				f_{SUB} = 32.768 kHz **Note 5**, T_A = +70°C	Square wave input		0.80	6.20	
					Resonator connection		1.00	6.39	
				f_{SUB} = 32.768 kHz **Note 5**, T_A = +85°C	Square wave input		1.65	10.56	
					Resonator connection		1.84	10.75	
	I_{DD3} **Note 6**	STOP mode **Note 8**	T_A = –40°C				0.19		µA
			T_A = +25°C				0.30	0.59	
			T_A = +50°C				0.41	3.42	
			T_A = +70°C				0.80	6.03	
			T_A = +85°C				1.53	10.39	

(Notes and Remarks are listed on the next page.)

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the RF transceiver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

Peripheral Functions (Common to all products)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 3.3 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	
		DTC operation			3.10		

Note 1. Current flowing to V_{DD}.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Note 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

Note 8. Current flowing during programming of the data flash.

Note 9. Current flowing during self-programming.

Note 10. For shift time to the SNOOZE mode, see **20.3.3 SNOOZE mode** in the User's Manual: Hardware.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

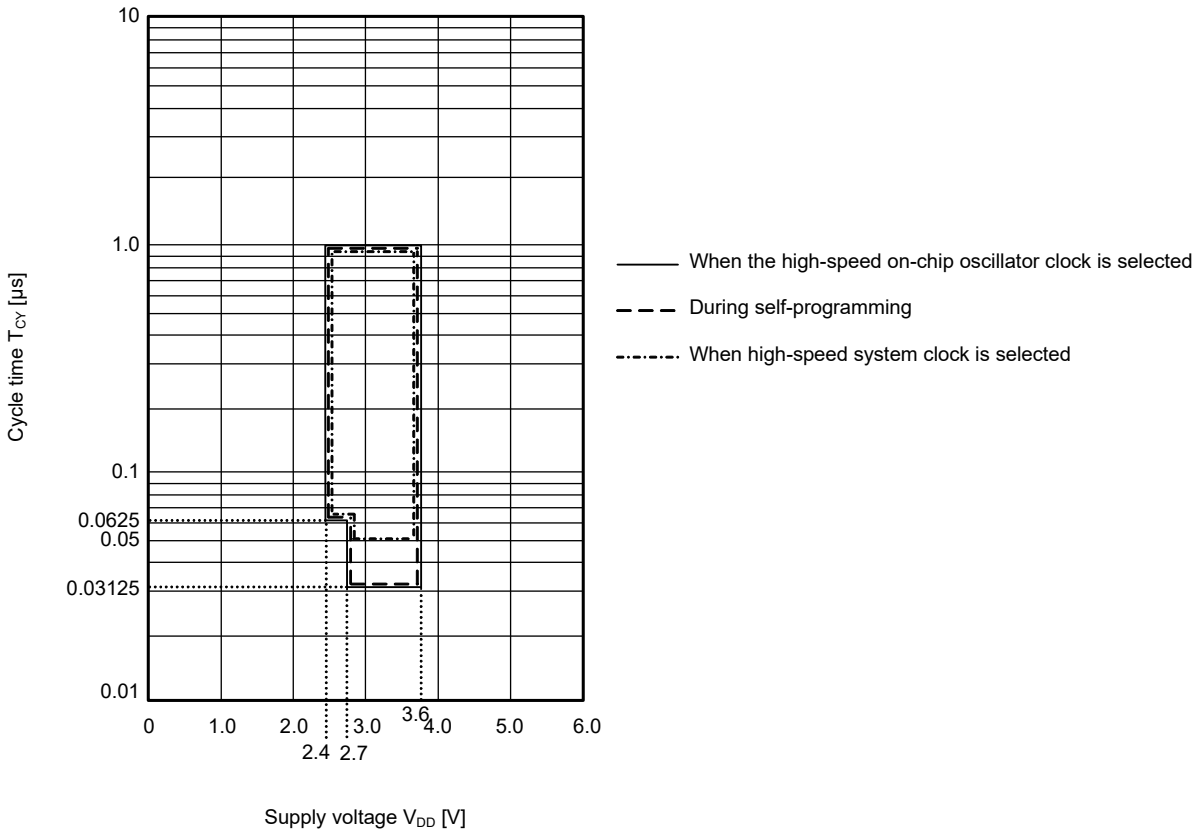
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	µs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	µs
		Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 3.6 V	28.5	30.5	31.3	µs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	µs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	µs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 3.6 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 3.6 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
		1.8 V ≤ V_{DD} < 2.4 V			60			ns
	t_{EXHS}, t_{EXLS}				13.7			µs
TI03 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO03 output frequency	f_{TO}	HS (high-speed main) mode		2.7 V ≤ V_{DD} ≤ 3.6 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
		LS (low-speed main) mode		1.8 V ≤ V_{DD} ≤ 3.6 V			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		2.7 V ≤ V_{DD} ≤ 3.6 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
		LS (low-speed main) mode		1.8 V ≤ V_{DD} ≤ 3.6 V			4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP4, INTP6, INTP7, INTP9 to INTP11		1.8 V ≤ V_{DD} ≤ 3.6 V	1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			µs

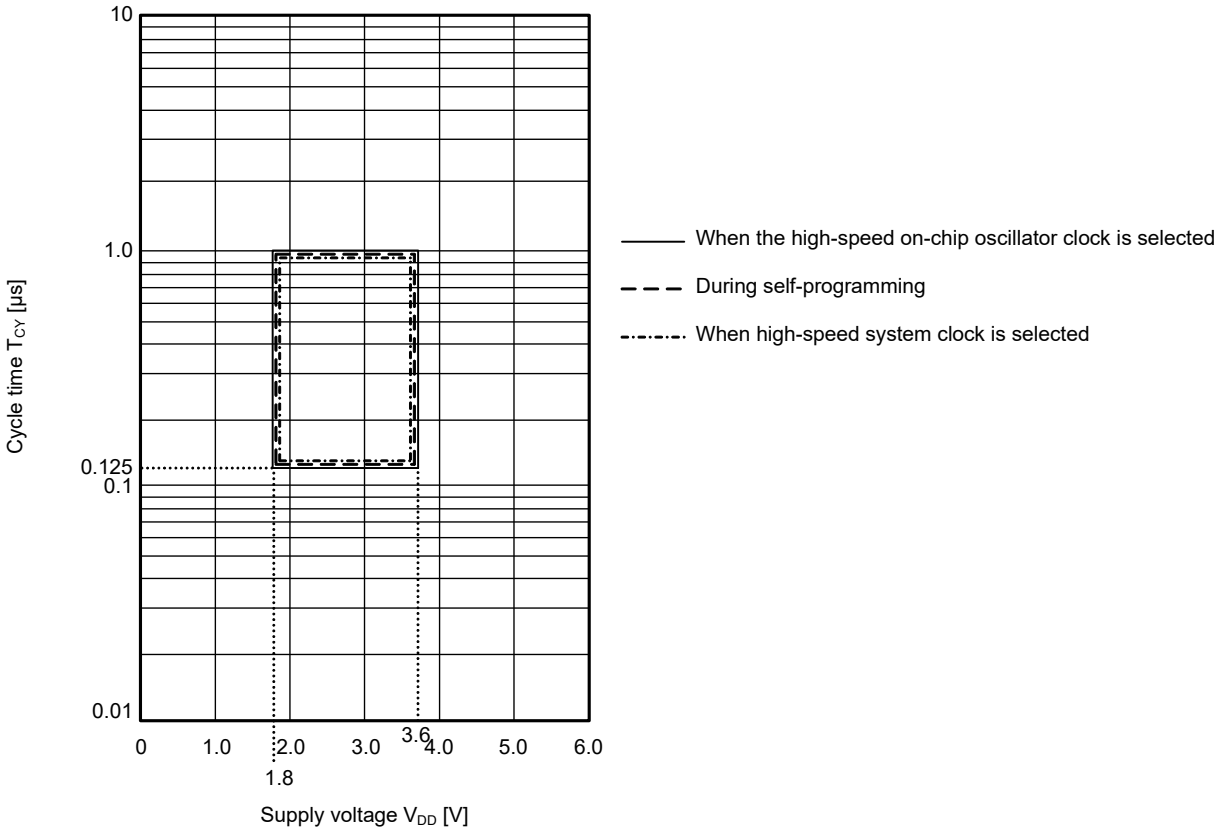
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 3))

Minimum Instruction Execution Time during Main System Clock Operation

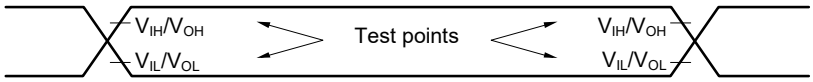
T_{CY} vs V_{DD} (HS (high-speed main) mode)



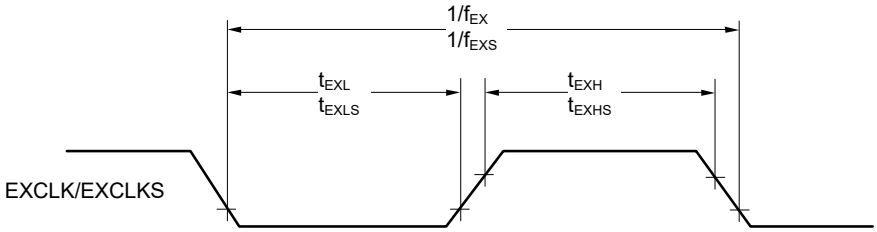
T_{CY} vs V_{DD} (LS (low-speed main) mode)



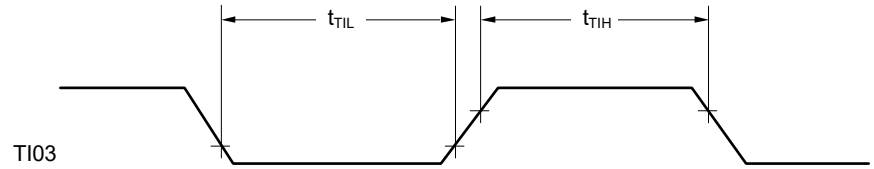
AC Timing Test Points

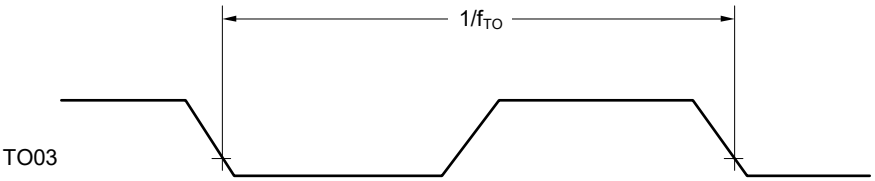


External System Clock Timing

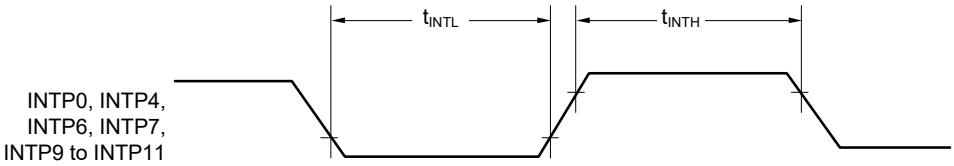


TI/TO Timing

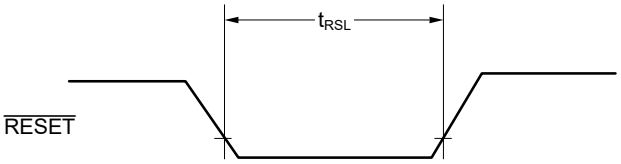




Interrupt Request Input Timing

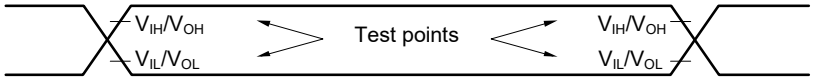


$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

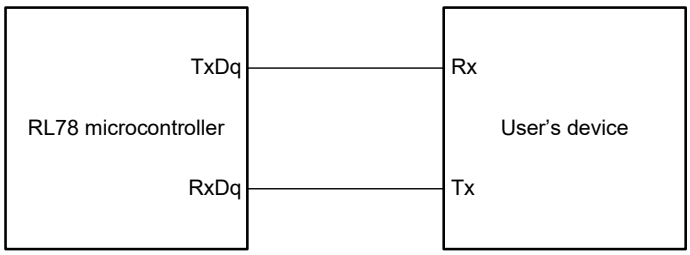
(TA = –40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate		2.4 V ≤ VDD ≤ 3.6 V		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK **Note**		5.3		1.3	Mbps
		1.8 V ≤ VDD ≤ 3.6 V		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note		5.3		1.3	Mbps

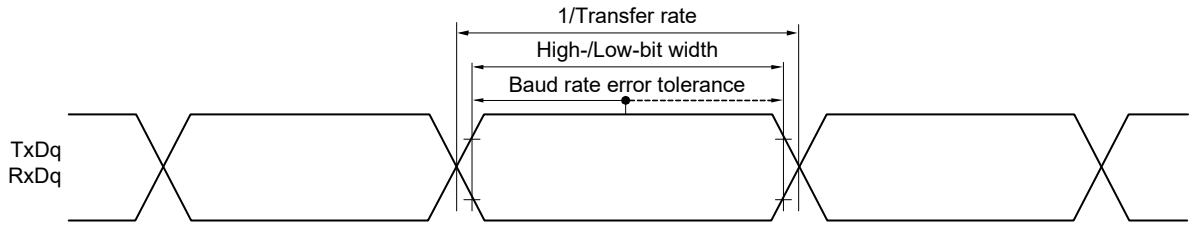
Note The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 3.6 V)
16 MHz (2.4 V ≤ VDD ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 3.6 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 1, 3), g: PIM and POM number (g = 0, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 02, 03, 12, 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 3.6 V	125		500		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	250		500		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	500		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		$t_{KCY1}/2 - 18$		$t_{KCY1}/2 - 50$		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		$t_{KCY1}/2 - 38$		$t_{KCY1}/2 - 50$		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
SIp setup time (to SCKp↑) **Note 1**	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		44		110		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		75		110		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		110		110		ns
SIp hold time (from SCKp↑) **Note 2**	t_{KSI1}	1.8 V ≤ V_{DD} ≤ 3.6 V		19		19		ns
Delay time from SCKp↓ to SOp output **Note 3**	t_{KSO1}	1.8 V ≤ V_{DD} ≤ 3.6 V C = 30 pF **Note 4**			25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 10, 21, 30), m: Unit number (m = 0, 1), n: Channel number (n = 1, 2),
g: PIM and POM number (g = 0, 14)

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supported only for CSI20)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.4 V ≤ V_{DD} ≤ 3.6 V	250		500		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	500		500		ns

Remark p: CSI number (p = 20)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V	16 MHz < f_{MCK}	8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
SIp setup time (to SCKp↑) **Note 1**	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) **Note 2**	t_{KSI2}	1.8 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output **Note 3**	t_{KSO2}	2.7 V ≤ V_{DD} ≤ 3.6 V	C = 30 pF **Note 4**		2/f_{MCK} + 44		2/f_{MCK} + 110	ns
		2.4 V ≤ V_{DD} ≤ 3.6 V			2/f_{MCK} + 75		2/f_{MCK} + 110	ns
		1.8 V ≤ V_{DD} ≤ 3.6 V			2/f_{MCK} + 100		2/f_{MCK} + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

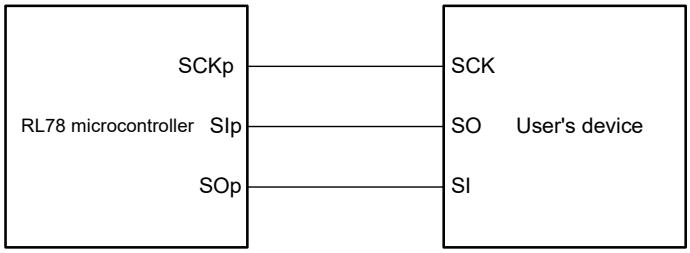
Note 4. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 10, 21, 30), m: Unit number (m = 0, 1), n: Channel number (n = 1, 2), g: PIM and POM number (g = 0, 14)

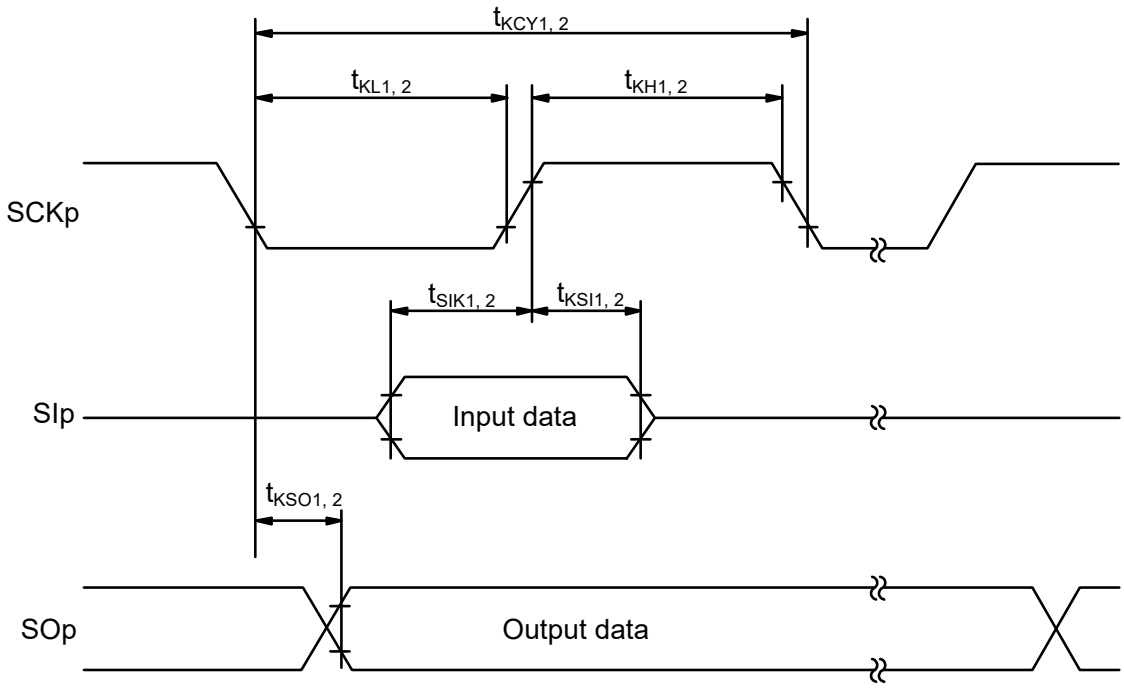
Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 02, 11, 12))

CSI mode connection diagram (during communication at same potential)

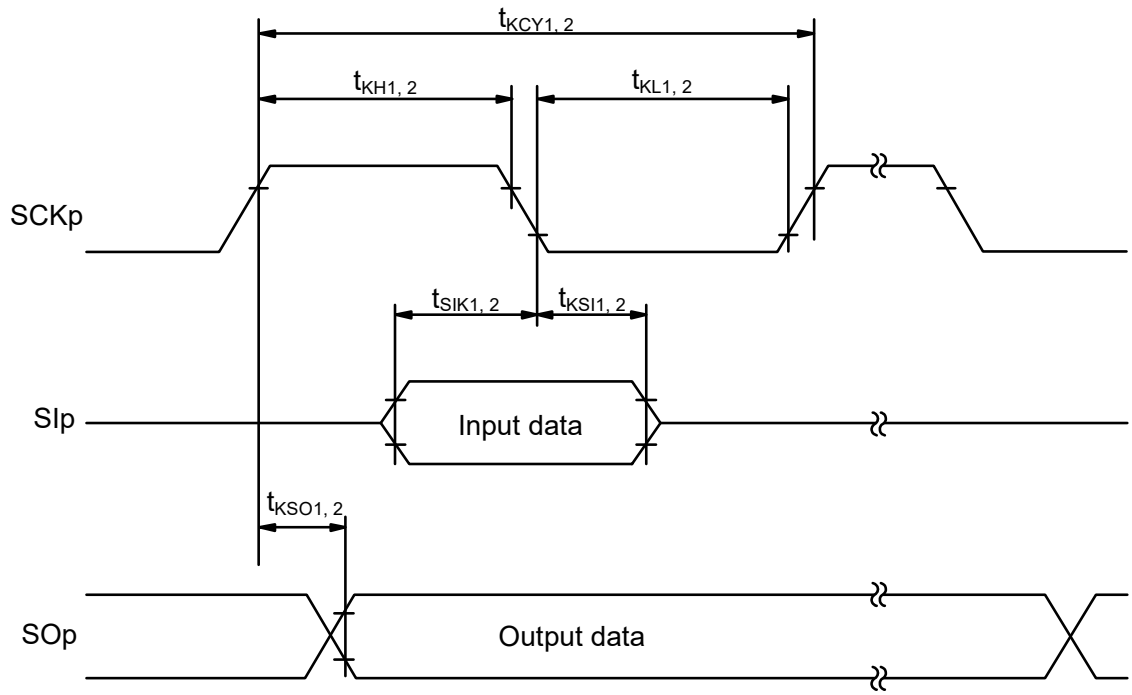


Remark p: CSI number (p = 10, 21, 30)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 10, 21, 30)
Remark 2. m: Unit number, n: Channel number (mn = 02, 11, 12)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 2**		5.3		1.3	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.8 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 **Note 1**		f_{MCK}/6 **Note 1**	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 2**		5.3		1.3	Mbps

Note 1. Use it with V_{DD} ≥ V_b.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 1, 3), g: PIM and POM number (g = 0, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 02, 03, 12, 13))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 **Note 2**		1.2 **Note 2**	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 3, 4**		**Notes 3, 4**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 **Note 5**		0.43 **Note 5**	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. Use it with $V_{DD} \geq V_b$.

Note 4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ V_{DD} < 3.3 V and 1.8 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

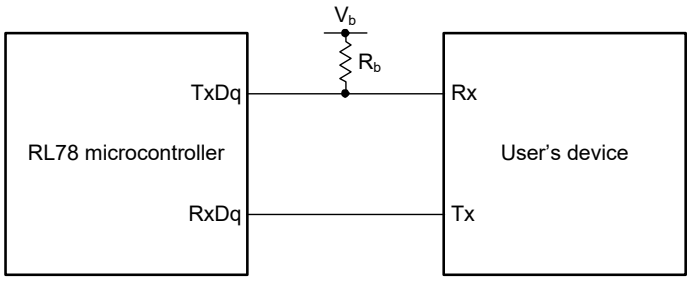
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

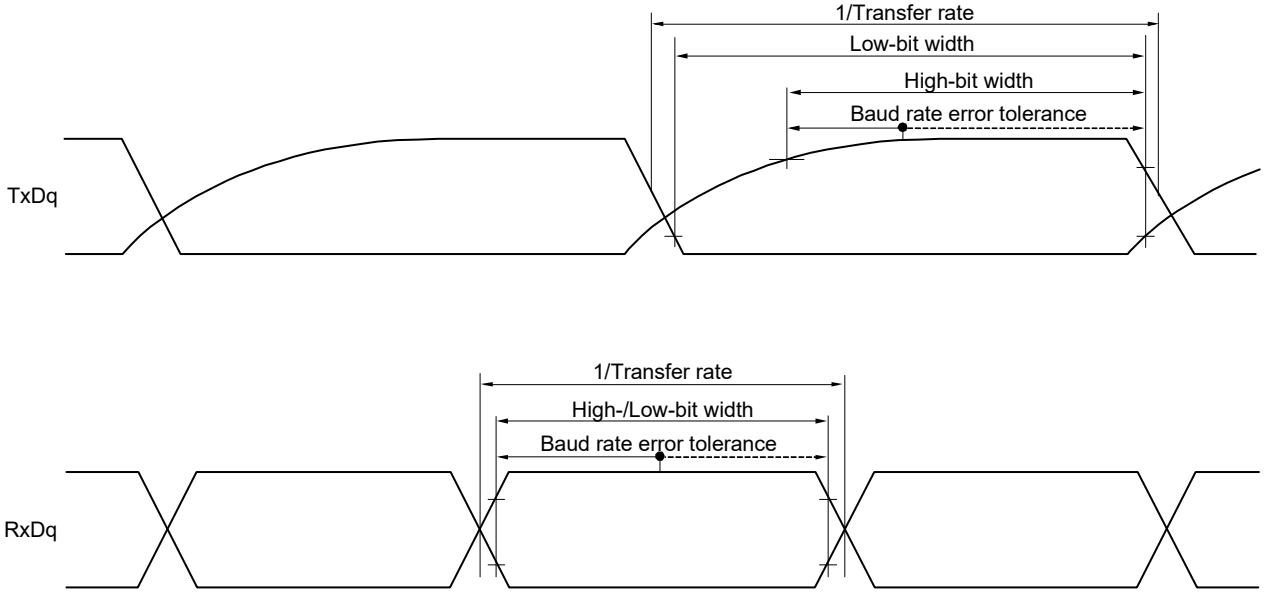
Note 5. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.
(Caution and Remarks are listed on the next page.)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 1, 3), g: PIM and POM number (g = 0, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 02, 03, 12, 13))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/3)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		ns
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns

Note Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) **Note 1**	t_{SIK1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 30 pF, R_b = 5.5 kΩ	479		479		ns
SIp hold time (from SCKp↑) **Note 1**	t_{KSI1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 30 pF, R_b = 5.5 kΩ	19		19		ns
Delay time from SCKp↓ to SOp output **Note 1**	t_{KSO1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 30 pF, R_b = 5.5 kΩ		483		483	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (3/3)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	110		110		ns
SIp hold time (from SCKp↓) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t_{KSO1}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		25		25	ns

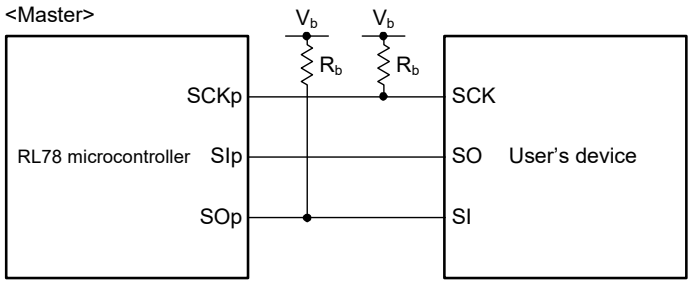
Note 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

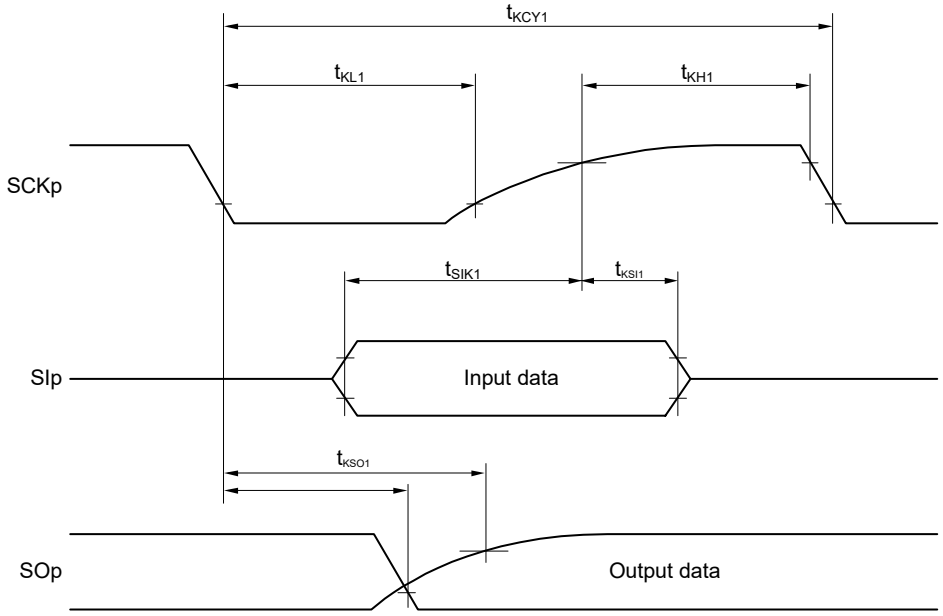


Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

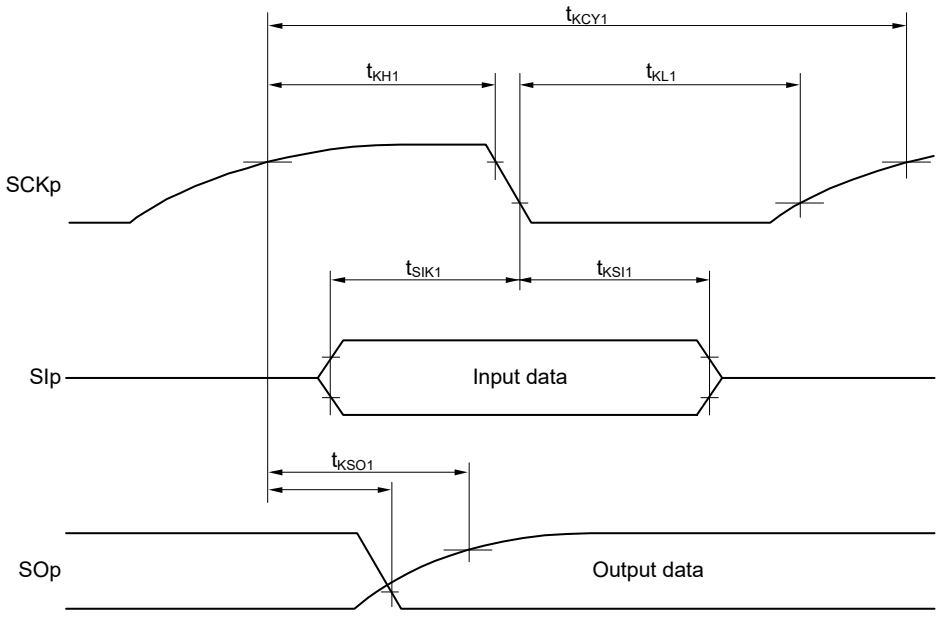
Remark 2. p: CSI number (p = 10, 30), m: Unit number (m = 0, 1), n: Channel number (n = 2), g: PIM and POM number (g = 0, 14)

Remark 3. CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 10, 30), m: Unit number (m = 0, 1), n: Channel number (n = 2),
g: PIM and POM number (g = 0, 14)

Remark 2. CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 1**	24 MHz < f_{MCK}	48/f_{MCK}		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 1**		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
SIp setup time (to SCKp↑) **Note 2**	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 1**		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) **Note 3**	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output **Note 4**	t_{KSO2}	2.7 V ≤ V_{DD} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.8 V ≤ V_b ≤ 2.0 V **Note 1**, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Note 1. Use it with V_{DD} ≥ V_b.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

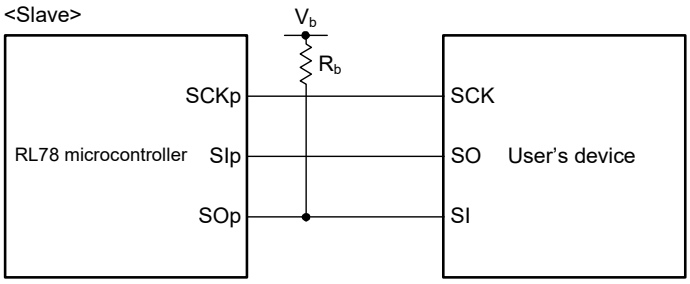
Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



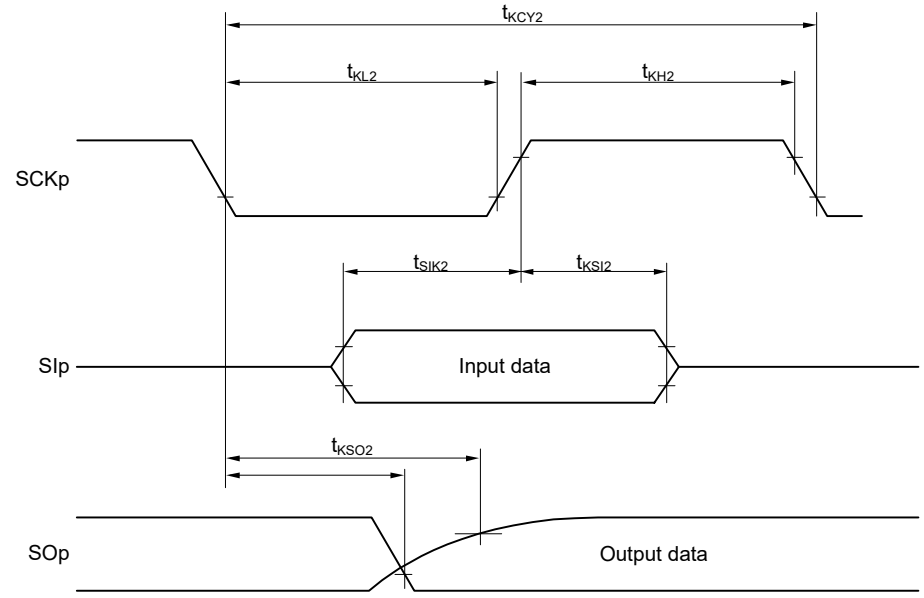
Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance,
V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 10, 30), m: Unit number (m = 0, 1), n: Channel number (n = 2),
g: PIM and POM number (g = 0, 14)

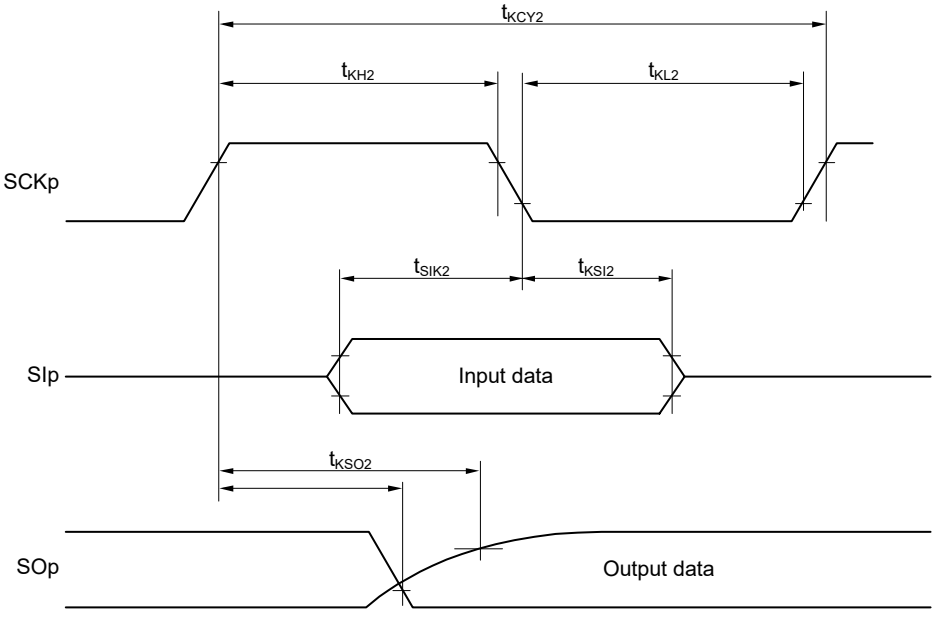
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 02, 12))

Remark 4. CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 10, 30), m: Unit number (m = 0, 1), n: Channel number (n = 2),
g: PIM and POM number (g = 0, 14)

Remark 2. CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	100	0	100	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	0	100	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		250		250		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		250		250		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	3.45	0	3.45	μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0	3.45	0	3.45	μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
Hold time **Note 1**	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		100		100		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		100		100		ns
Data hold time (transmission) **Note 2**	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

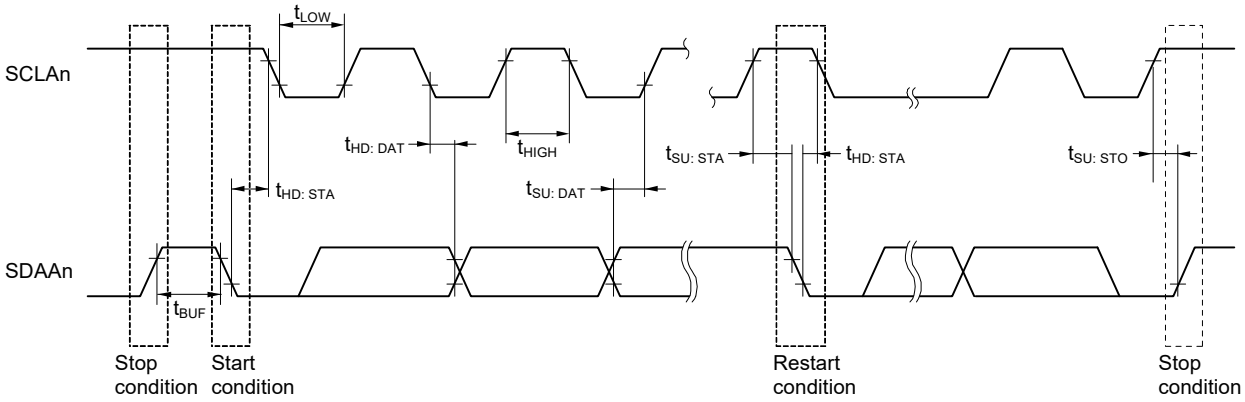
Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	1000	—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		μs
Hold time **Note 1**	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.5		—		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		50		—		ns
Data hold time (transmission) **Note 2**	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	0.45	—		μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.5		—		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = AVREFP Reference voltage (–) = AVREFM	Reference voltage (+) = VDD Reference voltage (–) = VSS
ANI0 to ANI2, ANI13, ANI14, ANI19	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (2)**.

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0 to ANI2, ANI13, ANI14, ANI19

(TA = –40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, 1.8 V ≤ AVREFP ≤ VDD ≤ 3.6 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (–) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error **Note 1**	AINL	10-bit resolution AVREFP = VDD **Notes 3, 4**	1.8 V ≤ AVREFP ≤ 3.6 V		1.2	±5.0	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI0 to ANI2, ANI13, ANI14, ANI19	2.7 V ≤ VDD ≤ 3.6 V	3.1875		39	μs
			1.8 V ≤ VDD ≤ 3.6 V	17		39	μs
Zero-scale error **Notes 1, 2**	EZS	10-bit resolution AVREFP = VDD **Notes 3, 4**	1.8 V ≤ AVREFP ≤ 3.6 V			±0.35	% FSR
Full-scale error **Notes 1, 2**	EFS	10-bit resolution AVREFP = VDD **Notes 3, 4**	1.8 V ≤ AVREFP ≤ 3.6 V			±0.35	% FSR
Integral linearity error **Note 1**	ILE	10-bit resolution AVREFP = VDD **Notes 3, 4**	1.8 V ≤ AVREFP ≤ 3.6 V			±3.5	LSB
Differential linearity error **Note 1**	DLE	10-bit resolution AVREFP = VDD **Notes 3, 4**	1.8 V ≤ AVREFP ≤ 3.6 V			±2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI2, ANI13, ANI14, ANI19		0		AVREFP	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.05% FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.20% FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.

(2) When reference voltage (+) = VDD (ADREFP0 = 0), reference voltage (–) = VSS (ADREFM = 0), target pin: ANI0 to ANI2, ANI13, ANI14, ANI19

(TA = –40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V, Reference voltage (+) = VDD, Reference voltage (–) = VSS)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ VDD ≤ 3.6 V		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI0 to ANI2, ANI13, ANI14, ANI19	2.7 V ≤ VDD ≤ 3.6 V	3.1875		39	μs
			1.8 V ≤ VDD ≤ 3.6 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	1.8 V ≤ VDD ≤ 3.6 V			±0.60	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	1.8 V ≤ VDD ≤ 3.6 V			±0.60	% FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ VDD ≤ 3.6 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ VDD ≤ 3.6 V			±2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI2, ANI13, ANI14, ANI19		0		VDD	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

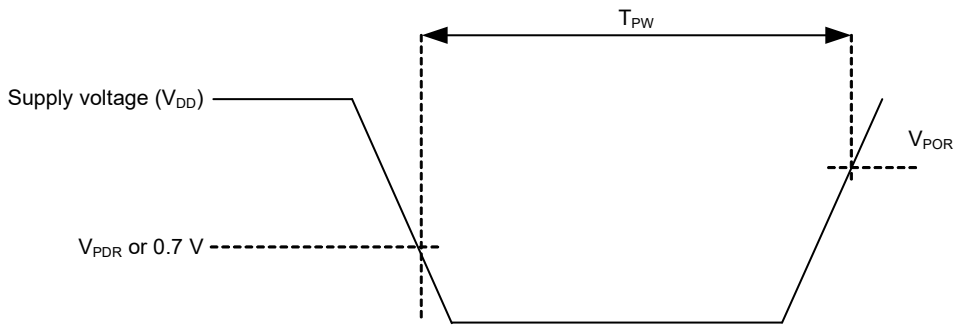
2.6.2 POR characteristics

(TA = –40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VPOR	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	VPDR	Voltage threshold on VDD falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	TPW		300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the voltage detection function or external reset pin before the voltage falls below the operating voltage range shown in **2.4 AC Characteristics**.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock (fMAIN) is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.3 LVD characteristics

(1) Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD2}	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		V_{LVD3}	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		V_{LVD4}	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		V_{LVD5}	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		V_{LVD6}	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		V_{LVD7}	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		V_{LVD8}	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		V_{LVD9}	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		V_{LVD10}	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		V_{LVD11}	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

(2) Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Voltage detection threshold	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V

2.6.4 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RF Transceiver Characteristics

2.7.1 Recommended operating conditions

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage		1.8	3.0	3.6	V
Operating ambient temperature		–40		85	°C
XIN frequency			48		MHz
Operating frequency		863		928	MHz
Channel interval		12.5/200/400/600			kHz
Data rate	2FSK/GFSK	10/20/40/50/100/150/200/300			kbps
	4FSK/GFSK	200/400			kbps
Modulation index	2FSK/GFSK	0.5/1.0			—
	4FSK/GFSK		0.33		—

2.7.2 XIN Frequency Deviation

2.7.2.1 Compatible with IEEE802.15.4g

XIN frequency accuracy is required according to the table below to satisfy the IEEE802.15.4g standard.

Frequency band [MHz]	Maximum frequency [MHz]	Symbol rate [ksymbol/s]	Variable index	MIN.	TYP.	MAX.	Unit	IEEE standard
863	870	50	1	–31.6	—	31.6	ppm	31.6
	870	100	1	–50.0	—	50.0	ppm	50.0
	870	100	0.33	–20.9	—	20.9	ppm	20.9
896	901	10	0.5	–3.1	—	3.1	ppm	3.1
	901	20	0.5	–6.1	—	6.1	ppm	6.1
	901	40	0.5	–12.2	—	12.2	ppm	12.2
901	902	10	0.5	–3.1	—	3.1	ppm	3.1
	902	20	0.5	–6.1	—	6.1	ppm	6.1
	902	40	0.5	–12.2	—	12.2	ppm	12.2
915	928	50	1	–29.6	—	29.6	ppm	29.6
	928	150	0.5	–44.4	—	44.4	ppm	44.4
	928	200	0.5	–50.0	—	50.0	ppm	50.0
917	923.5	50	1	–29.8	—	29.8	ppm	29.8
	923.5	150	0.5	–44.6	—	44.6	ppm	44.6
	923.5	200	0.5	–50.0	—	50.0	ppm	50.0
920	928	50	1	–29.6	—	29.6	ppm	29.6
	928	100	1	–50.0	—	50.0	ppm	50.0
	928	200	1	–50.0	—	50.0	ppm	50.0
	928	200	0.33	–39.1	—	39.1	ppm	39.1

2.7.2.2 Compatible with ARIB Standard

XIN frequency accuracy is required according to the table below to satisfy the ARIB standard.

Frequency band [MHz]	Maximum frequency [MHz]	Symbol rate [ksymbols/s]	Variable index	MIN.	TYP.	MAX.	Unit
920	928	50	1	–20	—	+20	ppm
	928	100	1	–20	—	+20	ppm
	928	200	1	–20	—	+20	ppm
	928	200	0.33	–20	—	+20	ppm

2.7.3 DC characteristics

(T_A = 25°C, V_{DDRF} =3.0 V, V_{SSRF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output current	I_{OHRF}	GPIO0 to GPIO4 INTOUT	1.8V ≤ V_{DDRF} ≤ 3.6 V		–2.0		mA
Low-level output current	I_{OLRF}	GPIO0 to GPIO4 INTOUT	1.8V ≤ V_{DDRF} ≤ 3.6 V		2.0		mA
High-level input voltage	V_{IHRF}	STANDBY, GPIO0 to GPIO4		0.85 V_{DDRF}		V_{DDRF}	V
Low-level input voltage	V_{ILRF}	STANDBY, GPIO0 to GPIO4, MODE1, MODE2		0		0.1 V_{DDRF}	V
High-level output voltage	V_{OHRF}	I_{OH} = –2.0 mA	GPIO0 to GPIO4, INTOUT	V_{DDRF} – 0.3			V
Low-level output voltage	V_{OLRF}	I_{OL} = 2.0 mA	GPIO0 to GPIO4, INTOUT			0.3	V
High-level input leak current	I_{LIHRF}	V_I = V_{DDRF}	STANDBY, GPIO0 to GPIO4			10	μA
Low-level input leak current	I_{LILRF}	V_I = V_{SSRF}	STANDBY, GPIO0 to GPIO4, MODE1, MODE2			–10	μA

2.7.4 Power supply current

(T_A = 25°C, V_{DDRF} =3.0 V, V_{SSRF} = 0 V)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Transmission current (100 kbps, 2GFSK)	+14.5 dBm		53		mA
	+13 dBm		36		
	+10 dBm		21		
Reception current (100 kbps, 2GFSK)	During reception operation RFIP –95 dBm, CW		6.9		mA
	Signal reception standby RFIP none		6.3		
SLEEP mode			0.1		μA
IDLE mode			1.3		mA

2.7.5 Transceiver reception characteristics

(T_A = 25°C, V_{DDRF} =3.0 V, V_{SSRF} = 0 V) (1/2)

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Reception sensitivity		2GFSK, BT = 0.5, BER < 0.1%, 10 kbps, m = 0.5	—	–114	–109	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 20 kbps, m = 0.5	—	–111	–106	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 40 kbps, m = 0.5	—	–108	–103	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 50 kbps, m = 1	—	–107	–102	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 100 kbps, m = 0.5	—	–104	–99	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 100 kbps, m = 1	—	–105	–100	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 150 kbps, m = 0.5	—	–102	–97	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 200 kbps, m = 0.5	—	–101	–96	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 200 kbps, m = 1	—	–102	–97	dBm
		2GFSK, BT = 0.5, BER < 0.1%, 300 kbps, m = 0.5	—	–97	–92	dBm
		4GFSK, BT = 0.5, BER < 0.1%, 200 kbps, m = 0.33	—	–102	–97	dBm
		4GFSK, BT = 0.5, BER < 0.1%, 400 kbps, m = 0.33	—	–100	–95	dBm
Maximum input level		2GFSK	0	12	—	dBm
Spurious radiation		1 GHz or lower	—	—	–57	dBm
		1 GHz or higher			–47	dBm
ED	Input range	2GFSK, BT = 0.5, 100 kbps, m = 1	–105		–5	dBm
	Total accuracy		–6		6	dB
RSSI	Input range	2GFSK, BT = 0.5, 100 kbps, m = 1	–100	—	–5	dBm
	Total accuracy		–6	—	6	dB
	Relative accuracy		–3	—	3	dB
Adjacent CH suppression ratio	±200 kHz (50 kbps, m = 1)	2GFSK, BT = 0.5, Desired signal 3 dB above the input sensitivity level, CW interferer, BER < 0.1%	—	35	—	dB
	±400 kHz (100 kbps, m = 1)		—	40	—	dB
Next-adjacent CH suppression ratio	±400 kHz (50 kbps, m = 1)	2GFSK, BT = 0.5, Desired signal 3 dB above the input sensitivity level, CW interferer, BER < 0.1%	—	45	—	dB
	±800 kHz (100 kbps, m = 1)		—	50	—	dB

(T_A = 25°C, V_{DDRF} =3.0 V, V_{SSRF} = 0 V) (2/2)

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Suppression ratio	±2 MHz	Desired signal 3 dB above the input sensitivity level, CW interferer, BER < 0.1%	—	48	—	dB
	±10 MHz		—	60	—	dB
	±60 MHz		—	60	—	dB
Image suppression ratio		Desired signal 3 dB above the input sensitivity level, CW interferer, -2* if frequency offset	—	25	—	dB

2.7.6 Transceiver transmission characteristics

(T_A = 25°C, V_{DDRF} =3.0 V, V_{SSRF} = 0 V)

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Maximum transmission output power		3.6 V ≥ V_{DDRF} > 2.4 V	14.5	15.3	—	dBm
		2.4 V ≥ V_{DDRF} ≥ 1.8 V	—	13.0	—	dBm
Minimum transmission output power			—	–14.0	—	dBm
Variable step size		Within 6 dB from maximum output power (3.6 V ≥ V_{DDRF} > 2.4 V).	—	0.5	—	dB
Transmission output power variation (Power supply voltage variation, temperature variation)		3.6 V ≥ V_{DDRF} ≥ 1.8 V –40 to 85°C	–1.5	—	1.5	dB
High frequency	2nd order harmonics	At +13 dBm output	—	—	–33.0	dBm
		At +14.5 dBm output	—	—	–31.5	dBm
	3rd order harmonics	At +13 dBm output	—	—	–33.0	dBm
		At +14.5 dBm output	—	—	–31.5	dBm

Caution Variable step size and variable range may vary depending on the maximum transmission output level setting.

<R> **Remark** For the characteristics of the RF transceiver, see the following application notes.
Electrical Characteristics of 920-MHz-Band RF Transceiver (R01AN3752)
Electrical Characteristics of 860-MHz-Band RF Transceiver (R01AN4027)
Electrical Characteristics of 915-MHz-Band RF Transceiver (FCC Part 15.247) (R01AN4557)

2.7.7 IEEE802.15.4g frequency/data rate table

Frequency band identifier	PHY	Frequency band (MHz)	Operating mode	Modulation	Data rate (kbps)	Symbol rate (ksps)	Modulation index	Channel spacing (kHz)	Total number of channels	Channel 0 frequency (MHz)
4	863 MHz (Europe)	863 to 870	#1	2FSK/2GFSK	50	50	1	200	34	863.125
			#2		100	100		400	17	863.225
			#3	4FSK/4GFSK	200	100	0.33			
5	896 MHz (US)	896 to 901	#1	2FSK/2GFSK	10	10	0.5	25	399	896.0125
			#2		20	20		50	397	896.025
			#3		40	40		100	393	896.05
6	901 MHz (US)	901 to 902	#1	2FSK/2GFSK	10	10	0.5	25	79	901.0125
			#2		20	20		50	77	901.025
			#3		40	40		100	73	901.05
7	915 MHz (US)	902 to 928	#1	2FSK/2GFSK	50	50	1	200	129	902.2
			#2		150	150	0.5	400	64	902.4
			#3		200	200				
8	917 MHz (Korea)	917 to 923.5	#1	2FSK/2GFSK	50	50	1	200	32	917.1
			#2		150	150	0.5	400	16	917.3
			#3		200	200				
9	920 MHz (Japan)	920 to 928	#1	2FSK/2GFSK	50	50	1	200	38	920.6
			#2		100	100		400	18	920.9
			#3		200	200		600	12	920.8
			#4	4FSK/4GFSK	400	200	0.33			

<R> **Caution Refer to the latest version of the application note Recommended Settings of Registers (R01AN3410) regarding settings when this product is to be used.**

2.7.8 AC Characteristics

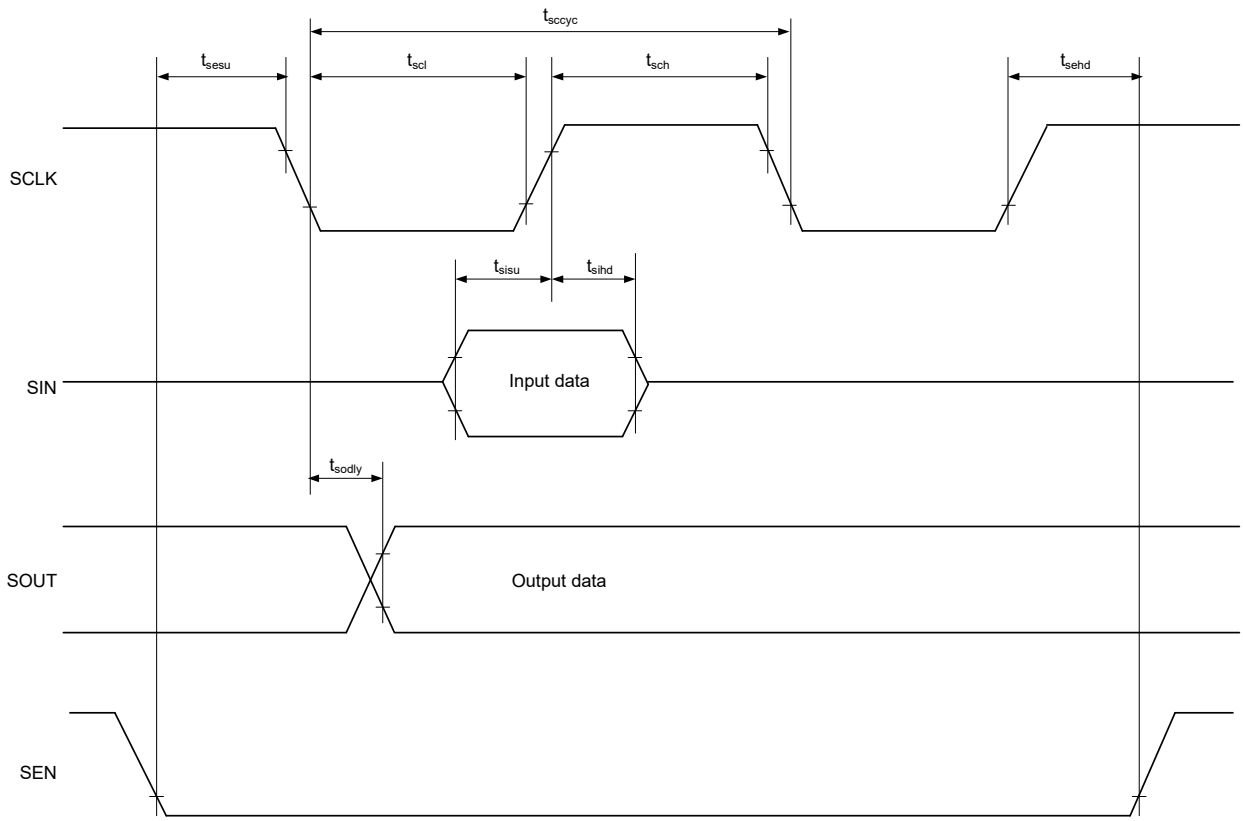
(T_A = –40°C, to +85°C, 2.4 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKL cycle time	tsccyc		250			ns
SEN setup time	tsesu		200			ns
SEN hold time	tsehd		200			ns

(T_A = –40°C, to +85°C, 1.8 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKL cycle time	tsccyc		500			ns
SEN setup time	tsesu		400			ns
SEN hold time	tsehd		400			ns

Figure 2 - 1 Data I/O timing



(T_A = –40°C, to +85°C, 1.8 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
STANDBYlow-level width	tstbyl		10			µs
OSCDRVSEL setup time (From STANDBY↑)	todssu	Crystal resonator	500			µs
DON setup time (From OSCDRVSEL↑)	tdonsu	Crystal resonator	50			µs
RFRESETB setup time (From DON↑)	trfrstsu	Crystal resonator	450			µs
RFRESETBsetup time (From STANDBY↑)	trfrstsu2	External clock input	450			µs

Figure 2 - 2 Timing using crystal resonator

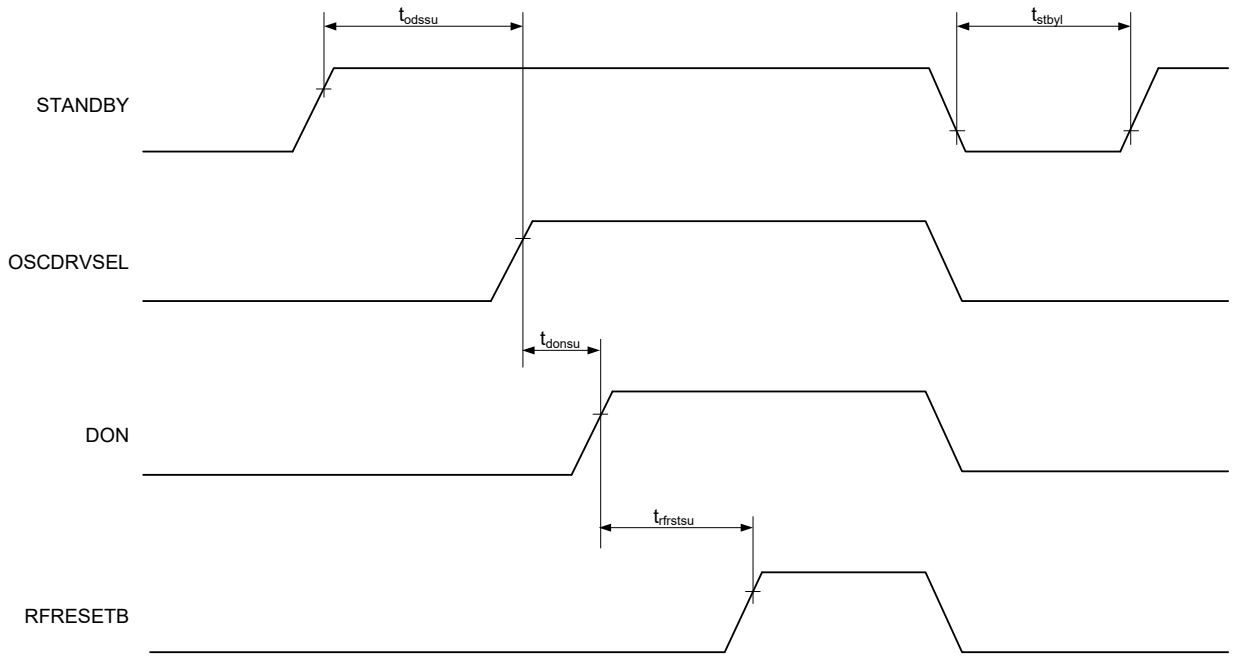
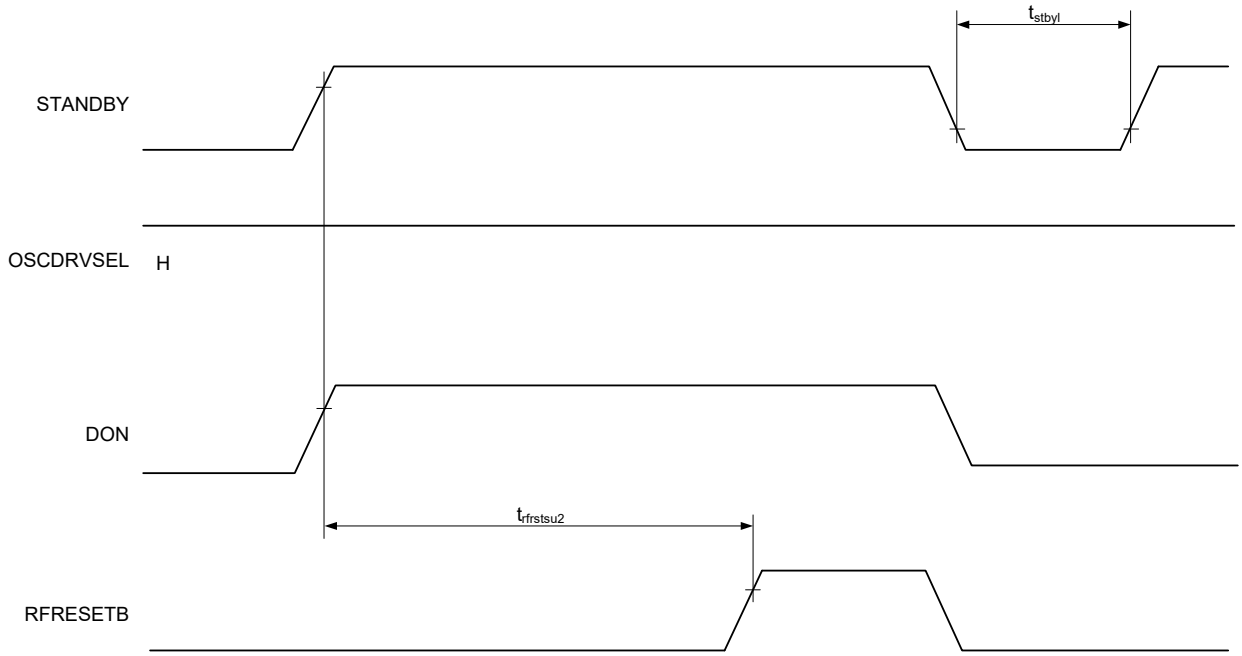


Figure 2 - 3 Timing input external clock

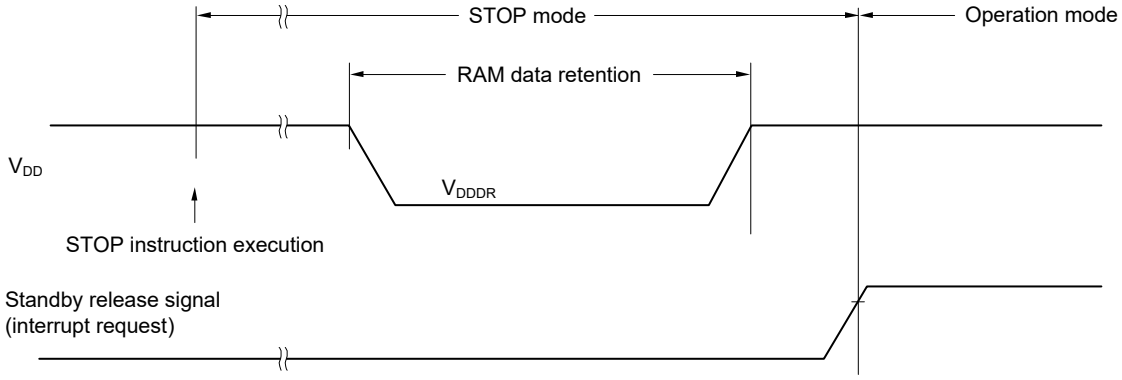


2.8 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	**V_{DDDR}**		1.46 **Note**		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.9 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 3.6 V		1		32	MHz
Number of code flash rewrites **Notes 1, 2, 3**	C_{erwr}	Retained for 20 years	T_A = 85°C	1,000			Times
Number of data flash rewrites **Notes 1, 2, 3**		Retained for 1 year	T_A = 25°C		1,000,000		
		Retained for 5 years	T_A = 85°C	100,000			
		Retained for 20 years	T_A = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.10 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 1.8 V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

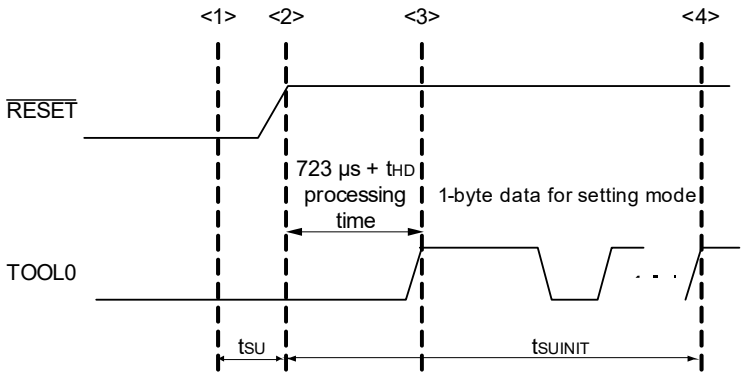
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.11 Timing for Switching Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

<R>



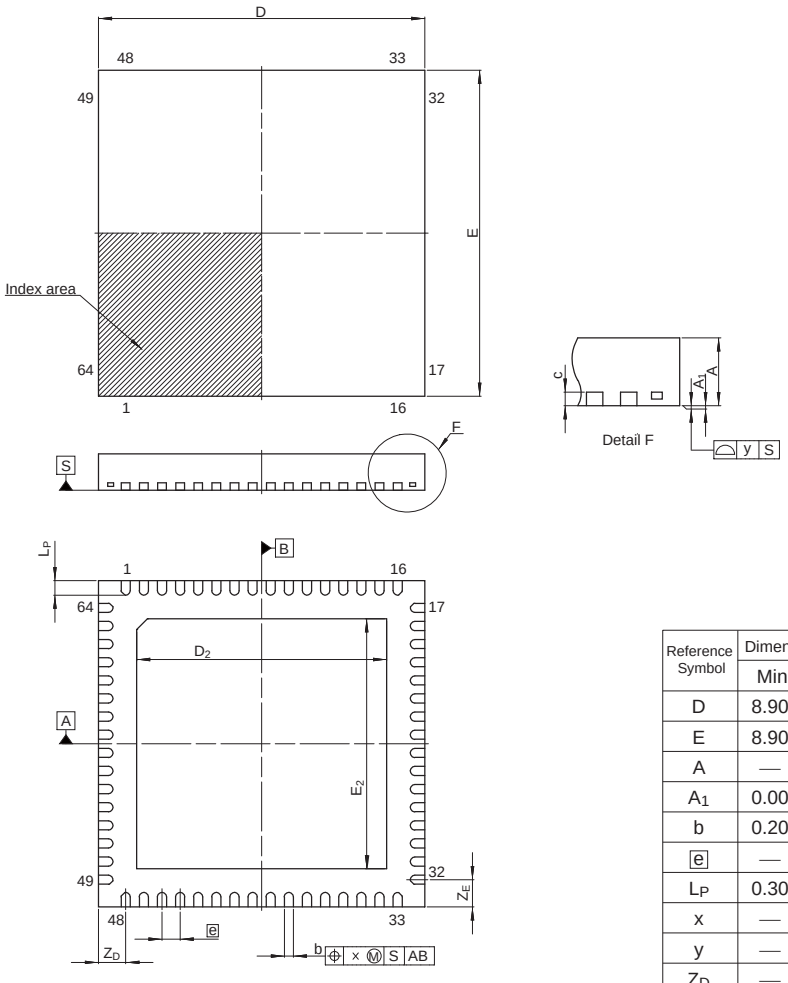
<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> The baud rate setting by UART reception is completed.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends.
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end. (excluding the processing time of the firmware to control the flash memory)

3. PACKAGE DRAWING

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HVQFN64-9x9-0.50	PVQN0064KC-A	—	0.21

Unit: mm



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	8.90	9.00	9.10
E	8.90	9.00	9.10
A	—	—	1.00
A_1	0.00	—	—
b	0.20	0.25	0.30
e	—	0.50	—
L_P	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c	—	0.20	—
D_2	—	6.90	—
E_2	—	6.90	—

REVISION HISTORY	RL78/G1H Datasheet

Rev.	Date	Description	
		Page	Summary
1.30	Dec 28, 2018	p.1	Modification of description in 1.1 Features
		p.7	Modification of 1.5 Block Diagram
		p.14	Deletion of note 4 in 2.3.1 Pin characteristics
		p.56	Addition of remark in 2.7.6 Transceiver transmission characteristics
		p.57	Addition of caution in 2.7.7 IEEE802.15.4g frequency/data rate table
		p.62	Modification of figure in 2.11 Timing for Switching Flash Memory Programming Modes
1.20	Dec 22, 2016	p.5	Change of Caution in 1.3 Pin Configuration (Top View)
		p.8	Change of 1.6 Outline of Functions
		pp.10 to 60	Change expression of conditions
		p.11	Addition of item and Note 3 to 2.1 Absolute Maximum Ratings
		p.57	Change of 2.7.7 IEEE802.15.4g frequency/data rate table
1.10	May 11, 2016	-	Issuing revision in accordance with revised user's manual (no change of the contents)
1.00	Feb 24, 2016	p.1	Change of 1.1 Features
		p.4	Change of Table 1 - 1 Ordering Part Number List
		p.5	Change of 1.3 Pin Configuration (Top View)
		p.6	Change of description in 1.4 Pin Identification
		p.7	Change of 1.5 Block Diagram
		p.8,9	Change of description in 1.6 Outline of Functions
		p.10	Change of the title and description in 2. ELECTRICAL SPECIFICATIONS
		p.11	Change of description in 2.1 Absolute Maximum Ratings
		p.13	Change of 2.2.2 On-chip oscillator characteristics
		p.14, 15, 18	Change of description in 2.3.1 Pin characteristics
		p.19, 21, 23	Change of 2.3.2 Supply current characteristics
		p.31	Change of remark in 2.5.1 (2) During communication at same potential (CSI mode) (master mode,SCKp... internal clock output)
		p.31	Deletion of remark 1 in 2.5.1 (3) uring communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supported only for CSI20)
		p.32	Change of remark 1 in 31.5.1 (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
		p.43	Change of remark 3 and 4 in CSI mode connection diagram (during communication at different potential)
		p.44	Change of remark 2 in Figure CSI mode serial transfer timing (slave mode) (during communication at different potential)(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
		p.52	Change of description in 2.7.1 Recommended operating conditions
		p.52	Change and addition of description in 2.7.2.1 Compatible with IEEE802.15.4g
		p.53	Addition of 2.7.2.2 Compatible with ARB Standard
		p.54	Change of 2.7.3 DC characteristics
		p.54	Change of 2.7.4 Power supply current
		p.55, 56	Change of 2.7.5 Transceiver reception characteristics
		p.56	Change of 2.7.6 Transceiver transmission characteristics
		p.57	Change of 2.7.7 IEEE802.15.4g frequency/data rate table
		pp.58 to 60	Addition of 2.7.8 AC Characteristics
		p.61	Change of description in 2.8 RAM Data Retention Characteristics
0.50	Jul 31, 2015	—	First Edition issued

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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