RL78/G10

RENESAS MCU

True Low Power Platform (as low as 46 µA/MHz), 2.0 to 5.5V Operation,
1 to 4 Kbyte Flash for General Purpose Applications

R01DS0207EJ0321
Rev.3.21
Mar 22, 2024

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 2.0 to 5.5 V operation from a single supply
- Stop (RAM retained): 0.56 µA
- Operating: 46 µA /MHz

RL78-S1 Core
- Instruction execution: 78 % of instructions can be executed in 1 to 2 clock cycles
- CISC architecture (Harvard) with 3-stage pipeline
- Multiply: 8 x 8 to 16-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 2 clock cycle
- 1-wire on-chip debug function

Main Flash Memory
- Density: 1 to 4 Kbyte
- Flash memory rewritable voltage: 4.5 to 5.5 V

RAM
- 128 to 512 Byte size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 20 MHz with +/-2 % accuracy over voltage (2.0 to 5.5 V) and temperature (-20 to +85°C)
- Pre-configured settings: 20 MHz, 10 MHz, 5 MHz, 2.5 MHz, and 1.25 MHz

Reset and Supply Management
- Selectable power-on reset (SPOR) generator with 4 setting options

Multiple Communication Interfaces
- 1 x I^2C master
- 1 x I^2C multi-master (only for 16-pin product)
- 1 x UART (7-, 8-bit)
- Up to 2 x Simplified SPI (CSI Note) (7-, 8-bit)

Extended-Function Timers
- Multi-function 16-bit timers: Up to 4 channels
- Interval timer: 12-bit, 1 channel (only for 16-pin product)
- 15 kHz watchdog timer: 1 channel

Rich Analog
- ADC: Up to 7 channels, 10-bit resolution, 3.4 µs conversion time
- Supports 2.4 V
- Internal reference voltage (0.815 V (typ.)) (only for 16-pin product)
- Comparator: 1 channel (only for 16-pin product)

Safety Features
- Detects execution of illegal instruction
- Detects watchdog timer program loop

General Purpose I/O
- High-current (up to 20 mA per pin)
- Open-drain, internal pull-up support

External Interrupt
- External interrupt input: Up to 4
- Key interrupt input: 6

Operating Ambient Temperature
- Standard: -40 to +85°C

Package Type and Pin Count
- SSOP: 10 and 16 pin

Note Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

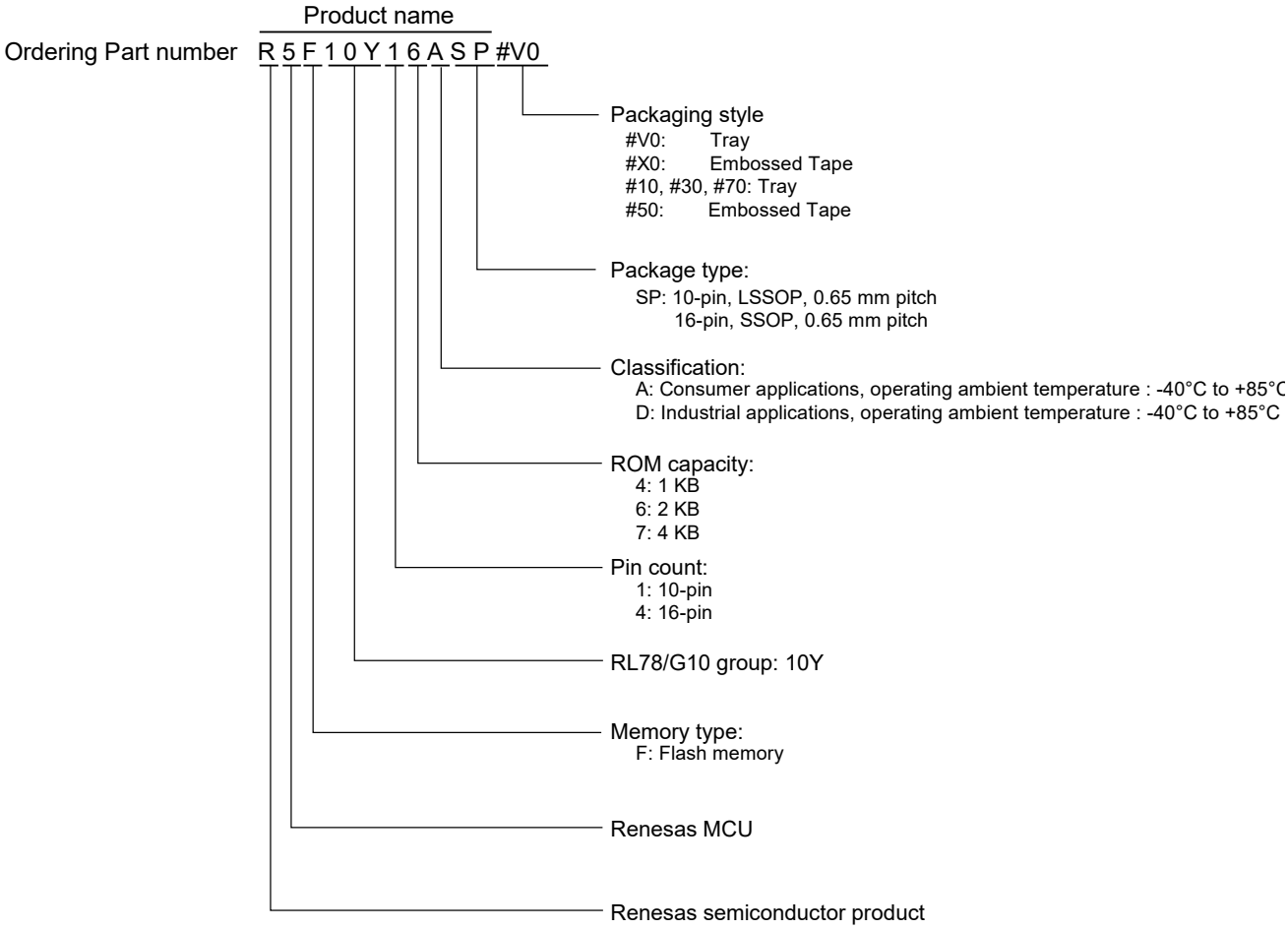
○ ROM, RAM capacities

Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	R5F10Y17	R5F10Y47
2 KB	256 B	R5F10Y16	R5F10Y46
1 KB	128 B	R5F10Y14	R5F10Y44

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Numbers

<R> **Figure 1-1. Part Number, Memory Size, and Package of RL78/G10**



<R> **Table 1-1. List of Ordering Part Numbers**

Pin count	Package	Fields of Application Note	Ordering Part Number		RENESAS Code
			Product Name	Packaging Specifications	
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)	A	R5F10Y14ASP, R5F10Y14ASP R5F10Y16ASP, R5F10Y16ASP	#V0,#X0,#10,#50,#70	PLSP0010JA-A
			R5F10Y17ASP, R5F10Y17ASP	#10,#30,#50,#70	
		D	R5F10Y14DSP, R5F10Y14DSP R5F10Y16DSP, R5F10Y16DSP R5F10Y17DSP, R5F10Y17DSP	#10,#30,#50,#70	
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)	A	R5F10Y44ASP, R5F10Y44ASP R5F10Y46ASP, R5F10Y46ASP R5F10Y47ASP, R5F10Y47ASP	#10,#30,#50,#70	PRSP0016JC-B
		D	R5F10Y44DSP, R5F10Y44DSP R5F10Y46DSP, R5F10Y46DSP R5F10Y47DSP, R5F10Y47DSP		

(**Notes** and **Caution** are listed on the next page.)

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G10**.

Caution The part number represents the number at the time of publication.
Be sure to review the latest part number through the target product page in the Renesas Electronics Corp.website.

1.3 Pin Configuration (Top View)

1.3.1 10-pin products

- 10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)

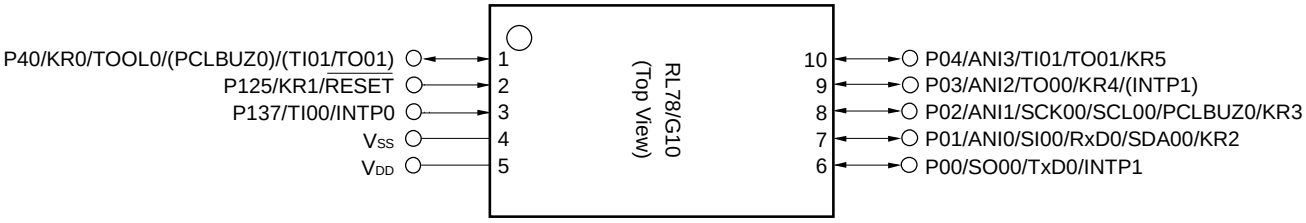


Table 1-2. Alternate Function of 10-pin products

Pin No.	I/O	Power supply, system clock, debug	Analog		HMI		Timer	Communication interface	
10LSSOP	Digital port		A/D converter	Comparator	Interrupt function	key interrupt function (KR)	Timer array unit	Serial array unit	Serial interface IICA
1	P40	TOOL0 (PCLBUZ0)				KR0	(TI01/TO01)		
2	P125	$\overline{\text{RESET}}$				KR1			
3	P137				INTP0		TI00		
4		V_{SS}							
5		V_{DD}							
6	P00				INTP1			SO00/TxD0	
7	P01		ANI0			KR2		SI00/RxD0/SDA00	
8	P02	PCLBUZ0	ANI1			KR3		SCK00/SCL00	
9	P03		ANI2		(INTP1)	KR4	TO00		
10	P04		ANI3			KR5	TI01/TO01		

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-6 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G10 User's Manual.

1.3.2 16-pin products

- **16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)**

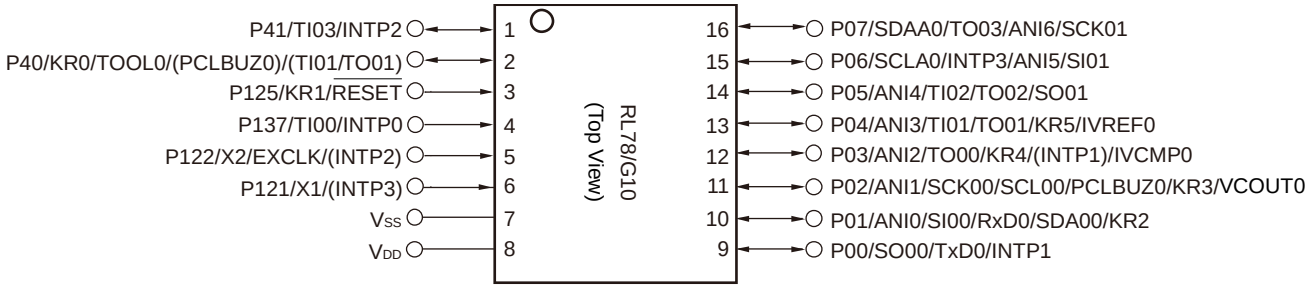


Table 1-3. Alternate Function of 16-pin products

Pin No.	I/O		Analog		HMI		Timer	Communication interface	
16SSOP	Digital port	Power supply, system clock, debug	A/D converter	Comparator	Interrupt function	Key interrupt function	Timer array unit	Serial array unit	Serial interface IICA
1	P41				INTP2		TI03		
2	P40	TOOL0 (PCLBUZ0)				KR0	(TI01/TO01)		
3	P125	$\overline{\text{RESET}}$				KR1			
4	P137				INTP0		TI00		
5	P122	X2 EXCLK			(INTP2)				
6	P121	X1			(INTP3)				
7		V_{SS}							
8		V_{DD}							
9	P00				INTP1			SO00/TxD0	
10	P01		ANI0			KR2		SI00/RxD0/SDA00	
11	P02	PCLBUZ0	ANI1	VCOUT0		KR3		SCK00/SCL00	
12	P03		ANI2	IVCMP0	(INTP1)	KR4	TO00		
13	P04		ANI3	IVREF0		KR5	TI01/TO01		
14	P05		ANI4				TI02/TO02	SO01	
15	P06		ANI5		INTP3			SI01	SCLA0
16	P07		ANI6				TO03	SCK01	SDAA0

Remarks 1. For pin identification, see **1.4 Pin Identification**.

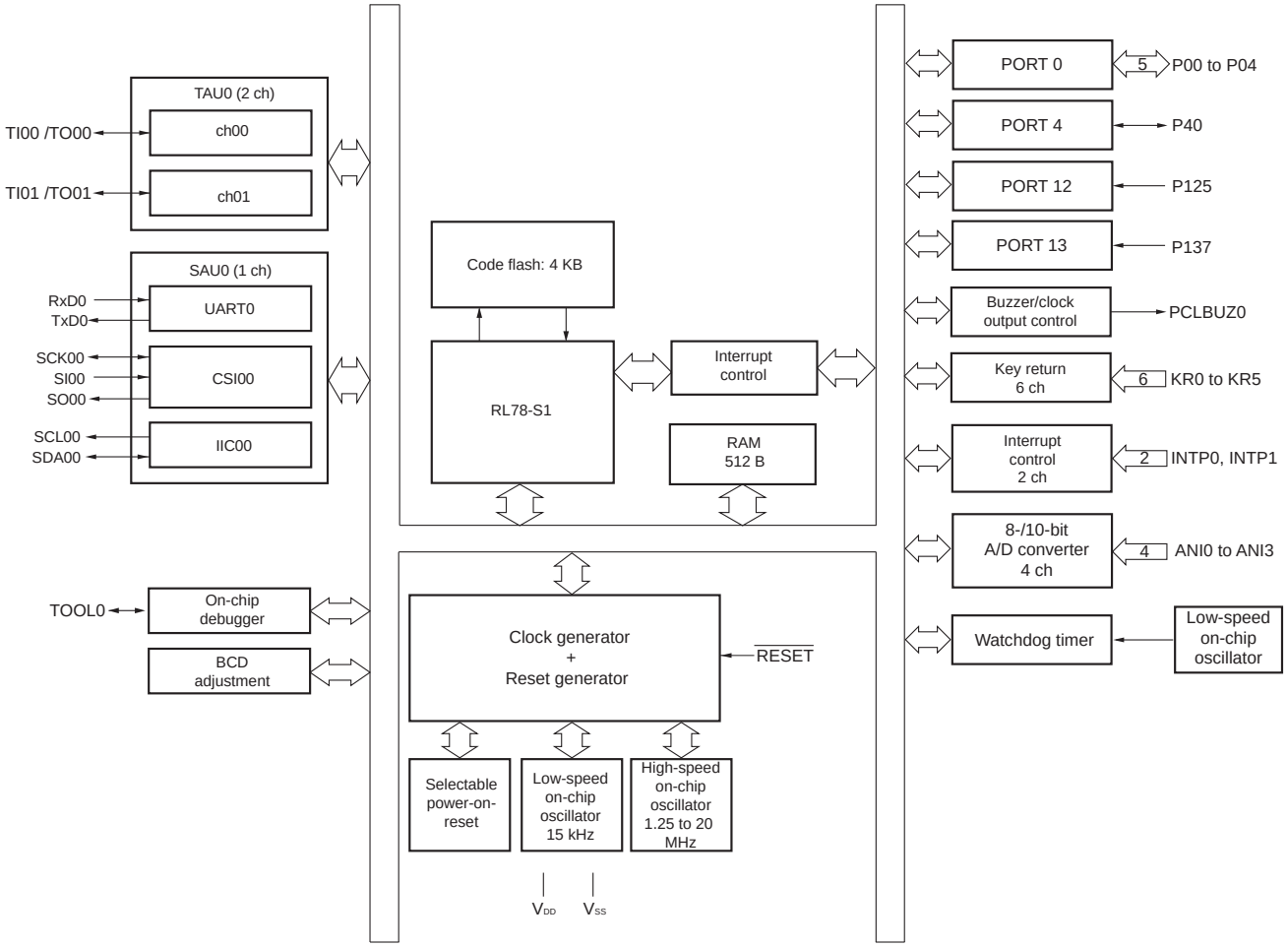
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-6 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G10 User's Manual.

1.4 Pin Identification

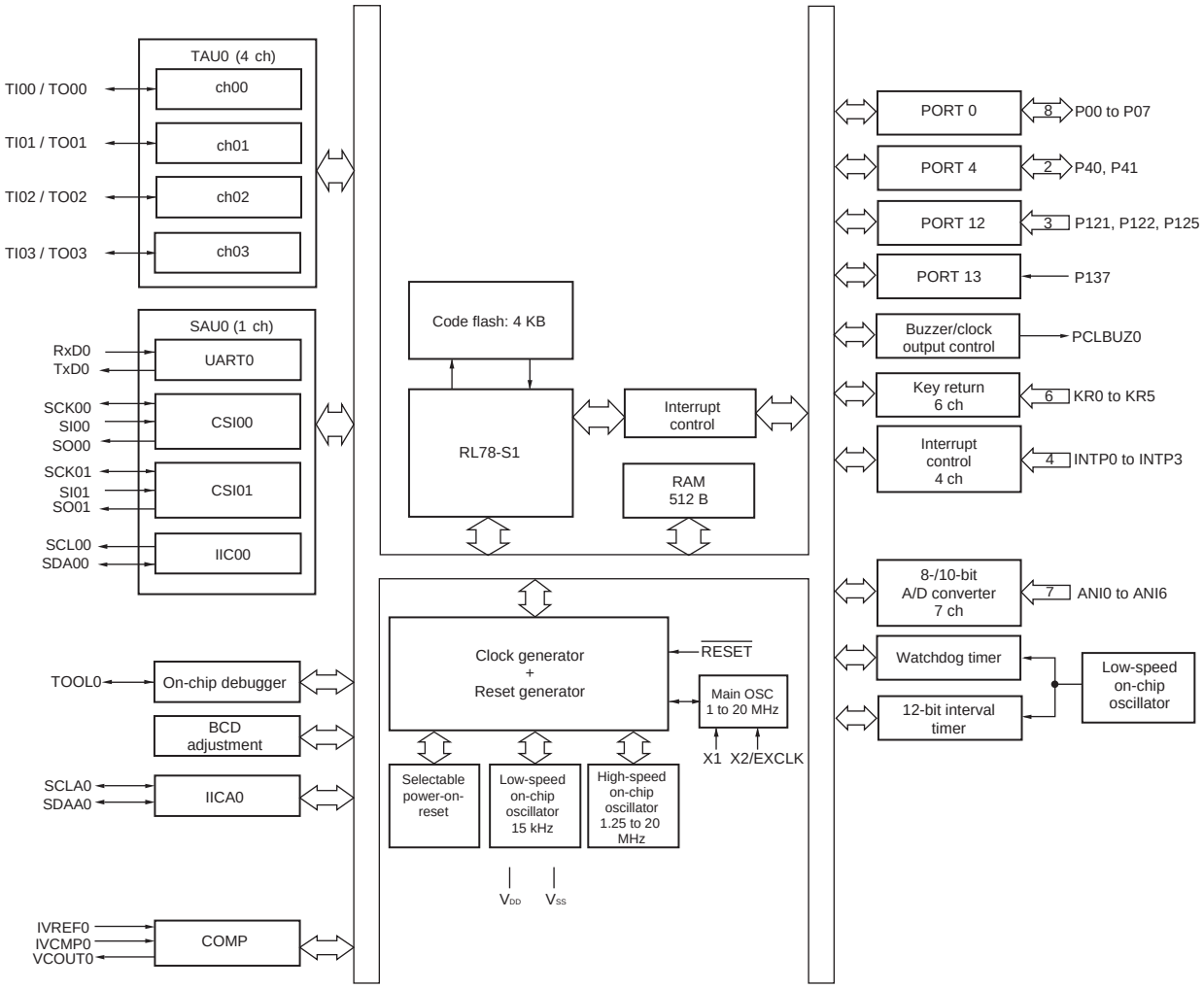
ANI0 to ANI6	: Analog Input
INTP0 to INTP3	: Interrupt Request From Peripheral
KR0 to KR5	: Key Return
P00 to P07	: Port 0
P40, P41	: Port 4
P121, P122, P125	: Port 12
P137	: Port 13
PCLBUZ0	: Programmable Clock Output/ Buzzer Output
EXCLK	: External Clock Input
X1, X2	: Crystal Oscillator (Main System Clock)
IVCMP0	: Comparator Input
VCOUT0	: Comparator Output
IVREF0	: Comparator Reference Input
$\overline{\text{RESET}}$	: Reset
RxD0	: Receive Data
SCK00, SCK01	: Serial Clock Input/Output
SCL00, SCLA0	: Serial Clock Output
SDA00, SDAA0	: Serial Data Input/Output
SI00, SI01	: Serial Data Input
SO00, SO01	: Serial Data Output
TI00 to TI03	: Timer Input
TO00 to TO03	: Timer Output
TOOL0	: Data Input/Output for Tool
TxD0	: Transmit Data
V_{DD}	: Power Supply
V_{SS}	: Ground

1.5 Block Diagram

1.5.1 10-pin products



1.5.2 16-pin products



1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

Item		10-pin			16-pin		
		R5F10Y14	R5F10Y16	R5F10Y17	R5F10Y44	R5F10Y46	R5F10Y47
Code flash memory		1 KB	2 KB	4 KB	1 KB	2 KB	4 KB
RAM		128 B	256 B	512 B	128 B	256 B	512 B
Main system clock	High-speed system clock	—			X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK): 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V 1 to 5 MHz: V_{DD} = 2.0 to 5.5 V Note 3		
	High-speed on-chip oscillator clock	• 1.25 to 20 MHz (V_{DD} = 2.7 to 5.5 V) • 1.25 to 5 MHz (V_{DD} = 2.0 to 5.5 V Note 3)					
Low-speed on-chip oscillator clock		15 kHz (TYP)					
General-purpose register		8-bit register × 8					
Minimum instruction execution time		0.05 μs (20 MHz operation)					
Instruction set		• Data transfer (8 bits) • Adder and subtractor/logical operation (8 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total	8			14		
	CMOS I/O	6 (N-ch open-drain output (V_{DD} tolerance): 2)			10 (N-ch open-drain output (V_{DD} tolerance): 4)		
	CMOS input	2			4		
Timer	16-bit timer	2 channels			4 channels		
	Watchdog timer	1 channel					
	12-bit interval timer	—			1 channel		
	Timer output	2 channels (PWM output: 1)			4 channels (PWM outputs: 3 Note 1)		
Clock output/buzzer output		1					
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)					
Comparator		—			1		
8-/10-bit resolution A/D converter		4 channels			7 channels		
Serial interface		[10-pin products] Simplified SPI (CSI): 1 channel/simplified I^2C: 1 channel/UART: 1 channel [16-pin products] Simplified SPI (CSI): 2 channels/simplified I^2C: 1 channel/UART: 1 channel					
	I^2C bus	—			1 channel		
Vectored interrupt sources	Internal	8			14		
	External	3			5		
Key interrupt		6					
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction execution Note 2 • Internal reset by data retention lower limit voltage					
Selectable power-on-reset circuit		• Detection voltage Rising edge (V_{SPOR}): 2.25 V/2.68 V/3.02 V/4.45 V (max.) Falling edge (V_{SPDR}): 2.20 V/2.62 V/2.96 V/4.37 V (max.)					

Item	10-pin			16-pin		
	R5F10Y14	R5F10Y16	R5F10Y17	R5F10Y44	R5F10Y46	R5F10Y47
On-chip debug function	Provided					
Power supply voltage	V_{DD} = 2.0 to 5.5 V Note 3					
Operating ambient temperature	T_A = - 40 to + 85 °C					

Notes 1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **6.9.4 Operation as multiple PWM output function** in the RL78/G10 User's Manual).

2. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.

2. ELECTRICAL SPECIFICATIONS

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions and 2.2.1 Functions for each product in the RL78/G10 User's Manual.

3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.

2.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to +6.5	V
Input Voltage	V_{I1}			−0.3 to V_{DD} + 0.3 Note	V
Output Voltage	V_{O1}			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins	P40, P41	−70	mA
			P00 to P07	−100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins	P40, P41	70	mA
			P00 to P07	100	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. The reference voltage is V_{SS}.

2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1		20	MHz
		2.0 V ≤ V_{DD} < 2.7 V	1		5	MHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G10 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation clock frequency [Notes 1, 2]	f_{IH}		1.25		20	MHz
High-speed on-chip oscillator oscillation clock frequency accuracy		T_A = -20 to +85°C	-2.0		+2.0	%
		T_A = -40 to -20°C	-3.0		+3.0	%
Low-speed on-chip oscillator oscillation clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator oscillation clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				-10.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-4.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			-3.0	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-60.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-12.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			-9.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-80.0	mA
Output current, low Note 4	I_{OL1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				20.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			6.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			1.2	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			12.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			2.4	mA
		Total of all pins (When duty ≤ 70% Note 3)				120.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. This is the output current value under conditions where the duty factor ≤ 70%.
The output current value when the duty factor > 70% can be calculated with the following expression (when changing the duty factor to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OH} = - 10.0 mA
  Total output current of pins = (- 10.0 × 0.7)/(80 × 0.01) ≅ - 8.7 mA
- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OL} = 10.0 mA
  Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Caution P00, P01, P06, and P07 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}			0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}			0		0.2 V_{DD}	V
Output voltage, high Note 1	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = -10 mA	V_{DD} - 1.5			V
			I_{OH} = -3.0 mA	V_{DD} - 0.7			V
		2.7 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = -2.0 mA	V_{DD} - 0.6			V
		2.0 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = -1.5 mA	V_{DD} - 0.5			V
Output voltage, low Note 2	V_{OL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 20 mA			1.3	V
			I_{OL} = 8.5 mA			0.7	V
		2.7 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 3.0 mA			0.6	V
			I_{OL} = 1.5 mA			0.4	V
		2.0 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 0.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	P00 to P07, P40, P41, P125, P137 V_I = V_{DD}				1	μA
	I_{LIH2}	P121, P122 (X1, X2, EXCLK) V_I = V_{DD}	In input port or external clock input			1	
			In resonator connection			10	
Input leakage current, low	I_{LIL1}	P00 to P07, P40, P41, P125, P137 V_I = V_{SS}				-1	μA
	I_{LIL2}	P121, P122 (X1, X2, EXCLK) V_I = V_{SS}	In input port or external clock input			-1	
			In resonator connection			-10	
On-chip pull-up resistance	R_U	V_I = V_{SS}		10	20	100	kΩ

Notes 1. The value under the condition which satisfies the high-level output current (I_{OH1}).

2. The value under the condition which satisfies the low-level output current (I_{OL1}).

Caution The maximum value of V_{IH} of P00, P01, P06, and P07 is V_{DD} even in N-ch open-drain mode. P00, P01, P06, and P07 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

2.3.2 Supply current characteristics

(1) Flash ROM: 1 and 2 KB of 10-pin products

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		0.91		mA
			Normal operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		1.57	2.04	
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		0.85	1.15	
	I_{DD2} Note 2	HALT mode		f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		350	820	µA
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		290	600	
	I_{DD3} Note 3	STOP mode		V_{DD} = 3.0 V			0.56	2.00	µA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Not including the current flowing into the watchdog timer.

Remarks 1. f_{IH}: High-speed on-chip oscillator clock frequency

2. Temperature condition of the typical value is T_A = 25°C

(2) Flash ROM: 4 KB of 10-pin products, and 16-pin products

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		0.92		mA
			Normal operation	f_{IH} = 20 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		1.59	2.14	
				f_{IH} = 5 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		0.87	1.20	
				f_{MX} = 20 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		1.43	1.93	
					Resonator connection		1.54	2.13	
				f_{MX} = 5 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		0.67	1.02	
					Resonator connection		0.72	1.12	
	I_{DD2} Note 2	HALT mode		f_{IH} = 20 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		360	900	µA
				f_{IH} = 5 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		310	660	
				f_{MX} = 20 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		200	700	
					Resonator connection		300	900	
				f_{MX} = 5 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		100	440	
					Resonator connection		150	540	
	I_{DD3} Note 3	STOP mode		V_{DD} = 3.0 V			0.61	2.25	µA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator (16-pin products only), I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Not including the current flowing into the 12-bit interval timer and watchdog timer.

4. When the high-speed system clock is stopped.

5. When the high-speed on-chip oscillator is stopped.

6. 16-pin products only

Remarks 1. f_{IH}: High-speed on-chip oscillator clock frequency

2. f_{MX}: High-speed system clock frequency (X1 clock oscillator frequency or external main system clock frequency)

3. Temperature condition of the typical value is T_A = 25°C

(3) Peripheral Functions (Common to all products)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.30		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 3				0.01		μA
Watchdog timer operating current	I_{WDT} Notes 1, 4				0.01		μA
A/D converter operating current	I_{ADC} Notes 1, 5	When conversion at maximum speed	V_{DD} = 5.0 V		1.30	1.90	mA
			V_{DD} = 3.0 V		0.50		mA
Comparator operating current	I_{CMP} Notes 1, 6	In high-speed mode	V_{DD} = 5.0 V		6.50		μA
		In low-speed mode	V_{DD} = 5.0 V		1.70		μA
Internal reference voltage operating current	I_{VREG} Note 1				10		μA

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{TMKA}, when the 12-bit interval timer is in operation.

4. Current flowing only to the watchdog timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{WDT} when the watchdog timer is in operation.

5. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the comparator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator is in operation.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the typical value is T_A = 25°C

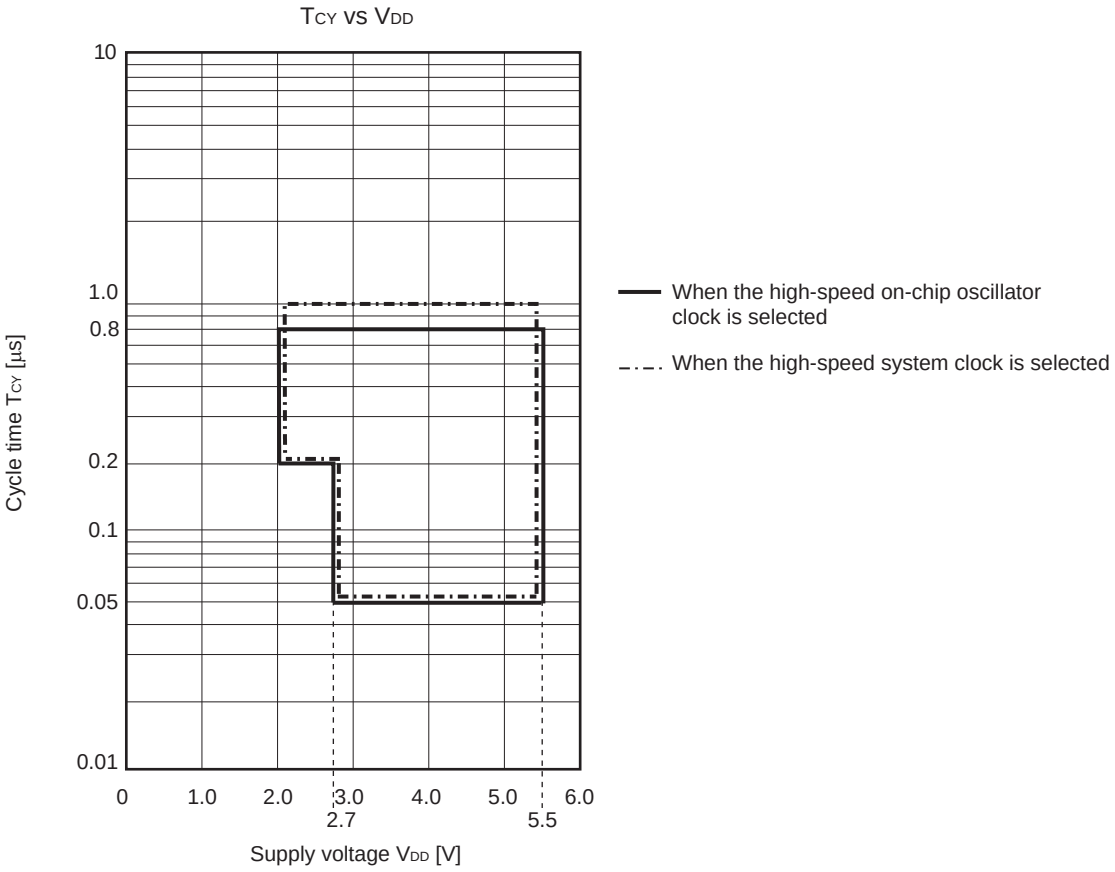
2.4 AC Characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

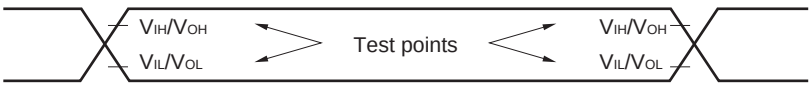
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	When high-speed on-chip oscillator clock (f_{IH}) is selected	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		0.8	µs
			2.0 V ≤ V_{DD} < 2.7 V	0.2		0.8	µs
		When high-speed system clock (f_{MX}) is selected	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		1.0	µs
			2.0 V ≤ V_{DD} < 2.7 V	0.2		1.0	µs
External system clock frequency	T_{EX}		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20	MHz
			2.0 V ≤ V_{DD} < 2.7 V	1.0		5	MHz
External system clock input high-level width, low-level width	T_{EXH}, T_{EXL}		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns
			2.0 V ≤ V_{DD} < 2.7 V	95			ns
TI00 to TI03 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used		1/f_{MCK} + 10			ns
TO00 to TO03 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n1 bit of timer mode register 0nH (TMR0nH). n: Channel number (n = 0 to 3))

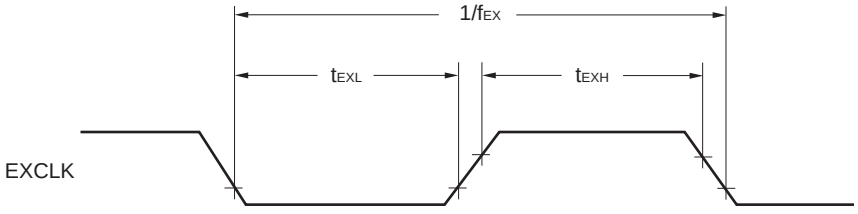
Minimum Instruction Execution Time during Main System Clock Operation



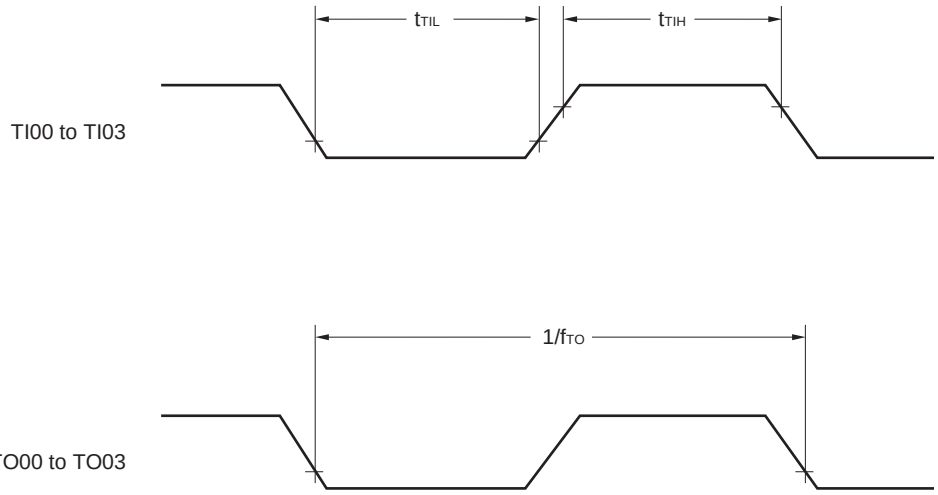
AC Timing Test Points



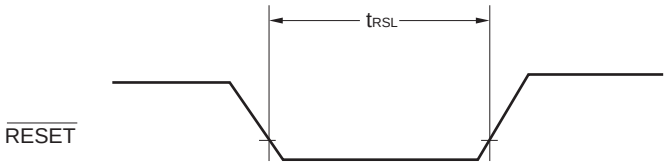
External System Clock Timing



TI/TO Timing

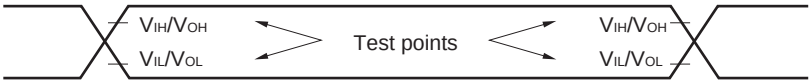


$\overline{\text{RESET}}$ Input Timing



2.5 Serial Interface Characteristics

AC Timing Test Points



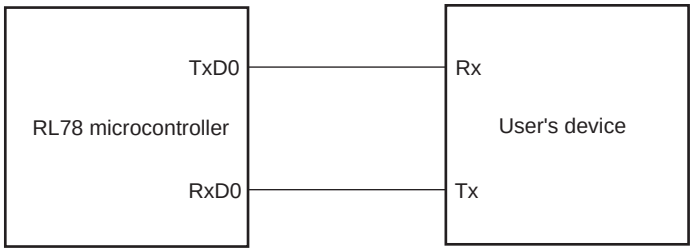
2.5.1 Serial array unit

(1) UART mode

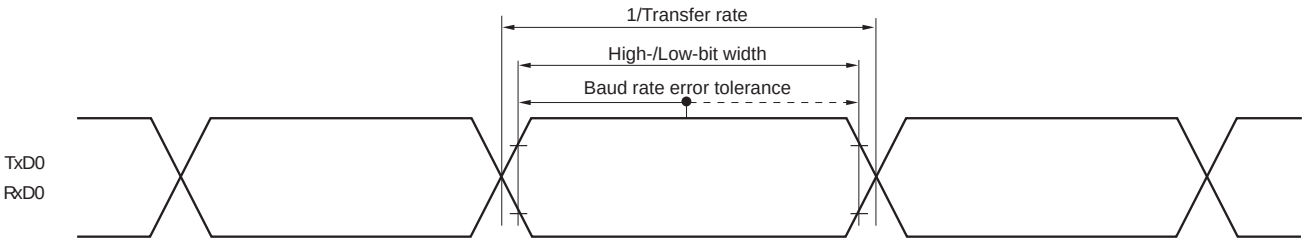
(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 20 MHz			3.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

(2) Simplified SPI (CSI) mode (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2$ - 18			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2$ - 50			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		47			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		110			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 30 pF Note 3				25	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to SCKp↓" and SIp hold time becomes "from SCKp↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from SCKp↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

(3) Simplified SPI (CSI) mode (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY2}/2$ - 18			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}	2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 50	ns
			2.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 110	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to SCKp↓" and the SIp hold time becomes "from SCKp↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

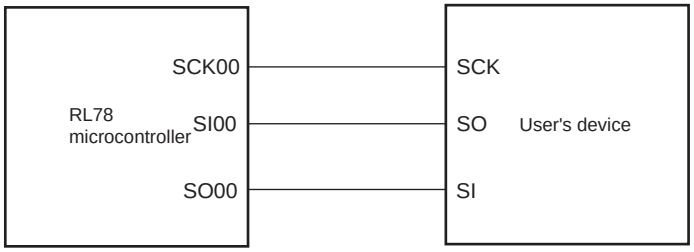
2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from SCKp↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. C is the load capacitance of the SOp output lines.

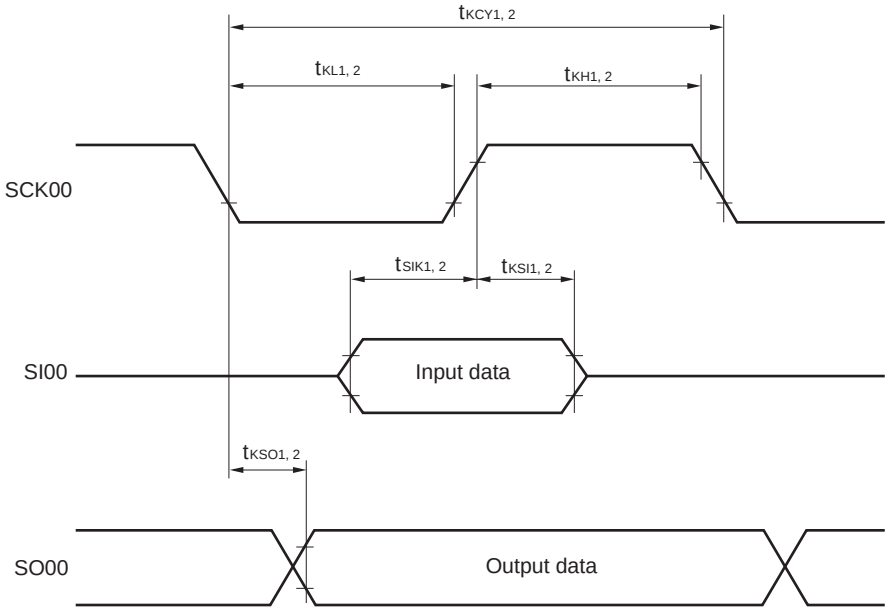
Remarks 1. p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

Simplified SPI (CSI) mode connection diagram



Simplified SPI (CSI) mode serial transfer timing
(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1.)



Remark p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

(4) Simplified I²C mode

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

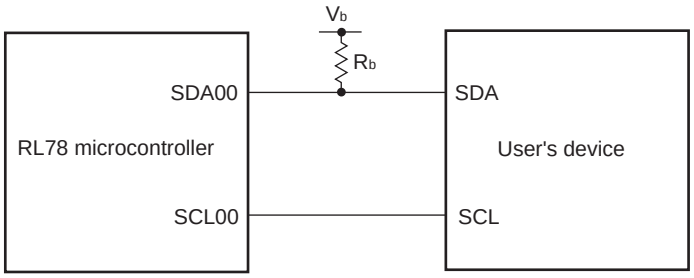
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = "H"	t_{HIGH}	C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 100 pF, R_b = 3 kΩ	0	355	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

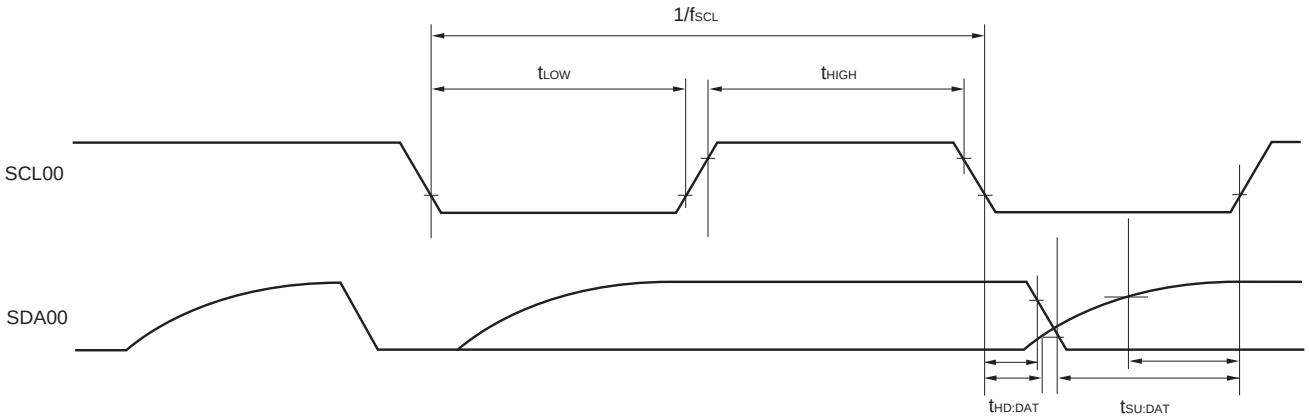
2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).

Simplified I²C mode connection diagram



Simplified I²C mode serial transfer timing



Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance,
C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IIC number (r = 00)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0))

2.5.2 Serial interface IICA

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz			0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		µs
Hold time[Note 1]	$t_{HD:STA}$		4.0		0.6		µs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

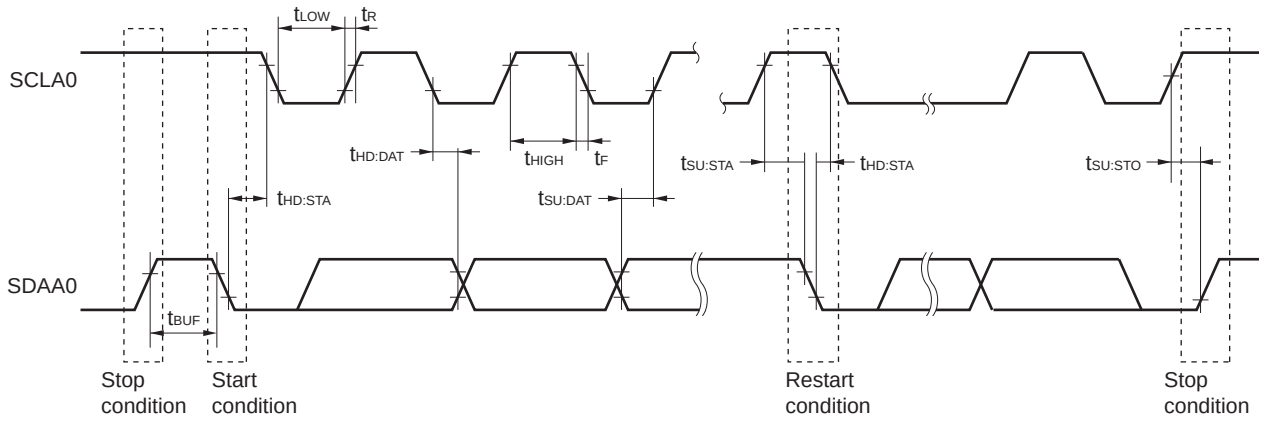
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 200 pF, R_b = 1.7 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(Target pin: ANI0 to ANI6, internal reference voltage)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Notes 1, 2, 3	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1	LSB
			V_{DD} = 3 V		±2.3	±4.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI6	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V Note 5	4.6		18.4	µs
		10-bit resolution Target pin: internal reference voltage Note 6	2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	µs
Zero-scale error Notes 1, 2, 3, 4	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19	%FSR
			V_{DD} = 3 V			±0.39	%FSR
Full-scale error Notes 1, 2, 3, 4	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29	%FSR
			V_{DD} = 3 V			±0.42	%FSR
Integral linearity error Notes 1, 2, 3	ILE	10-bit resolution	V_{DD} = 5 V			±1.8	LSB
			V_{DD} = 3 V			±1.7	LSB
Differential linearity error Notes 1, 2, 3	DLE	10-bit resolution	V_{DD} = 5 V			±1.4	LSB
			V_{DD} = 3 V			±1.5	LSB
Analog input voltage	V_{AIN}	Target pin: ANI0 to ANI6		0		V_{DD}	V
		Target pin: internal reference voltage Note 6		V_{REG} Note 7			V

Notes 1. TYP. Value is the average value at T_A = 25°C. MAX. value is the average value ±3σ at normal distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of 2.4 V ≤ V_{DD} < 2.7 V.

6. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when the internal reference voltage is selected as the target for conversion.

7. Refer to **2.6.3 Internal reference voltage characteristics**.

Cautions 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

3. Note that the internal reference voltage cannot be used as the reference voltage of the comparator when the internal reference voltage is selected as the target for A/D conversion.

2.6.2 Comparator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	I_{VREF}	IVREF0 pin input (when C0VFR bit = 0)		0		V_{DD} - 1.4	V
		Internal reference voltage (when C0VRF bit = 1) Note 1		V_{REG} Note 2			V
	I_{VCMP}	IVCMP0 pin input		-0.3		V_{DD} + 0.3	V
Output delay	t_d	V_{DD} = 3.0 V, input slew rate > 50 mV/µs	High-speed mode			0.5	µs
			Low-speed mode		2.0		µs
Operation stabilization wait time	t_{CMP}			100			µs

Notes 1. When the internal reference voltage is selected as the reference voltage of the comparator, the internal reference voltage cannot be used as the target for A/D conversion.

2. Refer to **2.6.3 Internal reference voltage characteristics**.

2.6.3 Internal reference voltage characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{REG}		0.74	0.815	0.89	V
Operation stabilization wait time	t_{AMP}	When A/D converter is used (ADS register = 07H)	5			µs

Note The internal reference voltage cannot be simultaneously used by the A/D converter and the comparator; only one of them must be selected.

2.6.4 SPOR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	The power supply voltage is rising.	4.08	4.28	4.45	V
			The power supply voltage is falling.	4.00	4.20	4.37	V
		V_{SPOR1}	The power supply voltage is rising.	2.76	2.90	3.02	V
			The power supply voltage is falling.	2.70	2.84	2.96	V
		V_{SPOR2}	The power supply voltage is rising.	2.44	2.57	2.68	V
			The power supply voltage is falling.	2.40	2.52	2.62	V
		V_{SPOR3}	The power supply voltage is rising.	2.05	2.16	2.25	V
			The power supply voltage is falling.	2.00	2.11	2.20	V
Minimum pulse width Note		T_{LSPW}		300			μs

Note Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPOR}.

Caution Set the detection voltage (V_{SPOR}) in the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H). The operating voltage range is as follows:
When the CPU operating frequency is from 1 MHz to 20 MHz: V_{DD} = 2.7 to 5.5 V
When the CPU operating frequency is from 1 MHz to 5 MHz: V_{DD} = 2.0 to 5.5 V

2.6.5 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

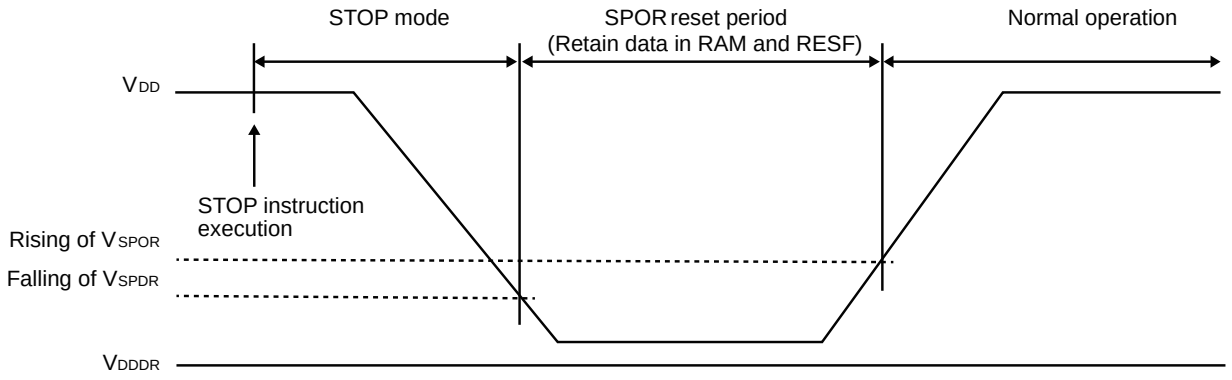
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.7 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.9		5.5	V

Caution Data in RAM is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}). Note that data in the RESF register might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}).



2.8 Flash Memory Programming Characteristics

(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Code flash memory rewritable times Notes 1, 2, 3	C_{erwr}	Retained for 20 years.	T_A = +85°C	1000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

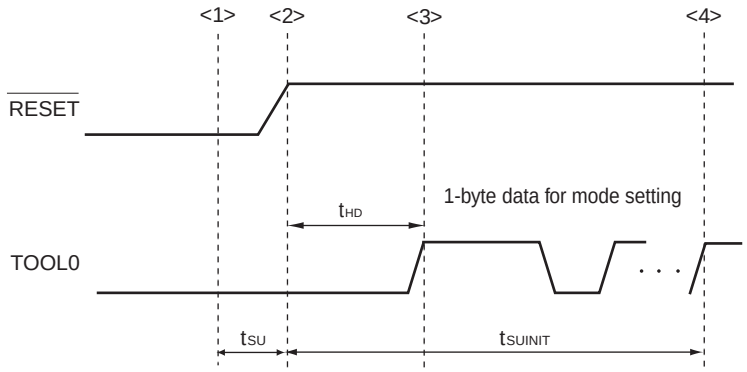
(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

Remark The transfer rate during flash memory programming is fixed to 115,200 bps.

2.10 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	SPOR reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	SPOR reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released	t_{HD}	SPOR reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (SPOR reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of entry to the flash memory programming mode by UART reception is completed.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

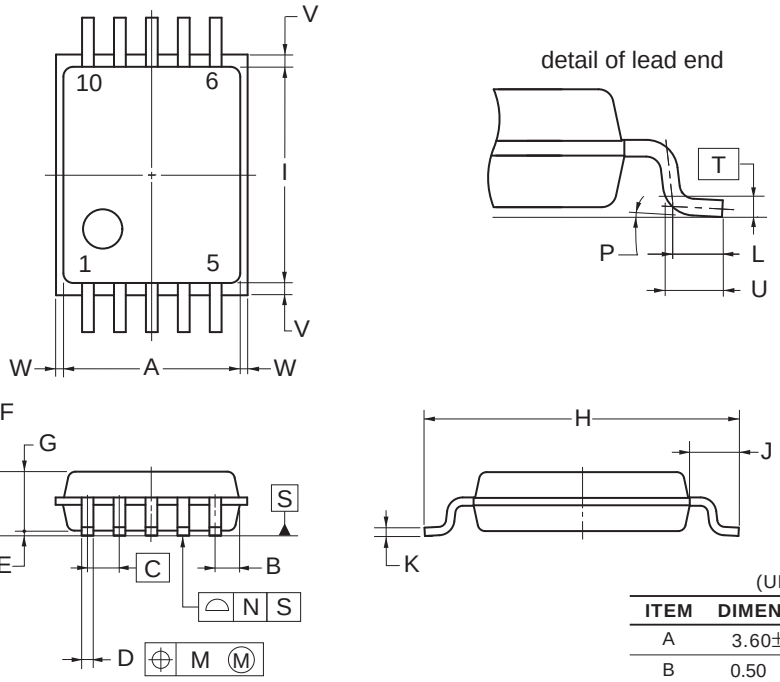
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released

3. PACKAGE DRAWINGS

3.1 10-pin products

R5F10Y17ASP, R5F10Y16ASP, R5F10Y14ASP
R5F10Y17DSP, R5F10Y16DSP, R5F10Y14DSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



(UNIT:mm)

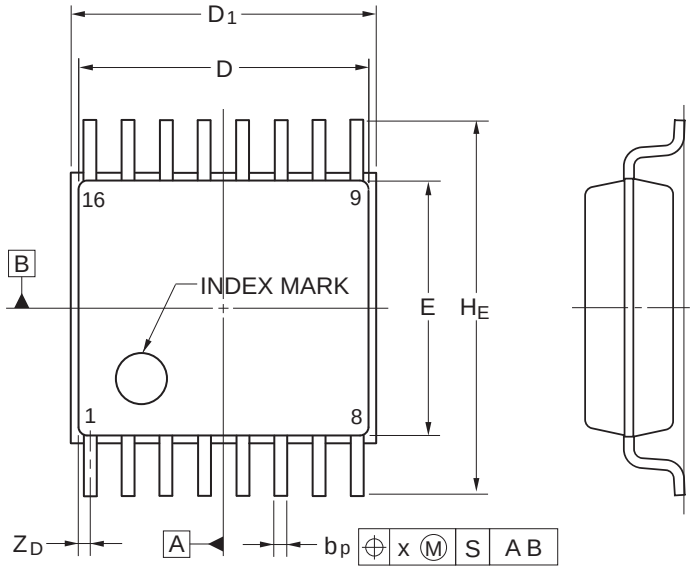
ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

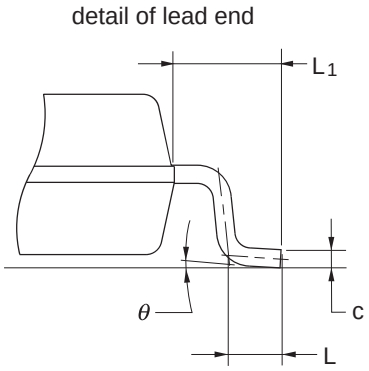
NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

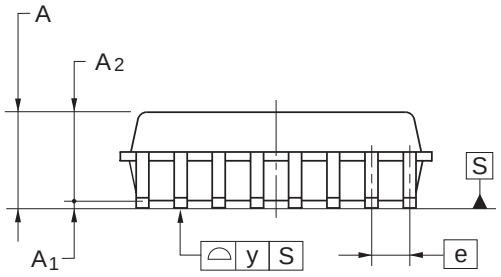
3.2 16-pin products

R5F10Y47ASP, R5F10Y46ASP, R5F10Y44ASP
R5F10Y47DSP, R5F10Y46DSP, R5F10Y44DSP

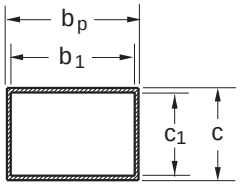
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-B	P16MA-65-FAB-1	0.08







Terminal cross section



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.85	5.00	5.15
D_1	5.05	5.20	5.35
E	4.20	4.40	4.60
A_2	—	1.50	—
A_1	0.075	0.125	0.175
A	—	—	1.725
b_p	0.17	0.24	0.32
b_1	—	0.22	—
c	0.14	0.17	0.20
c_1	—	0.15	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.225	—
L	0.35	0.50	0.65
L_1	—	1.00	—

Revision History	RL78/G10 Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 15, 2013	-	First Edition issued
2.00	Jan 10, 2014	1, 2	Modification of descriptions in 1.1 Features
		3	Modification of description in 1.2 List of Part Numbers
		4	Modification of remark 2 in 1.3.1 10-pin products and 1.3.2 16-pin products
		8, 9	Addition of description of R5F10Y17ASP in 1.6 Outline of Functions
		11	Modification of description in 2.1 Absolute Maximum Ratings
		12	Modification of description in 2.2 Oscillator Characteristics
		13, 14	Modification of description, notes 1 to 4, and caution in 2.3.1 Pin characteristics
		16	Addition of description, notes 1 to 6, and remarks 1 and 2 in (2) Flash ROM: 4 KB of 10-pin products, and 16-pin products
		17	Addition of description, notes 1 to 6, and remarks 1 to 3 in (3) Peripheral Functions (Common to all products)
		18	Modification of description in 2.4 AC Characteristics
		19	Addition of figure of Minimum Instruction Execution Time during Main System Clock Operation
		19	Addition of figure of External System Clock Timing
		20	Modification of TI/TO Timing
		25	Addition of description in 2.5.2 Serial interface IICA
		26	Modification of description and notes 1 to 6 in 2.6.1 A/D converter characteristics
		27	Addition of description, notes 1 and 2 in 2.6.2 Comparator characteristics
		27	Addition of description and note in 2.6.3 Internal reference voltage characteristics
		28	Addition of caution in 2.6.4 SPOR Circuit characteristics
		28	Addition of figure in 2.6.6 Data retention power supply voltage characteristics
		31	Addition of R5F10Y17ASP in 3.1 10-pin products
		32	Modification of package drawing in 3.2 16-pin products
3.00	Nov 19, 2014	3	Addition of industrial applications in Figure 1-1 Part Number, Memory Size, and Package of RL78/G10
		3	Addition of industrial applications in Table 1-1 List of Ordering Part Numbers
		4	Addition of description to pin configuration in 1.3.1 10-pin products and 1.3.2 16-pin products
		22	Correction of error in 2.5.1 Serial array unit, (3) CSI mode (slave mode, SCKp... external clock input)
		28	Renamed to 2.7 RAM Data Retention Characteristics and modification of figure
		31	Addition of industrial application in 3.1 10-pin products
		32	Addition of industrial application in 3.2 16-pin products and modification of package drawing
3.10	Aug 12, 2016	1	Addition of description to Rich Analog in 1.1 Features
		3	Corrected Table 1-1. List of Ordering Part Numbers
		4	Modification of 1.3 Pin Configuration (Top View)
		31, 32	Deletion of under development
3.20	Mar 20, 2023	All	The module name for CSI was changed to Simplified SPI (CSI)
		All	"wait" for IIC was modified to "clock stretch"
		1	Addition of note in 1.1 Features
		3	Modification of description in Figure 1-1. Part Number, Memory Size, and Package of RL78/G10
		3	Modification of description in Table 1-1. List of Ordering Part Numbers
		4	Addition of Table 1-2. Alternate Function of 10-pin products
		5	Addition of Table 1-3. Alternate Function of 16-pin products
		29	Modification of description in 2.6.4 SPOR circuit characteristics
3.21	Mar 22, 2024	3	Modification of description in Figure 1-1. Part Number, Memory Size, and Package of RL78/G10
		3	Modification of description in Table 1-1. List of Ordering Part Numbers

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.