

## RL78/F15 RENESAS MCU

R01DS0461EJ0110  
Rev.1.10  
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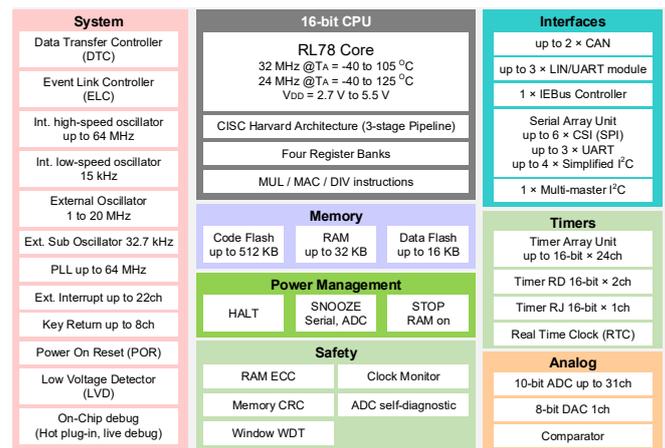
RL78/F15 automotive microcontrollers employ the RL78 core, which realizes high processing performance while delivering the lowest power consumption in its class. A high-speed on-chip oscillator provides 32MHz CPU operation. An enhanced motor control functionality is offered by the motor control timer (Timer RD). For easy migration, RL78/F15 is pin and software upwards compatible with RL78/F14. The RL78/F15 Group even supports 125 °C (target) operation, whereby a CPU clock of 24 MHz can be reached. In addition, an abundance of functions to support functional safety, like ECC on RAM and a stack pointer monitor as well as an A/D converter testing function are available. With packages from 48 to 144-pin, a memory range from 128KB to 512KB flash, and advanced IPs for LIN and 2 channels of CAN communication and IEBus, these products are very well suited for a broad range of cost-sensitive automotive applications like DC and BLDC motor control, HVAC, lighting and many kinds of body applications.

## 1. OVERVIEW

### 1.1 Features

- Minimum instruction execution time can be changed from high speed (0.03125 μs: @ 32 MHz operation with high-speed on-chip oscillator clock or PLL clock) to ultra low-speed (66.6 μs: @ 15 kHz operation with low-speed on-chip oscillator clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM: 128K to 512KB
- RAM: 10K to 32KB
- Data flash memory: 8KB/16KB
- High-speed on-chip oscillator clock  
Selectable from 32 MHz (Typ.), 24 MHz (Typ.), 16 MHz (Typ.), 12 MHz (Typ.), 8 MHz (Typ.), 4 MHz (Typ.), and 1 MHz (Typ.) (Selectable from 64 MHz (Typ.) and 48 MHz (Typ.) when using Timer RD)
- Low-speed on-chip oscillator clock: 15 kHz × 2 channels (one for WWDT and one for CPU and peripherals other than WWDT)
- On-chip PLL (×3, ×4, ×6, ×8)
- On-chip single-power-supply flash memory (with prohibition of block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the dedicated low-speed on-chip oscillator clock)
- Multiply/divide/multiply & accumulate instructions are supported
  - 16 bits × 16 bits = 32 bits (Unsigned or signed)
  - 32 bits ÷ 32 bits = 32 bits (Unsigned)
  - 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 44 to 136 (including one input-only pin)
- Timer
  - 16-bit timer array unit: 16 to 24 channels
  - 16-bit timer RD: 2 channels (six triangle-wave outputs; sawtooth wave/triangle-wave modulation)

- 16-bit timer RJ: 1 channel
- Watchdog timer: 1 channel
- Real-time clock: 1 channel
- Serial interface
  - CSI
  - UART/UART (LIN-bus supported)
  - LIN module (master/slave supported)
  - I<sup>2</sup>C/simplified I<sup>2</sup>C
  - CAN interface (RS-CAN lite)
  - IEBus controller
- 8/10-bit resolution A/D converter (VDD = 2.7 to 5.5 V): 18 to 31 channels
- DTC (Max. 52 sources)
- ELC (Max. 26 channels for event link source, Max. 9 channels for event link destination)
- Safety functions (CRC calculation, Clock monitor, AD test, SFR guard, etc.)
- 8-bit D/A converter
- On-chip comparator: 1 channel (input pin: 4 channels)
- Power supply voltage: VDD = 2.7 to 5.5 V
- Operating ambient temperature:
  - TA = -40 to +105°C (grade L)
  - TA = -40 to +125°C (grade K)



RL78/F15 Block Diagram (Outline)

### Applications

General automotive electrical applications (motor control, door control, headlight control, etc.), motorcycle engine control.

## 1.2 Product Lineup

Table 1-1. RL78/F15 Lineup

Code Flash	Data Flash	RAM	Pin Count					
			144 pins	100 pins	80 pins	64 pins	48 pins (HVQFN)	48 pins (LFQFP)
128 KB	8 KB	10 KB	R5F113TG	R5F113PG	–	–	–	–
192 KB		16 KB	R5F113TH	R5F113PH	–	–	–	–
256 KB		20 KB	R5F113TJ	R5F113PJ	–	–	–	–
384 KB	16 KB	26 KB	R5F113TK	R5F113PK	R5F113MK	R5F113LK	R5F113GK	R5F113GK
512 KB		32 KB	R5F113TL	R5F113PL	R5F113ML	R5F113LL	R5F113GL	R5F113GL

&lt;R&gt;

1.3 Function Overview

1.3.1 RL78/F15 Functions List

Table 1-2. RL78/F15 Functions List

Series Name		R5F113T	R5F113P	R5F113M	R5F113L	R5F113G
Pin Count		144 pins	100 pins	80 pins	64 pins	48 pins
Code flash		128K to 512KB		384K/512KB		
Data flash		8/16KB		16KB		
RAM		10K to 32KB		26/32KB		
Supply voltage range		2.7 V to 5.5 V				
Maximum operation frequency		32 MHz (grade L), 24 MHz (grade K)				
System clock	Main system clock oscillator	Crystal/ceramic/square wave 1 to 20 MHz (operating at 2.7 V to 5.5 V)				
	High-speed on-chip oscillator	Normal high accuracy 32 MHz (typ.)				
	Low-speed on-chip oscillator	For low-speed operation 15 kHz (typ.)				
	Subsystem clock oscillator	32.768 kHz				
PLL		PLL multiplication factor: $\times 3/\times 4/\times 6/\times 8$				
Clock for peripherals	Low-speed on-chip oscillator	For peripherals other than WDT		15 kHz (typ.)		
		For WDT		15 kHz (typ.)		
POR		When power supply is rising		1.56 V (typ.)		
		When power supply is falling		1.55 V (typ.)		
LVD	V <sub>DD</sub> voltage detection	When power supply is rising		2.81 V (typ.) to 4.74 V (typ.) (in 6 steps)		
		When power supply is falling		2.75 V (typ.) to 4.64 V (typ.) (in 6 steps)		
Safety functions	WWDT (window watchdog timer)		Yes			
	Illegal instruction execution detection function		Yes			
	Flash memory CRC operation function		Yes			
	RAM1 bit error correction function		Yes			
	RAM2 bit error detection function		Yes			
	Invalid memory access detection function		Yes			
	Frequency detection function		Yes			
	Clock monitor function		Yes			
	Stack pointer monitor function		Yes			
	I/O port output signal level detection function		Yes			
A/D test function		Yes				
I/O ports	Input/Output	CMOS	130ch	86ch	68ch	52ch
	Output	CMOS	1ch			
	Input	Shared with oscillator pins	4ch			
		Input only	1ch			
Power supply pins	For internal circuits		V <sub>DD</sub> , V <sub>SS</sub> , REGC			
	For I/O ports		EV <sub>DD0</sub> , EV <sub>SS0</sub> EV <sub>DD1</sub> , EV <sub>SS1</sub>	EV <sub>DD0</sub> , EV <sub>SS0</sub>		None
	For analog circuits (AD, DA, COMP)		V <sub>DD</sub> , V <sub>SS</sub> (AV <sub>REFP</sub> , AV <sub>REFM</sub> ; For AD)			
Multiply/divide and multiply-accumulate functions	Multiply		16 bits × 16 bits (signed)			
			16 bits × 16 bits (unsigned)			
	Divide		32 bits + 32 bits (unsigned)			
	Multiply-accumulate		16 bits × 16 bits + 32 bits (signed)			
Arithmetic instructions (extended instruction set)		16 bits × 16 bits + 32 bits (unsigned)				
Vectored interrupt sources	External <sup>Note 1,2</sup>		22ch	20ch	19ch	18ch
	Internal <sup>Note 1</sup>		51ch			
Key return detection		8ch				
DTC		52 sources	50 sources	46 sources		
Timer	TAU		16 bits (8ch × 3)	16 bits (8ch × 2)		
	RTC		1ch			
	Timer RJ		16 bits × 1			
	Timer RD		16 bits × 2			
Serial I/F	CSI/simplified I <sup>2</sup> C /UART		6ch/4ch/3ch		4ch/4ch/2ch	
	SPI		Yes			
	Multimaster I <sup>2</sup> C		1ch			
	IEBus controller		1ch			
	LIN/UART module (RLIN3)		3ch		2ch	
CAN interface (RS-CAN lite)		2ch				
A/D converter 10-bit SAR	V <sub>DD</sub>		24ch	18ch	17ch	13ch
	EV <sub>DD</sub>		7ch			
	Internal		2ch			
D/A converter 8-bit		1ch				
Comparator		1ch				
ELC		Link source: 26ch Link destination: 9ch				
PCLBUZ		1ch				
Self-programming		Yes				
On-chip debug	Trace		Yes			
	Hot plug-in		Yes			
Option byte		Yes				

(Notes and Caution are listed on the next page.)

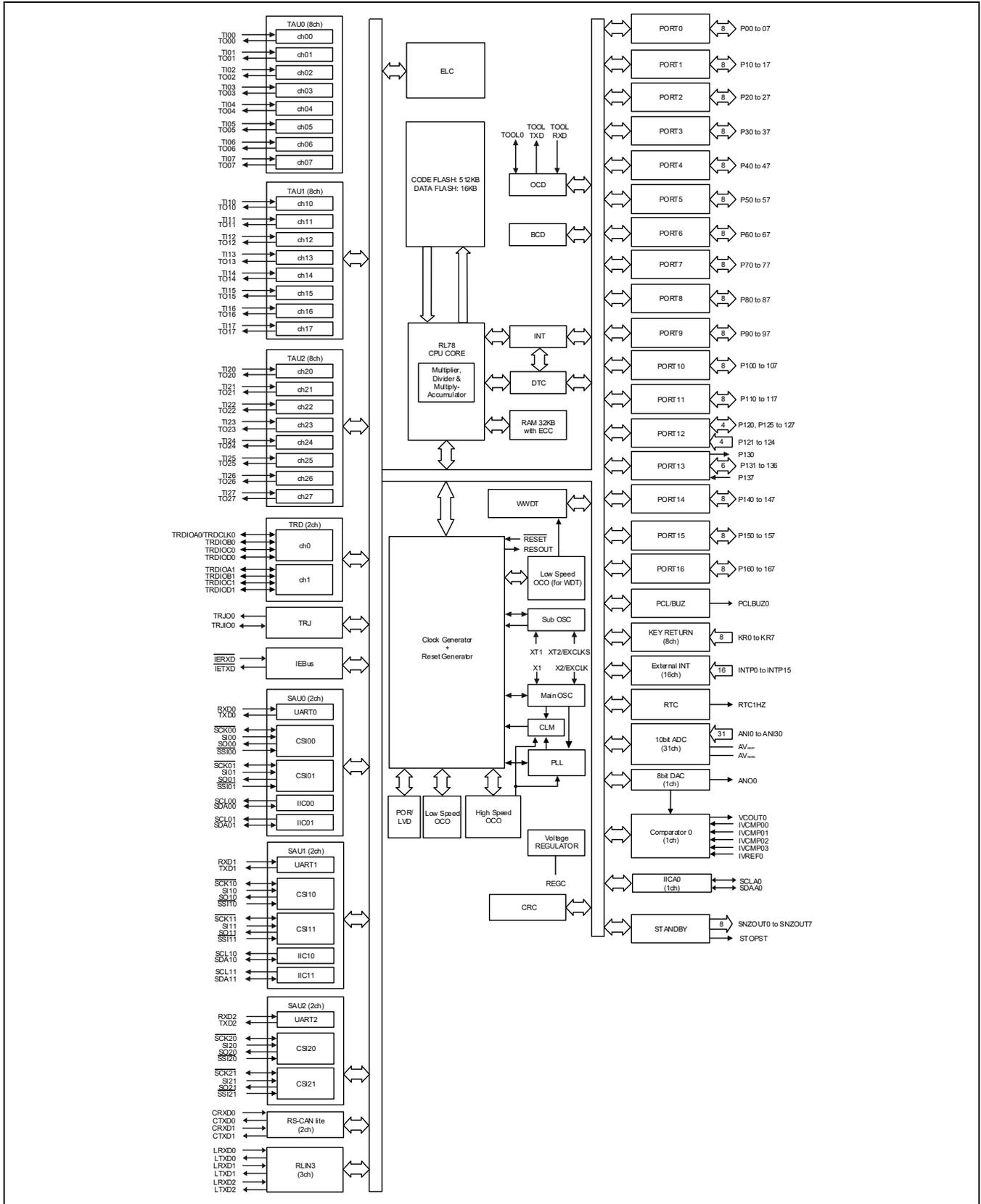
- Notes**
1. Both sources in the following pairs are counted as a single source in this number: INTPn and INTLIN0WUPH.
  2. The following pairs of internal and external sources are each counted as a single source in this number: INTPn and internal interrupt.

**Caution** For details, see 1.5 Pin Configurations.

### 1.4 Block Diagram

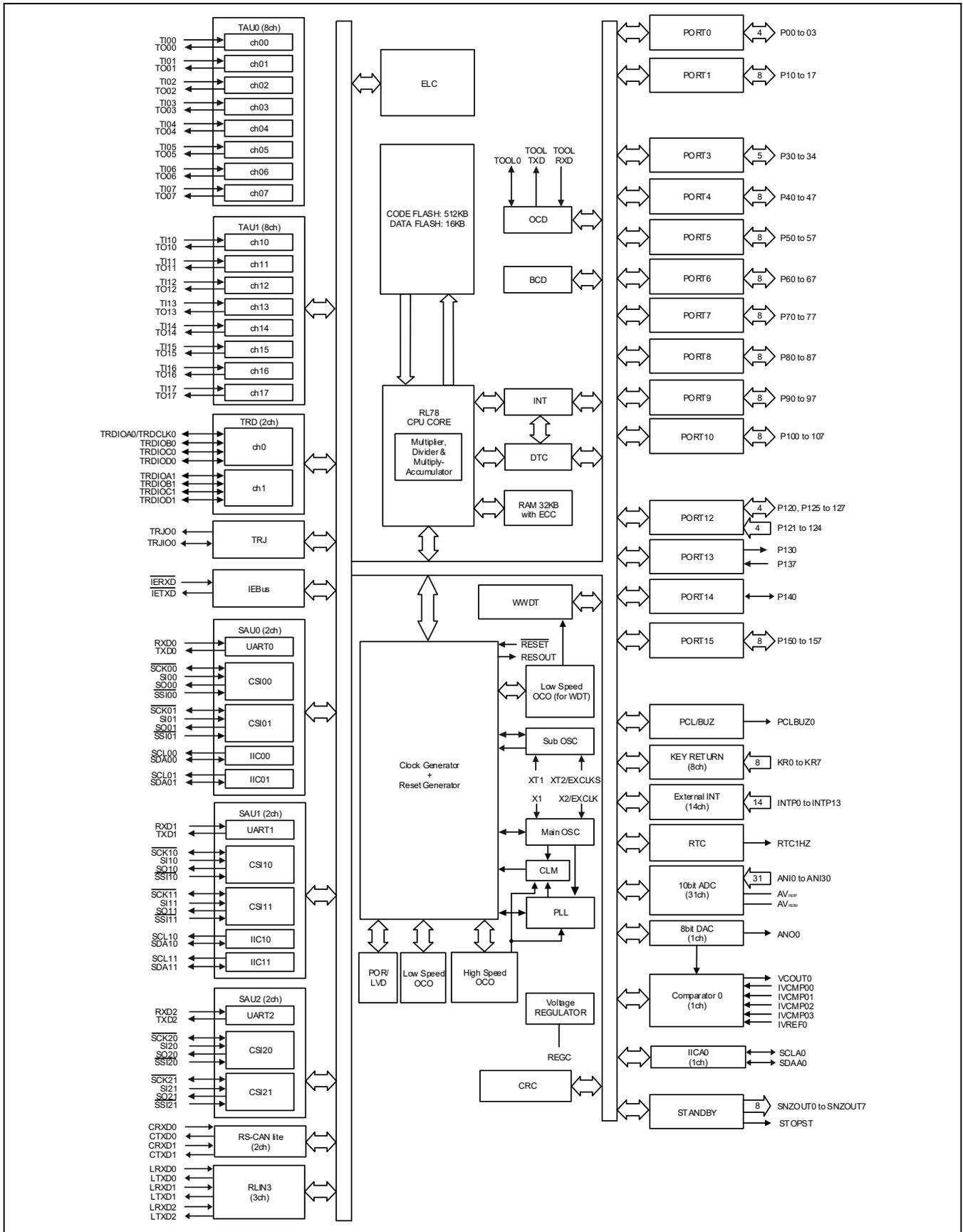
#### 1.4.1 RL78/F15: Block Diagram of R5F113TL 144-pin Products

Figure 1-1. Block Diagram



1.4.2 RL78/F15: Block Diagram of R5F113PL 100-pin Products

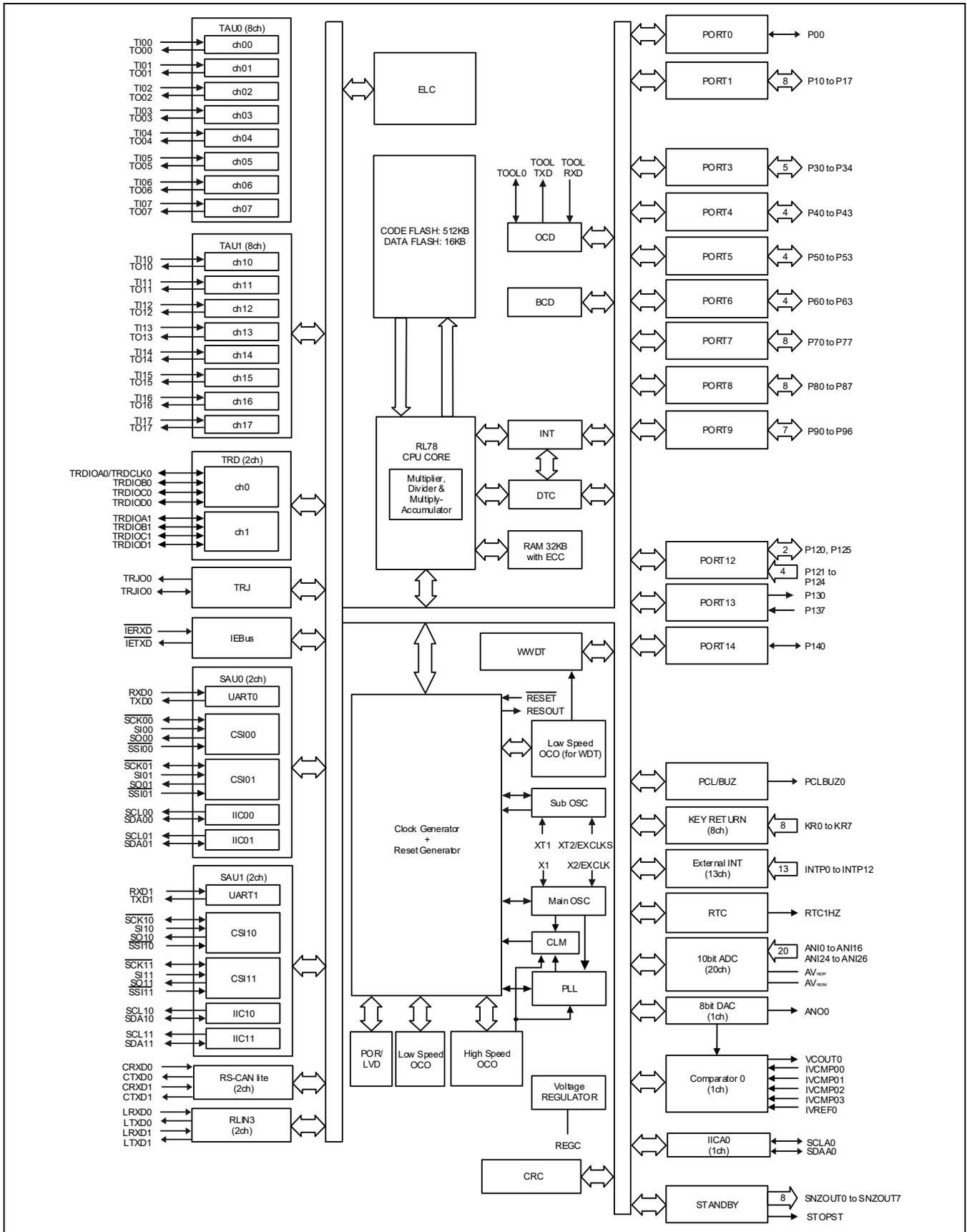
Figure 1-2. Block Diagram





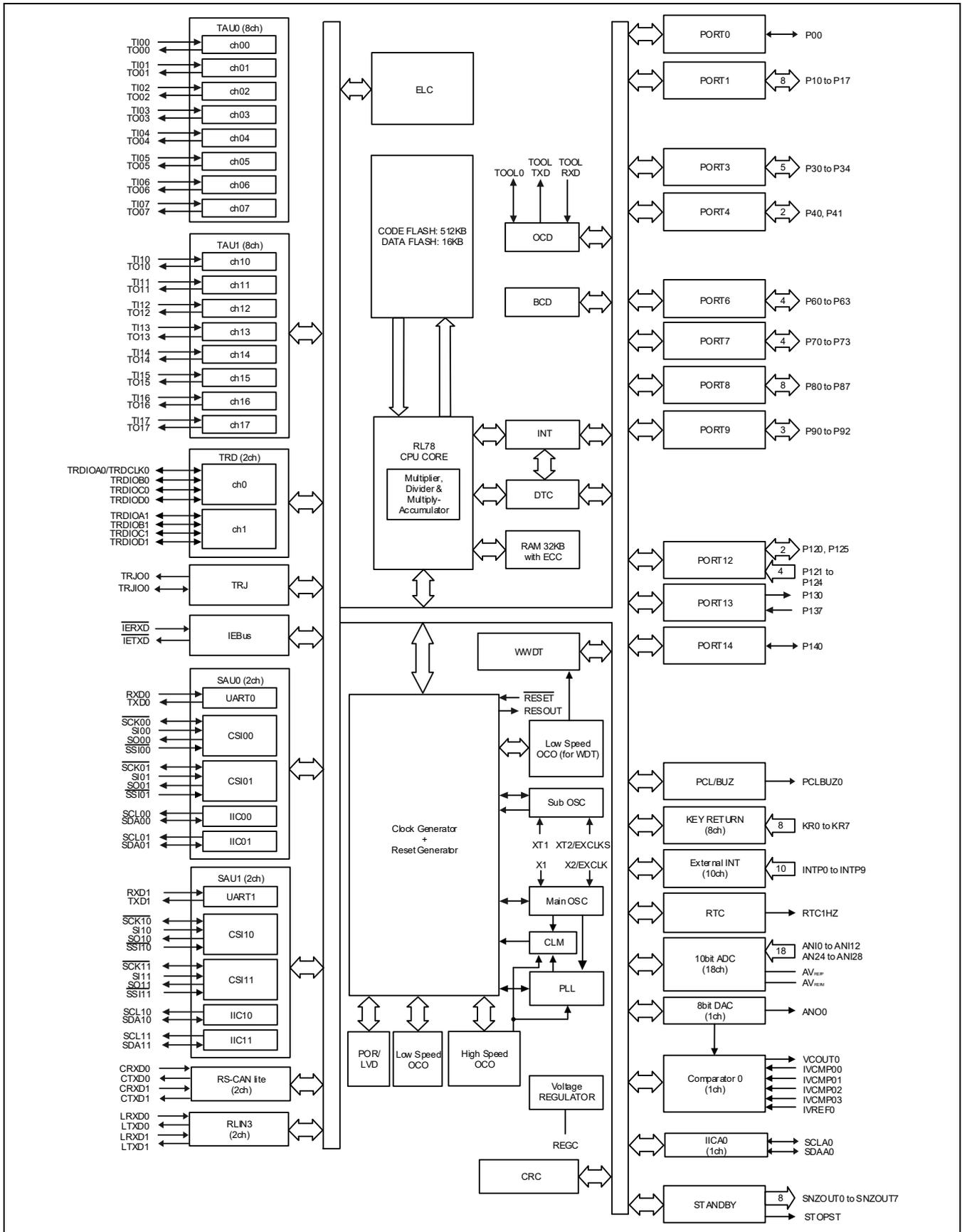
1.4.4 RL78/F15: Block Diagram of R5F113LL 64-pin Products

Figure 1-4. Block Diagram



1.4.5 RL78/F15: Block Diagram of R5F113GL 48-pin Products

Figure 1-5. Block Diagram

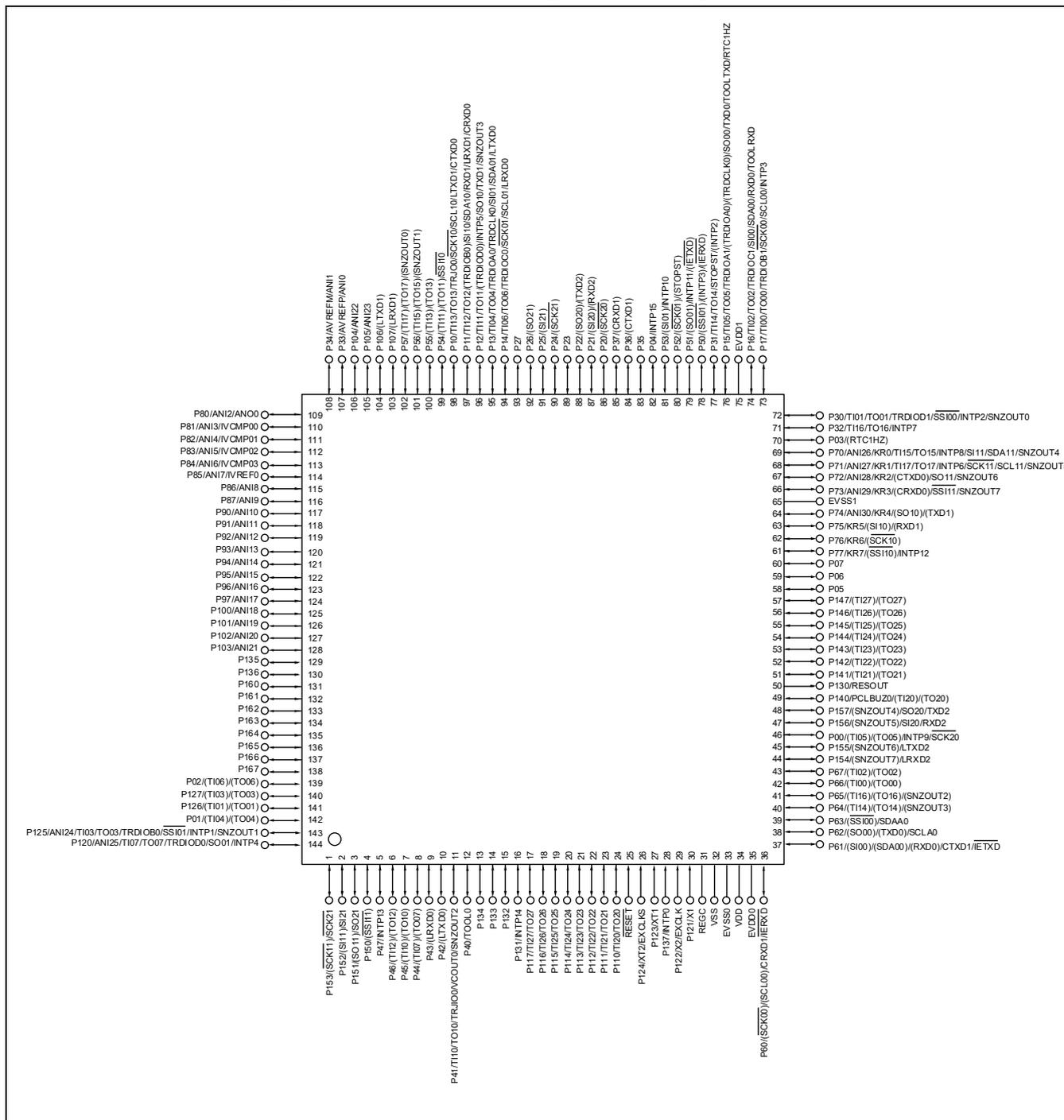


### 1.5 Pin Configurations

#### 1.5.1 RL78/F15 Pin Configuration for 144-pin Products

- RL78/F15: 144-pin Plastic LQFP (Fine Pitch) (20 x 20)

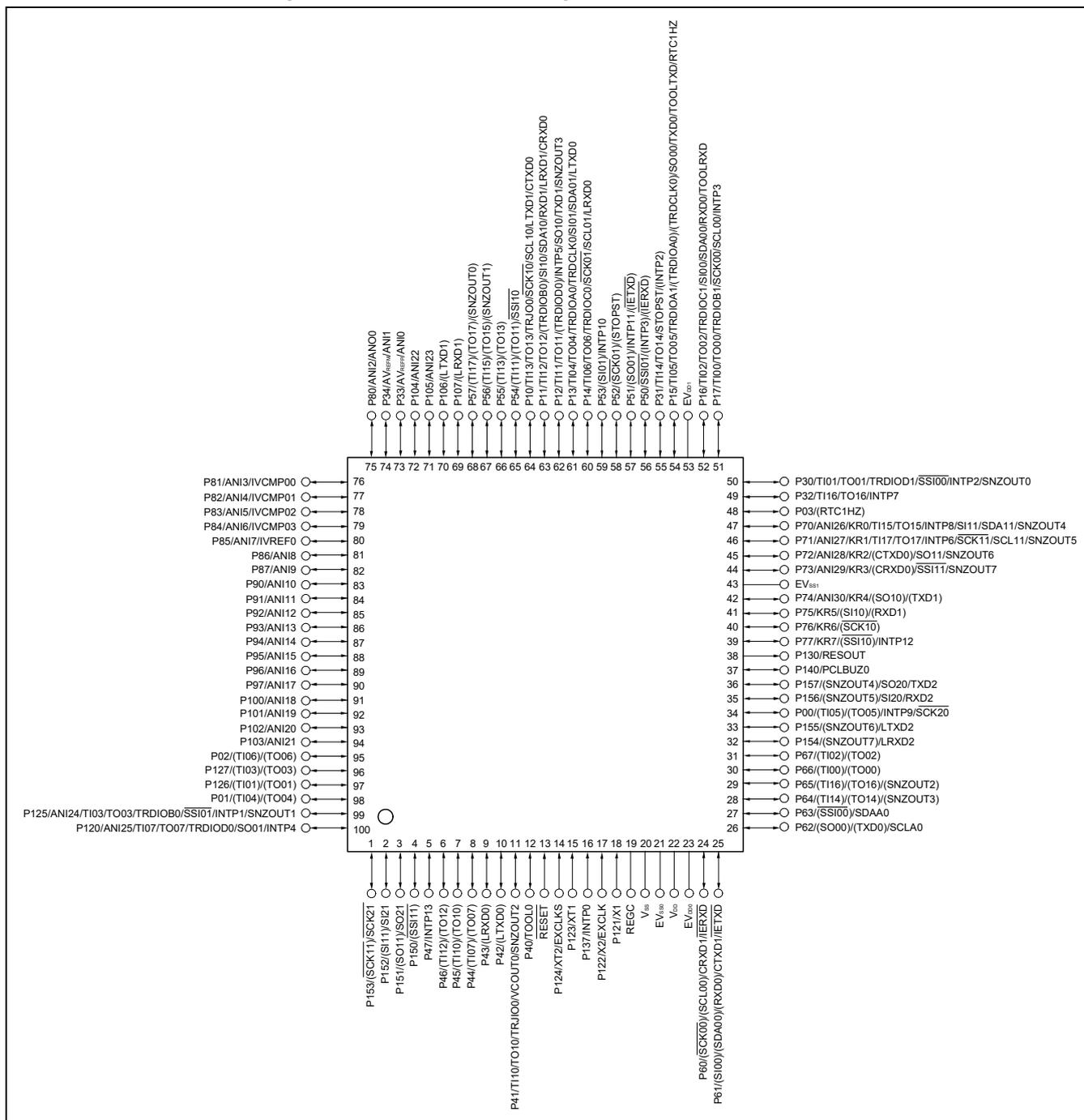
Figure 1-6. RL78/F15 Pin Configuration for 144-pin Products



1.5.2 RL78/F15 Pin Configuration for 100-pin Products

- RL78/F15: 100-pin Plastic LQFP (Fine Pitch) (14 x 14)

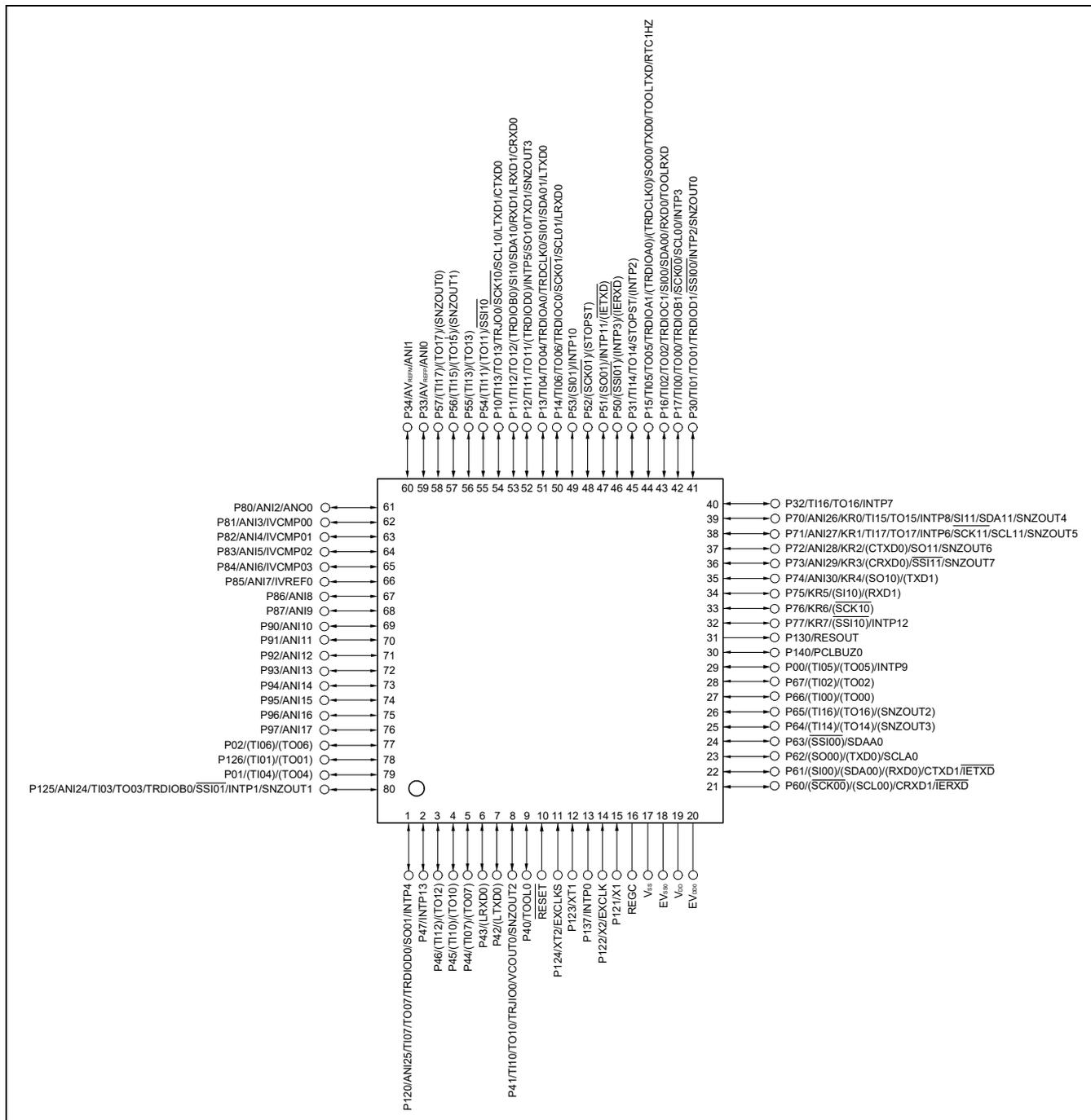
Figure 1-7. RL78/ F15 Pin Configuration for 100-pin Products



1.5.3 RL78/F15 Pin Configuration for 80-pin Products

- RL78/F15: 80-pin Plastic LQFP (Fine Pitch) (12 x 12)

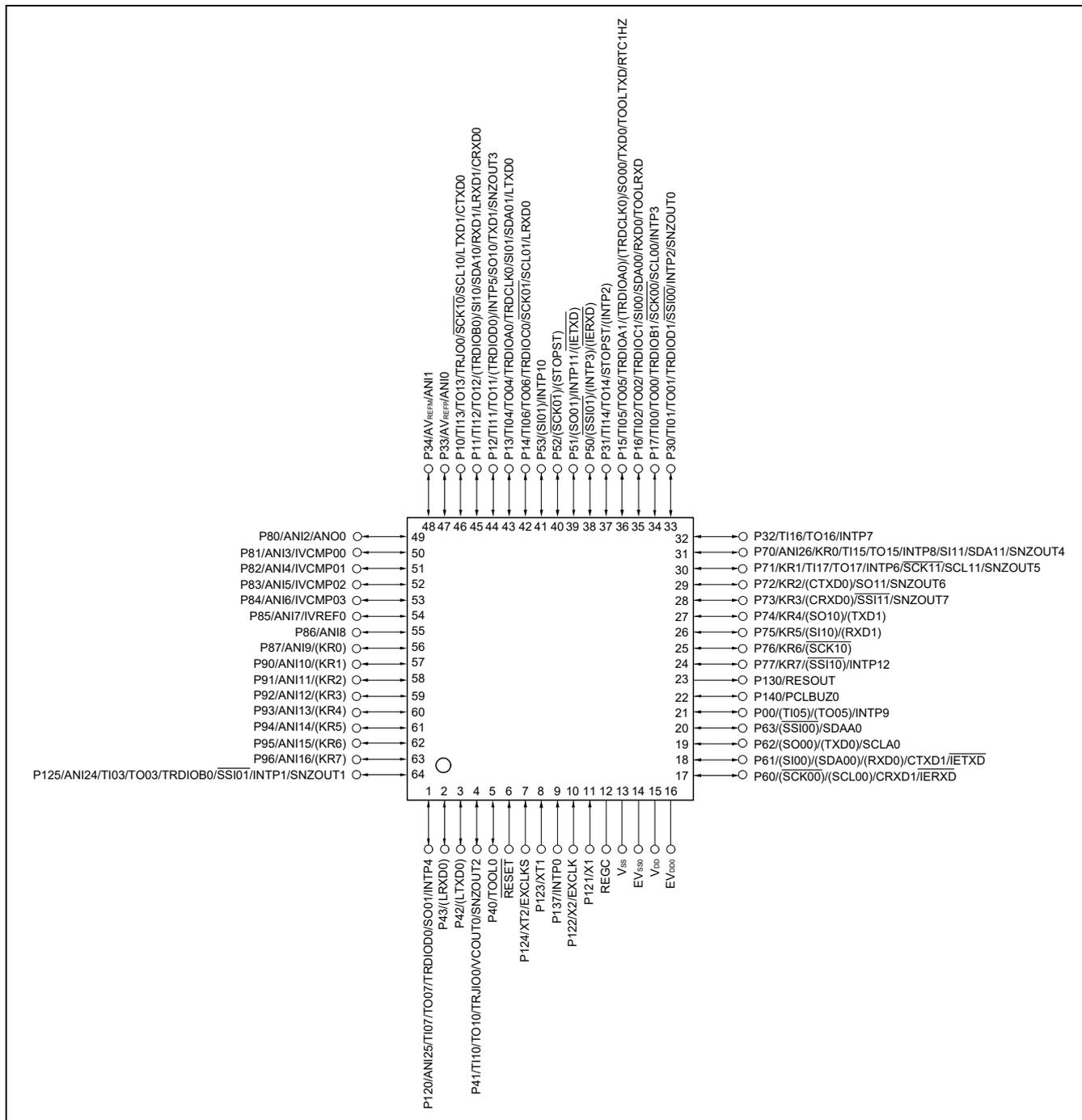
Figure 1-8. RL78/ F15 Pin Configuration for 80-pin Products



1.5.4 RL78/F15 Pin Configuration for 64-pin Products

- RL78/F15: 64-pin Plastic LQFP (Fine Pitch) (10 x 10)

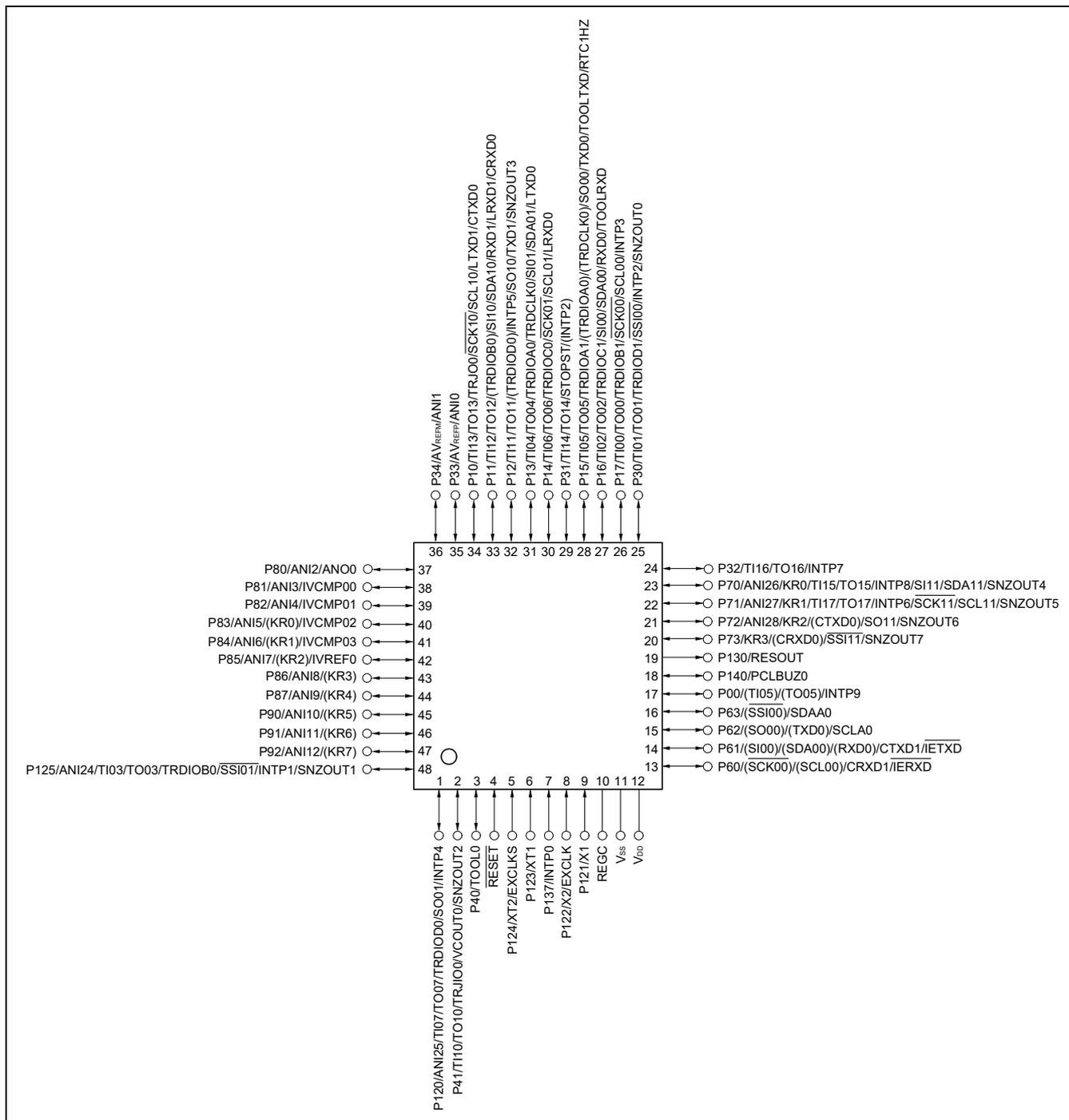
Figure 1-9. RL78/ F15 Pin Configuration for 64-pin Products



1.5.5 RL78/F15 Pin Configuration for 48-pin Products

- RL78/F15: 48-pin Plastic LFQFP (7 x 7), and HVQFN (7 x 7)

Figure 1-10. RL78/ F15 Pin Configuration for 48-pin Products



## 1.6 Order Information

Table 1-3 show the order information for RL78/F15.

**Table 1-3. Order Information for RL78/F15**

	Package	Device	Order Name
<R>	48-pin plastic LFQFP	Grade L	R5F113GKCLFB, R5F113GLCLFB
		Grade K	R5F113GKCKFB, R5F113GLCKFB
<R>	48-pin plastic HVQFN	Grade L	R5F113GKLNA, R5F113GLLNA
		Grade K	R5F113GKKNA, R5F113GLKNA
<R>	64-pin plastic LFQFP	Grade L	R5F113LKCLFB, R5F113LLCLFB
		Grade K	R5F113LKCKFB, R5F113LLCKFB
<R>	80-pin plastic LFQFP	Grade L	R5F113MKCLFB, R5F113MLCLFB
		Grade K	R5F113MKCKFB, R5F113MLCKFB
<R>	100-pin plastic LFQFP	Grade L	R5F113PGCLFB, R5F113PHCLFB, R5F113PJCLFB, R5F113PKCLFB, R5F113PLCLFB
		Grade K	R5F113PGCKFB, R5F113PHCKFB, R5F113PJCKFB, R5F113PKCKFB, R5F113PLCKFB
<R>	144-pin plastic LFQFP	Grade L	R5F113TGLFB, R5F113THLFB, R5F113TJLFB, R5F113TKLFB, R5F113TLLFB
		Grade K	R5F113TGKFB, R5F113THKFB, R5F113TJKFB, R5F113TKKFB, R5F113TLKFB

## 2. PIN FUNCTIONS

### 2.1 Pin Function List

Pin I/O buffer power supplies depend on the product. Table 2-1 shows the relationship between these power supplies and the pins.  $EV_{DD}$  indicates  $EV_{DD0}$  and  $EV_{DD1}$ .

**Table 2-1. Pin I/O Buffer Power Supplies**

#### (1) 48-pin products

Power Supply	Corresponding Pins
$V_{DD}$	All pins

#### (2) 64-pin products

Power Supply	Corresponding Pins
$EV_{DD0}$	<ul style="list-style-type: none"> <li>Port pins other than P33, P34, P80 to P87, P90 to P96, P121 to P124, and P137</li> </ul>
$V_{DD}$	<ul style="list-style-type: none"> <li>P33, P34, P80 to P87, P90 to P96, P121 to P124, and P137</li> <li>Pins other than port pins</li> </ul>

#### (3) 80-pin products

Power Supply	Corresponding Pins
$EV_{DD0}$	<ul style="list-style-type: none"> <li>Port pins other than P33, P34, P80 to P87, P90 to P97, P121 to P124, and P137</li> </ul>
$V_{DD}$	<ul style="list-style-type: none"> <li>P33, P34, P80 to P87, P90 to P97, P121 to P124, and P137</li> <li>Pins other than port pins</li> </ul>

#### (4) 100-pin and 144-pin products

Power Supply	Corresponding Pins
$EV_{DD0}$ , $EV_{DD1}$	<ul style="list-style-type: none"> <li>Port pins other than P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, and P137</li> </ul>
$V_{DD}$	<ul style="list-style-type: none"> <li>P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, and P137</li> <li>Pins other than port pins</li> </ul>

This subchapter describes the 144-pin products of RL78/F15.

2.1.1 RL78/F15 144-pin products

(1/3)

Function Name	I/O	Function	After Reset	Alternate Function	
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P00 the threshold level can be specified.	Input port	(TI05)/(TO05)/INTP9/SCK20	
P01				(TI04)/(TO04)	
P02				(TI06)/(TO06)	
P03				(RTC1HZ)	
P04				INTP15	
P05					
P06					
P07					
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJIO0/SCK10/SCL10/LTXD1/CTXD0	
P11				TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1/LRXD1/CRXD0	
P12				TI11/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3	
P13				TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0	
P14				TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0	
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ	
P16				TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD	
P17				TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3	
P20	I/O	Port 2 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P20, P21, P24, and P25, the threshold level can be specified.	Input port	(SCK20)	
P21				(SI20)/(RXD2)	
P22				(SO20)/(TXD2)	
P23					
P24				(SCK21)	
P25				(SI21)	
P26				(SO21)	
P27					
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32 and P35 to P37, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30, and P37 the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0	
P31				TI14/TO14/STOPST/(INTP2)	
P32				TI16/TO16/INTP7	
P33				Analog input port	AVREFP/ANI0
P34					AVREFM/ANI1
P35				Input port	
P36					(CTXD1)
P37					(CRXD1)
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P43, the threshold level can be specified.	Input port	TOOL0	
P41				TI10/TO10/TRJIO0/VCOUT0/SNZOUT2	
P42				(LTXD0)	
P43				(LRXD0)	
P44				(TI07)/(TO07)	
P45				(TI10)/(TO10)	
P46				(TI12)/(TO12)	
P47				INTP13	

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

(2/3)

Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5 Input of P54 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. For input to P50 and P52 to P54, the threshold level can be specified.	Input port	( $\overline{\text{SSI01}}$ )/( $\overline{\text{INTP3}}$ )/( $\overline{\text{IERXD}}$ )
P51				( $\text{SO01}$ )/ $\overline{\text{INTP11}}$ /( $\overline{\text{IETXD}}$ )
P52				( $\overline{\text{SCK01}}$ )/( $\overline{\text{STOPST}}$ )
P53				( $\text{SI01}$ )/ $\overline{\text{INTP10}}$
P54				( $\text{T111}$ )/( $\text{TO11}$ )/ $\overline{\text{SSI10}}$
P55				( $\text{T113}$ )/( $\text{TO13}$ )
P56				( $\text{T115}$ )/( $\text{TO15}$ )/( $\text{SNZOUT1}$ )
P57				( $\text{T117}$ )/( $\text{TO17}$ )/( $\text{SNZOUT0}$ )
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	( $\overline{\text{SCK00}}$ )/( $\overline{\text{SCL00}}$ )/ $\overline{\text{CRXD1}}$ / $\overline{\text{IERXD}}$
P61				( $\text{SI00}$ )/( $\text{SDA00}$ )/( $\text{RXD0}$ )/ $\overline{\text{CTXD1}}$ / $\overline{\text{IETXD}}$
P62				( $\text{SO00}$ )/( $\text{TXD0}$ )/ $\overline{\text{SCLA0}}$
P63				( $\overline{\text{SSI00}}$ )/ $\overline{\text{SDAA0}}$
P64				( $\text{T114}$ )/( $\text{TO14}$ )/( $\text{SNZOUT3}$ )
P65				( $\text{T116}$ )/( $\text{TO16}$ )/( $\text{SNZOUT2}$ )
P66				( $\text{TI00}$ )/( $\text{TO00}$ )
P67				( $\text{TI02}$ )/( $\text{TO02}$ )
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. P70 to P74 can be set to analog input. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Analog input port	ANI26/ $\overline{\text{KR0}}$ / $\overline{\text{T115}}$ / $\overline{\text{TO15}}$ / $\overline{\text{INTP8}}$ / $\overline{\text{SI11}}$ / $\overline{\text{SDA11}}$ / $\overline{\text{SNZOUT4}}$
P71				ANI27/ $\overline{\text{KR1}}$ / $\overline{\text{T117}}$ / $\overline{\text{TO17}}$ / $\overline{\text{INTP6}}$ / $\overline{\text{SCK11}}$ / $\overline{\text{SCL11}}$ / $\overline{\text{SNZOUT5}}$
P72				ANI28/ $\overline{\text{KR2}}$ /( $\overline{\text{CTXD0}}$ )/ $\overline{\text{SO11}}$ / $\overline{\text{SNZOUT6}}$
P73				ANI29/ $\overline{\text{KR3}}$ /( $\overline{\text{CRXD0}}$ )/ $\overline{\text{SSI11}}$ / $\overline{\text{SNZOUT7}}$
P74			ANI30/ $\overline{\text{KR4}}$ /( $\overline{\text{SO10}}$ )/( $\overline{\text{TXD1}}$ )	
P75			Input port	KR5/( $\text{SI10}$ )/( $\text{RXD1}$ )
P76				KR6/( $\overline{\text{SCK10}}$ )
P77				KR7/( $\overline{\text{SSI10}}$ )/ $\overline{\text{INTP12}}$
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2/ $\overline{\text{ANO0}}$
P81				ANI3/ $\overline{\text{IVCMP00}}$
P82				ANI4/ $\overline{\text{IVCMP01}}$
P83				ANI5/ $\overline{\text{IVCMP02}}$
P84				ANI6/ $\overline{\text{IVCMP03}}$
P85				ANI7/ $\overline{\text{IVREF0}}$
P86				ANI8
P87				ANI9
P90	I/O	Port 9 P90 to P97 can be set to analog input.	Analog input port	ANI10
P91				ANI11
P92				ANI12
P93				ANI13
P94				ANI14
P95				ANI15
P96				ANI16
P97				ANI17
P100	I/O	Port 10 P100 to P105 can be set to analog input. For P106 and P107, use of an on-chip pull-up resistor can be specified by a software setting. For input to P107, the threshold level can be specified.	Analog input port	ANI18
P101				ANI19
P102				ANI20
P103				ANI21
P104				ANI22
P105			ANI23	
P106			Input port	( $\overline{\text{LTXD1}}$ )
P107				( $\overline{\text{LRXD1}}$ )

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

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Function Name	I/O	Function	After Reset	Alternate Function
P110	I/O	Port 11 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	T120/TO20
P111				T121/TO21
P112				T122/TO22
P113				T123/TO23
P114				T124/TO24
P115				T125/TO25
P116				T126/TO26
P117				T127/TO27
P120	I/O	Port 12 Input of P125 can be set to TTL input buffer. P120 and P125 can be set to analog input. For P120 and P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting. Output from P120 can be set to N-ch open-drain output. For input to P125, the threshold level can be specified.	Analog input port	ANI25/TI07/TO07/TRDIOD0/SO01/INTP4
P121			Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P125	I/O		Analog input port	ANI24/TI03/TO03/TRDIOD0/SSI01/INTP1/SNZOUT1
P126			Input port	(TI01)/(TO01)
P127				(TI03)/(TO03)
P130	Output	Port 13	Output port	RESOUT
P131	I/O	For P131 to P136, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP14
P132				
P133				
P134				
P135				
P136				
P137			Input	
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0/(TI20)/(TO20)
P141				(TI21)/(TO21)
P142				(TI22)/(TO22)
P143				(TI23)/(TO23)
P144				(TI24)/(TO24)
P145				(TI25)/(TO25)
P146				(TI26)/(TO26)
P147				(TI27)/(TO27)
P150				I/O
P151	(SO11)/SO21			
P152	(SI11)/SI21			
P153	(SCK11)/SCK21			
P154	(SNZOUT7)/LRXD2			
P155	(SNZOUT6)/LTXD2			
P156	(SNZOUT5)/SI20/RXD2			
P157	(SNZOUT4)/SO20/TXD2			
P160	I/O	Port 16 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	
P161				
P162				
P163				
P164				
P165				
P166				
P167				

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

## 2.1.2 RL78/F15 100-pin products

(1/3)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P00, the threshold level can be specified.	Input port	(TI05)/(TO05)/INTP9/SCK20
P01				(TI04)/(TO04)
P02				(TI06)/(TO06)
P03				(RTC1HZ)
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJ00/SCK10/SCL10/LTXD1/CTXD0
P11				TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1/LRXD1/CRXD0
P12				TI11/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3
P13				TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
P14				TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ
P16				TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
P17				TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30 the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0
P31				TI14/TO14/STOPST/(INTP2)
P32				TI16/TO16/INTP7
P33			Analog input port	AVREFP/ANI0
P34				AVREFM/ANI1
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P43, the threshold level can be specified.	Input port	TOOL0
P41				TI10/TO10/TRJIO0/VCOUT0/SNZOUT2
P42				(LTXD0)
P43				(LRXD0)
P44				(TI07)/(TO07)
P45				(TI10)/(TO10)
P46				(TI12)/(TO12)
P47				INTP13
P50	I/O	Port 5 Input of P54 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. For input to P50 and P52 to P54, the threshold level can be specified.	Input port	(SSI01)/(INTP3)/(IERXD)
P51				(SO01)/INTP11/(IETXD)
P52				(SCK01)/(STOPST)
P53				(SI01)/INTP10
P54				(TI11)/(TO11)/SSI10
P55				(TI13)/(TO13)
P56				(TI15)/(TO15)/(SNZOUT1)
P57				(TI17)/(TO17)/(SNZOUT0)

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

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Function Name	I/O	Function	After Reset	Alternate Function
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	(SCK00)/(SCL00)/CRXD1/IERXD
P61				(SI00)/(SDA00)/(RXD0)/CTXD1/IETXD
P62				(SO00)/(TXD0)/SCLA0
P63				(SSI00)/SDAA0
P64				(TI14)/(TO14)/(SNZOUT3)
P65				(TI16)/(TO16)/(SNZOUT2)
P66				(TI00)/(TO00)
P67				(TI02)/(TO02)
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. P70 to P74 can be set to analog input. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Analog input port	ANI26/KR0/TI15/TO15/INTP8/SI11/SDA11/SNZOUT4
P71				ANI27/KR1/TI17/TO17/INTP6/SCK11/SCL11/SNZOUT5
P72				ANI28/KR2/(CTXD0)/SO11/SNZOUT6
P73				ANI29/KR3/(CRXD0)/SSI11/SNZOUT7
P74			ANI30/KR4/(SO10)/(TXD1)	Input port
P75			KR5/(SI10)/(RXD1)	
P76			KR6/(SCKT0)	
P77			KR7/(SSI10)/INTP12	
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2/AN00
P81				ANI3/IVCMP00
P82				ANI4/IVCMP01
P83				ANI5/IVCMP02
P84				ANI6/IVCMP03
P85				ANI7/IVREF0
P86				ANI8
P87				ANI9
P90	I/O	Port 9 P90 to P97 can be set to analog input.	Analog input port	ANI10
P91				ANI11
P92				ANI12
P93				ANI13
P94				ANI14
P95				ANI15
P96				ANI16
P97				ANI17
P100	I/O	Port 10 P100 to P105 can be set to analog input. For P106 and P107, use of an on-chip pull-up resistor can be specified by a software setting. For input to P107, the threshold level can be specified.	Analog input port	ANI18
P101				ANI19
P102				ANI20
P103				ANI21
P104				ANI22
P105				ANI23
P106			Input port	(LTXD1)
P107				(LRXD1)
P120	I/O	Port 12 Input of P125 can be set to TTL input buffer. P120 and P125 can be set to analog input. For P120 and P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting. Output from P120 can be set to N-ch open-drain output. For input to P125, the threshold level can be specified.	Analog input port	ANI25/TI07/TO07/TRDIOD0/SO01/INTP4
P121			Input port	X1
P122				X2/EXCLK
P123				XT1
P124	XT2/EXCLKS	Analog input port		
P125	ANI24/TI03/TO03/TRDIOD0/SSI07/INTP1/SNZOUT1			
P126	Input port		(TI01)/(TO01)	
P127		(TI03)/(TO03)		

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

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Function Name	I/O	Function	After Reset	Alternate Function
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0
P150	I/O	Port 15 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P150, P152 to P154 and P156, the threshold level can be specified.	Input port	( $\overline{\text{SSI11}}$ )
P151				(SO11)/SO21
P152				(SI11)/SI21
P153				( $\overline{\text{SCK11}}$ )/SCK21
P154				(SNZOUT7)/LRXD2
P155				(SNZOUT6)/LTXD2
P156				(SNZOUT5)/SI20/RXD2
P157				(SNZOUT4)/SO20/TXD2

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

2.1.3 RL78/F15 80-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P01				(TI04)/(TO04)
P02				(TI06)/(TO06)
P03				(RTC1HZ)
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJ00/SCK10/SCL10/LTXD0/CTXD0
P11				TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1/LRXD1/CRXD0
P12				TI11/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3
P13				TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
P14				TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ
P16				TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
P17				TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30 the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0
P31				TI14/TO14/STOPST/(INTP2)
P32				TI16/TO16/INTP7
P33			Analog input port	AVREFP/ANI0
P34				AVREFM/ANI1
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P43, the threshold level can be specified.	Input port	TOOL0
P41				TI10/TO10/TRJIO0/VCOUT0/SNZOUT2
P42				(LTXD0)
P43				(LRXD0)
P44				(TI07)/(TO07)
P45				(TI10)/(TO10)
P46				(TI12)/(TO12)
P47				INTP13
P50	I/O	Port 5 Input of P54 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. For input to P50 and P52 to P54, the threshold level can be specified.	Input port	(SSI01)/(INTP3)/(IERXD)
P51				(SO01)/INTP11/(IETXD)
P52				(SCK01)/(STOPST)
P53				(SI01)/INTP10
P54				(TI11)/(TO11)/SSI10
P55				(TI13)/(TO13)
P56				(TI15)/(TO15)/(SNZOUT1)
P57				(TI17)/(TO17)/(SNZOUT0)

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

(2/2)

Function Name	I/O	Function	After Reset	Alternate Function	
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	(SCK00)/(SCL00)/CRXD1/IERXD	
P61				(SI00)/(SDA00)/(RXD0)/CTXD1/IETXD	
P62				(SO00)/(TXD0)/SCLA0	
P63				(SSI00)/SDAA0	
P64				(TI14)/(TO14)/(SNZOUT3)	
P65				(TI16)/(TO16)/(SNZOUT2)	
P66				(TI00)/(TO00)	
P67				(TI02)/(TO02)	
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. P70 to P74 can be set to analog input. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Analog input port	ANI26/KR0/TI15/TO15/INTP8/SI11/SDA11/SNZOUT4	
P71				ANI27/KR1/TI17/TO17/INTP6/SCK11/SCL11/SNZOUT5	
P72				ANI28/KR2/(CTXD0)/SO11/SNZOUT6	
P73				ANI29/KR3/(CRXD0)/SSI11/SNZOUT7	
P74			ANI30/KR4/(SO10)/(TXD1)		
P75			Input port	KR5/(SI10)/(RXD1)	
P76				KR6/(SCK10)	
P77				KR7/(SSI10)/INTP12	
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2/AN00	
P81				ANI3/IVCMP00	
P82				ANI4/IVCMP01	
P83				ANI5/IVCMP02	
P84				ANI6/IVCMP03	
P85				ANI7/IVREF0	
P86				ANI8	
P87				ANI9	
P90	I/O	Port 9 P90 to P97 can be set to analog input.	Analog input port	ANI10	
P91				ANI11	
P92				ANI12	
P93				ANI13	
P94				ANI14	
P95				ANI15	
P96				ANI16	
P97				ANI17	
P120	I/O	Port 12 Input of P125 can be set to TTL input buffer. P120 and P125 can be set to analog input. For P120, P125 and P126 use of an on-chip pull-up resistor can be specified by a software setting. Output from P120 can be set to N-ch open-drain output. For input to P125, the threshold level can be specified.	Analog input port	ANI25/TI07/TO07/TRDIOD0/SO01/INTP4	
P121				Input port	X1
P122					X2/EXCLK
P123					XT1
P124	I/O		Analog input port	XT2/EXCLKS	
P125				ANI24/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1	
P126			Input port	(TI01)/(TO01)	
P130	Output	Port 13	Output port	RESOUT	
P137	Input		Input port	INTP0	
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0	

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

2.1.4 RL78/F15 64-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	T113/TO13/TRJ00/SCK10/SCL10/LTXD1/CTXD0
P11				T112/TO12/(TRDIOB0)/SI10/SDA10/RXD1/LRXD1/CRXD0
P12				T111/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3
P13				T104/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
P14				T106/TO06/TRDIOC0/SCK01/SCL01/LRXD0
P15				T105/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ
P16				T102/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
P17				T100/TO00/TRDIOB1/SCK00/SCL00/INTP3
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30 the threshold level can be specified.	Input port	T101/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0
P31				T114/TO14/STOPST/(INTP2)
P32				T116/TO16/INTP7
P33			Analog input port	AVREFP/ANI0
P34				AVREFM/ANI1
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P43, the threshold level can be specified.	Input port	TOOL0
P41				T110/TO10/TRJIO0/VCOUT0/SNZOUT2
P42				(LTXD0)
P43				(LRXD0)
P50	I/O	Port 5 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P50, P52 and P53 the threshold level can be specified.	Input port	(SSI01)/(INTP3)/(IERXD)
P51				(SO01)/INTP11/(IETXD)
P52				(SCK01)/(STOPST)
P53				(SI01)/INTP10
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	(SCK00)/(SCL00)/CRXD1/IERXD
P61				(SI00)/(SDA00)/(RXD0)/CTXD1/IETXD
P62				(SO00)/(TXD0)/SCLA0
P63				(SSI00)/SDAA0
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. P70 can be set to analog input. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Analog input port	ANI26/KR0/TI15/TO15/INTP8/SI11/SDA11/SNZOUT4
P71				KR1/TI17/TO17/INTP6/SCK11/SCL11/SNZOUT5
P72				KR2/(CTXD0)/SO11/SNZOUT6
P73				KR3/(CRXD0)/SSI11/SNZOUT7
P74				KR4/(SO10)/(TXD1)
P75			Input port	KR5/(SI10)/(RXD1)
P76				KR6/(SCK10)
P77				KR7/(SSI10)/INTP12

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2/ANO0
P81				ANI3/IVCMP00
P82				ANI4/IVCMP01
P83				ANI5/IVCMP02
P84				ANI6/IVCMP03
P85				ANI7/IVREF0
P86				ANI8
P87				ANI9/(KR0)
P90	I/O	Port 9 P90 to P96 can be set to analog input.	Analog input port	ANI10/(KR1)
P91				ANI11/(KR2)
P92				ANI12/(KR3)
P93				ANI13/(KR4)
P94				ANI14/(KR5)
P95				ANI15/(KR6)
P96				ANI16/(KR7)
P120				I/O
P121	Input	Input port	X1	
P122			X2/EXCLK	
P123			XT1	
P124			XT2/EXCLKS	
P125	I/O	Analog input port	ANI24/TI03/TO03/TRDIOD0/ SSI01/INTP1/SNZOUT1	
P126		Input port	(TI01)/(TO01)	
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

2.1.5 RL78/F15 48-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	T113/TO13/TRJ00/SCK10/SCL10/LTXD1/CTXD0
P11				T112/TO12/(TRDIOB0)/SI10/SDA10/RXD1/LRXD1/CRXD0
P12				T111/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3
P13				T104/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
P14				T106/TO06/TRDIOC0/SCK01/SCL01/LRXD0
P15				T105/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ
P16				T102/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
P17				T100/TO00/TRDIOB1/SCK00/SCL00/INTP3
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30 the threshold level can be specified.	Input port	T101/TO01/TRDIOD1/SSI00/INTP2/SNZOUT0
P31				T114/TO14/STOPST/(INTP2)
P32				T116/TO16/INTP7
P33			Analog input port	AVREFP/ANI0
P34				AVREFM/ANI1
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				T110/TO10/TRJIO0/VCOUT0/SNZOUT2
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	(SCK00)/(SCL00)/CRXD1/IERXD
P61				(SI00)/(SDA00)/(RXD0)/CTXD1/IETXD
P62				(SO00)/(TXD0)/SCLA0
P63				(SSI00)/SDAA0
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. P70 to P72 can be set to analog input. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, and P73 the threshold level can be specified.	Analog input port	ANI26/KR0/TI15/TO15/INTP8/SI11/SDA11/SNZOUT4
P71				ANI27/KR1/TI17/TO17/INTP6/SCK11/SCL11/SNZOUT5
P72				ANI28/KR2/(CTXD0)/SO11/SNZOUT6
P73				KR3/(CRXD0)/SI11/SNZOUT7
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2/ANO0
P81				ANI3/IVCMP00
P82				ANI4/IVCMP01
P83				ANI5/(KR0)/IVCMP02
P84				ANI6/(KR1)/IVCMP03
P85				ANI7/(KR2)/IVREF0
P86				ANI8/(KR3)
P87				ANI9/(KR4)
P90	I/O	Port 9 P90 to P92 can be set to analog input.	Analog input port	ANI10/(KR5)
P91				ANI11/(KR6)
P92				ANI12/(KR7)

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P120	I/O	Port 12 Input of P125 can be set to TTL input buffer. P120 and P125 can be set to analog input. For P120 and P125 use of an on-chip pull-up resistor can be specified by a software setting. Output from P120 can be set to N-ch open-drain output. For input to P125, the threshold level can be specified.	Analog input port	ANI25/TI07/TO07/TRDIOD0/SO01/INTP4
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P125	I/O	Analog input port	ANI24/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1	
P126	Input port		(TI01)/(TO01)	
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0

**Remark** Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

## 2.1.6 Pins for each product (pins other than port pins)

This subchapter shows the pins other than the ports shown in tables 2-2.

√ indicates the pin that is provided in the product and — indicates the pin that is not provided.

Table 2-2. List of RL78/F15 Pins Other than Port Pins (1/5)

Pin Function	I/O	Function	Pin Count				
			144-pin	100-pin	80-pin	64-pin	48-pin
ANI0	Input	A/D converter analog input (V <sub>DD</sub> connection)	√	√	√	√	√
ANI1	Input		√	√	√	√	√
ANI2	Input		√	√	√	√	√
ANI3	Input		√	√	√	√	√
ANI4	Input		√	√	√	√	√
ANI5	Input		√	√	√	√	√
ANI6	Input		√	√	√	√	√
ANI7	Input		√	√	√	√	√
ANI8	Input		√	√	√	√	√
ANI9	Input		√	√	√	√	√
ANI10	Input		√	√	√	√	√
ANI11	Input		√	√	√	√	√
ANI12	Input		√	√	√	√	√
ANI13	Input		√	√	√	√	—
ANI14	Input		√	√	√	√	—
ANI15	Input		√	√	√	√	—
ANI16	Input		√	√	√	√	—
ANI17	Input		√	√	√	—	—
ANI18	Input		√	√	—	—	—
ANI19	Input		√	√	—	—	—
ANI20	Input		√	√	—	—	—
ANI21	Input		√	√	—	—	—
ANI22	Input		√	√	—	—	—
ANI23	Input	√	√	—	—	—	
ANI24	Input	A/D converter analog input (EV <sub>DD</sub> connection)	√	√	√	√	√
ANI25	Input		√	√	√	√	√
ANI26	Input		√	√	√	√	√
ANI27	Input		√	√	√	—	√
ANI28	Input		√	√	√	—	√
ANI29	Input		√	√	√	—	—
ANI30	Input		√	√	√	—	—
IVCMP00	Input	Comparator analog voltage input	√	√	√	√	√
IVCMP01	Input		√	√	√	√	√
IVCMP02	Input		√	√	√	√	√
IVCMP03	Input		√	√	√	√	√
IVREF0	Input	Comparator reference voltage input	√	√	√	√	√

Table 2-2. List of RL78/F15 Pins Other than Port Pins (2/5)

Pin Function	I/O	Function	Pin Count				
			144-pin	100-pin	80-pin	64-pin	48-pin
KR0	Input	Key interrupt input	√	√	√	√	√
KR1	Input		√	√	√	√	√
KR2	Input		√	√	√	√	√
KR3	Input		√	√	√	√	√
KR4	Input		√	√	√	√	√
KR5	Input		√	√	√	√	√
KR6	Input		√	√	√	√	√
KR7	Input		√	√	√	√	√
ANO0	Output	D/A converter output	√	√	√	√	√
VCOUT0	Output	Comparator output	√	√	√	√	√
TI00	Input	16-bit timer 00 input	√	√	√	√	√
TI01	Input	16-bit timer 01 input (8-bit mode available)	√	√	√	√	√
TI02	Input	16-bit timer 02 input	√	√	√	√	√
TI03	Input	16-bit timer 03 input (8-bit mode available)	√	√	√	√	√
TI04	Input	16-bit timer 04 input	√	√	√	√	√
TI05	Input	16-bit timer 05 input	√	√	√	√	√
TI06	Input	16-bit timer 06 input	√	√	√	√	√
TI07	Input	16-bit timer 07 input	√	√	√	√	√
TI10	Input	16-bit timer 10 input	√	√	√	√	√
TI11	Input	16-bit timer 11 input (8-bit mode available)	√	√	√	√	√
TI12	Input	16-bit timer 12 input	√	√	√	√	√
TI13	Input	16-bit timer 13 input (8-bit mode available)	√	√	√	√	√
TI14	Input	16-bit timer 14 input	√	√	√	√	√
TI15	Input	16-bit timer 15 input	√	√	√	√	√
TI16	Input	16-bit timer 16 input	√	√	√	√	√
TI17	Input	16-bit timer 17 input	√	√	√	√	√
TI20	Input	16-bit timer 20 input	√	—	—	—	—
TI21	Input	16-bit timer 21 input	√	—	—	—	—
TI22	Input	16-bit timer 22 input	√	—	—	—	—
TI23	Input	16-bit timer 23 input	√	—	—	—	—
TI24	Input	16-bit timer 24 input	√	—	—	—	—
TI25	Input	16-bit timer 25 input	√	—	—	—	—
TI26	Input	16-bit timer 26 input	√	—	—	—	—
TI27	Input	16-bit timer 27 input	√	—	—	—	—
TO00	Output	16-bit timer 00 output	√	√	√	√	√
TO01	Output	16-bit timer 01 output (8-bit mode available)	√	√	√	√	√
TO02	Output	16-bit timer 02 output	√	√	√	√	√
TO03	Output	16-bit timer 03 output (8-bit mode available)	√	√	√	√	√
TO04	Output	16-bit timer 04 output	√	√	√	√	√
TO05	Output	16-bit timer 05 output	√	√	√	√	√
TO06	Output	16-bit timer 06 output	√	√	√	√	√
TO07	Output	16-bit timer 07 output	√	√	√	√	√
TO10	Output	16-bit timer 10 output	√	√	√	√	√

Table 2-2. List of RL78/F15 Pins Other than Port Pins (3/5)

Pin Function	I/O	Function	Pin Count				
			144pin	100-pin	80-pin	64-pin	48-pin
TO11	Output	16-bit timer 11 output (8-bit mode available)	√	√	√	√	√
TO12	Output	16-bit timer 12 output	√	√	√	√	√
TO13	Output	16-bit timer 13 output (8-bit mode available)	√	√	√	√	√
TO14	Output	16-bit timer 14 output	√	√	√	√	√
TO15	Output	16-bit timer 15 output	√	√	√	√	√
TO16	Output	16-bit timer 16 output	√	√	√	√	√
TO17	Output	16-bit timer 17 output	√	√	√	√	√
TO20	Output	16-bit timer 20 output	√	—	—	—	—
TO21	Output	16-bit timer 21 output	√	—	—	—	—
TO22	Output	16-bit timer 22 output	√	—	—	—	—
TO23	Output	16-bit timer 23 output	√	—	—	—	—
TO24	Output	16-bit timer 24 output	√	—	—	—	—
TO25	Output	16-bit timer 25 output	√	—	—	—	—
TO26	Output	16-bit timer 26 output	√	—	—	—	—
TO27	Output	16-bit timer 27 output	√	—	—	—	—
TRJIO0	I/O	Timer RJ input/output	√	√	√	√	√
TRJO0	Output	Timer RJ output	√	√	√	√	√
TRDCLK0	Input	Timer RD external clock input	√	√	√	√	√
TRDIOA0	I/O	Timer RD0 input/output	√	√	√	√	√
TRDIOB0	I/O		√	√	√	√	√
TRDIOC0	I/O		√	√	√	√	√
TRDIOD0	I/O		√	√	√	√	√
TRDIOA1	I/O	Timer RD1 input/output	√	√	√	√	√
TRDIOB1	I/O		√	√	√	√	√
TRDIOC1	I/O		√	√	√	√	√
TRDIOD1	I/O		√	√	√	√	√
RXD0	Input	Serial data input to UART0	√	√	√	√	√
RXD1	Input	Serial data input to UART1	√	√	√	√	√
RXD2	Input	Serial data input to UART2	√	√	—	—	—
TXD0	Output	Serial data output from UART0	√	√	√	√	√
TXD1	Output	Serial data output from UART1	√	√	√	√	√
TXD2	Output	Serial data output from UART2	√	√	—	—	—
SCLA0	I/O	Clock input/output for IICA0	√	√	√	√	√
SCL00	Output	Clock output from simplified I <sup>2</sup> C	√	√	√	√	√
SCL01	Output		√	√	√	√	√
SCL10	Output		√	√	√	√	√
SCL11	Output		√	√	√	√	√
SDAA0	I/O	Serial data input/output for IICA0	√	√	√	√	√
SDA00	I/O	Serial data input/output for simplified I <sup>2</sup> C	√	√	√	√	√
SDA01	I/O		√	√	√	√	√
SDA10	I/O		√	√	√	√	√
SDA11	I/O		√	√	√	√	√
SCK00	I/O	Clock input/output for CSI00	√	√	√	√	√
SCK01	I/O	Clock input/output for CSI01	√	√	√	√	√

**Table 2-2. List of RL78/F15 Pins Other than Port Pins (4/5)**

Pin Function	I/O	Function	Pin Count				
			144-pin	100-pin	80-pin	64-pin	48-pin
SCK10	I/O	Clock input/output for CSI10	√	√	√	√	√
SCK11	I/O	Clock input/output for CSI11	√	√	√	√	√
SCK20	I/O	Clock input/output for CSI20	√	√	—	—	—
SCK21	I/O	Clock input/output for CSI21	√	√	—	—	—
SI00	Input	Serial data input to CSI00	√	√	√	√	√
SI01	Input	Serial data input to CSI01	√	√	√	√	√
SI10	Input	Serial data input to CSI10	√	√	√	√	√
SI11	Input	Serial data input to CSI11	√	√	√	√	√
SI20	Input	Serial data input to CSI20	√	√	—	—	—
SI21	Input	Serial data input to CSI21	√	√	—	—	—
SO00	Output	Serial data output from CSI00	√	√	√	√	√
SO01	Output	Serial data output from CSI01	√	√	√	√	√
SO10	Output	Serial data output from CSI10	√	√	√	√	√
SO11	Output	Serial data output from CSI11	√	√	√	√	√
SO20	Output	Serial data output from CSI20	√	√	—	—	—
SO21	Output	Serial data output from CSI21	√	√	—	—	—
SSI00	Input	Slave select input to CSI00 (SPI00)	√	√	√	√	√
SSI01	Input	Slave select input to CSI01 (SPI01)	√	√	√	√	√
SSI10	Input	Slave select input to CSI10 (SPI10)	√	√	√	√	—
SSI11	Input	Slave select input to CSI11 (SPI11)	√	√	√	√	√
CRXD0	Input	Serial data input to CAN	√	√	√	√	√
CRXD1			√	√	√	√	√
CTXD0	Output	Serial data output from CAN	√	√	√	√	√
CTXD1			√	√	√	√	√
LRXD0	Input	Serial data input to LIN	√	√	√	√	√
LRXD1	Input		√	√	√	√	√
LRXD2	Input		√	√	—	—	—
LTXD0	Output	Serial data output from LIN	√	√	√	√	√
LTXD1	Output		√	√	√	√	√
LTXD2	Output		√	√	—	—	—
IERXD	Input	Serial data input of IEBus	√	√	√	√	√
IETXD	Output	Serial data output of IEBus	√	√	√	√	√
INTP0	Input	External interrupt input	√	√	√	√	√
INTP1	Input		√	√	√	√	√
INTP2	Input		√	√	√	√	√
INTP3	Input		√	√	√	√	√
INTP4	Input		√	√	√	√	√
INTP5	Input		√	√	√	√	√
INTP6	Input		√	√	√	√	√
INTP7	Input		√	√	√	√	√
INTP8	Input		√	√	√	√	√
INTP9	Input		√	√	√	√	√
INTP10	Input		√	√	√	√	—
INTP11	Input		√	√	√	√	—

Table 2-2. List of RL78/F15 Pins Other than Port Pins (5/5)

Pin Function	I/O	Function	Pin Count				
			144-pin	100-pin	80-pin	64-pin	48-pin
INTP12	Input	External interrupt input	√	√	√	√	—
INTP13	Input		√	√	√	—	—
INTP14	Input		√	—	—	—	—
INTP15	Input		√	—	—	—	—
PCLBUZ0	Output	Clock output/buzzer output 0	√	√	√	√	√
RESOUT	Output	Reset output	√	√	√	√	√
STOPST	Output	STOP status output	√	√	√	√	√
SNZOUT0	Output	SNOOZE status output	√	√	√	√	√
SNZOUT1	Output		√	√	√	√	√
SNZOUT2	Output		√	√	√	√	√
SNZOUT3	Output		√	√	√	√	√
SNZOUT4	Output		√	√	√	√	√
SNZOUT5	Output		√	√	√	√	√
SNZOUT6	Output		√	√	√	√	√
SNZOUT7	Output		√	√	√	√	√
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output	√	√	√	√	√
EXCLK	Input	External clock input for main system clock	√	√	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	√	√	√	√
X1	—	Resonator connection for main system clock	√	√	√	√	√
X2	—		√	√	√	√	√
XT1 <sup>Note 3</sup>	—	Resonator connection for subsystem clock	√	√	√	√	√
XT2 <sup>Note 3</sup>	—		√	√	√	√	√
RESET	Input	External reset input	√	√	√	√	√
REGC	—	Regulator output stabilization capacitance connection for internal operation. Connect to V <sub>SS</sub> via the capacitor (0.47 to 1 μF).	√	√	√	√	√
V <sub>DD</sub>	—	Positive power supply for the P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137, and RESET pins	√	√	√	√	√
EV <sub>DD0</sub>	—	Positive power supply for the pins that are not connected to V <sub>DD</sub>	√	√	√	√	—
EV <sub>DD1</sub>	—		√	√	—	—	—
AV <sub>REFP</sub>	Input	A/D converter reference voltage (+ side) input	√	√	√	√	√
AV <sub>REFM</sub>	Input	A/D converter reference voltage (- side) input	√	√	√	√	√
V <sub>SS</sub>	—	Ground potential for the P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137, and RESET pins	√	√	√	√	√
EV <sub>SS0</sub>	—	Ground potential for the pins that are not connected to V <sub>SS</sub>	√	√	√	√	—
EV <sub>SS1</sub>	—		√	√	—	—	—
TOOLRXD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√	√	√
TOOLTXD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√	√	√
TOOL0	I/O	Data input/output for flash memory programmer/debugger	√	√	√	√	√

### 3. ELECTRICAL SPECIFICATIONS (GRADE L)

- Cautions**
1. RL78/F15 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an EV<sub>DD0</sub>, EV<sub>DD1</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub> pin, replace EV<sub>DD0</sub> and EV<sub>DD1</sub> with V<sub>DD</sub>, or replace EV<sub>SS0</sub> and EV<sub>SS1</sub> with V<sub>SS</sub>.
  3. The pins mounted depending on the product. For details, refer to 1.5 Pin Configurations and 2.1 Pin Function List.

## 3.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$		-0.5 to +6.5	V
	$EV_{DD0}$ , $EV_{DD1}$	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	$V_{SS}$		-0.5 to +0.3	V
	$EV_{SS0}$ , $EV_{SS1}$	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	$V_{IREGC}$	REGC	-0.3 to +2.8 and -0.3 to $V_{DD}+0.3$ <sup>Note 1</sup>	V
Input voltage	$V_{I1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	-0.3 to $EV_{DD0} = EV_{DD1} + 0.3$ and -0.3 to $V_{DD}+0.3$ <sup>Note 2</sup>	V
	$V_{I2}$	P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137, RESET	-0.3 to $V_{DD}+0.3$ <sup>Note 2</sup>	V
Output voltage	$V_{O1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	-0.3 to $EV_{DD0} = EV_{DD1} + 0.3$ and -0.3 to $V_{DD}+0.3$ <sup>Note 2</sup>	V
	$V_{O2}$	P33, P34, P80 to P87, P90 to P97, P100 to P105	-0.3 to $V_{DD}+0.3$	V
Analog input voltage	$V_{AI1}$	ANI24 to ANI30	-0.3 to $EV_{DD0} = EV_{DD1} + 0.3$ and -0.3 to $AV_{REF(+)}+0.3$ <sup>Notes 2, 3</sup>	V
	$V_{AI2}$	ANI0 to ANI23	-0.3 to $V_{DD}+0.3$ and -0.3 to $AV_{REF(+)}+0.3$ <sup>Notes 2, 3</sup>	V

**Notes 1.** Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu$ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** For pins to be used in A/D conversion, the voltage should not exceed the value  $AV_{REF(+)} + 0.3$ .

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I <sub>OH1</sub>	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	-40	mA
		Total of all pins -170 mA	P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167	-70	mA
			P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157	-100	mA
	I <sub>OH2</sub>	Per pin	P33, P34, P80 to P87, P90 to P97, P100 to P105	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	I <sub>OL1</sub>	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	40
Total of all pins 170 mA			P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167	70	mA
			P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157	100	mA
I <sub>OL2</sub>		Per pin	P33, P34, P80 to P87, P90 to P97, P100 to P105	1	mA
		Total of all pins		5	mA
Operating ambient temperature		T <sub>A</sub>	In normal operation mode		-40 to +105
	In flash memory programming mode				
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 3.2 Oscillator Characteristics

#### 3.2.1 Main System Clock Oscillator Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator/ Crystal resonator		X1 clock oscillation frequency (fx)	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz

**Cautions 1.** When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as Vss.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

**2.** Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Customers are also requested to adequately evaluate the oscillation on their system. Determine the X1 clock oscillation stabilization time using the oscillation stabilization time of the oscillation stabilization time counter status register (OSTC) and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

### 3.2.2 On-chip Oscillator Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Oscillators	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency <sup>Note</sup>	$f_{\text{IH}}$		1		64	MHz
High-speed on-chip oscillator clock frequency accuracy	-		-2		+2	%
Low-speed on-chip oscillator clock frequency	$f_{\text{IL}}$ , $f_{\text{WDT}}$			15		kHz
Low-speed on-chip oscillator clock frequency accuracy	-		-15		+15	%

**Note** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/020C2H) and bits 0 to 2 of the HOCODIV register.

3.2.3 Subsystem Clock Oscillator Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Resonator	Recommended Circuit	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency ( $f_{XT}$ )	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	29.0	32.768	35.0	kHz

**Cautions 1.** When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
  - Do not cross the wiring with the other signal lines.
  - Do not route the wiring near a signal line through which a high fluctuating current flows.
  - Always make the ground point of the oscillator capacitor the same potential as Vss.
  - Do not ground the capacitor to a ground pattern through which a high current flows.
  - Do not fetch signals from the oscillator.
- 2.** The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption and thus required to be adequately evaluated on the system. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

## 3.2.4 PLL Circuit Characteristics

(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ E<sub>VDD0</sub> = E<sub>VDD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = E<sub>VSS1</sub> = 0 V)

Resonator	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
PLL input enable clock frequency <sup>Note 1</sup>	f <sub>PLLI</sub>	PLLMUL = 0	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
		PLLMUL = 1	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
PLL output frequency (center value)	f <sub>PLL</sub>	PLLMUL = 0	PLLDIV0 = 0	f <sub>PLLI</sub> × 12/2		MHz	
			PLLDIV0 = 1	f <sub>PLLI</sub> × 12/4		MHz	
		PLLMUL = 1	PLLDIV0 = 0	f <sub>PLLI</sub> × 16/2		MHz	
			PLLDIV0 = 1	f <sub>PLLI</sub> × 16/4		MHz	
Long-term jitter <sup>Notes 2, 3</sup>	t <sub>LJ</sub>	f <sub>PLL</sub> = 24 MHz (480 counts)		-2		+2	ns
		f <sub>PLL</sub> = 32 MHz (640 counts)		-2		+2	ns
		f <sub>PLL</sub> = 48 MHz (960 counts)		-2		+2	ns
		f <sub>PLL</sub> = 64 MHz (1280 counts)		-2		+2	ns

**Notes 1.** If the high-speed on-chip oscillator clock is to be selected as the PLL input clock, the minimum and maximum values will reflect the range of accuracy of the oscillation frequency by the high-speed on-chip oscillator clock.

**2.** Guaranteed by design, but not tested before shipment.

**3.** Indicates 20 μs.

3.3 DC Characteristics

3.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to 2. PIN FUNCTIONS.

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(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/6)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Output current, high <sup>Note 1</sup>	I <sub>OH1</sub>	Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			-5.0	mA	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			-3.0	mA	
		Per pin for P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V				-0.6	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V				-0.2	mA
		Total of P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167 (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V				-20.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V				-10.0	mA
		Total of P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157 (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V				-30.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V				-19.0	mA
		Total of all pins (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V				-50.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V				-29.0	mA
I <sub>OH2</sub>	Per pin for P33, P34, P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V				-0.1	mA	
		Total of all pins (for duty factors ≤ 70% <sup>Note 2</sup> )	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V				-2.0	mA

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from pins EV<sub>DD0</sub>, EV<sub>DD1</sub>, and V<sub>DD</sub> to an output pin.

**2.** These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I<sub>OH</sub> × 0.7)/(n × 0.01)  
 <Example> Where n = 80% and I<sub>OH</sub> = -10.0 mA  
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

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**Caution** P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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**(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/6)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Output current, low <sup>Note 1</sup>	I <sub>OL1</sub>	Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			8.5	mA	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			4.0	mA	
		Per pin for P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			0.59	mA	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			0.07	mA	
		Total of P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167 (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			20.0	mA	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			15.0	mA	
		Total of P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157 (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			45.0	mA	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			35.0	mA	
		Total of all pins (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			65.0	mA	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			50.0	mA	
		I <sub>OL2</sub>	Per pin for P33, P34, P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			0.4	mA
				Total of all pins (for duty factors ≤ 70% <sup>Note 2</sup> )	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			5.0

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows to the EV<sub>SS0</sub>, EV<sub>SS1</sub>, and V<sub>SS</sub> pins from an output pin.

**2.** These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I<sub>OL</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OL</sub> = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (3/6)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	$V_{IH1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167 (Schmitt 1 mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0.65 $EV_{DD0}$		$EV_{DD0}^{\text{Note}}$	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0.7 $EV_{DD0}$		$EV_{DD0}^{\text{Note}}$	V
	$V_{IH2}$	P00, P10, P11, P13, P14, P16, P17, P20, P21, P24, P25, P30, P37, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152 to P154, P156 (Schmitt 3 mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0.8 $EV_{DD0}$		$EV_{DD0}^{\text{Note}}$	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0.85 $EV_{DD0}$		$EV_{DD0}^{\text{Note}}$	V
	$V_{IH3}$	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	2.2		$EV_{DD0}^{\text{Note}}$	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	2.0		$EV_{DD0}^{\text{Note}}$	V
	$V_{IH4}$	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.8 $V_{DD}$		$V_{DD}$	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.85 $V_{DD}$		$V_{DD}$	V
	$V_{IH5}$	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.65 $V_{DD}$		$V_{DD}$	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.7 $V_{DD}$		$V_{DD}$	V
	$V_{IH6}$	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.8 $V_{DD}$		$V_{DD}$	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.8 $V_{DD}$		$V_{DD}$	V

**Note** The maximum value of  $V_{IH}$  of the pins P10 to P17, P60 to P63, P70 to P72, and P120 is  $EV_{DD0}$ , even in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (4/6)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, low	V <sub>IL1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167 (Schmitt 1 mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0		0.35 EV <sub>DD0</sub>	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0		0.3 EV <sub>DD0</sub>	V
	V <sub>IL2</sub>	P00, P10, P11, P13, P14, P16, P17, P20, P21, P24, P25, P30, P37, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152 to P154, P156 (Schmitt 3 mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0		0.5 EV <sub>DD0</sub>	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0		0.4 EV <sub>DD0</sub>	V
	V <sub>IL3</sub>	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0		0.8	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0		0.5	V
	V <sub>IL4</sub>	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0		0.5 V <sub>DD</sub>	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0		0.4 V <sub>DD</sub>	V
	V <sub>IL5</sub>	RESET (fixed to Schmitt 1 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0		0.35 V <sub>DD</sub>	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0		0.3 V <sub>DD</sub>	V
	V <sub>IL6</sub>	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0		0.2 V <sub>DD</sub>	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0		0.2 V <sub>DD</sub>	V

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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**(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (5/6)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V <sub>OH1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167 (normal slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -5.0 mA	EV <sub>DD0</sub> -0.9		V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -3.0 mA	EV <sub>DD0</sub> -0.7		V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -1.0 mA	EV <sub>DD0</sub> -0.5		V
	V <sub>OH2</sub>	P33, P34, P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V I <sub>OH2</sub> = -100 μA	V <sub>DD</sub> -0.5		V
	V <sub>OH3</sub>	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH3</sub> = -0.6 mA	EV <sub>DD0</sub> -0.8		V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH3</sub> = -0.2 mA	EV <sub>DD0</sub> -0.5		V
Output voltage, low	V <sub>OL1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167 (normal slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 8.5 mA		0.7	V
			4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 4.0 mA		0.4	V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 4.0 mA		0.7	V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 1.5 mA		0.4	V
	V <sub>OL2</sub>	P33, P34, P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V I <sub>OL2</sub> = 400 μA		0.4	V
	V <sub>OL3</sub>	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 0.6 mA		0.8	V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 0.07 mA		0.5	V

**Caution** P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (6/6)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I <sub>LIH1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	V <sub>I</sub> = EV <sub>DD0</sub>		1	μA		
			V <sub>I</sub> = V <sub>DD</sub>		1	μA		
	I <sub>LIH3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>DD</sub>		1	μA		
			In resonator connection		10	μA		
Input leakage current, low	I <sub>LIL1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	V <sub>I</sub> = EV <sub>SS0</sub>		-1	μA		
			V <sub>I</sub> = V <sub>SS</sub>		-1	μA		
	I <sub>LIL3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>SS</sub>		-1	μA		
			In resonator connection		-10	μA		
On-chip pull-up resistance	R <sub>U</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	V <sub>I</sub> = EV <sub>SS0</sub> , in input port		10	20	100	kΩ

**Caution** P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply Current Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (1/3)

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD1</sub>	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f <sub>IH</sub> = 64 MHz	f <sub>CLK</sub> = 32 MHz Notes 3, 4		7.8	16.0	mA
					f <sub>IH</sub> = 32 MHz	f <sub>CLK</sub> = f <sub>IH</sub> Notes 3, 4		7.5	15.0	mA
					f <sub>IH</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>IH</sub> Notes 3, 4		1.2	2.8	mA
				Resonator operation	f <sub>MX</sub> = 20 MHz	f <sub>CLK</sub> = f <sub>MX</sub> Notes 3, 5		5.1	10.0	mA
					f <sub>MX</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>MX</sub> Notes 3, 5		1.1	3.0	mA
				Resonator operation (PLL operation) (PLL input clock = f <sub>MX</sub> )	f <sub>PLL</sub> = 64 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 32 MHz Notes 3, 6		7.7	16.0	mA
					f <sub>PLL</sub> = 32 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 32 MHz Notes 3, 6		7.7	15.5	mA
					f <sub>PLL</sub> = 32 MHz, f <sub>MX</sub> = 4 MHz	f <sub>CLK</sub> = 32 MHz Notes 3, 6		7.4	15.0	mA
				Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz	f <sub>CLK</sub> = f <sub>SUB</sub> Note 7		7.1	90.0	μA
				Low-speed on-chip oscillator clock operation	f <sub>IL</sub> = 15 kHz	f <sub>CLK</sub> = f <sub>IL</sub> Note 8		3.6	80.0	μA

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>SS</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub>. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.
  - Current drawn when all the CPU instructions are executed.
  - The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit, A/D converter, D/A converter, and comparator are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency
  - f<sub>PLL</sub>: PLL clock frequency
  - f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
  - f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (2/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, 3	I <sub>DD2</sub>	HALT mode Note 2	High-speed on-chip oscillator clock operation	f <sub>IH</sub> = 64 MHz	f <sub>CLK</sub> = 32 MHz Note 5		1.3	11.0	mA
				f <sub>IH</sub> = 32 MHz	f <sub>CLK</sub> = f <sub>IH</sub> <sup>Note 5</sup>		1.0	10.0	mA
				f <sub>IH</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>IH</sub> <sup>Note 5</sup>		0.3	1.7	mA
			Resonator operation	f <sub>MX</sub> = 20 MHz	f <sub>CLK</sub> = f <sub>MX</sub> <sup>Note 6</sup>		0.7	7.0	mA
				f <sub>MX</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>MX</sub> <sup>Note 6</sup>		0.2	1.7	mA
			Resonator operation (PLL operation) (PLL input clock = f <sub>MX</sub> )	f <sub>PLL</sub> = 64 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 32 MHz Note 7		1.2	11.0	mA
				f <sub>PLL</sub> = 32 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 32 MHz Note 7		1.1	10.0	mA
				f <sub>PLL</sub> = 32 MHz, f <sub>MX</sub> = 4 MHz	f <sub>CLK</sub> = 32 MHz Note 7		1.0	10.0	mA
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz	f <sub>CLK</sub> = f <sub>SUB</sub> <sup>Note 8</sup>		0.7	90.0	μA
			Low-speed on-chip oscillator clock operation	f <sub>IL</sub> = 15 kHz	f <sub>CLK</sub> = f <sub>IL</sub> <sup>Note 9</sup>		0.7	80.0	μA
I <sub>DD3</sub>	STOP mode Note 4	T <sub>A</sub> = +25°C				0.5		μA	
		T <sub>A</sub> = +50°C					4.5		
		T <sub>A</sub> = +70°C							8.0
		T <sub>A</sub> = +105°C							50.0

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>SS</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub>. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.
  - When HALT mode is entered during fetch from the flash memory.
  - The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, A/D converter, D/A converter, and comparator are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency
  2.  $f_{SUB}$ : Subsystem clock frequency
  3.  $f_{PLL}$ : PLL clock frequency
  4.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  5.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency
  6.  $f_{CLK}$ : CPU/peripheral hardware clock frequency

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ ) (3/3)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current <sup>Notes 1, 2</sup>	I <sub>SNOZ</sub>	SNOOZE mode	A/D converter operation	During mode transition		1.0	1.7	mA
				During conversion	Low-voltage mode AV <sub>REFP</sub> = V <sub>DD</sub> = 5.0 V		2.1	3.4
			DTC operation			5.5		mA

- Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>SS</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub>. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.
- 2.** The values below the MAX. column include the STOP leakage current.

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	$I_{\text{WDT}}$ <sup>Notes 1, 2</sup>	$f_{\text{IL}} = 15\text{ kHz}$			0.22		$\mu\text{A}$
A/D converter operating current	$I_{\text{ADC}}$ <sup>Note 3</sup>	When conversion at maximum speed	Normal mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 5.0\text{ V}$		1.3	1.7	$\text{mA}$
		When internal reference voltage is selected <sup>Note 5</sup>			75.0		$\mu\text{A}$
LVD operating current	$I_{\text{LVD}}$ <sup>Note 4</sup>				0.08		$\mu\text{A}$
Temperature sensor operating current	$I_{\text{TMPS}}$				75.0		$\mu\text{A}$
D/A converter operating current	$I_{\text{DAC}}$	Per channel			0.8	1.5	$\text{mA}$
Comparator operating current	$I_{\text{CMP}}$				50.0		$\mu\text{A}$
BGO operating current	$I_{\text{BGO}}$ <sup>Note 6</sup>				2.50	12.20	$\text{mA}$

- Notes**
1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.
  2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of  $I_{\text{DD1}}$ ,  $I_{\text{DD2}}$ , or  $I_{\text{DD3}}$  and  $I_{\text{WDT}}$  when the watchdog timer operates in STOP mode.
  3. Current flowing only to the A/D converter. The current value is the sum of  $I_{\text{DD1}}$  or  $I_{\text{DD2}}$  and  $I_{\text{ADC}}$  when the A/D converter operates in operation mode or HALT mode.
  4. Current flowing only to the LVD circuit. The current value is the sum of  $I_{\text{DD1}}$ ,  $I_{\text{DD2}}$ , or  $I_{\text{DD3}}$  and  $I_{\text{LVD}}$  when the LVD circuit operates in operation mode, HALT mode, or STOP mode.
  5. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.
  6. Current increased by the BGO operation. The current value is the sum of  $I_{\text{DD1}}$  or  $I_{\text{DD2}}$  and  $I_{\text{BGO}}$  when the BGO operates in operation mode or HALT mode.

### 3.4 AC Characteristics

#### 3.4.1 Basic Operation

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	$T_{CY}$	High-speed on-chip oscillator clock operation	0.03125		1	$\mu\text{s}$
		High-speed system clock operation	0.05		1	$\mu\text{s}$
		PLL clock operation	0.03125		1	$\mu\text{s}$
		Subsystem clock operation	28.5	30.5	34.5	$\mu\text{s}$
		Low-speed on-chip oscillator clock operation		66.6		$\mu\text{s}$
		In self programming mode	0.03125		1	$\mu\text{s}$
CPU/peripheral hardware clock frequency	$f_{CLK}$		0.03125		66.6	$\mu\text{s}$
External system clock frequency	$f_{EX}$		1.0		20.0	MHz
	$f_{EXS}$		29		35	kHz
External system clock input high-level width, low-level width	$t_{EXH}$ , $t_{EXL}$		24			ns
	$t_{EXHS}$ , $t_{EXLS}$		13.7			$\mu\text{s}$
TI00 to TI07, TI10 to TI17, TI20 to TI27 input high-level width, low-level width	$t_{TIH}$ , $t_{TIL}$		$1/f_{MCK} + 10$			ns
TO00 to TO07, TO10 to TO17, TO20 to TO27 output frequency	$f_{TO}$	All TO pins, Normal slew rate, $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		16	MHz
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		8	MHz
		TO01, TO06, TO07, TO11, TO13 only, Special slew rate, $C = 30\text{ pF}$			2	MHz
PCLBUZ0 output frequency	$f_{PCL}$	Normal slew rate $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		16	MHz
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		8	MHz
		Special slew rate $C = 30\text{ pF}$			2	MHz
Timer RJ input cycle	$t_C$	TRJIO0	100			ns
Timer RJ input high-level width, low-level width	$t_{WH}$ , $t_{WL}$	TRJIO0	40			ns
Interrupt input high-level width, low-level width	$t_{INTH}$ , $t_{INTL}$	INTP0 to INTP15 <sup>Note</sup>	1			$\mu\text{s}$
KR0 to KR7 key interrupt input low-level width	$t_{KR}$		250			ns
RESET low-level width	$t_{RSL}$		10			$\mu\text{s}$

**Note** Pins RESET, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

**Caution** Excluding the error in oscillation frequency accuracy.

**Remark**  $f_{MCK}$ : Timer array unit operation clock frequency

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (2/2)

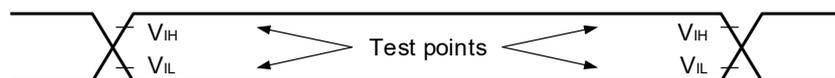
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Port output rise time, port output fall time	$t_{RO}, t_{FO}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167 (normal slew rate) $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			25	ns
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			55	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		25 <sup>Note</sup>	60	ns
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			100	ns

**Note**  $T_A = +25^\circ\text{C}$ ,  $EV_{DD0} = 5.0\text{ V}$

**Caution** Excluding the error in oscillation frequency accuracy.

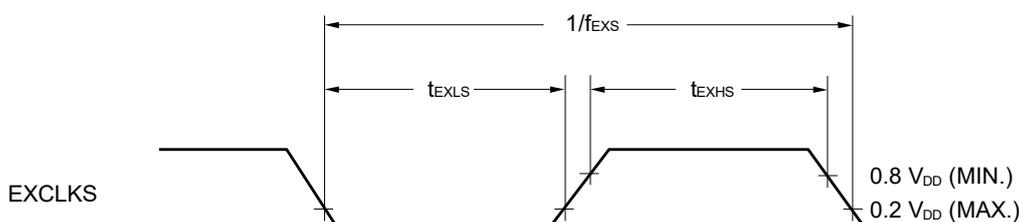
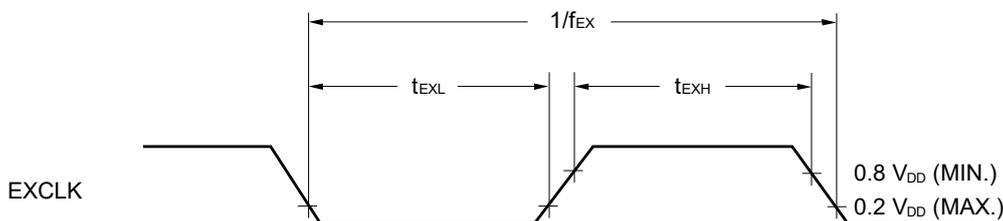
**Remark**  $f_{MCK}$ : Timer array unit operation clock frequency

AC Timing Test Points

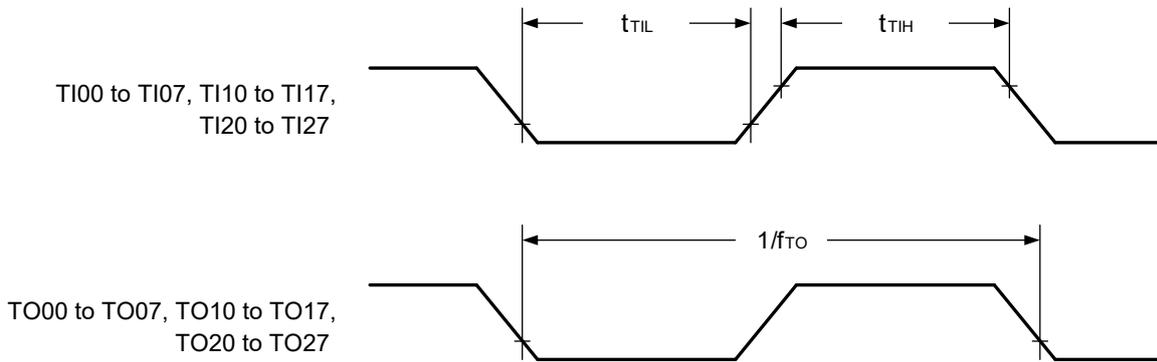


External System Clock Timing

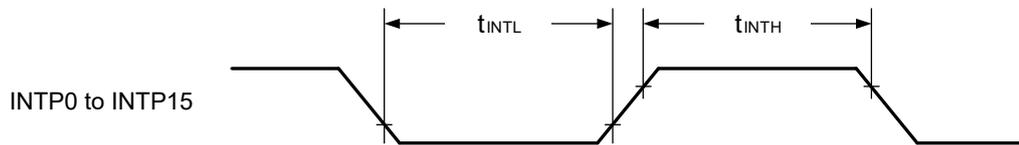
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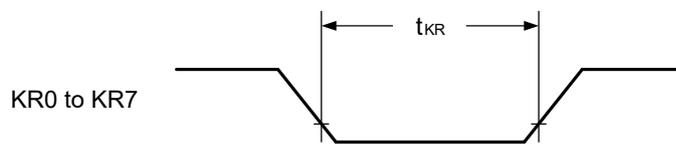
TI/TO Timing



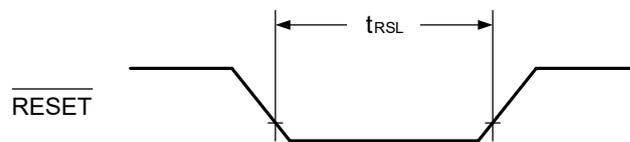
Interrupt Request Input Timing



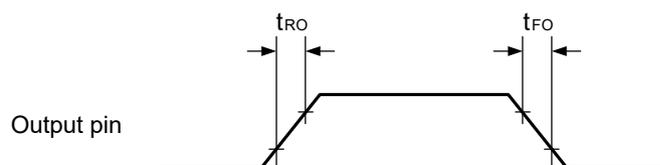
Key Interrupt Input Timing



$\overline{\text{RESET}}$  Input Timing



Output Rising and Falling Timing



### 3.5 Peripheral Functions Characteristics

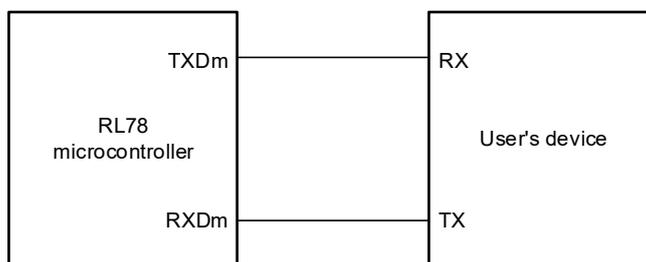
#### 3.5.1 Serial Array Unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

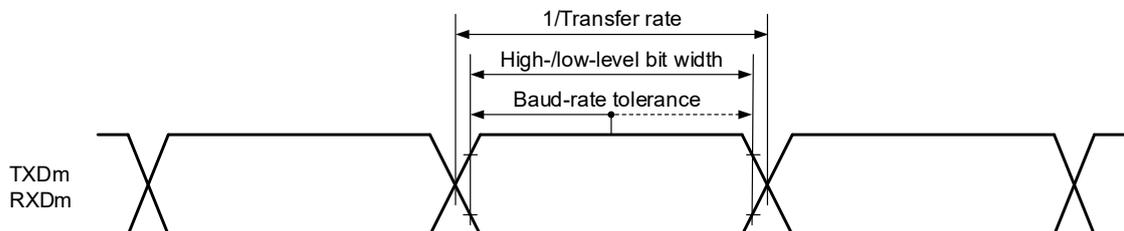
( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq E_{VDD0} = E_{VDD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = E_{VSS0} = E_{VSS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-				$f_{MCK}/6$	bps
		$f_{CLK} = 32\text{ MHz}$ ,	Normal slew rate		5.3	Mbps
		$f_{MCK} = f_{CLK}$	Special slew rate			2

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



**Caution** Select the normal input buffer for the RXD0 pin and RXD1 pin (RXD2 pin is fixed to normal input mode) and normal output mode for the TXD0 pin and TXD1 pin (TXD2 pin is fixed to normal output mode).

- Remarks**
1.  $f_{MCK}$ : Serial array unit operation clock frequency
  2. m: Unit m (m = 0 to 2)

(2) During communication at same potential (CSI mode) (master mode,  $\overline{\text{SCKp}}$  ... internal clock output, normal slew rate)

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	$t_{\text{KCY}1}$		125 <sup>Note 4</sup>			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH}1}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	$t_{\text{KCY}1}/2 - 12$			ns
	$t_{\text{KL}1}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$	$t_{\text{KCY}1}/2 - 18$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK}1}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	44			ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$	55			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{KSI}1}$		30			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO}1}$	$C = 30\text{ pF}$ <sup>Note 3</sup>			40	ns

- Notes**
1. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  2. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  3. C is the load capacitance of the  $\overline{\text{SCKp}}$  and SOp output lines.
  4.  $t_{\text{KCY}1} \geq 4/f_{\text{MCK}}$  must also be satisfied.

**Caution** Select the normal input buffer for the Slp pin and normal output mode for the SOp pin and  $\overline{\text{SCKp}}$  pin.

**Remark** p: CSIp (p = 00, 01, 10, 11, 20, 21), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)

**(3) During communication at same potential (CSI mode) (master mode,  $\overline{\text{SCKp}}$  ... internal clock output, special slew rate)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $4.0\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	$t_{\text{CY1}}$		500 <sup>Note 4</sup>			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH1}}$ , $t_{\text{KL1}}$		$t_{\text{CY1}}/2 - 60$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK1}}$		120			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{SIH1}}$		80			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO1}}$	$C = 30\text{ pF}$ <sup>Note 3</sup>			90	ns

- Notes**
1. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  2. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp hold time becomes "from  $\overline{\text{SCKp}}\uparrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  3. C is the load capacitance of the  $\overline{\text{SCKp}}$  and SOp output lines.
  4.  $t_{\text{CY1}} \geq 4/f_{\text{MCK}}$  must also be satisfied.

**Caution** Select the normal input buffer for the Slp pin and normal output mode and special slew rate for the SOp pin and  $\overline{\text{SCKp}}$  pin.

**Remark** p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

(4) During communication at same potential (CSI mode) (slave mode,  $\overline{\text{SCKp}}$  ... external clock input, normal slew rate)

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time <sup>Note 4</sup>	$t_{\text{KCY2}}$			$8/f_{\text{MCK}}$			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH2}}$ , $t_{\text{KL2}}$			$t_{\text{KCY2}}/2$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK2}}$			$1/f_{\text{MCK}} + 20$			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{SI2}}$			$1/f_{\text{MCK}} + 31$			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SO <sub>p</sub> output	$t_{\text{KS02}}$	$C = 30\text{ pF}$ <sup>Note 3</sup>	$4.0\text{V} \leq \text{V}_{\text{DD}} = \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq 5.5\text{V}$			$2/f_{\text{MCK}} + 44$	ns
			$2.7\text{V} \leq \text{V}_{\text{DD}} = \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} < 4.0\text{V}$			$2/f_{\text{MCK}} + 57$	ns
$\overline{\text{SSIp}}$ setup time	$t_{\text{SSIK}}$	DAP = 0		120			ns
		DAP = 1		$1/f_{\text{MCK}} + 120$			ns
$\overline{\text{SSIp}}$ hold time	$t_{\text{KSSI}}$	DAP = 0		$1/f_{\text{MCK}} + 120$			ns
		DAP = 1		120			ns

- Notes**
- When  $\text{DAP}_{\text{mn}} = 0$  and  $\text{CKP}_{\text{mn}} = 0$ , or  $\text{DAP}_{\text{mn}} = 1$  and  $\text{CKP}_{\text{mn}} = 1$ . The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAP}_{\text{mn}} = 0$  and  $\text{CKP}_{\text{mn}} = 1$  or  $\text{DAP}_{\text{mn}} = 1$  and  $\text{CKP}_{\text{mn}} = 0$ .
  - When  $\text{DAP}_{\text{mn}} = 0$  and  $\text{CKP}_{\text{mn}} = 0$  or  $\text{DAP}_{\text{mn}} = 1$  and  $\text{CKP}_{\text{mn}} = 1$ . The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAP}_{\text{mn}} = 0$  and  $\text{CKP}_{\text{mn}} = 1$  or  $\text{DAP}_{\text{mn}} = 1$  and  $\text{CKP}_{\text{mn}} = 0$ .
  - C is the load capacitance of the  $\overline{\text{SCKp}}$  and SO<sub>p</sub> output lines.
  - The transfer rate is MAX. 1 Mbps in SNOOSE mode.

**Caution** Select the normal input buffer for the Slp,  $\overline{\text{SCKp}}$  and  $\overline{\text{SSIp}}$  pins and normal output mode for the Sop pin.

- Remarks**
- p: CSIp (p = 00, 01, 10, 11, 20, 21),  $\overline{\text{SSIp}}$  (p = 00, 01, 10, 11), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)
  - $f_{\text{MCK}}$ : Serial array unit operation clock frequency

(5) During communication at same potential (CSI mode) (slave mode,  $\overline{\text{SCKp}}$  ... external clock input, special slew rate)

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $4.0\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

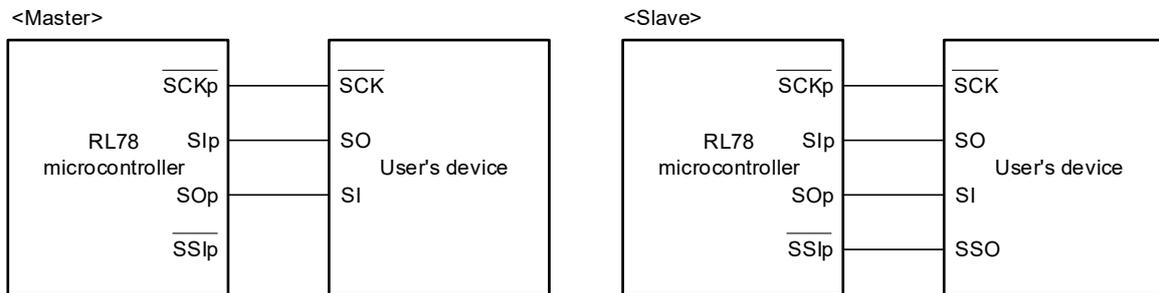
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	$t_{\text{KCY}2}$	$20\text{ MHz} < f_{\text{MCK}}$	$10/f_{\text{MCK}}$			ns
		$10\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$8/f_{\text{MCK}}$			ns
		$f_{\text{MCK}} \leq 10\text{ MHz}$	$6/f_{\text{MCK}}$			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH}2}$ , $t_{\text{KL}2}$		$t_{\text{KCY}2}/2$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK}2}$		$1/f_{\text{MCK}} + 50$			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{KSI}2}$		$1/f_{\text{MCK}} + 50$			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO}2}$	$C = 30\text{ pF}$ <sup>Note 3</sup>			$2/f_{\text{MCK}} + 80$	ns
$\overline{\text{SSIp}}$ setup time	$t_{\text{SSI}K}$	DAP = 0	120			ns
		DAP = 1	$1/f_{\text{MCK}} + 120$			ns
$\overline{\text{SSIp}}$ hold time	$t_{\text{KSSI}}$	DAP = 0	$1/f_{\text{MCK}} + 120$			ns
		DAP = 1	120			ns

- Notes 1.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1 or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
- 2.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0 or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1 or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
- 3.** C is the load capacitance of the  $\overline{\text{SCKp}}$  and SOp output lines.

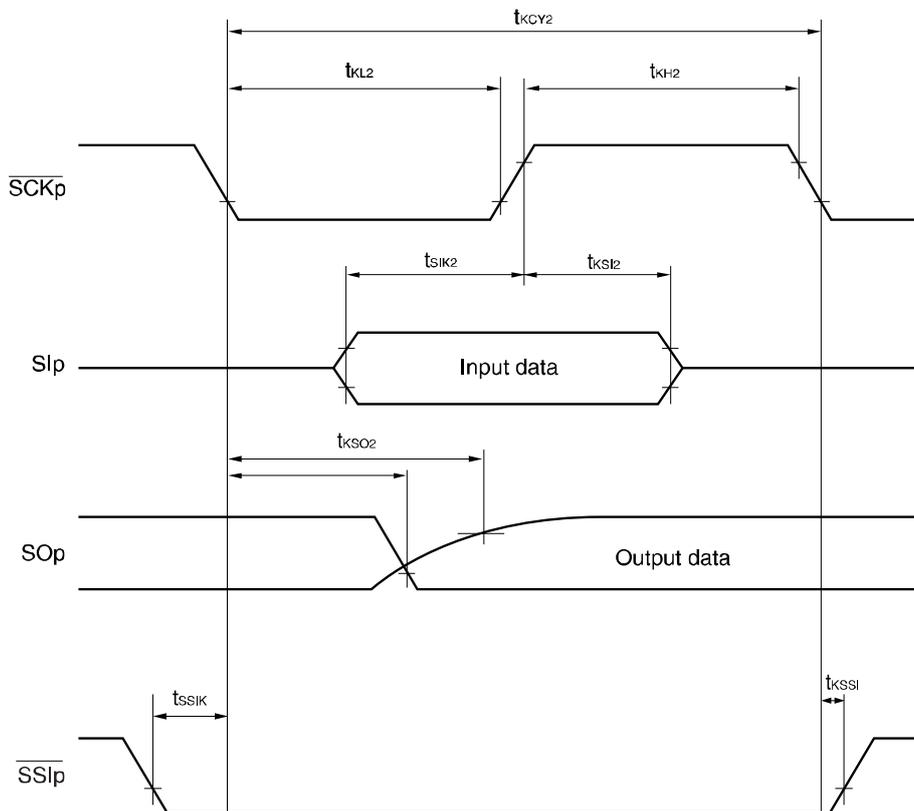
**Caution** Select the normal input buffer for the Slp,  $\overline{\text{SCKp}}$  and  $\overline{\text{SSIp}}$  pins and normal output mode and special slew rate for the SOp pin.

- Remarks 1.** p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)
- 2.**  $f_{\text{MCK}}$ : Serial array unit operation clock frequency

CSI mode connection diagram (during communication at same potential)

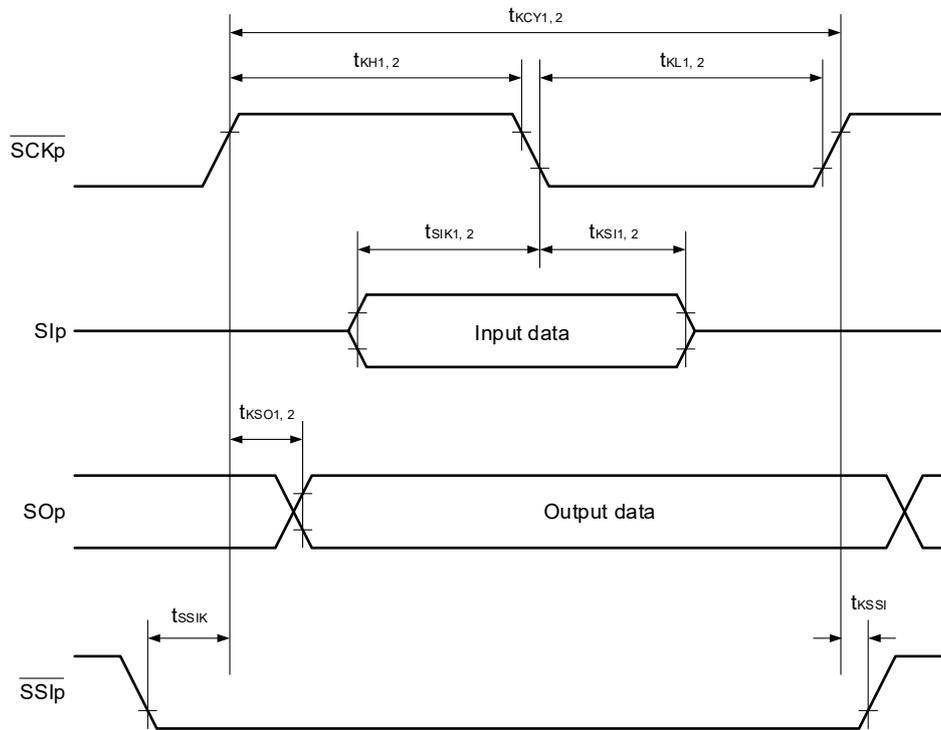


CSI mode serial transfer timing (during communication at same potential)  
(When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ )



**Remark** p: CSIp (p = 00, 01, 10, 11, 20, 21),  $\overline{\text{SSIp}}$  (p = 00, 01, 10, 11), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)

CSI mode serial transfer timing (during communication at same potential)  
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remark** p: CSIp (p = 00, 01, 10, 11, 20, 21),  $\overline{\text{SSIp}}$  (p = 00, 01, 10, 11), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)

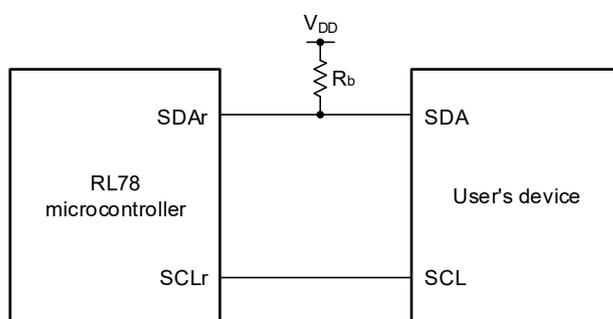
**(6) During communication at same potential (simplified I<sup>2</sup>C mode)**  
**(SDAr: N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode, SCLr: normal output mode)**

(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

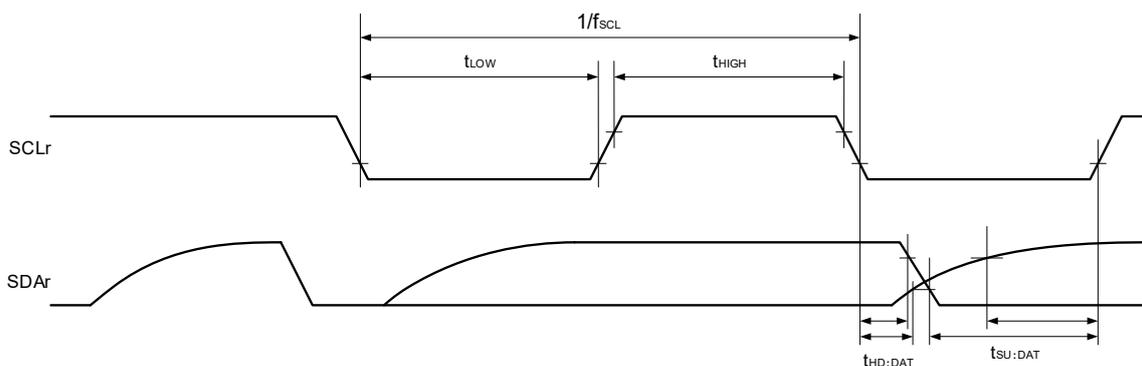
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLr clock frequency	f <sub>SCL</sub>				1000 <sup>Note</sup>	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>		475			ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>		475			ns
Data setup time (reception)	t <sub>SU:DAT</sub>		1/f <sub>MCK</sub> + 85			ns
Data hold time (transmission)	t <sub>HD:DAT</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0		305	ns

**Note** f<sub>SCL</sub> ≤ f<sub>MCK</sub>/4 must also be satisfied.

Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)



Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)



**Caution** Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and normal output mode for the SCLr pin.

- Remarks**
1. R<sub>b</sub> [Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub> [F]: Communication line (SCLr, SDAr) load capacitance
  2. r: IICr (r = 00, 01, 10, 11)
  3. f<sub>MCK</sub>: Serial array unit operation clock frequency

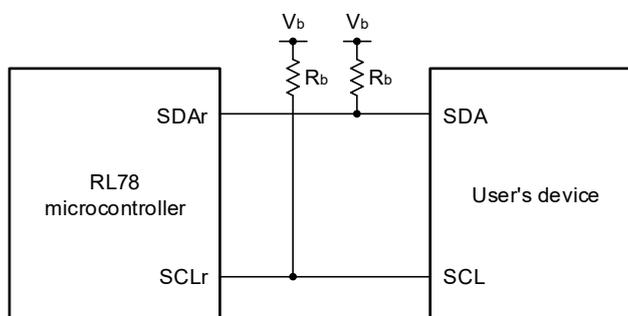
**(7) During communication at same potential (simplified I<sup>2</sup>C mode) (SDAr and SCLr: N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode)**

**(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f <sub>SCL</sub>			400 <sup>Note</sup>	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	1300		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ			
Hold time when SCLr = "H"	t <sub>HIGH</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	600		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ			
Data setup time (reception)	t <sub>SU: DAT</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	1/f <sub>MCK</sub> + 120		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 270		ns
Data hold time (transmission)	t <sub>HD: DAT</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	0	300	ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ			

**Note** f<sub>SCL</sub> ≤ f<sub>MCK</sub>/4 must also be satisfied.

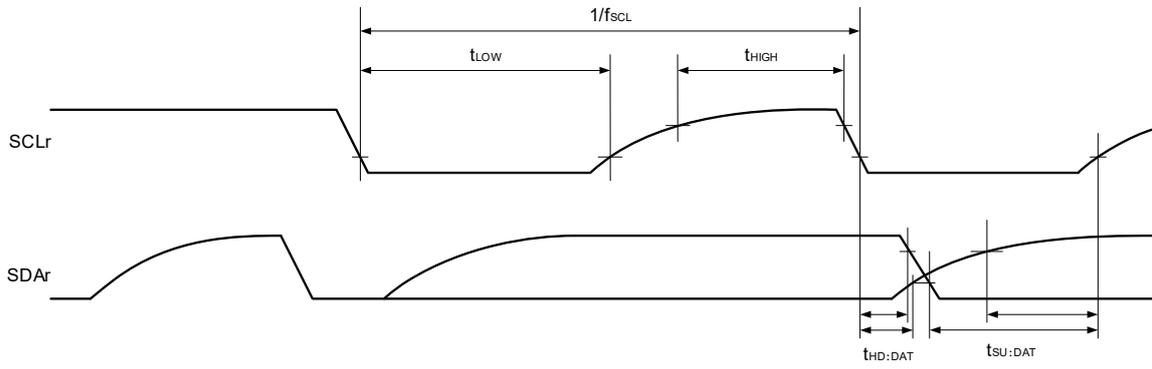
Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)



**Caution** Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and SCLr pin.

- Remarks**
1. R<sub>b</sub> [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C<sub>b</sub> [F]: Communication line (SDAr, SCLr) load capacitance, V<sub>b</sub>[V]: Communication line voltage
  2. r: IICr (r = 00, 01, 10, 11)
  3. f<sub>MCK</sub>: Serial array unit operation clock frequency

Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)



**Remark** r: IICr (r = 00, 01, 10, 11)

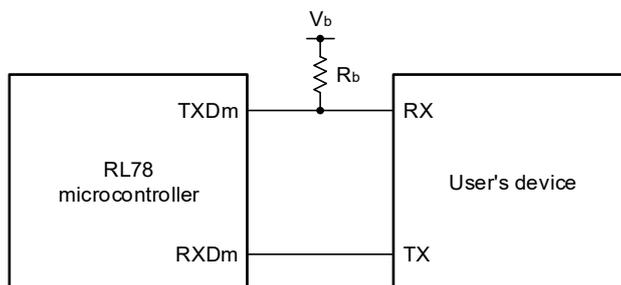
**(8) Communication at different potential (UART mode) (TXD output buffer: N-ch open-drain, RXD input buffer: TTL)**

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $4.0\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )**

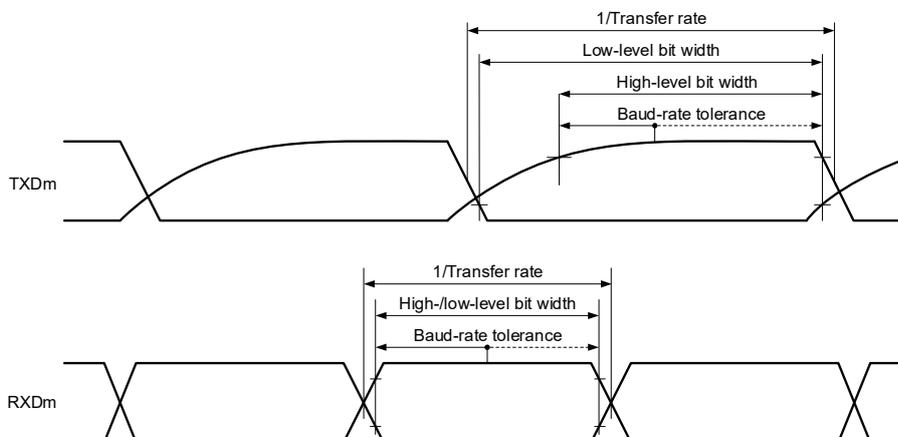
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-	Reception	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $V_{IH} = 2.2\text{ V}$ , $V_{IL} = 0.8\text{ V}$			$f_{mck}/6$	bps
						Theoretical value of the maximum transfer rate <sup>Note</sup> ( $C_b = 30\text{ pF}$ )	5.3
		Transmission	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $V_{OH} = 2.2\text{ V}$ , $V_{OL} = 0.8\text{ V}$			Smaller number of the values given by $f_{mck}/6$ and expression 1 is applicable.	bps
						Theoretical value of the maximum transfer rate <sup>Note</sup> ( $C_b = 30\text{ pF}$ ) Normal slew rate	5.3

**Note** Expression 1: Maximum transfer rate =  $1 / \{[-C_b \times R_b \times \ln(1 - 2.2/V_b)] \times 3\}$

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



**Caution** Select the TTL input buffer for the RXD0 pin and RXD1 pin and N-ch open-drain output mode for the TXD0 pin and TXD1 pin.

- Remarks**
1.  $R_b$  [ $\Omega$ ]: Communication line (TXD) pull-up resistance,  $C_b$  [F]: Communication line (TXD) load capacitance,  $V_b$  [V]: Communication line voltage
  2.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency
  3.  $m$ : Unit  $m$  ( $m = 0, 1$ )

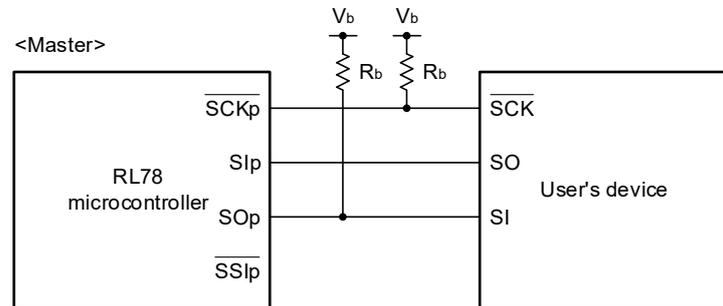
**(9) During communication at different potential (3-V supply system) (CSI mode) (master mode,  $\overline{\text{SCKp}}$  ... internal clock output, normal slew rate)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $4.0\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	$t_{\text{KCY1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	400 <sup>Note3</sup>			ns
$\overline{\text{SCKp}}$ high-level width	$t_{\text{KH1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 75$			ns
$\overline{\text{SCKp}}$ low-level width	$t_{\text{KL1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 20$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	150			ns
Slp setup time (to $\overline{\text{SCKp}}\downarrow$ ) <sup>Note 2</sup>	$t_{\text{SIK1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	70			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{KSI1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	30			ns
Slp hold time (from $\overline{\text{SCKp}}\downarrow$ ) <sup>Note 2</sup>	$t_{\text{KSI1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	30			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output <sup>Note1</sup>	$t_{\text{KSO1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$			120	ns
Delay time from $\overline{\text{SCKp}}\uparrow$ to SOp output <sup>Note2</sup>	$t_{\text{KSO1}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{EV}_{\text{DD0}}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$			40	ns

**Notes 1.** When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ .**2.** When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .**3.**  $t_{\text{KCY1}} \geq 4/f_{\text{MCK}}$  must also be satisfied.

&lt;R&gt;

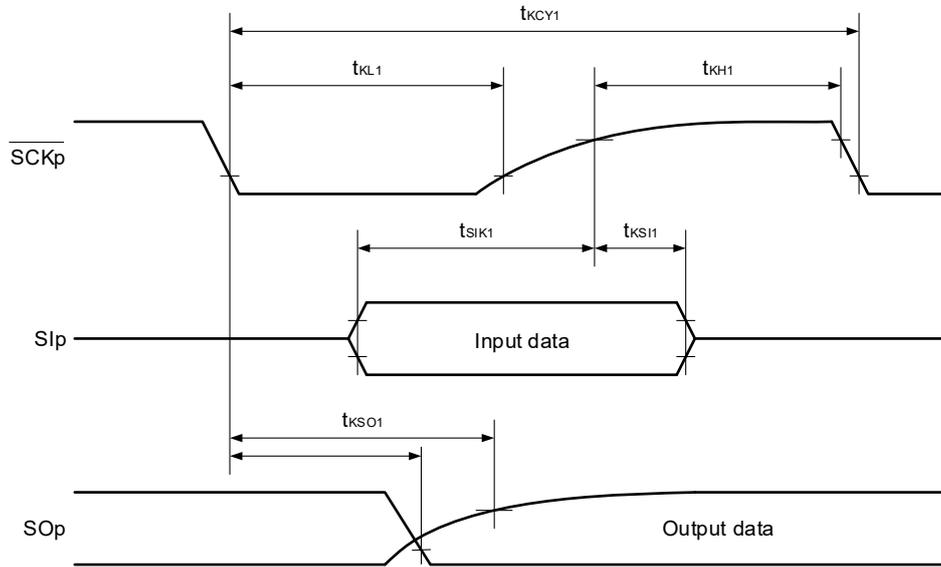
CSI mode connection diagram (during communication at different potential)



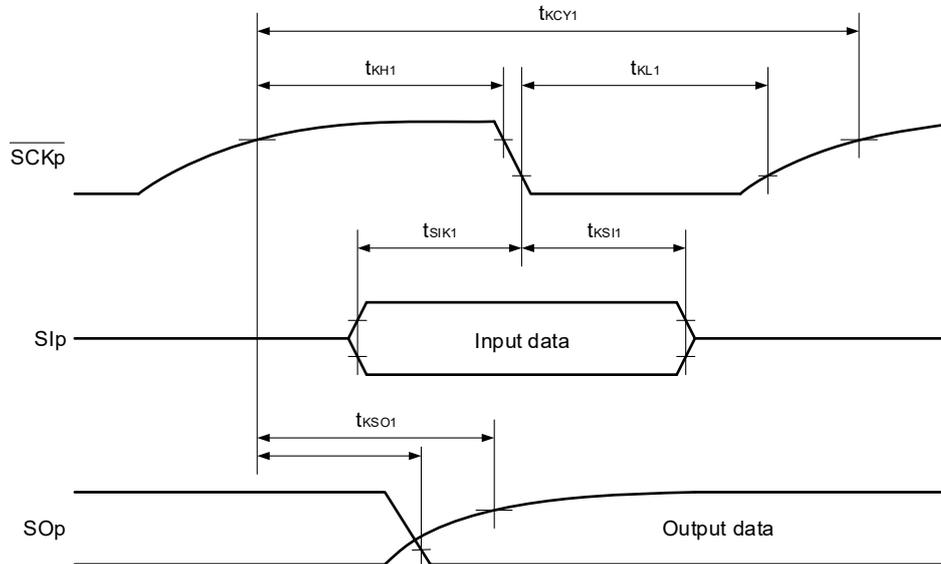
**Caution** Select the TTL input buffer for the  $\text{Slp}$  pin and N-ch open-drain output mode for the  $\text{SOp}$  pin and  $\overline{\text{SCKp}}$  pin.

- Remarks**
- $R_b$  [ $\Omega$ ]: Communication line ( $\overline{\text{SCKp}}$ ,  $\text{SOp}$ ) pull-up resistance,  $C_b$  [F]: Communication line ( $\text{SOp}$ ,  $\overline{\text{SCKp}}$ ) load capacitance,  $V_b$  [V]: Communication line voltage
  - $p$ : CSIp ( $p = 00, 01, 10, 11$ ),  $m$ : Unit  $m$  ( $m = 0, 1$ ),  $n$ : Channel  $n$  ( $n = 0, 1$ )
  - AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the  $V_{IH}$  and  $V_{IL}$  below:  
When  $4.0 \text{ V} \leq E_{V_{DD0}} \leq 5.5 \text{ V}$ ,  $2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$ :  $V_{IH} = 2.2 \text{ V}$ ,  $V_{IL} = 0.8 \text{ V}$

CSI mode serial transfer timing (master mode) (during communication at different potential)  
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)  
 (When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



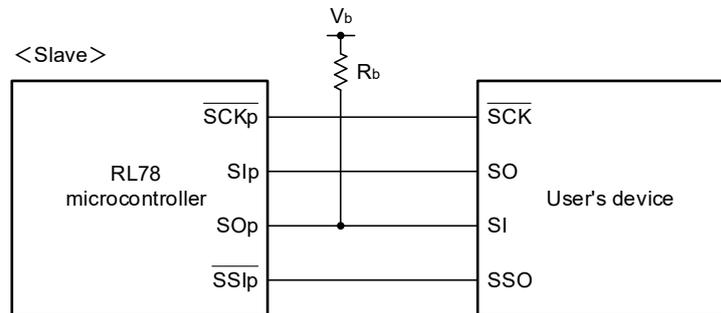
(10) During communication at different potential (3-V supply system) (CSI mode) (slave mode,  $\overline{\text{SCKp}}$  ... external clock input, normal slew rate)

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $4.0\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time <sup>Note 3</sup>	$t_{\text{KCY}2}$	$2.7\text{ V} \leq \text{V}_b \leq \text{V}_{\text{DD}}$	$24\text{ MHz} < f_{\text{MCK}}$	$14/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$12/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$10/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$8/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$6/f_{\text{MCK}}$		ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH}2}$ , $t_{\text{KL}2}$	$2.7\text{ V} \leq \text{V}_b \leq \text{V}_{\text{DD}}$	$t_{\text{KCY}2}/2 - 20$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK}2}$		90			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{KSI}2}$		$1/f_{\text{MCK}} + 50$			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO}2}$	$2.7\text{ V} \leq \text{V}_b \leq \text{V}_{\text{DD}}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			$2/f_{\text{MCK}} + 120$	ns
$\overline{\text{SSIp}}$ setup time	$t_{\text{SSI}K}$	DAP = 0	120			ns
		DAP = 1	$1/f_{\text{MCK}} + 120$			ns
$\overline{\text{SSIp}}$ hold time	$t_{\text{KSSI}}$	DAP = 0	$1/f_{\text{MCK}} + 120$			ns
		DAP = 1	120			ns

- Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.
- 2.** When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.
- 3.** The transfer rate is MAX. 1 Mbps in SNOOSE mode.

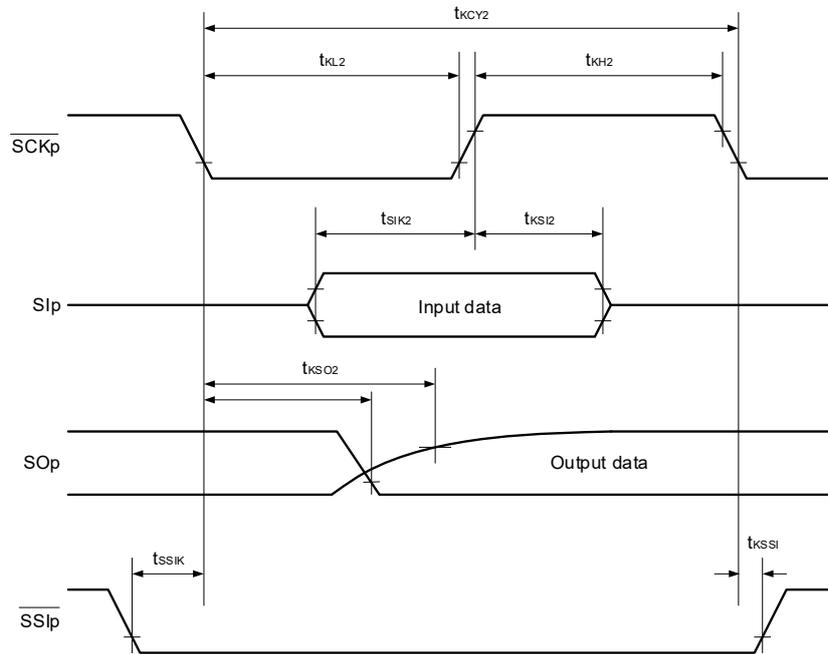
CSI mode connection diagram (during communication at different potential)



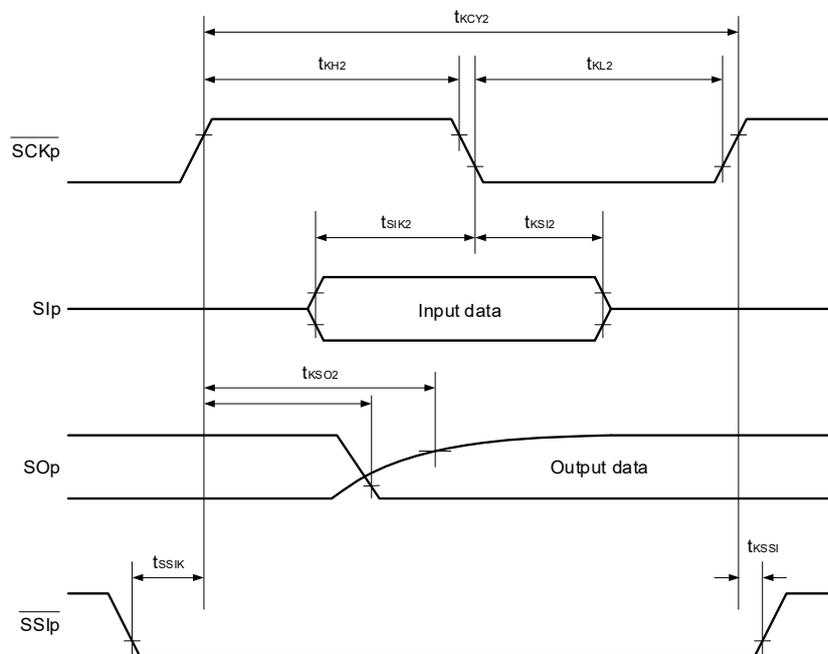
**Caution** Select the TTL input buffer for the  $\text{Slp}$ ,  $\overline{\text{SCKp}}$  and  $\overline{\text{SSIp}}$  pins and N-ch open-drain output mode for the  $\text{SOp}$  pin.

- Remarks**
- $R_b$  [ $\Omega$ ]: Communication line ( $\text{SOp}$ ) pull-up resistance,  $C_b$  [F]: Communication line ( $\text{SOp}$ ) load capacitance,  $V_b$  [V]: Communication line voltage
  - $p$ : CSIp ( $p = 00, 01, 10, 11$ ),  $m$ : Unit  $m$  ( $m = 0, 1$ ),  $n$ : Channel  $n$  ( $n = 0, 1$ )
  - AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the  $V_{IH}$  and  $V_{IL}$  below:  
When  $4.0 \text{ V} \leq E_{V_{DD0}} \leq 5.5 \text{ V}$ ,  $2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$ :  $V_{IH} = 2.2 \text{ V}$ ,  $V_{IL} = 0.8 \text{ V}$

CSI mode serial transfer timing (slave mode) (during communication at different potential)  
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (slave mode) (during communication at different potential)  
 (When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



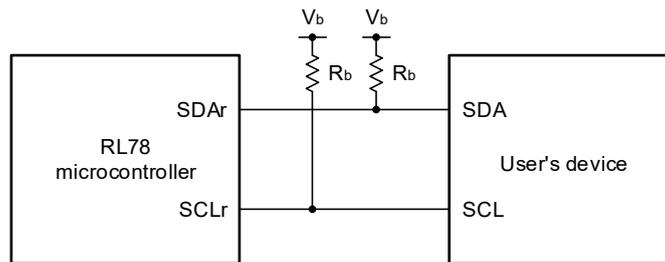
**(11) During communication at different potential (3-V supply system) (simplified I<sup>2</sup>C mode)**  
**(SDAr: TTL input buffer mode or N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode, SCLr: N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode)**

**(T<sub>A</sub> = -40 to +105°C, 4.0 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

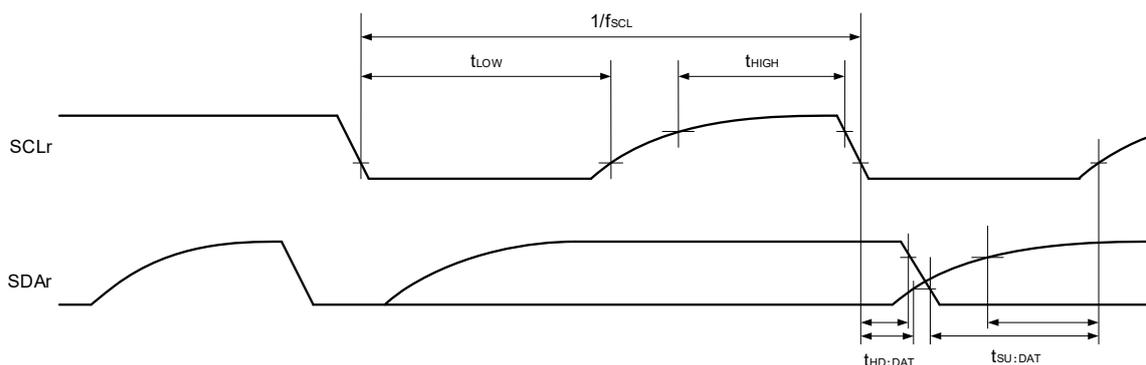
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ		400 <sup>Note</sup>	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	1200		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	600		ns
Data setup time (reception)	t <sub>SU:DAT</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	135 + 1/f <sub>MCK</sub>		ns
Data hold time (transmission)	t <sub>HD:DAT</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	0	140	ns

**Note** f<sub>SCL</sub> ≤ f<sub>MCK</sub>/4 must also be satisfied.

Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)



Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)



**Caution** Select the TTL input buffer and the N-ch open-drain output mode for the SDAr pin and N-ch open-drain output mode for the SCLr pin.

- Remarks**
- R<sub>b</sub> [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C<sub>b</sub> [F]: Communication line (SDAr, SCLr) load capacitance, V<sub>b</sub> [V]: Communication line voltage
  - r: IICr (r = 00, 01, 10, 11)
  - f<sub>MCK</sub>: Serial array unit operation clock frequency

3.5.2 Serial Interface IICA

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

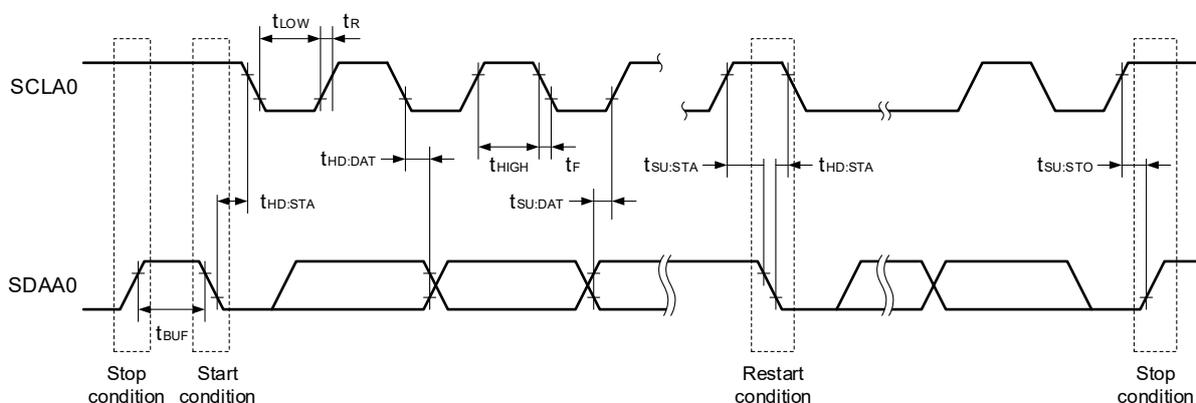
Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode plus: 10 MHz ≤ f <sub>MCK</sub>					0	1000	kHz
		Fast mode: 3.5 MHz ≤ f <sub>MCK</sub>			0	400			kHz
		Normal mode: 1 MHz ≤ f <sub>MCK</sub>	0	100					kHz
Setup time of restart condition <sup>Note 1</sup>	t <sub>SU:STA</sub>		4.7		0.6		0.26		μs
Hold time	t <sub>HD:STA</sub>		4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t <sub>LOW</sub>		4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t <sub>HIGH</sub>		4.0		0.6		0.26		μs
Data setup time (reception)	t <sub>SU:DAT</sub>		250		100		50		ns
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>		0	3.45	0	0.9	0		μs
Setup time of stop condition	t <sub>SU:STO</sub>		4.0		0.6		0.26		μs
Bus-free time	t <sub>BUF</sub>		4.7		1.3		0.5		μs

- Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.  
**2.** The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the  $\overline{\text{ACK}}$  (acknowledge) timing.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

- Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ
- Fast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩ
- Fast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ

IICA serial transfer timing



**3.5.3 On-chip Debug (UART)****(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-		115.2 k		1 M	bps

**3.5.4 LIN/UART Module (RLIN3) UART Mode****(T<sub>A</sub> = -40 to +105°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-	Operation mode, HALT mode	LIN communication clock source (f <sub>CLK</sub> or f <sub>MX</sub> ): 4 to 32 MHz			5333	kbps
		SNOOZE mode	LIN communication clock source (f <sub>CLK</sub> ): 1 to 32 MHz FRQSEL4 = 0 in the user option byte (000C2H/020C2H)			4.8	
			LIN communication clock source (f <sub>CLK</sub> ): 1 to 32 MHz FRQSEL4 = 1 in the user option byte (000C2H/020C2H)			2.4	

### 3.6 Analog Characteristics

#### 3.6.1 A/D Converter Characteristics

(1) When  $AV_{REF}(+) = AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ),  $AV_{REF}(-) = AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target ANI pin: ANI2 to ANI23 (power supply:  $V_{DD}$ )

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution	RES		8		10	bit	
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 3.0$	LSB
		$AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 3.5$	LSB
Conversion time	$t_{CONV}$	10-bit resolution	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
		$AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	3.1875		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EZS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.25$	%FSR
		$AV_{REFP} = V_{DD}$					
Full-scale error <sup>Notes 1, 2</sup>	EFS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.25$	%FSR
		$AV_{REFP} = V_{DD}$					
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.5$	LSB
		$AV_{REFP} = V_{DD}$					
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 1.5$	LSB
		$AV_{REFP} = V_{DD}$					
Reference voltage (+)	$AV_{REFP}$		2.7		$V_{DD}$	V	
Analog input voltage	$V_{AIN}$		0		$AV_{REFP}$	V	
Internal reference voltage (+)	$V_{BGR}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.38	1.45	1.5	V	

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

(2) When  $AV_{REF}(+) = AV_{REFP}/ANI0$  ( $ADREFP1 = 0, ADREFP0 = 1$ ),  $AV_{REF}(-) = AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target ANI pin: ANI24 to ANI30 (power supply:  $EV_{DD0}$ )

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ ,

Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution $AV_{REFP} = V_{DD}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 4.5$	LSB
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 5.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution $AV_{REFP} = V_{DD}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	3.1875		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EZS	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.35$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	EFS	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.35$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 3.5$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Reference voltage (+)	$AV_{REFP}$			2.7		$V_{DD}$	V
Analog input voltage	$V_{AIN}$			0		$AV_{REFP}$ and $EV_{DD0}$	V
Internal reference voltage (+)	$V_{BGR}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.38	1.45	1.5	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

(3) When  $AV_{REF}(+) = V_{DD}$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 0$ ),  $AV_{REF}(-) = V_{SS}$  ( $ADREFM = 0$ ), target ANI pin: ANI0 to ANI23, ANI24 to ANI30

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $V_{DD}$ ,

Reference voltage (-) =  $V_{SS}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution ANI0 to ANI23	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 5.0$	LSB
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 5.5$	LSB
		10-bit resolution ANI24 to ANI30	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 6.5$	LSB
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 7.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	3.1875		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EVS	10-bit resolution ANI0 to ANI23	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.50$	%FSR
		10-bit resolution ANI24 to ANI30	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	EFS	10-bit resolution ANI0 to ANI23	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.50$	%FSR
		10-bit resolution ANI24 to ANI30	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution ANI0 to ANI23	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 3.5$	LSB
		10-bit resolution ANI24 to ANI30	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 4.0$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Analog input voltage	$V_{AIN}$	ANI0 to ANI23 <sup>Note 3</sup>		0		$V_{DD}$	V
		ANI24 to ANI30 <sup>Note 3</sup>		$EV_{SS}$		$EV_{DD0}$	V
Internal reference voltage (+)	$V_{BGR}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.38	1.45	1.5	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** The number of pins depends on the product. For details, refer to **2.1 Pin Function List**.

(4) When  $AV_{REF}(+) = \text{internal reference voltage (ADREFP1 = 1, ADREFP0 = 0)}$ ,  $AV_{REF}(-) = AV_{REFM}/ANI1$   
(ADREFM = 1), target ANI pin: ANI0, ANI2 to ANI23, ANI24 to ANI30

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( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $V_{BGR}$ ,

Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	$t_{CONV}$	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EZS	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 1.0$	LSB
Reference voltage (+)	$V_{BGR}$			1.38	1.45	1.5	V
Analog input voltage	$V_{AIN}$			0		$V_{BGR}$	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

### 3.6.2 Temperatures Sensor Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	$V_{\text{TMPS25}}$	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.1		V
Reference output voltage	$V_{\text{CONST}}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	$F_{\text{VTMPS}}$	Temperature sensor that depends on the temperature		-3.3		mV/ $^\circ\text{C}$
Operation stabilization wait time	$t_{\text{AMP}}$		5			$\mu\text{s}$

### 3.6.3 D/A Converter Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				8	bit
Overall error	AINL	Rload = 4 M $\Omega$ $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			$\pm 2.5$	LSB
		Rload = 8 M $\Omega$ $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			$\pm 2.5$	LSB
Settling time	$t_{\text{SET}}$	Cload = 20 pF $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			3	$\mu\text{s}$

### 3.6.4 Comparator Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	$V_{\text{IOCOMP}}$			$\pm 5$	$\pm 40$	mV
Input voltage range	$V_{\text{ICMP}}$		0		$\text{V}_{\text{DD}}$	V
Response time	$t_{\text{CR}}$ , $t_{\text{CF}}$	Input amplitude $\pm 100\text{ mV}$		70	200	ns
Stabilization wait time during input channel switching <sup>Note 1</sup>	$t_{\text{WAIT}}$	Input amplitude $\pm 100\text{ mV}$	300			ns
Operation stabilization wait time <sup>Note 2</sup>	$t_{\text{CMP}}$	$3.3\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$	1			$\mu\text{s}$
		$2.7\text{ V} \leq \text{V}_{\text{DD}} < 3.3\text{ V}$	3			$\mu\text{s}$

- Notes**
1. Period of time from when the comparator input channel is switched until the comparator is switched to output
  2. Period of time from when the comparator operation is enabled (HCOMPON bit in CMPCTL is set to 1) until the comparator satisfies the DC/AC characteristics.

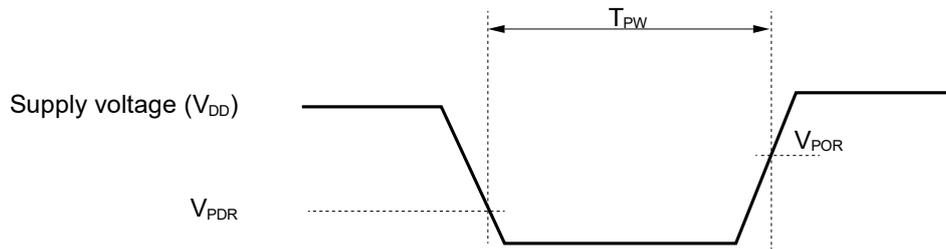
3.6.5 POR Circuit Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage <sup>Note 1</sup>	$V_{POR}$	Power supply rise time	1.48	1.56	1.62	V
	$V_{PDR}$	Power supply fall time	1.47	1.55	1.61	V
Minimum pulse width <sup>Note 2</sup>	$T_{PW}$		300			$\mu\text{s}$
Detection delay time	$T_{PD}$				350	$\mu\text{s}$

**Notes 1.** This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).

**2.** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ .



3.6.6 LVD Circuit Characteristics

(1) LVD detection voltage of interrupt mode or reset mode

(T<sub>A</sub> = -40 to +105°C, V<sub>PDR</sub> ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	V <sub>LVD0</sub>	Power supply rise time	4.62	4.74	4.84	V		
			Power supply fall time	4.52	4.64	4.74	V		
		V <sub>LVD1</sub>	Power supply rise time	4.50	4.62	4.72	V		
			Power supply fall time	4.40	4.52	4.62	V		
		V <sub>LVD2</sub>	Power supply rise time	4.30	4.42	4.51	V		
			Power supply fall time	4.21	4.32	4.41	V		
		V <sub>LVD3</sub>	Power supply rise time	3.13	3.22	3.29	V		
			Power supply fall time	3.07	3.15	3.22	V		
		V <sub>LVD4</sub>	Power supply rise time	2.95	3.02	3.09	V		
			Power supply fall time	2.89	2.96	3.02	V		
		V <sub>LVD5</sub>	Power supply rise time	2.74	2.81	2.87	V		
			Power supply fall time	2.68 <sup>Note</sup>	2.75	2.81	V		
		Minimum pulse width		t <sub>LW</sub>		300			μs
		Detection delay time		t <sub>LD</sub>				300	μs

**Note** The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V<sub>DD</sub> = 2.7 V) is possible until a reset is effected at the power supply falling time.

(2) LVD detection voltage of interrupt & reset mode

(T<sub>A</sub> = -40 to +105°C, V<sub>PDR</sub> ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	V <sub>LVD5</sub>	VPOC2, VPOC1, VPOC0 = 0, 0, 1 <sup>Note 1</sup> , falling reset voltage: 2.75 V	2.68 <sup>Note 2</sup>	2.75	2.81	V	
	V <sub>LVD2</sub>	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.51	V
			Falling interrupt voltage	4.21	4.32	4.41	V
	V <sub>LVD5</sub>	VPOC2, VPOC1, VPOC0 = 0, 1, 0 <sup>Note 1</sup> , falling reset voltage: 2.75 V	2.68 <sup>Note 2</sup>	2.75	2.81	V	
	V <sub>LVD1</sub>	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.72	V
			Falling interrupt voltage	4.40	4.52	4.62	V
	V <sub>LVD5</sub>	VPOC2, VPOC1, VPOC0 = 0, 1, 1 <sup>Note 1</sup> , falling reset voltage: 2.75 V	2.68 <sup>Note 2</sup>	2.75	2.81	V	
	V <sub>LVD3</sub>	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.29	V
			Falling interrupt voltage	3.07	3.15	3.22	V
	V <sub>LVD0</sub>	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.84	V
			Falling interrupt voltage	4.52	4.64	4.74	V

**Notes 1.** These values indicate setting values of option bytes.

**2.** The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V<sub>DD</sub> = 2.7 V) is possible until a reset is effected at the power supply falling time.

### 3.7 Power Supply Voltage Rising Time

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum power supply voltage rising slope	$S_{V_{max}}$	$0\text{ V} \rightarrow V_{DD}$ (VPOC2 = 0 or 1 <sup>Note 2</sup> )			50 <sup>Note 3</sup>	V/ms
Minimum power supply voltage rising slope <sup>Note 1</sup>	$S_{V_{min}}$	$0\text{ V} \rightarrow 2.7\text{ V}$	6.5			V/ms

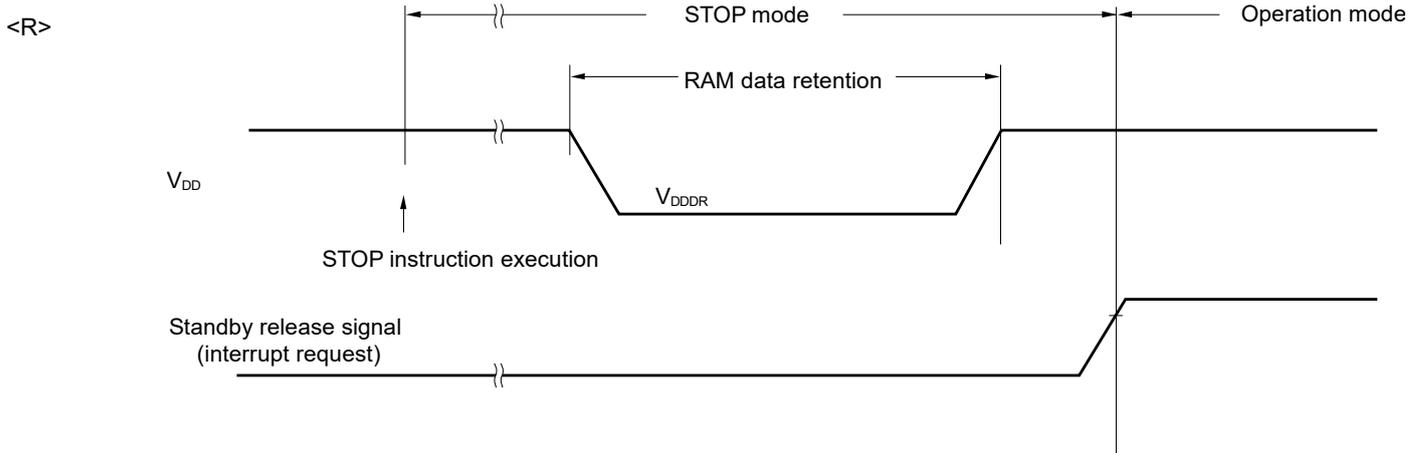
- Notes 1.** The minimum power supply voltage rising slope is applied only under the following condition.  
When the voltage detection (LVD) circuit is not used (VPOC2 = 1) and an external reset circuit is not used or when a reset is not effected until  $V_{DD} = 2.7\text{ V}$ .
- 2.** These values indicate setting values of option bytes.
- 3.** If the power supply drops below  $V_{PDR}$  and a POR reset is effected, this specification is also applied when the power supply is recovered without dropping to  $0\text{ V}$ .

<R> **3.8 RAM Data Retention Characteristics**

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.47 <sup>Note</sup>		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



### 3.9 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

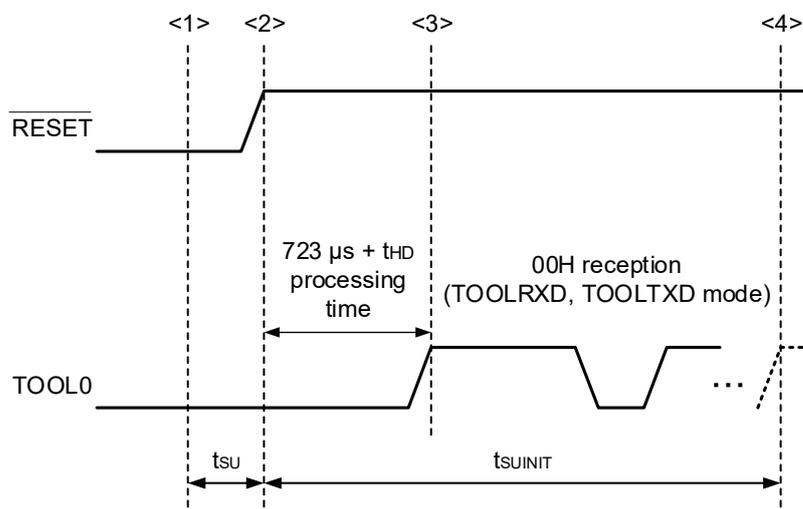
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	$f_{\text{CLK}}$		1		32	MHz
Number of code flash rewrites <sup>Notes 1, 2, 3</sup>	$C_{\text{erwr}}$	Retained for 20 years $T_A = +85^\circ\text{C}$ <sup>Note 4</sup>	1,000			Times
Number of data flash rewrites <sup>Notes 1, 2, 3</sup>		Retained for 20 years $T_A = +85^\circ\text{C}$ <sup>Note 4</sup>	10,000			
		Retained for 5 years $T_A = +85^\circ\text{C}$ <sup>Note 4</sup>	100,000			
Erase time	$T_{\text{erasa}}$	Block erase	5			ms
Write time	$T_{\text{wrwa}}$	1 word write	10			$\mu\text{s}$

- Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The starting point of the retaining years are after the erase.
2. When using flash memory programmer and Renesas Electronics self programming library
  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
  4. The average temperature for data retention.

3.10 Timing of Entry to Flash Memory Programming Modes

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{SUINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{SU}$	POR and LVD reset must be released before the external reset is released.	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{HD}$	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{SUINIT}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{SU}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

## 4. ELECTRICAL SPECIFICATIONS (GRADE K)

- Cautions**
1. RL78/F15 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an EV<sub>DD0</sub>, EV<sub>DD1</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub> pin, replace EV<sub>DD0</sub> and EV<sub>DD1</sub> with V<sub>DD</sub>, or replace EV<sub>SS0</sub> and EV<sub>SS1</sub> with V<sub>SS</sub>.
  3. The pins mounted depending on the product. For details, refer to 1.5 Pin Configurations and 2.1 Pin Function List.

## 4.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$		-0.5 to +6.5	V
	$EV_{DD0}$ , $EV_{DD1}$	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	$V_{SS}$		-0.5 to +0.3	V
	$EV_{SS0}$ , $EV_{SS1}$	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	$V_{IREGC}$	REGC	-0.3 to +2.8 and -0.3 to $V_{DD}+0.3$ <sup>Note 1</sup>	V
Input voltage	$V_{I1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	-0.3 to $EV_{DD0} = EV_{DD1} + 0.3$ and -0.3 to $V_{DD}+0.3$ <sup>Note 2</sup>	V
	$V_{I2}$	P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137, $\overline{RESET}$	-0.3 to $V_{DD}+0.3$ <sup>Note 2</sup>	V
Output voltage	$V_{O1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	-0.3 to $EV_{DD0} = EV_{DD1} + 0.3$ and -0.3 to $V_{DD}+0.3$ <sup>Note 2</sup>	V
	$V_{O2}$	P33, P34, P80 to P87, P90 to P97, P100 to P105	-0.3 to $V_{DD}+0.3$	V
Analog input voltage	$V_{AI1}$	ANI24 to ANI30	-0.3 to $EV_{DD0} = EV_{DD1} + 0.3$ and -0.3 to $AV_{REF(+)}+0.3$ <sup>Notes 2, 3</sup>	V
	$V_{AI2}$	ANI0 to ANI23	-0.3 to $V_{DD}+0.3$ and -0.3 to $AV_{REF(+)}+0.3$ <sup>Notes 2, 3</sup>	V

**Notes 1.** Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu$ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** For pins to be used in A/D conversion, the voltage should not exceed the value  $AV_{REF(+)} + 0.3$ .

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I <sub>OH1</sub>	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	-40	mA
		Total of all pins -170 mA	P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167	-70	mA
			P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157	-100	mA
	I <sub>OH2</sub>	Per pin	P33, P34, P80 to P87, P90 to P97, P100 to P105	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I <sub>OL1</sub>	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	40	mA
		Total of all pins 170 mA	P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167	70	mA
			P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157	100	mA
	I <sub>OL2</sub>	Per pin	P33, P34, P80 to P87, P90 to P97, P100 to P105	1	mA
		Total of all pins		5	mA
	Operating ambient temperature	T <sub>A</sub>	In normal operation mode		-40 to +125
In flash memory programming mode					
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

4.2 Oscillator Characteristics

4.2.1 Main System Clock Oscillator Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator/ Crystal resonator		X1 clock oscillation frequency (fx)	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz

**Cautions 1.** When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as Vss.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

**2.** Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Customers are also requested to adequately evaluate the oscillation on their system. Determine the X1 clock oscillation stabilization time using the oscillation stabilization time of the oscillation stabilization time counter status register (OSTC) and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

#### 4.2.2 On-chip Oscillator Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Oscillators	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency <sup>Note</sup>	$f_{\text{IH}}$		1		48	MHz
High-speed on-chip oscillator clock frequency accuracy	-		-3		+3	%
Low-speed on-chip oscillator clock frequency	$f_{\text{IL}}$ , $f_{\text{WDT}}$			15		kHz
Low-speed on-chip oscillator clock frequency accuracy	-		-15		+15	%

**Note** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/020C2H) and bits 0 to 2 of the HOCODIV register.

4.2.3 Subsystem Clock Oscillator Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Resonator	Recommended Circuit	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency ( $f_{XT}$ )	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	29.0	32.768	35.0	kHz

**Cautions 1.** When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
  - Do not cross the wiring with the other signal lines.
  - Do not route the wiring near a signal line through which a high fluctuating current flows.
  - Always make the ground point of the oscillator capacitor the same potential as  $V_{SS}$ .
  - Do not ground the capacitor to a ground pattern through which a high current flows.
  - Do not fetch signals from the oscillator.
- 2.** The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption and thus required to be adequately evaluated on the system. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

## 4.2.4 PLL Circuit Characteristics

(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
PLL input enable clock frequency <sup>Note 1</sup>	f <sub>PLLI</sub>	PLLMUL = 0	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
		PLLMUL = 1	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
PLL output frequency (center value)	f <sub>PLL</sub>	PLLMUL = 0	PLLDIV0 = 0	f <sub>PLLI</sub> × 12/2		MHz	
			PLLDIV0 = 1	f <sub>PLLI</sub> × 12/4		MHz	
		PLLMUL = 1 <sup>Note 4</sup>	PLLDIV0 = 0 <sup>Note 4</sup>	f <sub>PLLI</sub> × 16/2		MHz	
			PLLDIV0 = 1	f <sub>PLLI</sub> × 16/4		MHz	
Long-term jitter <sup>Notes 2, 3</sup>	t <sub>LJ</sub>	f <sub>PLL</sub> = 24 MHz (480 counts)		-2		+2	ns
		f <sub>PLL</sub> = 32 MHz (640 counts)		-2		+2	ns
		f <sub>PLL</sub> = 48 MHz (960 counts)		-2		+2	ns

- Notes 1.** If the high-speed on-chip oscillator clock is to be selected as the PLL input clock, the minimum and maximum values will reflect the range of accuracy of the oscillation frequency by the high-speed on-chip oscillator clock.
- 2.** Guaranteed by design, but not tested before shipment.
- 3.** Indicates 20 μs.
- 4.** Setting of PLLMUL = 1 and PLLDIV0 = 0 is prohibited when f<sub>PLLI</sub> > 6 MHz.

4.3 DC Characteristics

4.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to **2. PIN FUNCTIONS**.

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(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/6)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high Note 1	I <sub>OH1</sub>	Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			-5.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			-3.0	mA
		Per pin for P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			-0.6	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			-0.2	mA
		Total of P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167 (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			-20.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			-10.0	mA
		Total of P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157 (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			-19.0	mA
		Total of all pins (for duty factors ≤ 70% <sup>Note 2</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			-42.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			-29.0	mA
I <sub>OH2</sub>	Per pin for P33, P34, P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			-0.1	mA	
		Total of all pins (for duty factors ≤ 70% <sup>Note 2</sup> )	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			-2.0	mA

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from pins EV<sub>DD0</sub>, EV<sub>DD1</sub> and V<sub>DD</sub> to an output pin.

**2.** These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I<sub>OH</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OH</sub> = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

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**Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ ) (2/6)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Output current, low <sup>Note 1</sup>	I <sub>OL1</sub>	Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$			8.5	mA	
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$			4.0	mA	
		Per pin for P10, P12, P14, P30, P120, P140 (special slew rate)	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$			0.59	mA	
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$			0.07	mA	
		Total of P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167 (for duty factors $\leq 70\%$ <sup>Note 2</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$			20.0	mA	
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$			15.0	mA	
		Total of P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157 (for duty factors $\leq 70\%$ <sup>Note 2</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$			45.0	mA	
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$			35.0	mA	
		Total of all pins (for duty factors $\leq 70\%$ <sup>Note 2</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$			65.0	mA	
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$			50.0	mA	
		I <sub>OL2</sub>	Per pin for P33, P34, P80 to P87, P90 to P97, P100 to P105	$2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			0.4	mA
				Total of all pins (for duty factors $\leq 70\%$ <sup>Note 2</sup> )	$2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			5.0

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows to the EV<sub>SS0</sub>, EV<sub>SS1</sub> and V<sub>SS</sub> pins from an output pin.

**2.** These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins  $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{OL} = 10.0\text{ mA}$

Total output current of pins =  $(10.0 \times 0.7)/(80 \times 0.01) \approx 8.7\text{ mA}$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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**( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (3/6)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	$V_{IH1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167 (Schmitt 1 mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0.65 $EV_{DD0}$		$EV_{DD0}$ <sup>Note</sup>	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0.7 $EV_{DD0}$		$EV_{DD0}$ <sup>Note</sup>	V
	$V_{IH2}$	P00, P10, P11, P13, P14, P16, P17, P20, P21, P24, P25, P30, P37, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152 to P154, P156 (Schmitt 3 mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0.8 $EV_{DD0}$		$EV_{DD0}$ <sup>Note</sup>	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0.85 $EV_{DD0}$		$EV_{DD0}$ <sup>Note</sup>	V
	$V_{IH3}$	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	2.2		$EV_{DD0}$ <sup>Note</sup>	V
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	2.0		$EV_{DD0}$ <sup>Note</sup>	V
	$V_{IH4}$	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.8 $V_{DD}$		$V_{DD}$	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.85 $V_{DD}$		$V_{DD}$	V
	$V_{IH5}$	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.65 $V_{DD}$		$V_{DD}$	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.7 $V_{DD}$		$V_{DD}$	V
	$V_{IH6}$	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.8 $V_{DD}$		$V_{DD}$	V
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.8 $V_{DD}$		$V_{DD}$	V

**Note** The maximum value of  $V_{IH}$  of the pins P10 to P17, P60 to P63, P70 to P72, and P120 is  $EV_{DD0}$ , even in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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**(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (4/6)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, low	V <sub>IL1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167 (Schmitt 1 mode)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0		0.35 EV <sub>DD0</sub>	V
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V	0		0.3 EV <sub>DD0</sub>	V
	V <sub>IL2</sub>	P00, P10, P11, P13, P14, P16, P17, P20, P21, P24, P25, P30, P37, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152 to P154, P156 (Schmitt 3 mode)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0		0.5 EV <sub>DD0</sub>	V
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V	0		0.4 EV <sub>DD0</sub>	V
	V <sub>IL3</sub>	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0		0.8	V
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V	0		0.5	V
	V <sub>IL4</sub>	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		0.5 V <sub>DD</sub>	V
			2.7 V ≤ V <sub>DD</sub> < 4.0 V	0		0.4 V <sub>DD</sub>	V
	V <sub>IL5</sub>	RESET̄ (fixed to Schmitt 1 mode)	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		0.35 V <sub>DD</sub>	V
			2.7 V ≤ V <sub>DD</sub> < 4.0 V	0		0.3 V <sub>DD</sub>	V
	V <sub>IL6</sub>	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		0.2 V <sub>DD</sub>	V
			2.7 V ≤ V <sub>DD</sub> < 4.0 V	0		0.2 V <sub>DD</sub>	V

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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**(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (5/6)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V <sub>OH1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167 (normal slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -5.0 mA	EV <sub>DD0</sub> -0.9		V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -3.0 mA	EV <sub>DD0</sub> -0.7		V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -1.0 mA	EV <sub>DD0</sub> -0.5		V
	V <sub>OH2</sub>	P33, P34, P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V I <sub>OH2</sub> = -100 μA	V <sub>DD</sub> -0.5		V
	V <sub>OH3</sub>	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH3</sub> = -0.6 mA	EV <sub>DD0</sub> -0.8		V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OH3</sub> = -0.2 mA	EV <sub>DD0</sub> -0.5		V
Output voltage, low	V <sub>OL1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167 (normal slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 8.5 mA		0.7	V
			4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 4.0 mA		0.4	V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 4.0 mA		0.7	V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 1.5 mA		0.4	V
	V <sub>OL2</sub>	P33, P34, P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V I <sub>OL2</sub> = 400 μA		0.4	V
	V <sub>OL3</sub>	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 0.6 mA		0.8	V
			2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 0.07 mA		0.5	V

**Caution** P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (6/6)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I <sub>LIH1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	V <sub>I</sub> = EV <sub>DD0</sub>		1	μA		
			V <sub>I</sub> = V <sub>DD</sub>		1	μA		
	I <sub>LIH3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>DD</sub>		1	μA		
			In resonator connection		10	μA		
Input leakage current, low	I <sub>LIL1</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	V <sub>I</sub> = EV <sub>SS0</sub>		-1	μA		
			V <sub>I</sub> = V <sub>SS</sub>		-1	μA		
	I <sub>LIL3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>SS</sub>		-1	μA		
			In resonator connection		-10	μA		
On-chip pull-up resistance	R <sub>U</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P131 to P136, P140 to P147, P150 to P157, P160 to P167	V <sub>I</sub> = EV <sub>SS0</sub> , in input port		10	20	100	kΩ

**Caution** P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

4.3.2 Supply Current Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (1/3)

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD1</sub>	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f <sub>IH</sub> = 48 MHz	f <sub>CLK</sub> = 24 MHz Notes 3, 4		6.1	13.5	mA
					f <sub>IH</sub> = 24 MHz	f <sub>CLK</sub> = f <sub>IH</sub> Notes 3, 4		5.8	12.5	mA
					f <sub>IH</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>IH</sub> Notes 3, 4		1.2	2.8	mA
				Resonator operation	f <sub>MX</sub> = 20 MHz	f <sub>CLK</sub> = f <sub>MX</sub> Notes 3, 5		5.1	10.0	mA
					f <sub>MX</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>MX</sub> Notes 3, 5		1.1	3.0	mA
				Resonator operation (PLL operation) (PLL input clock = f <sub>MX</sub> )	f <sub>PLL</sub> = 48 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 24 MHz Notes 3, 6		6.1	13.5	mA
					f <sub>PLL</sub> = 24 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 24 MHz Notes 3, 6		6.1	12.5	mA
					f <sub>PLL</sub> = 24 MHz, f <sub>MX</sub> = 4 MHz	f <sub>CLK</sub> = 24 MHz Notes 3, 6		5.8	12.5	mA
				Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz	f <sub>CLK</sub> = f <sub>SUB</sub> Note 7		7.1	170.0	μA
				Low-speed on-chip oscillator clock operation	f <sub>IL</sub> = 15 kHz	f <sub>CLK</sub> = f <sub>IL</sub> Note 8		3.6	160.0	μA

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>SS</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub>. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.
  - Current drawn when all the CPU instructions are executed.
  - The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit, A/D converter, D/A converter, and comparator are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency
  - f<sub>PLL</sub>: PLL clock frequency
  - f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
  - f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (2/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, 3	I <sub>DD2</sub>	HALT mode Note 2	High-speed on-chip oscillator clock operation	f <sub>IH</sub> = 48 MHz	f <sub>CLK</sub> = 24 MHz Note 5		1.0	9.0	mA
				f <sub>IH</sub> = 24 MHz	f <sub>CLK</sub> = f <sub>IH</sub> <sup>Note 5</sup>		0.8	8.0	mA
				f <sub>IH</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>IH</sub> <sup>Note 5</sup>		0.3	1.7	mA
			Resonator operation	f <sub>MX</sub> = 20 MHz	f <sub>CLK</sub> = f <sub>MX</sub> <sup>Note 6</sup>		0.7	7.0	mA
				f <sub>MX</sub> = 1 MHz	f <sub>CLK</sub> = f <sub>MX</sub> <sup>Note 6</sup>		0.2	1.7	mA
			Resonator operation (PLL operation) (PLL input clock = f <sub>MX</sub> )	f <sub>PLL</sub> = 48 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 24 MHz Note 7		1.0	9.0	mA
				f <sub>PLL</sub> = 24 MHz, f <sub>MX</sub> = 8 MHz	f <sub>CLK</sub> = 24 MHz Note 7		0.9	8.0	mA
				f <sub>PLL</sub> = 24 MHz, f <sub>MX</sub> = 4 MHz	f <sub>CLK</sub> = 24 MHz Note 7		0.8	8.0	mA
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz	f <sub>CLK</sub> = f <sub>SUB</sub> <sup>Note 8</sup>		0.7	160.0	μA
			Low-speed on-chip oscillator clock operation	f <sub>IL</sub> = 15 kHz	f <sub>CLK</sub> = f <sub>IL</sub> <sup>Note 9</sup>		0.7	150.0	μA
I <sub>DD3</sub>	STOP mode Note 4	T <sub>A</sub> = +25°C				0.5		μA	
		T <sub>A</sub> = +50°C					4.5		
		T <sub>A</sub> = +70°C					8.0		
		T <sub>A</sub> = +105°C					50.0		
		T <sub>A</sub> = +125°C					100.0		

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>SS</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub>. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.
  - When HALT mode is entered during fetch from the flash memory.
  - The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, A/D converter, D/A converter, and comparator are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
  - When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency
  - f<sub>PLL</sub>: PLL clock frequency
  - f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
  - f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (3/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current <sup>†Notes 1, 2</sup>	I <sub>SNOZ</sub>	SNOOZE mode	A/D converter operation	During mode transition			1.0	1.7	mA
				During conversion	Low-voltage mode AV <sub>REFP</sub> = V <sub>DD</sub> = 5.0 V		2.1	3.4	mA
			DTC operation			5.5		mA	

**Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>SS</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub>. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

**2.** The values below the MAX. column include the STOP leakage current.

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	$I_{\text{WDT}}$ <sup>Notes 1, 2</sup>	$f_{\text{IL}} = 15\text{ kHz}$			0.22		$\mu\text{A}$
A/D converter operating current	$I_{\text{ADC}}$ <sup>Note 3</sup>	When conversion at maximum speed	Normal mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 5.0\text{ V}$		1.3	1.7	$\text{mA}$
		When internal reference voltage is selected <sup>Note 5</sup>			75.0		$\mu\text{A}$
LVD operating current	$I_{\text{LVD}}$ <sup>Note 4</sup>				0.08		$\mu\text{A}$
Temperature sensor operating current	$I_{\text{TMPS}}$				75.0		$\mu\text{A}$
D/A converter operating current	$I_{\text{DAC}}$	Per channel			0.8	1.5	$\text{mA}$
Comparator operating current	$I_{\text{CMP}}$				50.0		$\mu\text{A}$
BGO operating current	$I_{\text{BGO}}$ <sup>Note 6</sup>				2.50	12.20	$\text{mA}$

- Notes**
- When the high-speed on-chip oscillator clock and high-speed system clock are stopped.
  - Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of  $I_{\text{DD1}}$ ,  $I_{\text{DD2}}$ , or  $I_{\text{DD3}}$  and  $I_{\text{WDT}}$  when the watchdog timer operates in STOP mode.
  - Current flowing only to the A/D converter. The current value is the sum of  $I_{\text{DD1}}$  or  $I_{\text{DD2}}$  and  $I_{\text{ADC}}$  when the A/D converter operates in operation mode or HALT mode.
  - Current flowing only to the LVD circuit. The current value is the sum of  $I_{\text{DD1}}$ ,  $I_{\text{DD2}}$ , or  $I_{\text{DD3}}$  and  $I_{\text{LVD}}$  when the LVD circuit operates in operation mode, HALT mode, or STOP mode.
  - Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.
  - Current increased by the BGO operation. The current value is the sum of  $I_{\text{DD1}}$  or  $I_{\text{DD2}}$  and  $I_{\text{BGO}}$  when the BGO operates in operation mode or HALT mode.

## 4.4 AC Characteristics

### 4.4.1 Basic Operation

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	$T_{CY}$	High-speed on-chip oscillator clock operation	0.04166		1	$\mu\text{s}$
		High-speed system clock operation	0.05		1	$\mu\text{s}$
		PLL clock operation	0.04166		1	$\mu\text{s}$
		Subsystem clock operation	28.5	30.5	34.5	$\mu\text{s}$
		Low-speed on-chip oscillator clock operation		66.6		$\mu\text{s}$
		In self programming mode	0.04166		1	$\mu\text{s}$
CPU/peripheral hardware clock frequency	$f_{CLK}$		0.04166		66.6	$\mu\text{s}$
External system clock frequency	$f_{EX}$		1.0		20.0	MHz
	$f_{EXS}$		29		35	kHz
External system clock input high-level width, low-level width	$t_{EXH}, t_{EXL}$		24			ns
	$t_{EXHS}, t_{EXLS}$		13.7			$\mu\text{s}$
TI00 to TI07, TI10 to TI17, TI20 to TI27 input high-level width, low-level width	$t_{TIH}, t_{TIL}$		$1/f_{MCK} + 10$			ns
TO00 to TO07, TO10 to TO17, TO20 to TO27 output frequency	$f_{TO}$	All TO pins, Normal slew rate, $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		12	MHz
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		6	MHz
		TO01, TO06, TO07, TO11, TO13 only, Special slew rate, $C = 30\text{ pF}$			2	MHz
PCLBUZ0 output frequency	$f_{PCL}$	Normal slew rate $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		12	MHz
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		6	MHz
		Special slew rate $C = 30\text{ pF}$			2	MHz
Timer RJ input cycle	$t_C$	TRJIO0	100			ns
Timer RJ input high-level width, low-level width	$t_{WH}, t_{WL}$	TRJIO0	40			ns
Interrupt input high-level width, low-level width	$t_{INTH}, t_{INTL}$	INTP0 to INTP15 <sup>Note</sup>	1			$\mu\text{s}$
KR0 to KR7 key interrupt input low-level width	$t_{KR}$		250			ns
RESET low-level width	$t_{RSL}$		10			$\mu\text{s}$

**Note** Pins RESET, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

**Caution** Excluding the error in oscillation frequency accuracy.

**Remark**  $f_{MCK}$ : Timer array unit operation clock frequency

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ ) (2/2)

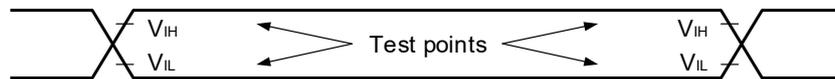
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Port output rise time, port output fall time	$t_{RO}, t_{FO}$	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to P157, P160 to P167 (normal slew rate) $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			25	ns
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			55	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) $C = 30\text{ pF}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		25 <sup>Note</sup>	60	ns
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			100	ns

**Note**  $T_A = +25^\circ\text{C}$ ,  $EV_{DD0} = 5.0\text{ V}$

**Caution** Excluding the error in oscillation frequency accuracy.

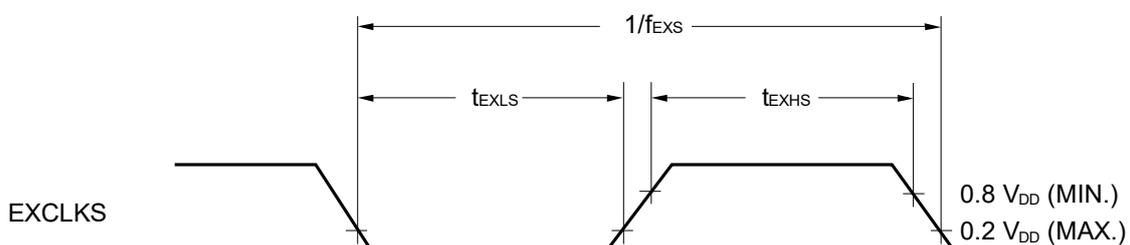
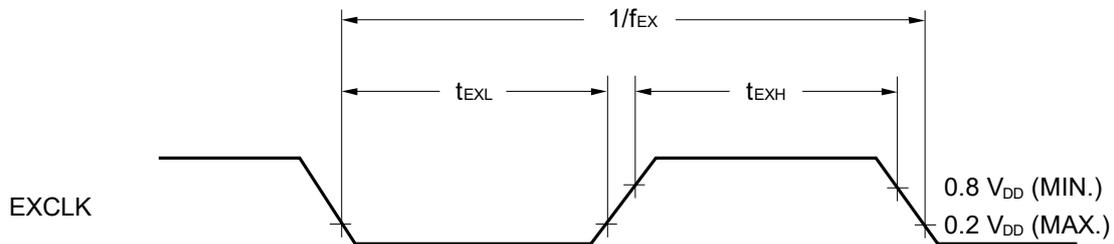
**Remark**  $f_{MCK}$ : Timer array unit operation clock frequency

AC Timing Test Points

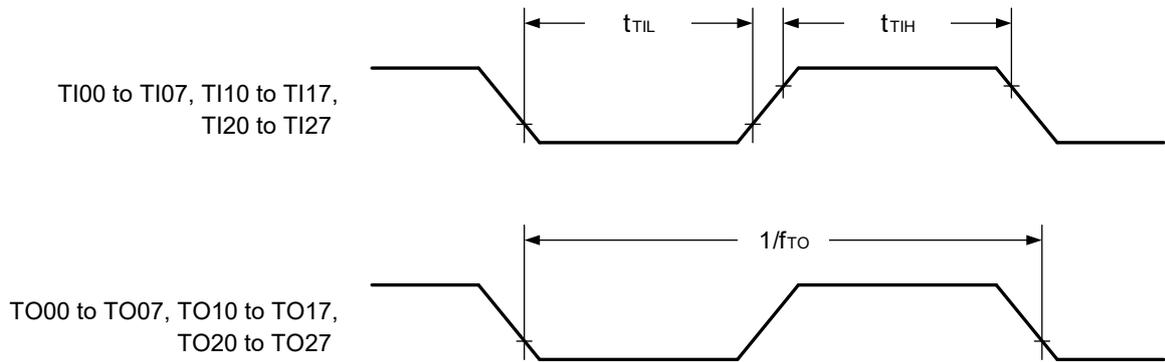


External System Clock Timing

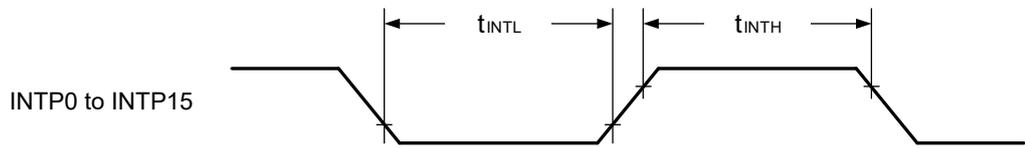
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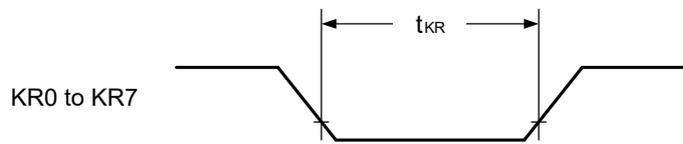
TI/TO Timing



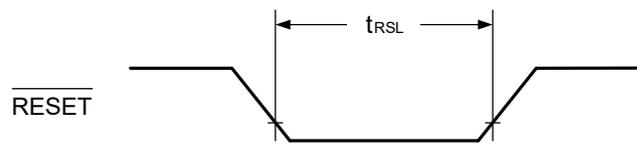
Interrupt Request Input Timing



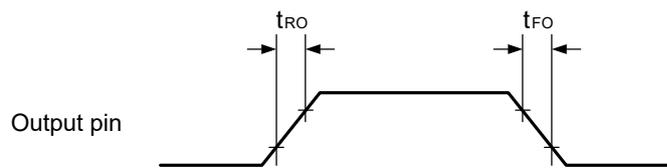
Key Interrupt Input Timing



RESET Input Timing



Output Rising and Falling Timing



### 4.5 Peripheral Functions Characteristics

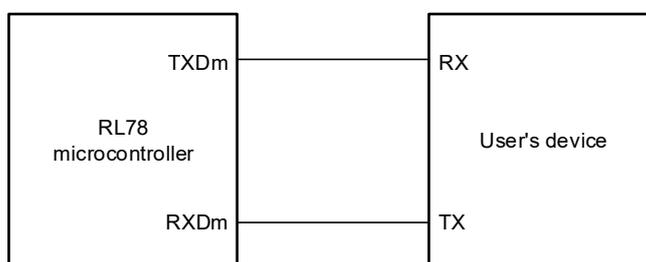
#### 4.5.1 Serial Array Unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

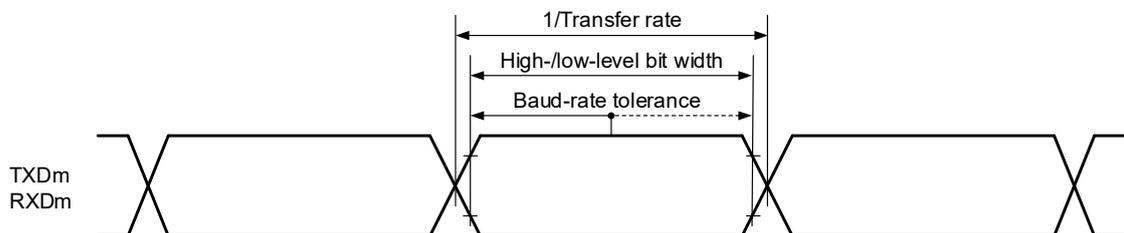
( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-				$f_{\text{MCK}}/6$	bps
		$f_{\text{CLK}} = 24\text{ MHz}$ ,	Normal slew rate		4	Mbps
		$f_{\text{MCK}} = f_{\text{CLK}}$	Special slew rate			2

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



**Caution** Select the normal input buffer for the RXD0 pin and RXD1 pin (RXD2 pin is fixed to normal input mode) and normal output mode for the TXD0 pin and TXD1 pin (TXD2 pin is fixed to normal output mode).

- Remarks**
- $f_{\text{MCK}}$ : Serial array unit operation clock frequency
  - m: Unit m (m = 0 to 2)

(2) During communication at same potential (CSI mode) (master mode,  $\overline{\text{SCKp}}$  ... internal clock output, normal slew rate)

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	$t_{\text{CY1}}$		166.6 <sup>Note 4</sup>			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH1}}$ $t_{\text{KL1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$t_{\text{CY1}}/2 - 12$			ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	$t_{\text{CY1}}/2 - 18$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	55			ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	66			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{SH1}}$		30			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO1}}$	$C = 30\text{ pF}$ <sup>Note 3</sup>			40	ns

- Notes**
1. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  2. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  3. C is the load capacitance of the  $\overline{\text{SCKp}}$  and SOp output lines.
  4.  $t_{\text{CY1}} \geq 4/f_{\text{MCK}}$  must also be satisfied.

**Caution** Select the normal input buffer for the Slp pin and normal output mode for the SOp pin and  $\overline{\text{SCKp}}$  pin.

**Remark** p: CSIp (p = 00, 01, 10, 11, 20, 21), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)

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**(3) During communication at same potential (CSI mode) (master mode,  $\overline{\text{SCKp}}$  ... internal clock output, special slew rate)**

**( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $4.0\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	$t_{\text{CY1}}$		500 <sup>Note 4</sup>			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH1}}$ , $t_{\text{KL1}}$		$t_{\text{CY1}}/2 - 60$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK1}}$		120			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{SIH1}}$		80			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO1}}$	$C = 30\text{ pF}$ <sup>Note 3</sup>			90	ns

- Notes**
1. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  2. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp hold time becomes "from  $\overline{\text{SCKp}}\uparrow$ " when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$  or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  3. C is the load capacitance of the  $\overline{\text{SCKp}}$  and SOp output lines.
  4.  $t_{\text{CY1}} \geq 4/f_{\text{MCK}}$  must also be satisfied.

**Caution** Select the normal input buffer for the Slp pin and normal output mode and special slew rate for the SOp pin and  $\overline{\text{SCKp}}$  pin.

**Remark** p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

**(4) During communication at same potential (CSI mode) (slave mode,  $\overline{\text{SCKp}}$  ... external clock input, normal slew rate)****( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time <sup>Note 4</sup>	$t_{\text{KCY}2}$			$8/f_{\text{MCK}}$			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH}2}$ , $t_{\text{KL}2}$			$t_{\text{KCY}2}/2$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK}2}$			$1/f_{\text{MCK}} + 20$			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{SI}2}$			$1/f_{\text{MCK}} + 31$			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SO <sub>p</sub> output	$t_{\text{KS}02}$	C = 30 pF <sup>Note 3</sup>	$4.0\text{V} \leq \text{V}_{\text{DD}} = \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq 5.5\text{V}$			$2/f_{\text{MCK}} + 44$	ns
			$2.7\text{V} \leq \text{V}_{\text{DD}} = \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} < 4.0\text{V}$			$2/f_{\text{MCK}} + 57$	ns
$\overline{\text{SSIp}}$ setup time	$t_{\text{SSI}K}$	DAP = 0		120			ns
		DAP = 1		$1/f_{\text{MCK}} + 120$			ns
$\overline{\text{SSIp}}$ hold time	$t_{\text{KSSI}}$	DAP = 0		$1/f_{\text{MCK}} + 120$			ns
		DAP = 1		120			ns

- Notes**
- When DAP<sub>m<sub>n</sub></sub> = 0 and CKP<sub>m<sub>n</sub></sub> = 0, or DAP<sub>m<sub>n</sub></sub> = 1 and CKP<sub>m<sub>n</sub></sub> = 1. The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when DAP<sub>m<sub>n</sub></sub> = 0 and CKP<sub>m<sub>n</sub></sub> = 1 or DAP<sub>m<sub>n</sub></sub> = 1 and CKP<sub>m<sub>n</sub></sub> = 0.
  - When DAP<sub>m<sub>n</sub></sub> = 0 and CKP<sub>m<sub>n</sub></sub> = 0 or DAP<sub>m<sub>n</sub></sub> = 1 and CKP<sub>m<sub>n</sub></sub> = 1. The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when DAP<sub>m<sub>n</sub></sub> = 0 and CKP<sub>m<sub>n</sub></sub> = 1 or DAP<sub>m<sub>n</sub></sub> = 1 and CKP<sub>m<sub>n</sub></sub> = 0.
  - C is the load capacitance of the  $\overline{\text{SCKp}}$  and SO<sub>p</sub> output lines.
  - The transfer rate is MAX. 1 Mbps in SNOOSE mode.

**Caution** Select the normal input buffer for the Slp,  $\overline{\text{SCKp}}$  and  $\overline{\text{SSIp}}$  pins and normal output mode for the Sop pin.

- Remarks**
- p: CSIp (p = 00, 01, 10, 11, 20, 21),  $\overline{\text{SSIp}}$  (p = 00, 01, 10, 11), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)
  - $f_{\text{MCK}}$ : Serial array unit operation clock frequency

(5) During communication at same potential (CSI mode) (slave mode,  $\overline{\text{SCKp}}$  ... external clock input, special slew rate)

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $4.0\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

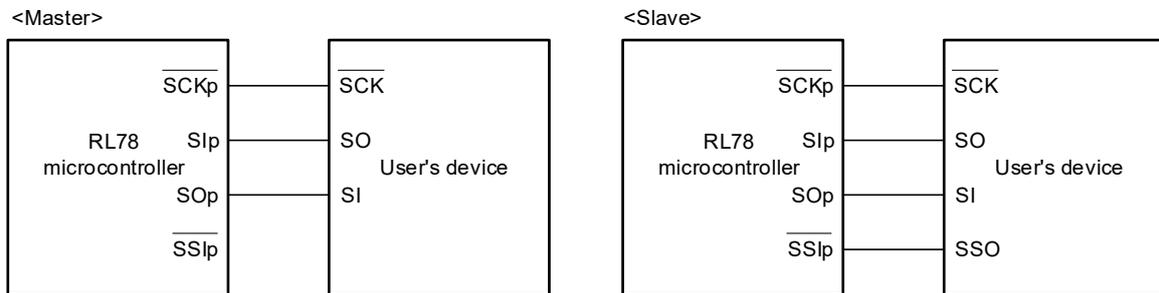
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	$t_{\text{KCY}2}$	$20\text{ MHz} < f_{\text{MCK}}$	$10/f_{\text{MCK}}$			ns
		$10\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$8/f_{\text{MCK}}$			ns
		$f_{\text{MCK}} \leq 10\text{ MHz}$	$6/f_{\text{MCK}}$			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH}2}$ , $t_{\text{KL}2}$		$t_{\text{KCY}2}/2$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK}2}$		$1/f_{\text{MCK}} + 50$			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{KSI}2}$		$1/f_{\text{MCK}} + 50$			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO}2}$	$C = 30\text{ pF}$ <sup>Note 3</sup>			$2/f_{\text{MCK}} + 80$	ns
$\overline{\text{SSIp}}$ setup time	$t_{\text{SSI}K}$	DAP = 0	120			ns
		DAP = 1	$1/f_{\text{MCK}} + 120$			ns
$\overline{\text{SSIp}}$ hold time	$t_{\text{KSSI}}$	DAP = 0	$1/f_{\text{MCK}} + 120$			ns
		DAP = 1	120			ns

- Notes**
- When DAP<sub>m</sub> = 0 and CKP<sub>m</sub> = 0, or DAP<sub>m</sub> = 1 and CKP<sub>m</sub> = 1. The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when DAP<sub>m</sub> = 0 and CKP<sub>m</sub> = 1 or DAP<sub>m</sub> = 1 and CKP<sub>m</sub> = 0.
  - When DAP<sub>m</sub> = 0 and CKP<sub>m</sub> = 0 or DAP<sub>m</sub> = 1 and CKP<sub>m</sub> = 1. The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when DAP<sub>m</sub> = 0 and CKP<sub>m</sub> = 1 or DAP<sub>m</sub> = 1 and CKP<sub>m</sub> = 0.
  - C is the load capacitance of the  $\overline{\text{SCKp}}$  and SOp output lines.

**Caution** Select the normal input buffer for the Slp,  $\overline{\text{SCKp}}$  and  $\overline{\text{SSIp}}$  pins and normal output mode and special slew rate for the SOp pin.

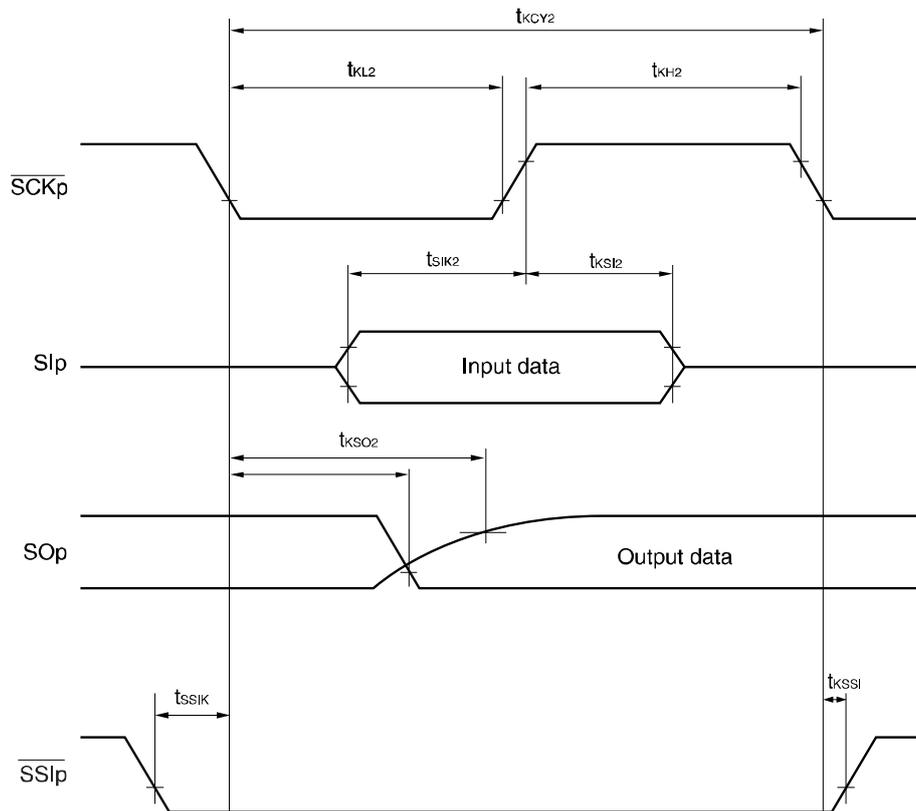
- Remarks**
- p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)
  - $f_{\text{MCK}}$ : Serial array unit operation clock frequency

CSI mode connection diagram (during communication at same potential)



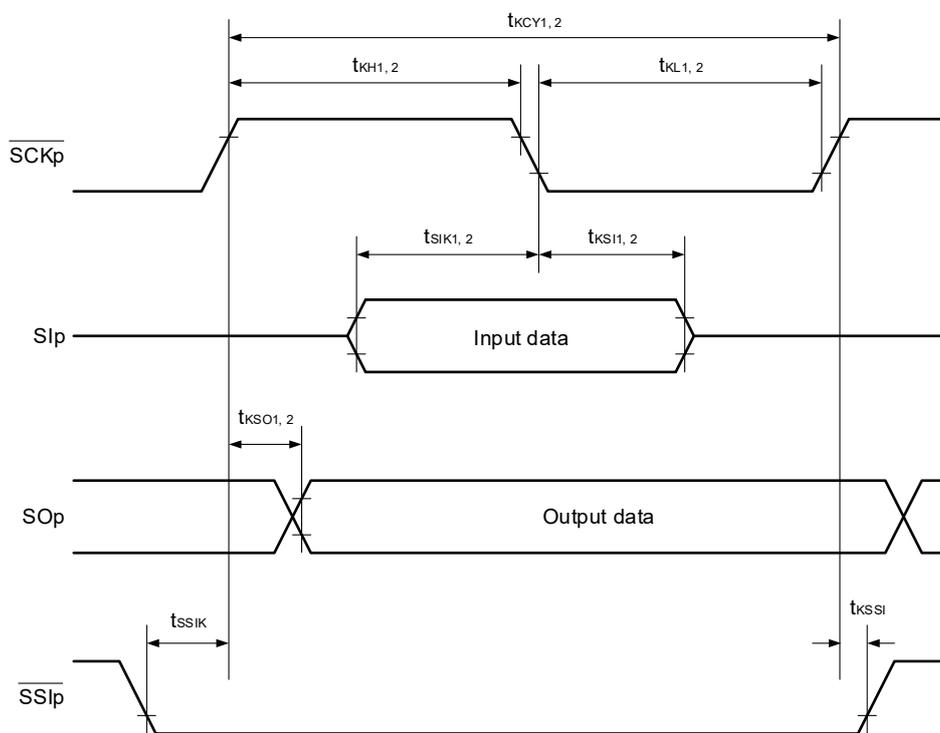
CSI mode serial transfer timing (during communication at same potential)

(When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ )



**Remark** p: CSIp (p = 00, 01, 10, 11, 20, 21),  $\overline{\text{SSIp}}$  (p = 00, 01, 10, 11), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)

CSI mode serial transfer timing (during communication at same potential)  
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remark** p: CSIp (p = 00, 01, 10, 11, 20, 21),  $\overline{\text{SSIp}}$  (p = 00, 01, 10, 11), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)

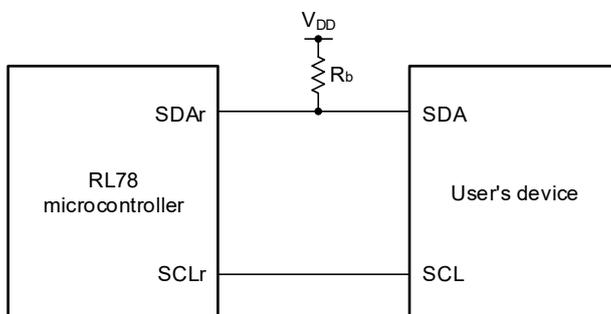
**(6) During communication at same potential (simplified I<sup>2</sup>C mode)**  
**(SDAr: N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode, SCLr: normal output mode)**

(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

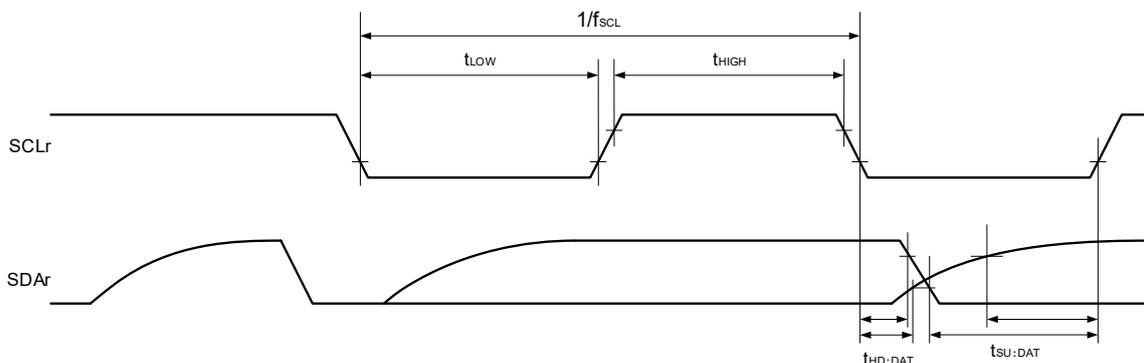
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLr clock frequency	f <sub>SCL</sub>				1000 <sup>Note</sup>	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>		475			ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>		475			ns
Data setup time (reception)	t <sub>SU:DAT</sub>		1/f <sub>MCK</sub> + 85			ns
Data hold time (transmission)	t <sub>HD:DAT</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0		305	ns

**Note** f<sub>SCL</sub> ≤ f<sub>MCK</sub>/4 must also be satisfied.

Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)



Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)



**Caution** Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and normal output mode for the SCLr pin.

- Remarks**
1. R<sub>b</sub> [Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub> [F]: Communication line (SCLr, SDAr) load capacitance
  2. r: IICr (r = 00, 01, 10, 11)
  3. f<sub>MCK</sub>: Serial array unit operation clock frequency

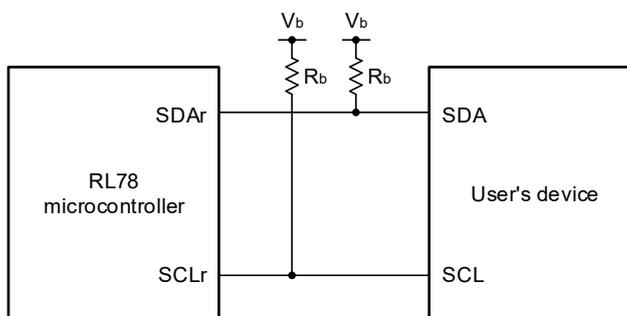
(7) During communication at same potential (simplified I<sup>2</sup>C mode) (SDAr and SCLr: N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode)

(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f <sub>SCL</sub>			400 <sup>Note</sup>	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	1300		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ			
Hold time when SCLr = "H"	t <sub>HIGH</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	600		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ			
Data setup time (reception)	t <sub>SU : DAT</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	1/f <sub>MCK</sub> + 120		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 270		ns
Data hold time (transmission)	t <sub>HD : DAT</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.7 kΩ	0	300	ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ			

**Note** f<sub>SCL</sub> ≤ f<sub>MCK</sub>/4 must also be satisfied.

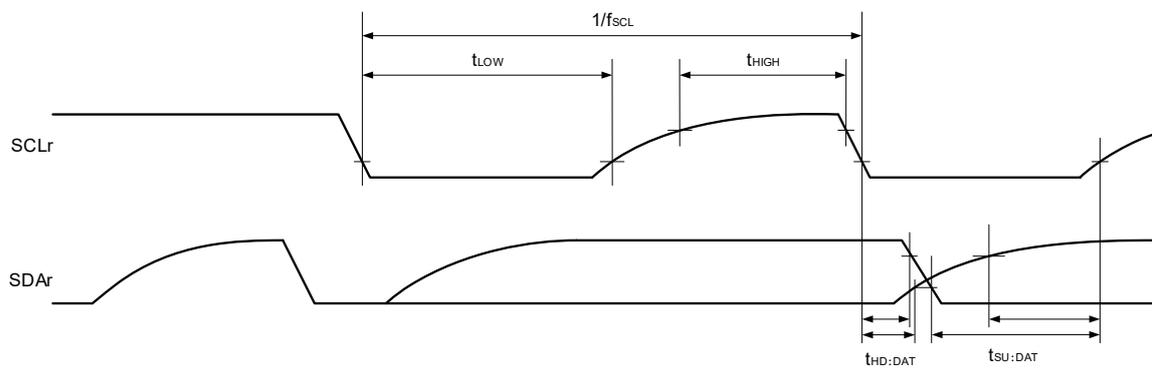
Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)



**Caution** Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and SCLr pin.

- Remarks**
1. R<sub>b</sub> [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C<sub>b</sub> [F]: Communication line (SDAr, SCLr) load capacitance, V<sub>b</sub>[V]: Communication line voltage
  2. r: IICr (r = 00, 01, 10, 11)
  3. f<sub>MCK</sub>: Serial array unit operation clock frequency

Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)



**Remark** r: IICr (r = 00, 01, 10, 11)

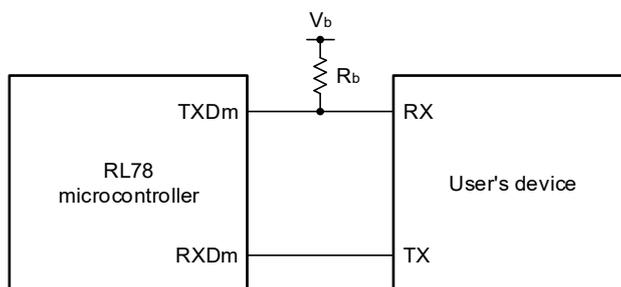
**(8) Communication at different potential (UART mode) (TXD output buffer: N-ch open-drain, RXD input buffer: TTL)**

**(T<sub>A</sub> = -40 to +125°C, 4.0 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

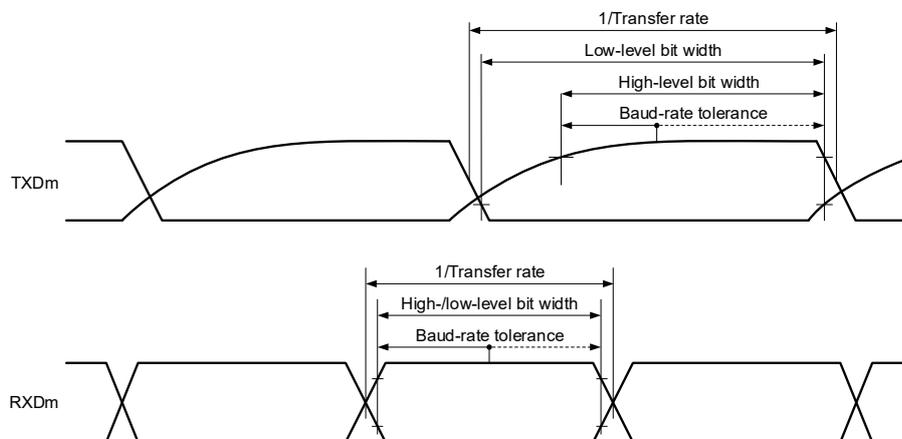
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Transfer rate	-	Reception	2.7 V ≤ V <sub>b</sub> ≤ EV <sub>DD0</sub> ,			f <sub>MCK</sub> /6	bps	
			V <sub>IH</sub> = 2.2 V, V <sub>IL</sub> = 0.8 V	Theoretical value of the maximum transfer rate <sup>Note</sup> (C <sub>b</sub> = 30 pF)			4.0	Mbps
		Transmission	2.7 V ≤ V <sub>b</sub> ≤ EV <sub>DD0</sub> ,				Smaller number of the values given by f <sub>MCK</sub> /6 and expression 1 is applicable.	bps
			V <sub>OH</sub> = 2.2 V, V <sub>OL</sub> = 0.8 V	Theoretical value of the maximum transfer rate <sup>Note</sup> (C <sub>b</sub> = 30 pF) Normal slew rate			4.0	Mbps

**Note** Expression 1: Maximum transfer rate = 1 / [{-C<sub>b</sub> × R<sub>b</sub> × ln (1 - 2.2/V<sub>b</sub>)} × 3]

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



**Caution** Select the TTL input buffer for the RXD0 pin and RXD1 pin and N-ch open-drain output mode for the TXD0 pin and TXD1 pin.

- Remarks**
1.  $R_b$  [ $\Omega$ ]: Communication line (TXD) pull-up resistance,  $C_b$  [F]: Communication line (TXD) load capacitance,  $V_b$  [V]: Communication line voltage
  2.  $f_{MCK}$ : Serial array unit operation clock frequency
  3.  $m$ : Unit  $m$  ( $m = 0, 1$ )

**(9) During communication at different potential (3-V supply system) (CSI mode) (master mode,  $\overline{SCKp}$  ... internal clock output, normal slew rate)**

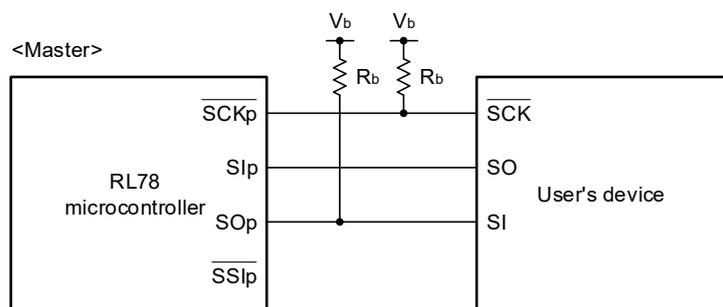
**( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $4.0\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	$t_{KCY1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	400 <sup>Note3</sup>			ns
$\overline{SCKp}$ high-level width	$t_{KH1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 75$			ns
$\overline{SCKp}$ low-level width	$t_{KL1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 20$			ns
Slp setup time (to $\overline{SCKp}\uparrow$ ) <sup>Note 1</sup>	$t_{SIK1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	150			ns
Slp setup time (to $\overline{SCKp}\downarrow$ ) <sup>Note 2</sup>	$t_{SIK1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	70			ns
Slp hold time (from $\overline{SCKp}\uparrow$ ) <sup>Note 1</sup>	$t_{SIH1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	30			ns
Slp hold time (from $\overline{SCKp}\downarrow$ ) <sup>Note 2</sup>	$t_{SIH1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	30			ns
Delay time from $\overline{SCKp}\downarrow$ to SOp output <sup>Note1</sup>	$t_{KSO1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			120	ns
Delay time from $\overline{SCKp}\uparrow$ to SOp output <sup>Note2</sup>	$t_{KSO1}$	$2.7\text{ V} \leq V_b \leq EV_{DD0}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			40	ns

- Notes**
1. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ .
  2. When  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  3.  $t_{KCY1} \geq 4/f_{MCK}$  must also be satisfied.

<R>

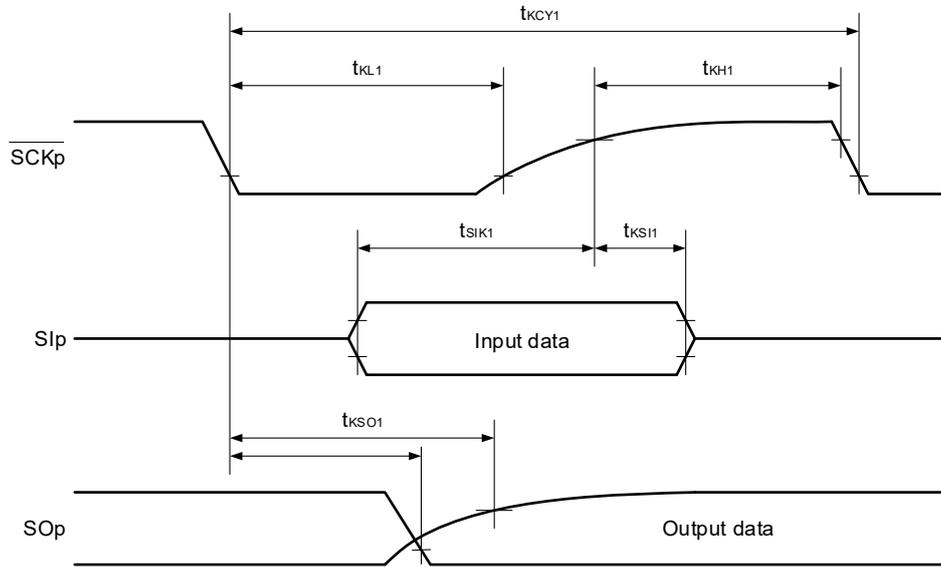
CSI mode connection diagram (during communication at different potential)



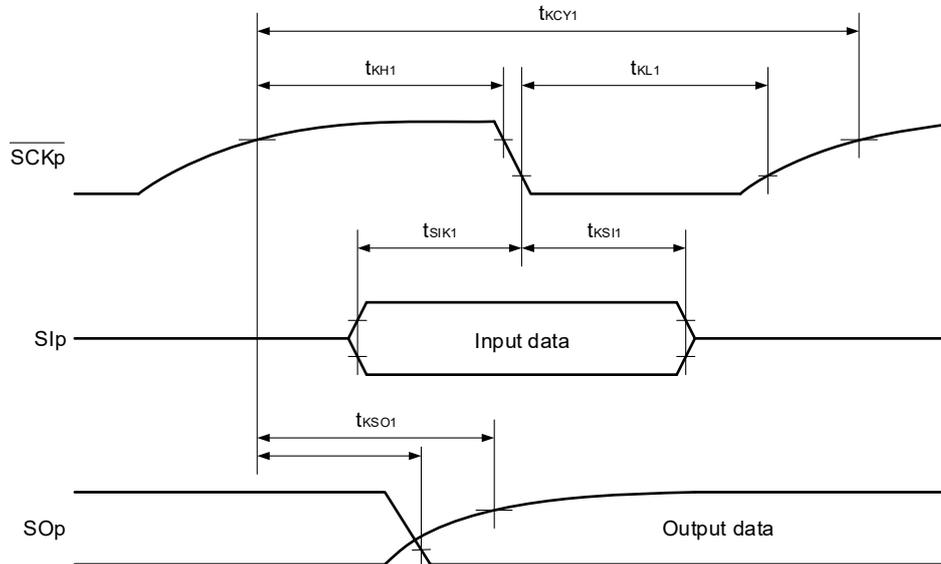
**Caution** Select the TTL input buffer for the Slp pin and N-ch open-drain output mode for the SOp pin and SCKp pin.

- Remarks**
1.  $R_b$  [ $\Omega$ ]: Communication line ( $\overline{\text{SCKp}}$ , SOp) pull-up resistance,  $C_b$  [F]: Communication line (SO,  $\overline{\text{SCKp}}$ ) load capacitance,  $V_b$  [V]: Communication line voltage
  2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)
  3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the  $V_{IH}$  and  $V_{IL}$  below:  
When  $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ ,  $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ :  $V_{IH} = 2.2\text{ V}$ ,  $V_{IL} = 0.8\text{ V}$

CSI mode serial transfer timing (master mode) (during communication at different potential)  
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)  
 (When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



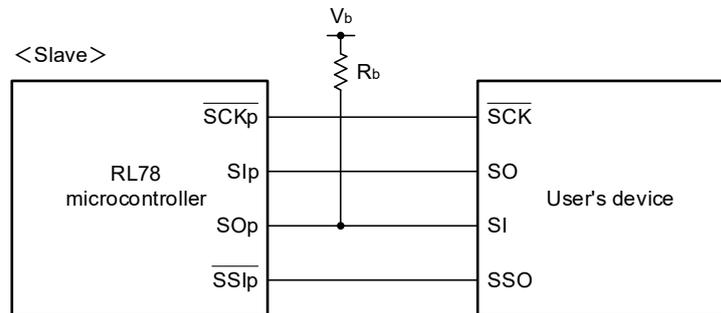
(10) During communication at different potential (3-V supply system) (CSI mode) (slave mode,  $\overline{\text{SCKp}}$  ... external clock input, normal slew rate)

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $4.0\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCKp}}$ cycle time <sup>Note 3</sup>	$t_{\text{KCY2}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{V}_{\text{DD}}$	$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$12/f_{\text{MCK}}$			ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$10/f_{\text{MCK}}$			ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$8/f_{\text{MCK}}$			ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$6/f_{\text{MCK}}$			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	$t_{\text{KH2}}$ , $t_{\text{KL2}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{V}_{\text{DD}}$	$t_{\text{KCY2}}/2 - 20$				ns
	Slp setup time (to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 1</sup>		$t_{\text{SIK2}}$	90			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 2</sup>	$t_{\text{SI2}}$		$1/f_{\text{MCK}} + 50$			ns	
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output	$t_{\text{KSO2}}$	$2.7\text{ V} \leq \text{V}_b \leq \text{V}_{\text{DD}}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			$2/f_{\text{MCK}} + 120$	ns	
SSlp setup time	$t_{\text{SSIK}}$	DAP = 0	120			ns	
		DAP = 1	$1/f_{\text{MCK}} + 120$			ns	
SSlp hold time	$t_{\text{KSSI}}$	DAP = 0	$1/f_{\text{MCK}} + 120$			ns	
		DAP = 1	120			ns	

- Notes**
- When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to  $\overline{\text{SCKp}}\downarrow$ " when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.
  - When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from  $\overline{\text{SCKp}}\downarrow$ " when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.
  - The transfer rate is MAX. 1 Mbps in SNOOSE mode.

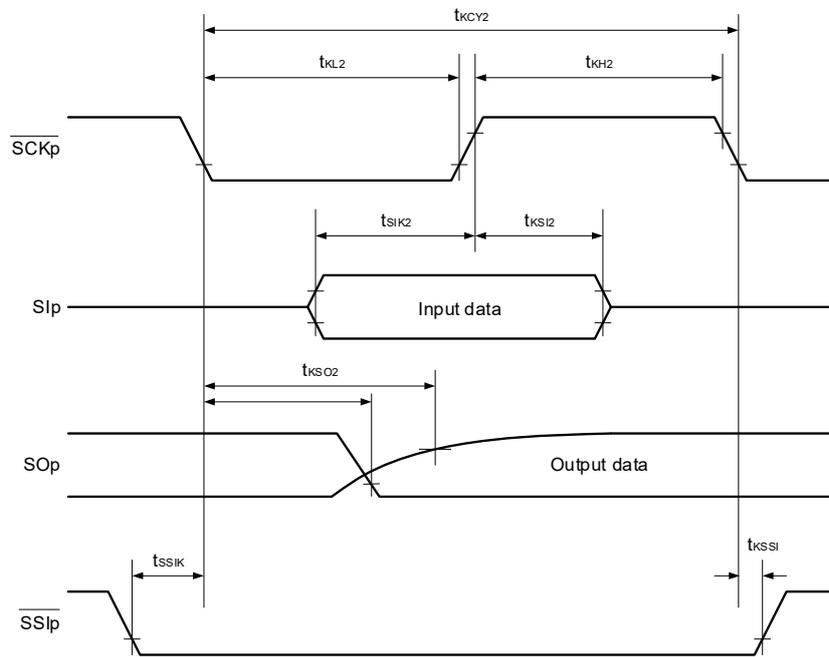
CSI mode connection diagram (during communication at different potential)



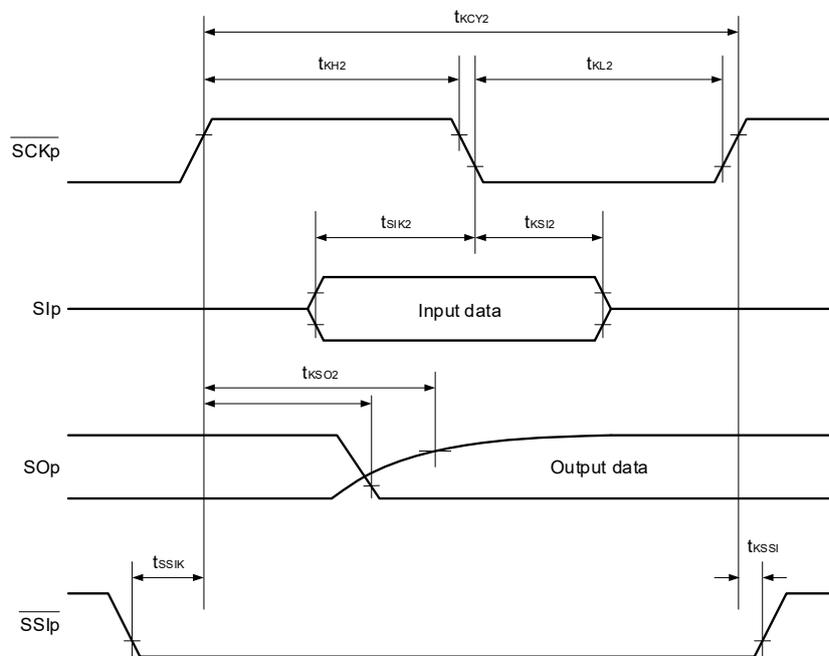
**Caution** Select the TTL input buffer for the  $\text{Slp}$ ,  $\overline{\text{SCKp}}$  and  $\overline{\text{SSIp}}$  pins and N-ch open-drain output mode for the  $\text{SOp}$  pin.

- Remarks**
- $R_b$  [ $\Omega$ ]: Communication line ( $\text{SOp}$ ) pull-up resistance,  $C_b$  [F]: Communication line ( $\text{SOp}$ ) load capacitance,  $V_b$  [V]: Communication line voltage
  - $p$ : CSIp ( $p = 00, 01, 10, 11$ ),  $m$ : Unit  $m$  ( $m = 0, 1$ ),  $n$ : Channel  $n$  ( $n = 0, 1$ )
  - AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the  $V_{IH}$  and  $V_{IL}$  below:  
When  $4.0 \text{ V} \leq E_{VDD0} \leq 5.5 \text{ V}$ ,  $2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$ :  $V_{IH} = 2.2 \text{ V}$ ,  $V_{IL} = 0.8 \text{ V}$

CSI mode serial transfer timing (slave mode) (during communication at different potential)  
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (slave mode) (during communication at different potential)  
 (When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



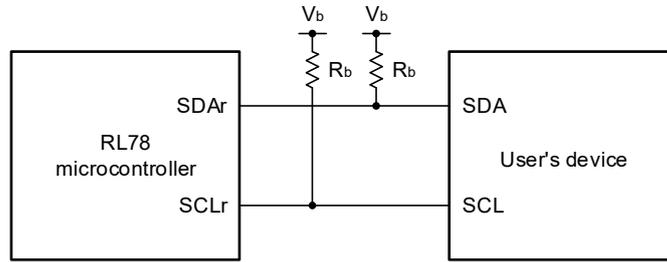
(11) During communication at different potential (3-V supply system) (simplified I<sup>2</sup>C mode)  
 (SDAr: TTL input buffer mode or N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode, SCLr: N-ch open-drain output (EV<sub>DD0</sub> tolerance) mode)

(T<sub>A</sub> = -40 to +125°C, 4.0 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

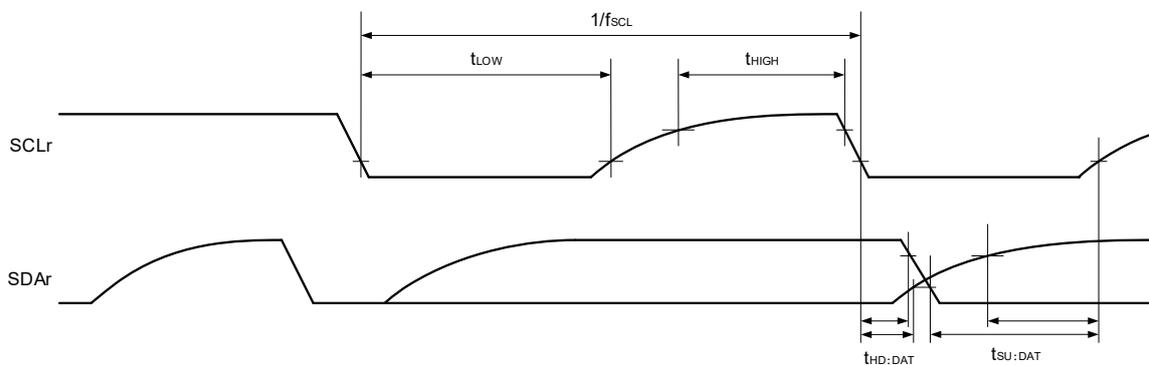
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ		400 <sup>Note</sup>	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	1200		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	600		ns
Data setup time (reception)	t <sub>SU:DAT</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	135 + 1/f <sub>MCK</sub>		ns
Data hold time (transmission)	t <sub>HD:DAT</sub>	2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 1.4 kΩ	0	140	ns

**Note** f<sub>SCL</sub> ≤ f<sub>MCK</sub>/4 must also be satisfied.

Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)



Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)



**Caution** Select the TTL input buffer and the N-ch open-drain output mode for the SDAr pin and N-ch open-drain output mode for the SCLr pin.

- Remarks**
1.  $R_b$  [ $\Omega$ ]: Communication line (SDAr, SCLr) pull-up resistance,  $C_b$  [F]: Communication line (SDAr, SCLr) load capacitance,  $V_b$  [V]: Communication line voltage
  2.  $r$ : IICr ( $r = 00, 01, 10, 11$ )
  3.  $f_{MCK}$ : Serial array unit operation clock frequency

4.5.2 Serial Interface IICA

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode plus: $10\text{ MHz} \leq f_{MCK}$					0	1000	kHz
		Fast mode: $3.5\text{ MHz} \leq f_{MCK}$			0	400			kHz
		Normal mode: $1\text{ MHz} \leq f_{MCK}$	0	100					kHz
Setup time of restart condition <sup>Note 1</sup>	t <sub>SU:STA</sub>		4.7		0.6		0.26		μs
Hold time	t <sub>HD:STA</sub>		4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t <sub>LOW</sub>		4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t <sub>HIGH</sub>		4.0		0.6		0.26		μs
Data setup time (reception)	t <sub>SU:DAT</sub>		250		100		50		ns
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>		0	3.45	0	0.9	0		μs
Setup time of stop condition	t <sub>SU:STO</sub>		4.0		0.6		0.26		μs
Bus-free time	t <sub>BUF</sub>		4.7		1.3		0.5		μs

- Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.  
**2.** The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the  $\overline{\text{ACK}}$  (acknowledge) timing.

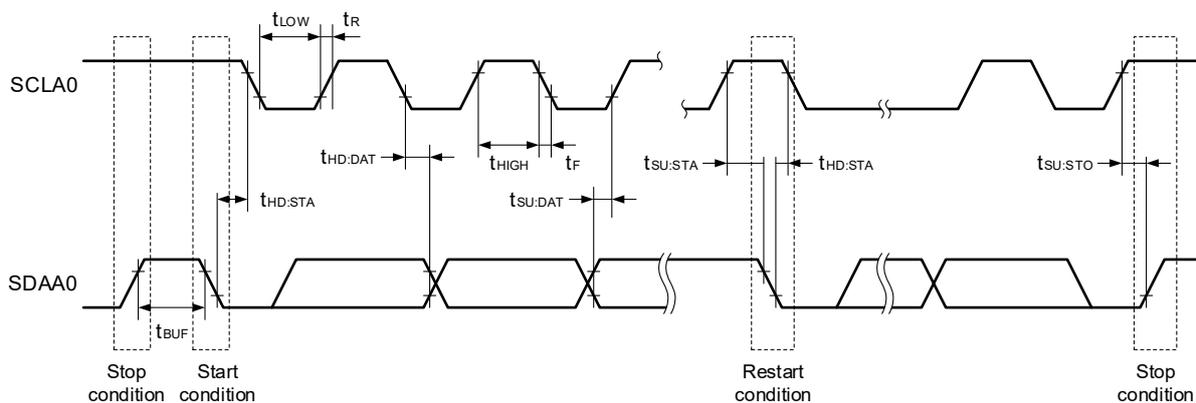
**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ

Fast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩ

Fast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ

IICA serial transfer timing



**4.5.3 On-chip Debug (UART)****(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-		115.2 k		1 M	bps

**4.5.4 LIN/UART Module (RLIN3) UART Mode****(T<sub>A</sub> = -40 to +125°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-	Operation mode, HALT mode	LIN communication clock source (f <sub>CLK</sub> or f <sub>MX</sub> ): 4 to 24 MHz			4000	kbps
		SNOOZE mode	LIN communication clock source (f <sub>CLK</sub> ): 1 to 24 MHz FRQSEL4 = 0 in the user option byte (000C2H/020C2H)			4.8	
			LIN communication clock source (f <sub>CLK</sub> ): 1 to 24 MHz FRQSEL4 = 1 in the user option byte (000C2H/020C2H)			2.4	

## 4.6 Analog Characteristics

### 4.6.1 A/D Converter Characteristics

(1) When  $AV_{REF}(+) = AV_{REFP}/ANI0$  ( $ADREFP1 = 0, ADREFP0 = 1$ ),  $AV_{REF}(-) = AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target ANI pin: ANI2 to ANI23 (power supply:  $V_{DD}$ )

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ ,

Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 3.0$	LSB
		$AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 3.5$	LSB
Conversion time	$t_{CONV}$	10-bit resolution	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
		$AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	3.1875		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EZS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.25$	%FSR
		$AV_{REFP} = V_{DD}$					
Full-scale error <sup>Notes 1, 2</sup>	EFS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.25$	%FSR
		$AV_{REFP} = V_{DD}$					
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.5$	LSB
		$AV_{REFP} = V_{DD}$					
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 1.5$	LSB
		$AV_{REFP} = V_{DD}$					
Reference voltage (+)	$AV_{REFP}$			2.7		$V_{DD}$	V
Analog input voltage	$V_{AIN}$			0		$AV_{REFP}$	V
Internal reference voltage (+)	$V_{BGR}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.38	1.45	1.5	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

(2) When  $AV_{REF}(+) = AV_{REFP}/ANI0$  ( $ADREFP1 = 0, ADREFP0 = 1$ ),  $AV_{REF}(-) = AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target ANI pin: ANI24 to ANI30 (power supply:  $EV_{DD0}$ )

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ ,

Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution $AV_{REFP} = V_{DD}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 4.5$	LSB
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 5.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution $AV_{REFP} = V_{DD}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	3.1875		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EZS	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.35$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	EFS	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.35$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 3.5$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Reference voltage (+)	$AV_{REFP}$			2.7		$V_{DD}$	V
Analog input voltage	$V_{AIN}$			0		$AV_{REFP}$ and $EV_{DD0}$	V
Internal reference voltage (+)	$V_{BGR}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.38	1.45	1.5	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

(3) When  $AV_{REF}(+) = V_{DD}$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 0$ ),  $AV_{REF}(-) = V_{SS}$  ( $ADREFM = 0$ ), target ANI pin: ANI0 to ANI23, ANI24 to ANI30

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $V_{DD}$ ,

Reference voltage (-) =  $V_{SS}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution ANI0 to ANI23	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 5.0$	LSB
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 5.5$	LSB
		10-bit resolution ANI24 to ANI30	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$\pm 1.2$	$\pm 6.5$	LSB
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		$\pm 1.2$	$\pm 7.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	3.1875		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EVS	10-bit resolution ANI0 to ANI23	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.50$	%FSR
		10-bit resolution ANI24 to ANI30	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	EFS	10-bit resolution ANI0 to ANI23	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.50$	%FSR
		10-bit resolution ANI24 to ANI30	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution ANI0 to ANI23	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 3.5$	LSB
		10-bit resolution ANI24 to ANI30	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 4.0$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Analog input voltage	$V_{AIN}$	ANI0 to ANI23 <sup>Note 3</sup>		0		$V_{DD}$	V
		ANI24 to ANI30 <sup>Note 3</sup>		$EV_{SS}$		$EV_{DD0}$	V
Internal reference voltage (+)	$V_{BGR}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.38	1.45	1.5	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** The number of pins depends on the product. For details, refer to **2.1 Pin Function List**.

(4) When  $AV_{REF}(+) = \text{internal reference voltage (ADREFP1 = 1, ADREFP0 = 0)}$ ,  $AV_{REF}(-) = AV_{REFM}/ANI1$   
( $ADREFM = 1$ ), target ANI pin: ANI0, ANI2 to ANI23, ANI24 to ANI30

&lt;R&gt;

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $V_{BGR}$ ,

Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	$t_{CONV}$	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EZS	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 1.0$	LSB
Reference voltage (+)	$V_{BGR}$			1.38	1.45	1.5	V
Analog input voltage	$V_{AIN}$			0		$V_{BGR}$	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

#### 4.6.2 Temperatures Sensor Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	$V_{\text{TMP}S25}$	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.1		V
Reference output voltage	$V_{\text{CONST}}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	$F_{\text{VTMP}S}$	Temperature sensor that depends on the temperature		-3.3		$\text{mV}/^\circ\text{C}$
Operation stabilization wait time	$t_{\text{AMP}}$		5			$\mu\text{s}$

#### 4.6.3 D/A Converter Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				8	bit
Overall error	AINL	Rload = 4 M $\Omega$ $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			$\pm 2.5$	LSB
		Rload = 8 M $\Omega$ $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			$\pm 2.5$	LSB
Settling time	$t_{\text{SET}}$	Cload = 20 pF $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			3	$\mu\text{s}$

#### 4.6.4 Comparator Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	$V_{\text{IOCOMP}}$			$\pm 5$	$\pm 40$	mV
Input voltage range	$V_{\text{ICOMP}}$		0		$\text{V}_{\text{DD}}$	V
Response time	$t_{\text{CR}}$ , $t_{\text{CF}}$	Input amplitude $\pm 100\text{ mV}$		70	200	ns
Stabilization wait time during input channel switching <sup>Note 1</sup>	$t_{\text{WAIT}}$	Input amplitude $\pm 100\text{ mV}$	300			ns
Operation stabilization wait time <sup>Note 2</sup>	$t_{\text{CMP}}$	$3.3\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$	1			$\mu\text{s}$
		$2.7\text{ V} \leq \text{V}_{\text{DD}} < 3.3\text{ V}$	3			$\mu\text{s}$

- Notes**
1. Period of time from when the comparator input channel is switched until the comparator is switched to output
  2. Period of time from when the comparator operation is enabled (HCOMPON bit in CMPCTL is set to 1) until the comparator satisfies the DC/AC characteristics.

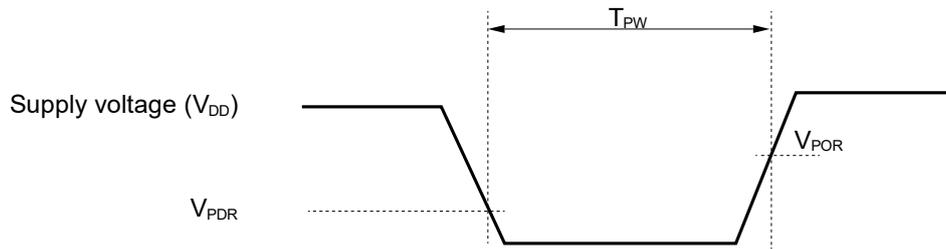
4.6.5 POR Circuit Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage <sup>Note1</sup>	$V_{POR}$	Power supply rise time	1.48	1.56	1.62	V
	$V_{PDR}$	Power supply fall time	1.47	1.55	1.61	V
Minimum pulse width <sup>Note2</sup>	$T_{PW}$		300			$\mu\text{s}$
Detection delay time	$T_{PD}$				350	$\mu\text{s}$

**Notes 1.** This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).

**2.** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ .



## 4.6.6 LVD Circuit Characteristics

## (1) LVD detection voltage of interrupt mode or reset mode

(T<sub>A</sub> = -40 to +125°C, V<sub>PDR</sub> ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	V <sub>LVD0</sub>	Power supply rise time	4.62	4.74	4.94	V		
			Power supply fall time	4.52	4.64	4.84	V		
		V <sub>LVD1</sub>	Power supply rise time	4.50	4.62	4.82	V		
			Power supply fall time	4.40	4.52	4.71	V		
		V <sub>LVD2</sub>	Power supply rise time	4.30	4.42	4.61	V		
			Power supply fall time	4.21	4.32	4.51	V		
		V <sub>LVD3</sub>	Power supply rise time	3.13	3.22	3.39	V		
			Power supply fall time	3.07	3.15	3.31	V		
		V <sub>LVD4</sub>	Power supply rise time	2.95	3.02	3.17	V		
			Power supply fall time	2.89	2.96	3.09	V		
		V <sub>LVD5</sub>	Power supply rise time	2.74	2.81	2.95	V		
			Power supply fall time	2.68 <sup>Note</sup>	2.75	2.88	V		
		Minimum pulse width		t <sub>LW</sub>		300			μs
		Detection delay time		t <sub>LD</sub>				300	μs

**Note** The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V<sub>DD</sub> = 2.7 V) is possible until a reset is effected at the power supply falling time.

## (2) LVD detection voltage of interrupt &amp; reset mode

(T<sub>A</sub> = -40 to +125°C, V<sub>PDR</sub> ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	V <sub>LVD5</sub>	VPOC2, VPOC1, VPOC0 = 0, 0, 1 <sup>Note 1</sup> , falling reset voltage: 2.75 V	2.68 <sup>Note 2</sup>	2.75	2.88	V	
	V <sub>LVD2</sub>	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.61	V
			Falling interrupt voltage	4.21	4.32	4.51	V
	V <sub>LVD5</sub>	VPOC2, VPOC1, VPOC0 = 0, 1, 0 <sup>Note 1</sup> , falling reset voltage: 2.75 V	2.68 <sup>Note 2</sup>	2.75	2.88	V	
	V <sub>LVD1</sub>	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.82	V
			Falling interrupt voltage	4.40	4.52	4.71	V
	V <sub>LVD5</sub>	VPOC2, VPOC1, VPOC0 = 0, 1, 1 <sup>Note 1</sup> , falling reset voltage: 2.75 V	2.68 <sup>Note 2</sup>	2.75	2.88	V	
	V <sub>LVD3</sub>	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.39	V
			Falling interrupt voltage	3.07	3.15	3.31	V
	V <sub>LVD0</sub>	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.94	V
			Falling interrupt voltage	4.52	4.64	4.84	V

**Notes 1.** These values indicate setting values of option bytes.

**2.** The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V<sub>DD</sub> = 2.7 V) is possible until a reset is effected at the power supply falling time.

#### 4.7 Power Supply Voltage Rising Time

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum power supply voltage rising slope	$S_{Vmax}$	$0\text{ V} \rightarrow V_{DD}$ ( $VPOC2 = 0$ or $1$ <sup>Note 2</sup> )			$50$ <sup>Note 3</sup>	V/ms
Minimum power supply voltage rising slope <sup>Note 1</sup>	$S_{Vmin}$	$0\text{ V} \rightarrow 2.7\text{ V}$	6.5			V/ms

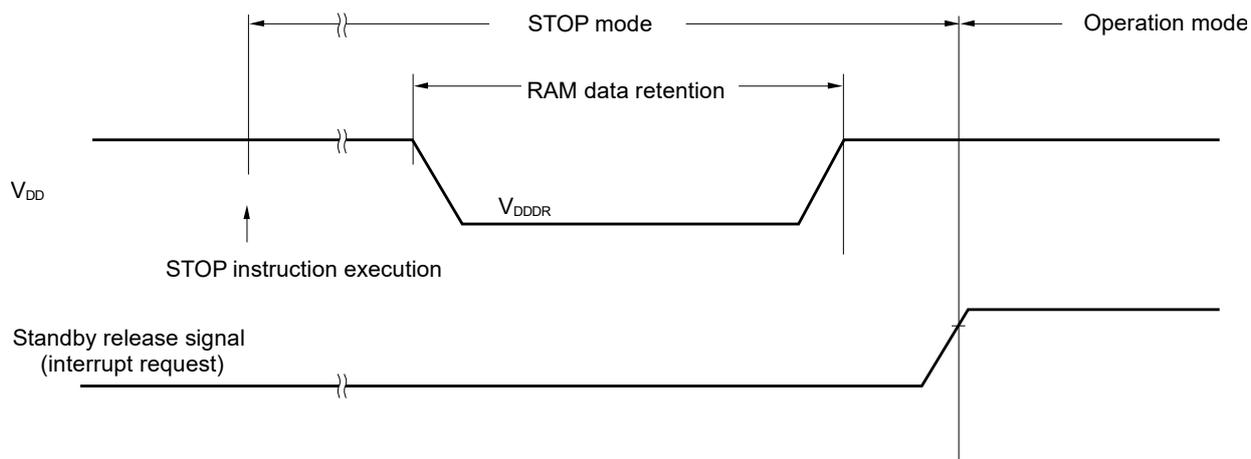
- Notes 1.** The minimum power supply voltage rising slope is applied only under the following condition.  
When the voltage detection (LVD) circuit is not used ( $VPOC2 = 1$ ) and an external reset circuit is not used or when a reset is not effected until  $V_{DD} = 2.7\text{ V}$ .
- 2.** These values indicate setting values of option bytes.
- 3.** If the power supply drops below  $V_{PDR}$  and a POR reset is effected, this specification is also applied when the power supply is recovered without dropping to  $0\text{ V}$ .

### 4.8 RAM Data Retention Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.47 <sup>Note</sup>		5.5	V

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



### 4.9 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7$  V  $\leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5$  V,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0$  V)

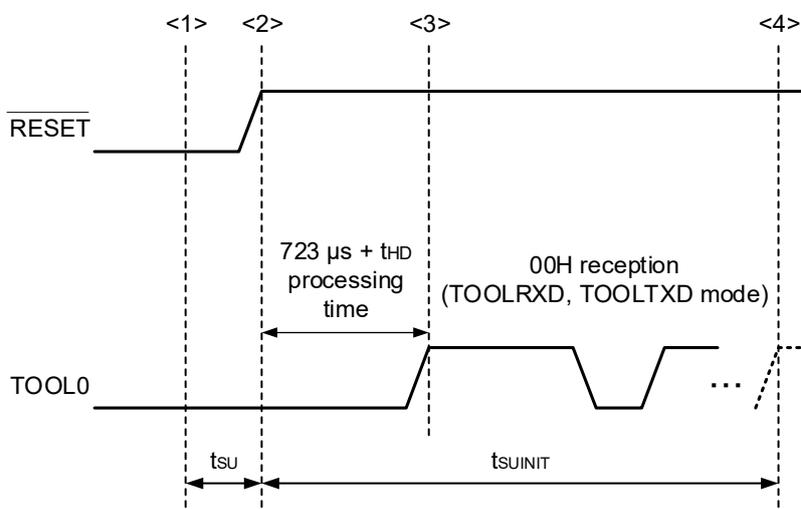
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	$f_{CLK}$		1		24	MHz
Number of code flash rewrites <sup>Notes 1, 2, 3</sup>	$C_{erwr}$	Retained for 20 years $T_A = +85^\circ\text{C}$ <sup>Note 4</sup>	1,000			Times
Number of data flash rewrites <sup>Notes 1, 2, 3</sup>		Retained for 20 years $T_A = +85^\circ\text{C}$ <sup>Note 4</sup>	10,000			
		Retained for 5 years $T_A = +85^\circ\text{C}$ <sup>Note 4</sup>	100,000			
Erase time	$T_{erasa}$	Block erase	5			ms
Write time	$T_{wrwa}$	1 word write	10			$\mu\text{s}$

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The starting point of the retaining years are after the erase.
  2. When using flash memory programmer and Renesas Electronics self programming library
  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
  4. The average temperature for data retention.

4.10 Timing of Entry to Flash Memory Programming Modes

( $T_A = -40$  to  $+125^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset must be released before the external reset is released.	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

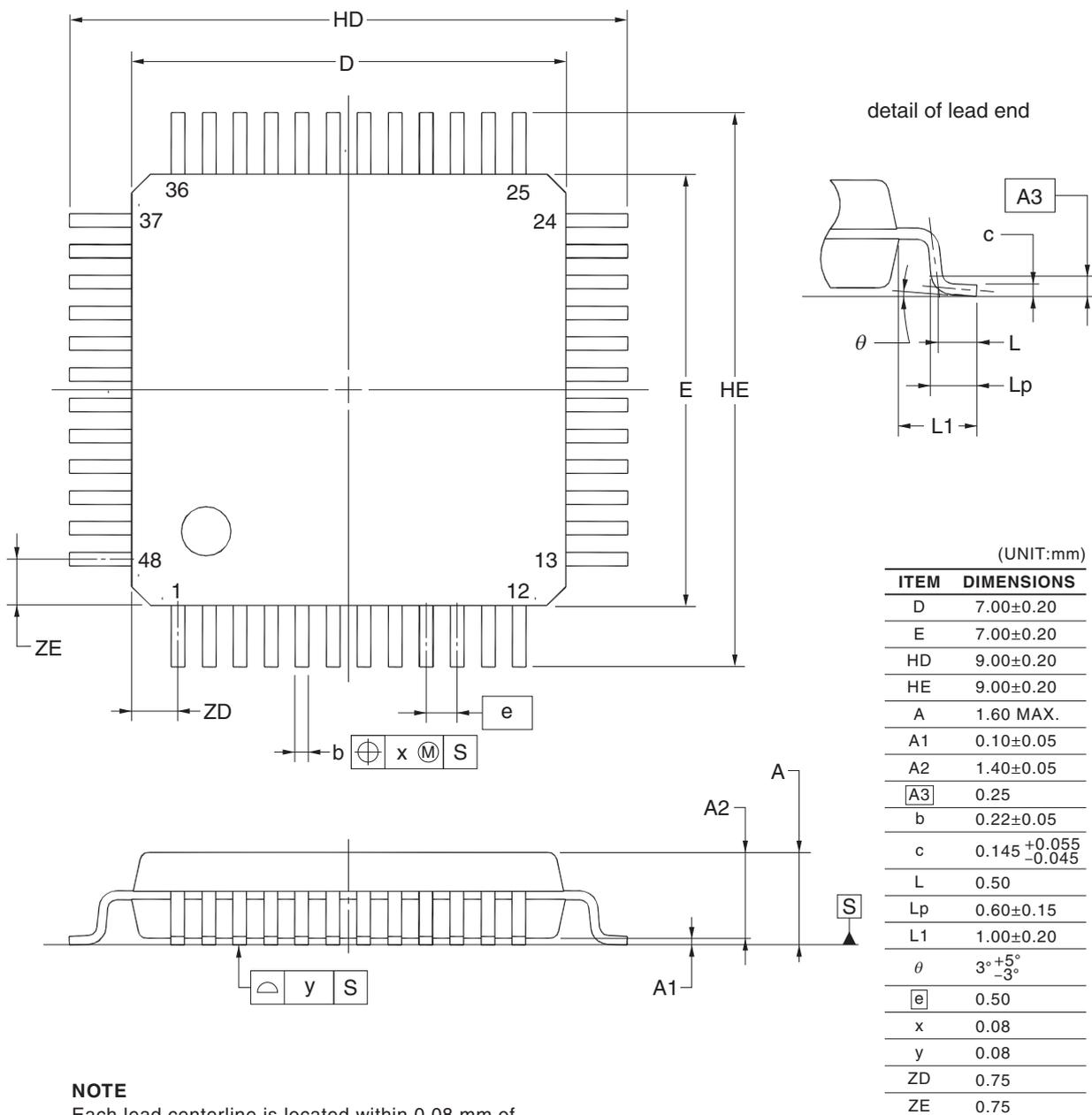
## 5. PACKAGE DRAWING

### 5.1 48-pin products

<R>

#### 5.1.1 48-pin LFQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

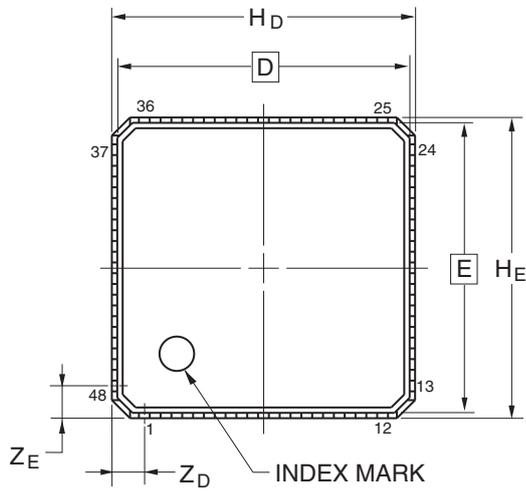


**NOTE**

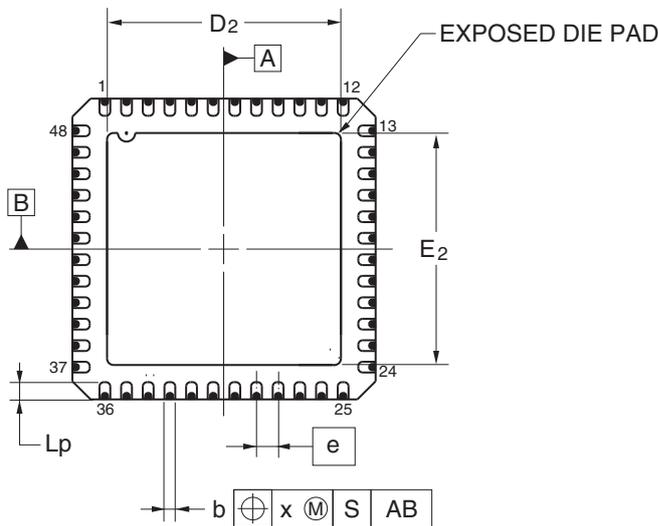
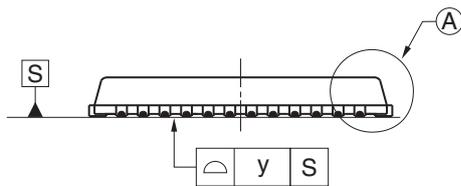
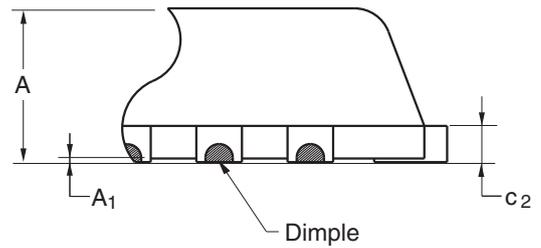
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

<R> 5.1.2 48-pin HVQFN

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN48-7x7-0.50	PVQN0048KG-A	P48K9-50A-BAJ	0.13



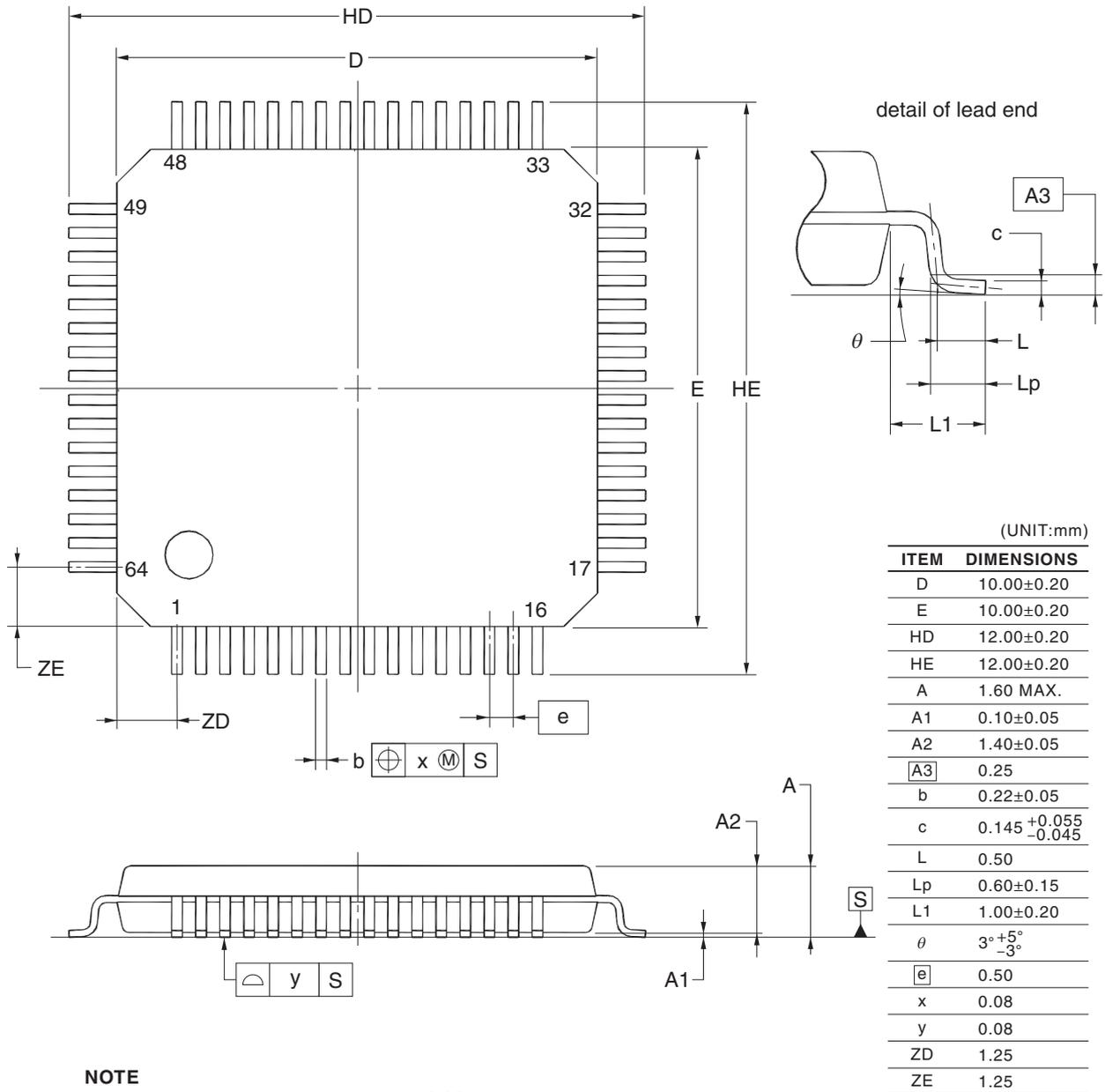
DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.75	—
E	—	6.75	—
A	—	—	0.90
A <sub>1</sub>	0.00	—	—
b	0.20	0.25	0.30
e	—	0.50	—
L <sub>p</sub>	0.30	0.40	0.50
x	—	—	0.10
y	—	—	0.05
H <sub>D</sub>	6.95	7.00	7.05
H <sub>E</sub>	6.95	7.00	7.05
Z <sub>D</sub>	—	0.75	—
Z <sub>E</sub>	—	0.75	—
c <sub>2</sub>	0.19	0.20	0.21
D <sub>2</sub>	—	5.40	—
E <sub>2</sub>	—	5.40	—

5.2 64-pin products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

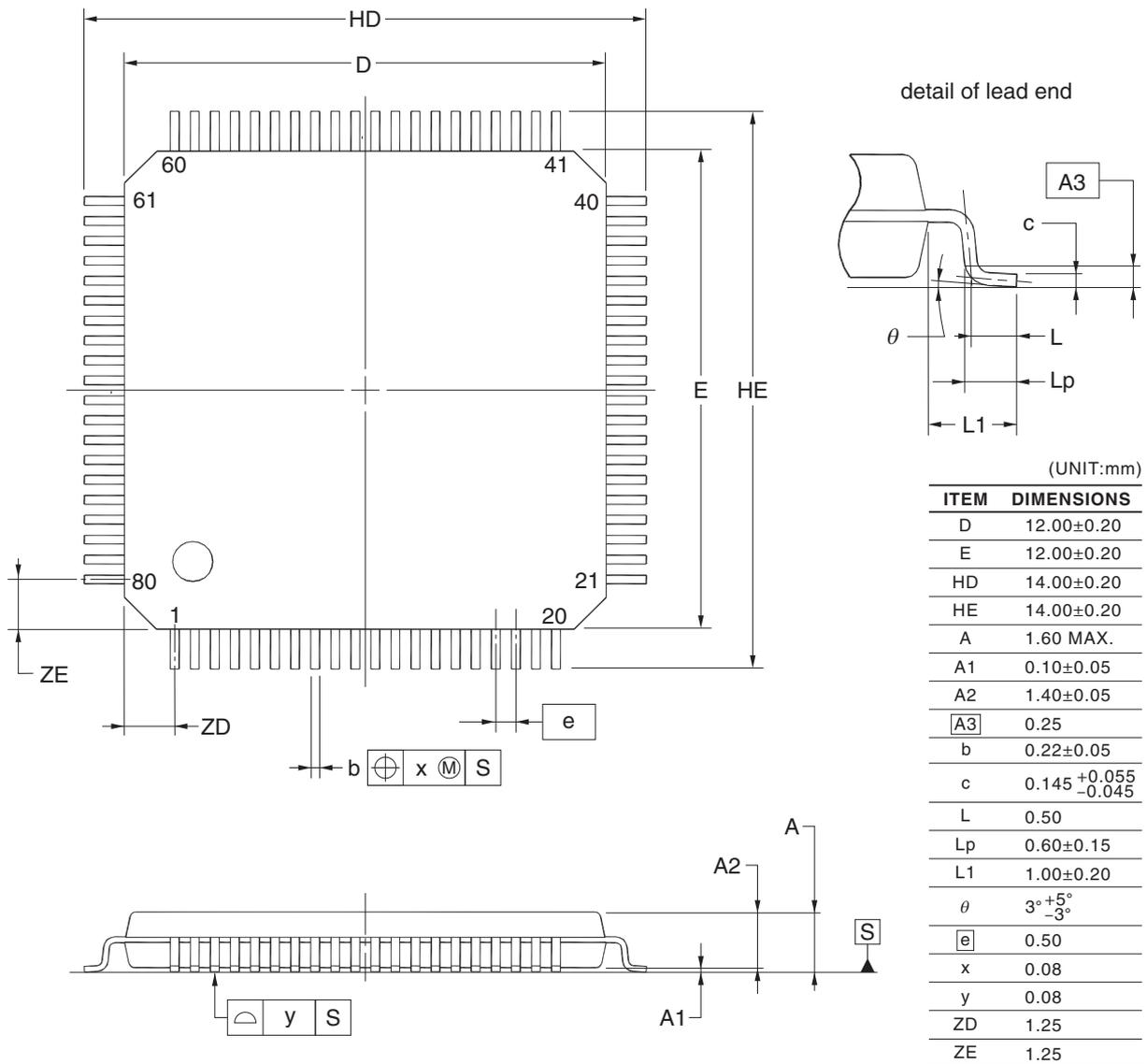


**NOTE**  
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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5.3 80-pin products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53

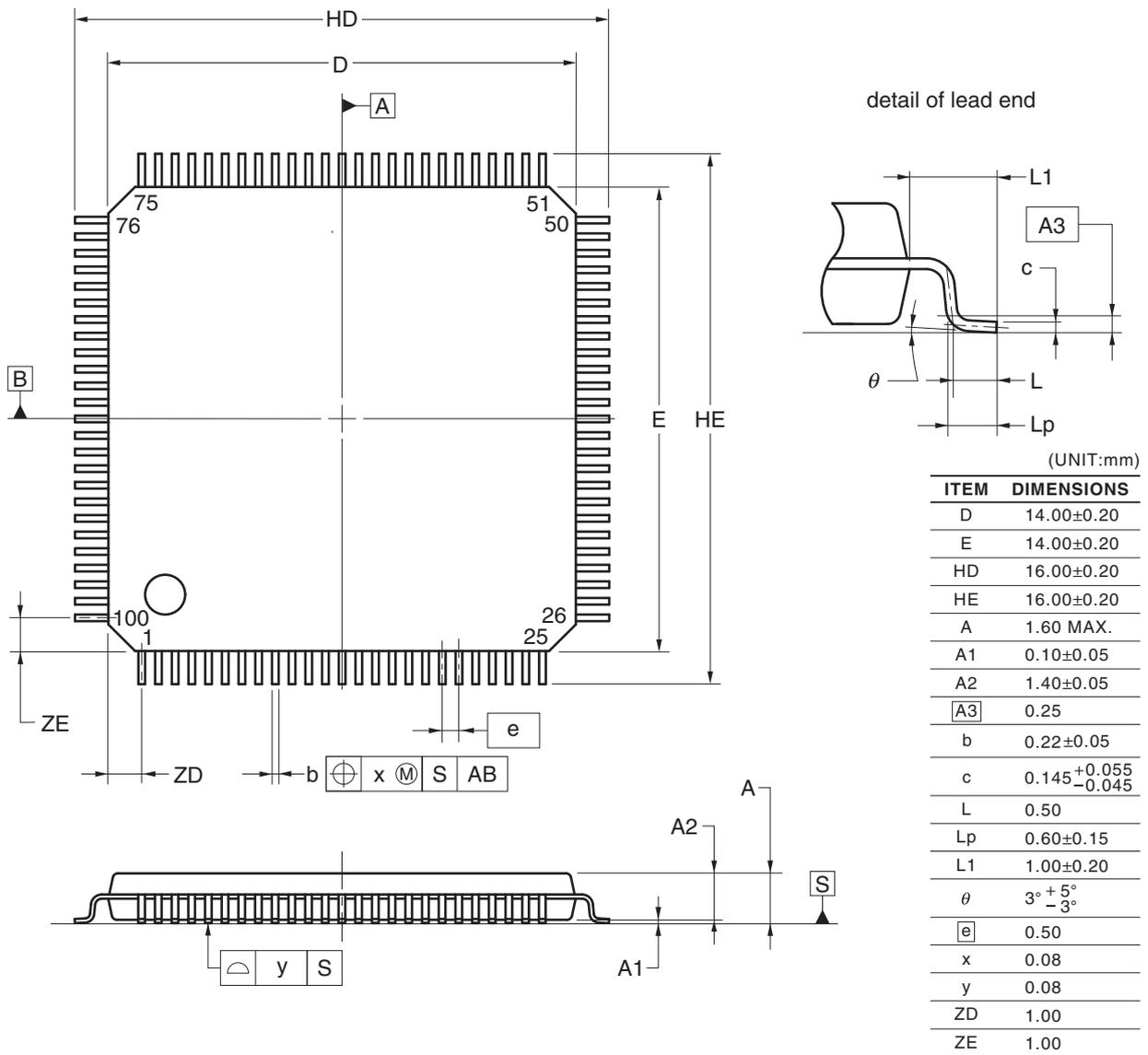


**NOTE**  
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5.4 100-pin products

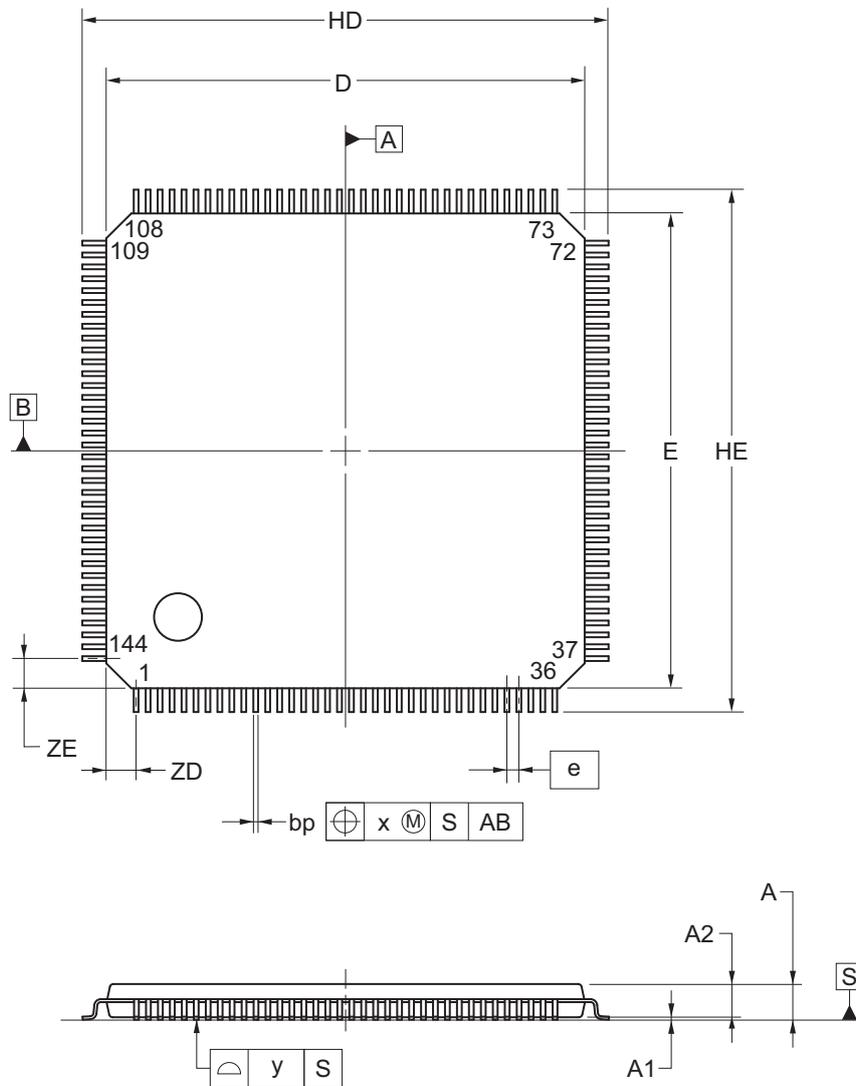
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



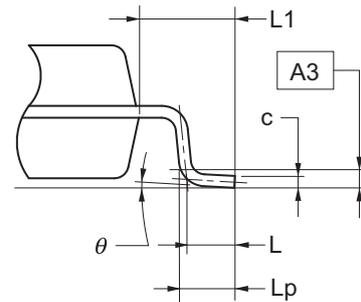
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5.5 144-pin products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP144-20x20-0.50	PLQP0144KD-E	P144GJ-50-UEN	1.3



detail of lead end



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.80	20.00	20.20
E	19.80	20.00	20.20
HD	21.80	22.00	22.20
HE	21.80	22.00	22.20
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.17	0.22	0.27
c	0.10	0.145	0.20
L	—	0.50	—
Lp	0.45	0.60	0.75
L1	0.80	1.00	1.20
$\theta$	0°	3°	8°
e	—	0.50	—
x	—	—	0.08
y	—	—	0.08
ZD	—	1.25	—
ZE	—	1.25	—

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## REVISION HISTORY

## RL78/F15 Datasheet

Rev	Date	Description	
		Page	Summary
1.00	Dec 27, 2024	–	First edition issued.
1.10	Jan 30, 2026	p.1	Modification of description in 1.1 Features
		p.2	Modification of Table 1-1. RL78/F15 Lineup in 1.2 Product Lineup
		p.10	Modification of title in 1.5.1 RL78/F15 Pin Configuration for 144-pin Products
		p.11	Modification of title in 1.5.2 RL78/F15 Pin Configuration for 100-pin Products
		p.12	Modification of title in 1.5.3 RL78/F15 Pin Configuration for 80-pin Products
		p.13	Modification of title in 1.5.4 RL78/F15 Pin Configuration for 64-pin Products
		p.14	Modification of title in 1.5.5 RL78/F15 Pin Configuration for 48-pin Products
		p.15	Modification of description in Table 1-3. Order Information for RL78/F15
		p.41 to 46	Modification of table in 3.3.1 Pin Characteristics
		p.41	Addition of Caution in 3.3.1 Pin Characteristics
		p.53	Modification of figure in 3.4.1 Basic Operation
		p.56	Modification of Note 4 in 3.5.1 Serial Array Unit (2)
		p.57	Modification of Note 4 in 3.5.1 Serial Array Unit (3)
		p.67	Modification of Note 3 in 3.5.1 Serial Array Unit (9)
		p.74	Modification of table in 3.5.2 Serial Interface IICA
		p.79	Modification of title in 3.6.1 A/D Converter Characteristics (4)
		p.81	Addition of Note 2 in 3.6.5 POR Circuit Characteristics
		p.81	Addition of figure in 3.6.5 POR Circuit Characteristics
		p.84	Modification of title in 3.8 RAM Data Retention Characteristics
		p.84	Modification of Note in 3.8 RAM Data Retention Characteristics
		p.84	Modification of figure in 3.8 RAM Data Retention Characteristics
		p.85	Modification of table in 3.9 Flash Memory Programming Characteristics
		p.85	Modification of Note 1 in 3.9 Flash Memory Programming Characteristics
		p.94 to 99	Modification of table in 4.3.1 Pin Characteristics
		p.94	Addition of Caution in 4.3.1 Pin Characteristics
		p.105	Modification of figure in 4.4.1 Basic Operation
		p.108	Modification of Note 4 in 4.5.1 Serial Array Unit (2)
		p.109	Modification of Note 4 in 4.5.1 Serial Array Unit (3)
		p.118	Modification of Note 3 in 4.5.1 Serial Array Unit (9)
		p.126	Modification of table in 4.5.2 Serial Interface IICA
		p.131	Modification of title in 4.6.1 A/D Converter Characteristics (4)
		p.133	Addition of Note 2 in 4.6.5 POR Circuit Characteristics
		p.133	Addition of figure in 4.6.5 POR Circuit Characteristics
p.136	Modification of title in 4.8 RAM Data Retention Characteristics		
p.136	Modification of Note in 4.8 RAM Data Retention Characteristics		
p.136	Modification of figure in 4.8 RAM Data Retention Characteristics		
p.136	Modification of table in 4.9 Flash Memory Programming Characteristics		
p.136	Modification of Note 1 in 4.9 Flash Memory Programming Characteristics		
p.138	Modification of title in 5.1.1 48-pin LQFP		
p.139	Modification of title in 5.1.2 48-pin HVQFN		

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## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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