RL78/F12

RENESAS MCU

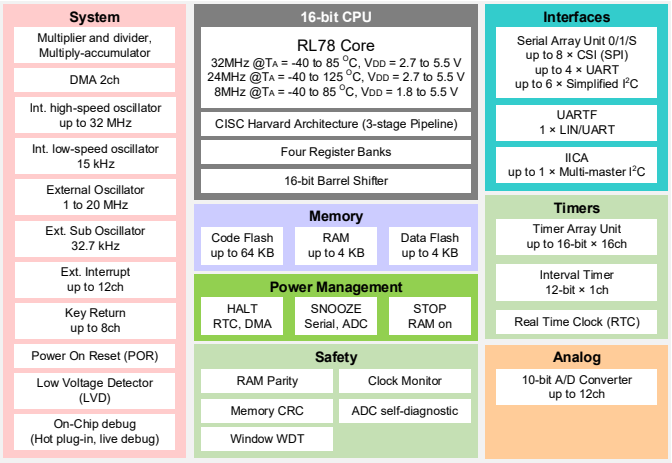
R01DS0462EJ0120
Rev.1.20
May 30, 2025

RL78/F12 microcontrollers are available in a 20 to 64-pin, 8 to 64 KB flash memory lineup, and realize the industry's lowest level of consumption current. They have a built-in LIN module as an automotive interface. With various built-in functions for realizing functional safety including flash memory CRC calculation, illegal memory access detection, RAM guard, A/D converter testing, and SFR guard, a highly reliable system can be built, so these microcontrollers can be used for industrial applications and of course automotive applications.

1. OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.03125 μs: @ 32 MHz operation with high-speed on-chip oscillator) to ultra low-speed (30.5 μs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM: 8 to 64 KB, RAM: 0.5 to 4 KB, Data flash memory: 4 KB
- High-speed on-chip oscillator
  Select from 32 MHz (TYP.), 24 MHz (TYP.), 16 MHz (TYP.), 12 MHz (TYP.), 8 MHz (TYP.), 4 MHz (TYP.), and 1 MHz (TYP.)
- On-chip single-power-supply flash memory
  (with prohibition of block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the dedicated internal low-speed on-chip oscillator)
- On-chip multiplier and divider/multiply-accumulator
  16 bits × 16 bits = 32 bits (Unsigned or signed)
  32 bits ÷ 32 bits = 32 bits (Unsigned)
  16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 16 to 44 (N-ch open drain: 0 to 4)
- Timer
  - 16-bit timer: 8 channels
  - Watchdog timer: 1 channel
  - Real-time clock: 1 channel
  Interval timer: 1 channel
  - Wakeup timer: 1 channel
- Serial interface
  - CSI: 0 to 8 channels
  - UART/UART (LIN-bus supported): 1 to 5 channels
  - I^2C/Simplified I^2C communication: 0 to 7 channels
- 8/10-bit resolution A/D converter (V_{DD} = 1.8 to 5.5 V): 4 to 12 channels
- Power supply voltage:
  V_{DD} = 1.8 to 5.5 V (J version)
  V_{DD} = 2.7 to 5.5 V (K version)
- Operating ambient temperature:
  T_A = –40 to +85°C (J version)
  T_A = –40 to +125°C (K version)



RL78/F12 Block Diagram (Outline)

Remark The functions mounted depend on the product.
See **1.6 Outline of Functions**.

- ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/F12				
			20 pins	30 pins	32 pins	48 pins	64 pins
64 KB	4 KB	4 KB Note	R5F1096E	R5F109AE	R5F109BE	R5F109GE	R5F109LE
48 KB		3 KB	R5F1096D	R5F109AD	R5F109BD	R5F109GD	R5F109LD
32 KB		2 KB	R5F1096C	R5F109AC	R5F109BC	R5F109GC	R5F109LC
24 KB		1.5 KB	R5F1096B	R5F109AB	R5F109BB	R5F109GB	R5F109LB
16 KB		1 KB	R5F1096A	R5F109AA	R5F109BA	R5F109GA	R5F109LA
8 KB		0.5 KB	R5F10968	–	–	–	–

Note This is 3 KB when the self-programming function is used.

1.2 Ordering Information

	Pin count	Package	Device	Part Number
<R>	20 pins	20-pin plastic LSSOP (7.62 mm (300))	J version	R5F10968JSP, R5F10968CJSP,R5F1096AJSP, R5F1096ACJSP, R5F1096BJSP, R5F1096BCJSP, R5F1096CJSP, R5F1096CCJSP, R5F1096DJSP, R5F1096DCJSP, R5F1096EJSP, R5F1096ECJSP
			K version	R5F10968KSP, R5F10968CKSP, R5F1096AKSP, R5F1096ACKSP, R5F1096BKSP, R5F1096BCKSP, R5F1096CKSP, R5F1096CCKSP, R5F1096DKSP, R5F1096DCKSP,R5F1096EKSP, R5F1096ECKSP
<R>	30 pins	30-pin plastic LSSOP (7.62 mm (300))	J version	R5F109AAJSP, R5F109AACJSP, R5F109ABJSP, R5F109ABCJSP, R5F109ACJSP, R5F109ACCJSP, R5F109ADJSP, R5F109ADCJSP, R5F109AEJSP, R5F109AECJSP
			K version	R5F109AAKSP, R5F109AACKSP, R5F109ABKSP, R5F109ABCKSP, R5F109ACKSP, R5F109ACCKSP, R5F109ADKSP, R5F109ADCKSP, R5F109AEKSP, R5F109AECKSP
<R>	32 pins	32-pin plastic HWQFN (fine pitch) (5 × 5)	J version	R5F109BAJNA, R5F109BACJNA, R5F109BBJNA, R5F109BBCJNA, R5F109BCJNA, R5F109BCCJNA, R5F109BDJNA, R5F109BDCJNA, R5F109BEJNA, R5F109BECJNA
			K version	R5F109BAKNA, R5F109BACKNA, R5F109BBKNA, R5F109BBCKNA, R5F109BCKNA, R5F109BCCKNA, R5F109BDKNA, R5F109BDCKNA, R5F109BEKNA, R5F109BECKNA
<R>	48 pins	48-pin plastic LFQFP (fine pitch) (7 × 7)	J version	R5F109GACJFB, R5F109GBCJFB, R5F109GCCJFB, R5F109GDCJFB, R5F109GECJFB
			K version	R5F109GACKFB, R5F109GBCKFB, R5F109GCCKFB, R5F109GDCKFB, R5F109GECKFB
		48-pin plastic HWQFN (7 × 7) **Note**	J version	R5F109GAJNA, R5F109GBJNA, R5F109GCJNA, R5F109GDJNA, R5F109GEJNA
			K version	R5F109GAKNA, R5F109GBKNA, R5F109GCKNA, R5F109GDKNA, R5F109GEKNA
<R>	64 pins	64-pin plastic LFQFP (fine pitch) (10 × 10)	J version	R5F109LACJFB, R5F109LBCJFB, R5F109LCCJFB, R5F109LDCJFB, R5F109LECJFB
			K version	R5F109LACKFB, R5F109LBCKFB, R5F109LCCKFB, R5F109LDCKFB, R5F109LECKFB

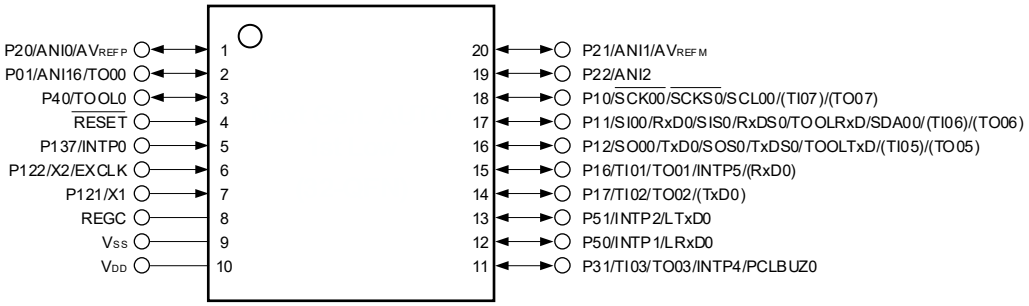
Note Contact Renesas local sales office or sales representative for further details on this package.

Caution The RL78/F12 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

<R> • 20-pin plastic LSSOP (7.62 mm (300))



Cautions 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

2. For the following each port, complete the following software processings before performing the operation that reads the port latch Pm having the target port latch Pm.n within 50ms after releasing reset (after staring CPU operation)

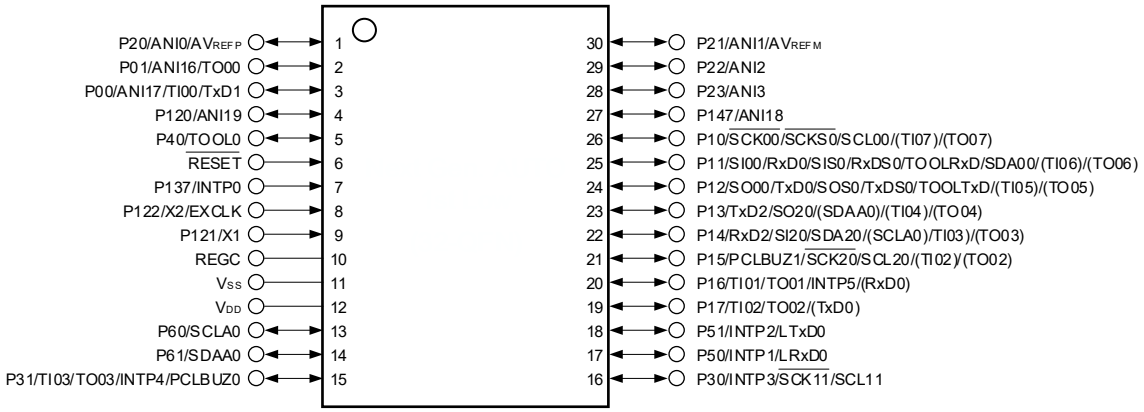
- **Set P00, P13, P14, P15, P30, P60, P61, and P147 to low level output mode by the software (clear the PMm.n and Pm.n bits for the target ports).**
- **Set P23 to digital port and low level output mode by the software (set P23 to digital mode with the ADPC register and clear the PM2.3 and P2.3 bits).**

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 30-pin products

<R> • 30-pin plastic LSSOP (7.62 mm (300))



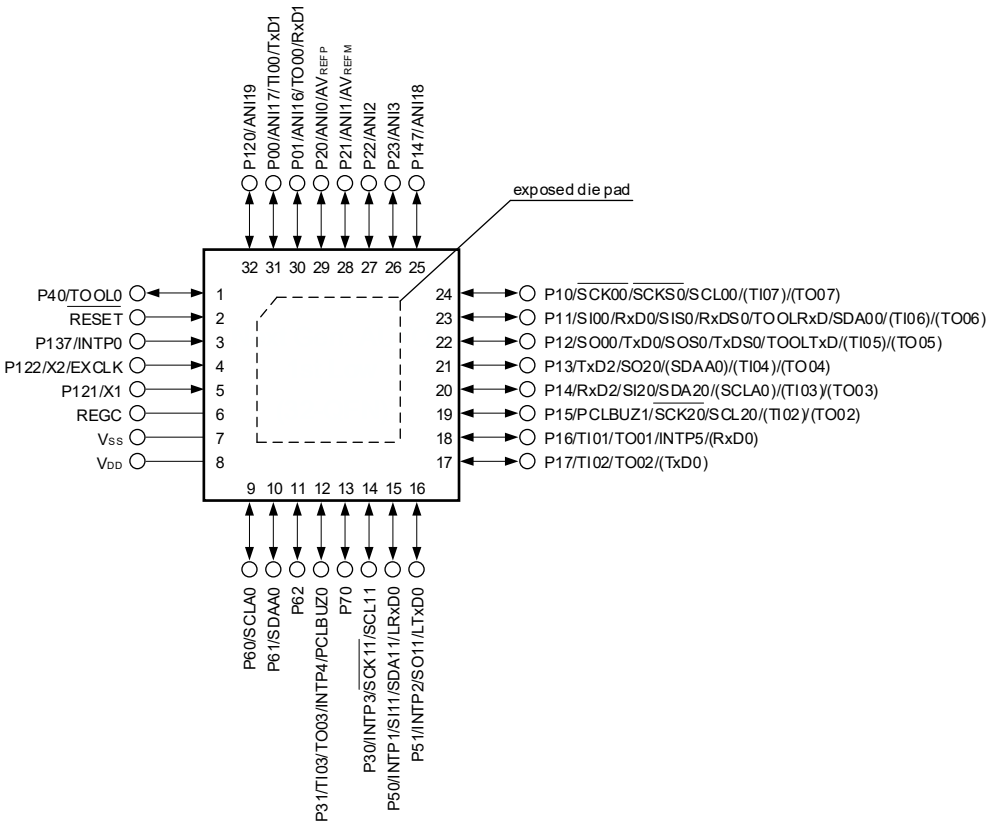
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.3 32-pin products

<R> • 32-pin plastic HWQFN (fine pitch) (5 × 5)



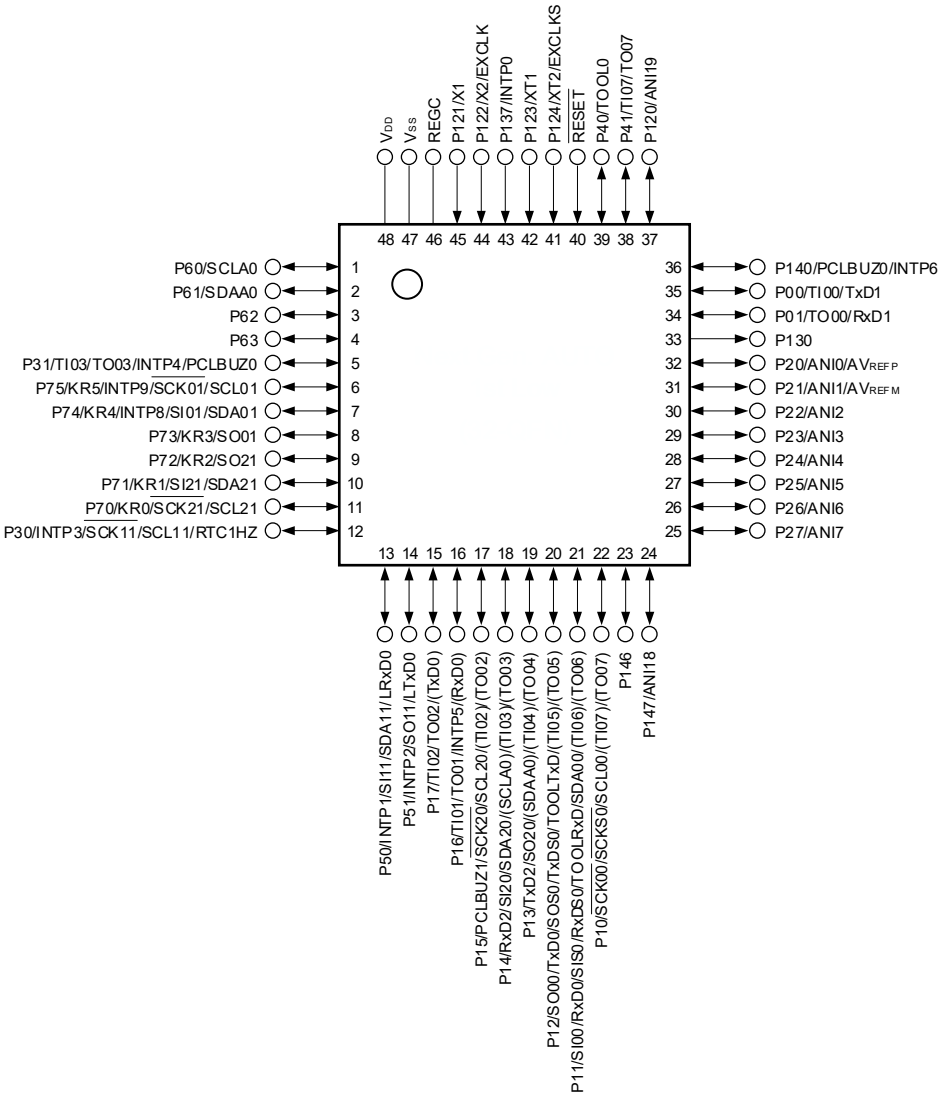
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.4 48-pin products

<R> • 48-pin plastic LFQFP (fine pitch) (7 × 7)

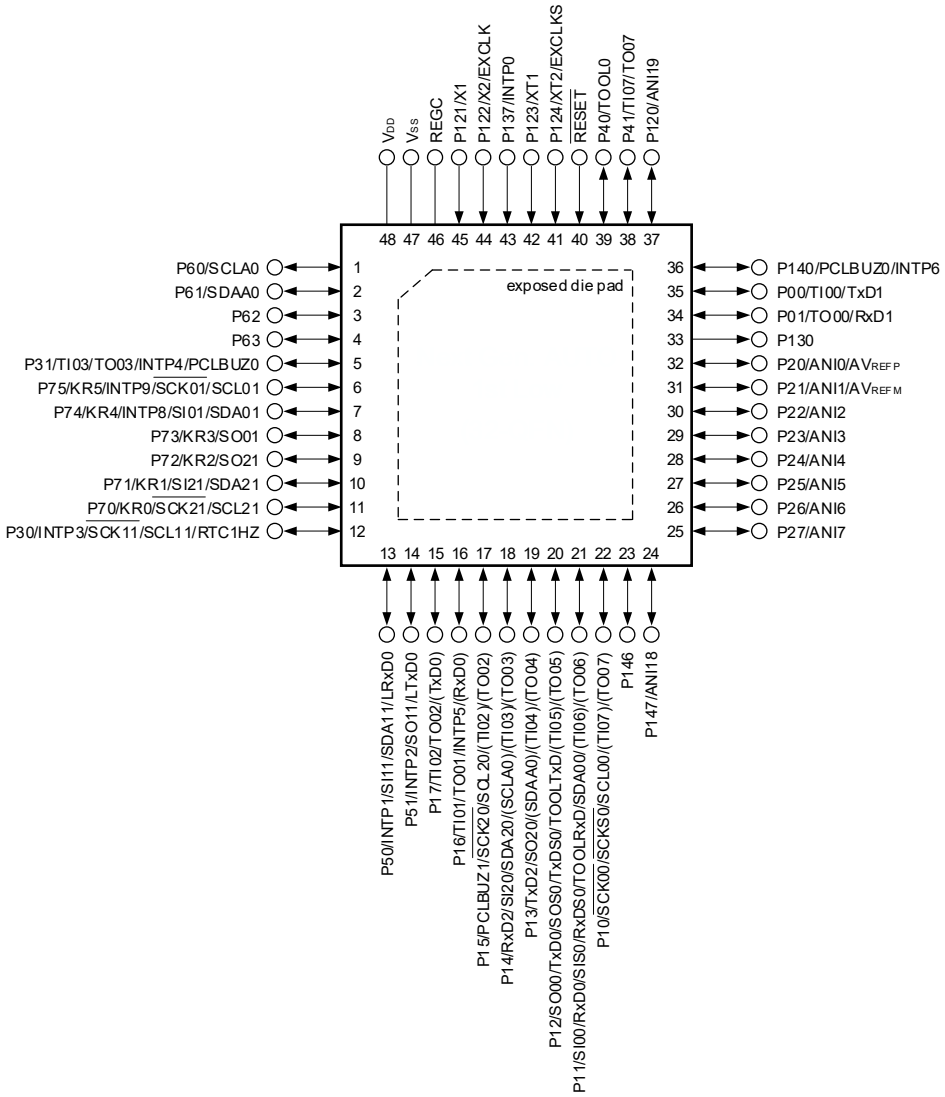


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> • 48-pin plastic HWQFN (7 × 7)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

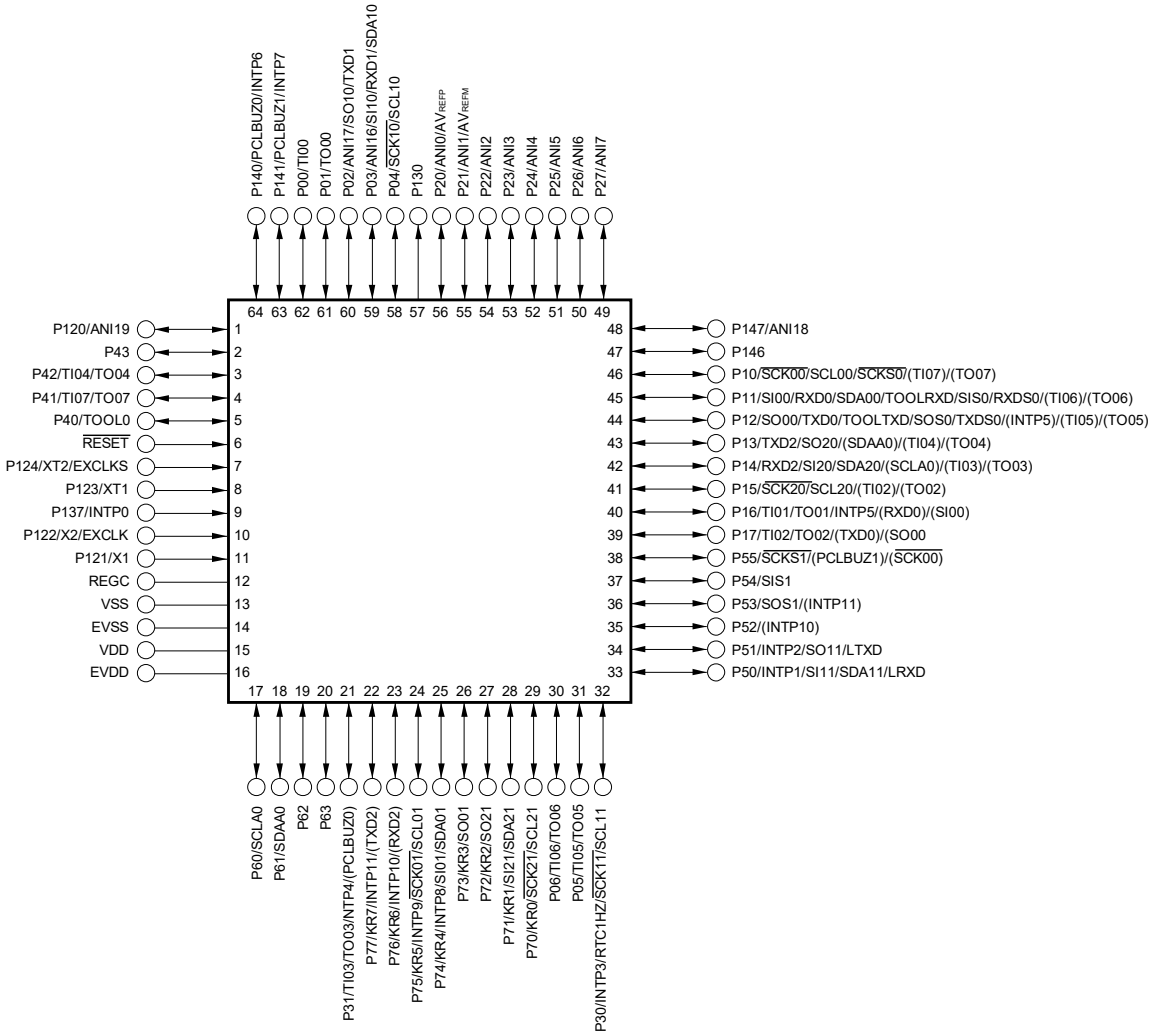
Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

3. Contact Renesas local sales office or sales representative for further details on this package.

1.3.5 64-pin products

<R> • 64-pin plastic LFQFP



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

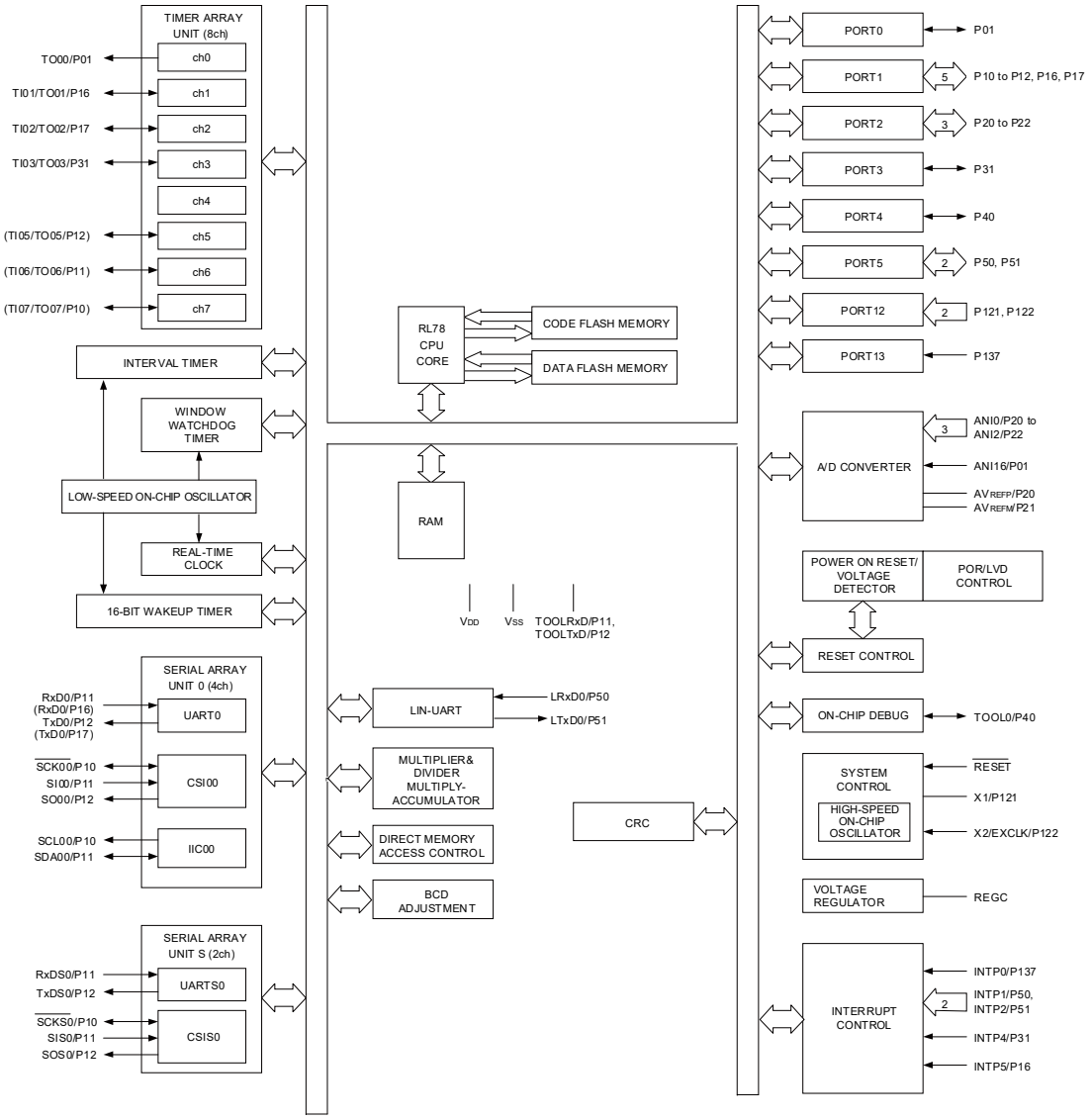
1.4 Pin Identification

ANI0 to ANI7, ANI16 to ANI19:	Analog input
AV_{REFM}:	A/D converter reference potential (– side) input
AV_{REFP}:	A/D converter reference potential (+ side) input
EXCLK:	External clock input (main system clock)
EXCLKS:	External clock input (sub system clock)
INTP0 to INTP11:	External interrupt input
KR0 to KR7:	Key return
LRxD0:	Receive Data
LTxD0:	Transmit Data
P00 to P06:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40 to P43:	Port 4
P50 to P55:	Port 5
P60 to P63:	Port 6
P70 to P77:	Port 7
P120 to P124:	Port 12
P130, P137:	Port 13
P140, P141, P146, P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Real-time clock correction clock (1 Hz) output
RxD0 to RxD2, RxDS0:	Receive data
$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, $\overline{\text{SCK21}}$, $\overline{\text{SCKS0}}$, $\overline{\text{SCKS1}}$:	Serial clock input/output
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCLA0:	Serial clock input/output
SDA00, SDA01, SDA10, SDA11,SDA20, SDA21, SDAA0:	Serial data input/output
SI00, SI01, SI10, SI11, SI20, SI21, SIS0, SIS1:	Serial data input
SO00, SO01, SO10, SO11, SO20, SO21, SOS0, SOS1:	Serial data output
TI00 to TI07:	Timer input
TO00 to TO07:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TxD0 to TxD2, TxDS0:	Transmit data
EV_{DD}, V_{DD}:	Power supply
EV_{SS}, V_{SS}:	Ground
X1, X2:	Crystal oscillator (main system clock)
XT1, XT2:	Crystal oscillator (subsystem clock)

1.5 Block Diagram

1.5.1 20-pin products

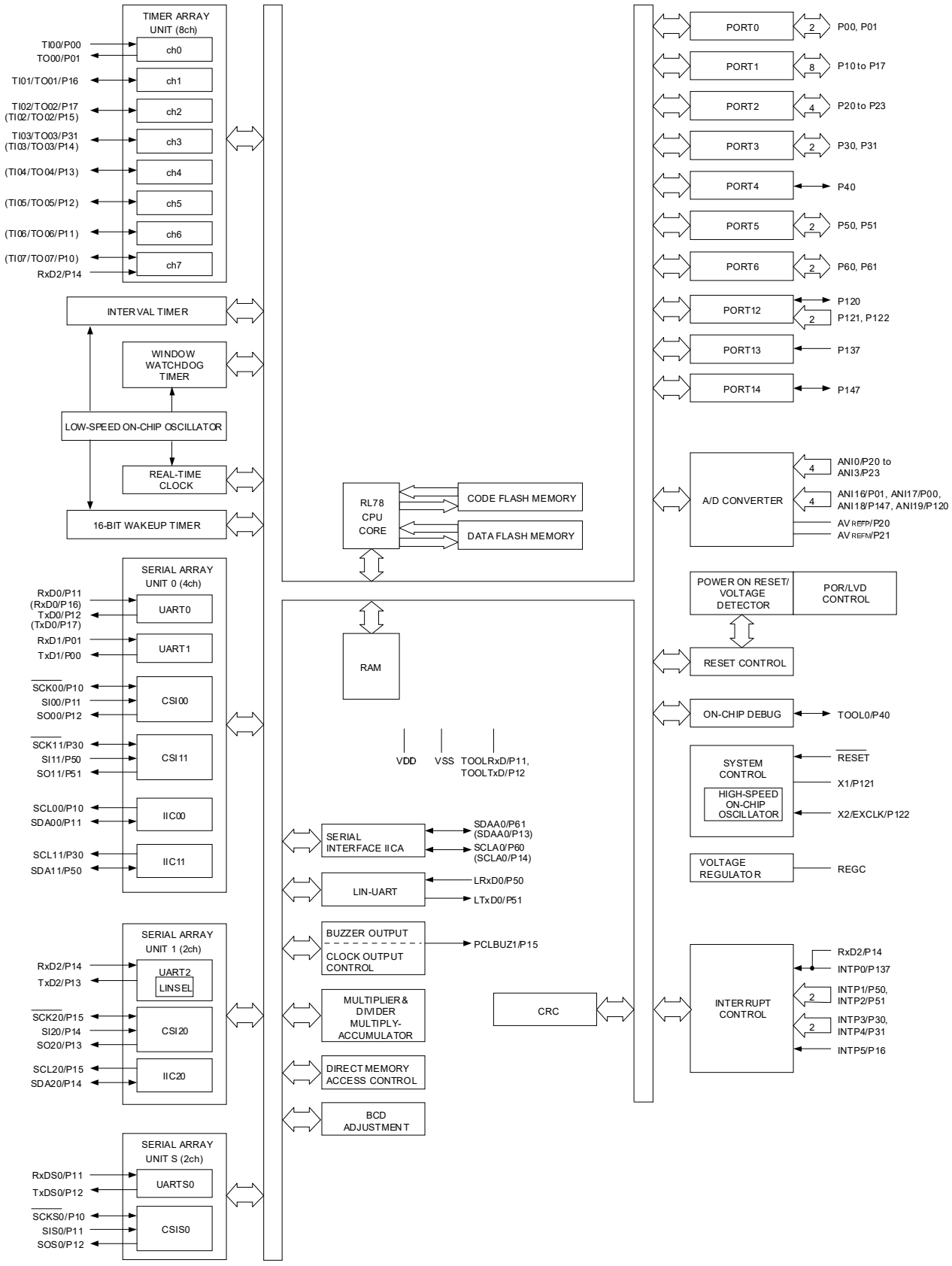
<R>



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.2 30-pin products

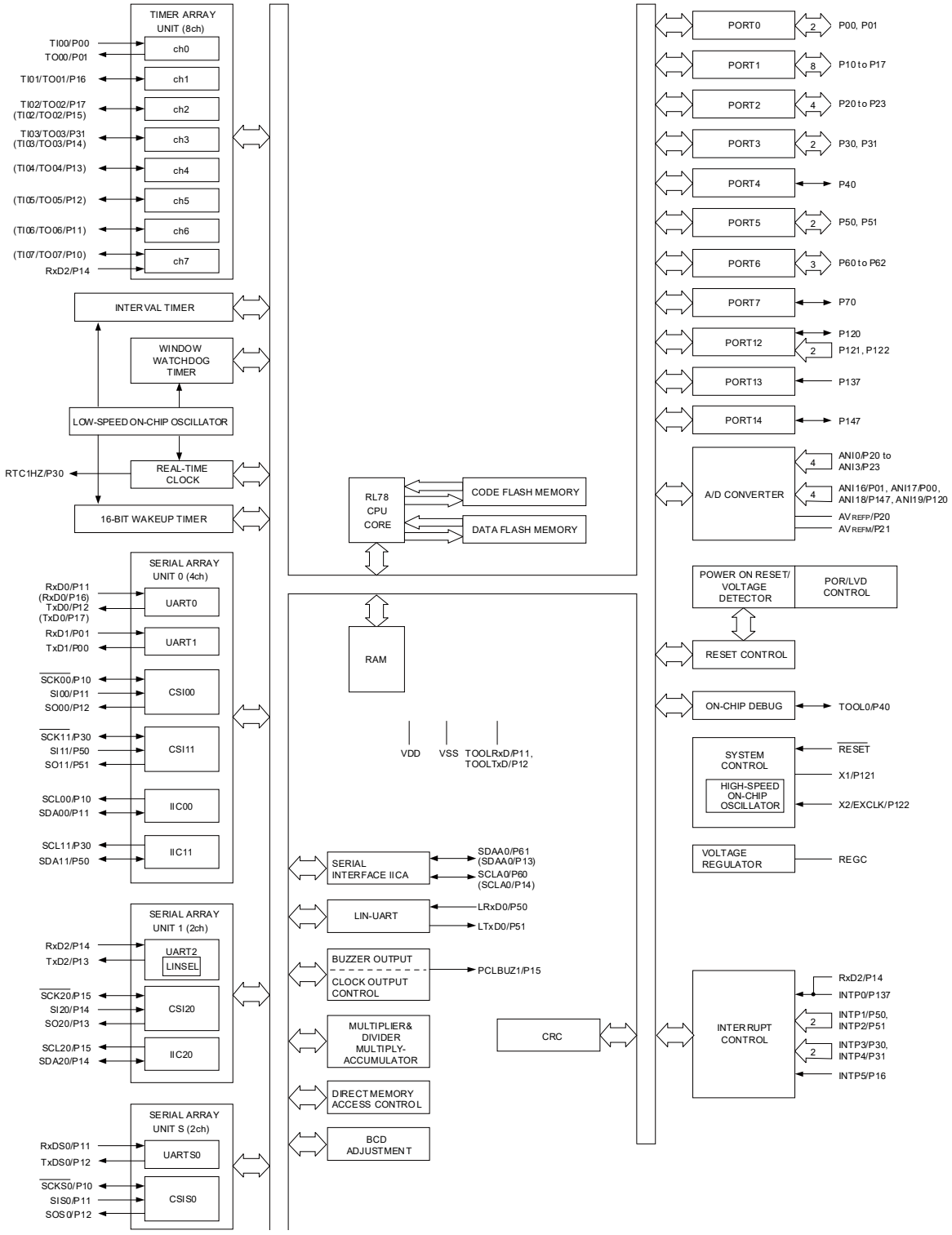
<R>



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.3 32-pin products

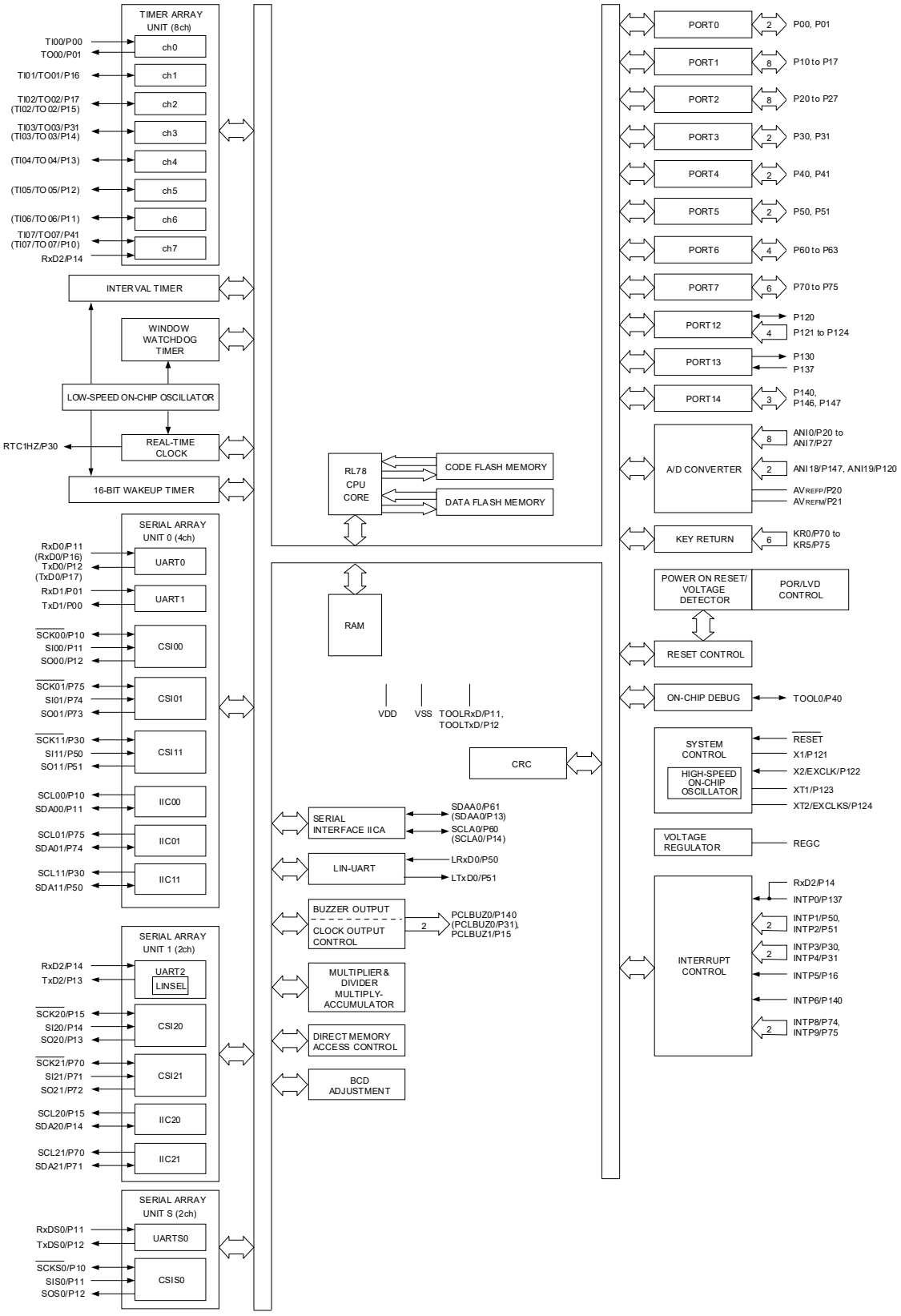
<R>



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.4 48-pin products

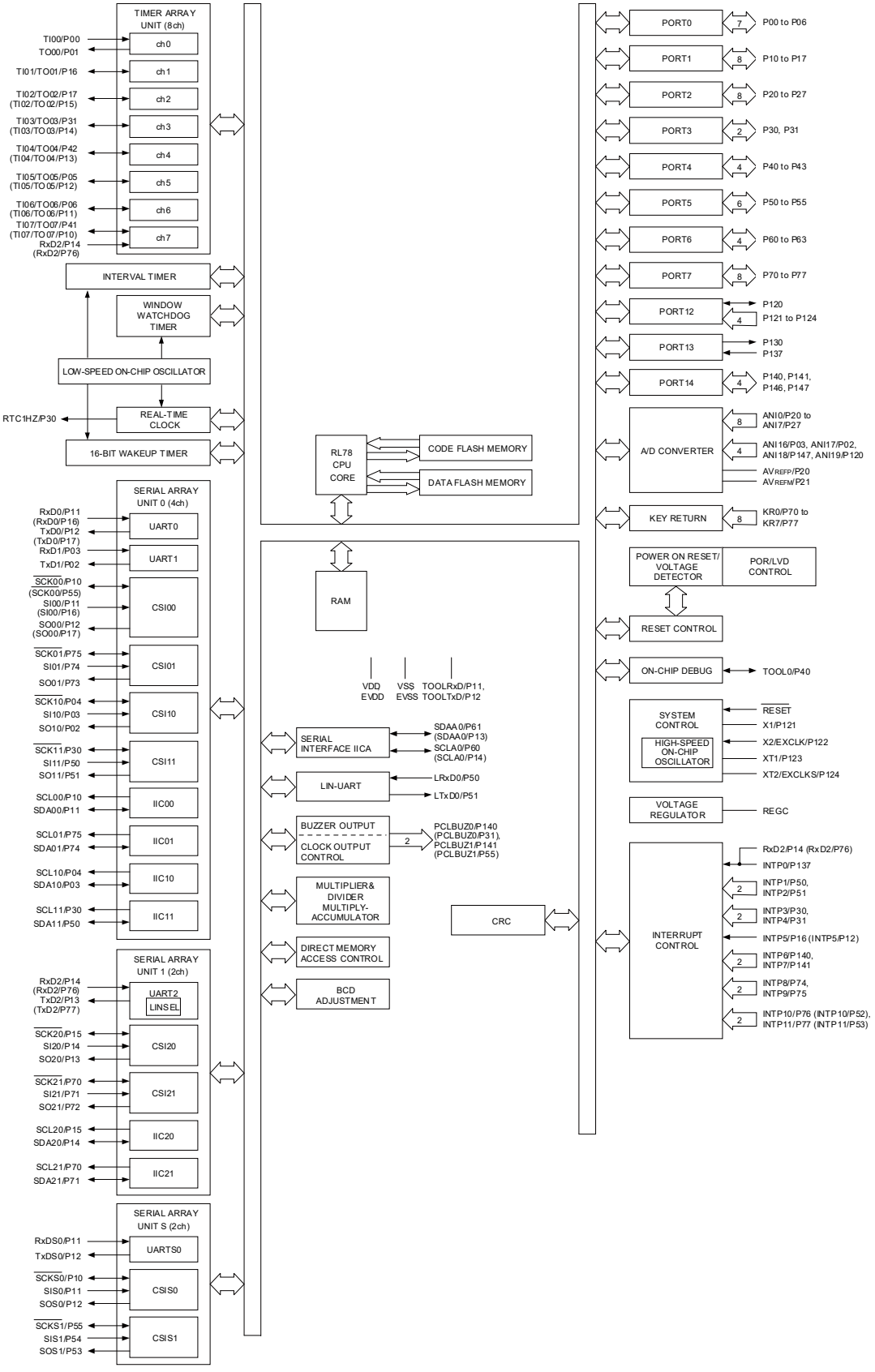
<R>



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.5 64-pin products

<R>



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin	30-pin	32-pin	48-pin	64-pin
		R5F1096x	R5F109Ax	R5F109Bx	R5F109Gx	R5F109Lx
Code flash memory (KB)		8 to 64	16 to 64	16 to 64	16 to 64	16 to 64
Data flash memory (KB)		4	4	4	4	4
RAM (KB)		0.5 to 4 Note1	1 to 4 Note1	1 to 4 Note1	1 to 4 Note1	1 to 4 Note1
Memory space		1 MB				
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V				
	High-speed on-chip oscillator clock	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V)				
Subsystem clock		–			XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 1.8 to 5.5 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.03125 μs (high-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)				
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)				
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation) Note3				
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.				
I/O port	Total	16	26	28	44	58
	CMOS I/O	13	21	22	34	48
	CMOS input	3	3	3	5	5
	CMOS output	–	–	–	1	1
	N-ch open-drain I/O (6 V tolerance)	–	2	3	4	4
Timer	16-bit timer	8 channels				
	Watchdog timer	1 channel				
	Real-time clock (RTC)	1 channel				
	Interval timer	1 channel				
	Wakeup timer	1 channel				
	Timer output	4 channels (PWM outputs: 3 Note2)			5 channels (PWM outputs: 4 Note2)	8 channels (PWM outputs: 4 Note2)
	RTC output	–			1 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	
Clock output/buzzer output		1	2	2	2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) Note3				

Notes 1. In the case of the 4 KB, this is 3 KB when the self-programming function is used.

2. The number of outputs varies, depending on the setting.

3. Available only in 48- and 64-pin products.

(2/2)

Item		20-pin	30-pin	32-pin	48-pin	64-pin
		R5F1096x	R5F109Ax	R5F109Bx	R5F109Gx	R5F109Lx
8/10-bit resolution A/D converter		4 channels (V_{DD}: 3 channels) (EV_{DD}: 1 channels)	8 channels (V_{DD}: 4 channels) (EV_{DD}: 4 channels)	8 channels (V_{DD}: 4 channels) (EV_{DD}: 4 channels)	10 channels (V_{DD}: 8 channels) (EV_{DD}: 2 channels)	12 channels (V_{DD}: 8 channels) (EV_{DD}: 4 channels)
Serial interface		[20-pin products] • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel • LIN-UART: 1 channel [30-pin, 32-pin products] • CSI: 2 channels/UART: 2 channels/simplified I^2C: 2 channels • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI (7 to 16 bits): 1 channel/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel [48-pin products] • CSI: 3 channels/UART: 2 channels/simplified I^2C: 3 channels • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI (7 to 16 bits): 1 channel/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel [64-pin products] • CSI: 4 channels/UART: 2 channels/simplified I^2C: 4 channels • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI (7 to 16 bits): 2 channels/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel				
	I^2C bus	–	1 channel			
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)				
DMA controller		2 channels				
Vectored interrupt sources	Internal	28	34	34	34 Note1	34 Note1
	External	5	6	6	10 Note1	12 Note1
Key interrupt		–			6	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note2 • Internal reset by RAM parity error • Internal reset by illegal-memory access				
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V				
Voltage detector		• Rising edge : 1.88 V to 4.06 V (12 stages) • Falling edge : 1.84 V to 3.98 V (12 stages)				
On-chip debug function		Provided				
Power supply voltage		V_{DD} = 1.8 to 5.5 V (J GRADE), V_{DD} = 2.7 to 5.5 V (K GRADE)				
Operating ambient temperature		T_A = –40 to +85 °C (J GRADE), T_A = –40 to +125 °C (K GRADE)				

Notes 1. INTP8, INTLR, INTP9, and INTLS are counted as one interrupt source in both an internal and external interrupt, respectively.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. PIN FUNCTIONS

2.1 Pin Function List

2.1.1 20-pin products

Function Name	I/O	Function	After Reset	Alternate Function
P01	I/O	Port 0. 1-bit I/O port. Input of P01 can be set to TTL input buffer. P01 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI16/TO00
P10	I/O	Port 1. 5-bit I/O port. Input of P16 and P17 can be set to TTL input buffer. Output of P10 to P12, and P17 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$/$\overline{SCKS0}$/ SCL00/(TI07)/(TO07)
P11				SI00/RxD0/ SIS0/RxDS0/ TOOLRxD/SDA00/ (TI06)/(TO06)
P12				SO00/TxD0/SOS0/ TxDS0/TOOLTxD/ (TI05)/(TO05)
P16				TI01/TO01/INTP5/ (RXD0)
P17				TI02/TO02/(TXD0)
P20	I/O	Port 2. 3-bit I/O port. Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV_{REFP}
P21				ANI1/AV_{REFM}
P22				ANI2
P31	I/O	Port 3. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI03/TO03/INTP4 PCLBUZ0
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P50	I/O	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/LRxD0
P51				INTP2/LTxD0
P121	Input	Port 12. 2-bit input port.	Input port	X1
P122				X2/EXCLK
P137	Input	Port 13. 1-bit input port.	Input port	INTP0

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2.1.2 30-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input of P01 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (V_{DD} tolerance). P00 and P01 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI17/TI00/TxD1
P01				ANI16/TO00/RxD1
P10	I/O	Port 1. 8-bit I/O port. Input of P13 to P17 can be set to TTL input buffer. Output of P10 to P15, and P17 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$/$\overline{SCKS0}$/ SCL00/(TI07)/(TO07)
P11				SI00/RxD0/ SIS0/RxDS0/ TOOLRxD/SDA00/ (TI06)/(TO06)
P12				SO00/TxD0/SOS0/ TxDS0/TOOLTxD/ (TI05)/(TO05)
P13				TxD2/SO20/(SDAA0)/ (TI04)/(TO04)
P14				RxD2/SI20/SDA20/ (SCLA0)/(TI03)/ (TO03)
P15				PCLBUZ1/$\overline{SCK20}$/ SCL20/(TI02)/(TO02)
P16				TI01/TO01/INTP5/ (RXD0)
P17				TI02/TO02/(TXD0)
P20	I/O	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV_{REFP}
P21				ANI1/AV_{REFM}
P22				ANI2
P23				ANI3
P30	I/O	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP3/ $\overline{SCK11}$/SCL11
P31				TI03/TO03/INTP4
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P50	I/O	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/SI11/SDA11/ LRxD0
P51				INTP2/SO11/LTxD0

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

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Function Name	I/O	Function	After Reset	Alternate Function
P60	I/O	Port 6. 2-bit I/O port. Output of P60 and P61 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCLA0
P61				SDAA0
P120	I/O	Port 12. 1-bit I/O port and 2-bit input port. P120 can be set to analog input. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI19
P121	Input		Input port	X1
P122				X2/EXCLK
P137	Input	Port 13. 1-bit input port.	Input port	INTP0
P147	I/O	Port 14. 1-bit I/O port. P147 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI18

2.1.3 32-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input of P01 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (V_{DD} tolerance) P00 and P01 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI17/TI00/TxD1
P01				ANI16/TO00/RxD1
P10	I/O	Port 1. 8-bit I/O port. Input of P13 to P17 can be set to TTL input buffer. Output of P10 to P15, and P17 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$/$\overline{SCKS0}$/ SCL00/(TI07)/(TO07)
P11				SI00/RxD0/ SIS0/RxDS0/ TOOLRxD/SDA00/ (TI06)/(TO06)
P12				SO00/TxD0/SOS0/ TxDS0/TOOLTxD/ (TI05)/(TO05)
P13				TxD2/SO20/(SDAA0)/ (TI04)/(TO04)
P14				RxD2/SI20/SDA20/ (SCLA0)/(TI03)/ (TO03)
P15				PCLBUZ1/$\overline{SCK20}$/ SCL20/(TI02)/(TO02)
P16				TI01/TO01/INTP5/ (RXD0)
P17				TI02/TO02/(TXD0)
P20	I/O	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV_{REFP}
P21				ANI1/AV_{REFM}
P22				ANI2
P23				ANI3
P30	I/O	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP3/$\overline{SCK11}$/ SCL11
P31				TI03/TO03/INTP4
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P50	I/O	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/SI11/SDA11/ LRxD0
P51				INTP2/SO11/LTxD0

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

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Function Name	I/O	Function	After Reset	Alternate Function
P60	I/O	Port 6. 3-bit I/O port. Output of P60 to P62 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCLA0
P61				SDAA0
P62				–
P70	I/O	Port 7. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P120	I/O	Port 12. 1-bit I/O port and 2-bit input port. P120 can be set to analog input. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI19
P121	Input		Input port	X1
P122				X2/EXCLK
P137	Input	Port 13. 1-bit input port.	Input port	INTP0
P147	I/O	Port 14. 1-bit I/O port. P147 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI18

2.1.4 48-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input of P01 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (V_{DD} tolerance) Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00/TxD1
P01				TO00/RxD1
P10	I/O	Port 1. 8-bit I/O port. Input of P13 to P17 can be set to TTL input buffer. Output of P10 to P15, and P17 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$/$\overline{SCKS0}$/ SCL00/(TI07)/(TO07)
P11				SI00/RxD0/ SIS0/RxDS0/ TOOLRxD/SDA00/ (TI06)/(TO06)
P12				SO00/TxD0/SOS0/ TxDS0/TOOLTxD/ (TI05)/(TO05)
P13				TxD2/SO20/(SDAA0)/ (TI04)/(TO04)
P14				RxD2/SI20/SDA20/ (SCLA0)/(TI03)/ (TO03)
P15				PCLBUZ1/$\overline{SCK20}$/ SCL20/(TI02)/ (TO02)
P16				TI01/TO01/INTP5/ (RXD0)
P17				TI02/TO02/(TXD0)
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV_{REFP}
P21				ANI1/AV_{REFM}
P22				ANI2
P23				ANI3
P24				ANI4
P25				ANI5
P26				ANI6
P27				ANI7
P30	I/O	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP3/RTC1HZ/ $\overline{SCK11}$/SCL11
P31				TI03/TO03/INTP4/ (PCLBUZ0)
P40	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TI07/TO07
				–

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

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Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/SI11/SDA11/ LRxD0
P51				INTP2/SO11/LTxD0
P60	I/O	Port 6. 4-bit I/O port. Output of P60 to P63 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCLA0
P61				SDAA0
P62				–
P63				–
P70	I/O	Port 7. 6-bit I/O port. Output of P71 and P74 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/$\overline{\text{SCK21}}$/SCL21
P71				KR1/SI21/SDA21
P72				KR2/SO21
P73				KR3/SO01
P74				KR4/INTP8/SI01/ SDA01
P75				KR5/INTP9/$\overline{\text{SCK01}}$/ SCL01
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. P120 can be set to analog input. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI19
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P130	Output	Port 13. 1-bit output port and 1-bit input port.	Output port	–
P137	Input		Input port	INTP0
P140	I/O	Port 14. 3-bit I/O port. P147 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0/INTP6
P146				–
P147			Analog input port	ANI18

2.1.5 64-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 7-bit I/O port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00, P02, P03 and P04 can be set to N-ch open-drain output (V_{DD} tolerance) Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00
P01				TO00
P02				ANI17/SO10/TXD1
P03				ANI16/SI10/RXD1/SDA10
P04				$\overline{SCK10}$/SCL10
P05				TI05/TO05
P06				TI06/TO06
P10	I/O	Port 1. 8-bit I/O port. Input of P13 to P17 can be set to TTL input buffer. Output of P10 to P15, and P17 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$/SCL00/$\overline{SCKS0}$/(TI07)/(TO07)
P11				SI00/RXD0/SDA00/TOOLRXD/SIS0/RXDS0/(TI06)/(TO06)
P12				SO00/TXD0/TOOLTXD/SOS0/TXDS0/(INTP5)/(TI05)/(TO05)
P13				TXD2/SO20/(SDAA0)/(TI04)/(TO04)
P14				RXD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
P15				$\overline{SCK20}$/SCL20/(TI02)/(TO02)
P16				TI01/TO01/INTP5/(RXD0)/(SI00)
P17				TI02/TO02/(TXD0)/(SO00)
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV_{REFP}
P21				ANI1/AV_{REFM}
P22				ANI2
P23				ANI3
P24				ANI4
P25				ANI5
P26				ANI6
P27				ANI7
P30	I/O	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP3/RTC1HZ/$\overline{SCK11}$/SCL11
P31				TI03/TO03/INTP4/(PCLBUZ0)
P40	I/O	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TI07/TO07
P42				TI04/TO04
P43				–

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

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Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 6-bit I/O port. Input of P55 can be set to TTL input buffer. Output of P50 and P55 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/SI11/SDA11/ LRXD
P51				INTP2/SO11/LTXD
P52				(INTP10)
P53				SOS1/(INTP11)
P54				SIS1
P55				$\overline{\text{SCKS1}}$/(PCLBUZ1)/ ($\overline{\text{SCK00}}$)
P60	I/O	Port 6. 4-bit I/O port. Output of P60 to P63 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCLA0
P61				SDAA0
P62				–
P63				–
P70	I/O	Port 7. 8-bit I/O port. Output of P71 and P74 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/$\overline{\text{SCK21}}$/SCL21
P71				KR1/SI21/SDA21
P72				KR2/SO21
P73				KR3/SO01
P74				KR4/INTP8/SI01/ SDA01
P75				KR5/INTP9/$\overline{\text{SCK01}}$/ SCL01
P76				KR6/INTP10/(RXD2)
P77				KR7/INTP11/(TXD2)
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. P120 can be set to analog input. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI19
P121	Input		Input port	X1
P122				X2/EXCLKS
P123				XT1
P124				XT2/EXCLKS
P130	Output	Port 13. 1-bit output port and 1-bit input port.	Output port	–
P137	Input		Input port	INTP0
P140	I/O	Port 14. 4-bit I/O port. P147 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0/INTP6
P141				PCLBUZ1/INTP7
P146				–
P147			Analog input port	ANI18

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2.1.6 Pins for each product (pins other than port pins)

(1/3)

Function Name	I/O	Function	64-pin	48-pin	32-pin	30-pin	20-pin
ANI0	Input	A/D converter analog input	√	√	√	√	√
ANI1			√	√	√	√	√
ANI2			√	√	√	√	√
ANI3			√	√	√	√	–
ANI4			√	√	–	–	–
ANI5			√	√	–	–	–
ANI6			√	√	–	–	–
ANI7			√	√	–	–	–
ANI16			√	–	√	√	√
ANI17			√	–	√	√	–
ANI18			√	√	√	√	–
ANI19			√	√	√	√	–
INTP0	Input	External interrupt request input	√	√	√	√	√
INTP1			√	√	√	√	√
INTP2			√	√	√	√	√
INTP3			√	√	√	√	–
INTP4			√	√	√	√	√
INTP5			√	√	√	√	√
INTP6			√	√	–	–	–
INTP8			√	√	–	–	–
INTP9			√	√	–	–	–
INTP10			√	–	–	–	–
INTP11			√	–	–	–	–
KR0	Input	Key interrupt input	√	√	–	–	–
KR1			√	√	–	–	–
KR2			√	√	–	–	–
KR3			√	√	–	–	–
KR4			√	√	–	–	–
KR5			√	√	–	–	–
KR6			√	–	–	–	–
KR7			√	–	–	–	–
LRxD0	Input	Serial data input to LIN-UART0	√	√	√	√	√
LTxD0	Output	Serial data output from LIN-UART0	√	√	√	√	√
PCLBUZ0	Output	Clock output/buzzer output	√	√	√	√	√
PCLBUZ1			√	√	√	√	–
REGC	–	Connecting regulator output stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	√	√	√	√	√
$\overline{\text{RESET}}$	Input	System reset input	√	√	√	√	√

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Function Name	I/O	Function	64-pin	48-pin	32-pin	30-pin	20-pin
RxD0	Input	Serial data input to UART0	√	√	√	√	√
RxD1		Serial data input to UART1	√	√	√	√	–
RxD2		Serial data input to UART2	√	√	√	√	–
RxDS0		Serial data input to UARTS0	√	√	√	√	√
$\overline{SCK00}$	I/O	Clock input/output for CSI00, CSI01, CSI10, CSI11, CSI20, CSI21,CSIS0 and CSIS1	√	√	√	√	√
$\overline{SCK01}$			√	√	–	–	–
$\overline{SCK10}$			√	–	–	–	–
$\overline{SCK11}$			√	√	√	√	–
$\overline{SCK20}$			√	√	√	√	–
$\overline{SCK21}$			√	√	–	–	–
$\overline{SCKS0}$			√	√	√	√	√
$\overline{SCKS1}$			√	–	–	–	–
SCLA0	I/O	Clock input/output for I^2C	√	√	√	√	–
SCL00	I/O	Clock input/output for simplified I^2C	√	√	√	√	√
SCL01			√	√	–	–	–
SCL10			√	–	–	–	–
SCL11			√	√	√	√	–
SCL20			√	√	√	√	–
SCL21			√	√	–	–	–
SDAA0	I/O	Serial data I/O for I^2C	√	√	√	√	–
SDA00	I/O	Serial data I/O for simplified I^2C	√	√	√	√	√
SDA01			√	√	–	–	–
SDA10			√	–	–	–	–
SDA11			√	√	√	√	–
SDA20			√	√	√	√	–
SDA21			√	√	–	–	–
SI00	Input	Serial data input to CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSIS0, and CSIS1	√	√	√	√	√
SI01			√	√	–	–	–
SI10			√	–	–	–	–
SI11			√	√	√	√	–
SI20			√	√	√	√	–
SI21			√	√	–	–	–
SIS0			√	√	√	√	√
SIS1			√	–	–	–	–
SO00	Output	Serial data output from CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSIS0, and CSIS1	√	√	√	√	√
SO01			√	√	–	–	–
SO10			√	–	–	–	–
SO11			√	√	√	√	–
SO20			√	√	√	√	–
SO21			√	√	–	–	–
SOS0			√	√	√	√	√
SOS1			√	–	–	–	–

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Function Name	I/O	Function	64-pin	48-pin	32-pin	30-pin	20-pin
TI00	Input	External count clock input to 16-bit timer 00	√	√	√	√	–
TI01		External count clock input to 16-bit timer 01	√	√	√	√	√
TI02		External count clock input to 16-bit timer 02	√	√	√	√	√
TI03		External count clock input to 16-bit timer 03	√	√	√	√	√
TI04		External count clock input to 16-bit timer 04	√	(√)	(√)	(√)	–
TI05		External count clock input to 16-bit timer 05	√	(√)	(√)	(√)	(√)
TI06		External count clock input to 16-bit timer 06	√	(√)	(√)	(√)	(√)
TI07		External count clock input to 16-bit timer 07	√	√	(√)	(√)	(√)
TO00	Output	16-bit timer 00 output	√	√	√	√	√
TO01		16-bit timer 01 output	√	√	√	√	√
TO02		16-bit timer 02 output	√	√	√	√	√
TO03		16-bit timer 03 output	√	√	√	√	√
TO04		16-bit timer 04 output	√	(√)	(√)	(√)	–
TO05		16-bit timer 05 output	√	(√)	(√)	(√)	(√)
TO06		16-bit timer 06 output	√	(√)	(√)	(√)	(√)
TO07		16-bit timer 07 output	√	√	(√)	(√)	(√)
TxD0	Output	Serial data output from UART0	√	√	√	√	√
TxD1		Serial data output from UART1	√	√	√	√	–
TxD2		Serial data output from UART2	√	√	√	√	–
TxDS0		Serial data output from UARTS0	√	√	√	√	√
X1	Input	Resonator connection for main system clock	√	√	√	√	√
X2	Output		√	√	√	√	√
EXCLK	Input	External clock input for main system clock	√	√	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	√	–	–	–
XT1	Input	Resonator connection for subsystem clock	√	√	–	–	–
XT2	Output		√	√	–	–	–
V_{DD}	–	Positive power supply for all pins	√	√	√	√	√
EV_{DD}	–	Positive power supply for pins other than above-mentioned V_{DD} connected pins	√	–	–	–	–
AV_{REFP}	Input	A/D converter reference potential (+ side) input	√	√	√	√	√
AV_{REFM}	Input	A/D converter reference potential (– side) input	√	√	√	√	√
V_{SS}	–	Ground potential for all pins	√	√	√	√	√
EV_{SS}	–	Ground potential for pins other than above-mentioned V_{SS} connected pins	√	–	–	–	–
TOOLRxD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√	√	√
TOOLTxD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√	√	√
TOOL0	I/O	Data I/O for flash memory programmer/debugger	√	√	√	√	√

Remark The checked function is available only when the bit corresponding to the function in the peripheral I/O redirection register (PIOR) is set to 1.

3. ELECTRICAL SPECIFICATIONS (J GRADE)

Cautions 1. RL78/F12 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. Pins mounted are as follows according to product.

3.1 Pins Mounted According to Product

3.1.1 Port functions

Refer to **2.1.1 20-pin products** to **2.1.5 64-pin products**.

3.1.2 Non-port functions

Refer to **2.1.6 Pins for each product (pins other than port pins)**.

Caution The pins mounted depend on the product.

3.2 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +6.5	V
	EV_{DD}		–0.5 to +6.5	V
	V_{SS}		–0.5 to +0.3	V
	EV_{SS}		–0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	–0.3 to +2.8 and –0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	–0.3 to EV_{DD}+0.3 and –0.3 to V_{DD}+0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	–0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, $\overline{\text{RESET}}$	–0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147	–0.3 to EV_{DD} +0.3 Note 2	V
	V_{O2}	P20 to P27	–0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AI1}	ANI0 to ANI7	–0.3 to V_{DD} +0.3 Note 2	V
	V_{AI2}	ANI16 to ANI19	–0.3 to EV_{DD} +0.3 Note 2	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	–40	mA
		Total of all pins –170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	–70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147	–100	mA
	I_{OH2}	Per pin	P20 to P27	–0.5	mA
		Total of all pins		–2	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

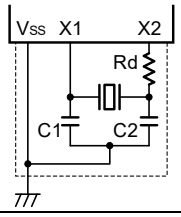
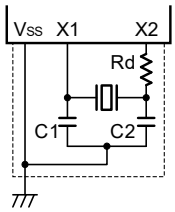
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

3.3 Oscillator Characteristics

3.3.1 Main system clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)**Note**	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	MHz
Crystal resonator		X1 clock oscillation frequency (f_X)**Note**	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	MHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Caution The pins mounted depend on the product.

3.3.2 On-chip oscillator characteristics

(T_A = –20 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	32 MHz selected	31.52	32.00	32.48	MHz
		24 MHz selected	23.64	24.00	24.36	MHz
		16 MHz selected	15.76	16.00	16.24	MHz
		8 MHz selected	7.88	8.00	8.12	MHz
		4 MHz selected	3.94	4.00	4.06	MHz
		1 MHz selected	0.985	1.00	1.015	MHz

Note This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

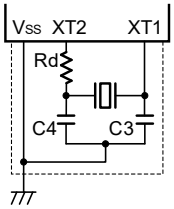
Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	32 MHz selected	31.36	32.00	32.64	MHz
		24 MHz selected	23.52	24.00	24.48	MHz
		16 MHz selected	15.68	16.00	16.32	MHz
		8 MHz selected	7.84	8.00	8.16	MHz
		4 MHz selected	3.92	4.00	4.08	MHz
		1 MHz selected	0.98	1.00	1.02	MHz
Low-speed on-chip oscillator clock frequency	f_{IL}		12.75	15	17.25	kHz

Note This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Caution The pins mounted depend on the product.

3.3.3 Subsystem clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Resonator	Recommended Circuit	Items	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})Note		29.0	32.768	35.0	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Caution The pins mounted depend on the product.

3.4 DC Characteristics

3.4.1 Pin characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V			–5.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–3.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–0.5	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–20.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–10.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–19.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–10.0	mA
		Total of all pins (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–50.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–29.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–15.0	mA
	I_{OH2}	Per pin for P20 to P27				–0.1	mA
		Total of all pins (When duty = 70% Note 2)				–0.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD} pin to an output pin.

2. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n% (the duty before change < n)).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) = –8.75 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P10 to P15, P17, P50, P71, P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ EV_{DD} < 4.0 V			4.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			0.6	mA
		Per pin for P60 to P63	4.0 V ≤ EV_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			4.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			2.0	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			50.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P27				0.4	mA
		Total of all pins (When duty = 70% Note 2)				3.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS} and V_{SS} pin.

2. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n% (the duty before change < n)).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) = 8.75 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 1)	0.8 EV_{DD}		EV_{DD}	V
	V_{IH2}	P01, P03, P04, P13 to P17, P55	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL input buffer 2.7 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL input buffer 1.8 V ≤ EV_{DD} < 2.7 V	0		0.3EV_{DD}	V
	V_{IH3}	P20 to P27		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 EV_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH6}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 0)	0.8 EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 1)	0		0.2 EV_{DD}	V
	V_{IL2}	P01, P03, P04, P13 to P17, P55	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 2.7 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.8 V ≤ EV_{DD} < 2.7 V	0		0.3EV_{DD}	V
	V_{IL3}	P20 to P27		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 EV_{DD}	V
	V_{IL5}	P121 to P124, P137, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL6}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 0) 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.5 EV_{DD}	V
			Normal input buffer (ITHL = 0) 2.7 V ≤ EV_{DD} < 4.0 V	0		0.4 EV_{DD}	V
			Normal input buffer 1.8 V ≤ EV_{DD} < 2.7 V	0		0.3 EV_{DD}	V

Cautions The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P50, P55, P71, P74 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins. The input pins of alternate-functions: CSIS0, CSIS1, UARTS, and UARTF, do not support TTL inputs.

Caution The pins mounted depend on the product.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V	I_{OH1} = –5.0 mA	EV_{DD} – 0.9			V
				I_{OH1} = –3.0 mA	EV_{DD} – 0.7			
				I_{OH1} = –1.0 mA	EV_{DD} – 0.5			
			2.7 V ≤ EV_{DD} ≤ 5.5 V	I_{OH1} = –3.0 mA	EV_{DD} – 0.7			V
				I_{OH1} = –1.0 mA	EV_{DD} – 0.5			
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –0.5 mA		EV_{DD} – 0.5			V
	V_{OH2}	P20 to P27	1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –0.1 mA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA				0.7	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 4.0 mA				0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 4.0 mA				0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA				0.4	V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA				0.4	V
	V_{OL2}	P20 to P27	1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA				2.0	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA				0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V	I_{OL3} = 4.0 mA			0.5	V
				I_{OL3} = 3.0 mA			0.4	
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA				0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P43, P50, P52 to P55, P71, P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, P146, P147	$V_I = EV_{DD}$				1	μA
	I_{LIH2}	P20 to P27, P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, P146, P147	$V_I = EV_{SS}$				–1	μA
	I_{LIL2}	P20 to P27, P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
On-chip pll-up resistance	R_U	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147			10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

3.4.2 Supply current characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	High-speed operation Note 5	f_{IH} = 32 MHz Note 2		5.6	8.2	mA
				f_{IH} = 24 MHz Note 2		4.5	6.5	mA
				f_{IH} = 16 MHz Note 2		3.3	4.8	mA
				f_{MX} = 20 MHz Note 3		4.0	5.5	mA
				f_{MX} = 10 MHz Note 3		2.4	3.1	mA
			Low-speed operation Note 5	f_{IH} = 8 MHz Note 2		1.6	2.3	mA
				f_{MX} = 8 MHz Note 3		1.5	2.3	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4		4.9	13.0	μA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values in the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors (when high-speed on-chip oscillator or subsystem clock, not including the current flowing into the BGO too).

2. When high-speed system clock and subsystem clock are stopped.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
High speed operation: V_{DD} = 2.7 to 5.5 V@1 MHz to 32 MHz
Low speed operation: V_{DD} = 1.8 to 5.5 V@1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	High-speed operation Note 7	f_{IH} = 32 MHz Note 3			0.55	3.2	mA
				f_{IH} = 24 MHz Note 3			0.48	2.42	
				f_{IH} = 16 MHz Note 3			0.40	1.75	
				f_{MX} = 20 MHz Note 4			0.43	1.80	
				f_{MX} = 10 MHz Note 4			0.28	0.97	
			Low-speed operation Note 7	f_{IH} = 8 MHz Note 3			0.30	0.84	mA
				f_{MX} = 8 MHz Note 4			0.18	0.60	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5	T_A ≤+50°C		0.52	2.15	μA
					T_A ≤+70°C			3.05	
					T_A ≤+85°C			4.24	
	I_{DD3} Note 6	STOP mode	T_A ≤+50°C				0.22	2.05	μA
			T_A ≤+70°C					2.95	
			T_A ≤+85°C					4.16	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values in the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and subsystem clock are stopped.

5. When operating real-time clock (RTC) and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped.

6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
High speed operation: V_{DD} = 2.7 to 5.5 V@1 MHz to 32 MHz
Low speed operation: V_{DD} = 1.8 to 5.5 V@1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	Real-time clock operation		0.02	0.13	μA
			Interval timer operation		0.02	0.33	μA
WUTM operating current	I_{WUTM}	f_{IL} = 15 kHz			0.25	0.4	μA
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 15 kHz			0.22	0.4	μA
A/D converter operating current	I_{ADC} Note 4	at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.30	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
		Internal reference voltage selected Note 7			75		μA
LVD operating current	I_{LVI} Note 5				0.08	0.20	μA
Temperature sensor operating current	I_{TMPS}				75		μA
BGO operating current	I_{BGO} Note 6				2.50	12.20	mA

Notes 1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the RL78/F12 is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time clock operating current. When the real-time clock operates during f_{CLK} = f_{SUB}, the TYP. value of I_{DD2} includes the real-time clock operating current.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 15 kHz on-chip oscillator). The current value of the RL78/F12 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode.

4. Current flowing only to the A/D converter. The current value of the RL78/F12 is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the LVD circuit. The current value of the RL78/F12 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

6. Current flowing only to the BGO. The current value of the RL78/F12 is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode or the HALT mode.

7. This indicates operating current which increases when the internal reference voltage is selected. The Current flows even if the conversion is stopped.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product.

3.5 AC Characteristics

3.5.1 Basic operation

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	High-speed main mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
			Low-speed main mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		Subsystem clock (f_{SUB}) operation SDIV=0			28.5	30.5	31.3	μs
External main system clock frequency	f_{EX}	EXCLK	2.7 V ≤ V_{DD} ≤ 5.5 V		1		20	MHz
			1.8 V ≤ V_{DD} < 2.7 V		1		8	MHz
	f_{EXS}	EXCLKS			29		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	EXCLK	2.7 V ≤ V_{DD} ≤ 5.5 V		24			ns
			1.8 V ≤ V_{DD} < 2.7 V		60			ns
	t_{EXHS}, t_{EXLS}	EXCLKS			13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				2/f_{MCK} +10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ EV_{DD} ≤ 5.5 V					16	MHz
		2.7 V ≤ EV_{DD} < 4.0 V					8	MHz
		1.8 V ≤ EV_{DD} < 2.7 V					4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	4.0 V ≤ EV_{DD} ≤ 5.5 V					16	MHz
		2.7 V ≤ EV_{DD} < 4.0 V					8	MHz
		1.8 V ≤ EV_{DD} < 2.7 V					4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP11			1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR7			250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock set by the CKS0n bit of Timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Caution The pins mounted depend on the product.

3.6 Peripheral Functions Characteristics

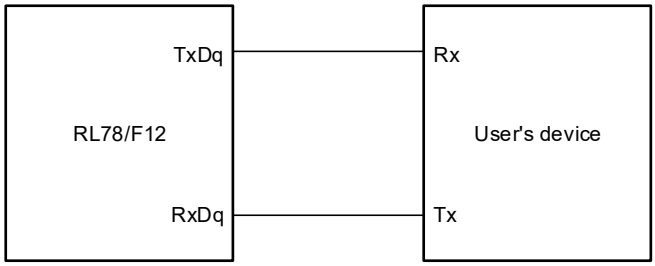
3.6.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

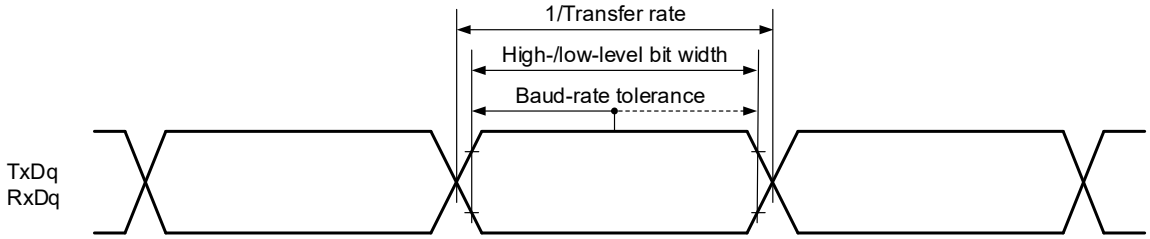
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		Other than SNOOZE mode	f_{MCK}/256		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate			5.3	Mbps
		Receivable baud rate at SNOOZE mode	4800		4800	bps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remarks 1. q: UART number (q = 0 to 2, S0), g: PIM number (g = 0, 1, 5), h: POM number (h = 0, 1, 5, 7)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11, S0, S1))

Caution The pins mounted depend on the product.

(2) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$: internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.		TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time Note 1	t_{KCY1}	CSI00	2.7 V ≤ EV_{DD} ≤ 5.5 V	125	Besides $2/f_{MCK}$ ≤			ns
			1.8 V ≤ EV_{DD} ≤ 2.7 V	500				ns
		Other than CSI00	2.7 V ≤ EV_{DD} ≤ 5.5 V	125	Besides $4/f_{MCK}$ ≤			ns
			1.8 V ≤ EV_{DD} ≤ 2.7 V	500				ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 12$				ns
		2.7 V ≤ EV_{DD} ≤ 4.0 V		$t_{KCY1}/2 - 18$				ns
		1.8 V ≤ EV_{DD} ≤ 2.7 V		$t_{KCY1}/2 - 50$				ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		44				ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		110				ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI1}			19				ns
SOp output delay time (from $\overline{SCKp}$↓) Note 3	t_{KSO1}	C = 30 pF Note 4					25	ns

Notes 1. The value must also be $2/f_{CLK}$ (CS100) or $4/f_{CLK}$ (other than CS100).

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21, S0, S1), m: Unit number (m = 0, 1, S),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 5), h: POM number (h = 0, 1, 5, 7)

Caution The pins mounted depend on the product.

(3) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$: external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ EV_{DD} < 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}			ns
		1.8 V ≤ EV_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑) **Note 1**	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+20			ns
		1.8 V ≤ EV_{DD} < 2.7 V		1/f_{MCK}+30			
SIp hold time (from $\overline{SCKp}$↑) **Note 1**	t_{KSI2}	1.8 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+31			ns
SOp output delay time (from $\overline{SCKp}$↓) **Note 2**	t_{KSO2}	C = 30 pF **Note 3**	2.7 V ≤ EV_{DD} ≤ 5.5 V			2/f_{MCK}+44	ns
			1.8 V ≤ EV_{DD} < 2.7 V			2/f_{MCK}+110	ns

Notes 1. This applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time is "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. This applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output is "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SOp output lines.

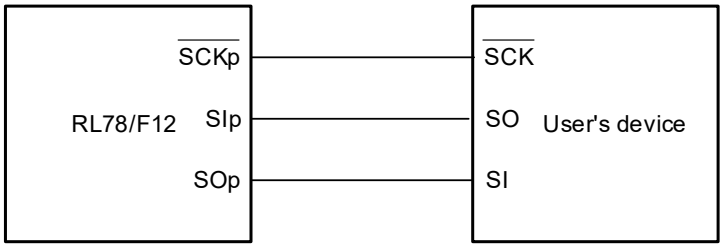
Caution Select the TTL input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, S0 ,S1), m: Unit number (m = 0, 1, S), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 5), h: POM number (h = 0, 1, 5, 7)

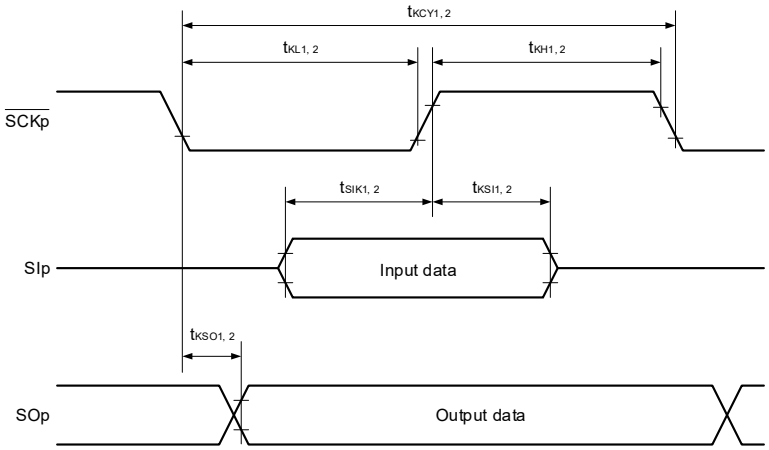
2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11, S0, S1))

Caution The pins mounted depend on the product.

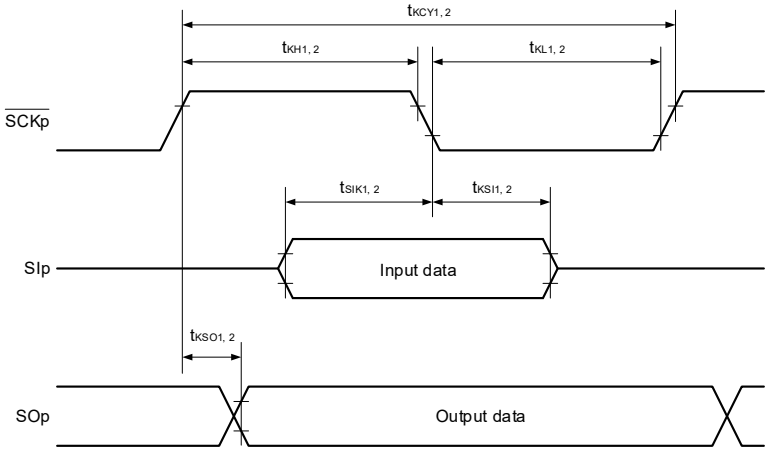
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, S0, S1)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11, S0, S1)

Caution The pins mounted depend on the product.

(4) During communication at same potential (simplified I^2C mode)

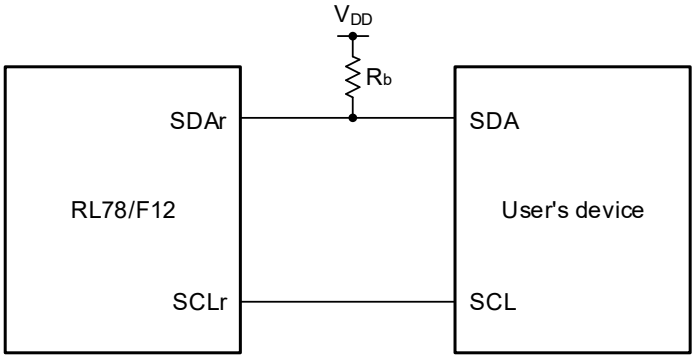
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400	kHz
Hold time when SCLr = “L”	t_{LOW}	1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = “H”	t_{HIGH}	1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 **Note**		ns
Data hold time (transmission)	$t_{HD:DAT}$	1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns

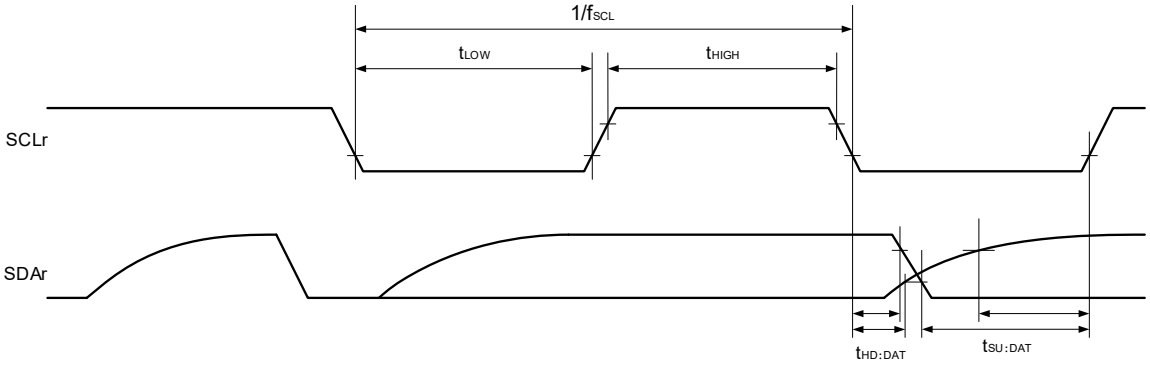
Note The value of f_{MCK} must be such that this does not exceed the hold time for SCLr = L or the hold time for SCLr = H.

Caution The pins mounted depend on the product.

Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remarks 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 5), h: POM number (h = 0, 1, 5, 7)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1, 2), n: Channel number (n = 0, 1), mn = 00, 01, 10, 11, 20, 21)

Caution The pins mounted depend on the product.

3.6.2 Serial interface IICA

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		Standard Mode		Fast Mode		Fast Mode Plus		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V					0	1000	kHz
		Fast mode: f_{CLK} ≥ 3.5 MHz	1.8 V ≤ EV_{DD} ≤ 5.5 V			0	400			kHz
		Normal mode: f_{CLK} ≥ 1 MHz	1.8 V ≤ EV_{DD} ≤ 5.5 V	0	100					kHz
Setup time of restart condition Note 1	$t_{SU:STA}$			4.7		0.6		0.26		μs
Hold time	$t_{HD:STA}$			4.0		0.6		0.26		μs
Hold time when SCLA0 = “L”	t_{LOW}			4.7		1.3		0.5		μs
Hold time when SCLA0 = “H”	t_{HIGH}			4.0		0.6		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$			250		100		50		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$			0	3.45	0	0.9	0		μs
Setup time of stop condition	$t_{SU:STO}$			4.0		0.6		0.26		μs
Bus-free time	t_{BUF}			4.7		1.3		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

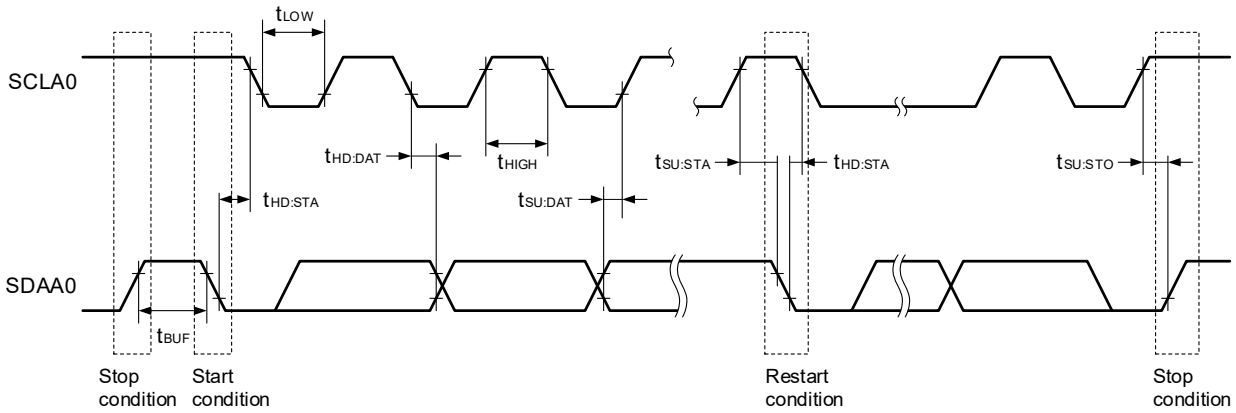
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

Caution The pins mounted depend on the product.

IICA serial transfer timing



3.6.3 LIN-UART

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	1/T			1 Note	Mbps

Note However, the upper limit is f_{CLK}/8.

Caution The pins mounted depend on the product.

3.7 Analog Characteristics

3.7.1 A/D converter characteristics

(1) When the setting of AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1) and AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), this applies to the following ANI pins: ANI2 to ANI7 (the ANI pins for which V_{DD} is the power-supply voltage).

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±3.0	LSB
			1.8 V ≤ V_{DD} < 4.0 V		±1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
Reference voltage (+)	AV_{REFP}			1.8		V_{DD}	V
Reference voltage (-)	AV_{REFM}			0			
Analog input voltage	V_{AIN}			AV_{REFM}		AV_{REFP}	V
	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

(2) When the setting of AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1) and AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), this applies to the following ANI pins: ANI16 to ANI19 (the ANI pins for which EV_{DD} is the power-supply voltage).

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} AV_{REFM} = V_{SS}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±4.5	LSB
			1.8 V ≤ V_{DD} < 4.0 V		±1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Reference voltage (+)	AV_{REFP}			1.8		V_{DD}	V
Reference voltage (-)	AV_{REFM}			0			V
Analog input voltage	V_{AIN}			AV_{REFM}		AV_{REFP}	V
	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

(3) When the setting of AVREF (+) = VDD (ADREFP1 = 0, ADREFP0 = 0) and AVREF (-) = VSS (ADREFM = 0), this applies to the following ANI pins: ANI0 to ANI7.

(TA = –40 to +85°C, 1.8 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V, reference voltage (+) = VDD, reference voltage (-) = VSS)

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Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Resolution	RES				8		10	bit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ VDD ≤ 5.5 V	ANI0-ANI7		±1.2	±5.0	LSB
			1.8 V ≤ VDD < 4.0 V	ANI0-ANI7		±1.2	±5.5	LSB
Conversion time	tCONV	10-bit resolution	4.0 V ≤ VDD ≤ 5.5 V		2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V		3.1875		39	μs
			1.8 V ≤ VDD ≤ 5.5 V		17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	1.8 V ≤ VDD ≤ 5.5 V				±0.50	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	1.8 V ≤ VDD ≤ 5.5 V				±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ VDD ≤ 5.5 V				±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ VDD ≤ 5.5 V				±2.0	LSB
Reference voltage (+)	AVREFP				VDD			V
Reference voltage (-)	AVREFM				VSS			V
Analog input voltage	VAIN	ANI0-ANI7			VSS		VDD	V
	VBGR	2.7 V ≤ VDD ≤ 5.5 V			1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

(4) When the setting of AV_{REF} (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0) and AV_{REF} (-) = V_{SS} (ADREFM = 0), this applies to the following ANI pins: ANI16 to ANI19.

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, reference voltage (+) = V_{DD}, reference voltage (-) = V_{SS})

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Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		10	Bit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	ANI16-ANI19		±1.2	±6.5	LSB
			1.8 V ≤ V_{DD} < 4.0 V	ANI16-ANI19		±1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V		2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V		3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V		17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V				±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V				±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V				±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V				±2.0	LSB
Reference voltage (+)	AV_{REFP}				V_{DD}			V
Reference voltage (-)	AV_{REFM}				V_{SS}			V
Analog input voltage	V_{AIN}	ANI16-ANI19			V_{SS}		V_{DD}	V
	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

Caution The pins mounted depend on the product.

3.7.2 Temperature sensor characteristics

(T_A = −40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		−3.6		mV/C
Operation stabilization wait time	t_{AMP}				5	μs

3.7.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.46	1.51	1.59	V
	V_{PDR}	Power supply fall time	1.45	1.50	1.58	V
Minimum pulse width	T_{PW}		300			μs
Detection delay time	T_{PD}				350	μs

Caution The pins mounted depend on the product.

3.7.4 LVD circuit characteristics

(a) Characteristics for LVD Detection at Reset and Interrupt modes

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}	Power supply rise time	3.96	4.06	4.25	V
			Power supply fall time	3.89	3.98	4.15	V
		V_{LVI1}	Power supply rise time	3.66	3.75	3.93	V
			Power supply fall time	3.58	3.67	3.83	V
		V_{LVI2}	Power supply rise time	3.06	3.13	3.28	V
			Power supply fall time	2.99	3.06	3.20	V
		V_{LVI3}	Power supply rise time	2.95	3.02	3.17	V
			Power supply fall time	2.89	2.96	3.09	V
		V_{LVI4}	Power supply rise time	2.85	2.92	3.07	V
			Power supply fall time	2.79	2.86	2.99	V
		V_{LVI5}	Power supply rise time	2.74	2.81	2.95	V
			Power supply fall time	2.68	2.75	2.88	V
		V_{LVI6}	Power supply rise time	2.64	2.71	2.85	V
			Power supply fall time	2.59	2.65	2.77	V
		V_{LVI7}	Power supply rise time	2.55	2.61	2.74	V
			Power supply fall time	2.49	2.55	2.67	V
		V_{LVI8}	Power supply rise time	2.44	2.50	2.63	V
			Power supply fall time	2.39	2.45	2.57	V
		V_{LVI9}	Power supply rise time	2.04	2.09	2.21	V
			Power supply fall time	1.99	2.04	2.14	V
		V_{LVI10}	Power supply rise time	1.93	1.98	2.09	V
			Power supply fall time	1.89	1.94	2.04	V
		V_{LVI11}	Power supply rise time	1.83	1.88	1.99	V
			Power supply fall time	1.79[Note]	1.84	1.94	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

Note The minimum value lowers the minimum guaranteed voltage for operation (1.8 V). However, LVD detection performs in the same way as in normal mode (operation according to the same specification when V_{DD} is 1.8 V) until it is reset at reset mode.

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 11
The following relationship is formed under the same temperature conditions: the detection voltage at power supply rise time > the detection voltage at power supply fall time.

Caution The pins mounted depend on the product.

(b) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVI11}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage: 1.8 V			1.79[Note]	1.84	1.94	V
	V_{LVI10}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.93	1.98	2.09	V
				Falling interrupt voltage	1.89	1.94	2.04	V
	V_{LVI9}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.04	2.09	2.21	V
				Falling interrupt voltage	1.99	2.04	2.14	V
	V_{LVI2}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.06	3.13	3.28	V
				Falling interrupt voltage	2.99	3.06	3.20	V
	V_{LVI8}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage: 2.4 V			2.39	2.45	2.57	V
	V_{LVI7}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.55	2.61	2.74	V
				Falling interrupt voltage	2.49	2.55	2.67	V
	V_{LVI6}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.64	2.71	2.85	V
				Falling interrupt voltage	2.59	2.65	2.77	V
	V_{LVI1}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.66	3.75	3.93	V
				Falling interrupt voltage	3.58	3.67	3.83	V
	V_{LVI5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage: 2.7 V			2.68	2.75	2.88	V
	V_{LVI4}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.85	2.92	3.07	V
				Falling interrupt voltage	2.79	2.86	2.99	V
	V_{LVI3}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.17	V
				Falling interrupt voltage	2.89	2.96	3.09	V
	V_{LVI0}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.96	4.06	4.25	V
				Falling interrupt voltage	3.89	3.98	4.15	V

Note The minimum value lowers the minimum guaranteed voltage for operation (1.8 V). However, LVD detection performs in the same way as in normal mode (operation according to the same specification when V_{DD} is 1.8 V) until it is reset at reset mode.

Remark The following relationship is formed under the same temperature conditions: the rising release reset voltage > the falling interrupt voltage > the falling reset voltage

Caution The pins mounted depend on the product.

3.7.5 Power supply rise time

(T_A = –40 to +85°C, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum slew rate for the supply voltage to rise	S_{vrmax}	0 V → V_{DD} (MIN.) Note 2 (VPOC2 = 0 or 1)			50 Note 1	V/ms
Minimum slew rate for the supply voltage to rise Note 3	S_{vrmin}	0V → 1.8 V (CMODE0 = 0)	3.5 Note 1			V/ms
		0V → 2.7 V (CMODE0 = 1)	6.5 Note 1			V/ms

Notes 1. In case the supply voltage falls to a level of V_{PDR} or below and a power-on reset is generated, the slew rate must not exceed the value S_{vrmax} even if the supply voltage does not go down to 0 V.

2. V_{DD} (MIN.) varies depending on the setting of the flash operation mode in the option byte (CMODE0 bit).
LS (low speed main) mode (CMODE0 = 0): V_{DD} (MIN.) = 1.8 V
HS (high speed main) mode (CMODE0 = 1): V_{DD} (MIN.) = 2.7 V

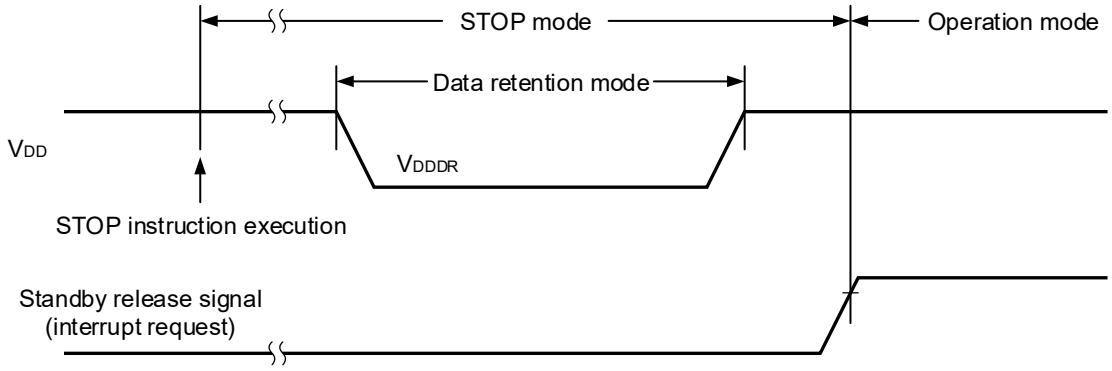
3. The minimum slew rate for the supply voltage (S_{vrmin}) must be met when the voltage detector (LVD) is not used (option byte bit VPOC2 = 1) and an external reset circuit releases before the supply voltage reaches V_{DD} (MIN.) (as specified in Note 2).

3.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.45 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



3.9 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency		f_{CLK}		1		32	MHz
Number of code flash rewrites Notes 1, 2, 3		C_{erwr}	20 years retention (after rewrite) T_A = +85°C	1000			Times
Number of data flash rewrites Notes 1, 2, 3			20 years retention (after rewrite) T_A = +85°C	10000			
			5 years retention (after rewrite) T_A = +85°C	100000			
Erase time	Block erase	T_{erasa}		5			ms
write time		T_{wrwa}		10			μs

Notes 1. Retention years indicate a period between time for a rewrite and the next.
2. When using flash memory programmer and Renesas Electronics self programming library.
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas.

4. ELECTRICAL SPECIFICATIONS (K GRADE)

Cautions 1. RL78/F12 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. Pins mounted are as follows according to product.

4.1 Pins Mounted According to Product

4.1.1 Port functions

Refer to **2.1.1 20-pin products** to **2.1.5 64-pin products**.

4.1.2 Non-port functions

Refer to **2.1.6 Pins for each product (pins other than port pins)**.

Caution The pins mounted depend on the product.

4.2 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +6.5	V
	EV_{DD}		–0.5 to +6.5	V
	V_{SS}		–0.5 to +0.3	V
	EV_{SS}		–0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	–0.3 to +2.8 and –0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	–0.3 to EV_{DD}+0.3 and –0.3 to V_{DD}+0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	–0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, $\overline{\text{RESET}}$	–0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147	–0.3 to EV_{DD} +0.3 Note 2	V
	V_{O2}	P20 to P27	–0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AI1}	ANI16 to ANI19	–0.3 to EV_{DD} +0.3 Note 2	V
	V_{AI2}	ANI0 to ANI7	–0.3 to V_{DD} +0.3 Note 2	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	–40	mA
		Total of all pins –170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	–70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147	–100	mA
	I_{OH2}	Per pin	P20 to P27	–0.5	mA
		Total of all pins		–2	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +125	°C
		In flash memory programming mode	Data	–40 to +125	
			Code	–40 to +105	
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

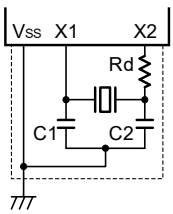
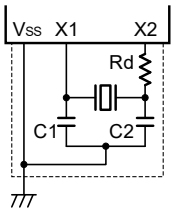
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

4.3 Oscillator Characteristics

4.3.1 Main system clock oscillator characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
Crystal resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Caution The pins mounted depend on the product.

4.3.2 On-chip oscillator characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

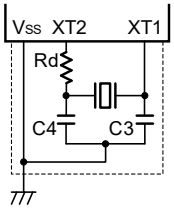
Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	24 MHz selected	23.52	24.00	24.48	MHz
		16 MHz selected	15.68	16.00	16.32	MHz
		8 MHz selected	7.84	8.00	8.16	MHz
		4 MHz selected	3.92	4.00	4.08	MHz
		1 MHz selected	0.98	1.00	1.02	MHz
Low-speed on-chip oscillator clock frequency	f_{IL}		12.75	15	17.25	kHz

Note This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Caution The pins mounted depend on the product.

4.3.3 Subsystem clock oscillator characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Resonator	Recommended Circuit	Items	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})Note		29.0	32.768	35.0	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Caution The pins mounted depend on the product.

4.4 DC Characteristics

4.4.1 Pin characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V			–5.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–3.0	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–20.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–10.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–19.0	mA
		Total of all pins (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–42.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–29.0	mA
	I_{OH2}	Per pin for P20 to P27				–0.1	mA
		Total of all pins (When duty = 70% Note 2)				–0.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD} pin to an output pin.

2. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n% (the duty before change < n)).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) = –8.75 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P10 to P15, P17, P50, P71, P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ EV_{DD} < 4.0 V			4.0	mA
		Per pin for P60 to P63	4.0 V ≤ EV_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			4.0	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
		Total of all pins (When duty = 70% Note 2)	4.0 V ≤ EV_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			50.0	mA
	I_{OL2}	Per pin for P20 to P27				0.4	mA
		Total of all pins (When duty = 70% Note 2)				3.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS} and V_{SS} pin.

2. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n% (the duty before change < n)).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) = 8.75 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 1)	0.8 EV_{DD}		EV_{DD}	V
	V_{IH2}	P01, P03, P04, P13 to P17, P55	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
	V_{IH3}	P20 to P27		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 EV_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH6}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 0)	0.8 EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 1)	0		0.2 EV_{DD}	V
	V_{IL2}	P01, P03, P04, P13 to P17, P55	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
	V_{IL3}	P20 to P27		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 EV_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL6}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer (ITHL = 0) 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.5 EV_{DD}	V
			Normal input buffer (ITHL = 0) 2.7 V ≤ EV_{DD} < 4.0 V	0		0.4 EV_{DD}	V

Cautions The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P50, P55, P71, P74 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins. The input pins of alternate-functions: CSIS0, CSIS1, UARTS, and UARTF, do not support TTL inputs.

Caution The pins mounted depend on the product.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –5.0 mA	EV_{DD} – 0.9			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	EV_{DD} – 0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –1.0 mA	EV_{DD} – 0.5			V
	V_{OH2}	P20 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	EV_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P20 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} =4.0 mA			0.5	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P50, P55, P71, P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, P146, P147	$V_I = EV_{DD}$				1	μA
	I_{LIH2}	P20 to P27, P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, P146, P147	$V_I = EV_{SS}$				–1	μA
	I_{LIL2}	P20 to P27, P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
On-chip pll-up resistance	R_U	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147			10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product.

4.4.2 Supply current characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	High-speed operation Note 5	f_{IH} = 24 MHz Note 2			4.5	6.9	mA
				f_{IH} = 16 MHz Note 2			3.3	5.2	mA
				f_{MX} = 20 MHz Note 3			4.0	5.9	mA
				f_{MX} = 10 MHz Note 3			2.4	3.5	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4	T_A ≤ + 85°C		4.9	13.0	μA
					T_A ≤ + 105°C			25.0	
					T_A ≤ + 125°C			59.0	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values in the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors (when high-speed on-chip oscillator or subsystem clock, not including the current flowing into the BGO too).

2. When high-speed system clock and subsystem clock are stopped.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
High speed operation: V_{DD} = 2.7 to 5.5 V@1 MHz to 24 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	High-speed operation Note 7	f_{IH} = 24 MHz Note 3		0.48	5.58	mA
				f_{IH} = 16 MHz Note 3		0.40	3.90	mA
				f_{MX} = 20 MHz Note 4		0.43	1.88	mA
				f_{MX} = 10 MHz Note 4		0.28	1.02	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A ≤ + 50°C		0.52	2.15	μA
				T_A ≤ + 70°C			3.05	
				T_A ≤ + 85°C			4.24	
				T_A ≤ + 105°C			15.0	
				T_A ≤ + 125°C			35.0	
	I_{DD3} Note 6	STOP mode	T_A ≤ + 50°C			0.22	2.05	μA
			T_A ≤ + 70°C				3.05	
			T_A ≤ + 85°C				4.24	
			T_A ≤ +105°C				15.0	
			T_A ≤ + 125°C				35.0	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values in the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and subsystem clock are stopped.

5. When operating real-time clock (RTC) and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped.

6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
High speed operation: V_{DD} = 2.7 to 5.5 V@1 MHz to 24 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	Real-time clock operation		0.02	0.17	μA
			Interval timer operation		0.02	0.37	μA
WUTM operating current	I_{WUTM}	f_{IL} = 15 kHz			0.25	0.6	μA
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 15 kHz			0.22	0.6	μA
A/D converter operating current	I_{ADC} Note 4	at maximum conversion speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
		Internal reference voltage selected Note 7			75		μA
LVD operating current	I_{LVI} Note 5				0.08	0.26	μA
Temperature sensor operating current	I_{TMPS}				75		μA
BGO operating current	I_{BGO} Note 6				2.5	12.2	mA

Notes 1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the RL78/F12 is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time clock operating current. When the real-time clock operates during f_{CLK} = f_{SUB}, the TYP. value of I_{DD2} includes the real-time clock operating current.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 15 kHz on-chip oscillator). The current value of the RL78/F12 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode.

4. Current flowing only to the A/D converter. The current value of the RL78/F12 is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the LVD circuit. The current value of the RL78/F12 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

6. Current flowing only to the BGO. The current value of the RL78/F12 is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode or the HALT mode.

7. This indicates operating current which increases when the internal reference voltage is selected. The Current flows even if the conversion is stopped.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product.

4.5 AC Characteristics

4.5.1 Basic operation

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation High-speed main mode	0.04		1	μs
		Subsystem clock (f_{SUB}) operation	28.5	30.5	34.5	μs
External main system clock frequency	f_{EX}		1		20	MHz
	f_{EXS}		29		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}		24			ns
	t_{EXHS}, t_{EXLS}		13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}		2/f_{MCK} +10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
		2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
		2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP11	1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR7	250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock set by the CKS0n bit of Timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Caution The pins mounted depend on the product.

4.6 Peripheral Functions Characteristics

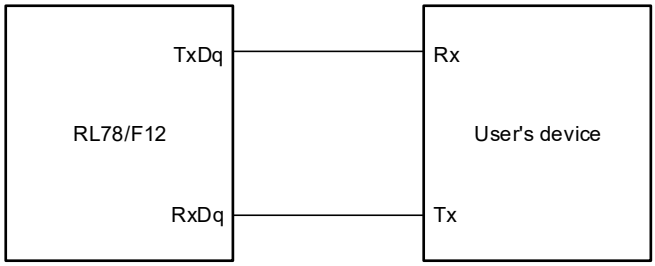
4.6.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

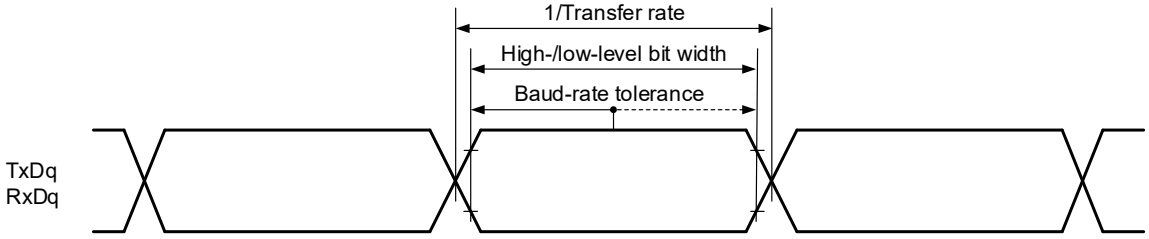
(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		Other than SNOOZE mode	f_{MCK}/256		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate			4.0	Mbps
		Receivable baud rate at SNOOZE mode	4800		4800	bps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remarks 1. q: UART number (q = 0 to 2, S0), g: PIM number (g = 0, 1, 5, 7), h: POM number (h = 0, 1, 5, 7)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 11, S0, S1))

Caution The pins mounted depend on the product.

(2) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$: internal clock output)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time Note 1	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V	CSI00 Note 1	125			ns
			Other than CSI00 Note 2	166.6			ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 – 12			ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 – 18			ns
SIp setup time (to $\overline{SCKp}$↑) Note 3	t_{SIK1}			44			ns
SIp hold time (from $\overline{SCKp}$↑) Note 3	t_{KSI1}			19			ns
SOp output delay time Note 4 (from $\overline{SCKp}$↓)	t_{KSO1}	C = 30 pF Note 5				25	ns

Notes 1. The value must also be 2/f_{CLK} or more.

2. The value must also be 4/f_{CLK} or more.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21, S0, S1), m: Unit number (m = 0, 1, S), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1, 5, 7), h: POM number (h = 0, 1, 5, 7)

Caution The pins mounted depend on the product.

(3) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$: external clock input)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}			
		2.7 V ≤ EV_{DD} < 4.0 V	f_{MCK} > 16 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑) **Note 1**	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+20			ns
SIp hold time (from $\overline{SCKp}$↑) **Note 1**	t_{KSI2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+31			ns
SOp output Delay time (from $\overline{SCKp}$↓) **Note 2**	t_{KSO2}	C = 30 pF **Note 3**	2.7 V ≤ EV_{DD} ≤ 5.5 V			2/f_{MCK}+44	ns

Notes 1. This applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time is "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. This applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output is "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SOp output lines.

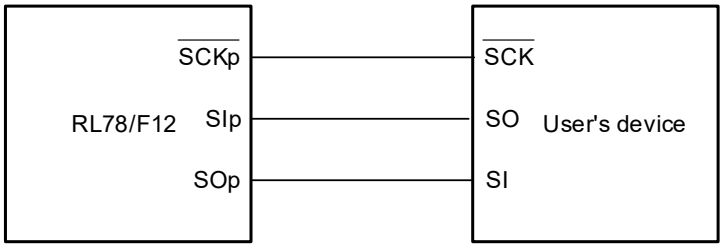
Caution Select the TTL input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, S0, S1), m: Unit number (m = 0, 1, S), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 5), h: POM number (h = 0, 1, 5, 7)

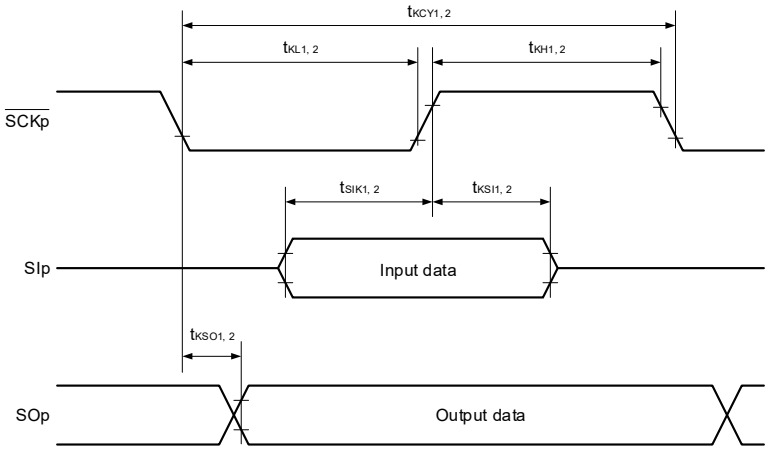
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11, S0, S1))

Caution The pins mounted depend on the product.

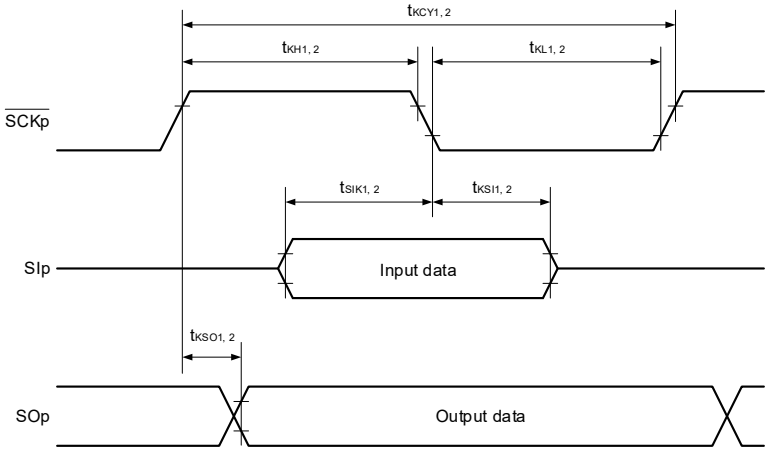
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, S0, S1)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11, S0, S1)

Caution The pins mounted depend on the product.

(4) During communication at same potential (simplified I^2C mode)

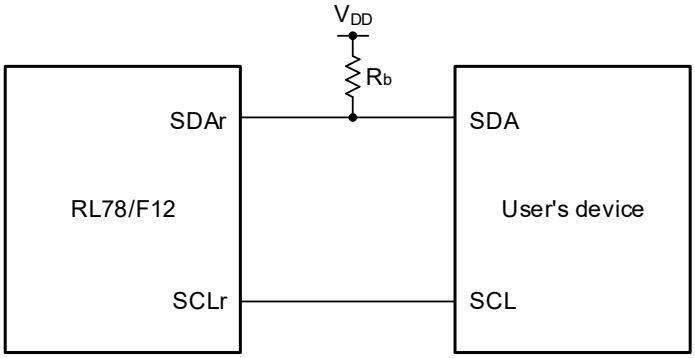
(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ		400	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 **Note**		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	0	355	ns

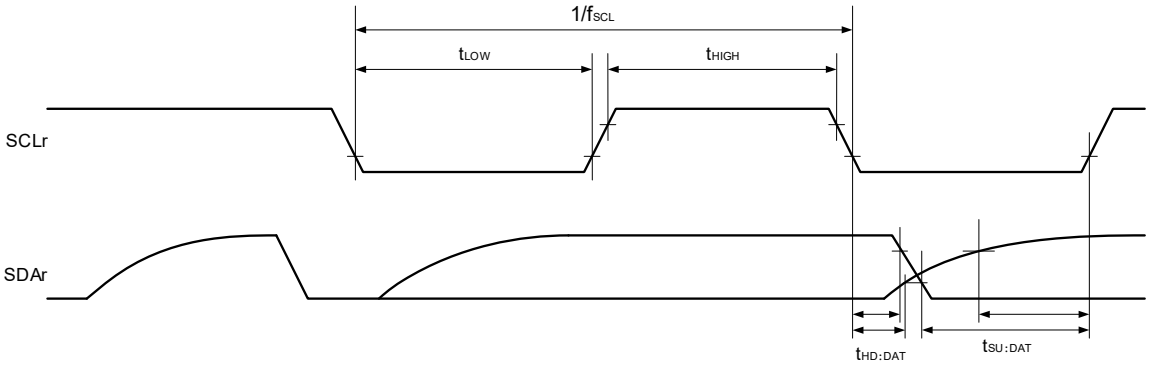
Note The value of f_{MCK} must be such that this does not exceed the hold time for SCLr = L or the hold time for SCLr = H.

Caution The pins mounted depend on the product.

Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 11, 20, 21), g: PIM number (g = 0, 1, 5), h: POM number (h = 0, 1, 5, 7)

3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11, S0, S1)

Caution The pins mounted depend on the product.

4.6.2 Serial interface IICA

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus:f_{CLK} ≥ 10 MHz					0	1000	kHz
		Fast mode:f_{CLK} ≥ 3.5 MHz			0	400			kHz
		Normal mode:f_{CLK} ≥ 1 MHz	0	100					kHz
Setup time of restart condition Note 1	$t_{SU:STA}$		4.7		0.6		0.26		μs
Hold time	$t_{HD:STA}$		4.0		0.6		0.26		μs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		0.5		μs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	3.45	0	0.9	0		μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		μs
Bus-free time	t_{BUF}		4.7		1.3		0.5		μs

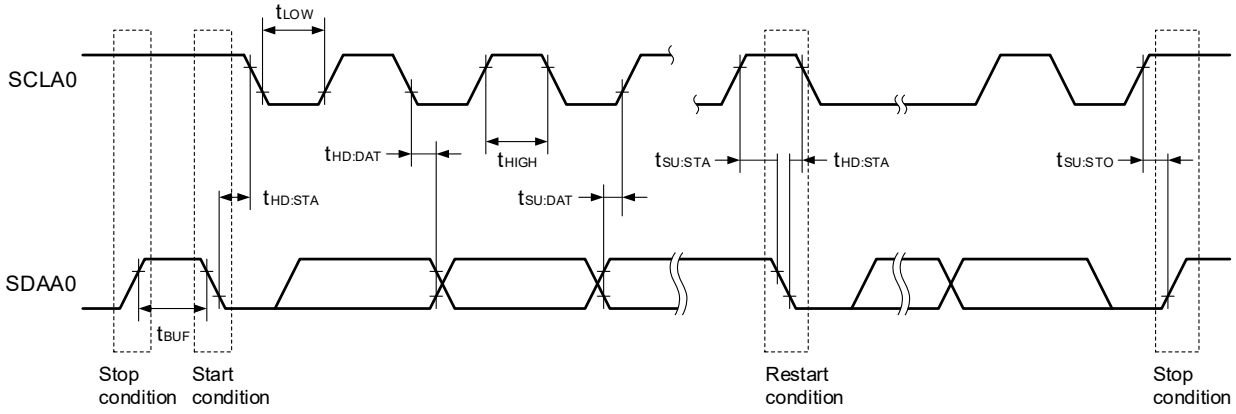
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Caution The pins mounted depend on the product.

4.6.3 LIN-UART

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.[Note]	Unit
Transfer rate	1/T			1	Mbps

Note However, the upper limit is f_{CLK}/8.

Caution The pins mounted depend on the product.

4.7 Analog Characteristics

4.7.1 A/D converter characteristics

(1) When the setting of AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1) and AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), this applies to the following ANI pins: ANI2 to ANI7 (the ANI pins for which V_{DD} is the power-supply voltage).

(T_A = –40 to +125°C, 2.7 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V)

<R>

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±3.0	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Reference voltage (-)	AV_{REFM}				0		V
Analog input voltage	V_{AIN}			AV_{REFM}		AV_{REFP}	V
	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

(2) When the setting of AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1) and AVREF (-) = AVREFM/ANI1 (ADREFM = 1), this applies to the following ANI pins: ANI16 to ANI19 (the ANI pins for which EVDD0 is the power-supply voltage).

(T_A = –40 to +125°C, 2.7 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V)

<R>

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±4.5	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Reference voltage (-)	AV_{REFM}				0		V
Analog input voltage	V_{AIN}			AV_{REFM}		AV_{REFP}	V
	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

(3) When the setting of AVREF (+) = VDD (ADREFP1 = 0, ADREFP0 = 0) and AVREF (-) = VSS (ADREFM = 0), this applies to the following ANI pins: ANI0 to ANI7.

(TA = –40 to +125°C, 2.7 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V, reference voltage (+) = VDD, reference voltage (-) = VSS)

<R>

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Resolution	RES				8		10	bit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ VDD ≤ 5.5 V	ANI0-ANI7		±1.2	±5.0	LSB
			2.7 V ≤ VDD < 5.5 V	ANI0-ANI7		±1.2	±5.5	LSB
Conversion time	tCONV	10-bit resolution	4.0 V ≤ VDD ≤ 5.5 V		2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V		3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±0.5	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±0.5	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±2.0	LSB
Reference voltage (+)	AVREFP				VDD			V
Reference voltage (-)	AVREFM				VSS			V
Analog input voltage	VAIN	ANI0-ANI7			VSS		VDD	V
	VBGR	2.7 V ≤ VDD ≤ 5.5 V			1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

(4) When the setting of AVREF (+) = VDD (ADREFP1 = 0, ADREFP0 = 0) and AVREF (-) = VSS (ADREFM = 0), this applies to the following ANI pins: ANI16 to ANI19.

(T_A = –40 to +125°C, 2.7 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V, reference voltage (+) = VDD, reference voltage (-) = VSS)

<R>

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		10	bit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ VDD ≤ 5.5 V	ANI16-ANI19		±1.2	±6.5	LSB
			2.7 V ≤ VDD < 5.5 V	ANI16-ANI19		±1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ VDD ≤ 5.5 V		2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V		3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V				±2.0	LSB
Reference voltage (+)	AV_{REFP}				VDD			V
Reference voltage (-)	AV_{REFM}				VSS			V
Analog input voltage	V_{AIN}	ANI16-ANI19			VSS		VDD	V
	V_{BGR}	2.7 V ≤ VDD ≤ 5.5 V			1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 2.1.1, 20-pin products to 2.1.5, 64-pin products, and 2.1.6, Pins for each product (pins other than port pins).

Caution The pins mounted depend on the product.

4.7.2 Temperature sensor characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/C
Operation stabilization wait time	t_{AMP}				5	μs

4.7.3 POR circuit characteristics

(T_A = –40 to +125°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.46	1.51	1.59	V
	V_{PDR}	Power supply fall time	1.45	1.50	1.58	V
Minimum pulse width	T_{PW}		300			μs
Detection delay time	T_{PD}				350	μs

4.7.4 LVD circuit characteristics

(a) Characteristics for LVD Detection at Reset and Interrupt modes

(T_A = –40 to +125°C, $V_{PDR} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}	Power supply rise time	3.96	4.06	4.25	V
			Power supply fall time	3.89	3.98	4.15	V
		V_{LVI1}	Power supply rise time	3.66	3.75	3.93	V
			Power supply fall time	3.58	3.67	3.83	V
		V_{LVI2}	Power supply rise time	3.06	3.13	3.28	V
			Power supply fall time	2.99	3.06	3.20	V
		V_{LVI3}	Power supply rise time	2.95	3.02	3.17	V
			Power supply fall time	2.89	2.96	3.09	V
		V_{LVI4}	Power supply rise time	2.85	2.92	3.07	V
			Power supply fall time	2.79	2.86	2.99	V
		V_{LVI5}	Power supply rise time	2.74	2.81	2.95	V
			Power supply fall time	2.68[Note]	2.75	2.88	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time		t_{LD}				300	μs

Note The minimum value lowers the minimum guaranteed voltage for operation (2.7 V). However, LVD detection performs in the same way as in normal mode (operation according to the same specification when V_{DD} is 2.7 V) until it is reset at reset mode.

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 5
The following relationship is formed under the same temperature conditions: the detection voltage at power supply rise time > the detection voltage at power supply fall time.

Caution The pins mounted depend on the product.

(b) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +125°C, $V_{PDR} \leq V_{DD} = EV_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVI5}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage: 2.7 V			2.68 Note	2.75	2.88	V
	V_{LVI4}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.85	2.92	3.07	V
				Falling interrupt voltage	2.79	2.86	2.99	V
	V_{LVI3}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.17	V
				Falling interrupt voltage	2.89	2.96	3.09	V
	V_{LVI0}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.96	4.06	4.25	V
				Falling interrupt voltage	3.89	3.98	4.15	V

Note The minimum value lowers the minimum guaranteed voltage for operation (2.7 V). However, LVD detection performs in the same way as in normal mode (operation according to the same specification when V_{DD} is 2.7 V) until it is reset at reset mode.

Remark The following relationship is formed under the same temperature conditions: the rising release reset voltage > the falling interrupt voltage > the falling reset voltage

4.7.5 Power supply rise time

(T_A = –40 to +125°C, $V_{SS} = EV_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum slew rate for the supply voltage to rise	S_{vrmax}	0 V → 2.7 V (CMODE0 = 1) (VPOC2 = 0 or 1)			50 Note 1	V/ms
Minimum slew rate for the supply voltage to rise Note 2	S_{vrmin}	0 V → 2.7 V (CMODE0 = 1)	6.5 Note 1			V/ms

Notes 1. In case the supply voltage falls to a level of V_{PDR} or below and a power-on reset is generated, the slew rate must not exceed the value S_{vrmax} even if the supply voltage does not go down to 0 V.

2. The minimum slew rate for the supply voltage (S_{vrmin}) must be met when the voltage detector (LVD) is not used (option byte bit VPOC2 = 1) and an external reset circuit releases before the supply voltage reaches V_{DD} (MIN.) (here 2.7 V).

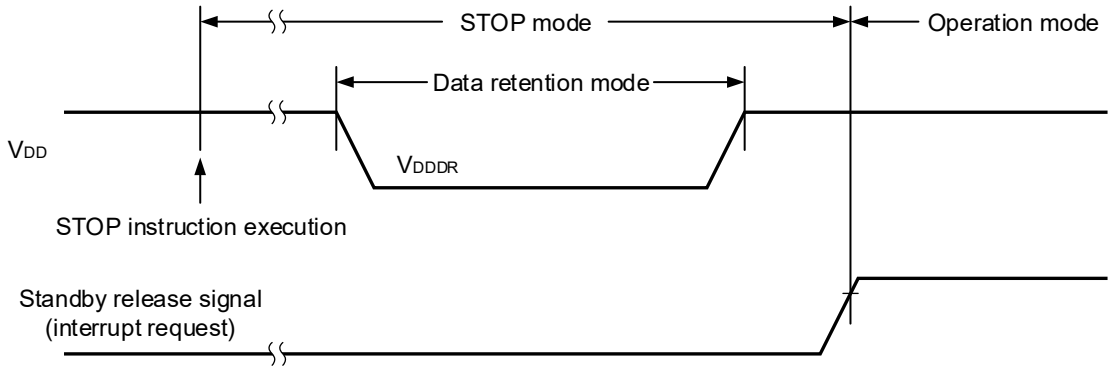
Caution The pins mounted depend on the product.

4.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +125°C V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}	STOP mode	1.45 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



4.9 Flash Memory Programming Characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency		f_{CLK}		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3		C_{erwr}	20 years retention (after rewrite) T_A = +85°C Note 4	1000			Times
Number of data flash rewrites Notes 1, 2, 3			20 years retention (after rewrite) T_A = +85°C Note 4	10000			
			5 years retention (after rewrite) T_A = +85°C Note 4	100000			
Erase time	Block erase	T_{erasa}		5			ms
write time		T_{wrwa}		10			μs

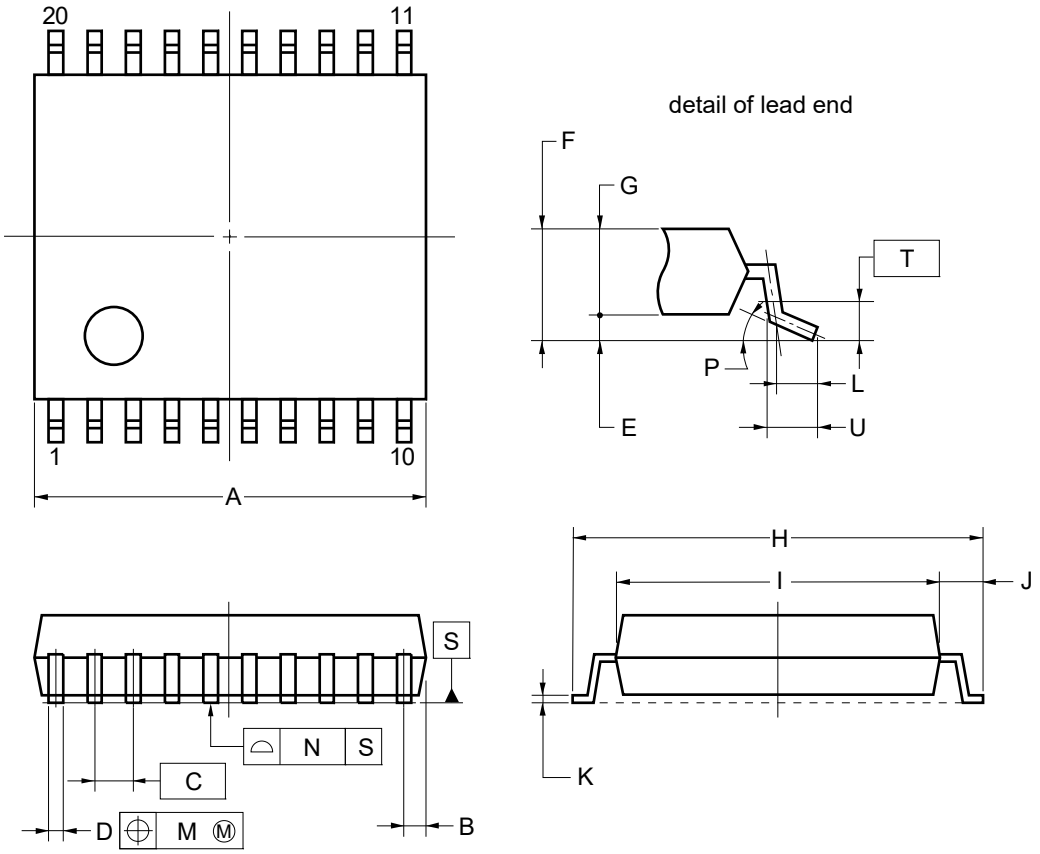
Notes 1. Retention years indicate a period between time for a rewrite and the next.
2. When using flash memory programmer and Renesas Electronics self programming library.
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas.
4. The specified data retention time is given under the condition that the average temperature (T_A) is 85°C or below.

5. PACKAGE DRAWING

5.1 20-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12



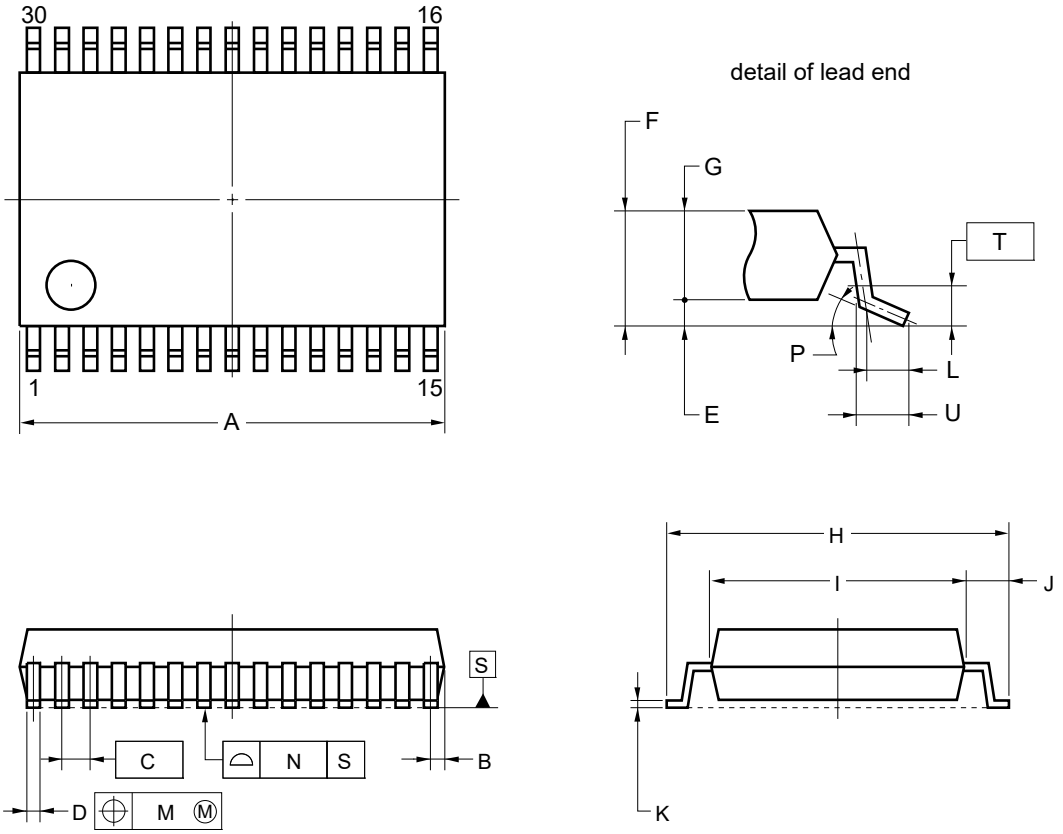
NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

5.2 30-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



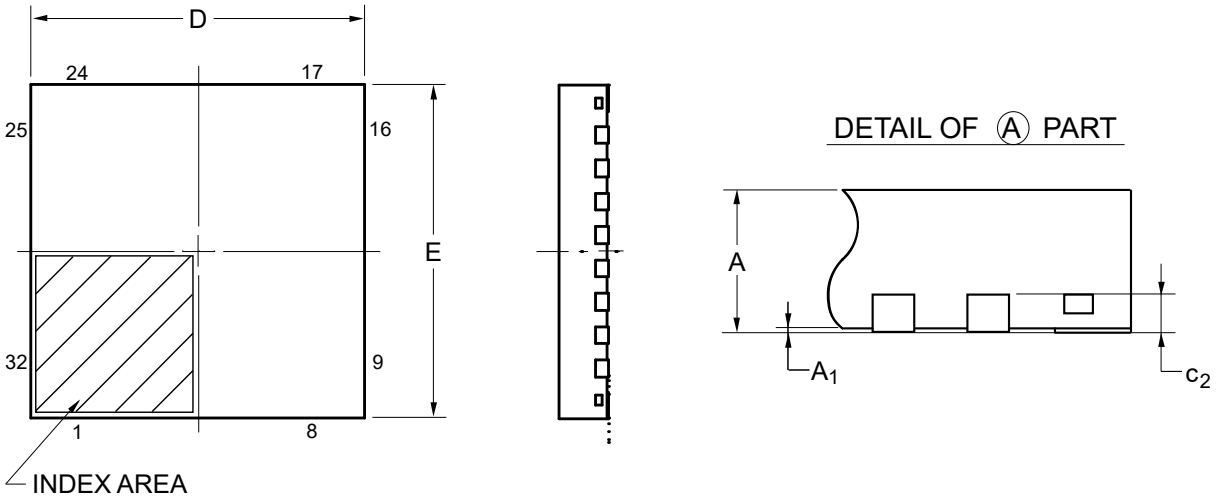
NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

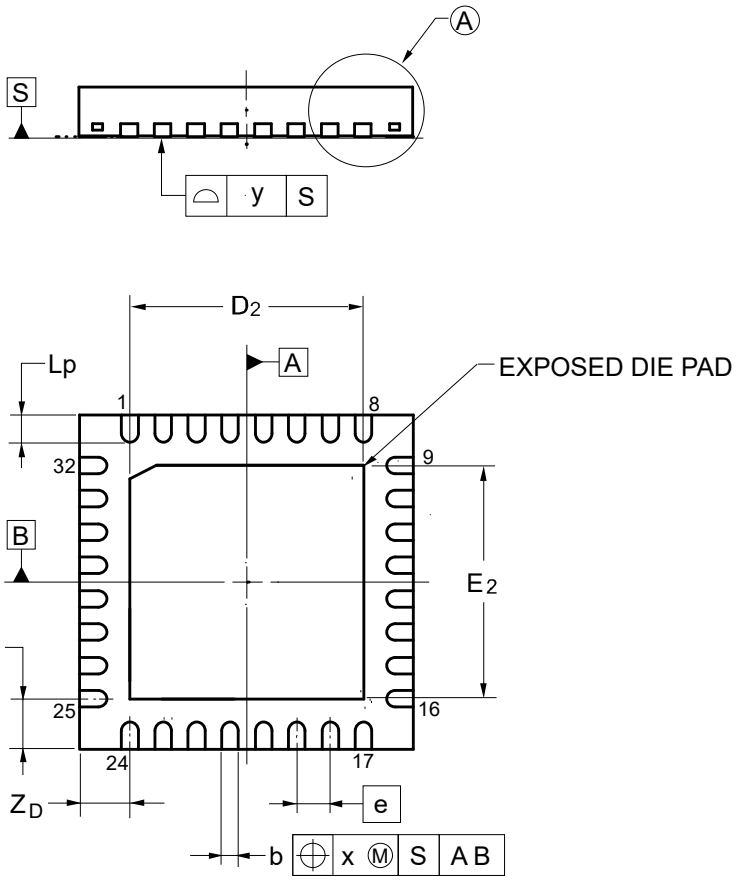
ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

5.3 32-pin products

<R>

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06

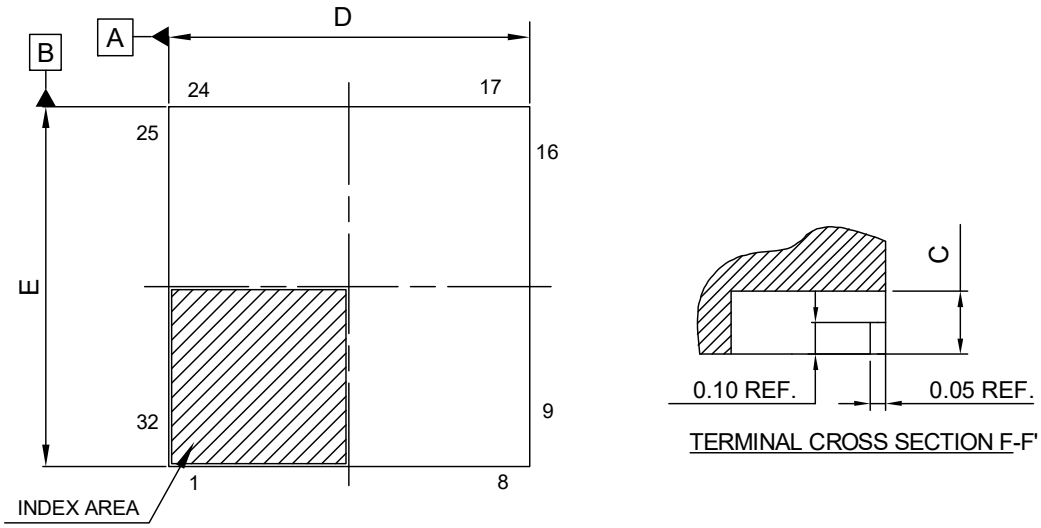


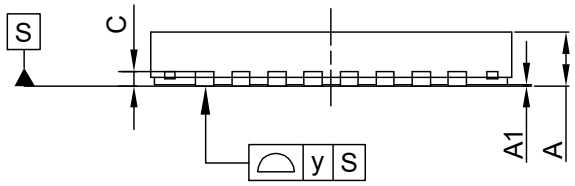


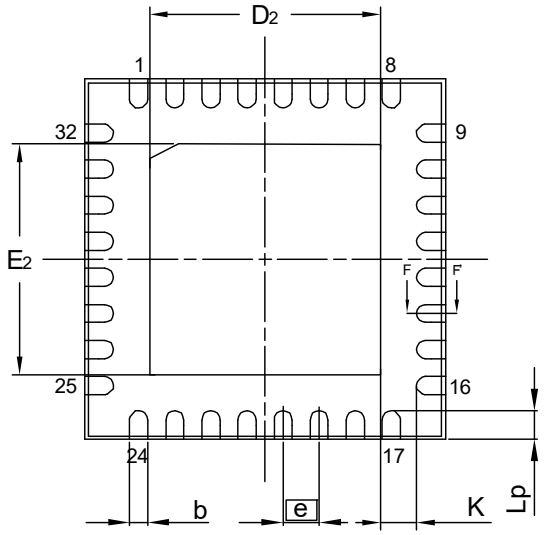
Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	3.50	—
E_2	—	3.50	—

<R>

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KH-A	0.06





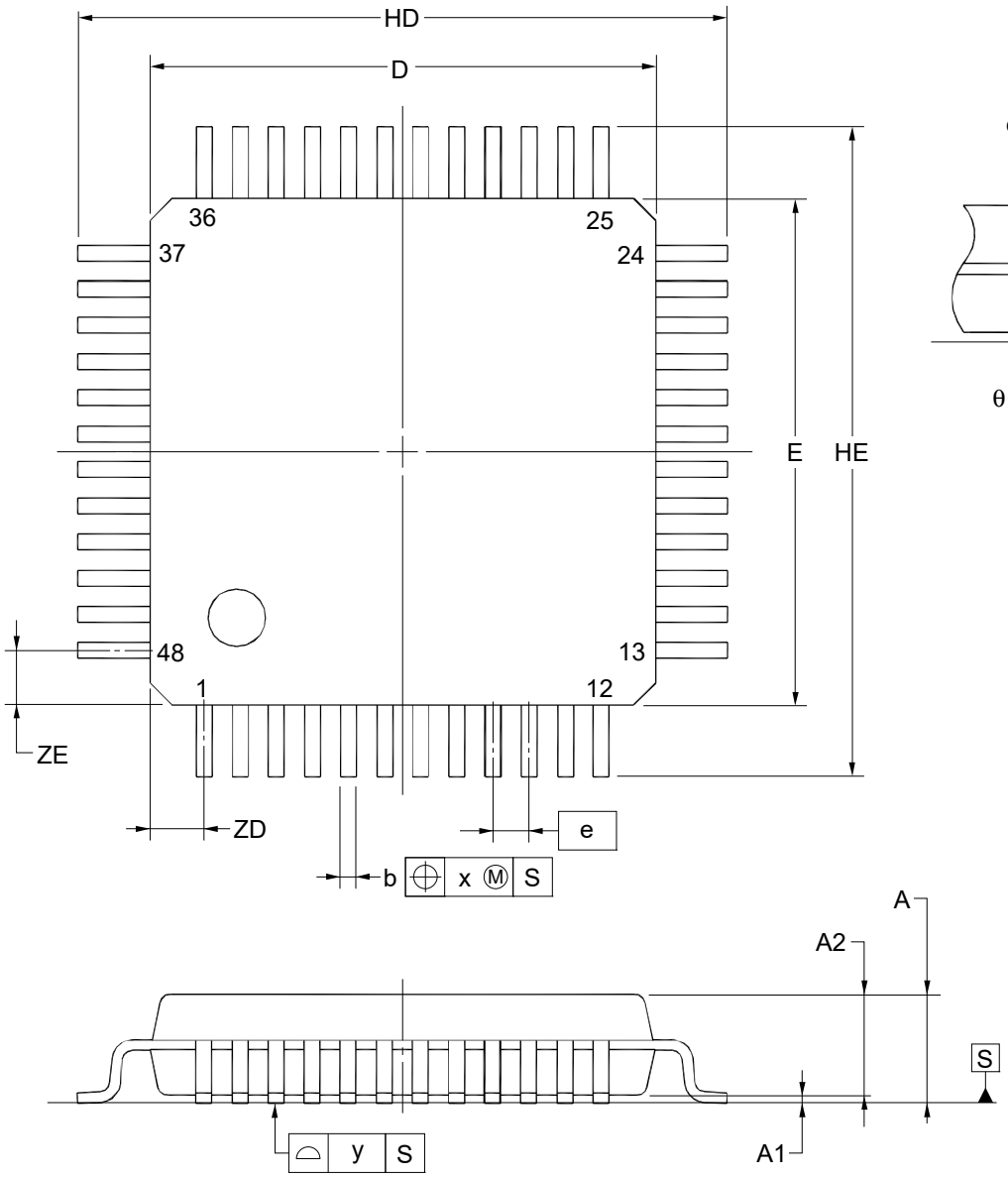


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	4.85	5.00	5.15
E	4.85	5.00	5.15
A	—	—	0.80
A_1	0.00	—	0.05
b	0.18	0.25	0.30
e	0.50 BSC		
Lp	0.35	0.40	0.45
y	—	—	0.08
c	—	0.20	—
K	0.20	—	—
D_2	—	3.20	—
E_2	—	3.20	—

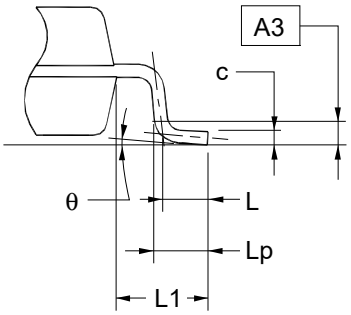
5.4 48-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



detail of lead end



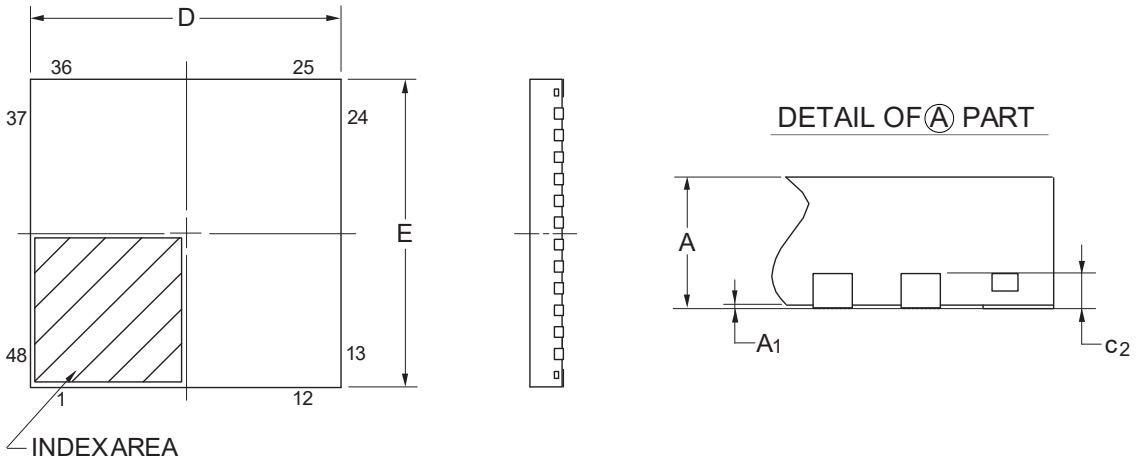
(UNIT:mm)

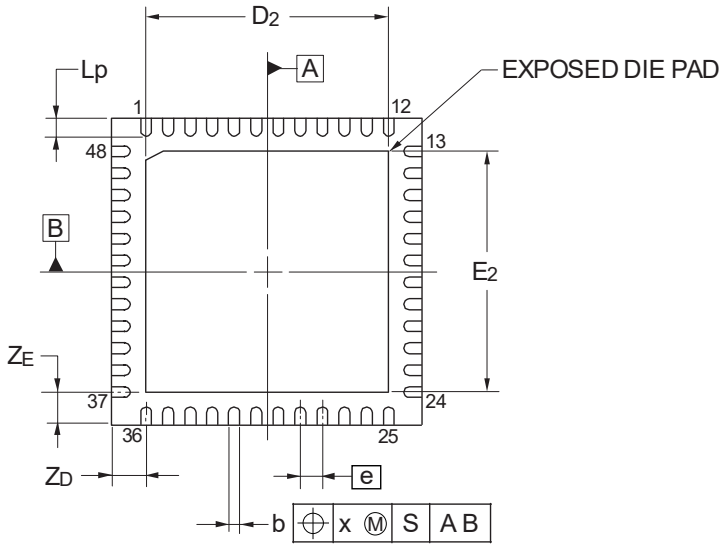
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13



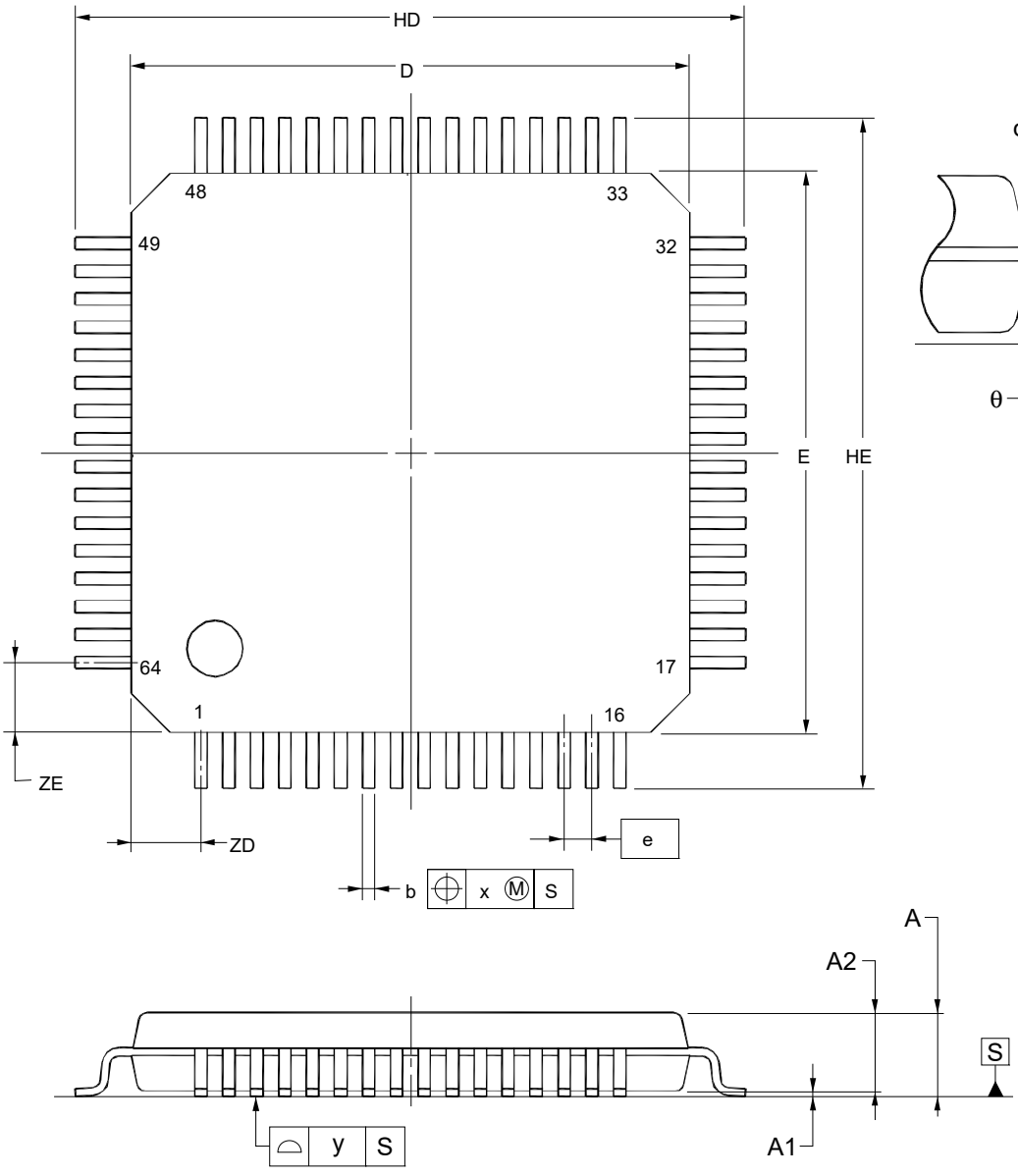


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2		5.50	—

5.5 64-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU	0.35



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

REVISION HISTORY	RL78/F12 Datasheet

Rev	Date	Description	
		Page	Summary
1.11	Dec 27, 2024	-	First edition issued.
1.20	May 30, 2025	2	Modification of Part Number in 1.2 Ordering Information
		3	Corrected the description of title (SSOP to LSSOP)
		4	Corrected the description of title (SSOP to LSSOP)
		5	Corrected the description of title (WQFN to HWQFN)
		6	Corrected the description of title (LQFP to LFQFP)
		7	Corrected the description of title (WQFN to HWQFN)
		8	Corrected the description of title (LQFP to LFQFP)
		10	Modification of Figure 1.5.1 20-pin products
		11	Modification of Figure 1.5.2 30-pin products
		12	Modification of Figure 1.5.3 32-pin products
		13	Modification of Figure 1.5.4 48-pin products
		14	Modification of Figure 1.5.5 64-pin products
		52-55	Corrected the description of "Overall error" in the table (TYP. 1.2 to ±1.2).
		84-87	Corrected the description of "Overall error" in the table (TYP. 1.2 to ±1.2).
		92	Modification of Figure 5.1 20-pin products
		93	Modification of Figure 5.2 30-pin products
		94	Modification of Figure 5.3 32-pin products
		95	Addition of Figure 5.3 32-pin products
		96	Modification of Figure 5.4 48-pin products
		97	Addition of Figure 5.4 48-pin products
		98	Modification of Figure 5.5 64-pin products

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

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