

RJL5014DPP-A0

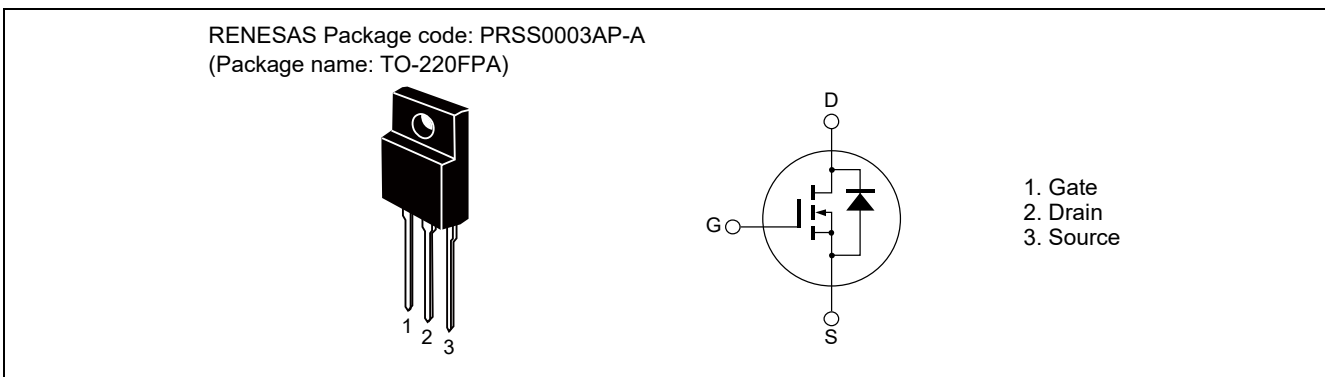
500V - 19A - MOS FET
High Speed Power Switching

R07DS1436EJ0100
Rev.1.00
Mar.23.2021

Features

- Built-in fast recovery diode
- Low on-resistance
 $R_{DS(on)} = 0.32 \Omega$ typ. (at $I_D = 9.5 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_a = 25 \text{ }^\circ\text{C}$)
- Low leakage current
- High speed switching
- Quality grade: Standard

Outline



Absolute Maximum Ratings

($T_a = 25 \text{ }^\circ\text{C}$)

| Item | Symbol | Ratings | Unit |
|---|------------------------|-------------|------------------|
| Drain to source voltage | V_{DSS} | 500 | V |
| Gate to source voltage | V_{GSS} | ± 30 | V |
| Drain current | I_D Notes4 | 19 | A |
| Drain peak current | $I_{D(pulse)}$ Notes1 | 57 | A |
| Body-drain diode reverse drain current | I_{DR} | 19 | A |
| Body-drain diode reverse drain peak current | $I_{DR(pulse)}$ Notes1 | 57 | A |
| Avalanche current | I_{AP} Notes3 | 4 | A |
| Avalanche energy | E_{AR} Notes3 | 0.88 | mJ |
| Channel dissipation | P_{ch} Notes2 | 35 | W |
| Channel temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

Note: Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data.

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1 \%$
 2. Value at $T_c = 25 \text{ }^\circ\text{C}$
 3. $ST_{ch} = 25 \text{ }^\circ\text{C}$, $T_{ch} \leq 150 \text{ }^\circ\text{C}$
 4. Limited by maximum safe operation area

Thermal Resistance Characteristics

(Ta = 25 °C)

| Item | Symbol | Max. Value ^{Notes5} | Unit |
|-----------------------------------|-----------------|------------------------------|------|
| Channel to case thermal impedance | θ_{ch-c} | 3.57 | °C/W |

Notes: 5. Designed target value on Renesas measurement condition. (Not tested)

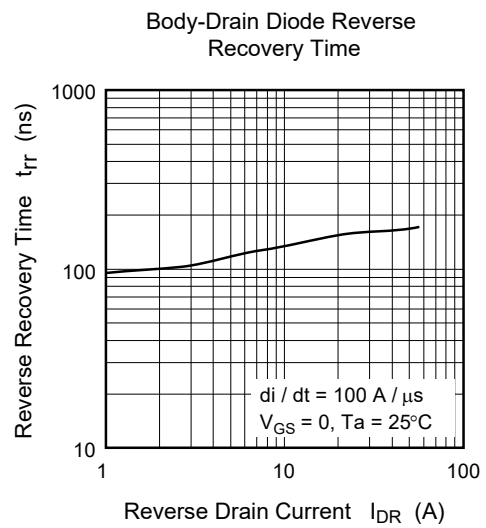
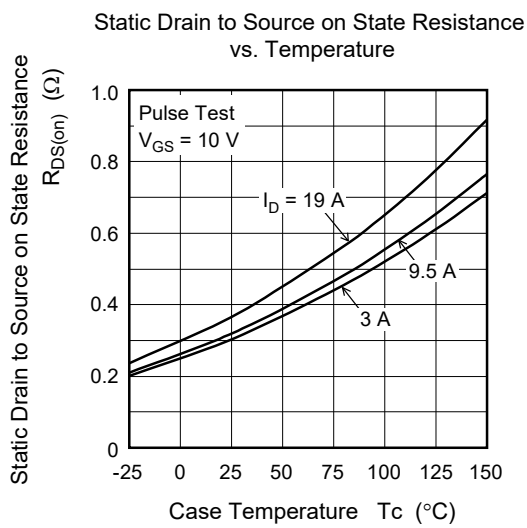
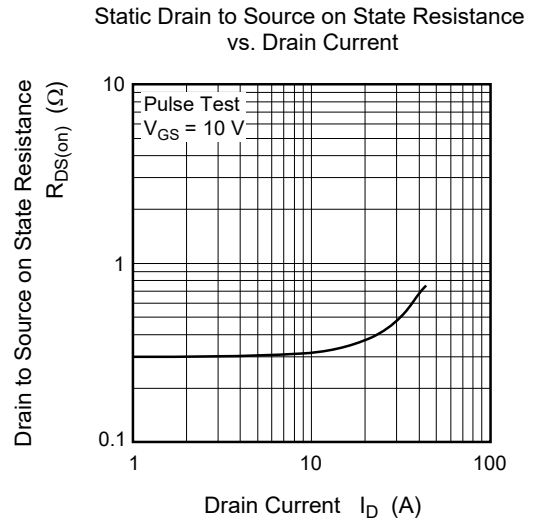
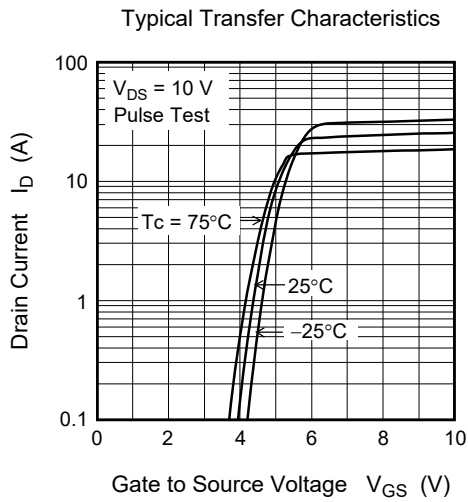
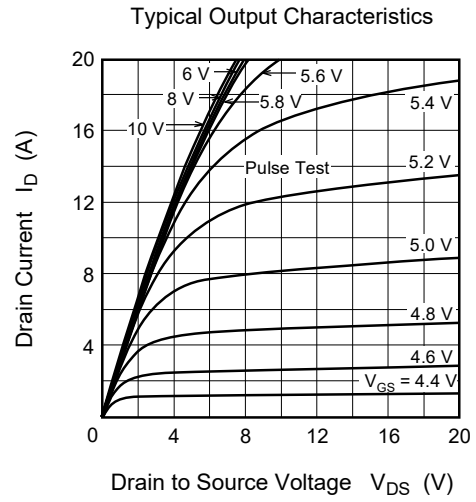
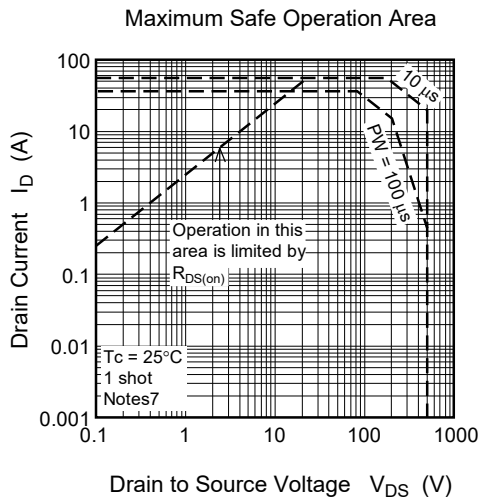
Electrical Characteristics

(Ta = 25 °C)

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---------------|-----|------|-----------|---------------|--|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 500 | — | — | V | $I_D = 10 \text{ mA}$, $V_{GS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | 10 | μA | $V_{DS} = 500 \text{ V}$, $V_{GS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 0.1 | μA | $V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 2.0 | — | 4.0 | V | $V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.32 | 0.40 | Ω | $I_D = 9.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Notes6} |
| Input capacitance | C_{iss} | — | 1700 | — | pF | $V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$ |
| Output capacitance | C_{oss} | — | 190 | — | pF | |
| Reverse transfer capacitance | C_{rss} | — | 23 | — | pF | |
| Turn-on delay time | $t_{d(on)}$ | — | 32 | — | ns | $I_D = 9.5 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 26.3 \Omega$ $R_g = 10 \Omega$ |
| Rise time | t_r | — | 27 | — | ns | |
| Turn-off delay time | $t_{d(off)}$ | — | 95 | — | ns | |
| Fall time | t_f | — | 20 | — | ns | |
| Total gate charge | Q_g | — | 43 | — | nC | $V_{DD} = 400 \text{ V}$ |
| Gate to source charge | Q_{gs} | — | 8.2 | — | nC | $V_{GS} = 10 \text{ V}$ |
| Gate to drain charge | Q_{gd} | — | 21.8 | — | nC | $I_D = 19 \text{ A}$ |
| Body-drain diode forward voltage | V_{DF} | — | 1.00 | 1.65 | V | $I_F = 19 \text{ A}$, $V_{GS} = 0$ ^{Notes6} |
| Body-drain diode reverse recovery time | t_{rr} | — | 160 | — | ns | $I_F = 19 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$ |

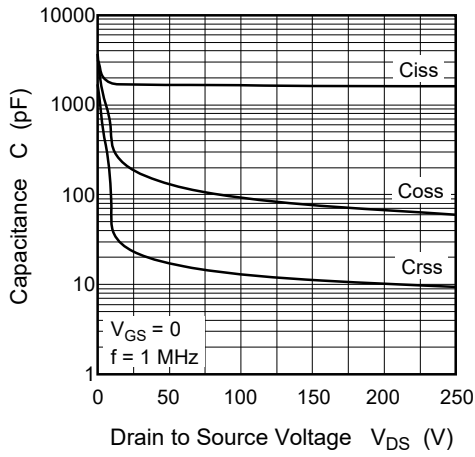
Notes: 6. Pulse test

Main Characteristics

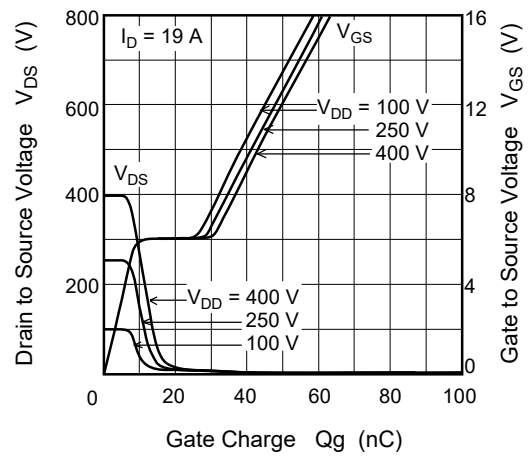


Notes: 7. Designed target value on Renesas measurement condition. (Not tested)
 Renesas recommends that operating conditions are designed according to a document "Power MOS FET - IGBT Attention of Handling Semiconductor Devices".

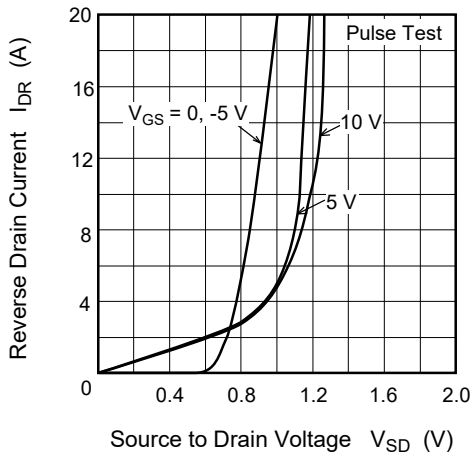
Typical Capacitance vs. Drain to Source Voltage



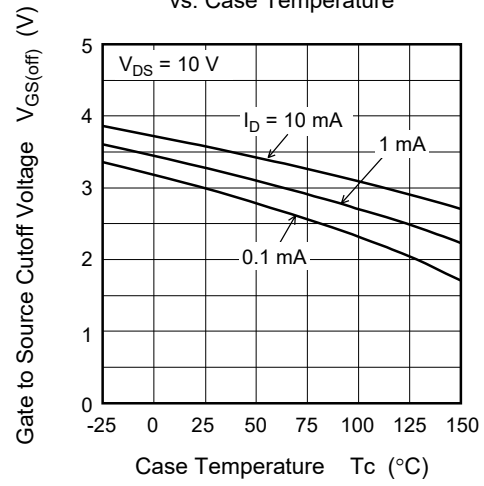
Dynamic Input Characteristics

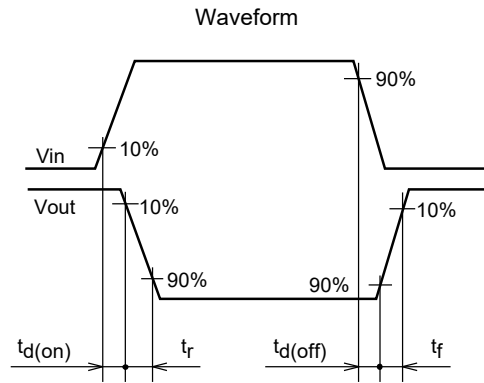
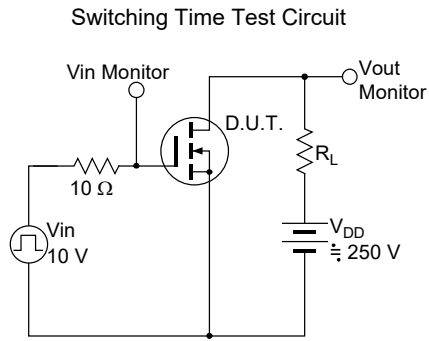
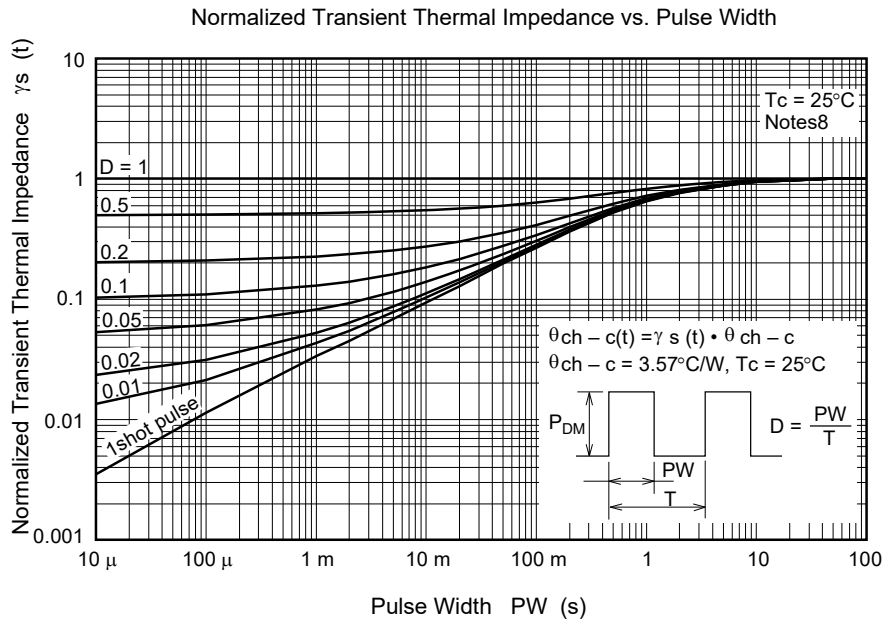


Reverse Drain Current vs. Source to Drain Voltage



Gate to Source Cutoff Voltage vs. Case Temperature



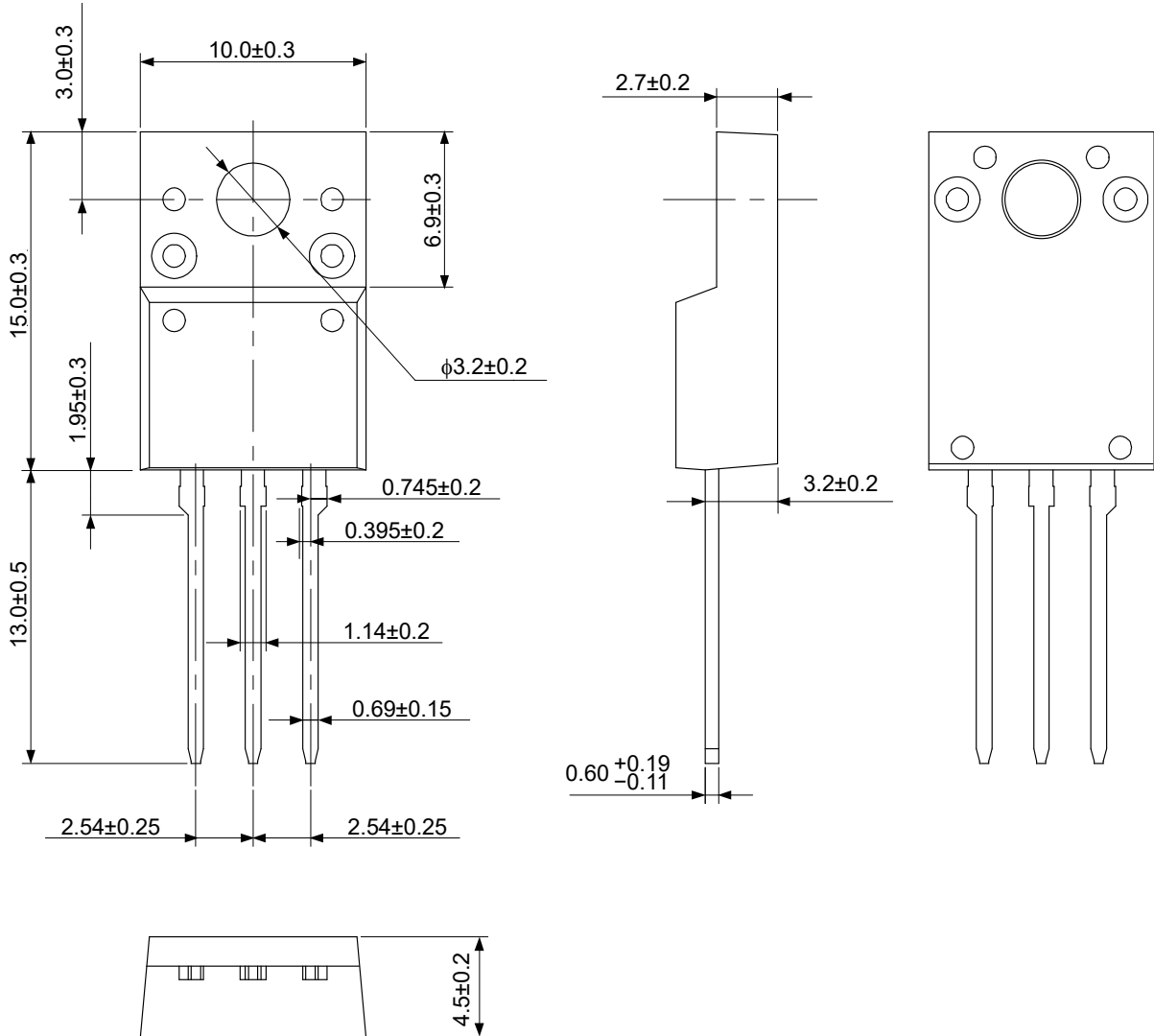


Notes: 8. Designed target value on Renesas measurement condition. (Not tested)

Package Dimensions

| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|--------------|--------------------|--------------|---------------|----------------|
| TO-220FPA | — | PRSS0003AP-A | TO-220FPA | 1.65 |

Unit: mm



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Ordering Information

| Orderable Part No. | Quantity | Shipping Container |
|--------------------|----------|--------------------|
| RJL5014DPP-A0#T2 | 2500 pcs | Box (Tube) |

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