RJK0635DSP

60V, 3.5A, 98mΩ max.
N Channel Power MOS FET
Power Switching

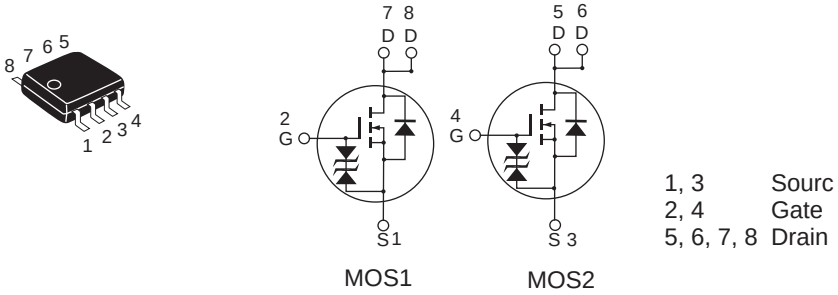
R07DS1345EJ0301
Rev.3.01
Nov.24.2016

Features

- Capable of 2.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
- Pb-free

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8<FP-8DAV>)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±12	V
Drain current	I_D	3.5	A
Drain peak current	$I_{D(pulse)}$ Note1	14	A
Body-drain diode reverse drain current	I_{DR}	3.5	A
Avalanche current	I_{AP} Note 2	3.5	A
Avalanche energy	E_{AS} Note 2	1.05	mJ
Channel dissipation	Pch Note3	1.2	W
Channel dissipation	Pch Note4	1.8	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s
4. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics

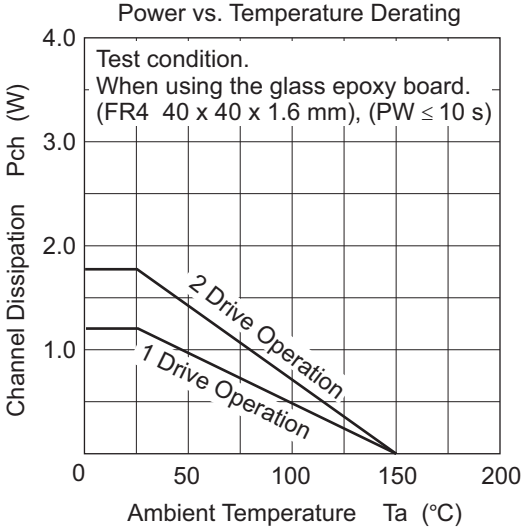
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±12	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±10 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1	μA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	75	98	mΩ	I_D = 1.75 A, V_{GS} = 4.5 V Note5
	$R_{DS(on)}$	—	85	119	mΩ	I_D = 1.75 A, V_{GS} = 2.5 V Note5
Forward transfer admittance	$\|y_{fs}\|$	6	10	—	S	I_D = 1.75 A, V_{DS} = 10 V Note5
Input capacitance	Ciss	—	590	—	pF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance	Coss	—	60	—	pF	
Reverse transfer capacitance	Crss	—	35	—	pF	
Total gate charge	Qg	—	6	—	nc	V_{DD} = 10 V, V_{GS} = 4.5 V, I_D = 3.5 A
Gate to source charge	Qgs	—	1.2	—	nc	
Gate to drain charge	Qgd	—	1.4	—	nc	
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	V_{GS} = 10 V, I_D = 1.75 A, V_{DD} ≅ 10 V, R_L = 5.7 Ω, Rg = 4.7 Ω
Rise time	t_r	—	70	—	ns	
Turn-off delay time	$t_{d(off)}$	—	41	—	ns	
Fall time	t_f	—	4.2	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.81	1.06	V	I_F = 3.5 A, V_{GS} = 0 Note5
Body–drain diode reverse recovery time	t_{rr}	—	20	—	ns	I_F = 3.5 A, V_{GS} = 0 V, di_F/dt = 100 A/μs

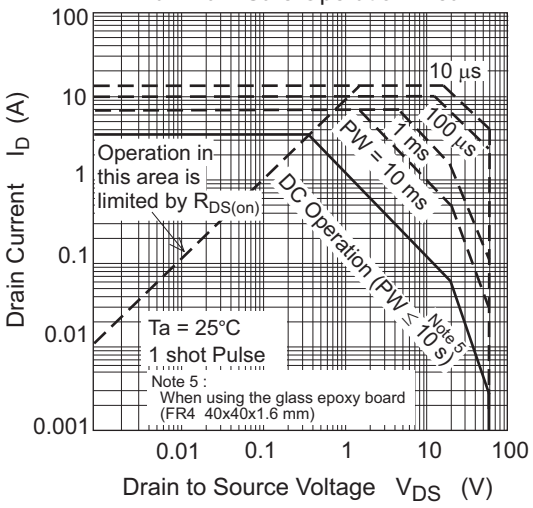
Notes: 5. Pulse test

Main Characteristics

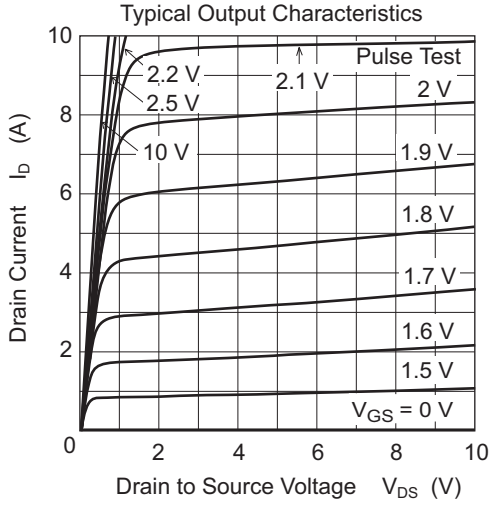
Power vs. Temperature Derating



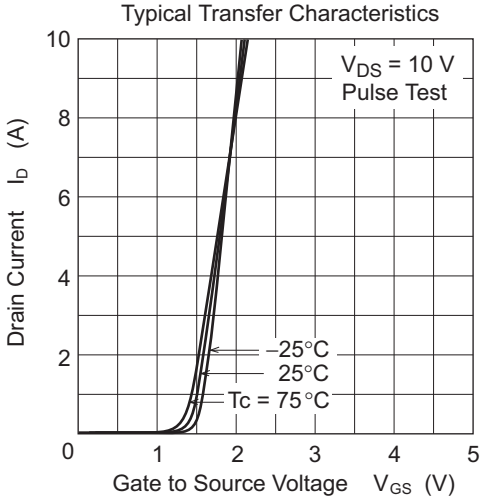
Maximum Safe Operation Area



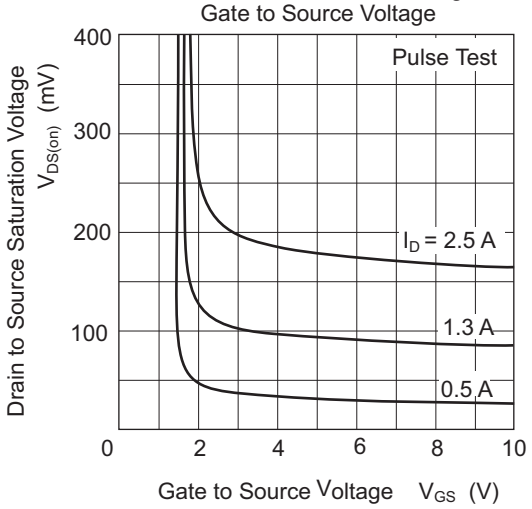
Typical Output Characteristics



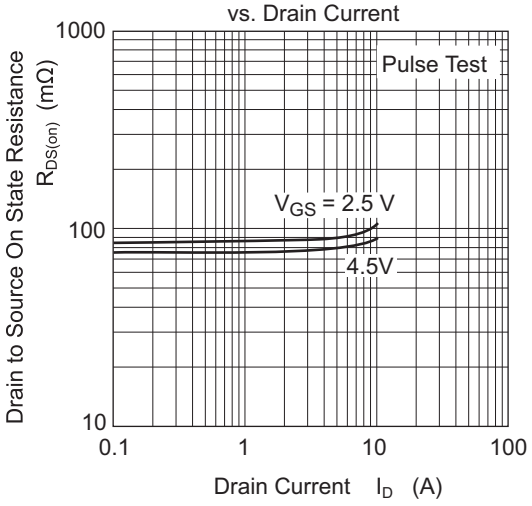
Typical Transfer Characteristics



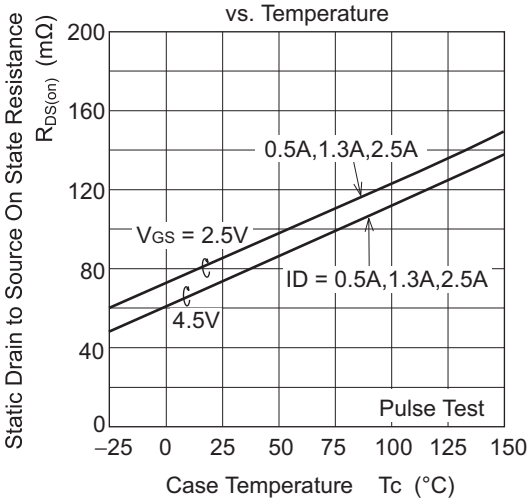
Drain to Source Saturation Voltage vs. Gate to Source Voltage



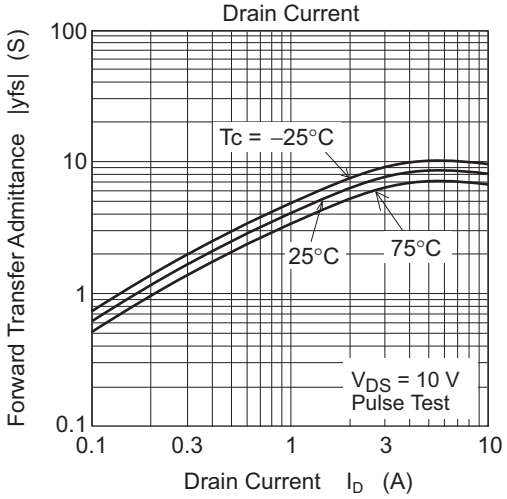
Static Drain to Source on State Resistance vs. Drain Current



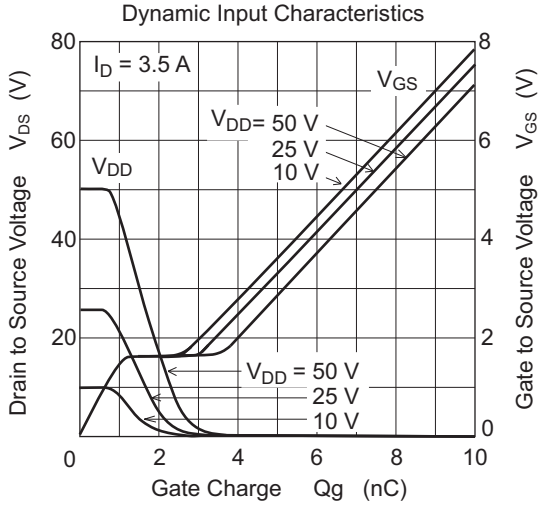
Static Drain to Source On State Resistance vs. Temperature



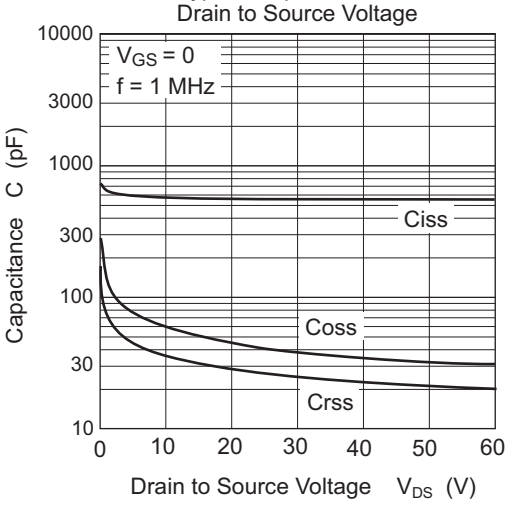
Forward Transfer Admittance vs. Drain Current



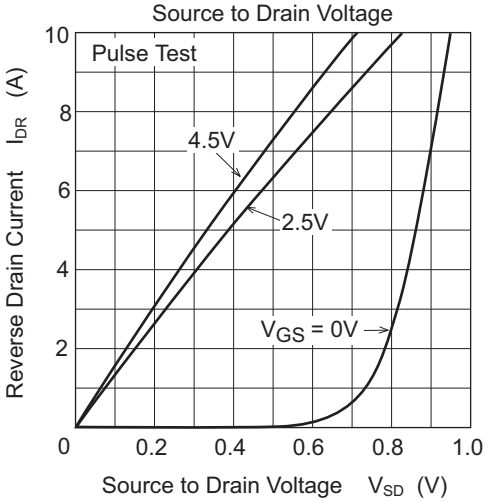
Dynamic Input Characteristics



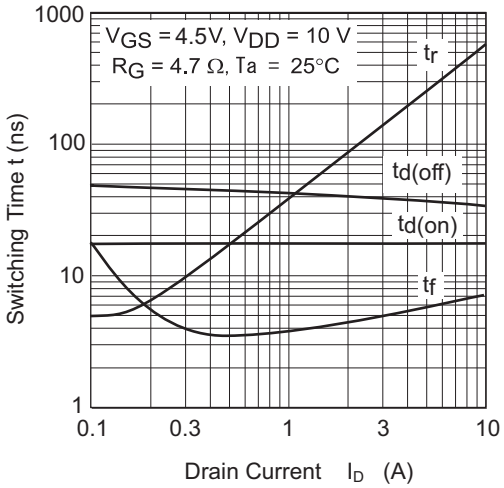
Typical Capacitance vs. Drain to Source Voltage



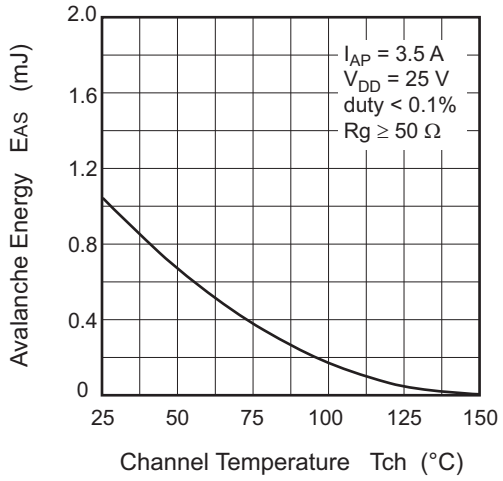
Reverse Drain Current vs. Source to Drain Voltage



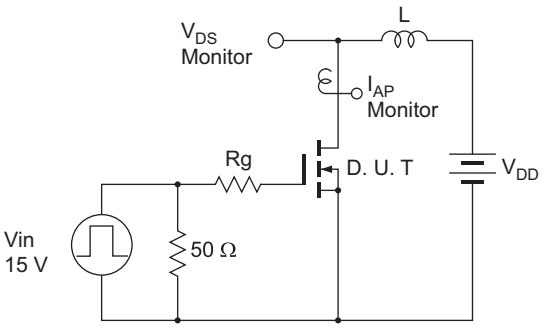
Switching Characteristics



Maximum Avalanche Energy vs.
Channel Temperature Derating

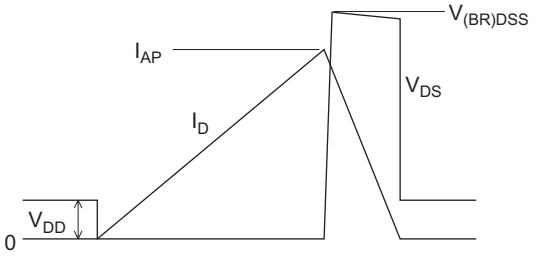


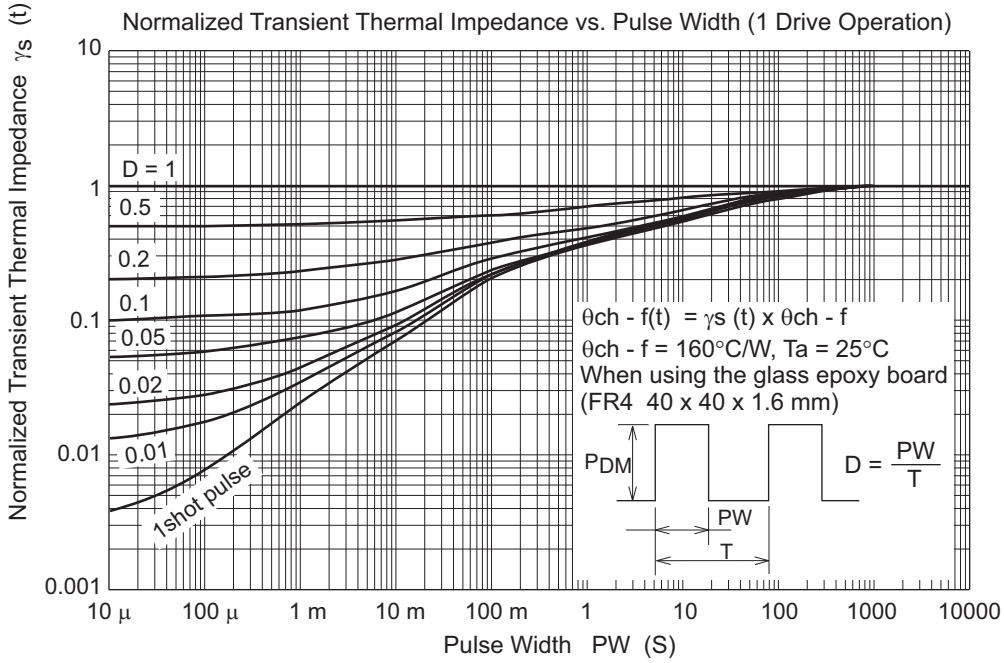
Avalanche Test Circuit

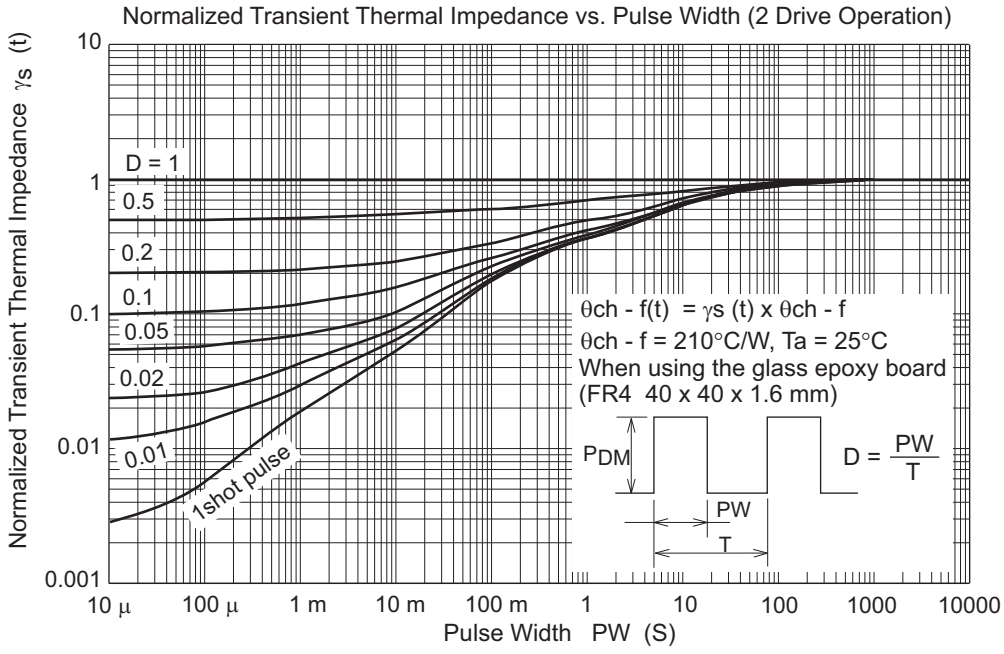


Avalanche Waveform

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

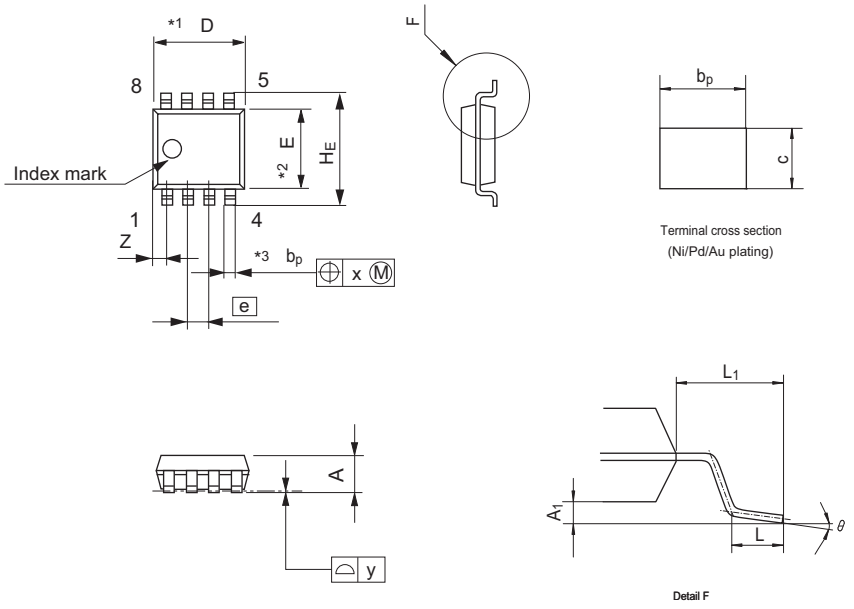



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) x θch - f
θch - f = 160°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)
PDM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) x θch - f
θch - f = 210°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)
PDM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK0635DSP-00-J0	2500 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将本文档中记载的瑞萨电子产品或技术用于与军事应用或者军事用途有关的任何目的（如大规模杀伤性武器的开发等）。在将本文档中记载的瑞萨电子产品或技术进行出口时，应当遵守相应的出口管制法律法规，并按照上述法律法规所规定的程序进行。
10. 向第三方分销或处分产品或者以其他方式将产品置于第三方控制之下的瑞萨电子产品买方或分销商，有责任事先向上述第三方通知本文档规定的内容和条件；对于用户或第三方因非法使用瑞萨电子产品而遭受的任何损失，瑞萨电子不承担任何责任。
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(注1) 瑞萨电子：在本文档中指瑞萨电子株式会社及其控股子公司。
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SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL Ⅱ Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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