RH850/P1M-E

Renesas microcontroller

Section 1 Overview

RH850/P1M-E is a product series of Renesas Electronics' single-chip microcontroller RH850 family. This section describes the overview of RH850/P1M-E.

This product has Security installed. For the specification of Security function, please contact with agent/distributor.

1.1 Outline

This product is a 32-bit single-chip microcontroller with multiple CPUs, Code Flash, Data Flash, RAM modules, DMA controllers, many communication interfaces that are used in the automotive applications, A/D converters, timer units, etc.
The main features are as below.

(1) RH850 CPU

This product contains two RH850G3Ms: one operates as the master CPU for normal operation and another as a checker CPU that monitors the operation of the master CPU. The two CPUs operate in lock step mode.

The architecture of this dual-core CPU unit realizes the compact footprint of the programs by 2-byte basic instructions and high-level language compiler oriented instruction sets. This dual-core CPU unit has very quick interrupt response time so that it can support hard real-time applications.

(2) On-chip Code Flash and Data Flash

This chip has high-speed Code Flash from which the CPU can fetch the instructions and the constant data. Its capacity is up to 2MB. This Code Flash can be reprogrammed in the situation that the chip is mounted in the application systems.

This chip also has Data Flash with EEPROM emulation capability. Its capacity is up to 64KB.

(3) Rich peripheral functionality

The RH850/P1M-E incorporates standard communication controllers such as CAN, LIN, FlexRay, and serial communications in addition to timers and A/D converters best suited for the automobile chassis applications. In addition, the RH850/P1M-E incorporates SENT and PSI5 communication controllers that can be used for sensor interface.

(4) Functional safety support

This chip equips several dedicated functionalities including the Lock-Step Dual Core configuration for the CPU, the memory protection with ECC, the bus protection with ECC, the peripheral module protection, and voltage/clock monitors to support the functional safety standard (ASIL) required in the automotive applications.

1.2 Application Fields

- Automotive field (including chassis control system)

1.3 Specification Overview

Table 1.1 Features in Each Product (1/2)

Product				RH850/P1M-E		
				100-pin	144-pin	
Package				LFQFP100 (14x14)	LFQFP144 (16x16)	LFQFP144 (20x20)
Product name	eVR	1MB		R7F701382	R7F701384	R7F701386
		2MB		R7F701376	R7F701378	R7F701380
	DPS	1MB		R7F701381	R7F701383	R7F701385
		2MB		R7F701375	R7F701377	R7F701379
CPU Subsystem	Frequency			160 MHz Main OSC = 16 MHz only		
	Main Core			1		
	Lockstep			Yes		
	FPU	Double prec.		Yes		
	MPU			16 ch		
	Cache (Inst.)			16 KB 4 way		
	RAM	Local RAM		128 KB		
		Global RAM		64 KB		
		Trace RAM		32 KB		
		ERAM (Emulation RAM)		32 KB[*1]/8 KB[*2]		
	INTC	INTC1		32 ch Redundant		
		INTC2		352 ch No Redundancy		
	DMA	DMAC		16 ch Redundant		
		DTS		128 ch Redundant		
Flash Memory	Code Flash			2 MB/1 MB		
	DATA Flash			64 KB[*1]/32 KB[*2]		
Safety	ECM			Yes		
	CVM			Yes		
	BIST with status flag			Yes		
	ERROROUT			Yes		
	Clock monitor			Yes		
A/D Converter	ADC 12 bit	module		2		
		Temperature sensor		Yes		
		Analog input	ADCG0	9 ch	12 ch	
			ADCG1	10 ch	12 ch	
		T & H	ADCG0	6		
			ADCG1	4		

Table 1.1 Features in Each Product (2/2)

Product			RH850/P1M-E	
			100-pin	144-pin
Timer	TAUD (16 bit × 16 ch)	modules	3	
	TAUJ (32 bit × 4 ch)	modules	3	
	TSG3	modules	2	
	TAPA (Hi-Z control)	modules	4	
	ENCA	modules	2	
	OSTM	modules	5	
	OSTM (Output)	modules	2	
	WDT	modules	1	
	TPBA (Timer Pattern Buffer)	modules	2	
	PIC (Peripheral interconnect)		Yes	
	Clock out	modules	2	
Communication Interface	RS-CANFD	channels	3	
	FlexRay	channels	2	
	PSI5	channels	2	
	RSENT	channels	5	6
	SCI 3 (Sync/Async USART)	channels	3	
	RLIN3 (LIN master/UART)	channels	2	
	CSIG (SPI)	channels	1	
	CSIH (SPI)	channels	4	
DataCRC			4	
Security (ICUS)			Yes	
Debug	Nexus-JTAG		Yes	
	LDU		Yes	
	AUD-RAM monitor		No	
	Branch Trace (for Debug) (Output)		No	
	Data Trace (for Debug) (Output)		No	
	Internal Branch Trace (to Trace RAM)		Yes	
	Internal Data Trace (to Trace RAM)		Yes	
	Measurement (Memory Read)		Yes	
Power Supply	Core		1.25 (DPS), eVR	
	I/O		3.3/5.0	
	ADC		3.3/5.0	

Note 1. Only available in devices with 2-MB flash memory.
Note 2. Only available in devices with 1-MB flash memory.

1.4 Pin Connection Diagram

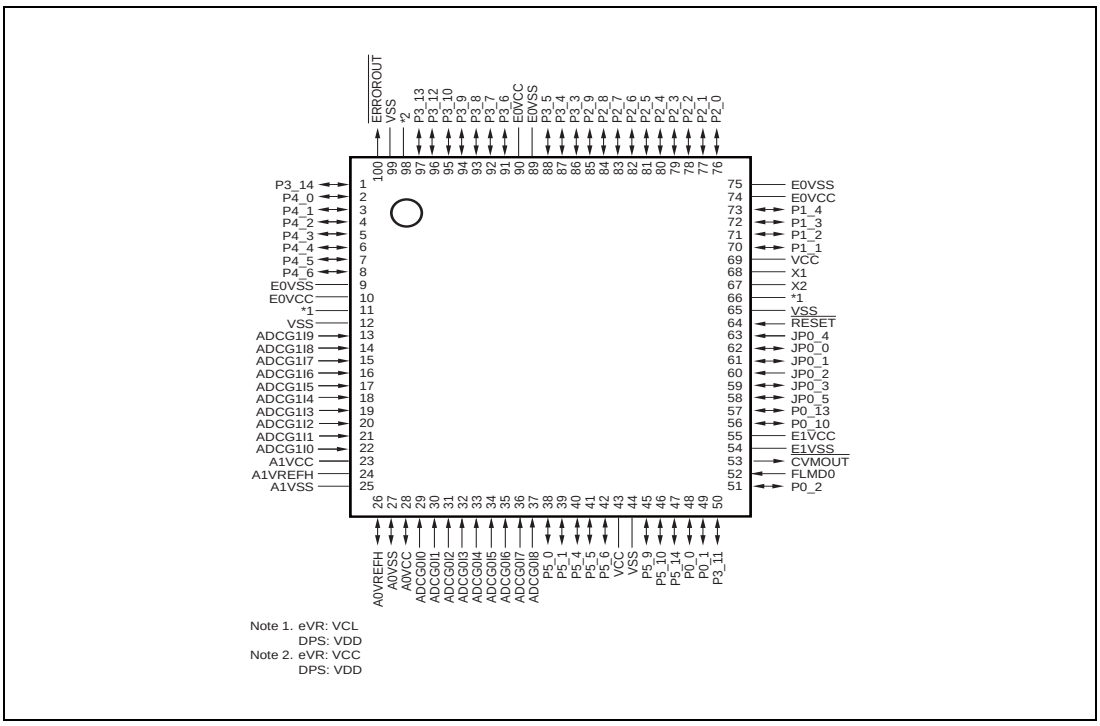
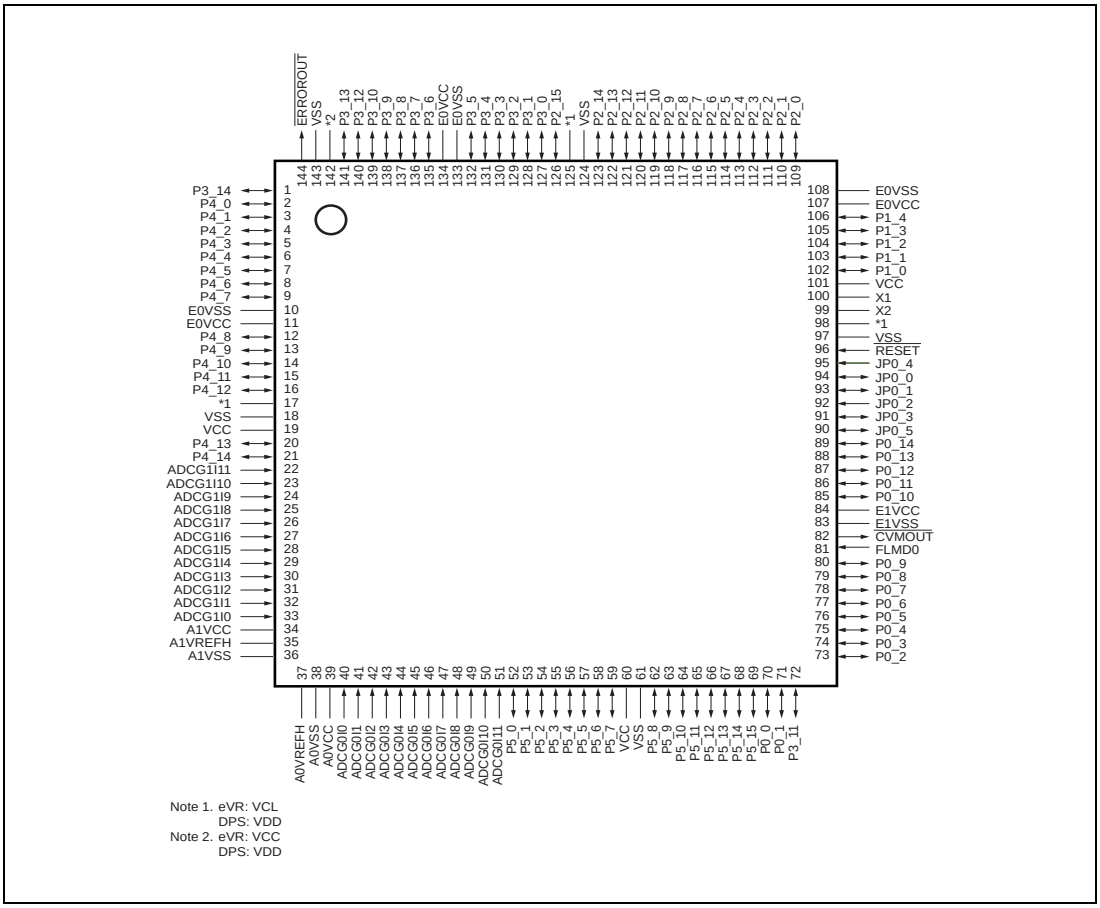


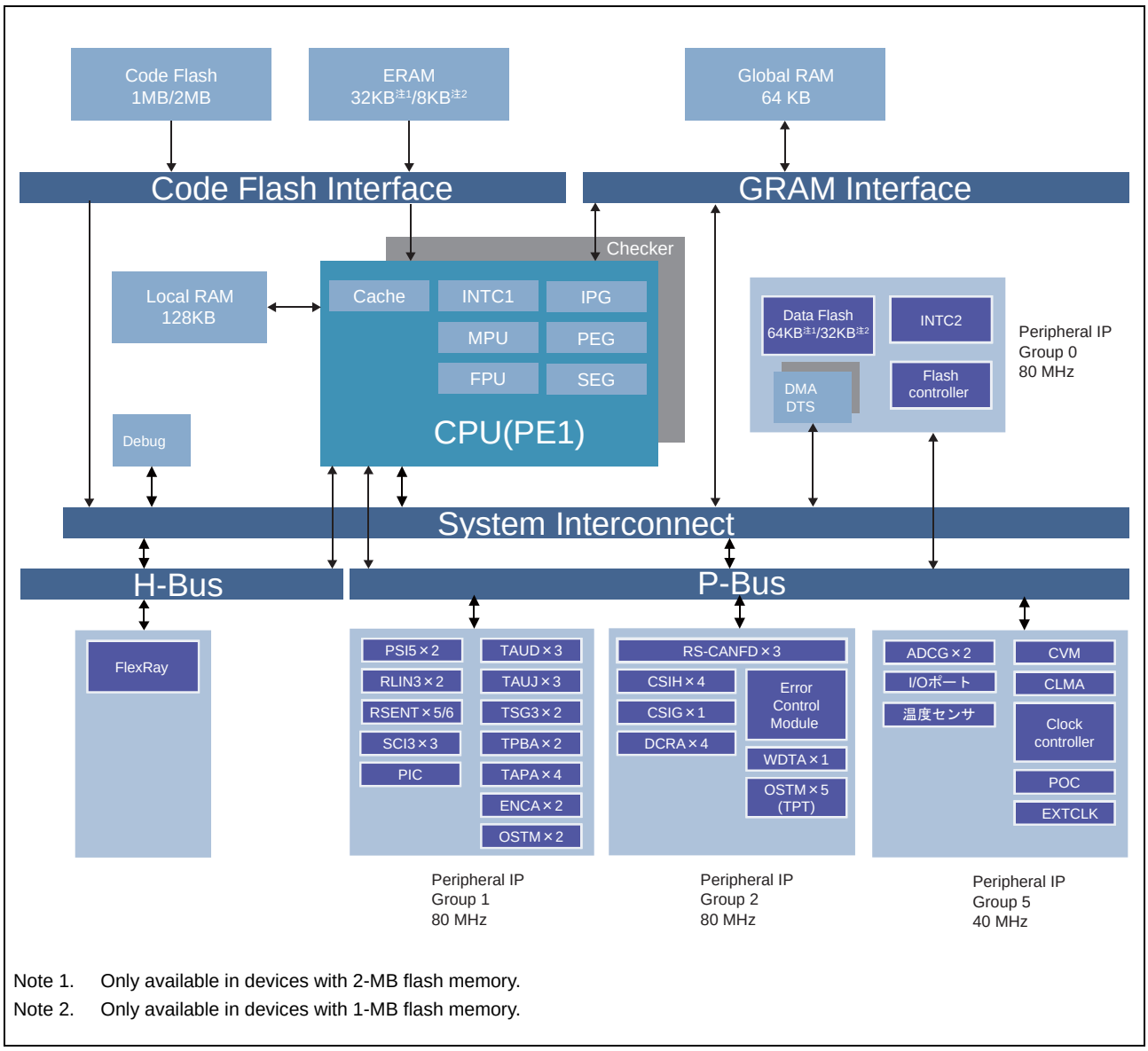
Figure 1.1 Pin Connection Diagram (100 pins)



Note 1. eVR: VCL
DPS: VDD
Note 2. eVR: VCC
DPS: VDD

Figure 1.2 Pin Connection Diagram (144 pins)

1.5 Block Configuration



Note 1. Only available in devices with 2-MB flash memory.
Note 2. Only available in devices with 1-MB flash memory.

Figure 1.3 Internal Block Diagram

Section 2 Pin Functions

2.1 Pin List

2.1.1 Pin List and Function assignment

Table 2.1 shows the pin assignment.

CAUTION

There are restrictions on the combinations of the CSIG, CSIH, SCI3, RLIN3, RSCAN, FlexRay, and RSENT pins that can be used. For details, see the Combinations of Pins and Ports table in each section.

Table 2.1 Pin Assignment (1/5)

Pin Name	Pin Number				Power Domain
	Pkg 100 (eVR)	Pkg 100 (DPS)	Pkg 144 (eVR)	Pkg 144 (DPS)	
P3_14 / CSIH1SI / TAPA0ESO / INTP7 / TPBA1O / EXTCLK0O / NMI / TSG31O7/FLMD1	1	1	1	1	E0VCC
P4_0 / CSIH1SO / TAUJ0I0 / TAUJ0O0 / RLIN30RX / INTP3 / TSG30PTSI0 / ENCA0E0 / FLXA0TXDA / ADCG1CNV0	2	2	2	2	E0VCC
P4_1 / CSIH1SCI / CSIH1SCO / TAUJ0I1 / TAUJ0O1 / RLIN30TX / TSG30PTSI1 / ENCA0E1 / FLXA0TXENA / ADCG1CNV1	3	3	3	3	E0VCC
P4_2 / RSCAN0RX1 / INTP6 / CSIH1RYO / TAUJ0I2 / TAUJ0O2 / SCI30SCI / SCI30SCO / TSG30PTSI2 / ENCA0EC / FLXA0RXDA / INTP11 / ADCG1CNV2	4	4	4	4	E0VCC
P4_3 / CSIH2RYI / RSCAN0TX1 / TAUJ0I3 / TAUJ0O3 / OSTM1O / TSG30CLKI / CSIH1CSS0 / FLXA0RXDB / INTP12 / ADCG1CNV3 / TAUD2I0 / TAUD2O0	5	5	5	5	E0VCC
P4_4 / CSIH2SI / TAPA1ESO / INTP8 / CSIH2CSS7 / TSG31PTSI0 / ENCA1E0 / CSIH1CSS1 / FLXA0STPWT / ADCG1CNV4 / TAUD2I1 / TAUD2O1	6	6	6	6	E0VCC
P4_5 / CSIH2SO / SCI30RX / INTP0 / RSCAN0RX0 / INTP5 / EXTCLK1O / TSG31PTSI1 / ENCA1E1 / CSIH1CSS2 / FLXA0TXDB / TAUD2I2 / TAUD2O2	7	7	7	7	E0VCC
P4_6 / CSIH2SCI / CSIH2SCO / SCI30TX / RSCAN0TX0 / TSG31PTSI2 / ENCA1EC / CSIH1CSS3 / FLXA0TXENB / TAUD2I3 / TAUD2O3	8	8	8	8	E0VCC
P4_7 / RSCAN0RX1 / INTP6 / CSIH2RYO / TAUD1O0 / ENCA0TIN0 / CSIH2CSS0 / TSG31CLKI / CSIH1CSS4 / TAUD2I4 / TAUD2O4	—	—	9	9	E0VCC
E0VSS	9	9	10	10	—
E0VCC	10	10	11	11	—
P4_8 / FLXA0RXDA / INTP11 / TAUD1O1 / ENCA0TIN1 / CSIH2CSS1 / CSIH1SSI/ CSIH1CSS5 / TAUD2I5 / TAUD2O5	—	—	12	12	E0VCC
P4_9 / FLXA0TXDA / TAUD1O2 / ENCA1TIN0 / CSIH2CSS2 / CSIH1RYI / CSIH1CSS6 / TAUD2I6 / TAUD2O6	—	—	13	13	E0VCC
P4_10 / FLXA0TXENA / TAUD1O3 / ENCA1TIN1 / CSIH2CSS3 / CSIH1RYO / CSIH1CSS7 / TAUD2I7 / TAUD2O7	—	—	14	14	E0VCC
P4_11 / FLXA0RXDB / INTP12 / TAUD1O4 / CSIH2CSS4 / TAUJ1I0 / TAUJ1O0 / TAUD2I8 / TAUD2O8	—	—	15	15	E0VCC
P4_12 / FLXA0TXDB / TAUD1O5 / CSIH2CSS5 / TAUJ1I1 / TAUJ1O1 / TAUD2I9 / TAUD2O9	—	—	16	16	E0VCC
VCL	11	—	17	—	—
VDD	—	11	—	17	—
VSS	12	12	18	18	—
VCC	—	—	19	19	—
P4_13 / FLXA0TXENB / TAUD1O6 / $\overline{\text{CSIH2SSI}}$ / TAUJ1I2 / TAUJ1O2 / TAUD2I10 / TAUD2O10	—	—	20	20	E0VCC
P4_14 / FLXA0STPWT / TAUD1O7 / CSIH2CSS6 / TAUJ1I3 / TAUJ1O3 / TAUD2I11 / TAUD2O11	—	—	21	21	E0VCC
ADCG1I11	—	—	22	22	A1VCC
ADCG1I10	—	—	23	23	A1VCC
ADCG1I9	13	13	24	24	A1VCC

Table 2.1 Pin Assignment (2/5)

Pin Name	Pin Number				Power Domain
	Pkg 100 (eVR)	Pkg 100 (DPS)	Pkg 144 (eVR)	Pkg 144 (DPS)	
ADCG1I8	14	14	25	25	A1VCC
ADCG1I7	15	15	26	26	A1VCC
ADCG1I6	16	16	27	27	A1VCC
ADCG1I5	17	17	28	28	A1VCC
ADCG1I4	18	18	29	29	A1VCC
ADCG1I3	19	19	30	30	A1VCC
ADCG1I2	20	20	31	31	A1VCC
ADCG1I1	21	21	32	32	A1VCC
ADCG1I0	22	22	33	33	A1VCC
A1VCC	23	23	34	34	—
A1VREFH	24	24	35	35	—
A1VSS	25	25	36	36	—
A0VREFH	26	26	37	37	—
A0VSS	27	27	38	38	—
A0VCC	28	28	39	39	—
ADCG0I0	29	29	40	40	A0VCC
ADCG0I1	30	30	41	41	A0VCC
ADCG0I2	31	31	42	42	A0VCC
ADCG0I3	32	32	43	43	A0VCC
ADCG0I4	33	33	44	44	A0VCC
ADCG0I5	34	34	45	45	A0VCC
ADCG0I6	35	35	46	46	A0VCC
ADCG0I7	36	36	47	47	A0VCC
ADCG0I8	37	37	48	48	A0VCC
ADCG0I9	—	—	49	49	A0VCC
ADCG0I10	—	—	50	50	A0VCC
ADCG0I11	—	—	51	51	A0VCC
P5_0 / CSIG0SI / TAUD0O0 / TAUD0I1 / TAUD0O1 / CSIH2CSS1 / SCI30RX / INTP0	38	38	52	52	E1VCC
P5_1 / CSIG0SO / TAUD0O2 / TAUD0I3 / ADCG0CNV0 / TAUD0O3 / TAUD0I2 / CSIH2CSS2 / TAUD0I11 / SCI30TX	39	39	53	53	E1VCC
P5_2 / CSIG0SCI / CSIG0SCO / TAUD0O2 / TAUD0I14 / TAUD0O3 / TAUD0I15 / CSIH2CSS0 / SCI30SCI / SCI30SCO	—	—	54	54	E1VCC
P5_3 / TAUD0I7 / TAUD0I6	—	—	55	55	E1VCC
P5_4 / CSIG0SCI / CSIG0SCO / TAUD0O4 / TAUD0I5 / ADCG0CNV1 / TAUD0O5 / TAUD0I4 / CSIH2CSS3 / SCI30SCI / SCI30SCO	40	40	56	56	E1VCC
P5_5 / SENT0RX / SENT0SPCO / TAUD0O6 / TAUD0I7 / ADCG0CNV2 / TAUD0O7 / TAUD0I6 / CSIH2CSS4 / SCI31RX / INTP1 / RSCAN0TX2	41	41	57	57	E1VCC
P5_6 / INTP10 / RSCAN0RX2 / SENT0SPCO / TAUD0O8 / TAUD0I9 / ADCG0CNV3 / TAUD0O9 / TAUD0I8 / CSIH2CSS5 / SCI31TX	42	42	58	58	E1VCC
P5_7 / RSCAN0TX2 / TAUD0O10 / TAUD0I11 / ADCG0CNV4 / TAUD0O11 / TAUD0I10 / CSIH2CSS6 / SCI31SCI / SCI31SCO	—	—	59	59	E1VCC
VCC	43	43	60	60	—
VSS	44	44	61	61	—
P5_8 / SENT1RX / SENT1SPCO / TAUD0O12 / TAUD0I13 / TAUD0O13 / TAUD0I12 / CSIH2CSS7 / SCI32RX / INTP2	—	—	62	62	E1VCC

Table 2.1 Pin Assignment (3/5)

Pin Name	Pin Number				Power Domain
	Pkg 100 (eVR)	Pkg 100 (DPS)	Pkg 144 (eVR)	Pkg 144 (DPS)	
P5_9 / TAUD0I14 / SENT1SPCO / TAUD0O14 / TAUD0I15 / TAUD0O15 / PSI51DIN / CSIH2SI / SCI32TX	45	45	63	63	E1VCC
P5_10 / RLIN30RX / INTP3 / TAUD0O12 / SENT1RX / SENT1SPCO / ADCGTRG0 / ADCG0CNV0 / TAUD0I12 / PSI51DOUT / SCI32SCI / SCI32SCO	46	46	64	64	E1VCC
P5_11 / RLIN30TX / SENT3RX / SENT3SPCO / TAUD1O10 / $\overline{\text{CSIH2SSI}}$	—	—	65	65	E1VCC
P5_12 / RLIN31RX / INTP4 / SENT2RX / SENT2SPCO / TAUD1O11 /CSIH2RYI	—	—	66	66	E1VCC
P5_13 / RLIN31TX / SENT2SPCO / TAUD1O12 / TAUD0I13 / TAUD0I12 / CSIH2RYO	—	—	67	67	E1VCC
P5_14 / TAUJ0I0 / TAUJ0O0 / SENT3RX / SENT3SPCO / TAUD1O13 / ADCGTRG1 / ADCG0CNV1 / PSI50DIN / CSIH2SO / RLIN30RX / INTP3	47	47	68	68	E1VCC
P5_15 / RLIN31RX / INTP4 / SENT3SPCO / CSIH2SCI / CSIH2SCO / RLIN30TX	—	—	69	69	E1VCC
P0_0 / TAUJ0I1 / TAUJ0O1 / TAUD0I13 / SENT3SPCO / TAUD1O14 / ADCG0CNV2 / TSG31CLKI / PSI50DOUT / RLIN30TX	48	48	70	70	E1VCC
P0_1 / TAUJ0I2 / TAUJ0O2 / SENT4RX / SENT4SPCO / TAUD1O15 / ADCG0CNV3 / TAUD0O10 / RLIN31RX / INTP4	49	49	71	71	E1VCC
P3_11 / TAUJ0I3 / TAUJ0O3 / SENT4SPCO / ADCG0CNV4 / $\overline{\text{ERROROUT\_C}}$ / RLIN31TX	50	50	72	72	E1VCC
P0_2 / SCI30RX / INTP0 / TAPA1ESO / INTP8 / TAUD2I0 / ADCG0CNV0 / TAUD2O0 / SCI32RX / INTP2 / TSG31O0 / SENT5RX / SENT5SPCO	51	51	73	73	E1VCC
P0_3 / SCI30TX / TAUD1O8 / TAUD2I1 / ADCG0CNV1 / TAUD2O1 / TSG31O1 / SENT5SPCO	—	—	74	74	E1VCC
P0_4 / SCI30SCI / SCI30SCO / TAUD1O9 / TAUD2I2 / ADCG0CNV2 / TAUD2O2 / TSG31O2 / SENT4SPCO	—	—	75	75	E1VCC
P0_5 / TAUJ1I0 / TAUJ1O0 / TAUD1O10 / TAUD2I3 / ADCG0CNV3 / TAUD2O3 / TSG31O3 / SENT3SPCO	—	—	76	76	E1VCC
P0_6 / TAUJ1I1 / TAUJ1O1 / TAUD1O11 / TAUD2I4 / TAUD2O4 / TSG31O4 / SENT2SPCO	—	—	77	77	E1VCC
P0_7 / TAUJ1I2 / TAUJ1O2 / TAUD1O12 / TAUD2I5 / ADCGTRG0 / TAUD2O5 / TSG31O5 / SENT1SPCO	—	—	78	78	E1VCC
P0_8 / TAUJ1I3 / TAUJ1O3 / TAUD1O13 / TAUD2I6 / ADCGTRG1 / TAUD2O6 / TSG31O6 / SENT0SPCO	—	—	79	79	E1VCC
P0_9 / ADCG1CNV1 / TAUD1O14 / TAUD2I7 / ADCG0CNV4 / TAUD2O7 / TSG31O7	—	—	80	80	E1VCC
FLMD0	52	52	81	81	E1VCC
$\overline{\text{CVMOUT}}$	53	53	82	82	E1VCC
E1VSS	54	54	83	83	—
E1VCC	55	55	84	84	—
P0_10 / $\overline{\text{RESETOUT}}$ / ADCG1CNV0 / $\overline{\text{EVTO}}$	56	56	85	85	E1VCC
P0_11 / ADCG1CNV2 / TSG31PTSI0 / ENCA1E0	—	—	86	86	E1VCC
P0_12 / ADCG1CNV3 / TSG31PTSI1 / ENCA1E1	—	—	87	87	E1VCC
P0_13 / OSTM0O / TAUD1O15 / TAUD2I7 / INTP9 / TAUD2O7/ $\overline{\text{EVTI}}$ / TSG31PTSI2 / ENCA1EC / SCI31SCI / SCI31SCO	57	57	88	88	E1VCC
P0_14 / ADCG1CNV4	—	—	89	89	E1VCC
JP0_5 / $\overline{\text{DCUTRDY}}$ / LPDCLKOUT	58	58	90	90	E1VCC
JP0_3 / DCUTMS	59	59	91	91	E1VCC
JP0_2 / FLSCI3SCKI (FPCK) / DCUTCK / LPDCLK	60	60	92	92	E1VCC
JP0_1 / FLSCI3TXD (FPDT) / DCUTDO / LPDO	61	61	93	93	E1VCC
JP0_0 / FLSCI3RXD (FPDR) / FLSCI3TXD (FPDT) / DCUTDI / LPDI	62	62	94	94	E1VCC

Table 2.1 Pin Assignment (4/5)

Pin Name	Pin Number				Power Domain
	Pkg 100 (eVR)	Pkg 100 (DPS)	Pkg 144 (eVR)	Pkg 144 (DPS)	
JP0_4 / $\overline{\text{DCUTRST}}$	63	63	95	95	VCC
$\overline{\text{RESET}}$	64	64	96	96	VCC
VSS	65	65	97	97	—
VDD	—	66	—	98	—
VCL	66	—	98	—	—
X2	67	67	99	99	VCC
X1	68	68	100	100	VCC
VCC	69	69	101	101	—
P1_0 / RLIN30TX / CSIH3RYO	—	—	102	102	E0VCC
P1_1 / TAUJ2I0 / TAUJ2O0 / TAUJ1I0 / TAUJ1O0 / TAUD2I12 / TAUD2O12 / RLIN30RX / INTP3 / CSIH2CSS0 / TAUD0I6 / CSIH3RYI	70	70	103	103	E0VCC
P1_2 / TAUJ2I1 / TAUJ2O1 / TAUJ1I1 / TAUJ1O1 / TAUD2I13 / TAUD2O13 / CSIH2SI / TAUD0I8 / CSIH3SI	71	71	104	104	E0VCC
P1_3 / TAUJ2I2 / TAUJ2O2 / TAUJ1I2 / TAUJ1O2 / TAUD2I14 / TAUD2O14 / CSIH2SO / TAUD0I10 / CSIH3SO	72	72	105	105	E0VCC
P1_4 / TAUJ2I3 / TAUJ2O3 / TAUJ1I3 / TAUJ1O3 / TAUD2I15 / TAUD2O15 / CSIH2SCI / CSIH2SCO / CSIH3SCI / CSIH3SCO	73	73	106	106	E0VCC
E0VCC	74	74	107	107	—
E0VSS	75	75	108	108	—
P2_0 / RSCAN0RX0 / INTP5 / CSIH2SI / TAUD2I11 / TAUD2O11 / CSIH3CSS6	76	76	109	109	E0VCC
P2_1 / RSCAN0TX0 / CSIH2SO / TAUD2I12 / TAUD2O12 / CSIH3CSS7 / TSG30O7	77	77	110	110	E0VCC
P2_2 / RSCAN0RX1 / INTP6 / CSIH2SCI / CSIH2SCO / TAUD2I13 / TAUD2O13 / TPBA0O / TSG30O0 / CSIH0CSS5	78	78	111	111	E0VCC
P2_3 / RSCAN0TX1 / CSIH2RYI / CSIH2CSS0 / TAUD2I14 / TAUD2O14 / TPBA1O / TSG30O1	79	79	112	112	E0VCC
P2_4 / CSIH2RYO / CSIH0CSS2 / RLIN31TX / TAUJ1I3 / TAUJ1O3 / CSIH0SI / TAUD2I11 / TAUD2O11	80	80	113	113	E0VCC
P2_5 / SCI30RX / INTP0 / CSIH0CSS3 / RLIN31RX / INTP4 / CSIH3SO / TSG30O2 / CSIH0SO	81	81	114	114	E0VCC
P2_6 / SCI30TX / OSTM1O / CSIH0SCI / CSIH0SCO / CSIH3SI / CSIH0CSS4 / TSG30O3 / TAUD1I0 / TAUD1O0	82	82	115	115	E0VCC
P2_7 / SCI30SCI / SCI30SCO / CSIH0CSS5 / CSIH1SI / CSIH3SCI / CSIH3SCO / TSG30O4 / TAUD1I1 / TAUD1O1	83	83	116	116	E0VCC
P2_8 / SCI31RX / INTP1 / CSIH3RYO / CSIH0CSS6 / CSIH1SO / CSIH3RYI / CSIH3CSS0 / TSG30O5 / TAUD1I2 / TAUD1O2	84	84	117	117	E0VCC
P2_9 / SCI31TX / CSIH0CSS7 / CSIH1SCI / CSIH1SCO / CSIH3CSS1 / TSG30O6 / TAUD1I3 / TAUD1O3	85	85	118	118	E0VCC
P2_10 / SENT5RX / SENT5SPCO / TAUD2I10 / TAUD2O10 / CSIH0RYI / CSIH0CSS6 / OSTM1O	—	—	119	119	E0VCC
P2_11 / TAUD1I0 / SENT5SPCO / TAUD1O0 / TAUD1I1 / TAUD1O1 / CSIH0CSS5 / CSIH1RYI / CSIH0RYO	—	—	120	120	E0VCC
P2_12 / TAUD1I2 / TAUD1O2 / TAUD1I3 / TAUD1O3 / CSIH0CSS4 / CSIH0SO	—	—	121	121	E0VCC
P2_13 / TAUD1I4 / TAUD1O4 / TAUD1I5 / TAUD1O5 / CSIH0CSS3 / CSIH1RYO	—	—	122	122	E0VCC
P2_14 / TAUD1I6 / TAUD1O6 / TAUD1I7 / TAUD1O7 / CSIH0CSS2	—	—	123	123	E0VCC
VSS	—	—	124	124	—
VCL	—	—	125	—	—
VDD	—	—	—	125	—
P2_15 / TAUD1I8 / TAUD1O8 / TAUD1I9 / TAUD1O9 / CSIH0RYI	—	—	126	126	E0VCC

Table 2.1 Pin Assignment (5/5)

Pin Name	Pin Number				Power Domain
	Pkg 100 (eVR)	Pkg 100 (DPS)	Pkg 144 (eVR)	Pkg 144 (DPS)	
P3_0 / TAUD1I10 / TAUD1O10 / TAUD1I11 / TAUD1O11 / CSIH0SO / CSIG0SI	—	—	127	127	E0VCC
P3_1 / TAUD1I12 / TAUD1O12 / TAUD1I13 / TAUD1O13 / CSIH0SCI / CSIH0SCO / CSIG0SO	—	—	128	128	E0VCC
P3_2 / TAUD1I14 / TAUD1O14 / TAUD1I15 / TAUD1O15 / CSIH0SI / CSIH0CSS7 / CSIG0SCI / CSIG0SCO	—	—	129	129	E0VCC
P3_3 / CSIH0RYI / SCI32TX / TAUD1I0 / CSIH2CSS1 / $\overline{\text{CSIH3SSI}}$ / CSIH3CSS4 / TAUD1O0 / TAUD1O1	86	86	130	130	E0VCC
P3_4 / SCI32RX / INTP2 / TAUD1I2 / CSIH2CSS2 / RLIN30RX / INTP3 / CSIG0RYO*1 / CSIH3CSS3 / TAUD1O2 / TAUD1O3	87	87	131	131	E0VCC
P3_5 / SCI31SCI / SCI31SCO / TAUD0I0 / CSIH2CSS3 / CSIG0RYI *1/ RLIN30TX / CSIH3CSS2 / TAUD0O0 / TAUD0O1	88	88	132	132	E0VCC
E0VSS	89	89	133	133	—
E0VCC	90	90	134	134	—
P3_6 / CSIH0SI / TSG31O0 / TAUD0O2 / CSIH3RYI / CSIH2CSS4 / TAUD0O3	91	91	135	135	E0VCC
P3_7 / CSIH0SO / TSG31O1 / RSCAN0RX0 / INTP5 / SCI30RX / INTP0 / CSIH2RYI / CSIH2CSS5 / TAUD0O5	92	92	136	136	E0VCC
P3_8 / CSIH0SCI / CSIH0SCO / TSG31O2 / RSCAN0TX0 / TPBA1O / $\overline{\text{CSIH0SSI}}$ / CSIH2CSS6 / TAUD0O7	93	93	137	137	E0VCC
P3_9 / SCI32SCI / SCI32SCO / TSG31O3 / CSIH3CSS5 / CSIH0RYI / CSIH2CSS7 / TAUD0O9	94	94	138	138	E0VCC
P3_10 / TSG31O4 / TAUD1I6 / TAUD0O11	95	95	139	139	E0VCC
P3_12 / CSIH1RYO / TSG31O5 / RSCAN0RX1 / INTP6 / SCI30TX / TAUD1I8 / CSIH0CSS0 / TAUD0O13	96	96	140	140	E0VCC
P3_13 / CSIH1RYI / TSG31O6 / RSCAN0TX1 / SCI30SCI / SCI30SCO / TAUD1I10 / CSIH0CSS1 / TAUD0O15	97	97	141	141	E0VCC
VDD	—	98	—	142	—
VCC	98	—	142	—	—
VSS	99	99	143	143	—
$\overline{\text{ERROROUT}}$	100	100	144	144	E0VCC

Note 1. Only in 144-pin products.

2.1.2 Pin Function name

Table 2.2 lists functions of each pin. “Port number” in the table indicates that the function is supported, while “—” indicates that the function is not supported. Do not use the pin function that is not supported.

Table 2.2 Pin Function (1/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
NMI	NMI	I	External non-maskable interrupt input	P3_14	P3_14	P3_14	P3_14
INTP	INTP0	I	External interrupt input 0	P3_7/ P2_5/ P0_2/ P5_0/ P4_5	P3_7/ P2_5/ P0_2/ P5_0/ P4_5	P3_7/ P2_5/ P0_2/ P5_0/ P4_5	P3_7/ P2_5/ P0_2/ P5_0/ P4_5
	INTP1	I	External interrupt input 1	P2_8/ P5_5	P2_8/ P5_5	P2_8/ P5_5	P2_8/ P5_5
	INTP2	I	External interrupt input 2	P0_2/ P3_4	P0_2/ P3_4	P0_2/ P3_4/ P5_8	P0_2/ P3_4/ P5_8
	INTP3	I	External interrupt input 3	P3_4/ P1_1/ P5_14/ P5_10/ P4_0	P3_4/ P1_1/ P5_14/ P5_10/ P4_0	P3_4/ P1_1/ P5_14/ P5_10/ P4_0	P3_4/ P1_1/ P5_14/ P5_10/ P4_0
	INTP4	I	External interrupt input 4	P2_5/ P0_1	P2_5/ P0_1	P2_5/ P0_1/ P5_15/ P5_12	P2_5/ P0_1/ P5_15/ P5_12
	INTP5	I	External interrupt input 5	P3_7/ P2_0/ P4_5	P3_7/ P2_0/ P4_5	P3_7/ P2_0/ P4_5	P3_7/ P2_0/ P4_5
	INTP6	I	External interrupt input 6	P3_12/ P2_2/ P4_2	P3_12/ P2_2/ P4_2	P3_12/ P2_2/ P4_7/ P4_2	P3_12/ P2_2/ P4_7/ P4_2
	INTP7	I	External interrupt input 7	P3_14	P3_14	P3_14	P3_14
	INTP8	I	External interrupt input 8	P0_2/ P4_4	P0_2/ P4_4	P0_2/ P4_4	P0_2/ P4_4
	INTP9	I	External interrupt input 9	P0_13	P0_13	P0_13	P0_13
	INTP10	I	External interrupt input 10	P5_6	P5_6	P5_6	P5_6
	INTP11	I	External interrupt input 11	P4_2	P4_2	P4_8/ P4_2	P4_8/ P4_2
	INTP12	I	External interrupt input 12	P4_3	P4_3	P4_11/ P4_3	P4_11/ P4_3
TAUD0	TAUD0I0	I	TAUD0 channel input 0	P3_5	P3_5	P3_5	P3_5
	TAUD0I1	I	TAUD0 channel input 1	P5_0	P5_0	P5_0	P5_0
	TAUD0I2	I	TAUD0 channel input 2	P5_1	P5_1	P5_1	P5_1
	TAUD0I3	I	TAUD0 channel input 3	P5_1	P5_1	P5_1	P5_1
	TAUD0I4	I	TAUD0 channel input 4	P5_4	P5_4	P5_4	P5_4
	TAUD0I5	I	TAUD0 channel input 5	P5_4	P5_4	P5_4	P5_4

Table 2.2 Pin Function (2/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
TAUD0	TAUD0I6	I	TAUD0 channel input 6	P1_1/ P5_5	P1_1/ P5_5	P1_1/ P5_5/ P5_3	P1_1/ P5_5/ P5_3
	TAUD0I7	I	TAUD0 channel input 7	P5_5	P5_5	P5_5/ P5_3	P5_5/ P5_3
	TAUD0I8	I	TAUD0 channel input 8	P1_2/ P5_6	P1_2/ P5_6	P1_2/ P5_6	P1_2/ P5_6
	TAUD0I9	I	TAUD0 channel input 9	P5_6	P5_6	P5_6	P5_6
	TAUD0I10	I	TAUD0 channel input 10	P1_3	P1_3	P1_3/ P5_7	P1_3/ P5_7
	TAUD0I11	I	TAUD0 channel input 11	P5_1	P5_1	P5_1/ P5_7	P5_1/ P5_7
	TAUD0I12	I	TAUD0 channel input 12	P5_10	P5_10	P5_13/ P5_10/ P5_8	P5_13/ P5_10/ P5_8
	TAUD0I13	I	TAUD0 channel input 13	P0_0	P0_0	P5_13/ P5_8/ P0_0	P5_13/ P5_8/ P0_0
	TAUD0I14	I	TAUD0 channel input 14	P5_9	P5_9	P5_9/ P5_2	P5_9/ P5_2
	TAUD0I15	I	TAUD0 channel input 15	P5_9	P5_9	P5_9/ P5_2	P5_9/ P5_2
	TAUD0O0	O	TAUD0 channel output 0	P3_5/ P5_0	P3_5/ P5_0	P3_5/ P5_0	P3_5/ P5_0
	TAUD0O1	O	TAUD0 channel output 1	P3_5/ P5_0	P3_5/ P5_0	P3_5/ P5_0	P3_5/ P5_0
	TAUD0O2	O	TAUD0 channel output 2	P3_6/ P5_1	P3_6/ P5_1	P3_6/ P5_2/ P5_1	P3_6/ P5_2/ P5_1
	TAUD0O3	O	TAUD0 channel output 3	P3_6/ P5_1	P3_6/ P5_1	P3_6/ P5_2/ P5_1	P3_6/ P5_2/ P5_1
	TAUD0O4	O	TAUD0 channel output 4	P5_4	P5_4	P5_4	P5_4
	TAUD0O5	O	TAUD0 channel output 5	P3_7/ P5_4	P3_7/ P5_4	P3_7/ P5_4	P3_7/ P5_4
	TAUD0O6	O	TAUD0 channel output 6	P5_5	P5_5	P5_5	P5_5
	TAUD0O7	O	TAUD0 channel output 7	P3_8/ P5_5	P3_8/ P5_5	P3_8/ P5_5	P3_8/ P5_5
	TAUD0O8	O	TAUD0 channel output 8	P5_6	P5_6	P5_6	P5_6
	TAUD0O9	O	TAUD0 channel output 9	P3_9/ P5_6	P3_9/ P5_6	P3_9/ P5_6	P3_9/ P5_6
	TAUD0O10	O	TAUD0 channel output 10	P0_1	P0_1	P0_1/ P5_7	P0_1/ P5_7
	TAUD0O11	O	TAUD0 channel output 11	P3_10	P3_10	P3_10/ P5_7	P3_10/ P5_7
	TAUD0O12	O	TAUD0 channel output 12	P5_10	P5_10	P5_8/ P5_10	P5_8/ P5_10
	TAUD0O13	O	TAUD0 channel output 13	P3_12	P3_12	P3_12/ P5_8	P3_12/ P5_8
	TAUD0O14	O	TAUD0 channel output 14	P5_9	P5_9	P5_9	P5_9
	TAUD0O15	O	TAUD0 channel output 15	P3_13/ P5_9	P3_13/ P5_9	P3_13/ P5_9	P3_13/ P5_9

Table 2.2 Pin Function (3/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
TAUD1	TAUD1I0	I	TAUD1 channel input 0	P3_3/ P2_6	P3_3/ P2_6	P3_3/ P2_11/ P2_6	P3_3/ P2_11/ P2_6
	TAUD1I1	I	TAUD1 channel input 1	P2_7	P2_7	P2_11/ P2_7	P2_11/ P2_7
	TAUD1I2	I	TAUD1 channel input 2	P3_4/ P2_8	P3_4/ P2_8	P3_4/ P2_12/ P2_8	P3_4/ P2_12/ P2_8
	TAUD1I3	I	TAUD1 channel input 3	P2_9	P2_9	P2_12/ P2_9	P2_12/ P2_9
	TAUD1I4	I	TAUD1 channel input 4	—	—	P2_13	P2_13
	TAUD1I5	I	TAUD1 channel input 5	—	—	P2_13	P2_13
	TAUD1I6	I	TAUD1 channel input 6	P3_10	P3_10	P3_10/ P2_14	P3_10/ P2_14
	TAUD1I7	I	TAUD1 channel input 7	—	—	P2_14	P2_14
	TAUD1I8	I	TAUD1 channel input 8	P3_12	P3_12	P3_12/ P2_15	P3_12/ P2_15
	TAUD1I9	I	TAUD1 channel input 9	—	—	P2_15	P2_15
	TAUD1I10	I	TAUD1 channel input 10	P3_13	P3_13	P3_13/ P3_0	P3_13/ P3_0
	TAUD1I11	I	TAUD1 channel input 11	—	—	P3_0	P3_0
	TAUD1I12	I	TAUD1 channel input 12	—	—	P3_1	P3_1
	TAUD1I13	I	TAUD1 channel input 13	—	—	P3_1	P3_1
	TAUD1I14	I	TAUD1 channel input 14	—	—	P3_2	P3_2
	TAUD1I15	I	TAUD1 channel input 15	—	—	P3_2	P3_2
	TAUD1O0	O	TAUD1 channel output 0	P3_3/ P2_6	P3_3/ P2_6	P3_3/ P2_11/ P2_6/ P4_7	P3_3/ P2_11/ P2_6/ P4_7
	TAUD1O1	O	TAUD1 channel output 1	P3_3/ P2_7	P3_3/ P2_7	P3_3/ P2_11/ P2_7/ P4_8	P3_3/ P2_11/ P2_7/ P4_8
	TAUD1O2	O	TAUD1 channel output 2	P3_4/ P2_8	P3_4/ P2_8	P3_4/ P2_12/ P2_8/ P4_9	P3_4/ P2_12/ P2_8/ P4_9
	TAUD1O3	O	TAUD1 channel output 3	P3_4/ P2_9	P3_4/ P2_9	P3_4/ P2_12/ P2_9/ P4_10	P3_4/ P2_12/ P2_9/ P4_10
	TAUD1O4	O	TAUD1 channel output 4	—	—	P2_13/ P4_11	P2_13/ P4_11
	TAUD1O5	O	TAUD1 channel output 5	—	—	P2_13/ P4_12	P2_13/ P4_12
	TAUD1O6	O	TAUD1 channel output 6	—	—	P2_14/ P4_13	P2_14/ P4_13
	TAUD1O7	O	TAUD1 channel output 7	—	—	P2_14/ P4_14	P2_14/ P4_14
	TAUD1O8	O	TAUD1 channel output 8	—	—	P2_15/ P0_3	P2_15/ P0_3
	TAUD1O9	O	TAUD1 channel output 9	—	—	P2_15/ P0_4	P2_15/ P0_4
	TAUD1O10	O	TAUD1 channel output 10	—	—	P3_0/ P0_5/ P5_11	P3_0/ P0_5/ P5_11
	TAUD1O11	O	TAUD1 channel output 11	—	—	P3_0/ P0_6/ P5_12	P3_0/ P0_6/ P5_12

Table 2.2 Pin Function (4/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
TAUD1	TAUD1O12	O	TAUD1 channel output 12	—	—	P3_1/ P0_7/ P5_13	P3_1/ P0_7/ P5_13
	TAUD1O13	O	TAUD1 channel output 13	P5_14	P5_14	P3_1/ P0_8/ P5_14	P3_1/ P0_8/ P5_14
	TAUD1O14	O	TAUD1 channel output 14	P0_0	P0_0	P3_2/ P0_9/ P0_0	P3_2/ P0_9/ P0_0
	TAUD1O15	O	TAUD1 channel output 15	P0_13/ P0_1	P0_13/ P0_1	P3_2/ P0_13/ P0_1	P3_2/ P0_13/ P0_1
TAUD2	TAUD2I0	I	TAUD2 channel input 0	P0_2/ P4_3	P0_2/ P4_3	P0_2/ P4_3	P0_2/ P4_3
	TAUD2I1	I	TAUD2 channel input 1	P4_4	P4_4	P0_3/ P4_4	P0_3/ P4_4
	TAUD2I2	I	TAUD2 channel input 2	P4_5	P4_5	P0_4/ P4_5	P0_4/ P4_5
	TAUD2I3	I	TAUD2 channel input 3	P4_6	P4_6	P0_5/ P4_6	P0_5/ P4_6
	TAUD2I4	I	TAUD2 channel input 4	—	—	P0_6/ P4_7	P0_6/ P4_7
	TAUD2I5	I	TAUD2 channel input 5	—	—	P0_7/ P4_8	P0_7/ P4_8
	TAUD2I6	I	TAUD2 channel input 6	—	—	P0_8/ P4_9	P0_8/ P4_9
	TAUD2I7	I	TAUD2 channel input 7	P0_13	P0_13	P0_13/ P0_9/ P4_10	P0_13/ P0_9/ P4_10
	TAUD2I8	I	TAUD2 channel input 8	—	—	P4_11	P4_11
	TAUD2I9	I	TAUD2 channel input 9	—	—	P4_12	P4_12
	TAUD2I10	I	TAUD2 channel input 10	—	—	P2_10/ P4_13	P2_10/ P4_13
	TAUD2I11	I	TAUD2 channel input 11	P2_4/ P2_0	P2_4/ P2_0	P2_4/ P2_0/ P4_14	P2_4/ P2_0/ P4_14
	TAUD2I12	I	TAUD2 channel input 12	P2_1/ P1_1	P2_1/ P1_1	P2_1/ P1_1	P2_1/ P1_1
	TAUD2I13	I	TAUD2 channel input 13	P2_2/ P1_2	P2_2/ P1_2	P2_2/ P1_2	P2_2/ P1_2
	TAUD2I14	I	TAUD2 channel input 14	P2_3/ P1_3	P2_3/ P1_3	P2_3/ P1_3	P2_3/ P1_3
	TAUD2I15	I	TAUD2 channel input 15	P1_4	P1_4	P1_4	P1_4
	TAUD2O0	O	TAUD2 channel output 0	P0_2/ P4_3	P0_2/ P4_3	P0_2/ P4_3	P0_2/ P4_3
	TAUD2O1	O	TAUD2 channel output 1	P4_4	P4_4	P0_3/ P4_4	P0_3/ P4_4
	TAUD2O2	O	TAUD2 channel output 2	P4_5	P4_5	P0_4/ P4_5	P0_4/ P4_5
	TAUD2O3	O	TAUD2 channel output 3	P4_6	P4_6	P0_5/ P4_6	P0_5/ P4_6
	TAUD2O4	O	TAUD2 channel output 4	—	—	P0_6/ P4_7	P0_6/ P4_7
	TAUD2O5	O	TAUD2 channel output 5	—	—	P0_7/ P4_8	P0_7/ P4_8
	TAUD2O6	O	TAUD2 channel output 6	—	—	P0_8/ P4_9	P0_8/ P4_9

Table 2.2 Pin Function (5/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
TAUD2	TAUD2O7	O	TAUD2 channel output 7	P0_13	P0_13	P0_13/ P0_9/ P4_10	P0_13/ P0_9/ P4_10
	TAUD2O8	O	TAUD2 channel output 8	—	—	P4_11	P4_11
	TAUD2O9	O	TAUD2 channel output 9	—	—	P4_12	P4_12
	TAUD2O10	O	TAUD2 channel output 10	—	—	P2_10/ P4_13	P2_10/ P4_13
	TAUD2O11	O	TAUD2 channel output 11	P2_4/ P2_0	P2_4/ P2_0	P2_4/ P2_0/ P4_14	P2_4/ P2_0/ P4_14
	TAUD2O12	O	TAUD2 channel output 12	P2_1/ P1_1	P2_1/ P1_1	P2_1/ P1_1	P2_1/ P1_1
	TAUD2O13	O	TAUD2 channel output 13	P2_2/ P1_2	P2_2/ P1_2	P2_2/ P1_2	P2_2/ P1_2
	TAUD2O14	O	TAUD2 channel output 14	P2_3/ P1_3	P2_3/ P1_3	P2_3/ P1_3	P2_3/ P1_3
	TAUD2O15	O	TAUD2 channel output 15	P1_4	P1_4	P1_4	P1_4
TAUJ0	TAUJ0I0	I	TAUJ0 channel input 0	P5_14/ P4_0	P5_14/ P4_0	P5_14/ P4_0	P5_14/ P4_0
	TAUJ0I1	I	TAUJ0 channel input 1	P0_0/ P4_1	P0_0/ P4_1	P0_0/ P4_1	P0_0/ P4_1
	TAUJ0I2	I	TAUJ0 channel input 2	P0_1/ P4_2	P0_1/ P4_2	P0_1/ P4_2	P0_1/ P4_2
	TAUJ0I3	I	TAUJ0 channel input 3	P3_11/ P4_3	P3_11/ P4_3	P3_11/ P4_3	P3_11/ P4_3
	TAUJ0O0	O	TAUJ0 channel output 0	P5_14/ P4_0	P5_14/ P4_0	P5_14/ P4_0	P5_14/ P4_0
	TAUJ0O1	O	TAUJ0 channel output 1	P0_0/ P4_1	P0_0/ P4_1	P0_0/ P4_1	P0_0/ P4_1
	TAUJ0O2	O	TAUJ0 channel output 2	P0_1/ P4_2	P0_1/ P4_2	P0_1/ P4_2	P0_1/ P4_2
	TAUJ0O3	O	TAUJ0 channel output 3	P3_11/ P4_3	P3_11/ P4_3	P3_11/ P4_3	P3_11/ P4_3
TAUJ1	TAUJ1I0	I	TAUJ1 channel input 0	P1_1	P1_1	P1_1/ P0_5/ P4_11	P1_1/ P0_5/ P4_11
	TAUJ1I1	I	TAUJ1 channel input 1	P1_2	P1_2	P1_2/ P0_6/ P4_12	P1_2/ P0_6/ P4_12
	TAUJ1I2	I	TAUJ1 channel input 2	P1_3	P1_3	P1_3/ P0_7/ P4_13	P1_3/ P0_7/ P4_13
	TAUJ1I3	I	TAUJ1 channel input 3	P2_4/ P1_4	P2_4/ P1_4	P2_4/ P1_4/ P0_8/ P4_14	P2_4/ P1_4/ P0_8/ P4_14
	TAUJ1O0	O	TAUJ1 channel output 0	P1_1	P1_1	P1_1/ P0_5/ P4_11	P1_1/ P0_5/ P4_11
	TAUJ1O1	O	TAUJ1 channel output 1	P1_2	P1_2	P1_2/ P0_6/ P4_12	P1_2/ P0_6/ P4_12
	TAUJ1O2	O	TAUJ1 channel output 2	P1_3	P1_3	P1_3/ P0_7/ P4_13	P1_3/ P0_7/ P4_13
	TAUJ1O3	O	TAUJ1 channel output 3	P2_4/ P1_4	P2_4/ P1_4	P2_4/ P1_4/ P0_8/ P4_14	P2_4/ P1_4/ P0_8/ P4_14

Table 2.2 Pin Function (6/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
TAUJ2	TAUJ2I0	I	TAUJ2 channel input 0	P1_1	P1_1	P1_1	P1_1
	TAUJ2I1	I	TAUJ2 channel input 1	P1_2	P1_2	P1_2	P1_2
	TAUJ2I2	I	TAUJ2 channel input 2	P1_3	P1_3	P1_3	P1_3
	TAUJ2I3	I	TAUJ2 channel input 3	P1_4	P1_4	P1_4	P1_4
	TAUJ2O0	O	TAUJ2 channel output 0	P1_1	P1_1	P1_1	P1_1
	TAUJ2O1	O	TAUJ2 channel output 1	P1_2	P1_2	P1_2	P1_2
	TAUJ2O2	O	TAUJ2 channel output 2	P1_3	P1_3	P1_3	P1_3
	TAUJ2O3	O	TAUJ2 channel output 3	P1_4	P1_4	P1_4	P1_4
TSG30	TSG30O0	O	TSG30 timer up / down status output	P2_2	P2_2	P2_2	P2_2
	TSG30O1	O	TSG30 PWM output 1	P2_3	P2_3	P2_3	P2_3
	TSG30O2	O	TSG30 PWM output 2	P2_5	P2_5	P2_5	P2_5
	TSG30O3	O	TSG30 PWM output 3	P2_6	P2_6	P2_6	P2_6
	TSG30O4	O	TSG30 PWM output 4	P2_7	P2_7	P2_7	P2_7
	TSG30O5	O	TSG30 PWM output 5	P2_8	P2_8	P2_8	P2_8
	TSG30O6	O	TSG30 PWM output 6	P2_9	P2_9	P2_9	P2_9
	TSG30O7	O	TSG30 AD trigger diagnostic output	P2_1	P2_1	P2_1	P2_1
	TSG30PTSI0	I	TSG30 hall sensor input 0	P4_0	P4_0	P4_0	P4_0
	TSG30PTSI1	I	TSG30 hall sensor input 1	P4_1	P4_1	P4_1	P4_1
	TSG30PTSI2	I	TSG30 hall sensor input 2	P4_2	P4_2	P4_2	P4_2
	TSG30CLKI	I	TSG30 external clock input enable	P4_3	P4_3	P4_3	P4_3
TSG31	TSG31O0	O	TSG31 timer up / down status output	P0_2/ P3_6	P0_2/ P3_6	P0_2/ P3_6	P0_2/ P3_6
	TSG31O1	O	TSG31 PWM output 1	P3_7	P3_7	P0_3/ P3_7	P0_3/ P3_7
	TSG31O2	O	TSG31 PWM output 2	P3_8	P3_8	P0_4/ P3_8	P0_4/ P3_8
	TSG31O3	O	TSG31 PWM output 3	P3_9	P3_9	P0_5/ P3_9	P0_5/ P3_9
	TSG31O4	O	TSG31 PWM output 4	P3_10	P3_10	P0_6/ P3_10	P0_6/ P3_10
	TSG31O5	O	TSG31 PWM output 5	P3_12	P3_12	P0_7/ P3_12	P0_7/ P3_12
	TSG31O6	O	TSG31 PWM output 6	P3_13	P3_13	P0_8/ P3_13	P0_8/ P3_13
	TSG31O7	O	TSG31 AD trigger diagnostic output	P3_14	P3_14	P0_9/ P3_14	P0_9/ P3_14
	TSG31PTSI0	I	TSG31 hall sensor input 0	P4_4	P4_4	P0_11/ P4_4	P0_11/ P4_4
	TSG31PTSI1	I	TSG31 hall sensor input 1	P4_5	P4_5	P0_12/ P4_5	P0_12/ P4_5
	TSG31PTSI2	I	TSG31 hall sensor input 2	P0_13/ P4_6	P0_13/ P4_6	P0_13/ P4_6	P0_13/ P4_6
	TSG31CLKI	I	TSG31 external clock input enable	P0_0	P0_0	P0_0/ P4_7	P0_0/ P4_7
ESO	TAPA0ESO	I	Emergency Hi-Z input 0	P3_14	P3_14	P3_14	P3_14
	TAPA1ESO	I	Emergency Hi-Z input 1	P0_2/ P4_4	P0_2/ P4_4	P0_2/ P4_4	P0_2/ P4_4

Table 2.2 Pin Function (7/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
ENCA0	ENCA0TIN0	I	ENCA0 capture trigger input 0	—	—	P4_7	P4_7
	ENCA0TIN1	I	ENCA0 capture trigger input 1	—	—	P4_8	P4_8
	ENCA0E0	I	ENCA0 encoder input	P4_0	P4_0	P4_0	P4_0
	ENCA0E1	I	ENCA0 encoder input	P4_1	P4_1	P4_1	P4_1
	ENCA0EC	I	ENCA0 encoder input	P4_2	P4_2	P4_2	P4_2
ENCA1	ENCA1TIN0	I	ENCA1 capture trigger input 0	—	—	P4_9	P4_9
	ENCA1TIN1	I	ENCA1 capture trigger input 1	—	—	P4_10	P4_10
	ENCA1E0	I	ENCA1 encoder input	P4_4	P4_4	P0_11/ P4_4	P0_11/ P4_4
	ENCA1E1	I	ENCA1 encoder input	P4_5	P4_5	P0_12/ P4_5	P0_12/ P4_5
	ENCA1EC	I	ENCA1 encoder input	P0_13/ P4_6	P0_13/ P4_6	P0_13/ P4_6	P0_13/ P4_6
OSTM0	OSTM0O	O	OSTM0 timer output	P0_13	P0_13	P0_13	P0_13
OSTM1	OSTM1O	O	OSTM1 timer output	P2_6/ P4_3	P2_6/ P4_3	P2_10/ P2_6/ P4_3	P2_10/ P2_6/ P4_3
TPBA0	TPBA0O	O	TPBA0 timer pattern buffer output 0	P2_2	P2_2	P2_2	P2_2
TPBA1	TPBA1O	O	TPBA0 timer pattern buffer output 1	P3_8/ P2_3/ P3_14	P3_8/ P2_3/ P3_14	P3_8/ P2_3/ P3_14	P3_8/ P2_3/ P3_14
CLKDIV0	EXTCLK0O	O	Clock controller output	P3_14	P3_14	P3_14	P3_14
CLKDIV1	EXTCLK1O	O	Clock controller output	P4_5	P4_5	P4_5	P4_5
CSIG0	CSIG0RYI	I	CSIG0 ready (1) / busy (0) input signal	—	—	P3_5	P3_5
	CSIG0RYO	O	CSIG0 ready (1) / busy (0) output signal	—	—	P3_4	P3_4
	CSIG0SCI	I	CSIG0 serial clock input signal	P5_4	P5_4	P3_2/ P5_4/ P5_2	P3_2/ P5_4/ P5_2
	CSIG0SCO	O	CSIG0 serial clock output signal	P5_4	P5_4	P3_2/ P5_4/ P5_2	P3_2/ P5_4/ P5_2
CSIG0	CSIG0SI	I	CSIG0 serial data input	P5_0	P5_0	P3_0/ P5_0	P3_0/ P5_0
	CSIG0SO	O	CSIG0 serial data output	P5_1	P5_1	P3_1/ P5_1	P3_1/ P5_1

Table 2.2 Pin Function (8/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
CSIH0	CSIH0CSS0	O	CSIH0 serial peripheral chip select signal 0	P3_12	P3_12	P3_12	P3_12
	CSIH0CSS1	O	CSIH0 serial peripheral chip select signal 1	P3_13	P3_13	P3_13	P3_13
	CSIH0CSS2	O	CSIH0 serial peripheral chip select signal 2	P2_4	P2_4	P2_14/ P2_4	P2_14/ P2_4
	CSIH0CSS3	O	CSIH0 serial peripheral chip select signal 3	P2_5	P2_5	P2_13/ P2_5	P2_13/ P2_5
	CSIH0CSS4	O	CSIH0 serial peripheral chip select signal 4	P2_6	P2_6	P2_12/ P2_6	P2_12/ P2_6
	CSIH0CSS5	O	CSIH0 serial peripheral chip select signal 5	P2_7/ P2_2	P2_7/ P2_2	P2_11/ P2_7/ P2_2	P2_11/ P2_7/ P2_2
	CSIH0CSS6	O	CSIH0 serial peripheral chip select signal 6	P2_8	P2_8	P2_10/ P2_8	P2_10/ P2_8
	CSIH0CSS7	O	CSIH0 serial peripheral chip select signal 7	P2_9	P2_9	P3_2/ P2_9	P3_2/ P2_9
	CSIH0SSI	I	CSIH0 serial SS function control input signal	P3_8	P3_8	P3_8	P3_8
	CSIH0RYI	I	CSIH0 ready (1) / busy (0) input signal	P3_9/ P3_3	P3_9/ P3_3	P3_9/ P3_3/ P2_15/ P2_10	P3_9/ P3_3/ P2_15/ P2_10
	CSIH0RYO	O	CSIH0 ready (1) / busy (0) output signal	—	—	P2_11	P2_11
	CSIH0SCI	I	CSIH0 serial clock input signal	P3_8/ P2_6	P3_8/ P2_6	P3_8/ P3_1/ P2_6	P3_8/ P3_1/ P2_6
	CSIH0SCO	O	CSIH0 serial clock output signal	P3_8/ P2_6	P3_8/ P2_6	P3_8/ P3_1/ P2_6	P3_8/ P3_1/ P2_6
	CSIH0SI	I	CSIH0 serial data input	P3_6/ P2_4	P3_6/ P2_4	P3_6/ P3_2/ P2_4	P3_6/ P3_2/ P2_4
	CSIH0SO	O	CSIH0 serial data output	P3_7/ P2_5	P3_7/ P2_5	P3_7/ P3_0/ P2_12/ P2_5	P3_7/ P3_0/ P2_12/ P2_5
CSIH1	CSIH1CSS0	O	CSIH1 serial peripheral chip select signal 0	P4_3	P4_3	P4_3	P4_3
	CSIH1CSS1	O	CSIH1 serial peripheral chip select signal 1	P4_4	P4_4	P4_4	P4_4
	CSIH1CSS2	O	CSIH1 serial peripheral chip select signal 2	P4_5	P4_5	P4_5	P4_5
	CSIH1CSS3	O	CSIH1 serial peripheral chip select signal 3	P4_6	P4_6	P4_6	P4_6
	CSIH1CSS4	O	CSIH1 serial peripheral chip select signal 4	—	—	P4_7	P4_7
	CSIH1CSS5	O	CSIH1 serial peripheral chip select signal 5	—	—	P4_8	P4_8
	CSIH1CSS6	O	CSIH1 serial peripheral chip select signal 6	—	—	P4_9	P4_9
	CSIH1CSS7	O	CSIH1 serial peripheral chip select signal 7	—	—	P4_10	P4_10
	$\overline{\text{CSIH1SSI}}$	I	CSIH1 serial SS function control input signal	—	—	P4_8	P4_8
	CSIH1RYI	I	CSIH1 ready (1) / busy (0) input signal	P3_13	P3_13	P3_13/ P2_11/ P4_9	P3_13/ P2_11/ P4_9
	CSIH1RYO	O	CSIH1 ready (1) / busy (0) output signal	P3_12/ P4_2	P3_12/ P4_2	P3_12/ P2_13/ P4_10/ P4_2	P3_12/ P2_13/ P4_10/ P4_2
	CSIH1SCI	I	CSIH1 serial clock input signal	P2_9/ P4_1	P2_9/ P4_1	P2_9/ P4_1	P2_9/ P4_1

Table 2.2 Pin Function (9/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
CSIH1	CSIH1SCO	O	CSIH1 serial clock output signal	P2_9/ P4_1	P2_9/ P4_1	P2_9/ P4_1	P2_9/ P4_1
	CSIH1SI	I	CSIH1 serial data input	P2_7/ P3_14	P2_7/ P3_14	P2_7/ P3_14	P2_7/ P3_14
	CSIH1SO	O	CSIH1 serial data output	P2_8/ P4_0	P2_8/ P4_0	P2_8/ P4_0	P2_8/ P4_0
CSIH2	CSIH2CSS0	O	CSIH2 serial peripheral chip select signal 0	P2_3/ P1_1	P2_3/ P1_1	P2_3/ P1_1/ P4_7/ P5_2	P2_3/ P1_1/ P4_7/ P5_2
	CSIH2CSS1	O	CSIH2 serial peripheral chip select signal 1	P3_3/ P5_0	P3_3/ P5_0	P3_3/ P5_0/ P4_8	P3_3/ P5_0/ P4_8
	CSIH2CSS2	O	CSIH2 serial peripheral chip select signal 2	P3_4/ P5_1	P3_4/ P5_1	P3_4/ P5_1/ P4_9	P3_4/ P5_1/ P4_9
	CSIH2CSS3	O	CSIH2 serial peripheral chip select signal 3	P3_5/ P5_4	P3_5/ P5_4	P3_5/ P5_4/ P4_10	P3_5/ P5_4/ P4_10
	CSIH2CSS4	O	CSIH2 serial peripheral chip select signal 4	P3_6/ P5_5	P3_6/ P5_5	P3_6/ P5_5/ P4_11	P3_6/ P5_5/ P4_11
	CSIH2CSS5	O	CSIH2 serial peripheral chip select signal 5	P3_7/ P5_6	P3_7/ P5_6	P3_7/ P5_6/ P4_12	P3_7/ P5_6/ P4_12
	CSIH2CSS6	O	CSIH2 serial peripheral chip select signal 6	P3_8	P3_8	P3_8/ P5_7/ P4_14	P3_8/ P5_7/ P4_14
	CSIH2CSS7	O	CSIH2 serial peripheral chip select signal 7	P3_9/ P4_4	P3_9/ P4_4	P3_9/ P5_8/ P4_4	P3_9/ P5_8/ P4_4
	$\overline{\text{CSIH2SSI}}$	I	CSIH2 serial SS function control input signal	—	—	P4_13/ P5_11	P4_13/ P5_11
	CSIH2RYI	I	CSIH2 ready (1) / busy (0) input signal	P3_7/ P2_3/ P4_3	P3_7/ P2_3/ P4_3	P3_7/ P2_3/ P4_3/ P5_12	P3_7/ P2_3/ P4_3/ P5_12
	CSIH2RYO	O	CSIH2 ready (1) / busy (0) output signal	P2_4	P2_4	P2_4/ P4_7/ P5_13	P2_4/ P4_7/ P5_13
	CSIH2SCI	I	CSIH2 serial clock input signal	P2_2/ P1_4/ P4_6	P2_2/ P1_4/ P4_6	P2_2/ P1_4/ P4_6/ P5_15	P2_2/ P1_4/ P4_6/ P5_15
	CSIH2SCO	O	CSIH2 serial clock output signal	P2_2/ P1_4/ P4_6	P2_2/ P1_4/ P4_6	P2_2/ P1_4/ P4_6/ P5_15	P2_2/ P1_4/ P4_6/ P5_15
	CSIH2SI	I	CSIH2 serial data input	P2_0/ P1_2/ P4_4/ P5_9	P2_0/ P1_2/ P4_4/ P5_9	P2_0/ P1_2/ P4_4/ P5_9	P2_0/ P1_2/ P4_4/ P5_9
	CSIH2SO	O	CSIH2 serial data output	P2_1/ P1_3/ P4_5/ P5_14	P2_1/ P1_3/ P4_5/ P5_14	P2_1/ P1_3/ P4_5/ P5_14	P2_1/ P1_3/ P4_5/ P5_14
CSIH3	CSIH3CSS0	O	CSIH3 serial peripheral chip select signal 0	P2_8	P2_8	P2_8	P2_8
	CSIH3CSS1	O	CSIH3 serial peripheral chip select signal 1	P2_9	P2_9	P2_9	P2_9
	CSIH3CSS2	O	CSIH3 serial peripheral chip select signal 2	P3_5	P3_5	P3_5	P3_5
	CSIH3CSS3	O	CSIH3 serial peripheral chip select signal 3	P3_4	P3_4	P3_4	P3_4
	CSIH3CSS4	O	CSIH3 serial peripheral chip select signal 4	P3_3	P3_3	P3_3	P3_3
	CSIH3CSS5	O	CSIH3 serial peripheral chip select signal 5	P3_9	P3_9	P3_9	P3_9

Table 2.2 Pin Function (10/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
CSIH3	CSIH3CSS6	O	CSIH3 serial peripheral chip select signal 6	P2_0	P2_0	P2_0	P2_0
	CSIH3CSS7	O	CSIH3 serial peripheral chip select signal 7	P2_1	P2_1	P2_1	P2_1
	CSIH3SSI	I	CSIH3 serial SS function control input signal	P3_3	P3_3	P3_3	P3_3
	CSIH3RYI	I	CSIH3 ready (1) / busy (0) input signal	P3_6/ P2_8/ P1_1	P3_6/ P2_8/ P1_1	P3_6/ P2_8/ P1_1	P3_6/ P2_8/ P1_1
	CSIH3RYO	O	CSIH3 ready (1) / busy (0) output signal	P2_8	P2_8	P2_8/ P1_0	P2_8/ P1_0
	CSIH3SCI	I	CSIH3 serial clock input signal	P2_7/ P1_4	P2_7/ P1_4	P2_7/ P1_4	P2_7/ P1_4
	CSIH3SCO	O	CSIH3 serial clock output signal	P2_7/ P1_4	P2_7/ P1_4	P2_7/ P1_4	P2_7/ P1_4
	CSIH3SI	I	CSIH3 serial data input	P2_6/ P1_2	P2_6/ P1_2	P2_6/ P1_2	P2_6/ P1_2
	CSIH3SO	O	CSIH3 serial data output	P2_5/ P1_3	P2_5/ P1_3	P2_5/ P1_3	P2_5/ P1_3
SCI30	SCI30RX	I	SCI30 data input	P3_7/ P2_5/ P0_2/ P5_0/ P4_5	P3_7/ P2_5/ P0_2/ P5_0/ P4_5	P3_7/ P2_5/ P0_2/ P5_0/ P4_5	P3_7/ P2_5/ P0_2/ P5_0/ P4_5
	SCI30TX	O	SCI30 data output	P3_12/ P2_6/ P5_1/ P4_6	P3_12/ P2_6/ P5_1/ P4_6	P3_12/ P2_6/ P0_3/ P5_1/ P4_6	P3_12/ P2_6/ P0_3/ P5_1/ P4_6
	SCI30SCI	I	SCI30 serial clock input	P3_13/ P2_7/ P5_4/ P4_2	P3_13/ P2_7/ P5_4/ P4_2	P3_13/ P2_7/ P0_4/ P5_4/ P5_2/ P4_2	P3_13/ P2_7/ P0_4/ P5_4/ P5_2/ P4_2
	SCI30SCO	O	SCI30 serial clock output	P3_13/ P2_7/ P5_4/ P4_2	P3_13/ P2_7/ P5_4/ P4_2	P3_13/ P2_7/ P0_4/ P5_4/ P5_2/ P4_2	P3_13/ P2_7/ P0_4/ P5_4/ P5_2/ P4_2
SCI31	SCI31RX	I	SCI31 data input	P2_8/ P5_5	P2_8/ P5_5	P2_8/ P5_5	P2_8/ P5_5
	SCI31TX	O	SCI31 data output	P2_9/ P5_6	P2_9/ P5_6	P2_9/ P5_6	P2_9/ P5_6
	SCI31SCI	I	SCI31 serial clock input	P0_13/ P3_5	P0_13/ P3_5	P0_13/ P3_5/ P5_7	P0_13/ P3_5/ P5_7
	SCI31SCO	O	SCI31 serial clock output	P0_13/ P3_5	P0_13/ P3_5	P0_13/ P3_5/ P5_7	P0_13/ P3_5/ P5_7
SCI32	SCI32RX	I	SCI32 data input	P0_2/ P3_4	P0_2/ P3_4	P0_2/ P3_4/ P5_8	P0_2/ P3_4/ P5_8
	SCI32TX	O	SCI32 data output	P3_3/ P5_9	P3_3/ P5_9	P3_3/ P5_9	P3_3/ P5_9
	SCI32SCI	I	SCI32 serial clock input	P3_9/ P5_10	P3_9/ P5_10	P3_9/ P5_10	P3_9/ P5_10
	SCI32SCO	O	SCI32 serial clock output	P3_9/ P5_10	P3_9/ P5_10	P3_9/ P5_10	P3_9/ P5_10
RLIN30	RLIN30RX	I	RLIN30 data input	P3_4/ P1_1/ P5_14/ P5_10/ P4_0	P3_4/ P1_1/ P5_14/ P5_10/ P4_0	P3_4/ P1_1/ P5_14/ P5_10/ P4_0	P3_4/ P1_1/ P5_14/ P5_10/ P4_0

Table 2.2 Pin Function (11/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
RLIN30	RLIN30TX	O	RLIN30 data output	P3_5/ P0_0/ P4_1	P3_5/ P0_0/ P4_1	P3_5/ P1_0/ P0_0/ P5_15/ P5_11/ P4_1	P3_5/ P1_0/ P0_0/ P5_15/ P5_11/ P4_1
RLIN31	RLIN31RX	I	RLIN31 data input	P2_5/ P0_1	P2_5/ P0_1	P2_5/ P0_1/ P5_15/ P5_12	P2_5/ P0_1/ P5_15/ P5_12
	RLIN31TX	O	RLIN31 data output	P2_4/ P3_11	P2_4/ P3_11	P2_4/ P3_11/ P5_13	P2_4/ P3_11/ P5_13
RSCANFD0	RSCAN0RX0	I	RSCAN0 receive data input 0	P3_7/ P2_0/ P4_5	P3_7/ P2_0/ P4_5	P3_7/ P2_0/ P4_5	P3_7/ P2_0/ P4_5
	RSCAN0TX0	O	RSCAN0 transmit data output 0	P3_8/ P2_1/ P4_6	P3_8/ P2_1/ P4_6	P3_8/ P2_1/ P4_6	P3_8/ P2_1/ P4_6
	RSCAN0RX1	I	RSCAN0 receive data input 1	P3_12/ P2_2/ P4_2	P3_12/ P2_2/ P4_2	P3_12/ P2_2/ P4_7/ P4_2	P3_12/ P2_2/ P4_7/ P4_2
	RSCAN0TX1	O	RSCAN0 transmit data output 1	P3_13/ P2_3/ P4_3	P3_13/ P2_3/ P4_3	P3_13/ P2_3/ P4_3	P3_13/ P2_3/ P4_3
	RSCAN0RX2	I	RSCAN0 receive data input 2	P5_6	P5_6	P5_6	P5_6
	RSCAN0TX2	O	RSCAN0 transmit data output 2	P5_5	P5_5	P5_5/ P5_7	P5_5/ P5_7
FLXA0	FLXA0RXDA	I	FLXA0 channel A receive data input	P4_2	P4_2	P4_8/ P4_2	P4_8/ P4_2
	FLXA0RXDB	I	FLXA0 channel B receive data input	P4_3	P4_3	P4_11/ P4_3	P4_11/ P4_3
	FLXA0STPWT	I	FLXA0 stop watch trigger input	P4_4	P4_4	P4_14/ P4_4	P4_14/ P4_4
	FLXA0TXDA	O	FLXA0 channel A transmit data output	P4_0	P4_0	P4_9/ P4_0	P4_9/ P4_0
	FLXA0TXDB	O	FLXA0 channel B transmit data output	P4_5	P4_5	P4_12/ P4_5	P4_12/ P4_5
	FLXA0TXENA	O	FLXA0 channel A transmit enable	P4_1	P4_1	P4_10/ P4_1	P4_10/ P4_1
	FLXA0TXENB	O	FLXA0 channel B transmit enable	P4_6	P4_6	P4_13/ P4_6	P4_13/ P4_6
PSI50	PSI50DIN	I	PSI50 receive data input	P5_14	P5_14	P5_14	P5_14
	PSI50DOUT	O	PSI50 transmit data output	P0_0	P0_0	P0_0	P0_0
PSI51	PSI51DIN	I	PSI51 receive data input	P5_9	P5_9	P5_9	P5_9
	PSI51DOUT	O	PSI51 transmit data output	P5_10	P5_10	P5_10	P5_10
SENT0	SENT0RX	I	SENT ch0 sensor data input	P5_5	P5_5	P5_5	P5_5
	SENT0SPCO	O	SENT ch0 SPC extension output	P5_6/ P5_5	P5_6/ P5_5	P0_8/ P5_6/ P5_5	P0_8/ P5_6/ P5_5
SENT1	SENT1RX	I	SENT ch1 sensor data input	P5_10	P5_10	P5_8/ P5_10	P5_8/ P5_10
	SENT1SPCO	O	SENT ch1 SPC extension output	P5_9/ P5_10	P5_9/ P5_10	P0_7/ P5_9/ P5_8/ P5_10	P0_7/ P5_9/ P5_8/ P5_10
SENT2	SENT2RX	I	SENT ch2 sensor data input	—	—	P5_12	P5_12

Table 2.2 Pin Function (12/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
SENT2	SENT2SPCO	O	SENT ch2 SPC extension output	—	—	P0_6/ P5_13/ P5_12	P0_6/ P5_13/ P5_12
SENT3	SENT3RX	I	SENT ch3 sensor data input	P5_14	P5_14	P5_14/ P5_11	P5_14/ P5_11
	SENT3SPCO	O	SENT ch3 SPC extension output	P0_0/ P5_14	P0_0/ P5_14	P0_5/ P0_0/ P5_15/ P5_14/ P5_11	P0_5/ P0_0/ P5_15/ P5_14/ P5_11
SENT4	SENT4RX	I	SENT ch4 sensor data input	P0_1	P0_1	P0_1	P0_1
	SENT4SPCO	O	SENT ch4 SPC extension output	P3_11/ P0_1	P3_11/ P0_1	P0_4/ P3_11/ P0_1	P0_4/ P3_11/ P0_1
SENT5	SENT5RX	I	SENT ch5 sensor data input	P0_2	P0_2	P0_2/ P2_10	P0_2/ P2_10
	SENT5SPCO	O	SENT ch5 SPC extension output	P0_2	P0_2	P0_3/ P0_2/ P2_11/ P2_10	P0_3/ P0_2/ P2_11/ P2_10
ADCG0	ADCGTRG0	I	AD trigger input 0	P5_10	P5_10	P0_7/ P5_10	P0_7/ P5_10
	ADCG0CNV0	O	ADCG0 AD conversion start signal	P0_2/ P5_10/ P5_1	P0_2/ P5_10/ P5_1	P0_2/ P5_10/ P5_1	P0_2/ P5_10/ P5_1
	ADCG0CNV1	O	ADCG0 AD conversion start signal	P5_14/ P5_4	P5_14/ P5_4	P0_3/ P5_14/ P5_4	P0_3/ P5_14/ P5_4
	ADCG0CNV2	O	ADCG0 AD conversion start signal	P0_0/ P5_5	P0_0/ P5_5	P0_4/ P0_0/ P5_5	P0_4/ P0_0/ P5_5
	ADCG0CNV3	O	ADCG0 AD conversion start signal	P0_1/ P5_6	P0_1/ P5_6	P0_5/ P0_1/ P5_6	P0_5/ P0_1/ P5_6
	ADCG0CNV4	O	ADCG0 AD conversion start signal	P3_11	P3_11	P0_9/ P3_11/ P5_7	P0_9/ P3_11/ P5_7
	ADCG0I0	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I1	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I2	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I3	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I4	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I5	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I6	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I7	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I8	I	ADCG0 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG0I9	I	ADCG0 input channel	—	—	Not alternative	Not alternative
	ADCG0I10	I	ADCG0 input channel	—	—	Not alternative	Not alternative
	ADCG0I11	I	ADCG0 input channel	—	—	Not alternative	Not alternative

Table 2.2 Pin Function (13/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
ADCG1	ADCGTRG1	I	AD trigger input 1	P5_14	P5_14	P0_8/ P5_14	P0_8/ P5_14
	ADCG1CNV0	O	ADCG1 AD conversion start signal	P0_10/ P4_0	P0_10/ P4_0	P0_10/ P4_0	P0_10/ P4_0
	ADCG1CNV1	O	ADCG1 AD conversion start signal	P4_1	P4_1	P0_9/ P4_1	P0_9/ P4_1
	ADCG1CNV2	O	ADCG1 AD conversion start signal	P4_2	P4_2	P0_11/ P4_2	P0_11/ P4_2
	ADCG1CNV3	O	ADCG1 AD conversion start signal	P4_3	P4_3	P0_12/ P4_3	P0_12/ P4_3
	ADCG1CNV4	O	ADCG1 AD conversion start signal	P4_4	P4_4	P0_14/ P4_4	P0_14/ P4_4
	ADCG1I0	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I1	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I2	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I3	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I4	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I5	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I6	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I7	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I8	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I9	I	ADCG1 input channel	Not alternative	Not alternative	Not alternative	Not alternative
	ADCG1I10	I	ADCG1 input channel	—	—	Not alternative	Not alternative
	ADCG1I11	I	ADCG1 input channel	—	—	Not alternative	Not alternative
Nexus	DCUTCK	I	Debug clock	JP0_2	JP0_2	JP0_2	JP0_2
	DCUTDI	I	Debug data input	JP0_0	JP0_0	JP0_0	JP0_0
	DCUTDO	O	Debug data output	JP0_1	JP0_1	JP0_1	JP0_1
	DCUTMS	I	Debug mode select	JP0_3	JP0_3	JP0_3	JP0_3
	$\overline{\text{DCUTRDY}}$	O	Debug ready	JP0_5	JP0_5	JP0_5	JP0_5
	$\overline{\text{DCUTRST}}$*1	I	Debug reset	JP0_4	JP0_4	JP0_4	JP0_4
LPD	LPDCLK	I	LPD clock input (4-pin mode)	JP0_2	JP0_2	JP0_2	JP0_2
	LPDCLKOUT	O	LPD clock output (4-pin mode)	JP0_5	JP0_5	JP0_5	JP0_5
	LPDI	I	LPD data input (4-pin mode)	JP0_0	JP0_0	JP0_0	JP0_0
	LPDO	O	LPD data output (4-pin mode)	JP0_1	JP0_1	JP0_1	JP0_1
Nexus	$\overline{\text{EVTO}}$	O	Debug I/F event output signal	P0_10	P0_10	P0_10	P0_10
	$\overline{\text{EVTI}}$	I	Debug I/F event input signal	P0_13	P0_13	P0_13	P0_13
FLSCI3	FLSCI3TXD (FPDT)	O	Flash Writer I/F TxD	JP0_0/ JP0_1	JP0_0/ JP0_1	JP0_0/ JP0_1	JP0_0/ JP0_1
	FLSCI3RXD (FPDR)	I	Flash Writer I/F RxD	JP0_0	JP0_0	JP0_0	JP0_0
	FLSCI3SCKI (FPCK)	I	Flash Writer I/F SCK	JP0_2	JP0_2	JP0_2	JP0_2

Table 2.2 Pin Function (14/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
MODE	FLMD1	I	Secondary operating mode select pin	P3_14	P3_14	P3_14	P3_14
System	FLMD0	I	Primary operating mode select	Not alternative	Not alternative	Not alternative	Not alternative
	$\overline{\text{RESET}}$	I	Reset input	Not alternative	Not alternative	Not alternative	Not alternative
	$\overline{\text{RESETOUT}}$	O	Reset output	P0_10	P0_10	P0_10	P0_10
	X1	—	Main clock crystal oscillator connections	Not alternative	Not alternative	Not alternative	Not alternative
	X2	—	Main clock crystal oscillator connections	Not alternative	Not alternative	Not alternative	Not alternative
CVM	$\overline{\text{CVMOUT}}$	O	CVM internal voltage error detection output signal	Not alternative	Not alternative	Not alternative	Not alternative
Safety	$\overline{\text{ERROROUT}}$	O	Error output signal	Not alternative	Not alternative	Not alternative	Not alternative
	$\overline{\text{ERROROUT\_C}}$	O	Error output signal C	P3_11	P3_11	P3_11	P3_11
JPORT0	JP0_0	I/O	JTAG port	JP0_0	JP0_0	JP0_0	JP0_0
	JP0_1	I/O	JTAG port	JP0_1	JP0_1	JP0_1	JP0_1
	JP0_2	I	JTAG port	JP0_2	JP0_2	JP0_2	JP0_2
	JP0_3	I/O	JTAG port	JP0_3	JP0_3	JP0_3	JP0_3
	JP0_4	I	JTAG port	JP0_4	JP0_4	JP0_4	JP0_4
	JP0_5	I/O	JTAG port	JP0_5	JP0_5	JP0_5	JP0_5
P0	P0_0	I/O	Port	P0_0	P0_0	P0_0	P0_0
	P0_1	I/O	Port	P0_1	P0_1	P0_1	P0_1
	P0_2	I/O	Port	P0_2	P0_2	P0_2	P0_2
	P0_3	I/O	Port	—	—	P0_3	P0_3
	P0_4	I/O	Port	—	—	P0_4	P0_4
	P0_5	I/O	Port	—	—	P0_5	P0_5
	P0_6	I/O	Port	—	—	P0_6	P0_6
	P0_7	I/O	Port	—	—	P0_7	P0_7
	P0_8	I/O	Port	—	—	P0_8	P0_8
	P0_9	I/O	Port	—	—	P0_9	P0_9
	P0_10	I/O	Port	P0_10	P0_10	P0_10	P0_10
	P0_11	I/O	Port	—	—	P0_11	P0_11
	P0_12	I/O	Port	—	—	P0_12	P0_12
	P0_13	I/O	Port	P0_13	P0_13	P0_13	P0_13
	P0_14	I/O	Port	—	—	P0_14	P0_14
P1	P1_0	I/O	Port	—	—	P1_0	P1_0
	P1_1	I/O	Port	P1_1	P1_1	P1_1	P1_1
	P1_2	I/O	Port	P1_2	P1_2	P1_2	P1_2
	P1_3	I/O	Port	P1_3	P1_3	P1_3	P1_3
	P1_4	I/O	Port	P1_4	P1_4	P1_4	P1_4

Table 2.2 Pin Function (15/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
P2	P2_0	I/O	Port	P2_0	P2_0	P2_0	P2_0
	P2_1	I/O	Port	P2_1	P2_1	P2_1	P2_1
	P2_2	I/O	Port	P2_2	P2_2	P2_2	P2_2
	P2_3	I/O	Port	P2_3	P2_3	P2_3	P2_3
	P2_4	I/O	Port	P2_4	P2_4	P2_4	P2_4
	P2_5	I/O	Port	P2_5	P2_5	P2_5	P2_5
	P2_6	I/O	Port	P2_6	P2_6	P2_6	P2_6
	P2_7	I/O	Port	P2_7	P2_7	P2_7	P2_7
	P2_8	I/O	Port	P2_8	P2_8	P2_8	P2_8
	P2_9	I/O	Port	P2_9	P2_9	P2_9	P2_9
	P2_10	I/O	Port	—	—	P2_10	P2_10
	P2_11	I/O	Port	—	—	P2_11	P2_11
	P2_12	I/O	Port	—	—	P2_12	P2_12
	P2_13	I/O	Port	—	—	P2_13	P2_13
	P2_14	I/O	Port	—	—	P2_14	P2_14
	P2_15	I/O	Port	—	—	P2_15	P2_15
P3	P3_0	I/O	Port	—	—	P3_0	P3_0
	P3_1	I/O	Port	—	—	P3_1	P3_1
	P3_2	I/O	Port	—	—	P3_2	P3_2
	P3_3	I/O	Port	P3_3	P3_3	P3_3	P3_3
	P3_4	I/O	Port	P3_4	P3_4	P3_4	P3_4
	P3_5	I/O	Port	P3_5	P3_5	P3_5	P3_5
	P3_6	I/O	Port	P3_6	P3_6	P3_6	P3_6
	P3_7	I/O	Port	P3_7	P3_7	P3_7	P3_7
	P3_8	I/O	Port	P3_8	P3_8	P3_8	P3_8
	P3_9	I/O	Port	P3_9	P3_9	P3_9	P3_9
	P3_10	I/O	Port	P3_10	P3_10	P3_10	P3_10
	P3_11	I/O	Port	P3_11	P3_11	P3_11	P3_11
	P3_12	I/O	Port	P3_12	P3_12	P3_12	P3_12
	P3_13	I/O	Port	P3_13	P3_13	P3_13	P3_13
	P3_14	I/O	Port	P3_14	P3_14	P3_14	P3_14
P4	P4_0	I/O	Port	P4_0	P4_0	P4_0	P4_0
	P4_1	I/O	Port	P4_1	P4_1	P4_1	P4_1
	P4_2	I/O	Port	P4_2	P4_2	P4_2	P4_2
	P4_3	I/O	Port	P4_3	P4_3	P4_3	P4_3
	P4_4	I/O	Port	P4_4	P4_4	P4_4	P4_4
	P4_5	I/O	Port	P4_5	P4_5	P4_5	P4_5
	P4_6	I/O	Port	P4_6	P4_6	P4_6	P4_6
	P4_7	I/O	Port	—	—	P4_7	P4_7
	P4_8	I/O	Port	—	—	P4_8	P4_8
	P4_9	I/O	Port	—	—	P4_9	P4_9
	P4_10	I/O	Port	—	—	P4_10	P4_10
	P4_11	I/O	Port	—	—	P4_11	P4_11
	P4_12	I/O	Port	—	—	P4_12	P4_12

Table 2.2 Pin Function (16/16)

Category	Pin name	IO	Function	Alternative Port			
				100-pin		144-pin	
				eVR	DPS	eVR	DPS
P4	P4_13	I/O	Port	—	—	P4_13	P4_13
	P4_14	I/O	Port	—	—	P4_14	P4_14
P5	P5_0	I/O	Port	P5_0	P5_0	P5_0	P5_0
	P5_1	I/O	Port	P5_1	P5_1	P5_1	P5_1
	P5_2	I/O	Port	—	—	P5_2	P5_2
	P5_3	I/O	Port	—	—	P5_3	P5_3
	P5_4	I/O	Port	P5_4	P5_4	P5_4	P5_4
	P5_5	I/O	Port	P5_5	P5_5	P5_5	P5_5
	P5_6	I/O	Port	P5_6	P5_6	P5_6	P5_6
	P5_7	I/O	Port	—	—	P5_7	P5_7
	P5_8	I/O	Port	—	—	P5_8	P5_8
	P5_9	I/O	Port	P5_9	P5_9	P5_9	P5_9
	P5_10	I/O	Port	P5_10	P5_10	P5_10	P5_10
	P5_11	I/O	Port	—	—	P5_11	P5_11
	P5_12	I/O	Port	—	—	P5_12	P5_12
	P5_13	I/O	Port	—	—	P5_13	P5_13
	P5_14	I/O	Port	P5_14	P5_14	P5_14	P5_14
	P5_15	I/O	Port	—	—	P5_15	P5_15

Note 1. This is a dedicated pin. Do not use it as a port pin.

Section 3 Electrical Specifications

3.1 Overview

The specifications in this section are for devices operating under the following conditions. Where a special condition is required for a given specification, the condition will be indicated. Furthermore, the specifications in this section are not guaranteed unless the conditions listed below are met.

3.1.1 General Measurement Conditions

3.1.1.1 Common Conditions

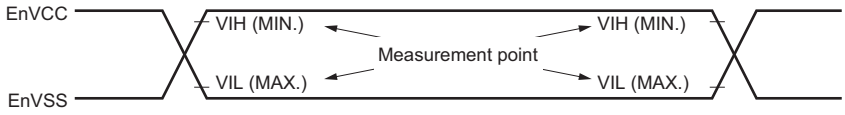
- Power supply
  - VCC = 3.0 V to 5.5 V
  - EnVCC = 3.0 V to 5.5 V
  - VDD = 1.20 V to 1.35 V*1
  - A0VCC, A1VCC = 3.0 V to 5.5 V
  - A0VREFH = 3.0 V to 5.5 V
  - A1VREFH = 3.0 V to 5.5 V
  - EnVSS = VSS = A0VSS = A1VSS = 0 V
- Capacitance of the internal regulator
  - CVCL: 0.1 µF +/– 30%*2
- Operating temperature
  - Tj = –40 to +150°C
- Load conditions
  - CL = 30 pF

Note 1. Only applicable for DPS products

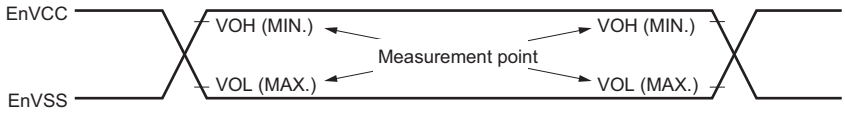
Note 2. See **Section 3.7, Regulator Characteristics**.

3.1.1.2 AC Characteristic Measurement Condition

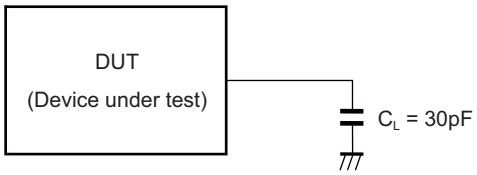
(1) AC test input measurement points



(2) AC test output measurement points



(3) Load conditions



CAUTION

If the load capacitance exceeds 30 pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce the capacitance to a value less than or equal to 30 pF.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are shown in the table below.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power voltage	VCC		–0.3		6.5	V
	EnVCC		–0.3		6.5	V
	A0VCC		–0.3		6.5	V
	A1VCC		–0.3		6.5	V
	VDD		–0.3		1.8	V
Input voltage	VI	EnVCC pin	–0.3		EnVCC+0.3	V
		VCC pin	–0.3		VCC+0.3	V
Analogue reference voltage	A0VREFH		–0.3		A0VCC+0.3	V
	A1VREFH		–0.3		A1VCC+0.3	V
Analog input voltage	VAIN	A0VCC pin	–0.3		A0VCC+0.3	V
		A1VCC pin	–0.3		A1VCC+0.3	V
Low level output current	IOL	1 pin			10	mA
		Total			80	mA
High level output current	IOH	1 pin			–10	mA
		Total			–80	mA
Junction temperature	Tj		–40		150	°C
Storage temperature	Tstg		–55		150	°C

Note: Ta = 25°C
VSS = EnVSS = A0VSS = A1VSS = 0 V

CAUTIONS

1. Using this device without observing these absolute maximum ratings may result in permanent breakdown of the device.
2. This device is used in combination of multiple power voltages simultaneously in some cases. Use this device by observing the power pin connections, conditions for combination of power voltages to be applied, voltages that can be applied to pins, and output voltage conditions, which are specified in the manual. Using this device with other than specified power connection or voltage may result in permanent breakdown of the device or damage to the system that contains the device.
3. The input voltage, analog reference voltage and analog input voltage must not exceed 6.5 V.

3.3 Supply Voltage Characteristics

Symbol	MIN.	TYP.	MAX.	Unit
VCC[*1]	3.0		5.5	V
EnVCC[*1]	3.0		5.5	V
VDD[*2]	1.20		1.35	V
A0VCC A1VCC	3.0		5.5	V
A0VREFH[*3] A1VREFH	3.0		5.5	V

Note: VSS = EnVSS = A0VSS = A1VSS = 0 V

Note 1. VCC and EnVCC should be supplied from the same power source.

Note 2. Applicable only for DPS products.

Note 3. Do not exceed A0VCC or A1VCC.

CAUTION

During operations, supply the specified voltages to all power lines. When stopping operation, turn off all of the power supplies.

3.4 Oscillator Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC}			16		MHz

CAUTION

Oscillation stabilization times differ according to matching with the crystal oscillator. Secure an oscillation stabilization time determined through evaluation of matching.

3.5 Characteristics of High-Speed Internal Oscillator Circuit

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-speed internal oscillator circuit (HS IntOSC) frequency	f_{RH}		15.44	16	16.56	MHz

3.6 PLL Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLLICLK}$			16		MHz
Output frequency (PLL for CPU)	f_{CPLL}	—		160		MHz

3.7 Regulator Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	VCC		3.0		5.5	V
Output voltage	VCL		1.15	1.25	1.35	V
Capacitance	CVCL	Per pin*1	0.07	0.1	0.13	µF

Note 1. For the connection of the VCL pin, see RH850/P1M-E Group User's Manual: Hardware **Section 2.5, DNF**.

3.8 DC Characteristics

3.8.1 Relationship between Power Name and Pin

The table below shows the relationship between power supply names and pins.

Pin Name	Power Supply Name	I/O	Input Buffer Type	Note
JP0_4	VCC	I	SchmittA	5 V tolerant
JP0_2	E1VCC	I	CMOS/SchmittA	
JPx_x other than the above	E1VCC	I/O	CMOS/SchmittB	Output driving ability selectable
P0_10	E1VCC	I/O	CMOS	Output driving ability selectable
Py_y Pins listed in RH850/ P1M-E User's Manual: Hardware **Table 2.34**	EnVCC[*1]	I/O	CMOS/SchmittB	Output driving ability selectable
Pz_z other than the above	EnVCC[*1]	I/O	SchmittB	Output driving ability selectable
ADCG0Ixx	A0VCC	I	Analog (ADC)	
ADCG1Ixx	A1VCC	I	Analog (ADC)	
$\overline{\text{RESET}}$	VCC	I	SchmittA	5 V tolerant
FLMD0	E1VCC	I	SchmittC	5 V tolerant
$\overline{\text{ERROROUT}}$	E0VCC	O	—	
$\overline{\text{CVMOUT}}$	E1VCC	O	—	
X1	VCC	I	—	
X2	VCC	O	—	

Note 1. Regarding the power supply names (E0VCC or E1VCC), please refer to **Table 2.1, Pin Assignment**.

3.8.2 Buffer Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Measuring Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS	3.0 V ≤ EnVCC < 4.3 V	0.65 × EnVCC		EnVCC + 0.3	V
			4.3 V ≤ EnVCC ≤ 5.5 V	0.65 × EnVCC		EnVCC + 0.3	V
		SchmittA	3.0 V ≤ EnVCC < 4.3 V	0.8 × EnVCC 0.8 × VCC		EnVCC + 0.3 VCC + 0.3	V
			4.3 V ≤ EnVCC ≤ 5.5 V	0.75 × EnVCC 0.75 × VCC		EnVCC + 0.3 VCC + 0.3	V
		SchmittB	3.0 V ≤ EnVCC < 4.3 V	0.75 × EnVCC		EnVCC + 0.3	V
			4.3 V ≤ EnVCC ≤ 5.5 V	0.75 × EnVCC		EnVCC + 0.3	V
		SchmittC	3.0 V ≤ EnVCC < 4.3 V	0.75 × EnVCC		EnVCC + 0.3	V
			4.3 V ≤ EnVCC ≤ 5.5 V	0.7 × EnVCC		EnVCC + 0.3	V
Low level input voltage	VIL	CMOS	3.0 V ≤ EnVCC < 4.3 V	–0.3		0.35 × EnVCC	V
			4.3 V ≤ EnVCC ≤ 5.5 V	–0.3		0.35 × EnVCC	V
		SchmittA	3.0 V ≤ EnVCC < 4.3 V	–0.3		0.25 × EnVCC 0.25 × VCC	V
			4.3 V ≤ EnVCC ≤ 5.5 V	–0.3		0.25 × EnVCC 0.25 × VCC	V
		SchmittB	3.0 V ≤ EnVCC < 4.3 V	–0.3		0.4 × EnVCC	V
			4.3 V ≤ EnVCC ≤ 5.5 V	–0.3		0.42 × EnVCC	V
		SchmittC	3.0 V ≤ EnVCC ≤ 5.5V	–0.3		0.3 × EnVCC	V
High level output voltage	VOH	IOH = –3mA[*1]	3.0 V ≤ EnVCC < 4.3 V	EnVCC –1.0			V
			4.3 V ≤ EnVCC ≤ 5.5 V	EnVCC –1.0			V
		IOH = –1mA[*1]	3.0 V ≤ EnVCC < 4.3 V	EnVCC –1.0			V
			4.3 V ≤ EnVCC ≤ 5.5 V	EnVCC –1.0			V
		IOH = –0.1mA[*1]	3.0 V ≤ EnVCC < 4.3 V	EnVCC –0.5			V
			4.3 V ≤ EnVCC ≤ 5.5 V	EnVCC –0.5			V
Low level output voltage	VOL	IOL = 3mA[*1]	3.0 V ≤ EnVCC < 4.3 V			0.6	V
			4.3 V ≤ EnVCC ≤ 5.5 V			0.5	V
		IOL = 1mA[*1]	3.0 V ≤ EnVCC < 4.3 V			0.4	V
			4.3 V ≤ EnVCC ≤ 5.5 V			0.4	V
Pull-up resistance	RU	Other than below VIN = EnVSS	3.0V ≤ EnVCC < 4.3 V	30	60	150	kΩ
			4.3V ≤ EnVCC ≤ 5.5V	20	40	100	kΩ
		FLMD0 VIN = EnVSS	3.0V ≤ EnVCC < 4.3V	10	19	50	kΩ
			4.3V ≤ EnVCC ≤ 5.5V	10	19	50	kΩ
Pull-down resistance	RD	Other than below VIN = EnVCC	3.0 V ≤ EnVCC < 4.3 V	15	40	125	kΩ
			4.3 V ≤ EnVCC ≤ 5.5 V	15	40	100	kΩ
		$\overline{\text{RESET}}$, FLMD0 VIN = EnVCC	3.0 V ≤ EnVCC < 3.6 V	20	60	150	kΩ
			3.6 V ≤ EnVCC < 4.3 V	20	60	150	kΩ
			4.3 V ≤ EnVCC ≤ 5.5 V	20	40	100	kΩ
Input leak current	ILIH1	Other than below	Vin = VCC, EnVCC			2	µA
		ADCGnIm (n = 0,1, m = 0 to 11)	Vin = A0VCC, A1VCC When AD conversion is not performed:			0.2	µA
	ILIL1	Other than below	Vin = 0 V			–2	µA
		ADCGnIm (n = 0,1, m = 0 to 11)	Vin = 0 V When AD conversion is not performed:			–0.2	µA
Hysteresis width	VH	SchmittA			0.27 × EnVCC		V
		SchmittB			0.1 × EnVCC		V
		SchmittC			0.2 × EnVCC		V

Note 1. Total load current is 48 mA for the pins when everything is switched on at the same time. However, the total load current must be no greater than 12 mA for pins 38 to 53 on 100-pin devices and no greater than 30 mA for pins 52 to 82 on 144-pin devices.

3.8.3 Allowable Output Current

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	MIN.	TYP.	MAX.	Unit
Output high-level allowable current (per pin)	I_{OH}			–3	mA
Output high-level allowable current (total)*1	ΣI_{OH}			–48	mA
Output low-level allowable current (per pin)	I_{OL}			3	mA
Output low-level allowable current (total)*1	ΣI_{OL}			48	mA

Note 1. Total load current is 48 mA for the pins when everything is switched on at the same time. However, the total load current must be no greater than 12 mA for pins 38 to 53 on 100-pin devices and no greater than 30 mA for pins 52 to 82 on 144-pin devices.

CAUTION

This item affects the calorific value and Tj of the chip. In addition to these restrictions, take thermal design into consideration.

3.8.4 Injection Current

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item		Symbol	MIN.	TYP.	MAX.	Unit
DC injection current (per pin)	Digital pin	IINJ_DIN	–2		2	mA
	Analogue pin	IINJ_AIN	–3		3	mA
DC injection current (Total)		IINJ_TOT	–50		50	mA

3.8.5 Input Capacitance

Conditions: See **Section 3.1.1.1, Common Conditions**. As for temperature conditions, refer measurement conditions.

Item	Symbol	MIN.	TYP.	MAX.	Unit	Measuring Condition
Input capacitance	CI			10	pF	f = 1 MHz Pins not to be measured: 0 V Tj = 25°C
Input/output capacitance	CIO			10	pF	
Output capacitance	CO			10	pF	
Input capacitance for X1	CX1			20	pF	

NOTE

For the analogue input pins (ADCGnlm), see the description of the equal input capacitance in related **Section 3.14, A/D Converter Characteristics**.

3.8.6 Power Current Characteristics

Table 3.1 Power Current of eVR Product

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item		Symbol	MIN.	TYP.	MAX.	Unit
VCC power current[*1]	RUN mode	IVCCEVR			230	mA
	When BIST is executed	IVCCBEVR			230	mA
	When rewriting flash memory[*2]	IVCCFEVR			230	mA
AnVCC power current		IAVCC			6.5	mA
AnVREFH current		IAVREF			0.5	mA

Note 1. The MAX. value includes the operating current of peripheral devices. However, the current in A/D converter, I/O port, or on-chip pull-up/-down resistor is not included.

Note 2. This is the value of the power current when rewriting code flash memory or data flash memory.

Table 3.2 Power Current of DPS Product

Conditions: See **Section 3.1.1.1, Common Conditions.**

Item		Symbol	MIN.	TYP.	MAX.	Unit
VDD power current[*1]	RUN mode	IVDDDPS			210	mA
	When BIST is executed	IVDDBDPS			210	mA
	When rewriting flash memory[*2]	IVDDFDPS			185	mA
VCC power current	RUN mode	IVCCDPS			20	mA
	When BIST is executed	IVCCBDPS			20	mA
	When rewriting flash memory[*2]	IVCCFDPS			45	mA

Note 1. The MAX. value includes the operating current of peripheral devices. However, the current in A/D converter, I/O port, or on-chip pull-up/-down resistor is not included.

Note 2. This is the value of the power current when rewriting code flash memory or data flash memory.

Note 3. AnVCC and AnVREFH current are the same as those of the eVR products.

3.9 AC Characteristics

3.9.1 Power UP/Down Timing

Table 3.3 eVR Products

Conditions: See **Section 3.1.1.1, Common Conditions**.

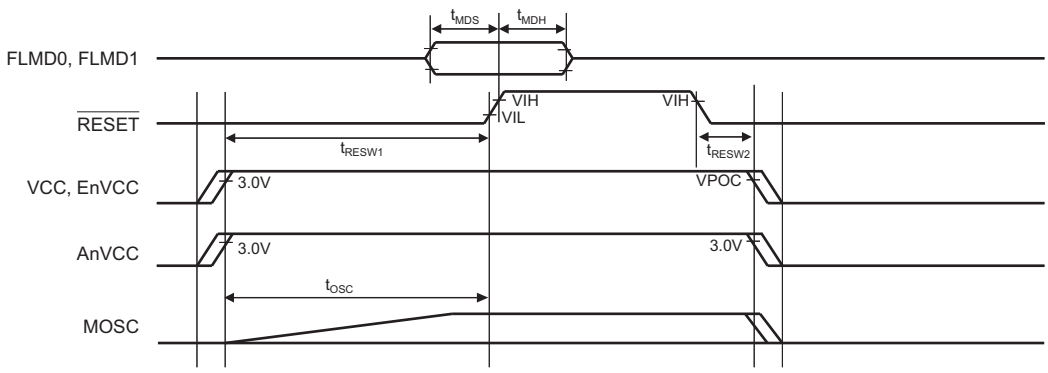
Item	Symbol	MIN.	MAX.	Unit	Remarks
Pin reset time at low level for power on	t_{RESW1}	10		ms	*1
Pin reset time at low level for power off	t_{RESW2}	2		µs	*2
Operating mode setup time	t_{MDS}	1		ms	
Operating mode hold time	t_{MDH}	1		ms	
VCC/AnVCC voltage ramp	t_{VS1}	0.02	500	V/ms	

Note 1. t_{RESW1} is the time over which assertion of the reset signal is required to continue until the supply of internal clock signals becomes stable after all power supplies have been turned on. Release the pin reset after the periods of t_{RESW1} and t_{OSC} have elapsed. VCC and EnVCC should be supplied from the same source. No restriction applies to potential differences between the levels of the VCC/EnVCC supplies and the AnVCC supply during power up.

Note 2. t_{RESW2} is the time over which assertion of the reset signal is required until either of the power voltages has dropped below the lower limit.

Note 3. The states of I/O pins are not reset during the noise cancellation interval (max. 1.2 µs) of the reset signal following its assertion while power is being turned off. During that time, do not allow any input of mid-range potential to a pin or the contention of output data.

Note 4. If the power is turned off during the programming or erasure of flash memory, the data in the area that was programmed or erased cannot be guaranteed.



Note: t_{OSC}: OSC oscillation stabilization time

Figure 3.1 Power UP/Down Timing: eVR Products

Table 3.4 DPS Products

Conditions: See **Section 3.1.1.1, Common Conditions**.

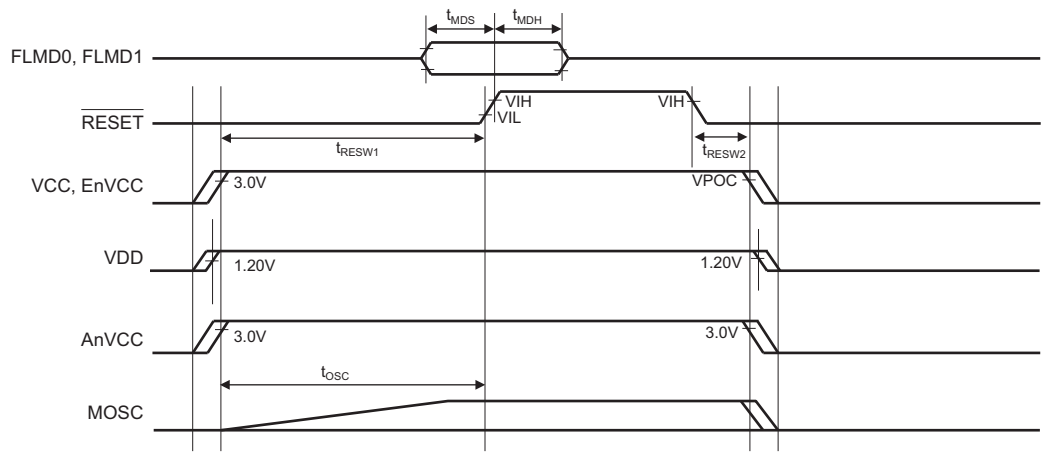
Item	Symbol	MIN.	MAX.	Unit	Remarks
Pin reset time at low level for power on	t_{RESW1}	10		ms	*1
Pin reset time at low level for power off	t_{RESW2}	2		µs	*2
Operating mode setup time	t_{MDS}	1		ms	
Operating mode hold time	t_{MDH}	1		ms	
VCC/AnVCC voltage ramp	t_{VS1}	0.02	500	V/ms	
VDD voltage ramp	t_{VS2}	2	500	V/ms	

Note 1. t_{RESW1} is the time over which assertion of the reset signal is required to continue until the supply of internal clock signals becomes stable after all power supplies have been turned on. Release the pin reset after the periods of t_{RESW1} and t_{OSC} have elapsed. VCC and EnVCC should be supplied from the same source. No restriction applies to potential differences between the levels of the VCC/EnVCC supplies, the AnVCC supply, and the VDD supply during power up.

Note 2. t_{RESW2} is the time over which assertion of the reset signal is required until either of the power voltages has dropped below the lower limit.

Note 3. The states of I/O pins are not reset during the noise cancellation interval (max. 1.2 µs) of the reset signal following its assertion while power is being turned off. During that time, do not allow any input of mid-range potential to a pin or the contention of output data.

Note 4. If the power is turned off during the programming or erasure of flash memory, the data in the area that was programmed or erased cannot be guaranteed.



Note: t_{OSC}: OSC oscillation stabilization time

Figure 3.2 Power UP/Down Timing: DPS Products

3.9.2 Driving Ability

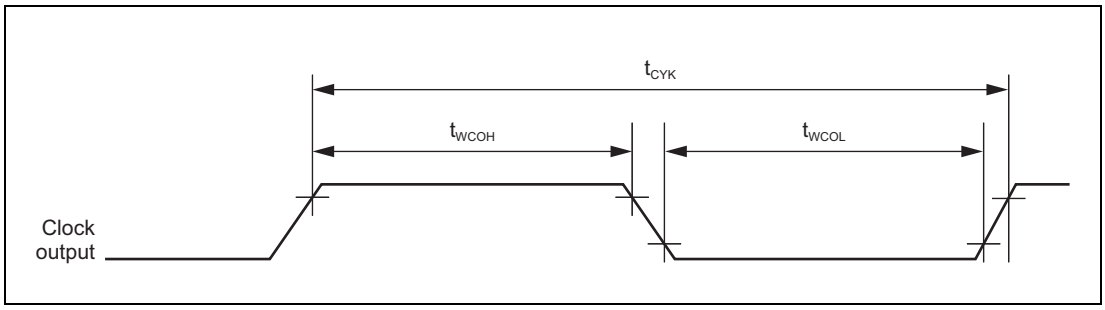
Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output frequency		High-speed mode			20	MHz
		Medium-speed mode			14	MHz
		Low-speed mode			4	MHz
Output rising/falling time		High-speed mode			10	ns
		Medium-speed mode			20	ns
		Low-speed mode			50	ns

3.9.3 Clock Output Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.
Output pin are the fast mode.

Item	Symbol	MIN.	TYP.	MAX.	Unit
Clock output cycle time	t_{CYK}	50 (20MHz)			ns
Clock output high level width	t_{WCOH}	$t_{CYK}/2 - 12$			ns
Clock output low level width	t_{WCOL}	$t_{CYK}/2 - 12$			ns

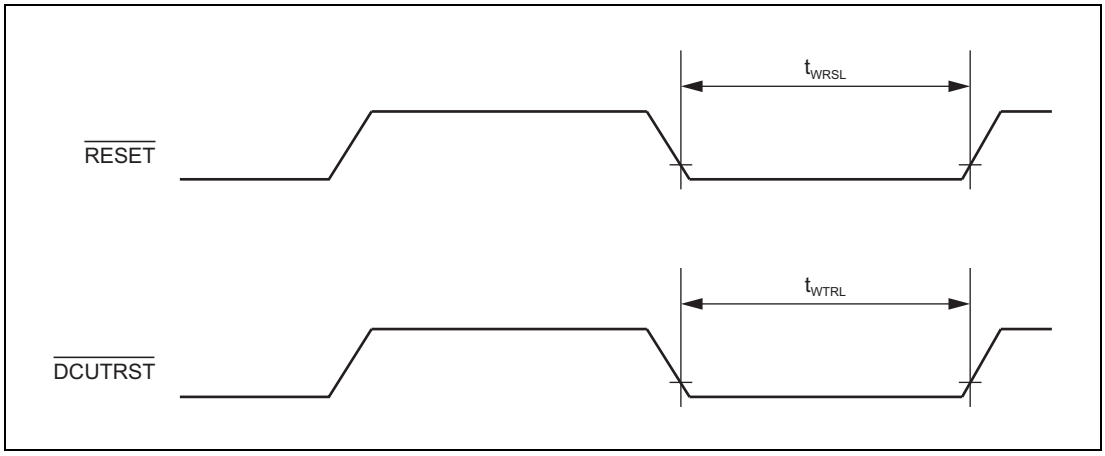


3.9.4 Control Signal Timing

3.9.4.1 Reset

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}	Other than power-on	1.5	—	—	µs
$\overline{\text{DCUTRST}}$ input low level width	t_{WTRL}		1.5	—	—	µs



3.9.4.2 Interrupts/ADTRG

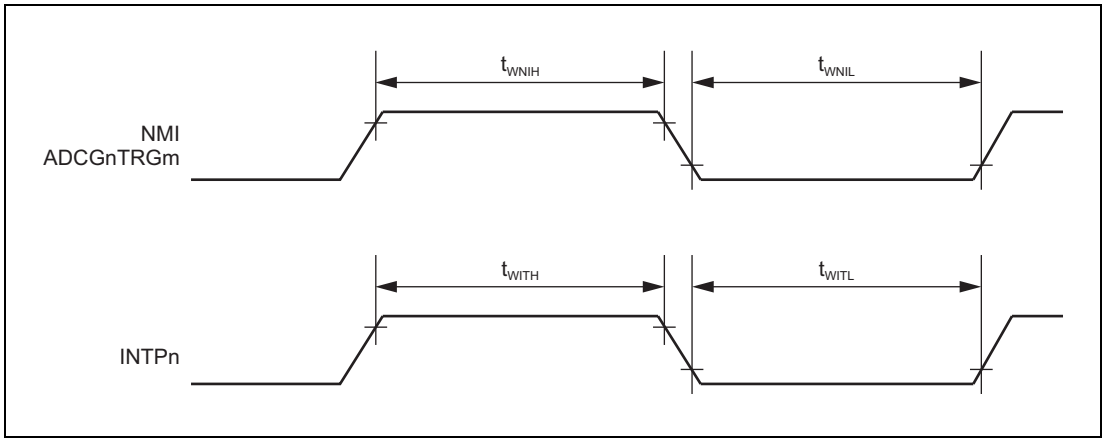
Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}	Digital filter	k × Tsamp + 20[*1]			ns
NMI input low level width	t_{WNIL}	Digital filter	k × Tsamp + 20[*1]			ns
INTPn input high level width	t_{WITH}	Digital filter	k × Tsamp + 20[*1]			ns
		Analog filter, n = 7, 8	600			ns
INTPn input low level width	t_{WITL}	Digital filter	k × Tsamp + 20[*1]			ns
		Analog filter, n = 7, 8	600			ns
ADCGnTRGm input high level width	t_{WNIH}	Digital filter, n = 0,1, m = 0, 1	k × Tsamp + 20[*1]			ns
ADCGnTRGm input low level	t_{WNIL}	Digital filter, n = 0, 1, m = 0, 1	k × Tsamp + 20[*1]			ns

Note 1. k is the number of samples taken by the digital noise filter for the input.
Tsamp is the sampling interval of the digital noise filter for the input.

CAUTION

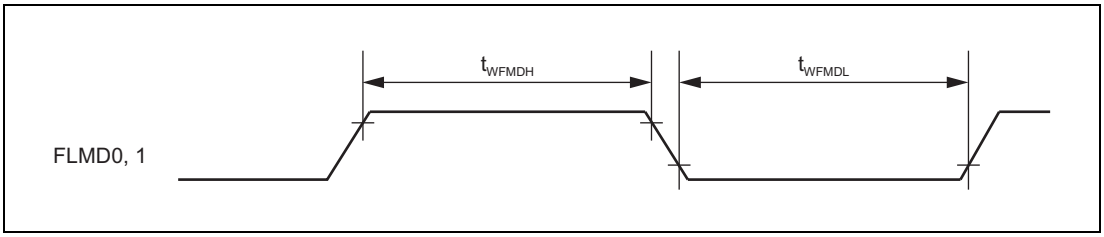
The specifications above indicate the pulse width to be always detected as an effective edge. Even when a pulse width smaller than above is input, such value may be detected as an effective edge.



3.9.4.3 Mode

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0,1 input high level width	t_{WFMDH}		600			ns
FLMD0,1 input low level width	t_{WFMDL}		600			ns



3.9.5 Timer Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high/low level width (n = 3, m = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		k × Tsamp + 20[*1]			ns
TAUJnIm input high/low level width (n = 3, m = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		k × Tsamp + 20[*1]			ns
ENCAnTINm input high/low level width (n = 0, 1; m = 0, 1)	t_{WTDIH}/ t_{WTDIL}		k × Tsamp + 20[*1]			ns
ENCAnEm input high/low level width (n = 0, 1, m = 0, 1, C)	t_{WENIH}/ t_{WENIL}		k × Tsamp + 20[*1]			ns
TSG3nPTSIm input high/low level width (n = 0, 1, m = 0, 1, 2)	t_{WTSPIH}/ t_{WTSPIL}		k × Tsamp + 20[*1]			ns
TSG3nCLKI input high/low level width (n = 0, 1)	t_{WTSCIH}/ t_{WTSCIL}		k × Tsamp + 20[*1]			ns
TAPAnESO input high/low level width (n = 0, 1)	t_{WESIH}/ t_{WESIL}		600			ns

Note 1. k is the number of samples taken by the digital noise filter for the input.
Tsamp is the sampling interval of the digital noise filter for the input.

3.9.6 CSI Timing

3.9.6.1 CSIG Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.
Output are specified for buffer "fast mode".

Table 3.5 CSIG Timing (Master Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		125			ns
CSIGnSC high level width	t_{KWHMGn}		t_{KCYMGn} /2 – 12			ns
CSIGnSC low level width	t_{KWLMGn}		t_{KCYMGn} /2 – 12			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay time (vs. CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	2 × t_{KCYGn} + 25			ns

Table 3.6 CSIG Timing (Slave Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		150			ns
CSIGnSC high level width	t_{KWHSGn}		t_{KCYSGn} /2 – 12			ns
CSIGnSC low level width	t_{KWLSGn}		t_{KCYSGn} /2 – 12			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSISGn}		t_{KCYGn} + 5			ns
CSIGnSO output delay time (vs. CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay time (vs. CSIGnSC)	t_{SRYOGn}				38	ns

3.9.6.2 CSIH Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.
Output are specified for buffer "fast mode".

Table 3.7 CSIH Timing (Master Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		$t_{KCYMHn}/2 - 12$			ns
CSIHnSC low level width	t_{KWLMHn}		$t_{KCYMHn}/2 - 12$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSIMHn}		25			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSIMHn}		0			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	$2 \times t_{KCYMHn} + 25$			ns
CSIHnCSS0 to CSIHnCSS7 inactive level width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 20			ns
CSIHnCSS0 to CSIHnCSS7 setup time (vs. CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAPx = 0	CSSETUP × t_{KCYMHn} – 10			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAPx = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 10			ns
CSIHnCSS0 to CSIHnCSS7 hold time (vs. CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSHOLD × t_{KCYMHn} – 10			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSHOLD + 0.5) × t_{KCYMHn} – 10			ns

Note: CSSETUP: The values set in CSIHnCFGx.CSIHnSPx[3:0]
CSHOLD: The values set in CSIHnCFGx.CSIHnHDx[3:0]
CSIDLE: The value set in CSIHnCFGx.CSIHnIDx[2:0]

Table 3.8 CSIH Timing (Slave Mode)

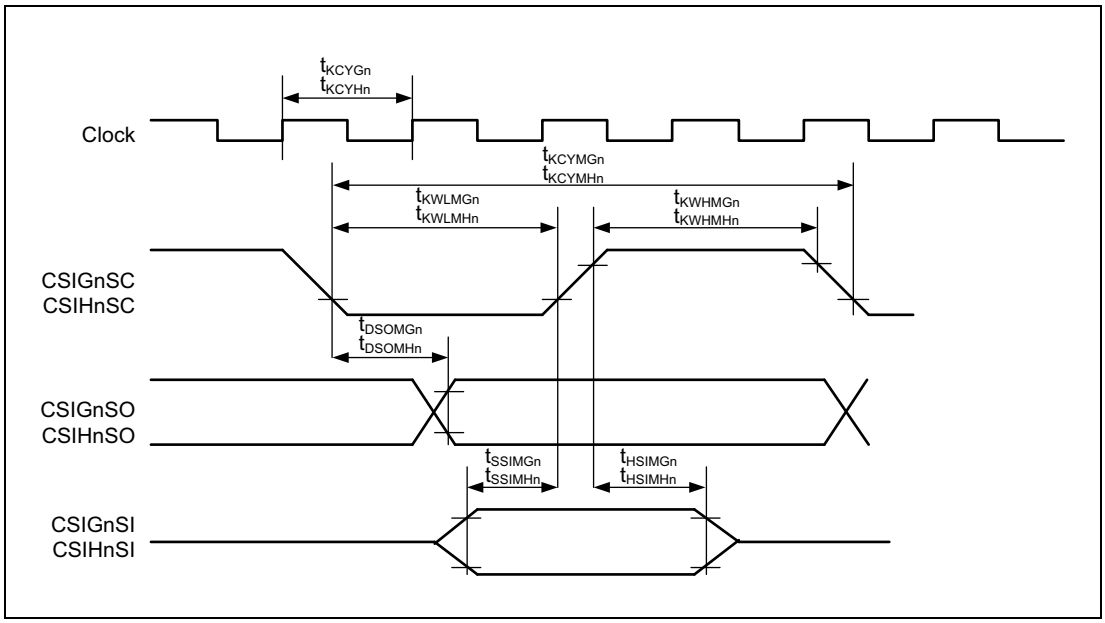
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		150			ns
CSIHnSC high level width	t_{KWHSHn}		$t_{KCYSHn}/2 - 12$			ns
CSIHnSC low level width	t_{KWLSHn}		$t_{KCYSHn}/2 - 12$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay time (vs. CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay time (vs. CSIHnSC)	t_{SRYOHn}				38	ns
CSIHnSSI setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$t_{KCYSHn}/2 - 5$			ns
CSIHnSSI hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 30$			ns

3.9.6.3 CSIG/CSIH Timing Charts

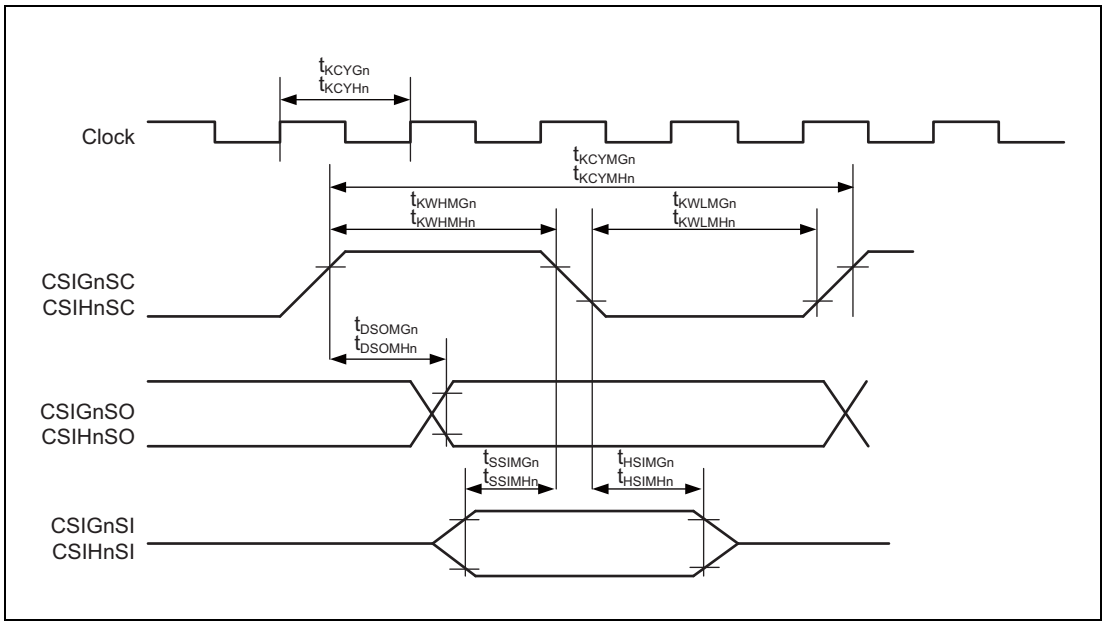
(1) SCKO/SI/SO

Master Mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



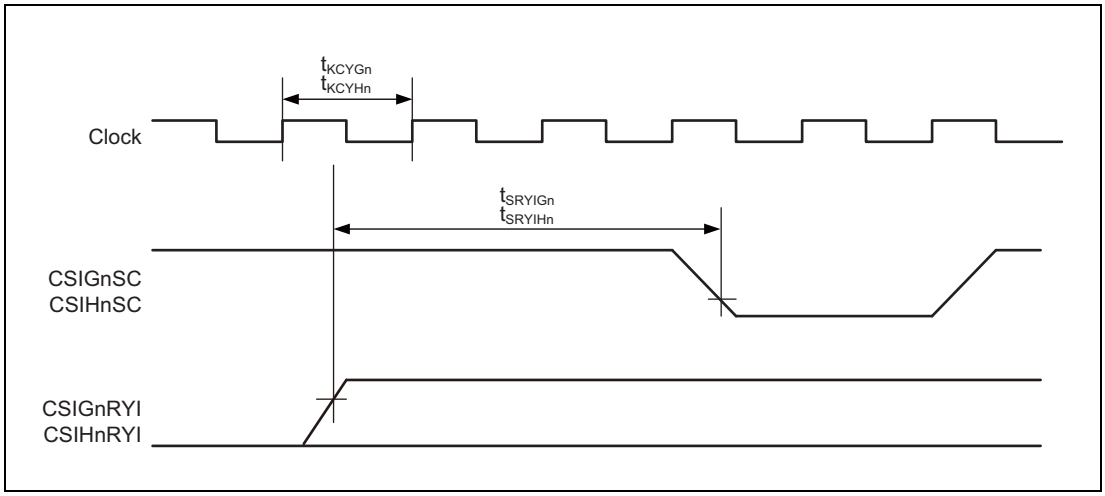
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



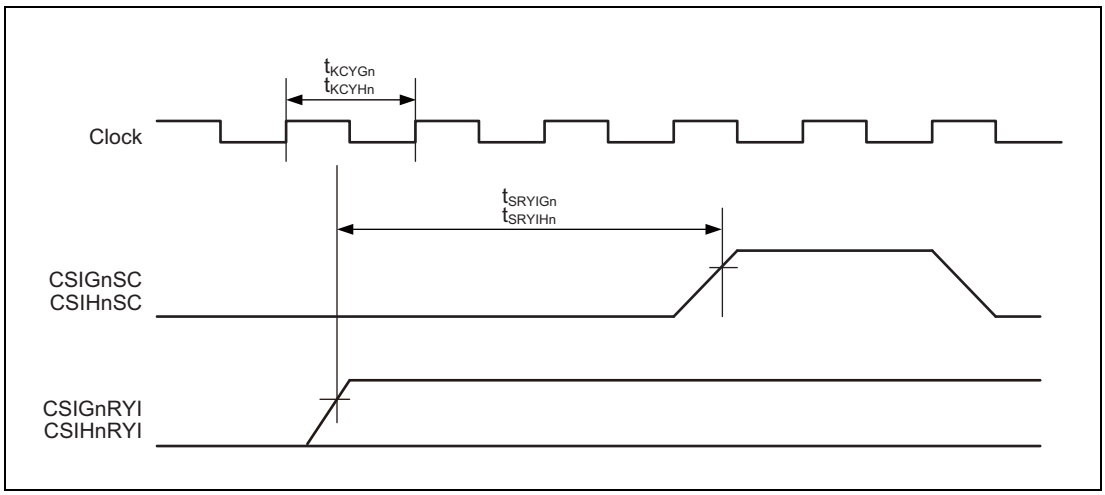
(2) RYI

- CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)
- CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

  – CSIG (CSIGnCTL1: CSIGnCKR = 0)
  – CSIH (CSIHnCFGx: CSIHnCKPx = 0)



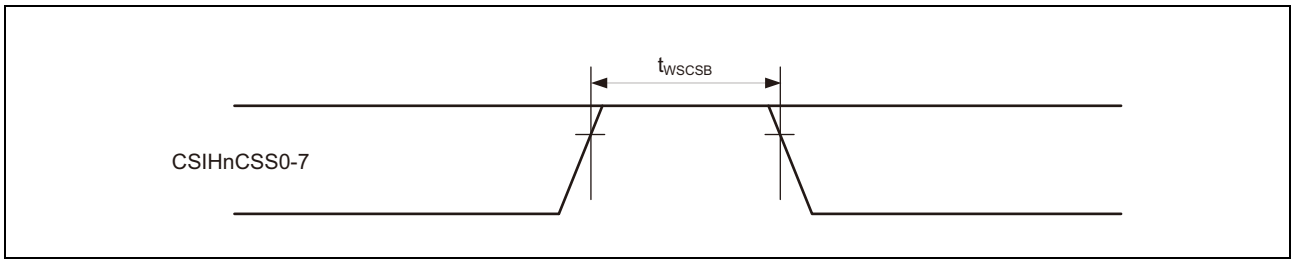
  – CSIG (CSIGnCTL1: CSIGnCKR = 1)
  – CSIH (CSIHnCFGx: CSIHnCKPx = 1)



(3) CSSn

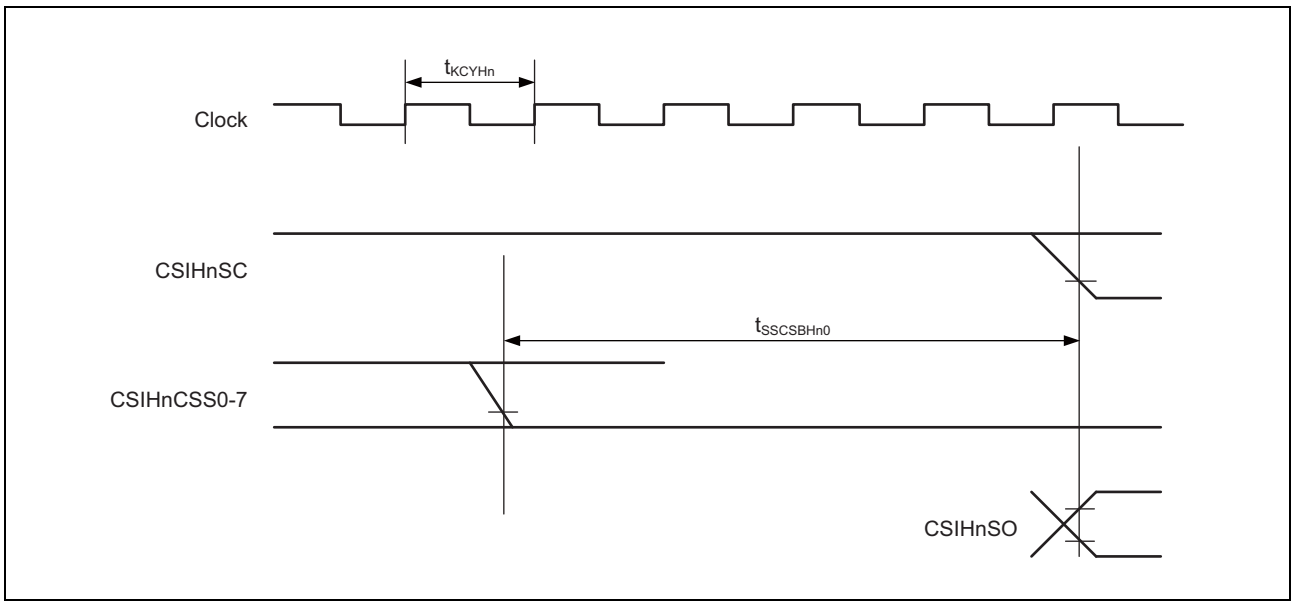
Only Master Mode (Inactive Level Width):

- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0

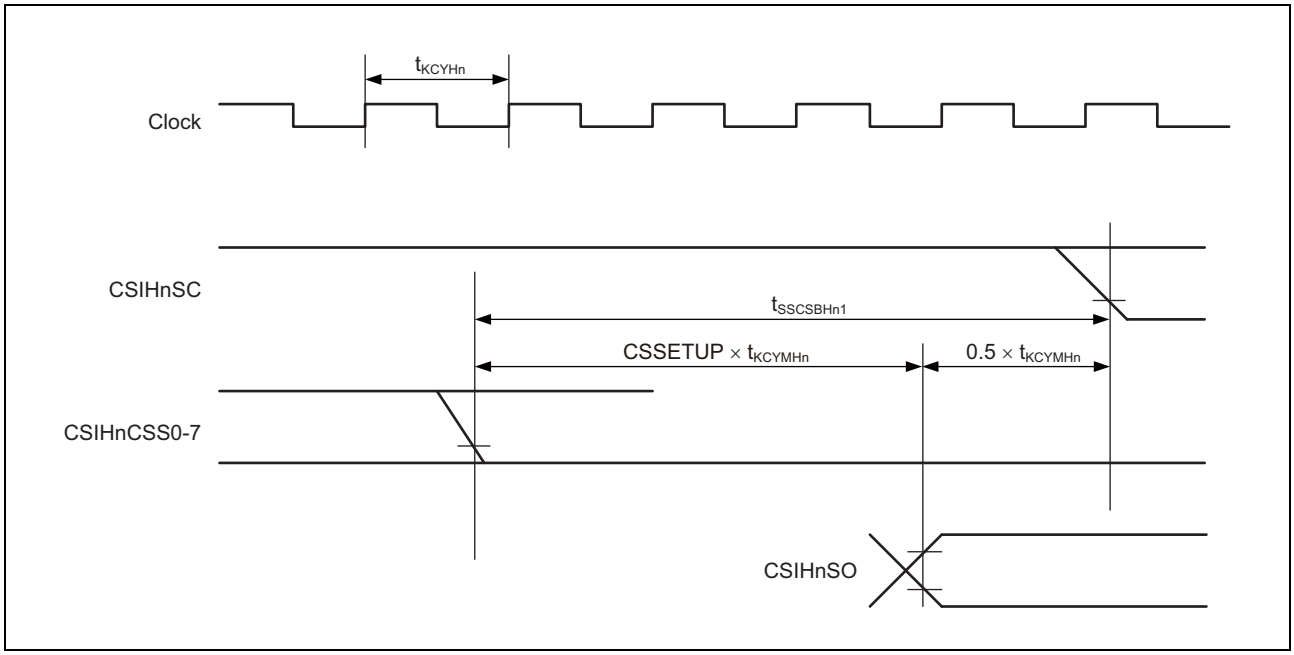


Only Master Mode (Setup Time):

- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0

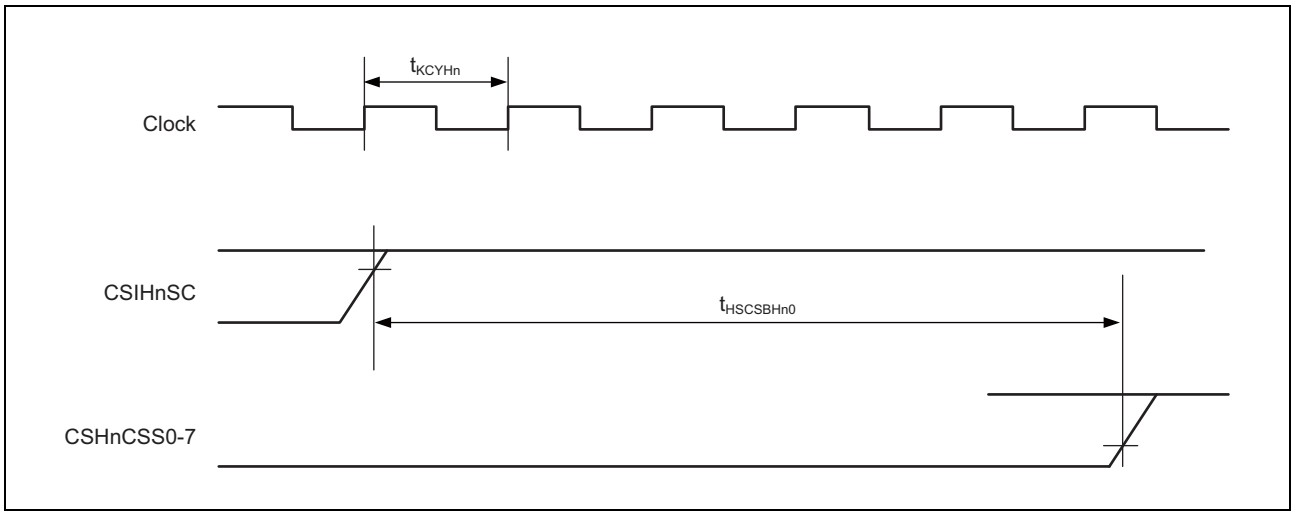


- CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 1

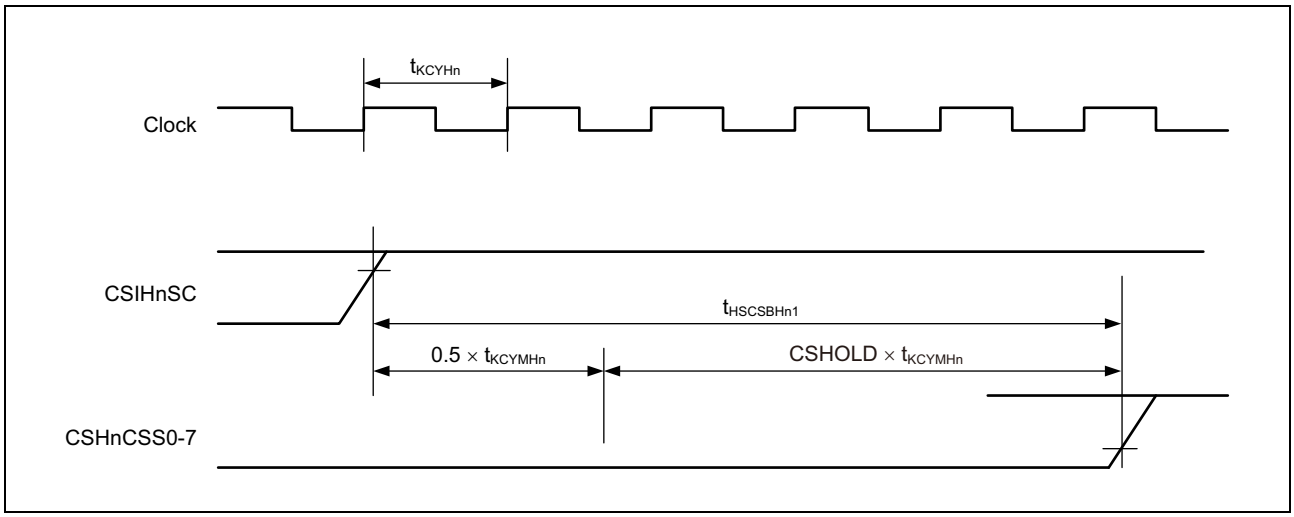


Only Master Mode (Hold Time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



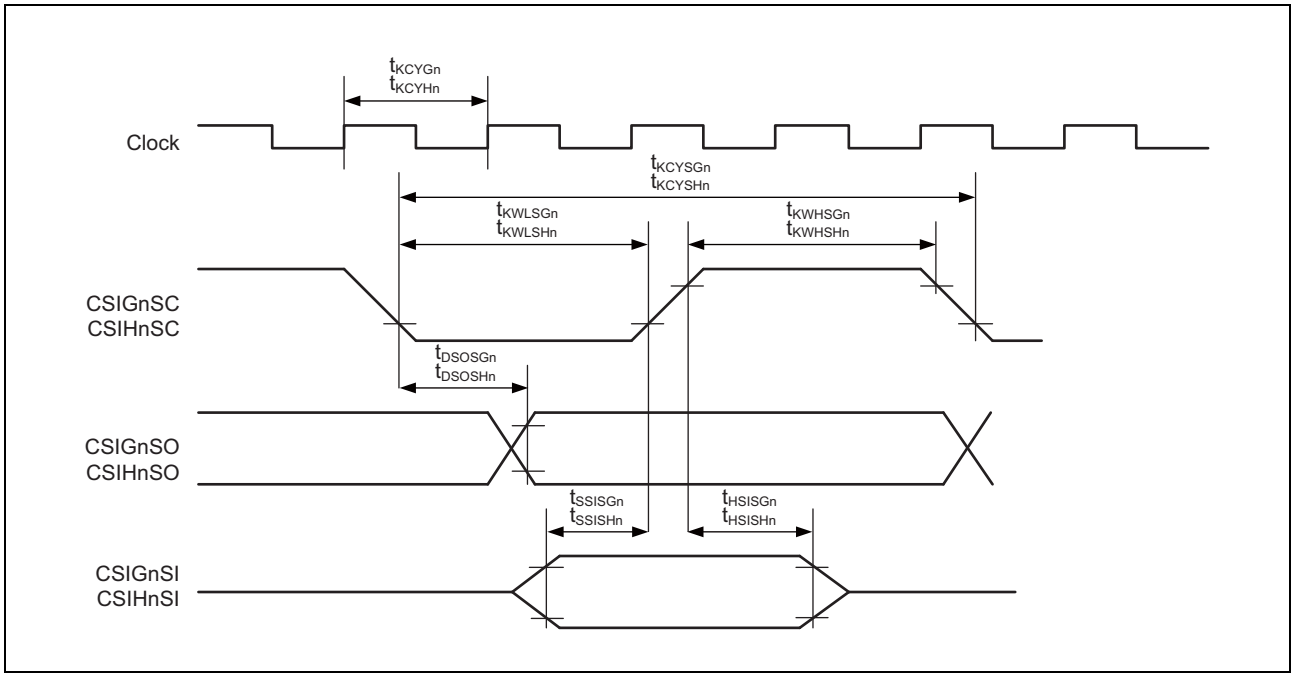
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGx: CSIHnCKPx = 0, CSIHnCFGx: CSIHnDAPx = 0



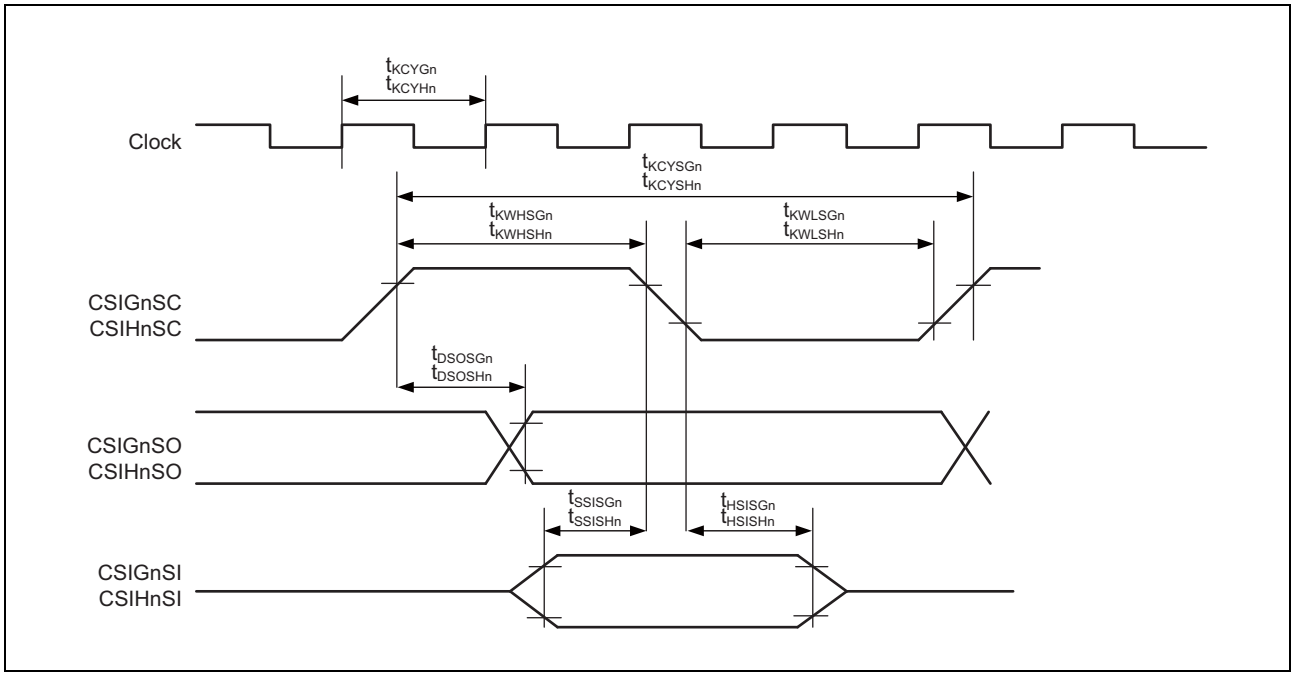
(4) SCKO/SI/SO

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP = 0/0 or 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)

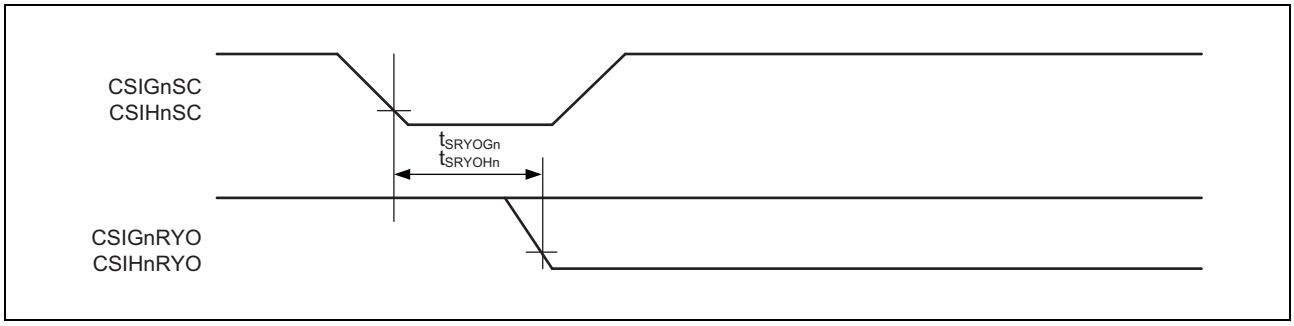


- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP = 1/0 or 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)

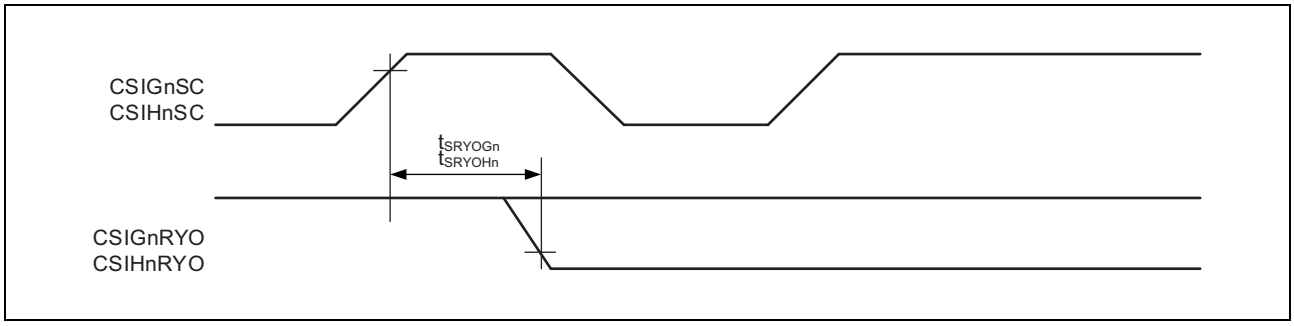


(5) RYO

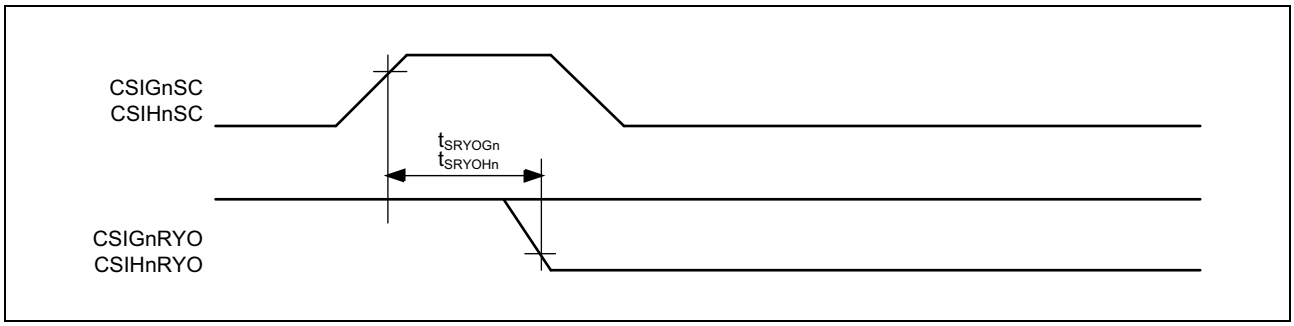
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0)



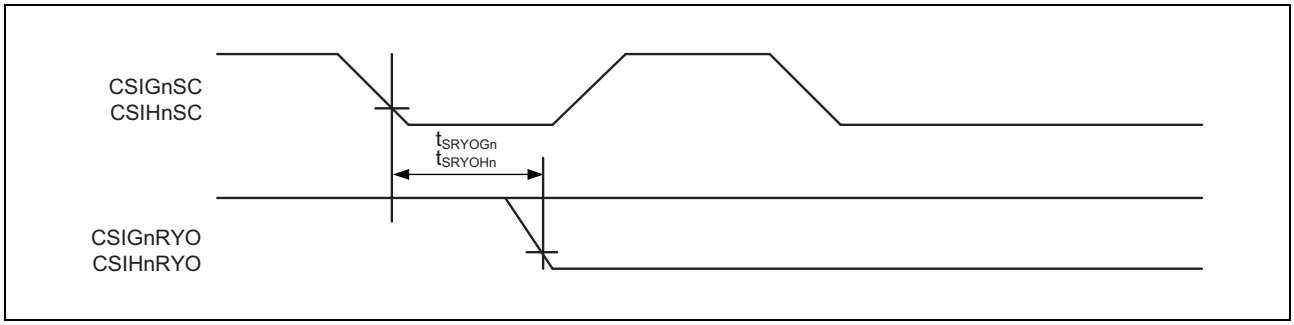
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP = 0/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/1)



- CCSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP = 1/0)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0)



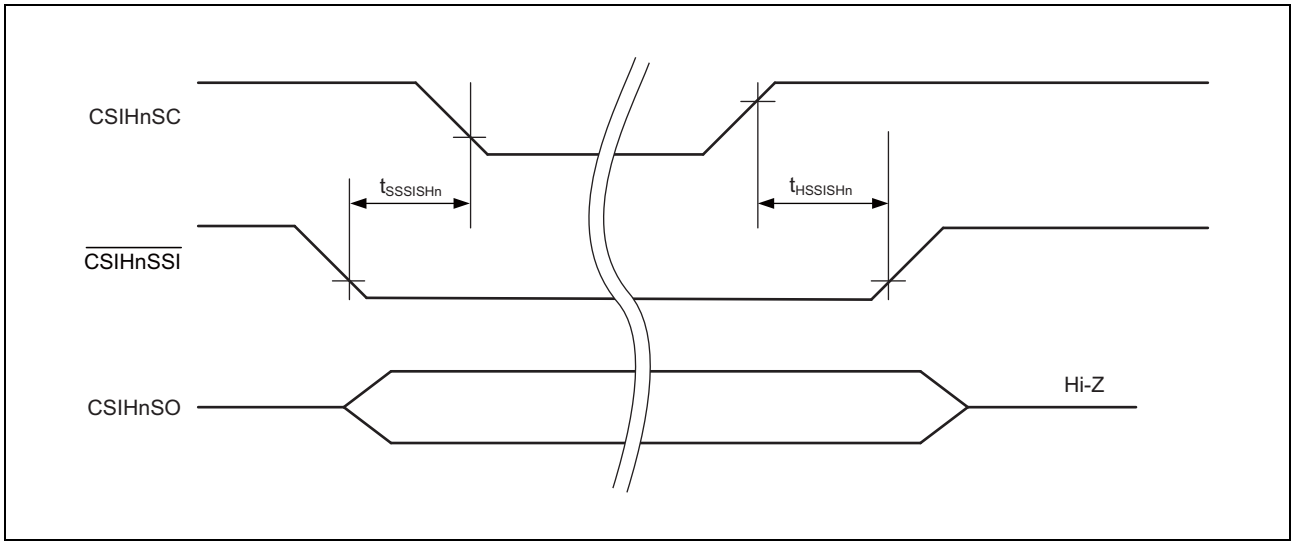
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP = 1/1)
- CSIH (CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/1)



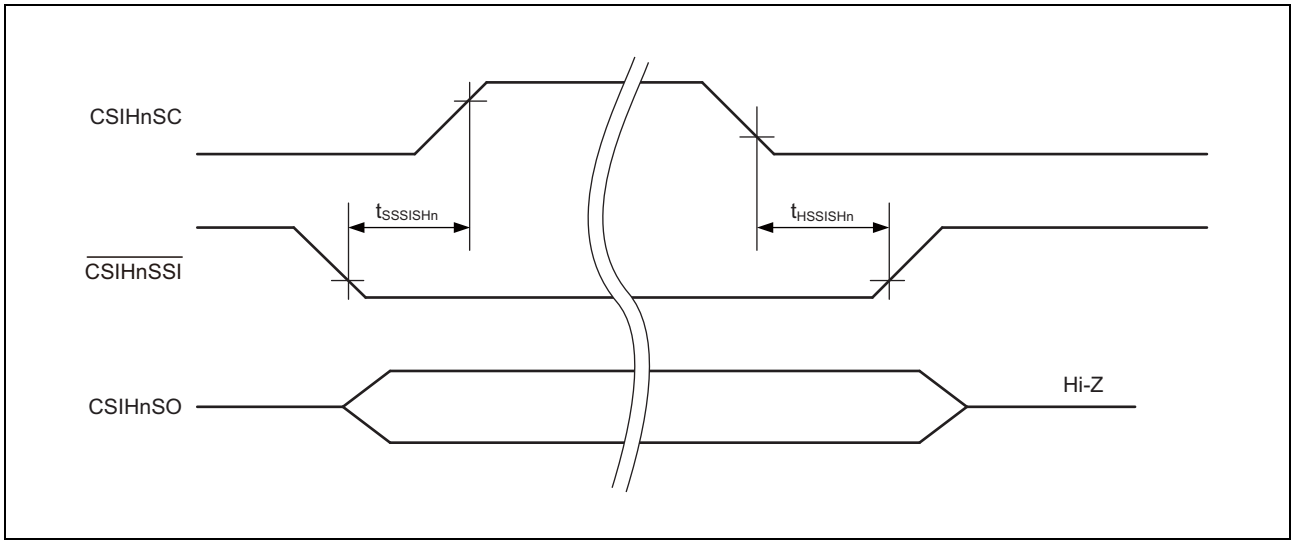
(6) SSI

Slave Mode:

- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 0/0 or 1/1)



- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGx: CSIHnCKPx/CSIHnCFGx: CSIHnDAPx = 1/0 or 0/1)



3.9.7 SCI3 Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.
Output pin are specified for buffer “fast mode".

Table 3.9 SCI3 Timing (Master Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output cycle time	t_{Scyc}	Asynchronous	16 × t_{PCLK}			ns
		Clock synchronous	16 × t_{PCLK}			ns
Output clock pulse width	t_{SCKW}		0.4 × t_{Scyc}		0.6 × t_{Scyc}	ns
Transmit data delay time	t_{TXD}				40	ns
Receive data setup time	t_{RXS}	Clock synchronous	2 × t_{PCLK}			ns
Receive data hold time	t_{RXH}	Clock synchronous	2 × t_{PCLK}			ns

Note: t_{PCLK} is the operating clock of SCI3.

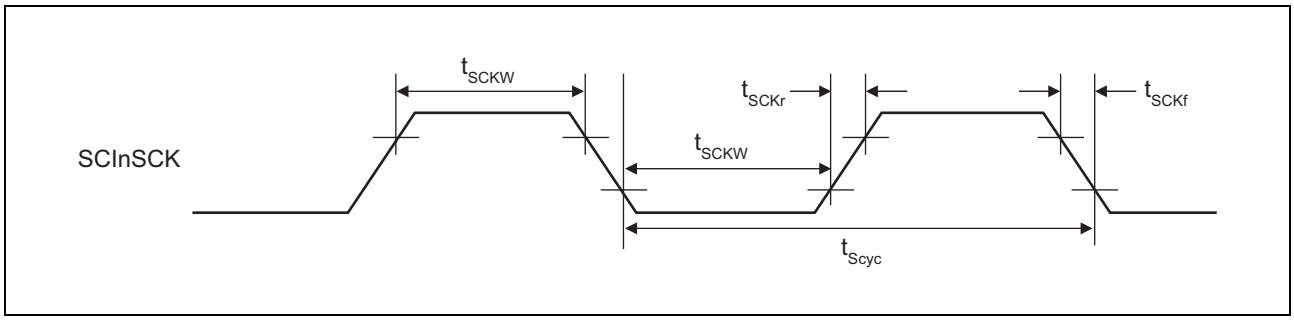


Figure 3.3 SCI Clock Input/Output Timing

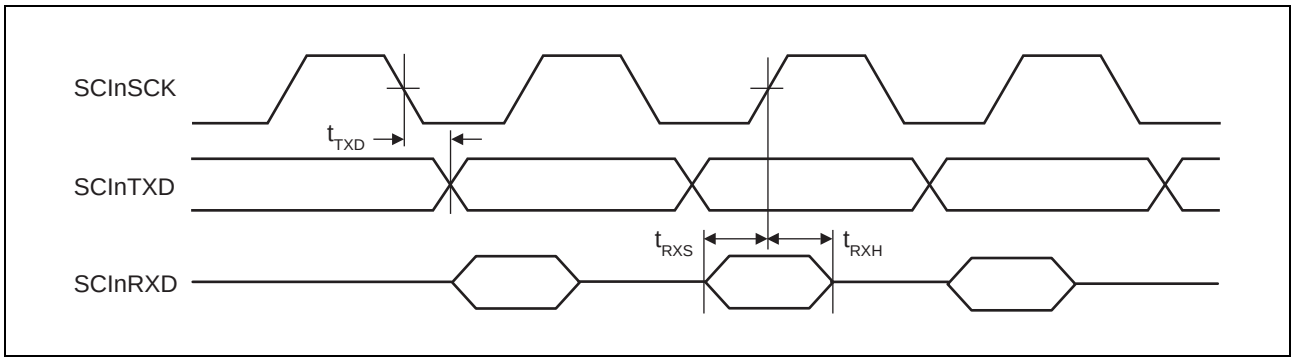


Figure 3.4 SCI Input/Output Timing, Clock Synchronous Mode (in Master Mode)

Table 3.10 SCI3 Timing (Slave Mode)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Input cycle time	t_{Scyc}	12 × t_{PCLK}			ns
Input clock pulse width	t_{SCKW}	0.4 × t_{Scyc}		0.6 × t_{Scyc}	ns
Transmit data delay time*1	t_{TXD}	2 × t_{PCLK}		50 + 3 × t_{PCLK}	ns
Input clock rising time	t_{SCKr}			20	ns
Input clock falling time	t_{SCKf}			20	ns
Receive data setup time	t_{RXS}	2 × t_{PCLK}			ns
Receive data hold time	t_{RXH}	2 × t_{PCLK}			ns

Note 1. This does not apply to transmission of Data 0 (the first bit), which is not transferred in continuous transfer mode.
Transmission of Data 0 (the first bit), which is not transferred in continuous transfer mode, starts when TDRE becomes 0.

Note: t_{PCLK} is the operating clock of SCI3.

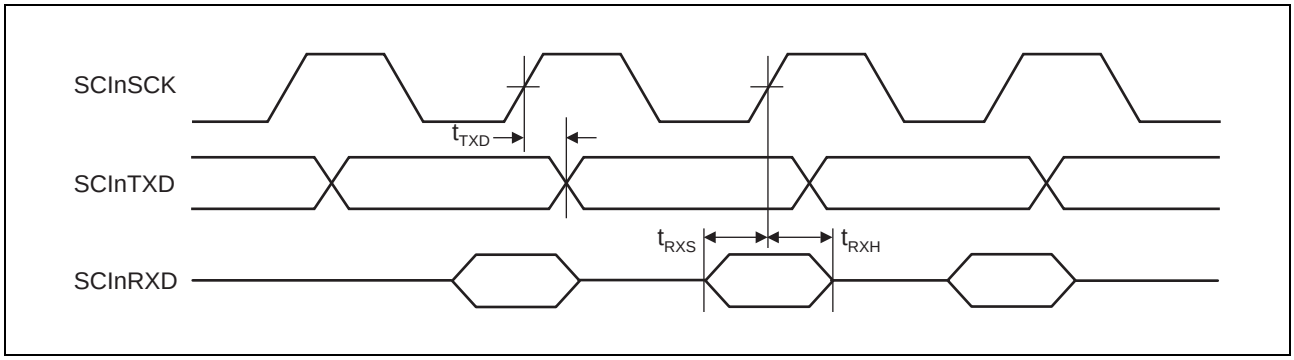
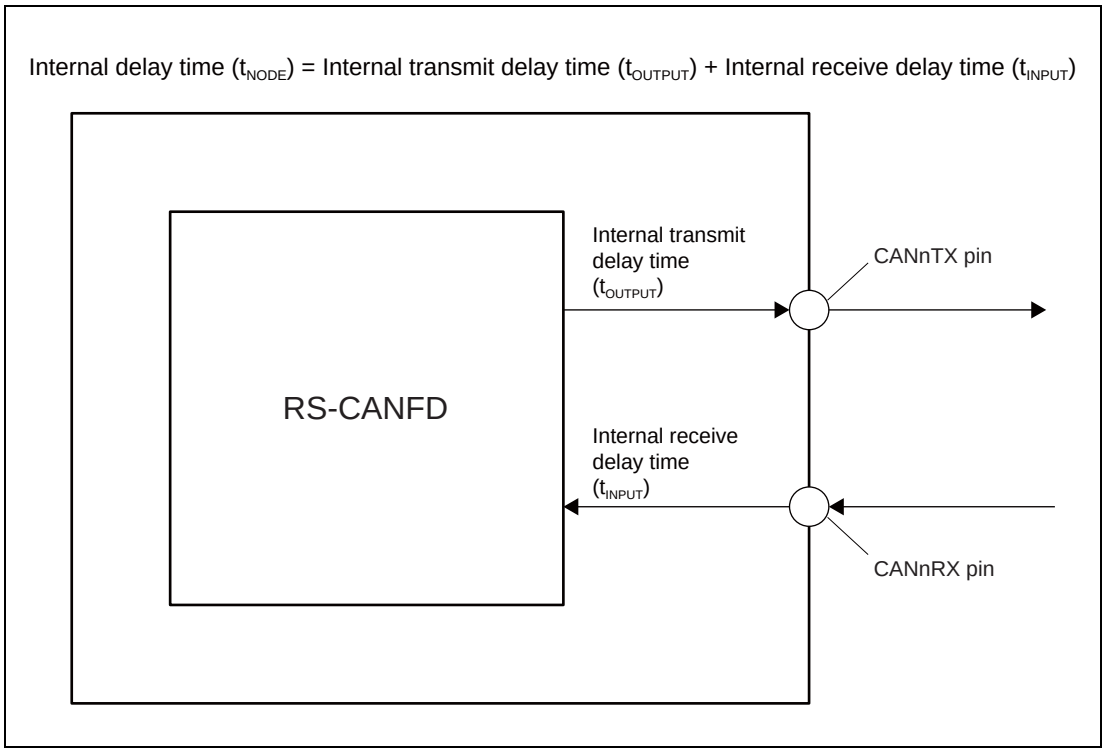


Figure 3.5 SCI Input/Output Timing, Clock Synchronous Mode (in Slave Mode)

3.9.8 RS-CANFD Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.
Output signals are specified for the buffer “fast mode” and “middle mode”.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Internal delay time	t_{NODE}				50	ns
Transfer rate		CAN FD arbitration and CAN 2.0B			1	Mbps
		CAN FD data phase			8	Mbps



3.9.9 RLIN3 Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN function	1		20	Kbps
		UART function			8	Mbps

3.9.10 FlexRay Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.
Output signals are specified for the buffer “fast mode”.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					10	Mbps

3.9.11 PSI5 Timing

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bit time	(1)	125 Kbps	7.6	8.0	8.4	µs
	(2)	189 Kbps	5.0	5.3	5.6	µs
	(3)	250 Kbps		4.0		µs
Gap time	(4)	125 Kbps	8.4			µs
	(5)	189 Kbps	5.6			µs
	(6)	250 Kbps	2.0			µs

3.9.12 RSENT Timing

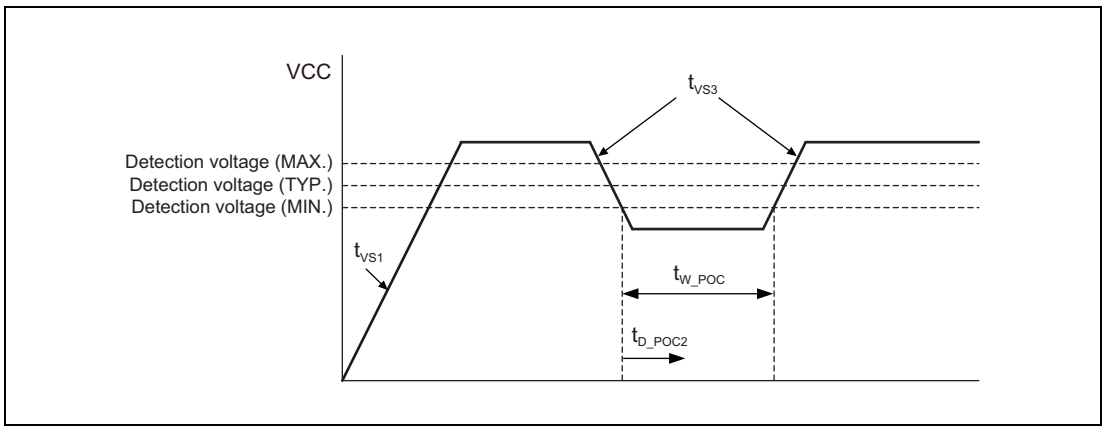
Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Tick Time			1		90	µs

3.10 POC Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOC	Rising	2.7	2.85	3.0	V
		Falling	2.7	2.8	2.9	V
Response time 2	t_{D_POC2}	After power on Voltage ramp (t_{VS3}) = 0.02 V/ms to 20 V/ms			2	ms
VCC minimum width	t_{W_POC}		0.2			ms
VCC voltage ramp	t_{VS3}		0.02		20	V/ms



3.11 Core Voltage Monitor Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High VDD Detection voltage	VCVMH		1.35	1.40	1.45	V
Low VDD Detection voltage	VCVML		1.10	1.15	1.20	V
Response time	t_{D_CVM}				12	µs

3.12 Temperature Sensor

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Temperature precision		Tj = +25 to +150°C	–6		6	°C
		Tj = –40 to +25°C	–12		12	°C
Operation stabilization waiting time	t_{TSSB}		200			µs

3.13 BIST Execution Time

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
BIST execution time					30	ms

3.14 A/D Convertor Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Macro operation clock						40	MHz
Resolution	RESn				12		bit
Conversion time	t_{CONn}	ADCGnSMPCR = 0000_H, CLK_ADC = 40 MHz			1		µs
Total errors[*1]	TOEn	AnVCC, AnVREFH = 4.3 V to 5.5 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±4.0	LSB
			ADCGnIm, When channel T&H is used			±6.0	LSB
		AnVCC, AnVREFH = 3.0 V to 4.3 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±6.0	LSB
			ADCGnIm, When channel T&H is used			±8.0	LSB
Integral nonlinear [*1]	ILEn	AnVCC, AnVREFH = 4.3 V to 5.5 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±2.0	LSB
			ADCGnIm, When channel T&H is used			±3.0	LSB
		AnVCC, AnVREFH = 3.0 V to 4.3 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±3.0	LSB
			ADCGnIm, When channel T&H is used			±4.0	LSB
Differential nonlinear[*1]	DLEn	AnVCC, AnVREFH = 4.3 V to 5.5 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±1.0	LSB
			ADCGnIm, When channel T&H is used			±1.0	LSB
		AnVCC, AnVREFH = 3.0 V to 4.3 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			+2.0, –1.0	LSB
			ADCGnIm, When channel T&H is used			+3.0, –1.0	LSB

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Offset error*1	ZSEn	AnVCC, AnVREFH = 4.3 V to 5.5 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±3.5	LSB
			ADCGnIm, When channel T&H is used			±5.5	LSB
		AnVCC, AnVREFH = 3.0 V to 4.3 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±5.5	LSB
			ADCGnIm, When channel T&H is used			±7.5	LSB
Full-scale error*1	FSEn	AnVCC, AnVREFH = 4.3 V to 5.5 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±3.5	LSB
			ADCGnIm, When channel T&H is used			±5.5	LSB
		AnVCC, AnVREFH = 3.0 V to 4.3 V, AnVCC – AnVREFH < 1V	ADCGnIm, When channel T&H is not used			±5.5	LSB
			ADCGnIm, When channel T&H is used			±7.5	LSB
Analog input voltage	VAINmSN	AnVCC – AnVREFH < 1 V	When channel T&H is not used	AnVSS		AnVREFH	V
			When channel T&H is used	AnVSS + 0.2 V		AnVREFH –0.2 V	V
Sampling time	t_{SMP}	ADCGnSMPCR = 0000_H, CLK_ADC = 40 MHz			t_{CONn} × (18/40)		µs
Channel T&H hold time*2	t_{THHOLD}					10	µs
Pull-up resistor for A/D wiring break detection	RU_AIN	VIN = AnVSS		10	20	40	kΩ
Pull-down resistor for A/D wiring break	RD_AIN	VIN = AnVCC		10	20	40	kΩ
Total errors at self-diagnosis	TESH0SN	When A/D conversion circuit self-diagnostic function is used				±40	LSB
		When pin-level self-diagnosis is used	AnVREFH = 4.3 V to 5.5 V			±80	LSB
			AnVREFH = 3.0 V to 4.3 V			±170	LSB
Equivalent input capacitance	CIN	During standby				10	pF
		During sampling				20	pF
Allowable analog signal impedance		Apply 0.1µF to analog pin				20	kΩ

Note 1. The values in the above table do not include quantization errors.

Note 2. Available retain time of sampling value by T&H circuit. Between sampling completion by T&H circuit and sampling completion of 12 bit SAR-AD by S/H circuit need to be executed within this time.

Note: n = 0,1 (number of units)
m = 0 to 11 (number of channels)

CAUTION

If current is injected to an analog input pin during the pin-level self-diagnosis, the conversion accuracy of the diagnostic voltage for the corresponding channel is not guaranteed.

3.15 Code Flash Characteristics

Table 3.11 Code Flash Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Sequencer Operating frequency	f_{CLKP_L}				40	MHz
Programming endurance*1	CWRT	Retained for 20 years*2	1000			Times
Temperature range of programming	TPRG	Tj	–40		150	°C
Temperature range of reading	TREAD	Tj	–40		150	°C

Note 1. Programming endurance is defined as the number of times each block is erased. Where programming endurance is n times (n = 1000 in this case), each block is erasable n times. For example, given a memory device that has 32-Kbyte erasure blocks, programming in the address range of each 256-byte programming block (128 programming operations, one for each block) in an erasure block and then erasing the block counts as one time in terms of programming endurance. However, programming of a given address range more than once after erasure is not possible (overwriting after programming is prohibited).

Note 2. This is the case when the average Ta is 85°C.

Table 3.12 Code Flash Programming Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time*1	Programming endurance < 100 times	256 B		2*1	6*1	ms
		32 KB		200	360	ms
	Programming endurance ≥ 100 times	256 B		2.4*1	7.2*1	ms
		32 KB		240	432	ms
Erasing time*1	Programming endurance < 100 times	8 KB		50	120	ms
		32 KB		200	480	ms
	Programming endurance ≥ 100 times	8 KB		60	144	ms
		32 KB		240	576	ms

Note 1. Values are only for processing by hardware. Software overhead is not taken into account.

3.16 Data Flash Characteristics

Table 3.13 Data Flash Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Sequencer Operating frequency	f_{CLKP_L}				40	MHz
Programming endurance[*1]	DWRT	Retained for 20 years[*2]	125000			Times
		Retained for 3 years[*2]	250000			Times
Temperature range of programming	TPRG	Tj	–40		150	°C
Temperature range of reading	TREAD	Tj	–40		150	°C

Note 1. Programming endurance is defined as the number of times each block is erased. Where programming endurance is n times (n = 125000 in this case), each block is erasable n times. For example, given a memory device that has 64-byte erasure blocks, programming in the address range of each 4-byte programming block (16 programming operations, one for each block) in an erasure block and then erasing the block counts as one time in terms of programming endurance. However, programming of a given address range more than once after erasure is not possible (overwriting after programming is prohibited).

Note 2. This is the case when the average Ta is 85°C.

Table 3.14 Data Flash Programming Characteristics

Conditions: See **Section 3.1.1.1, Common Conditions**.

Item	Block Size	MIN.	TYP.	MAX.	Unit
Programming time	4 B		0.3[*1]	1.7[*1]	ms
	32 KB		2.5	6.8	s
Erasing time	64 B		3[*1]	10[*1]	ms
	32 KB		1.6	5.2	s
Blank check time	4 B			30[*1]	µs
	64 B			100[*1]	µs

Note 1. Values are only for processing by hardware. Software overhead is not taken into account.

3.17 Debug Interface

3.17.1 JTAG/Nexus Timing

Table 3.15 JTAG/Nexus Timing

Conditions: Tj = –40°C to 150°C, CL = 30 pF

Item	Symbol	Condition	MIN.	MAX.	Unit
TCK cycle time	t_{TCKW}		40	—	ns
TCK high level width	t_{TCKWH}		16	—	ns
TCK low level width	t_{TCKWL}		16	—	ns
TMS/TDI setup time (vs TCK↑)	t_{TISU}		12	—	ns
TMS/TDI retaining time (vs TCK ↑)	t_{TIH}		12	—	ns
TDO output delay time (vs TCK↓)	t_{TDOD}		—	t_{TCKW} – 20	ns
RDY output delay time (vs TCK ↓)	t_{RDYD}		—	t_{TCKW} – 20	ns
$\overline{\text{TRST}}$ low level width	t_{TRSTWL}		1500	—	ns
TCK/$\overline{\text{TRST}}$/TMS/TDI input rising time	t_{TIR}		—	12	ns
TCK/$\overline{\text{TRST}}$/TMS/TDI input falling time	t_{TIF}		—	12	ns

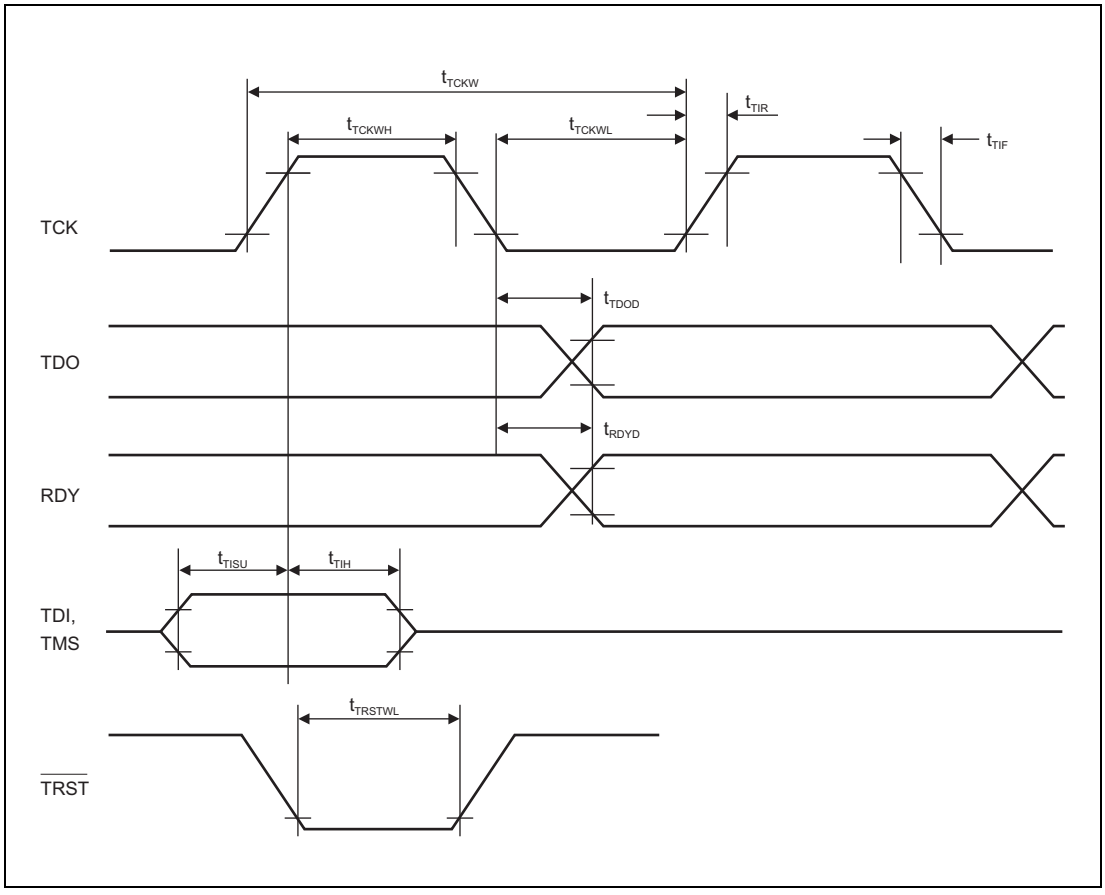


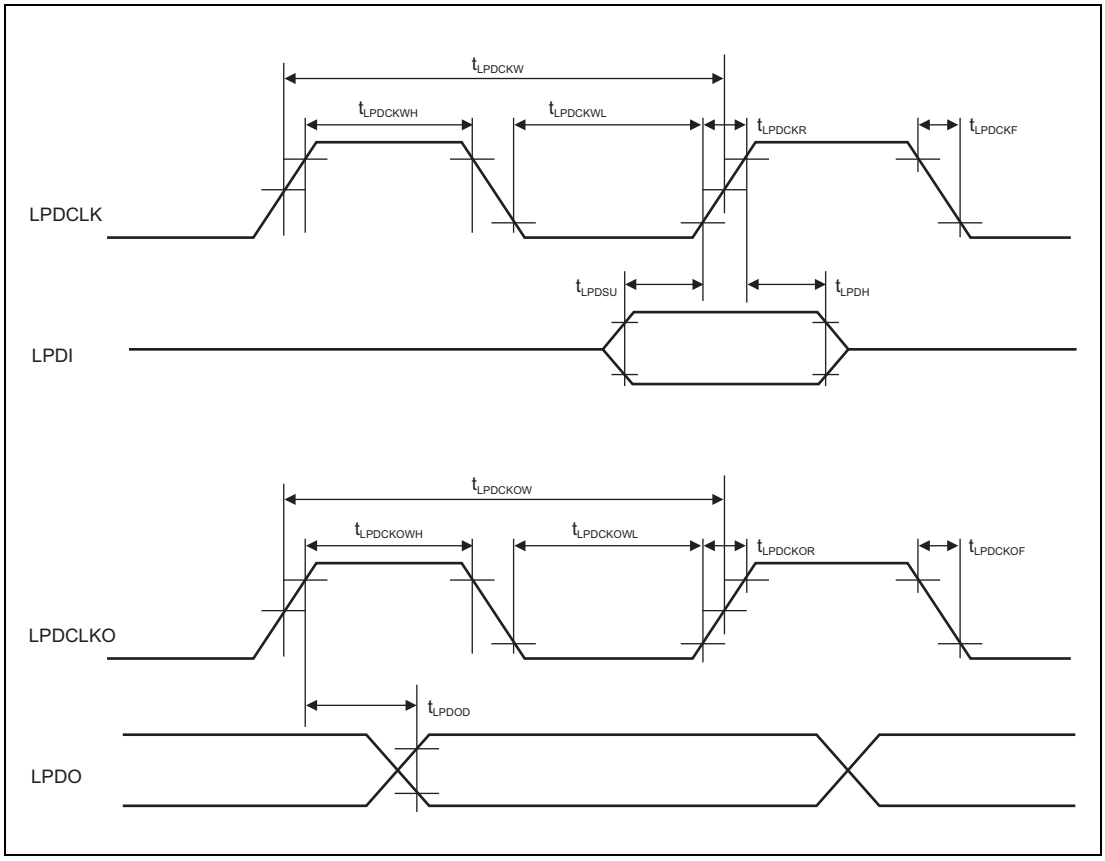
Figure 3.6 JTAG/Nexus Timing

3.17.2 LDU 4-Wire Timing

Table 3.16 LDU 4-Wire Timing

Conditions: Tj = –40°C to 150°C, CL = 30 pF

Item	Symbol	Condition	MIN.	MAX.	Unit
LPDCLK cycle time	t_{LPDCKW}		83.3 (max.12MHz)	—	ns
LPDCLK high level width	$t_{LPDCKWH}$		t_{LPDCKW}/ 2 – 10	—	ns
LPDCLK low level width	$t_{LPDCKWL}$		t_{LPDCKW}/ 2 – 10	—	ns
LPDCLK input rising time	t_{LPDCKR}		—	12	ns
LPDCLK input falling time	t_{LPDCKF}		—	12	ns
LPDI setup time (vs LPDCLK ↑)	t_{LPDSU}		41	—	ns
LPDI retaining time (vs LPDCLK ↑)	t_{LPDH}		3	—	ns
LPDCLKO cycle time	$t_{LPDCKOW}$		83.3 (max.12MHz)	—	ns
LPDCLKO high level width	$t_{LPDCKOWH}$		$t_{LPDCKWH}$ – 12	—	ns
LPDCLKO low level width	$t_{LPDCKOWL}$		$t_{LPDCKWL}$ – 12	—	ns
LPDCLKO rising time	$t_{LPDCKOR}$		—	12	ns
LPDCLKO falling time	$t_{LPDCKOF}$		—	12	ns
LPDO output delay (vs LPDCLKO ↑)	t_{LPDOD}		0	15	ns



3.18 Thermal Characteristics

Table 3.17 Thermal Resistance of RH850/P1M-E

Device	Parameter	Package	Condition	Estimated Value	Unit
P1M-E	ψjb1	LFQFP100 (14 × 14)	JEDEC, JESD51-7, f_{CPLL} = 160MHz, TJ, max = 150°C	27.3	°C/W
	ψjb2	LFQFP144 (16 × 16)	JEDEC, JESD51-7, f_{CPLL} = 160MHz, TJ, max = 150°C	25.4	°C/W
	ψjb3	LFQFP144 (20 × 20)	JEDEC, JESD51-7, f_{CPLL} = 160MHz, TJ, max = 150°C	26.6	°C/W

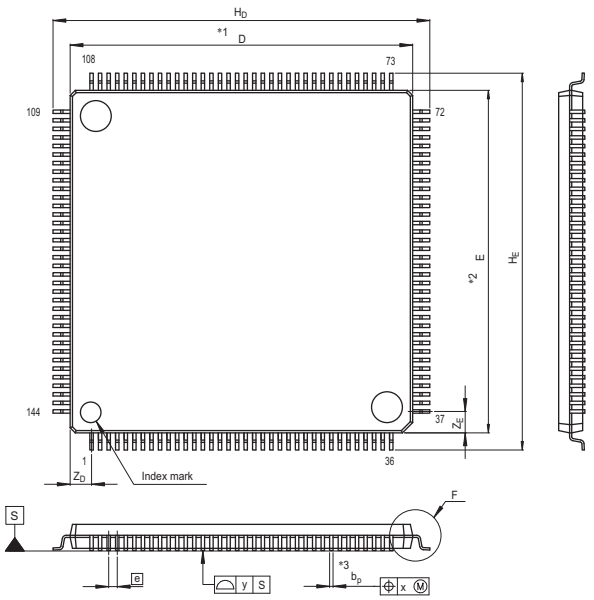
Note: The parameter values of thermal resistance and characteristics vary depending on the usage environment.

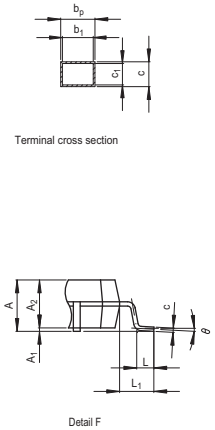
Section 4 Package

4.1 Package Outline

4.1.1 LFQFP144 (20x20) Package Drawing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

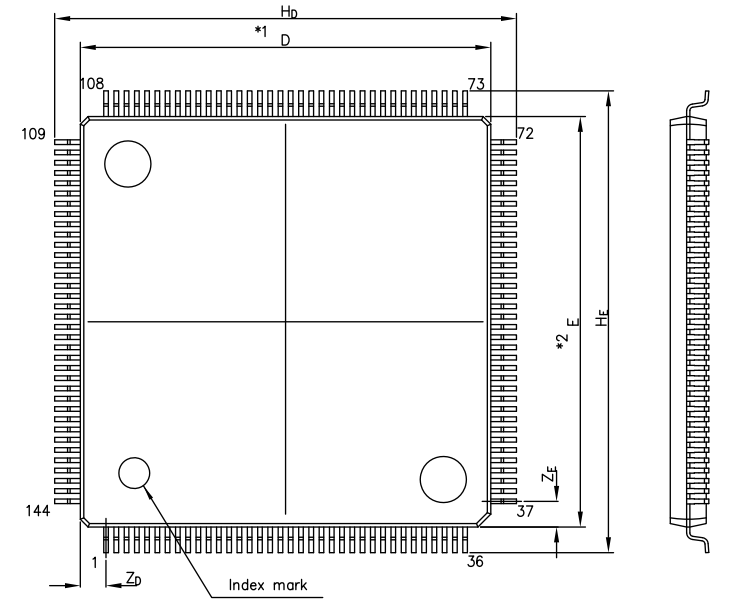
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

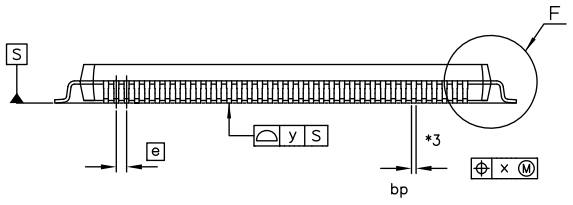
Figure 4.1 LFQFP (144pin, 20x20) outline

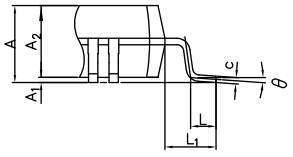
4.1.2 LQFP144 (16x16) Package Drawing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-16x16-0.40	PLQP0144LB-A	——	0.9g

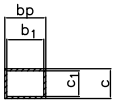
Unit: mm







Detail F



Terminal cross section

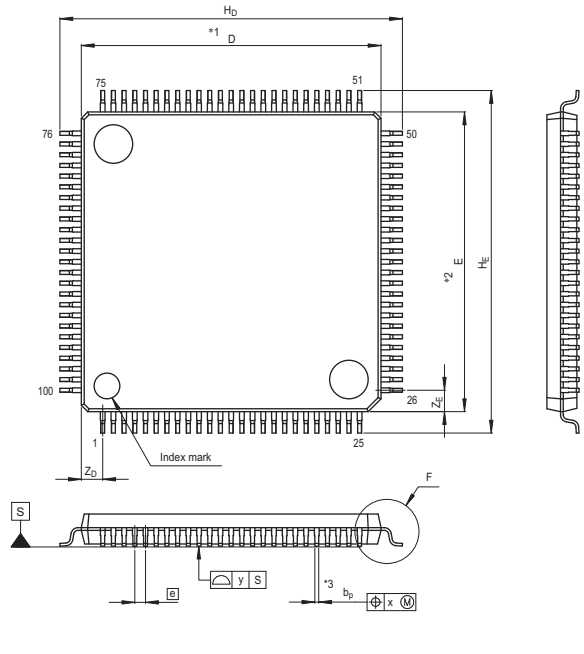
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A2	——	1.4	——
HD	17.8	18.0	18.2
HE	17.8	18.0	18.2
A	——	——	1.7
A1	0.05	0.10	0.15
bp	0.13	0.18	0.23
b1	——	0.16	——
c	0.09	0.145	0.20
c1	——	0.125	——
θ	0°	——	8°
e	——	0.4	——
x	——	——	0.07
y	——	——	0.08
ZD	——	1.0	——
ZE	——	1.0	——
L	0.35	0.5	0.65
L1	——	1.0	——

Figure 4.2 LFQFP (144pin, 16x16) outline

4.1.3 LQFP100 (14x14) Package Drawing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 4.3 LFQFP (100pin, 14x14) outline

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025.09.30	-	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

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