RH850/C1M-A

Renesas Microcontroller

Section 1 Overview

The RH850/C1M-A is a series of single-chip microcomputers in the RH850 Family from Renesas Electronics. This section covers the features of the RH850/C1M-A.

1.1 Features of RH850/C1M-A Products

(1) High speed processing

The CPU of these products is the G3MH of the RH850 Family running at 320 or 240 MHz for high-speed processing. These products incorporate ROM, RAM, DMA, various timers including timers for motor control, various serial interfaces including a CAN interface, and a 12-bit A/D converter (ADCC).

(2) Rich peripheral functionality

They also incorporate the set of peripheral functions, which are an R/D converter (RDC3A) that converts the signal output by a resolver into digital values representing angles, and a motor control unit (EMU3) that is capable of operating in parallel with the CPU, is optimized for HEV and EV motor control.

(3) Two products

Two products, the one for controlling two motors and the other for controlling one motor, are available. The products are provided in 252-pin BGA (for two-motor control) and 176-pin QFP (for one-motor control) packages.

(4) Functional Safety support

This microcontroller includes several dedicated functionalities such as the memory protection with ECC on data and clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(5) Security support

This microcontroller supports standard features for automotive security defined by the SHE (Secure Hardware Extension) standard. The Intelligent Cryptographic Unit -Slave(ICUSE) has some secure peripherals such a True Random Number Generator (TRNG).

Applications

Automotive (motor control for HEVs and EVs)

1.1.1 Functions of the RH850/C1M-A

Table 1.1 Overview of Products (1/2)

Item		C1M-A2	C1M-A1
CPU	CPU system	G3MH (LSDC*1) + G3MH	G3MH (LSDC*1)
	CPU frequency	320 MHz	240 MHz
	PE internal peripheral device protection function (IPG)	Provided	Provided
	System error notification control function (SEG)	Provided	Provided
	Memory protection unit (MPU)	Provided	Provided
	Floating-point unit (FPU)	Provided	Provided
	Mutual Exclusion Control Registers (MEV)	Provided	Not provided
On-chip memory	Code Flash	2 MB × 2	2 MB
	Instruction cache (Icache)	8 KB × 2	8 KB
	Local RAM	64 KB × 2	64 KB
	Data Flash	64 KB	64 KB
	Global RAM	128 KB	64 KB
External Interrupts	Maskable interrupt (IRQ)	8	8
DMA, DTS		16 channels, 128 channels	16 channels, 128 channels
Clock	Main oscillator (main OSC)	20 MHz	20 MHz
	PLL	Provided	Provided
Security	Intelligence cryptographic unit E (ICUSE)	Provided	Provided
	Secure watchdog timer A (SWDTA)	2	1
I/O ports		99	81
Timers	Timer array unit D (TAUD)	4 units	2 units
	Timer array unit J (TAUJ)	2 units	1 unit
	Motor control timer (TSG3)	3 units	2 units
	Timer option (TAPA)	6 units	4 units
	Timer pattern buffer (TPBA)	2 units	1 unit
	OS timer (OSTM)	4 units	3 units
	Encoder timer (ENCA)	2 units	2 units
	Watchdog timer (WDTA)	2 units	1 unit
Serial interface	Clocked Serial Interface H (CSIH)	3 channels	3 channels
	CAN interface (RS-CANFD)	4 channels	4 channels
	LIN interface (RLIN3)	3 channels	3 channels
	Serial Communication Interface (SCI3)	3 channels	3 channels
	RSENT (Single Edge Nibble Transmission)	4 channels	4 channels

Table 1.1 Overview of Products (2/2)

Item		C1M-A2	C1M-A1
A/D converter	12-bit A/D core	3 units	3 units
	ADCC0 : Number of input pins	16	11
	ADCC0 : Number of T&H	6	6
	ADCC1 : Number of input pins	16	14
	ADCC1 : Number of T&H	6	6
	ADCC2 : Number of input pins	16	5
	ADCC2 : Number of T&H	4	4
Motor control	R/D converter (RDC3A)	2 units	1 unit
	Enhanced motor control unit (EMU3): Number of units	1 unit (2 channels)	1 unit (1 channels)
	Enhanced motor control unit (EMU3): SubCPU frequency	320 MHz	240 MHz
Other functions	Error control module (ECM)	Provided	Provided
	Clock Monitor (CLMA)	Provided	Provided
	Data CRC (DCRA)	2 units	2 units
	Error correction coding (ECC)	Provided	Provided
	On-chip debug (OCD)	Provided	Provided
	Boundary scan	Provided	Provided
	Peripheral interconnection 1 (PIC1B)	2 units	1 unit
	Peripheral interconnection 2 (PIC2D)	1 unit	1 unit
Power supply voltage	Internal power supply	1.25 V ± 0.1 V	1.25 V ± 0.1 V
	I/O power supply	5.0 V ± 0.5 V	5.0 V ± 0.5 V
	R/D converter power supply	5.0 V ± 0.5 V	5.0 V ± 0.5 V
	A/D converter power supply	5.0 V ± 0.5 V	5.0 V ± 0.5 V
Temperature	Junction temperature (Tj)	– 40°C to 150°C	– 40°C to 150°C
Package		252-pin BGA	176-pin QFP

Note 1. LSDC (Lock Step Dual Core)

Table 1.2 List of Products

Group Name	Part Number	Package
RH850/C1M-A2	R7F701275EABG	252-pin plastic BGA (0.8-mm ball pitch) (17 × 17 mm)
RH850/C1M-A1	R7F701278EAFP	176-pin plastic QFP (0.5-mm pin pitch) (24 × 24 mm)

1.1.2 Internal Block Diagram

CPU1, CPU2, and the SubCPU include their own CPU peripherals. They can access only their own CPU peripherals. The same address is assigned to all the CPU peripherals of CPU1, CPU2, and the SubCPU, but CPU1 always accesses the CPU peripheral of CPU1, CPU2 always accesses the CPU peripheral of CPU2, and the SubCPU always accesses the CPU peripheral of the SubCPU.

For the peripheral modules in each peripheral group, see RH850/C1M-A1,C1M-A2 Group User's Manual:Hardware **Section 3.1.2, Configuration of Peripheral Groups.**

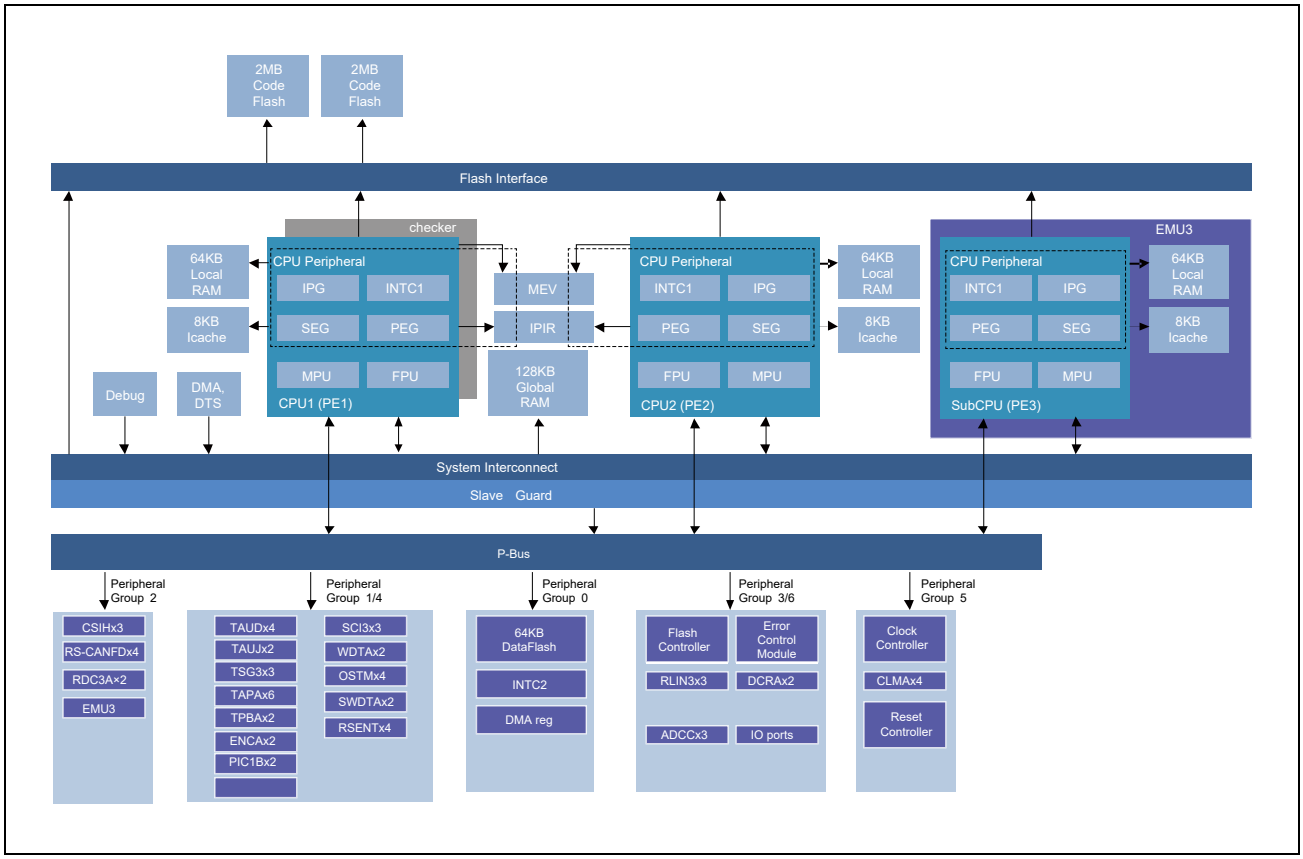


Figure 1.1 Internal Block Diagram of RH850/C1M-A2

CPU1 and the SubCPU include their own CPU peripherals. They can access only their own CPU peripherals.

For the peripheral modules in each peripheral group, see RH850/C1M-A1,C1M-A2 Group User's Manual:Hardware **Section 3.1.2, Configuration of Peripheral Groups**.

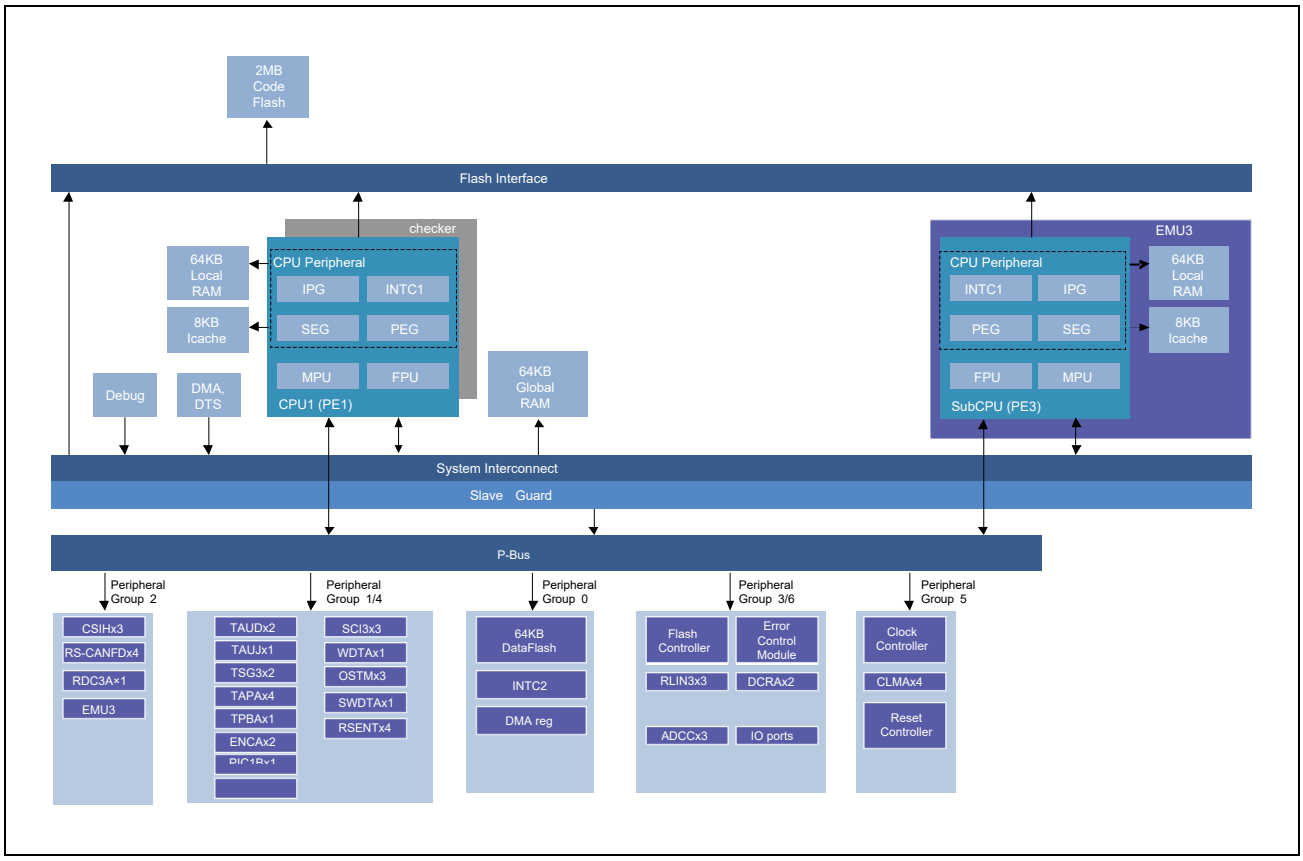


Figure 1.2 Internal Block Diagram of RH850/C1M-A1

1.2 Pin Connection Diagram (Top View)

1.2.1 RH850/C1M-A2 (252-Pin BGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	A0VSS (N.C.)	A0VSS (N.C.)	ADCC0I01	ADCC0I10	ADCC0I13	ADCC0I22	RDC3A1S2	RDC3A1RSO	RDC3A0RSO	RDC3A0S2	ADCC1I31	ADCC1I03	ADCC1I10	ADCC1I21	ADCC1I23	A2VSS	A2VCC	ADCC2I00	A2VSS (N.C.)	A2VSS (N.C.).	A
B	A0VSS (N.C.)	A0VREFH	ADCC0I00	ADCC0I03	ADCC0I12	ADCC0I21	RDC3A1S1	RDC3A1COM	RDC3A0COM	RDC3A0S1	ADCC1I30	ADCC1I01	ADCC1I11	ADCC1I22	ADCC1I33	A1VREFH	A2VREFH	ADCC2I22	ADCC2I01	A2VSS (N.C.)	B
C	ADCC0I32	ADCC0I33	ADCC0I23	ADCC0I02	ADCC0I11	ADCC0I20	RDC3A1S3	RVSS	RVCC	RDC3A0S3	ADCC1I00	ADCC1I02	ADCC1I13	ADCC1I32	A1VSS	A1VCC	ADCC2I20	ADCC2I21	ADCC2I02	ADCC2I03	C
D	ADCC0I30	ADCC0I31	A0VSS				RDC3A1S4	RVSS	RVCC	RDC3A0S4	VDD	VSS	ADCC1I12	ADCC1I20				ADCC2I31	ADCC2I23	ADCC2I30	D
E	P7_2	P7_0	A0VCC															ADCC2I33	ADCC2I32	ADCC2I10	E
F	P7_5	P7_3	P7_1															ADCC2I11	ADCC2I12	ADCC2I13	F
G	P7_4	P7_7	P7_6	VDD													VSS	P3_7	P3_6	P3_5	G
H	P5_0	P5_2	P5_1	VSS													VDD	P3_3	P3_2	P3_4	H
J	P5_3	P5_4	P5_6	P5_5					VDD	VSS	VSS	VDD					VSS	P2_7	P3_1	P3_0	J
K	P5_7	P5_8	P5_9	VCC					VDD	VSS	VSS	VDD					VCC	P2_6	P2_5	P2_4	K
L	P4_0	P4_1	P4_2	VSS					VDD	VSS	VSS	VDD					P2_1	P2_2	P2_3	P2_0	L
M	P4_3	P4_5	P4_4	VSS					VDD	VSS	VSS	VDD					P1_15	P1_12	P1_13	P1_14	M
N	P4_6	P4_7	P4_8	VDD													VSS	P1_9	P1_10	P1_11	N
P	P4_9	P4_10	P4_13	P4_12													VDD	P1_6	P1_7	P1_8	P
R	P4_11	P4_14	VDD															P1_3	P1_4	P1_5	R
T	P4_15	P6_10	VSS															P1_1	P1_0	P1_2	T
U	P6_11	$\overline{\text{AUDRST}}$	ADUCK				VDD	VSS	VSS	VCC	VSS	VDD	MD1	VSS				P6_8	P0_5	P6_9	U
V	P6_12	$\overline{\text{AUDSYNC}}$	AUDATA3	AUDATA1	P6_2	P6_3	P6_6	P0_8	P0_12	P0_15	VSS	VDD	$\overline{\text{DCUTRST}}$	VSS	SYSVCC	VCC	VSS	P0_2	P0_3	P0_4	V
W	VSS (N.C.)	P6_13	AUDATA2	AUDATA0	P6_0	P6_4	$\overline{\text{ERRROUT\_M}}$	P0_9	P0_11	P0_14	DCUTDO	DCUTDI	DCUTMS	P7_8	SYSVCC	$\overline{\text{RESET}}$	FLMODE	P0_0	P6_7	VSS (N.C.)	W
Y	VSS (N.C.)	VSS (N.C.)	P6_14	P6_15	P6_1	P6_5	P0_6	P0_7	P0_10	P0_13	$\overline{\text{DCURDY}}$	DCUTCK	VSS	X2	X1	VCC	MD0	P0_1	VSS (N.C.)	VSS (N.C.)	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.3 Pin Connections of RH850/C1M-A2

CAUTION

Though the pins indicated with the names of power supply pins (and as N.C.) do not affect operation of the microcontroller even if they are open-circuit, we recommend connecting the pins to the power supply of the same name as those that do not include N.C. to ensure that the power supply is stable.

In addition, be sure to mount solder balls on the substrate. The pins indicated with the names of power supply pins (and as N.C.) are internally connected with the power supply of the same name as those that do not include N.C.

Table 1.3 Pin Assignments of RH850/C1M-A2 (1/6)

Pin Number	Pin Name
1A	A0VSS(N.C.)
1B	A0VSS(N.C.)
1C	ADCC0I32
1D	ADCC0I30
1E	P7_2/TAUD0I7/TAUD0O7/TAUJ0I2/TAUJ0O2/SCI0RXD/CSIH2SO
1F	P7_5/CSIH2CSS0
1G	P7_4/TAUD0I8/TAUD0O8/TAUJ0I3/TAUJ0O3/SCI0TXD/CSIH2SI
1H	P5_0/RLIN32RX/SCI0RXD/CSIH2CSS3
1J	P5_3/RLIN31TX/SCI1SCK
1K	P5_7/SCI2SCK
1L	P4_0/CSIH1SI
1M	P4_3/CAN0RX/CSIH1CSS0
1N	P4_6/CAN1TX/CSIH0CSS3/CSIH1CSS3
1P	P4_9/CSIH0SC
1R	P4_11/CAN2TX/CSIH0CSS1
1T	P4_15/CAN3TX/ $\overline{\text{ERROROUT\_C}}$
1U	P6_11/TAUD3I11/TAUD3O11
1V	P6_12/TAUD3I12/TAUD3O12
1W	VSS(N.C.)
1Y	VSS(N.C.)
2A	A0VSS(N.C.)
2B	A0VREFH
2C	ADCC0I33
2D	ADCC0I31
2E	P7_0/TAUD0I5/TAUD0O5/TAUJ0I0/TAUJ0O0/ADCC1TRG/CSIH2SC
2F	P7_3/ENCA1TIN1/CSIH2CSS2
2G	P7_7
2H	P5_2/RLIN31RX/SCI0SCK/CSIH2RYI/CSIH2RYO
2J	P5_4/RLIN30RX/SCI1RXD
2K	P5_8/SCI2RXD
2L	P4_1/CSIH1SO
2M	P4_5/CAN1RX/CSIH0CSS2/CSIH1CSS2
2N	P4_7/CSIH0SI/CSIH1SSI
2P	P4_10/TPBA0O/CAN2RX/CSIH0CSS0
2R	P4_14/CAN3RX
2T	P6_10/TAUD3I10/TAUD3O10
2U	$\overline{\text{AUDRST}}$
2V	$\overline{\text{AUDSYNC}}$
2W	P6_13/TAUD3I13/TAUD3O13
2Y	VSS(N.C.)
3A	ADCC0I01
3B	ADCC0I00
3C	ADCC0I23
3D	A0VSS

Table 1.3 Pin Assignments of RH850/C1M-A2 (2/6)

Pin Number	Pin Name
3E	A0VCC
3F	P7_1/ENCA1TIN0/ADCC0TRG/CSIH2CSS1
3G	P7_6
3H	P5_1/RLIN32TX/SCI0TXD/CSIH2SSI
3J	P5_6/TPBA1O/TAPA0ESO
3K	P5_9/SCI2TXD
3L	P4_2/CSIH1SC
3M	P4_4/CAN0TX/CSIH1CSS1
3N	P4_8/CSIH0SO/CSIH1RYI/CSIH1RYO
3P	P4_13/RLIN30TX/CSIH0RYI/CSIH0RYO
3R	VDD
3T	VSS
3U	AUDCK
3V	AUDATA3
3W	AUDATA2
3Y	P6_14/TAUD3I14/TAUD3O14
4A	ADCC0I10
4B	ADCC0I03
4C	ADCC0I02
4G	VDD
4H	VSS
4J	P5_5/RLIN30TX/SCI1TXD/$\overline{\text{ERROROUT\_C}}$
4K	VCC
4L	VSS
4M	VSS
4N	VDD
4P	P4_12/RLIN30RX/CSIH0SSI
4V	AUDATA1
4W	AUDATA0
4Y	P6_15/TAUD3I15/TAUD3O15
5A	ADCC0I13/RDC3A1COSMNT
5B	ADCC0I12/RDC3A1SINMNT
5C	ADCC0I11
5V	P6_2/TAUD3I2/TAUD3O2/ENCA1TIN0/RDC3A0_OUT_W/ADCC0TRG
5W	P6_0/TAUD3I0/TAUD3O0/TAUJ1I2/TAUJ1O2/$\overline{\text{ERROROUT\_C}}$
5Y	P6_1/TAUD3I1/TAUD3O1/TAUJ1I3/TAUJ1O3
6A	ADCC0I22
6B	ADCC0I21
6C	ADCC0I20
6V	P6_3/TAUD3I3/TAUD3O3/RDC3A1_OUT_W
6W	P6_4/TAUD3I4/TAUD3O4/ENCA1TIN1/RDC3A0_OUT_V
6Y	P6_5/TAUD3I5/TAUD3O5/RDC3A1_OUT_V
7A	RDC3A1S2
7B	RDC3A1S1

Table 1.3 Pin Assignments of RH850/C1M-A2 (3/6)

Pin Number	Pin Name
7C	RDC3A1S3
7D	RDC3A1S4
7U	VDD
7V	P6_6/TAUD3I6/TAUD3O6/RDC3A0_OUT_U/TAPA0ESO
7W	$\overline{\text{ERROROUT\_M}}$
7Y	P0_6/TAUD0I6/TAUD0O6/TAUJ0I1/TAUJ0O1/ENCA0E0/RDC3A0_OUT_U/INTP3
8A	RDC3A1RSO
8B	RDC3A1COM
8C	RVSS
8D	RVSS
8U	VSS
8V	P0_8/TAUD0I8/TAUD0O8/TAUJ0I3/TAUJ0O3/ENCA0EC/RDC3A0_OUT_W/INTP5
8W	P0_9/TAUD0I9/TAUD0O9/TAUD3I3/TAUD3O3/TAPA5ESO/INTP6
8Y	P0_7/TAUD0I7/TAUD0O7/TAUJ0I2/TAUJ0O2/ENCA0E1/RDC3A0_OUT_V/INTP4
9A	RDC3A0RSO
9B	RDC3A0COM
9C	RVCC
9D	RVCC
9J	VDD
9K	VDD
9L	VDD
9M	VDD
9U	VSS
9V	P0_12/TAUD0I12/TAUD0O12/TAPA0VP/TAUD3I9/TAUD3O9/RSENT0RX/RSENT0SPCO
9W	P0_11/TAUD0I11/TAUD0O11/TAPA0UN/TAUD3I7/TAUD3O7/TSGTRG
9Y	P0_10/TAUD0I10/TAUD0O10/TAPA0UP/TAUD3I5/TAUD3O5/INTP7
10A	RDC3A0S2
10B	RDC3A0S1
10C	RDC3A0S3
10D	RDC3A0S4
10J	VSS
10K	VSS
10L	VSS
10M	VSS
10U	VCC
10V	P0_15/TAUD0I15/TAUD0O15/TAPA0WN/TAUD3I15/TAUD3O15/RSENT1SPCO
10W	P0_14/TAUD0I14/TAUD0O14/TAPA0WP/TAUD3I13/TAUD3O13/RSENT1RX/RSENT1SPCO
10Y	P0_13/TAUD0I13/TAUD0O13/TAPA0VN/TAUD3I11/TAUD3O11/RSENT0SPCO
11A	ADCC1I31
11B	ADCC1I30
11C	ADCC1I00/RDC3A0SINMNT
11D	VDD
11J	VSS
11K	VSS

Table 1.3 Pin Assignments of RH850/C1M-A2 (4/6)

Pin Number	Pin Name
11L	VSS
11M	VSS
11U	VSS
11V	VSS
11W	DCUTDO
11Y	$\overline{\text{DCURDY}}$
12A	ADCC1I03
12B	ADCC1I01/RDC3A0COSMNT
12C	ADCC1I02
12D	VSS
12J	VDD
12K	VDD
12L	VDD
12M	VDD
12U	VDD
12V	VDD
12W	DCUTDI
12Y	DCUTCK
13A	ADCC1I10
13B	ADCC1I11
13C	ADCC1I13
13D	ADCC1I12
13U	MD1
13V	$\overline{\text{DCUTRST}}$
13W	DCUTMS
13Y	VSS
14A	ADCC1I21
14B	ADCC1I22
14C	ADCC1I32
14D	ADCC1I20
14U	VSS
14V	VSS
14W	P7_8
14Y	X2
15A	ADCC1I23
15B	ADCC1I33
15C	A1VSS
15V	SYSVCC
15W	SYSVCC
15Y	X1
16A	A2VSS
16B	A1VREFH
16C	A1VCC
16V	VCC

Table 1.3 Pin Assignments of RH850/C1M-A2 (5/6)

Pin Number	Pin Name
16W	$\overline{\text{RESET}}$
16Y	VCC
17A	A2VCC
17B	A2VREFH
17C	ADCC2I20
17G	VSS
17H	VDD
17J	VSS
17K	VCC
17L	P2_1/TAUD2I1/TAUD2O1/TSG31O7/INTP1
17M	P1_15/TAUD1I15/TAUD1O15/TAPA1WN/TSG32O6
17N	VSS
17P	VDD
17V	VSS
17W	FLMODE
17Y	MD0
18A	ADCC2I00
18B	ADCC2I22
18C	ADCC2I21
18D	ADCC2I31
18E	ADCC2I33
18F	ADCC2I11
18G	P3_7/TAUD2I15/TAUD2O15/TAPA2WN/ADCC2TRG/RSENT3SPCO
18H	P3_3/TAUD2I11/TAUD2O11/TAPA2UN/ENCA1E0/RDC3A1_OUT_U
18J	P2_7/TAUD2I7/TAUD2O7/TSG31O6/INTP7
18K	P2_6/TAUD2I6/TAUD2O6/TSG31O4/INTP6
18L	P2_2/TAUD2I2/TAUD2O2/TSG31O1/INTP2
18M	P1_12/TAUD1I12/TAUD1O12/TAPA1VP/TAUD1O13/TSG32O5
18N	P1_9/TAUD1I9/TAUD1O9/TSG32O7/TAPA4ESO
18P	P1_6/TAUD1I6/TAUD1O6/TAUD1O7/TSG30O4
18R	P1_3/TAUD1I3/TAUD1O3/TSG30O3
18T	P1_1/TAUD1I1/TAUD1O1/ENCA0TIN1/TSG30O7
18U	P6_8/TAUD3I8/TAUD3O8/TAUJ1I0/TAUJ1O0
18V	P0_2/TAUD0I2/TAUD0O2/TAUJ0I2/TAUJ0O2/TAPA3ESO
18W	P0_0/TAUD0I0/TAUD0O0/TAUJ0I0/TAUJ0O0
18Y	P0_1/TAUD0I1/TAUD0O1/TAUJ0I1/TAUJ0O1/TAPA5ESO
19A	A2VSS(N.C.)
19B	ADCC2I01
19C	ADCC2I02
19D	ADCC2I23
19E	ADCC2I32
19F	ADCC2I12
19G	P3_6/TAUD2I14/TAUD2O14/TAPA2WP/RSENT3RX/RSENT3SPCO
19H	P3_2/TAUD2I10/TAUD2O10/TAPA2UP/ADCC1TRG

Table 1.3 Pin Assignments of RH850/C1M-A2 (6/6)

Pin Number	Pin Name
19J	P3_1/TAUD2I9/TAUD2O9/ADCC0TRG/RSENT2SPCO/TAPA2ESO
19K	P2_5/TAUD2I5/TAUD2O5/TSG31O2/INTP5
19L	P2_3/TAUD2I3/TAUD2O3/TSG31O3/INTP3
19M	P1_13/TAUD1I13/TAUD1O13/TAPA1VN/TSG32O2
19N	P1_10/TAUD1I10/TAUD1O10/TAPA1UP/TAUD1O11/TSG32O1
19P	P1_7/TAUD1I7/TAUD1O7/TSG30O6
19R	P1_4/TAUD1I4/TAUD1O4/TAUD1O5/TSG30O5
19T	P1_0/TAUD1I0/TAUD1O0/ENCA0TIN0/TAUD1O1/TSG30O0
19U	P0_5/TAUD0I5/TAUD0O5/TAUJ0I0/TAUJ0O0/TAPA4ESO/INTP2
19V	P0_3/TAUD0I3/TAUD0O3/TAUJ0I3/TAUJ0O3/CAN2RX/INTP0
19W	P6_7/TAUD3I7/TAUD3O7/RDC3A1_OUT_U/TAPA1ESO
19Y	VSS(N.C.)
20A	A2VSS(N.C.)
20B	A2VSS(N.C.)
20C	ADCC2I03
20D	ADCC2I30
20E	ADCC2I10
20F	ADCC2I13
20G	P3_5/TAUD2I13/TAUD2O13/TAPA2VN/ENCA1EC/RDC3A1_OUT_W/TAPA0ESO
20H	P3_4/TAUD2I12/TAUD2O12/TAPA2VP/ENCA1E1/RDC3A1_OUT_V/ADCC0TRG/TAPA3ESO
20J	P3_0/TAUD2I8/TAUD2O8/RSENT2RX/RSENT2SPCO/TAPA1ESO
20K	P2_4/TAUD2I4/TAUD2O4/TSG31O5/INTP4
20L	P2_0/TAUD2I0/TAUD2O0/TSG31O0/INTP0
20M	P1_14/TAUD1I14/TAUD1O14/TAPA1WP/TAUD1O15/TSG32O4
20N	P1_11/TAUD1I11/TAUD1O11/TAPA1UN/TSG32O3
20P	P1_8/TAUD1I8/TAUD1O8/TAUD1O9/TSG32O0/TAPA2ESO
20R	P1_5/TAUD1I5/TAUD1O5/TSG30O2
20T	P1_2/TAUD1I2/TAUD1O2/TAUD1O3/TSG30O1
20U	P6_9/TAUD3I9/TAUD3O9/TAUJ1I1/TAUJ1O1
20V	P0_4/TAUD0I4/TAUD0O4/TAUD3I1/TAUD3O1/CAN2TX/INTP1
20W	VSS(N.C.)
20Y	VSS(N.C.)

1.2.2 RH850/C1M-A1 (176-Pin QFP)

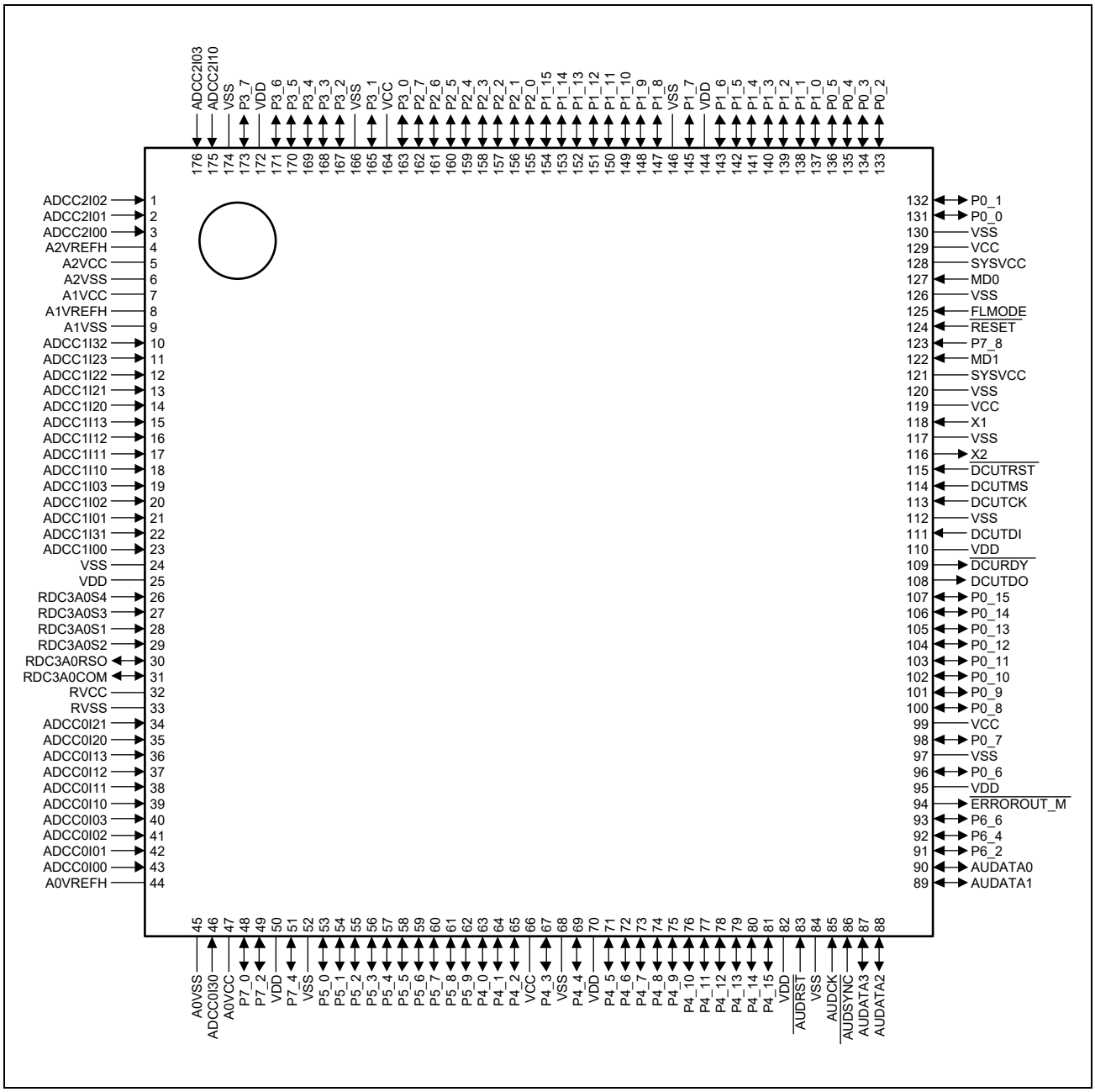


Figure 1.4 Pin Connections of RH850/C1M-A1

Table 1.4 Pin Assignments of RH850/C1M-A1 (1/4)

Pin Number	Pin Name
1	ADCC2I02
2	ADCC2I01
3	ADCC2I00
4	A2VREFH
5	A2VCC
6	A2VSS
7	A1VCC
8	A1VREFH
9	A1VSS
10	ADCC1I32
11	ADCC1I23
12	ADCC1I22
13	ADCC1I21
14	ADCC1I20
15	ADCC1I13
16	ADCC1I12
17	ADCC1I11
18	ADCC1I10
19	ADCC1I03
20	ADCC1I02
21	ADCC1I01/RDC3A0COSMNT
22	ADCC1I31
23	ADCC1I00/RDC3A0SINMNT
24	VSS
25	VDD
26	RDC3A0S4
27	RDC3A0S3
28	RDC3A0S1
29	RDC3A0S2
30	RDC3A0RSO
31	RDC3A0COM
32	RVCC
33	RVSS
34	ADCC0I21
35	ADCC0I20
36	ADCC0I13
37	ADCC0I12
38	ADCC0I11
39	ADCC0I10
40	ADCC0I03
41	ADCC0I02
42	ADCC0I01
43	ADCC0I00
44	A0VREFH

Table 1.4 Pin Assignments of RH850/C1M-A1 (2/4)

Pin Number	Pin Name
45	A0VSS
46	ADCC0I30
47	A0VCC
48	P7_0/TAUD0I5/TAUD0O5/TAUJ0I0/TAUJ0O0/ADCC1TRG/CSIH2SC
49	P7_2/TAUD0I7/TAUD0O7/TAUJ0I2/TAUJ0O2/SCI0RXD/CSIH2SO
50	VDD
51	P7_4/TAUD0I8/TAUD0O8/TAUJ0I3/TAUJ0O3/SCI0TXD/CSIH2SI
52	VSS
53	P5_0/RLIN32RX/SCI0RXD/CSIH2CSS3
54	P5_1/RLIN32TX/SCI0TXD/CSIH2SSI
55	P5_2/RLIN31RX/SCI0SCK/SCI0SCK/CSIH2RYI/CSIH2RYO
56	P5_3/RLIN31TX/SCI1SCK
57	P5_4/RLIN30RX/SCI1RXD
58	P5_5/RLIN30TX/SCI1TXD/$\overline{\text{ERROROUT\_C}}$
59	P5_6/TAPA0ESO
60	P5_7/SCI2SCK
61	P5_8/SCI2RXD
62	P5_9/SCI2TXD
63	P4_0/CSIH1SI
64	P4_1/CSIH1SO
65	P4_2/CSIH1SC
66	VCC
67	P4_3/CAN0RX/CSIH1CSS0
68	VSS
69	P4_4/CAN0TX/CSIH1CSS1
70	VDD
71	P4_5/CAN1RX/CSIH0CSS2/CSIH1CSS2
72	P4_6/CAN1TX/CSIH0CSS3/CSIH1CSS3
73	P4_7/CSIH0SI/CSIH1SSI
74	P4_8/CSIH0SO/CSIH1RYI/CSIH1RYO
75	P4_9/CSIH0SC
76	P4_10/TPBA0O/CAN2RX/CSIH0CSS0
77	P4_11/CAN2TX/CSIH0CSS1
78	P4_12/RLIN30RX/CSIH0SSI
79	P4_13/RLIN30TX/CSIH0RYI/CSIH0RYO
80	P4_14/CAN3RX
81	P4_15/CAN3TX/$\overline{\text{ERROROUT\_C}}$
82	VDD
83	$\overline{\text{AUDRST}}$
84	VSS
85	AUDCK
86	$\overline{\text{AUDSYNC}}$
87	AUDATA3
88	AUDATA2

Table 1.4 Pin Assignments of RH850/C1M-A1 (3/4)

Pin Number	Pin Name
89	AUDATA1
90	AUDATA0
91	P6_2/ENCA1TIN0/RDC3A0_OUT_W/ADCC0TRG
92	P6_4/ENCA1TIN1/RDC3A0_OUT_V
93	P6_6/RDC3A0_OUT_U/TAPA0ESO
94	$\overline{\text{ERROROUT\_M}}$
95	VDD
96	P0_6/TAUD0I6/TAUD0O6/TAUJ0I1/TAUJ0O1/ENCA0E0/RDC3A0_OUT_U/INTP3
97	VSS
98	P0_7/TAUD0I7/TAUD0O7/TAUJ0I2/TAUJ0O2/ENCA0E1/RDC3A0_OUT_V/INTP4
99	VCC
100	P0_8/TAUD0I8/TAUD0O8/TAUJ0I3/TAUJ0O3/ENCA0EC/RDC3A0_OUT_W/INTP5
101	P0_9/TAUD0I9/TAUD0O9/INTP6
102	P0_10/TAUD0I10/TAUD0O10/TAPA0UP/INTP7
103	P0_11/TAUD0I11/TAUD0O11/TAPA0UN/TSGTRG
104	P0_12/TAUD0I12/TAUD0O12/TAPA0VP/RSENT0RX/RSENT0SPCO
105	P0_13/TAUD0I13/TAUD0O13/TAPA0VN/RSENT0SPCO
106	P0_14/TAUD0I14/TAUD0O14/TAPA0WP/RSENT1RX/RSENT1SPCO
107	P0_15/TAUD0I15/TAUD0O15/TAPA0WN/RSENT1SPCO
108	DCUTDO
109	$\overline{\text{DCURDY}}$
110	VDD
111	DCUTDI
112	VSS
113	DCUTCK
114	DCUTMS
115	$\overline{\text{DCUTRST}}$
116	X2
117	VSS
118	X1
119	VCC
120	VSS
121	SYSVCC
122	MD1
123	P7_8
124	$\overline{\text{RESET}}$
125	FLMODE
126	VSS
127	MD0
128	SYSVCC
129	VCC
130	VSS
131	P0_0/TAUD0I0/TAUD0O0/TAUJ0I0/TAUJ0O0
132	P0_1/TAUD0I1/TAUD0O1/TAUJ0I1/TAUJ0O1

Table 1.4 Pin Assignments of RH850/C1M-A1 (4/4)

Pin Number	Pin Name
133	P0_2/TAUD0I2/TAUD0O2/TAUJ0I2/TAUJ0O2/TAPA3ESO
134	P0_3/TAUD0I3/TAUD0O3/TAUJ0I3/TAUJ0O3/CAN2RX/INTP0
135	P0_4/TAUD0I4/TAUD0O4/CAN2TX/INTP1
136	P0_5/TAUD0I5/TAUD0O5/TAUJ0I0/TAUJ0O0/TAPA4ESO/INTP2
137	P1_0/TAUD1I0/TAUD1O0/ENCA0TIN0/TAUD1O1/TSG30O0
138	P1_1/TAUD1I1/TAUD1O1/ENCA0TIN1/TSG30O7
139	P1_2/TAUD1I2/TAUD1O2/TAUD1O3/TSG30O1
140	P1_3/TAUD1I3/TAUD1O3/TSG30O3
141	P1_4/TAUD1I4/TAUD1O4/TAUD1O5/TSG30O5
142	P1_5/TAUD1I5/TAUD1O5/TSG30O2
143	P1_6/TAUD1I6/TAUD1O6/TAUD1O7/TSG30O4
144	VDD
145	P1_7/TAUD1I7/TAUD1O7/TSG30O6
146	VSS
147	P1_8/TAUD1I8/TAUD1O8/TAUD1O9
148	P1_9/TAUD1I9/TAUD1O9/TAPA4ESO
149	P1_10/TAUD1I10/TAUD1O10/TAPA1UP/TAUD1O11
150	P1_11/TAUD1I11/TAUD1O11/TAPA1UN
151	P1_12/TAUD1I12/TAUD1O12/TAPA1VP/TAUD1O13
152	P1_13/TAUD1I13/TAUD1O13/TAPA1VN
153	P1_14/TAUD1I14/TAUD1O14/TAPA1WP/TAUD1O15
154	P1_15/TAUD1I15/TAUD1O15/TAPA1WN
155	P2_0/TSG31O0/INTP0
156	P2_1/TSG31O7/INTP1
157	P2_2/TSG31O1/INTP2
158	P2_3/TSG31O3/INTP3
159	P2_4/TSG31O5/INTP4
160	P2_5/TSG31O2/INTP5
161	P2_6/TSG31O4/INTP6
162	P2_7/TSG31O6/INTP7
163	P3_0/RSENT2RX/RSENT2SPCO/TAPA1ESO
164	VCC
165	P3_1/ADCC0TRG/RSENT2SPCO
166	VSS
167	P3_2/ADCC1TRG
168	P3_3/ENCA1E0
169	P3_4/ENCA1E1/ADCC0TRG/TAPA3ESO
170	P3_5/ENCA1EC/TAPA0ESO
171	P3_6/RSENT3RX/RSENT3SPCO
172	VDD
173	P3_7/ADCC2TRG/RSENT3SPCO
174	VSS
175	ADCC2I10
176	ADCC2I03

Section 2 Pins

2.1 Pin Description

2.1.1 List of Pin Functions

Function of each pin is described below.

Table 2.1 C1M-A2 Pin Function (1/3)

Pin Name	I/O	Function
AnVREFH (n = 0 to 2)	—	ADCCn voltage supply and reference voltage
AnVSS (n = 0 to 2)	—	ADCCn ground
$\overline{\text{ADCCnTRG}}$ (n = 0 to 2)	I	ADCCn trigger
ADCCnIpq (n = 0 to 2, p = 0 to 3, q = 0 to 3)	I	ADCCn input channel pq
AUDATAm (m = 0 to 3)	IO	AUDR command / address / data / flag m
AUDCK	I	AUDR clock
$\overline{\text{AUDRST}}$	I	AUDR reset
$\overline{\text{AUDSYNC}}$	I	AUDR timing control
AnVCC (n = 0 to 2)	—	ADCCn voltage supply
CANmRX (m = 0 to 3)	I	CANm receive data input
CANmTX (m = 0 to 3)	O	CANm transmit data output
CSIHnCSS0 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 0
CSIHnCSS1 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 1
CSIHnCSS2 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 2
CSIHnCSS3 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 3
CSIHnRYI (n = 0 to 2)	I	CSIHn ready (1) / busy (0) input signal
CSIHnRYO (n = 0 to 2)	O	CSIHn ready (1) / busy (0) output signal
CSIHnSC (n = 0 to 2)	IO	CSIHn serial clock signal
CSIHnSI (n = 0 to 2)	I	CSIHn serial data input
CSIHnSO (n = 0 to 2)	O	CSIHn serial data output
$\overline{\text{CSIHnSSI}}$ (n = 0 to 2)	I	CSIHn slave select input signal
$\overline{\text{DCURDY}}$	O	Debug ready
DCUTCK	I	Debug clock
DCUTDI	I	Debug data input
DCUTDO	O	Debug data output
DCUTMS	I	Debug mode select
$\overline{\text{DCUTRST}}$	I	Debug reset
FLSCI3TX (FPDT)	O	Transmit data output
FLSCI3RX (FPDR)	I	Receive data input
FLSCI3SCK (FPCK)	I	Serial clock input
ENCAnE0 (n = 0, 1)	I	ENCAn encoder input (count pulse 0)
ENCAnE1 (n = 0, 1)	I	ENCAn encoder input (count pulse 1)

Table 2.1 C1M-A2 Pin Function (2/3)

Pin Name	I/O	Function
ENCAnTINm (n = 0, 1, m = 0, 1)	I	ENCAn capture trigger input nm
ENCAnEC (n = 0, 1)	I	ENCAn encoder input (clear pulse)
$\overline{\text{ERROROUT\_M}}$	O	ECM error output (main)
$\overline{\text{ERROROUT\_C}}$	O	ECM error output (checker)
FLMODE	I	Operating mode select pin
MD0	I	Operating mode select pin 0
MD1	I	Operating mode select pin 1
INTPm (m = 0 to 7)	I	External interrupt input m
LPDCLK	I	LPD clock input (4-pin mode)
LPDCLKOUT	O	LPD clock output (4-pin mode)
LPDI	I	LPD data input (4-pin mode)
LPDO	O	LPD data output (4-pin mode)
$\overline{\text{LPDRST}}$	I	LPD Reset (4-pin mode)
P0_m (m = 0 to 15)	IO	Port 0_m
P1_m (m = 0 to 15)	IO	Port 1_m
P2_m (m = 0 to 7)	IO	Port 2_m
P3_m (m = 0 to 7)	IO	Port 3_m
P4_m (m = 0 to 15)	IO	Port 4_m
P5_m (m = 0 to 9)	IO	Port 5_m
P6_m (m = 0 to 15)	IO	Port 6_m
P7_m (m = 0 to 7)	IO	Port 7_m
P7_m (m = 8)	I	Port 7_m
SYSVCC	—	Voltage supply for system and PLL
VCC	—	Voltage supply for oscillator, flash memory, and port buffer
VDD	—	Voltage regulators voltage supply
VSS	—	Ground
RVCC	—	Voltage supply for RDC
RVSS	—	Ground for RDC
$\overline{\text{RESET}}$	I	External reset input
RDC3AnCOM (n = 0, 1)	IO	Excitation common signal input/output
RDC3AnCOSMNT (n = 0, 1)	O	COS-side monitoring signal output
RDC3AnRSO (n = 0, 1)	IO	Excitation signal input/output
RDC3AnS1 (n = 0, 1)	I	Resolver signal input
RDC3AnS2 (n = 0, 1)	I	Resolver signal input
RDC3AnS3 (n = 0, 1)	I	Resolver signal input
RDC3AnS4 (n = 0, 1)	I	Resolver signal input
RDC3AnSINMNT (n = 0, 1)	O	SIN-side monitoring signal output
RLIN3mRX (m = 0 to 2)	I	RLIN3m receive data input
RLIN3mTX (m = 0 to 2)	O	RLIN3m transmit data output
SCInRXD (n = 0 to 2)	I	SCIn receive data

Table 2.1 C1M-A2 Pin Function (3/3)

Pin Name	I/O	Function
SCInSCK (n = 0 to 2)	IO	SCIn clock
SCInTXD (n = 0 to 2)	O	SCIn transmit data
TAPAnESO (n = 0 to 5)	I	Hi-Z control
TAPAnUN (n = 0 to 2)	O	Motor control output U phase (negative)
TAPAnUP (n = 0 to 2)	O	Motor control output U phase (positive)
TAPAnVN (n = 0 to 2)	O	Motor control output V phase (negative)
TAPAnVP (n = 0 to 2)	O	Motor control output V phase (positive)
TAPAnWN (n = 0 to 2)	O	Motor control output W phase (negative)
TAPAnWP (n = 0 to 2)	O	Motor control output W phase (positive)
TPBAnO (n = 0, 1)	O	TPBAn channel output
TAUDnIm (n = 0 to 3, m = 0 to 15)	I	TAUDn channel input m
TAUDnOm (n = 0 to 3, m = 0 to 15)	O	TAUDn channel output m
TAUJnIm (n = 0 to 1, m = 0 to 3)	I	TAUJn channel input m
TAUJnOm (n = 0 to 1, m = 0 to 3)	O	TAUJn channel output m
TSG3nOm (n = 0 to 2, m = 0 to 7)	O	TSG3n channel output m
X1, X2	—	Crystal oscillator connections
RSENTnRX (n = 0 to 3)	I	SENT input
RSENTnSPCO (n = 0 to 3)	O	SENT control output
RDC3An_OUT_U (n = 0, 1)	O	RDC U-phase output
RDC3An_OUT_V (n = 0, 1)	O	RDC V-phase output
RDC3An_OUT_W (n = 0, 1)	O	RDC W-phase output

CAUTION

In C1M-A2, use SCI30 with the alternative function pins within the same port group.

- When serial clock I/O signals are used
  - P5_0(SCI0RXD), P5_1(SCI0TXD), P5_2(SCI0SCK)
- When serial clock I/O signals are not used
  - P5_0(SCI0RXD), P5_1(SCI0TXD)
  - P7_2(SCI0RXD), P7_4(SCI0TXD)

Table 2.2 C1M-A1 Pin Function (1/3)

Pin Name	I/O	Function
AnVREFH (n = 0 to 2)	—	ADCCn voltage supply and reference voltage
AnVSS (n = 0 to 2)	—	ADCCn ground
$\overline{\text{ADCCnTRG}}$ (n =0 to 2)	I	ADCCn trigger
ADCC0Ipq (p = 0 to 3, q = 0 to 3) This excludes the combination of p = 2 and q = 2 or 3 and of p = 3 and q = 1 to 3.	I	ADCC0 input channel pq
ADCC1Ipq (p = 0 to 3, q = 0 to 3) This excludes the combination of p = 3 and q = 0 or 3.	I	ADCC1 input channel pq
ADCC2Ipq (p = 0 to 1, q = 0 to 3) This excludes the combination of p = 1 and q = 1 to 3.	I	ADCC2 input channel pq
AUDATAm (m = 0 to 3)	IO	AUDR command / address / data / flag m
AUDCK	I	AUDR clock
$\overline{\text{AUDRST}}$	I	AUDR reset
$\overline{\text{AUDSYNC}}$	I	AUDR timing control
AnVCC (n = 0 to 2)	—	ADCCn voltage supply
CANmRX (m = 0 to 3)	I	CANm receive data input
CANmTX (m = 0 to 3)	O	CANm transmit data output
CSIHnCSS0 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 0
CSIHnCSS1 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 1
CSIHnCSS2 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 2
CSIHnCSS3 (n = 0 to 2)	O	CSIHn serial peripheral chip select signal 3
CSIHnRYI (n = 0 to 2)	I	CSIHn ready (1) / busy (0) input signal
CSIHnRYO (n = 0 to 2)	O	CSIHn ready (1) / busy (0) output signal
CSIHnSC (n = 0 to 2)	IO	CSIHn serial clock signal
CSIHnSI (n = 0 to 2)	I	CSIHn serial data input
CSIHnSO (n = 0 to 2)	O	CSIHn serial data output
$\overline{\text{CSIHnSSI}}$ (n = 0 to 2)	I	CSIHn slave select input signal
$\overline{\text{DCURDY}}$	O	Debug ready
DCUTCK	I	Debug clock
DCUTDI	I	Debug data input
DCUTDO	O	Debug data output
DCUTMS	I	Debug mode select
$\overline{\text{DCUTRST}}$	I	Debug reset
FLSCI3TX (FPDT)	O	Transmit data output
FLSCI3RX (FPDR)	I	Receive data input
FLSCI3SCK (FPCK)	I	Serial clock input
ENCAnE0 (n = 0, 1)	I	ENCAn encoder input (count pulse 0)
ENCAnE1 (n = 0, 1)	I	ENCAn encoder input (count pulse 1)

Table 2.2 C1M-A1 Pin Function (2/3)

Pin Name	I/O	Function
ENCAnTINm (n = 0, 1, m = 0, 1)	I	ENCAn capture trigger input nm
ENCAnEC (n = 0, 1)	I	ENCAn encoder input (clear pulse)
$\overline{\text{ERROROUT\_M}}$	O	ECM error output (main)
$\overline{\text{ERROROUT\_C}}$	O	ECM error output (checker)
FLMODE	I	Operating mode select pin
MD0	I	Operating mode select pin 0
MD1	I	Operating mode select pin 1
INTPm (m = 0 to 7)	I	External interrupt input m
LPDCLK	I	LPD clock input (4-pin mode)
LPDCLKOUT	O	LPD clock output (4-pin mode)
LPDI	I	LPD data input (4-pin mode)
LPDO	O	LPD data output (4-pin mode)
$\overline{\text{LPDRST}}$	I	LPD Reset (4-pin mode)
P0_m (m = 0 to 15)	IO	Port 0_m
P1_m (m = 0 to 15)	IO	Port 1_m
P2_m (m = 0 to 7)	IO	Port 2_m
P3_m (m = 0 to 7)	IO	Port 3_m
P4_m (m = 0 to 15)	IO	Port 4_m
P5_m (m = 0 to 9)	IO	Port 5_m
P6_m (m = 2, 4, 6)	IO	Port 6_m
P7_m (m = 0, 2, 4)	IO	Port 7_m
P7_m (m = 8)	I	Port 7_m
SYSVCC	—	Voltage supply for system and PLL
VCC	—	Voltage supply for oscillator, flash memory, and port buffer
VDD	—	Voltage regulators voltage supply
VSS	—	Ground
RVCC	—	Voltage supply for RDC
RVSS	—	Ground for RDC
$\overline{\text{RESET}}$	I	External reset input
RDC3AnCOM (n = 0)	IO	Excitation common signal input/output
RDC3AnCOSMNT (n = 0)	O	COS-side monitoring signal output
RDC3AnRSO (n = 0)	IO	Excitation signal input/output
RDC3AnS1 (n = 0)	I	Resolver signal input
RDC3AnS2 (n = 0)	I	Resolver signal input
RDC3AnS3 (n = 0)	I	Resolver signal input
RDC3AnS4 (n = 0)	I	Resolver signal input
RDC3AnSINMNT (n = 0)	O	SIN-side monitoring signal output
RLIN3mRX (m = 0 to 2)	I	RLIN3m receive data input
RLIN3mTX (m = 0 to 2)	O	RLIN3m transmit data output
SCInRXD (n = 0 to 2)	I	SCIn receive data

Table 2.2 C1M-A1 Pin Function (3/3)

Pin Name	I/O	Function
SCInSCK (n = 0 to 2)	IO	SCIn clock
SCInTXD (n = 0 to 2)	O	SCIn transmit data
TAPAnESO (n = 0 to 1,3 to 4)	I	Hi-Z control
TAPAnUN (n = 0 to 1)	O	Motor control output U phase (negative)
TAPAnUP (n = 0 to 1)	O	Motor control output U phase (positive)
TAPAnVN (n = 0 to 1)	O	Motor control output V phase (negative)
TAPAnVP (n = 0 to 1)	O	Motor control output V phase (positive)
TAPAnWN (n = 0 to 1)	O	Motor control output W phase (negative)
TAPAnWP (n = 0 to 1)	O	Motor control output W phase (positive)
TPBAnO (n = 0)	O	TPBAn channel output
TAUDnIm (n = 0 to 1, m = 0 to 15)	I	TAUDn channel input m
TAUDnOm (n = 0 to 1, m = 0 to 15)	O	TAUDn channel output m
TAUJnIm (n = 0, m = 0 to 3)	I	TAUJn channel input m
TAUJnOm (n = 0, m = 0 to 3)	O	TAUJn channel output m
TSG3nOm (n = 0 to 1, m = 0 to 7)	O	TSG3n channel output m
X1, X2	—	Crystal oscillator connections
RSENTnRX (n = 0 to 3)	I	SENT input
RSENTnSPCO (n = 0 to 3)	O	SENT control output
RDC3An_OUT_U (n = 0)	O	RDC U-phase output
RDC3An_OUT_V (n = 0)	O	RDC V-phase output
RDC3An_OUT_W (n = 0)	O	RDC W-phase output

CAUTION

In C1M-A1, use SCI30 with the alternative function pins within the same port group.

- When serial clock I/O signals are used
  - P5_0(SCI0RXD), P5_1(SCI0TXD), P5_2(SCI0SCK)
- When serial clock I/O signals are not used
  - P5_0(SCI0RXD), P5_1(SCI0TXD)
  - P7_2(SCI0RXD), P7_4(SCI0TXD)

Section 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1 lists absolute maximum ratings.

Table 3.1 Absolute Maximum Ratings

Item		Symbol	Rated Value	Unit	Note
Power voltage*1	SYSVCC, VCC	VCC	– 0.3 to + 6.5	V	
	VDD	VDD	– 0.3 to + 1.8	V	
Input voltage	SYSVCC power pin	Vin	– 0.3 to SYSVCC + 0.3	V	See **Table 3.2** for intended pins
	VCC power pin	Vin	– 0.3 to VCC + 0.3	V	
Analog power voltage		A0VCC, A1VCC, A2VCC	– 0.3 to + 6.5	V	
		RVCC	– 0.3 to + 6.5	V	
Analog reference voltage		A0VREFH	– 0.3 to A0VCC + 0.3	V	
		A1VREFH	– 0.3 to A1VCC + 0.3	V	
		A2VREFH	– 0.3 to A2VCC + 0.3	V	
Analog input voltage		V_{AIN}	– 0.3 to A0VCC + 0.3 – 0.3 to A1VCC + 0.3 – 0.3 to A2VCC + 0.3	V	
		V_{RIN}	– 0.3 to RVCC + 0.3	V	
VSS differential voltage (Condition: Between any two of VSS, A0VSS, A1VSS, A2VSS, and RVSS)			– 0.1 to + 0.1	V	
Maximum input current (per pin)	Digital input pin	Imax	– 25 to + 25	mA	Only 1 pin simultaneously
	Analog input pin	Imax	– 25 to + 25	mA	
Junction temperature*1		Tj	– 40 to + 150	ºC	
Storage temperature		Tstg	– 55 to + 150	ºC	After installation

Note 1. Cumulative hours of operation of this LSI with Tj in the range from 125°C to 150°C must be kept within 3000

NOTE

Using this LSI without observing these absolute maximum ratings may result in permanent breakdown of the LSI.

This product is used in combination of multiple power voltages simultaneously in some cases. Use this LSI conforming to power pin connections, conditions for combination of power voltages to be applied, voltages that can be applied to pins, and output voltage conditions, which are specified in the manual. Using this LSI with unspecified power connection or voltage may result in permanent breakdown of the LSI or damage to the system that contains this LSI.

Input voltage, analog reference voltage and analog input voltage must not exceed 6.5 V.

3.2 DC Characteristics

3.2.1 Relationship between Power Name and Pin

Table 3.2 shows the relationship between power name and pin.

Table 3.2 Relationship between Power Name and Pin

Pin Name (Initial Value)	Circuit Power Name	I/O	Input Buffer Type	Note
Px_x	VCC	I/O	Schmitt B	Variable driving ability
P7_8	SYSVCC	I	Schmitt A	
ADCC0Ixx	A0VCC	I*1	Analog (ADC)	
ADCC1Ixx	A1VCC	I	Analog (ADC)	
ADCC2Ixx	A2VCC	I	Analog (ADC)	
RDC3AnSx*2	RVCC	I	Analog (RDC)	
RDC3AnRSO*2	RVCC	IO	—	
RDC3AnCOM*2	RVCC	IO	—	
$\overline{\text{RESET}}$	SYSVCC	I	Schmitt A	
FLMODE	SYSVCC	I	Schmitt A	
MD0	SYSVCC	I	Schmitt A	
MD1	SYSVCC	I	Schmitt A	
$\overline{\text{ERROROUT\_M}}$	VCC	O	—	
X1	VCC	I	CMOS	
X2	VCC	O	—	
$\overline{\text{AUDRST}}$	VCC	I	Schmitt A	
AUDCK	VCC	I	CMOS	
AUDSYNC	VCC	I	CMOS	
AUDATAx	VCC	I/O	CMOS	
$\overline{\text{DCUTRST}}$ / $\overline{\text{LPDTRST}}$	VCC	I	Schmitt A	
DCUTDO/LPDO	VCC	O	—	
DCUTMS	VCC	I	CMOS	
DCUTCK/LPDCLK	VCC	I	CMOS	
DCUTDI/LPDI	VCC	I	CMOS	
$\overline{\text{DCURDY}}$ /LPDCLKOUT	VCC	O	—	

Note 1. Some pins also serve as RDC3A pins. Following pins are I/O for both functions.
ADCC1I00/RDC3A0SINMNT, ADCC1I01/RDC3A0COSMNT, ADCC0I12/RDC3A1SINMNT, ADCC0I13/RDC3A1COSMNT

Note 2. C1M-A2: n = 0-1, C1M-A1: n = 0

NOTE

A through current may develop within the pin when an intermediate potential is applied in a DC manner, even if the input buffer is of the Schmitt buffer type (Schmitt A, B).

3.2.2 Recommended Operating Conditions

Table 3.3 Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit	Note
SYSVCC	4.5	5.0	5.5	V	—
VCC	4.5	5.0	5.5		—
VDD	1.15	1.25	1.35		—
A0VCC, A1VCC,A2VCC*1	4.5	5.0	5.5		—
RVCC*1	4.5	5.0	5.5		—
A0VREFH, A1VREFH, A2VREFH*2	4.5	5.0	5.5		—

Note: VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V must be kept.

Note 1. A0VCC, A1VCC, A2VCC, and RVCC must be connected to the same electric potential.

Note 2. Do not exceed A0VCC, A1VCC, or A2VCC.

3.2.3 Input Voltage Characteristics

Table 3.4 DC Characteristics (Input Voltage)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = – 40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Schmitt trigger input voltage (Buffer type A)	SYSVCC VCC	V_T^+ (V_{IH})	SYSVCC × 0.75 VCC × 0.75	—	SYSVCC + 0.3 VCC + 0.3	V	**Table 3.2** (Item of Schmitt A input buffer type)
		V_T^- (V_{IL})	–0.3	—	SYSVCC × 0.25 VCC × 0.25	V	
		V_{HS}	SYSVCC × 0.2 VCC × 0.2	—	—	V	
Schmitt trigger input voltage (Buffer type B)	VCC	V_T^+ (V_{IH})	VCC × 0.7	—	VCC + 0.3	V	**Table 3.2** (Item of Schmitt B input buffer type)
		V_T^- (V_{IL})	–0.3	—	VCC × 0.42	V	
		V_{HS}	VCC × 0.082	—	—	V	
CMOS input voltage	VCC	V_{IH}	VCC × 0.7	—	VCC + 0.3	V	**Table 3.2** (Item of CMOS input buffer type)
		V_{IL}	–0.3	—	VCC × 0.2	V	

3.2.4 Input Leak Current Characteristics

Table 3.5 DC Characteristics (Input Leak Current)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Input leak current	Other than A/D port and R/D port*1	I lin I	—	—	1	µA	Vin = 0 V to SYSVCC Vin = 0 V to VCC
	A/D port	I lin I	—	—	0.1	µA	Vin = 0 V to A0VCC, A1VCC, A2VCC
	R/D port	I lin I	—	—	0.3	µA	Vin = 0 V to RVCC, and stopping RDC3A

Note 1. X1 pin is not intended. Pull-up/pull-down pins are also not intended.

3.2.5 Pull-Up/Pull-Down MOS Current Characteristics

Table 3.6 DC Characteristics (Pull-Up/pull-Down MOS Current)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Input pull-up MOS current	DCUTMS, DCUTCK, DCUTDI	I_{pu}	—	—	350	µA	Vin = 0 V VCC = 4.5 to 5.5 V
	AUDCK, $\overline{\text{AUDSYNC}}$, AUDATA3-0*1		—	—	350	µA	Vin = 0 V VCC = 4.5 to 5.5 V
	General port		—	—	350	µA	Vin = 0 V, VCC = 4.5 to 5.5 V
Input pull-down MOS current	$\overline{\text{RESET}}$	I_{pd}	25	160	350	µA	Vin = SYSVCC = 4.5 to 5.5 V
	$\overline{\text{DCUTRST}}$		—	—	350	µA	Vin = SYSVCC = 4.5 to 5.5 V
	FLMODE, MD0, MD1		15	—	350	µA	Vin = SYSVCC = 4.5 to 5.5 V
	$\overline{\text{AUDRST}}$		—	—	350	µA	Vin = VCC = 4.5 to 5.5 V
	General port		—	—	350	µA	Vin = VCC = 4.5 to 5.5 V

Note 1. The pull-up of AUDATA3-0 is valid not only in input but also in output.

3.2.6 Output Voltage Characteristics

Table 3.7 DC Characteristics (Output Voltage)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Output high level voltage	VCC power supply system pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = 200 µA VCC = 4.5 to 5.5 V
			VCC – 1.0	—	—	V	I_{OH} = 1 mA VCC = 4.5 to 5.5 V
Output low level voltage	VCC power supply system pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA VCC = 4.5 to 5.5 V
			—	—	1.2	V	I_{OL} = 4 mA VCC = 4.5 to 5.5 V

3.2.7 Allowable Output Current

Table 3.8 DC Characteristics (Allowable Output Current)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Output low-level allowable current (per pin)	IOL	—	—	4.0	mA	
Output low-level allowable current (total)	ΣIOL	—	—	80.0	mA	
Output high-level allowable current (per pin)	IOH	—	—	2.0	mA	
Output high-level allowable current (total)	ΣIOH	—	—	25.0	mA	

This item affects the calorific value and Tj of the chip. In addition to these restrictions, you also need to take thermal design into consideration.

3.2.8 Injection Current

Table 3.9 DC Characteristics (Injection Current)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit
DC injection current (per pin)	Logic pin	IIC	–2.0	—	2.0	mA
	Analog pin*1		–3.0	—	3.0	mA
DC injection current (total)		Σ|IIC|	–50.0	—	50.0	mA

This item affects the calorific value and Tj of the chip. In addition to these restrictions, you also need to take thermal design into consideration.

Note 1. The objects are ADCCn pins. However, the following pins are excluded:
ADCC1I00, ADCC1I01, ADCC0I12, ADCC0I13

3.2.9 Input Capacitance

Table 3.10 DC Characteristics (Input Capacitance)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Input capacitance	All pins	Cin	—	10	20	pF	Vin = 0 V, f = 1 MHz Tj = 25ºC

3.2.10 Supply Current Characteristics

Table 3.11 DC Characteristics (Supply Current: C1M-A2)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Core supply current	Normal operation	I_{dd}	—	—	730	mA	
(VDD power supply)	Current during reset	I_{ddrst}	—	—	335	mA	
VCC power supply current	Normal operation (excluding erasure of code flash)	I_{CC}	—	—	25	mA	Excluding I/O current
	Erasure of code flash	$I_{cc\_cferase}$	—	—	60	mA	Excluding I/O current, *1
	Current during reset	I_{ccrst}	—	—	15	mA	
System supply current	Normal operation	I_{SYS}	—	—	7	mA	Including PLL current
(SYSVCC power supply)	Current during reset	I_{sysrst}	—	—	3	mA	
Analog power supply current (A0VCC, A1VCC, A2VCC power supply)		I_{AVCC}	—	—	30	mA	
Analog power supply current (RVCC power supply)		I_{RVCC}	—	—	20	mA	
ADC reference power supply current (A0VREFH, A1VREFH, A2VREFH)		I_{AVREF}	—	—	0.5	mA	

Note 1. Large fluctuations in current occur during erasure. The average current is 15 mA.

CAUTIONS

1. When the A/D converter is not used or it is in the standby state, do not open the A0VCC pin, A1VCC pin, A2VCC pin, A0VREFH pin, A1VREFH pin, A2VREFH pin, A0VSS pin, A1VSS pin, and A2VSS pin.
2. Supply current values are those measured when VIHmin = VCC – 0.5 V and VIL = 0.5 V with no load applied to all output pins.

Table 3.12 DC Characteristics (Supply Current: C1M-A1)

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Core supply current	Normal operation	I_{dd}	—	—	540	mA	
(VDD power supply)	Current during reset	I_{ddrst}	—	—	335	mA	
VCC power supply current	Normal operation (excluding erasure of code flash)	I_{CC}	—	—	25	mA	Excluding I/O current
	Erasure of code flash	$I_{cc\_cferase}$	—	—	60	mA	Excluding I/O current, *1
	Current during reset	I_{ccrst}	—	—	15	mA	
System supply current	Normal operation	I_{SYS}	—	—	7	mA	Including PLL current
(SYSVCC power supply)	Current during reset	I_{sysrst}	—	—	3	mA	
Analog power supply current (A0VCC, A1VCC, A2VCC power supply)		I_{AVCC}	—	—	30	mA	
Analog power supply current (RVCC power supply)		I_{RVCC}	—	—	10	mA	
ADC reference power supply current (A0VREFH, A1VREFH, A2VREFH)		I_{AVREF}	—	—	0.5	mA	

Note 1. Large fluctuations in current occur during erasure. The average current is 15 mA.

CAUTIONS

1. When the A/D converter is not used or it is in the standby state, do not open the A0VCC pin, A1VCC pin, A2VCC pin, A0VREFH pin, A1VREFH pin, A2VREFH pin, A0VSS pin, A1VSS pin, and A2VSS pin.
2. Supply current values are those measured when VIHmin = VCC – 0.5 V and VIL = 0.5 V with no load applied to all output pins.

3.3 AC Characteristics

Unless otherwise described, the following timing conditions are applied.

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

- In the port control register, conditions where all output pins of the module used in the same channel are set to the same driving ability are applied to output pins whose driving ability is selectable. Unless otherwise specified, all driving ability settings are included.

- Unless otherwise described, AC measurement conditions described in the figure below are applied.

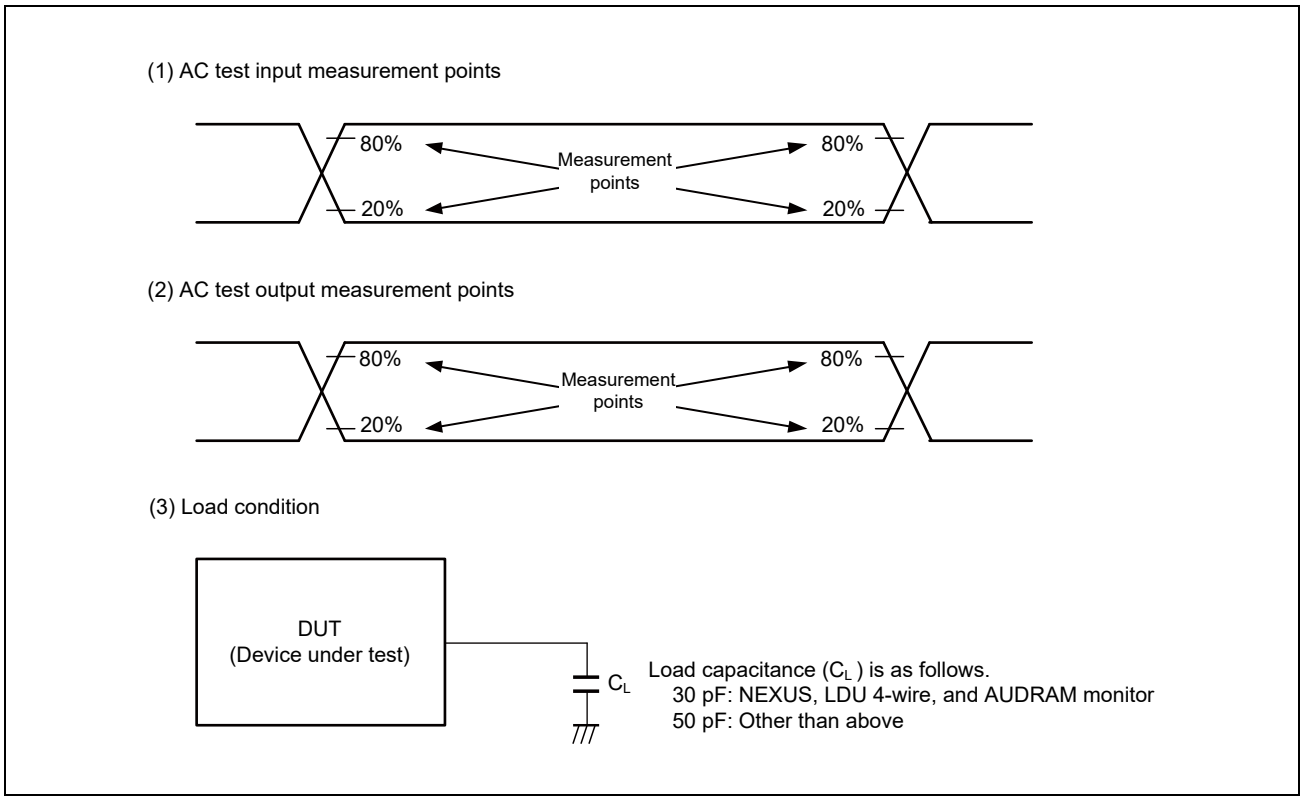


Figure 3.1 AC Measurement Conditions

3.3.1 Power On/Off Timings

Table 3.13 Power On/Off Timings

Item	Symbol	Min.	Max.	Unit	Note
Pin reset L time at power-on	tRESW1	10	—	ms	*1
Pin reset L time at power-off	tRESW2	0	—	µs	*2
PLL1 lock-in time	tPLL1L0	—	1	ms	*3

Note 1. tRESW1 is the reset time required for the supply of internal clock signals to become stable after all power voltages are turned on.

Note 2. tRESW2 is the time from assertion of the reset signal until all of the power voltages have dropped below the lower-limit voltages.

Note 3. tPLL1L0 is the time required for PLL1 to lock in after MOSC (main oscillator) oscillation has become stable.

CAUTIONS

- The states of I/O pins are not reset during the reset noise cancellation interval (max. 1.2 µs) following assertion of the reset signal while power is being turned off.
- If power is disconnected during programming or erasure of flash memory, data in the area of the flash memory that was being programmed or erased are not guaranteed.

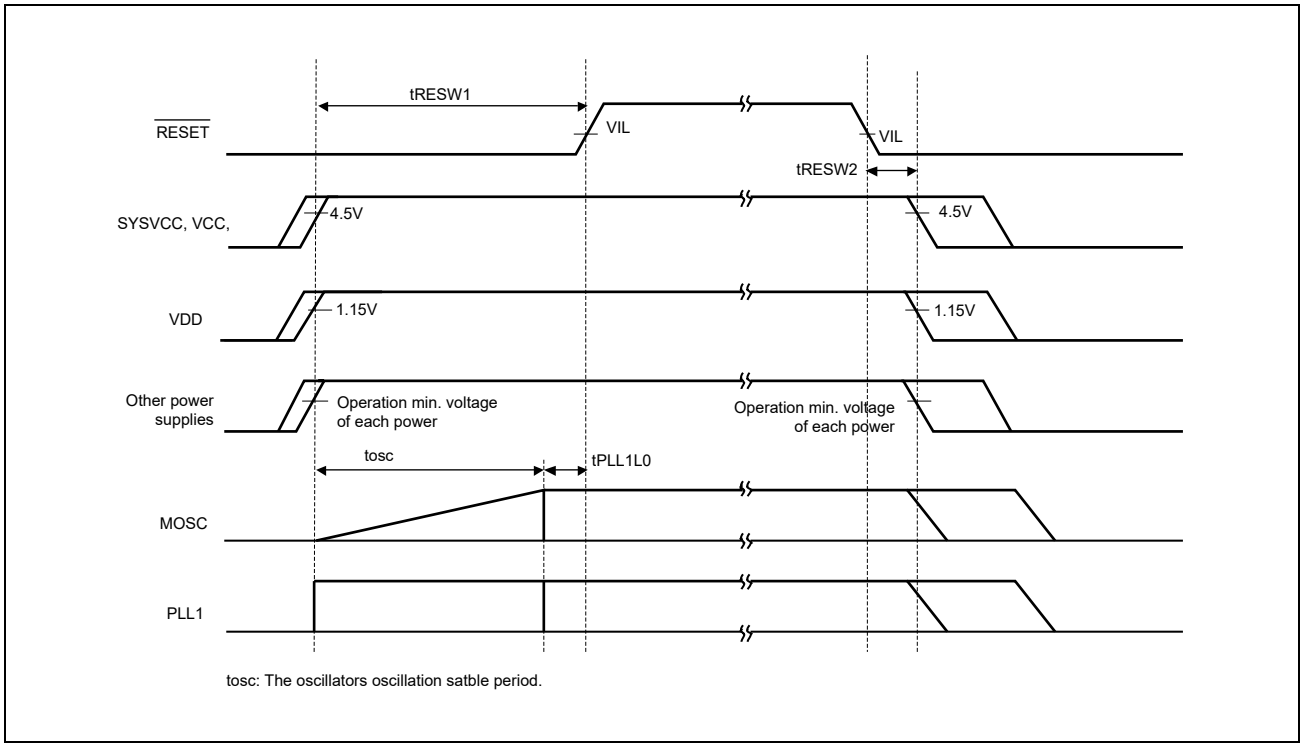


Figure 3.2 Power On/Off Timings

3.3.2 Clock Timing

3.3.2.1 Spread Spectrum Clock Generator

Table 3.14 SSCG Timing

Item	Symbol	Min.	Typ.	Max.	Unit
Modulation frequency*1	f_{mod}	20	—	100	kHz
Frequency dithering range*1	f_{dit}	4.1	—	—	%
Frequency stabilization time (OFF → ON)		—	—	1.6	ms

Note 1. The modulation method is applied only to down spread.

3.3.2.2 Oscillation Frequency Accuracy of the On-Chip Oscillator

Table 3.15 Oscillation Frequency Accuracy of the On-Chip Oscillator

Item	Symbol	Min.	Typ.	Max.	Unit
CLK_LIOSC oscillation frequency	fLIOSC	160	240	360	kHz

3.3.3 Output Slew Rate

VCC power supply pins

Table 3.16 Selection of Driving Ability = High

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rising time/falling time slew rate	tR, tF	CL = 25 pF	—	4	6	ns
		CL = 50 pF	—	6	12	ns
		CL = 75 pF	—	8	16	ns
		CL = 100 pF	—	10	20	ns

Table 3.17 Selection of Driving Ability = Mid

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rising time/falling time slew rate	tR, tF	CL = 25 pF	—	8	15	ns
		CL = 50 pF	—	15	30	ns
		CL = 75 pF	—	23	45	ns
		CL = 100 pF	—	30	60	ns

Table 3.18 Selection of Driving Ability = Low

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rising time/falling time slew rate	tR, tF	CL = 25 pF	—	25	50	ns
		CL = 50 pF	—	50	100	ns
		CL = 75 pF	—	70	120	ns
		CL = 100 pF	—	85	150	ns

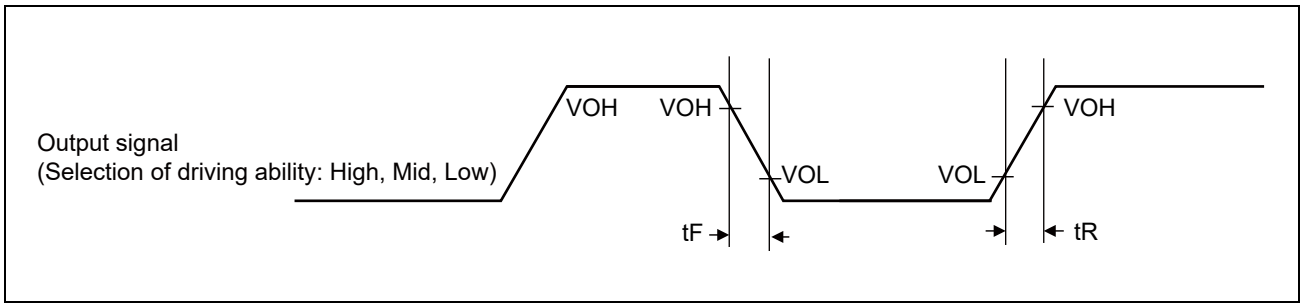


Figure 3.3 Output Signal Timing

3.3.4 Control Signal Timing

Table 3.19 Control Signals

Item	Symbol	Min.	Typ.	Max.	Unit
Reset pulse width*1	tRESW3	1.5	—	—	µs
Reset noise cancel width	tRESNCW	0.2	0.4	1.2	µs
IRQ pulse width*2	tIRQ	50	—	—	ns
Operating mode setup time	tMDS	1	—	—	ms
Operating mode hold time	tMDH	1	—	—	ms

Note 1. The reset pulse width must be equal to or more than the minimum tRESW3 value.
Any reset whose pulse width is less than the minimum value of the reset noise cancellation width will not be accepted.

Note 2. In case noise removal is disabled by DNF.

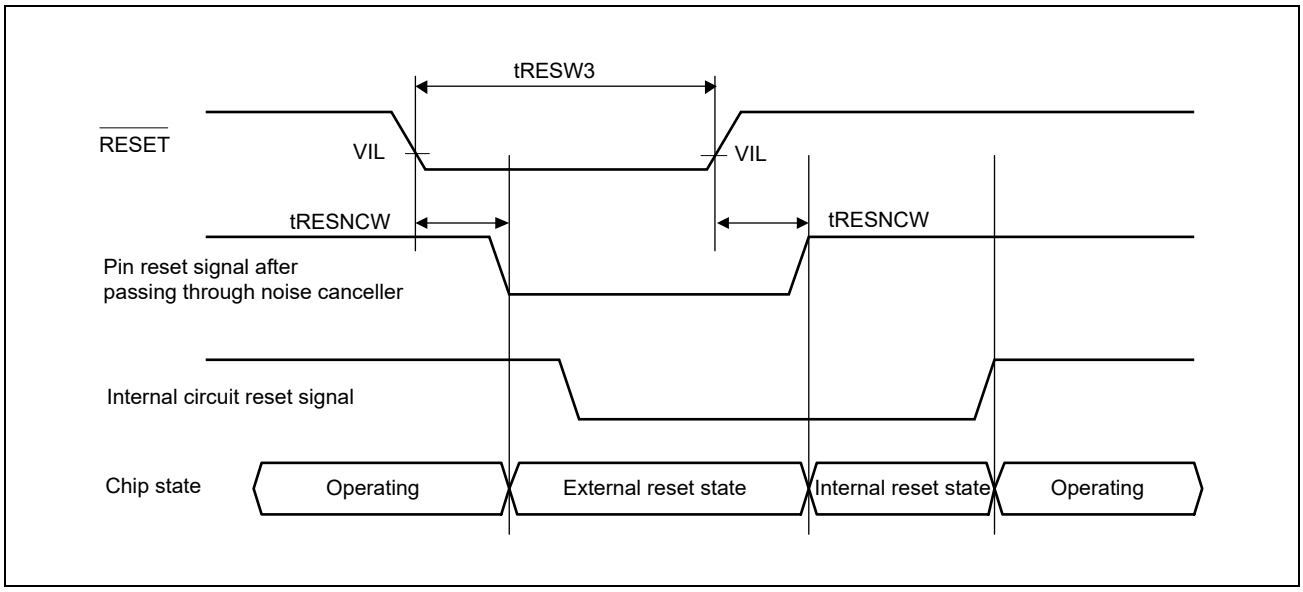


Figure 3.4 Reset Timing

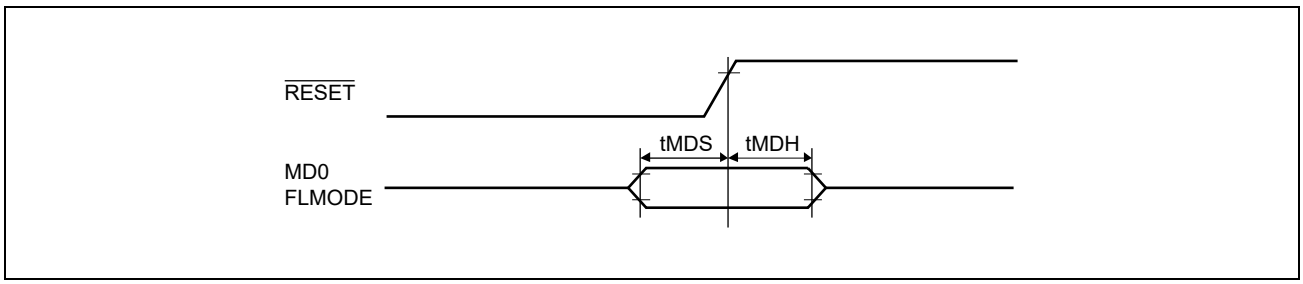


Figure 3.5 Control Signal Timing

3.3.5 CSIH Timing

3.3.5.1 Master Mode

Table 3.20 CSIH Timing in Master Mode

Conditions: CL = 50 pF, selection of driving ability = High

Item	Symbol	Condition	Min.	Max.	Unit
CSIHnSC cycle	tKCYM		100	—	ns
CSIHnSC output high-level width	tKWHM		(tKCYM/2) – 20	—	ns
CSIHnSC output low-level width	tKWLM		(tKCYM/2) – 20	—	ns
CSIHnSI input setup time	tSSIM		18	—	ns
CSIHnSI input hold time	tHSIM		10	—	ns
CSIHnSO output delay time	tDSOM		—	10	ns
CSIHnSO output hold time (vs. CSIHnSC)	tHSOM		tKWHM – 10	—	ns
CSIHnRYI setup time	tSRYI	HSE = 1	(2 × tPAck) + 30	—	ns
CSIHnCSSx inactive level width	tWSCSB	*1	(CSidle + 0.5) × tKCYM – 20	—	ns
		Other than above	CSidle × tKCYM – 20	—	ns
CSIHnCSSx setup time	tSSCSB0	DAP = 0	CSsetup × tKCYM – 10	—	ns
	tSSCSB1	DAP = 1	(CSsetup + 0.5) × tKCYM – 10	—	ns
CSIHnCSSx hold time	tHSCSB0	SIT = 0	CShold × tKCYM – 10	—	ns
	tHSCSB1	SIT = 1	(CShold + 0.5) × tKCYM – 10	—	ns

Note 1. When the serial clock level is changed during communication and when the idle time is set to 0.5 transmission clock periods.

Note: tPAck is the operating clock cycle of CSIH (80 MHz SSCG)

n = 0 to 2, x = 0 to 3

CSsetup : CSIHnCFGx.CSIHnSPx3-0 set value

CShold : CSIHnCFGx.CSIHnHDx3-0 set value

CSidle : CSIHnCFGx.CSIHnIDx2-0 set value

DAP : CSIHnCFGx.CSIHnDAPx bit

SIT : CSIHnCTL1.CSIHnSIT bit

HSE : CSIHnCTL1.CSIHnHSE bit

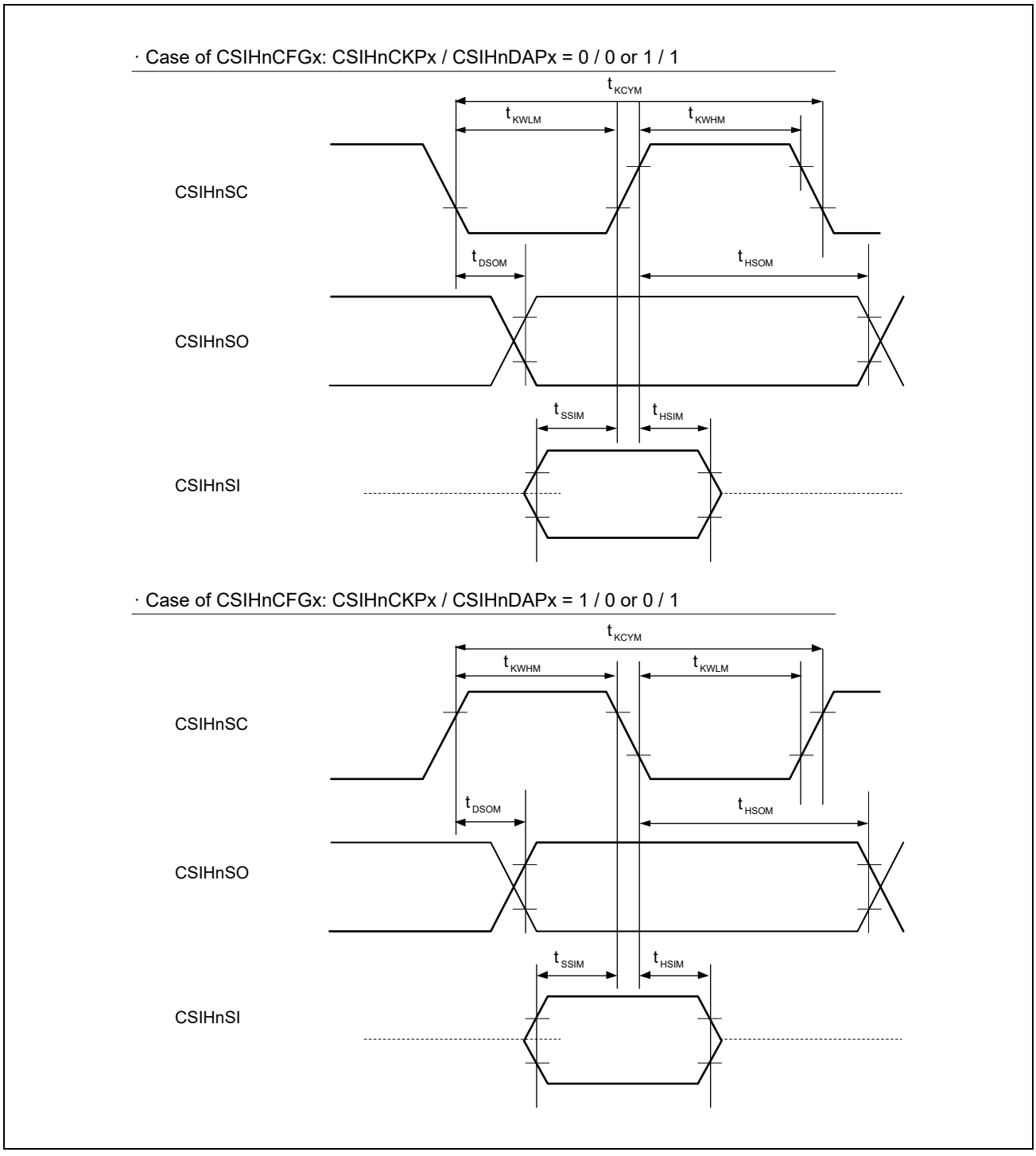


Figure 3.6 CSIH Timing (Master Mode) (1/4)

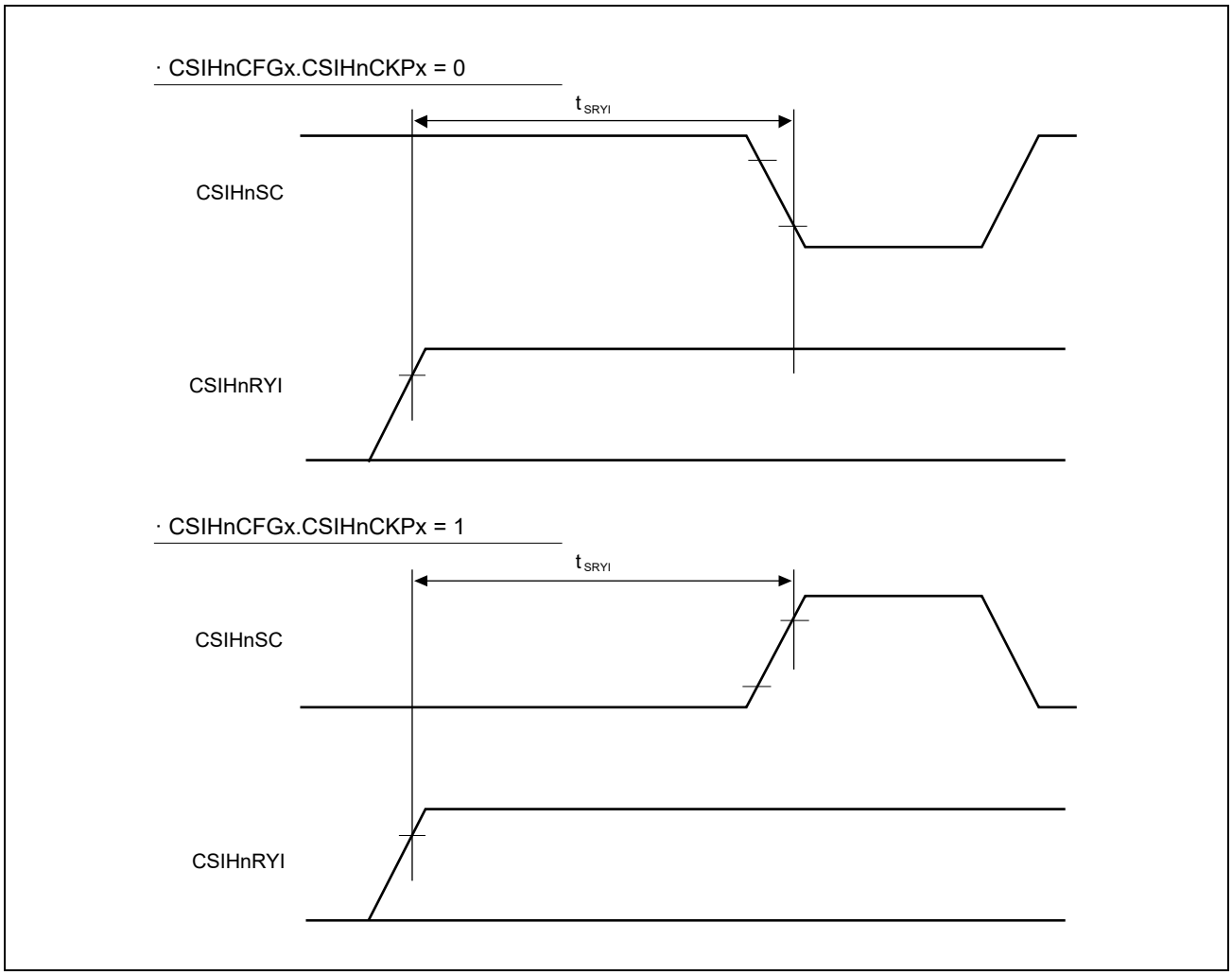


Figure 3.6 CSIH Timing (Master Mode) (2/4)

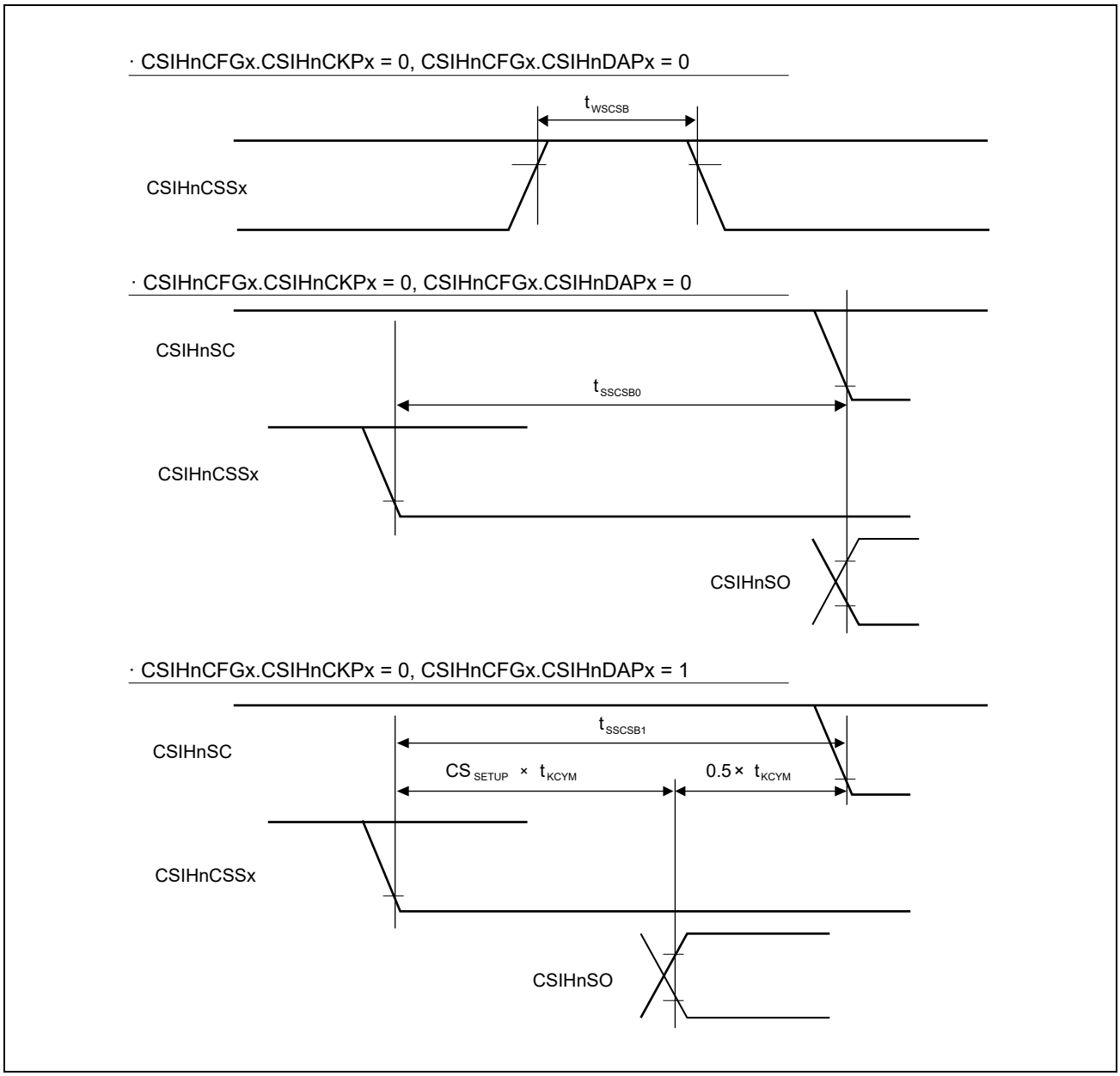


Figure 3.6 CSIH Timing (Master Mode) (3/4)

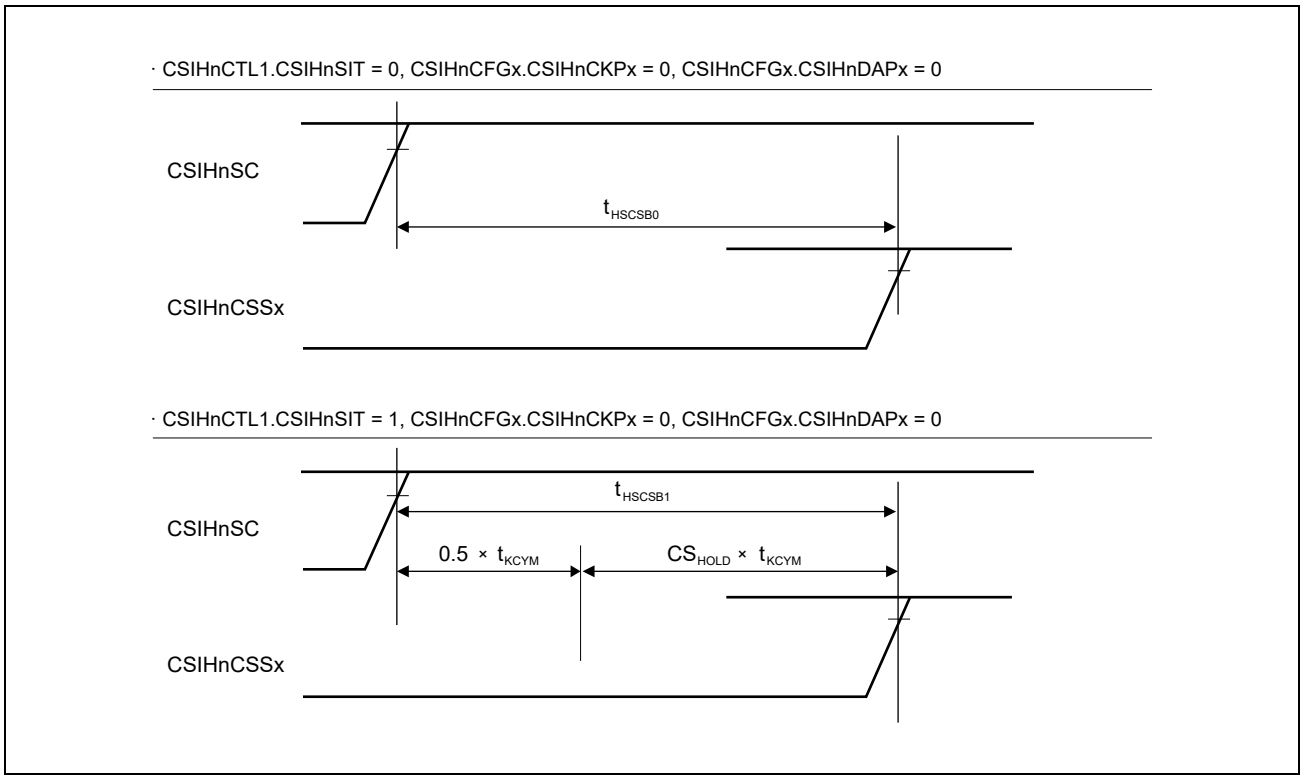


Figure 3.6 CSIH Timing (Master Mode) (4/4)

3.3.5.2 Slave Mode

Table 3.21 CSIH Timing in Slave Mode

Conditions: CL = 50 pF, selection of driving ability = High

Item	Symbol	Condition	Min.	Max.	Unit
CSIHnSC cycle	tKCYS		200	—	ns
CSIHnSC input high-level width	tKWHS		(tKCYS/2) – 30	—	ns
CSIHnSC input low-level width	tKWLS		(tKCYS/2) – 30	—	ns
CSIHnSI input setup time	tSSIS		15	—	ns
CSIHnSI input hold time	tHSIS		tPAck + 15	—	ns
CSIHnSO output delay time	tDSOS		—	30	ns
CSIHnSO output hold time (vs. CSIHnSC)	tHSOS		tKWHS	—	ns
CSIHnRYO output delay time	tSRYO		—	30	ns
$\overline{\text{CSIHnSSI}}$ setup time	tSSSIS		0.5 × tKCYS	—	ns
$\overline{\text{CSIHnSSI}}$ hold time	tHSSIS		tPAck + 30	—	ns
Slave output release time	tREL		—	100	ns

Note: tPAck is the operating clock cycle of CSIH (80 MHz SSCG).

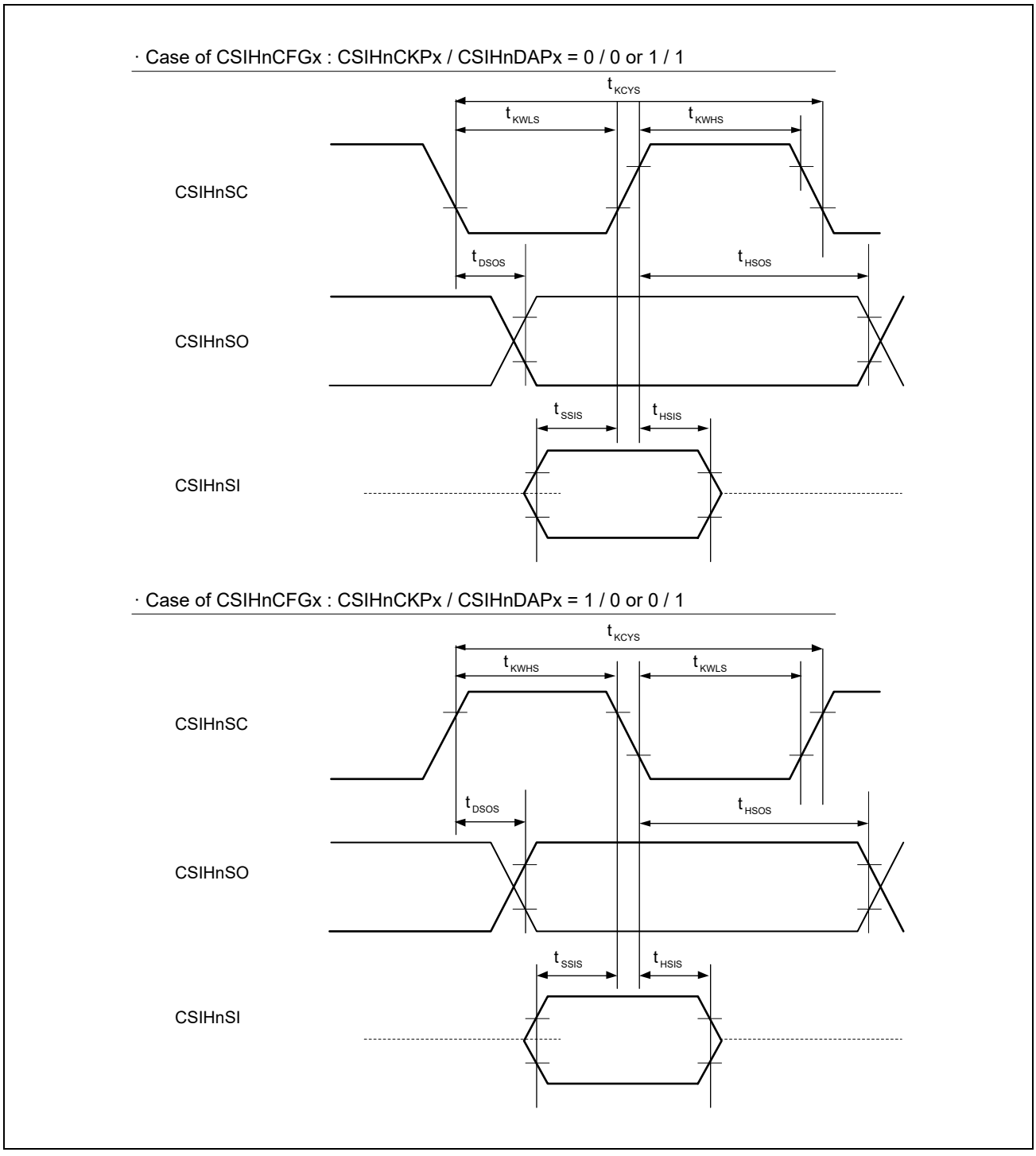


Figure 3.7 CSIH Timing (Slave Mode) (1/3)

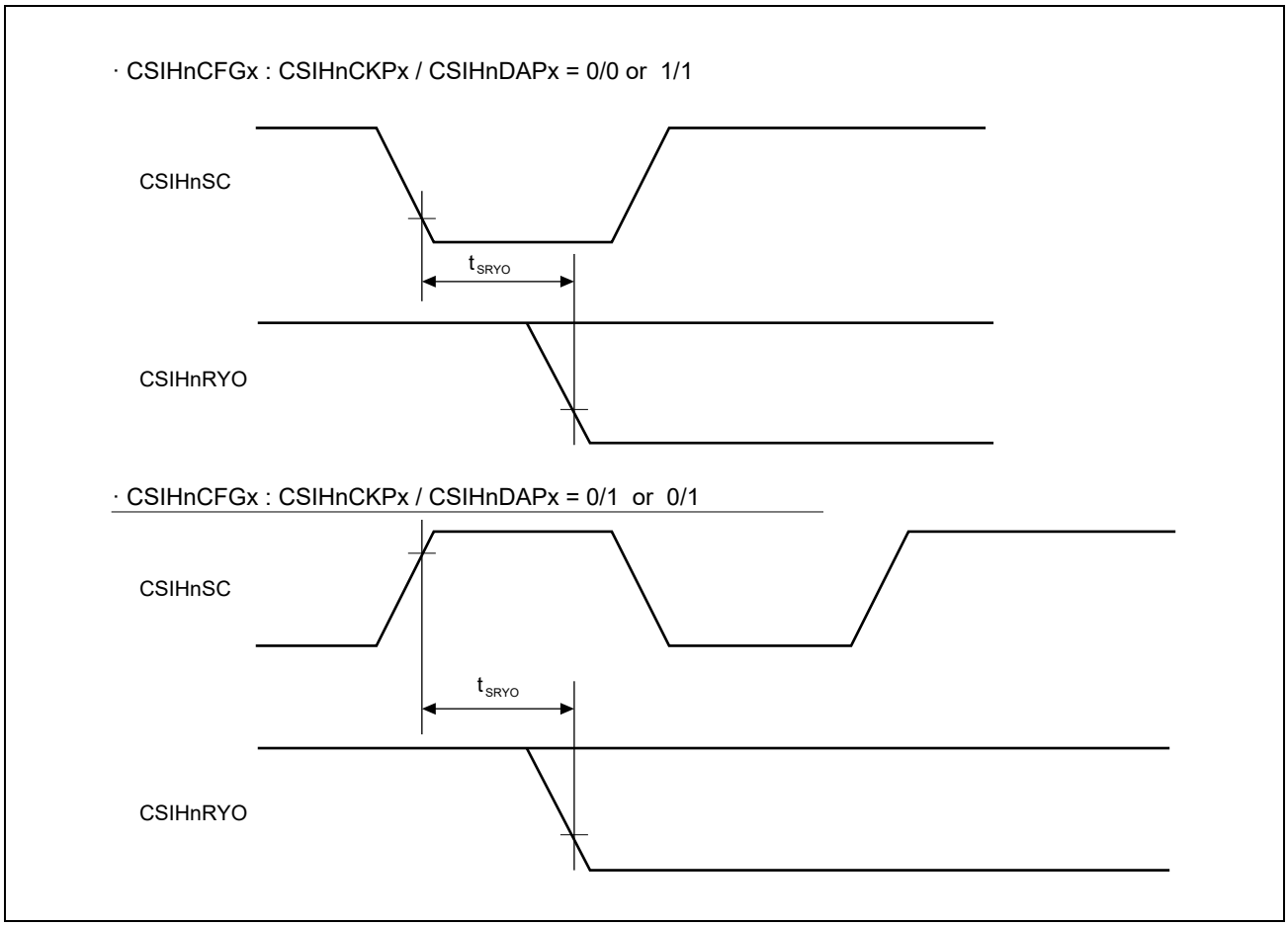


Figure 3.7 CSIH Timing (Slave Mode) (2/3)

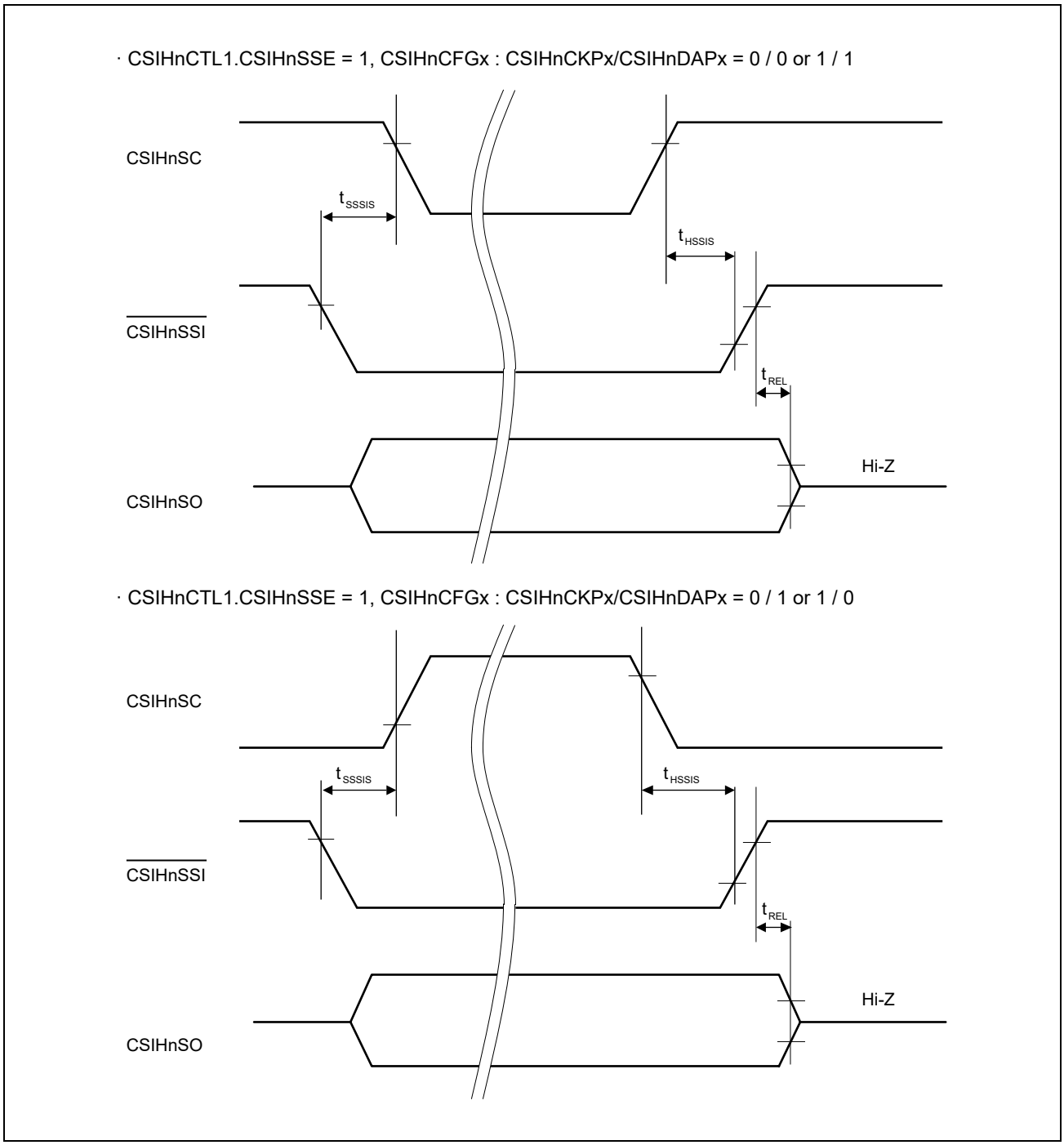


Figure 3.7 CSIH Timing (Slave Mode) (3/3)

3.3.6 SCI/FLSCI Timing

Table 3.22 SCI3 Timing (Master Mode)

Conditions: CL = 50 pF, selection of driving ability = High

Item	Symbol	Condition	Min.	Max.	Unit
Output clock cycle	tScyc	Asynchronous	8 × tPck	—	ns
		Clock synchronous	8 × tPck	—	ns
Output clock pulse width	tSCKW		0.4 × tScyc	0.6 × tScyc	ns
Transmit data delay time	tTXD	Clock synchronous	—	40	ns
Receive data setup time	tRXS	Clock synchronous	2 × tPck	—	ns
Receive data hold time	tRXH	Clock synchronous	2 × tPck	—	ns

Note: tPck is the operating clock cycle of SCI (40 MHz clean clock).

CAUTION

FLSCI does not support master mode.

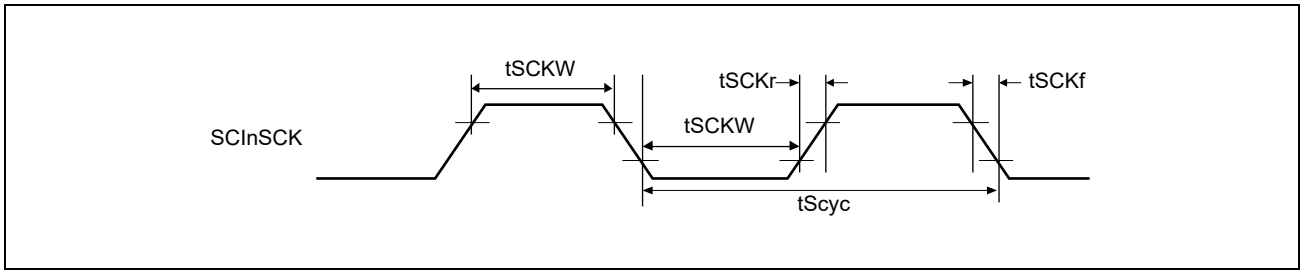


Figure 3.8 SCI Clock Input/Output Timing

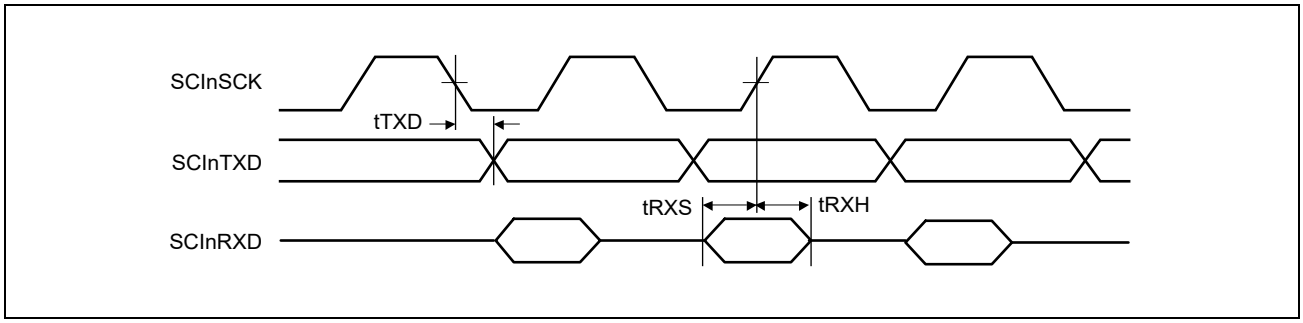


Figure 3.9 SCI Input/Output Timing, Clock Synchronous Mode

Table 3.23 SCI3 Timing (Slave Mode)

Conditions: CL = 50 pF, selection of driving ability = High

Item	Symbol	Min.	Typ.	Max.	Unit
Input clock cycle	tScyc	12 × tPck	—	—	ns
Input clock pulse width	tSCKW	0.4 × tScyc	—	0.6 × tScyc	ns
Input clock rising time	tSCKr	—	—	20	ns
Input clock falling time	tSCKf	—	—	20	ns
Transmit data delay time*1	tTXD	2 × tPck	—	50 + 3 × tPck	ns
Receive data setup time	tRXS	2 × tPck	—	—	ns
Receive data hold time	tRXH	2 × tPck	—	—	ns

Note 1. Applies to data other than “non-continuous transfer mode Data0 (1st bit).” The transmission of “non-continuous mode Data0 (1st bit)” is initiated at the same time TDRE is set to 0.

Note: tPck is the operating clock cycle of SCI (40 MHz clean clock).
Asynchronous clock input mode is not supported.

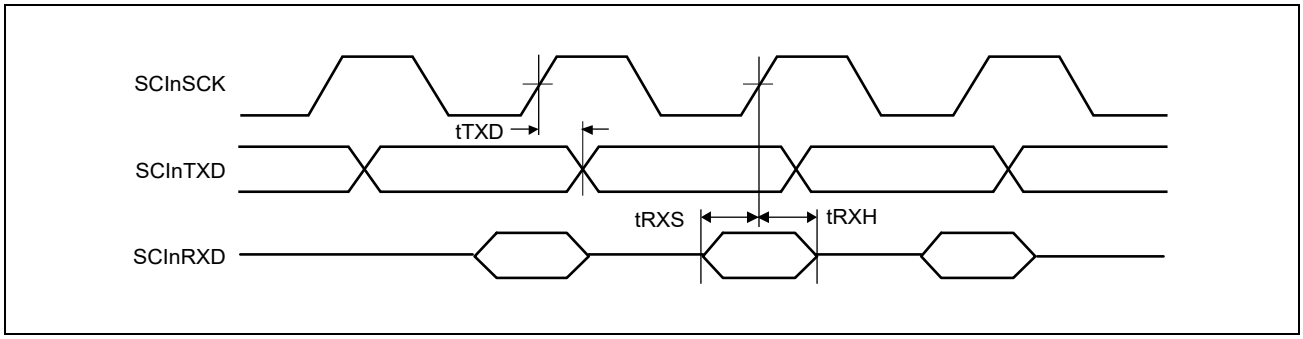


Figure 3.10 SCI Input/Output Timing, Clock Synchronous Mode (in Slavel Mode)

3.3.7 RS-CANFD Timing

Table 3.24 RS-CANFD Timing

Conditions: CL = 50 pF, selection of driving ability = High

Item	Symbol	Condition.	Min.	Typ.	Max.	Unit
Transfer rate			—	—	5	Mbps
Internal delay time	t_{NODE}		—	—	50	ns

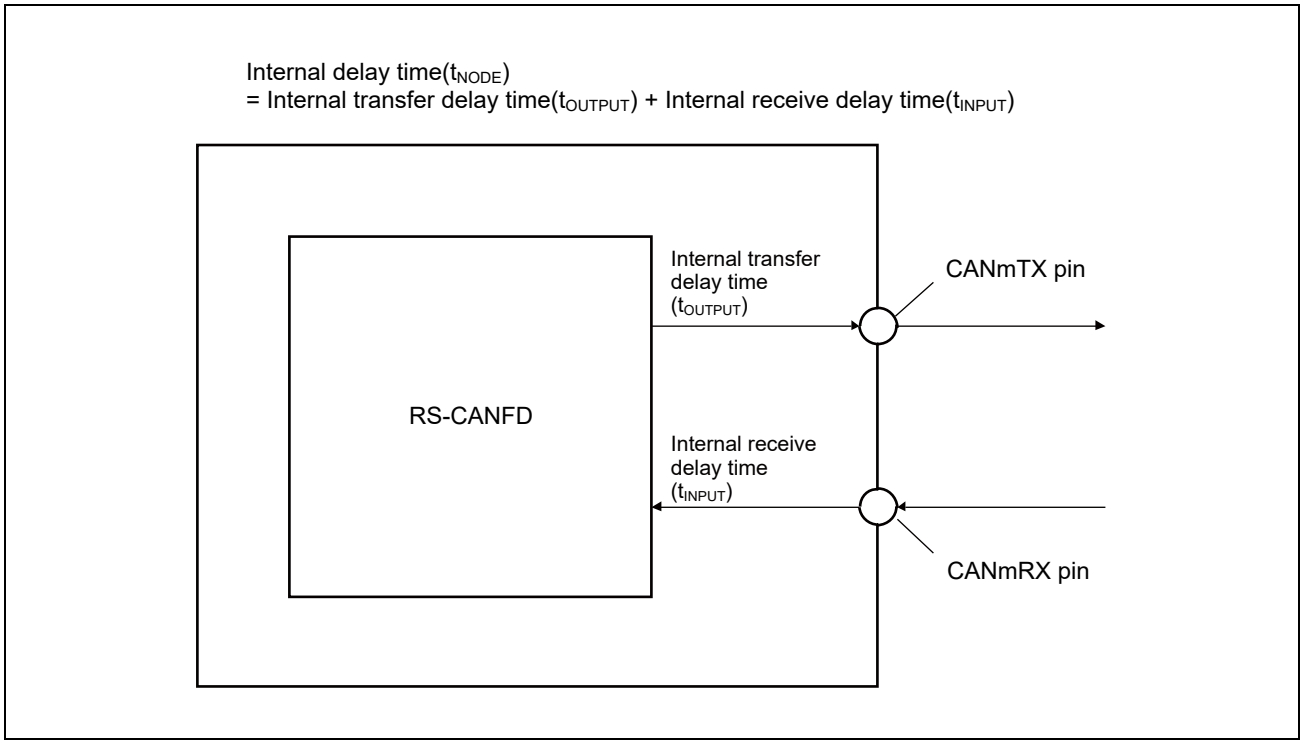


Figure 3.11 RS-CANFD Timing

Definition of internal delay time of RS-CANFD

Internal delay time (tNODE) = tOUTPUT + tINPUT

3.3.8 RLIN3 Timing

Table 3.25 RLIN3 Timing

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate		LIN function	—	—	20	kbps
		UART function	—	—	1.5	Mbps

3.3.9 Motor Control Signals Timing

Table 3.26 Motor Control Signals Timing

Item	Symbol	Condition	Min.	Max.	Unit
Input high-level width	tTIH	ENCAnE0-1, ENCAnEC*1, TAPAnESO	1.5 × tPck	—	ns
Input low-level width	tTIL	ENCAnE0-1, ENCAnEC*1, TAPAnESO	1.5 × tPck	—	ns

Note: In case noise removal is disabled by DNF

Note 1. When used as hall sensor inputs (TSG3nPTSI0-I2).

Note: tPck is the operating clock cycle of TSG3 (80 MHz clean clock).

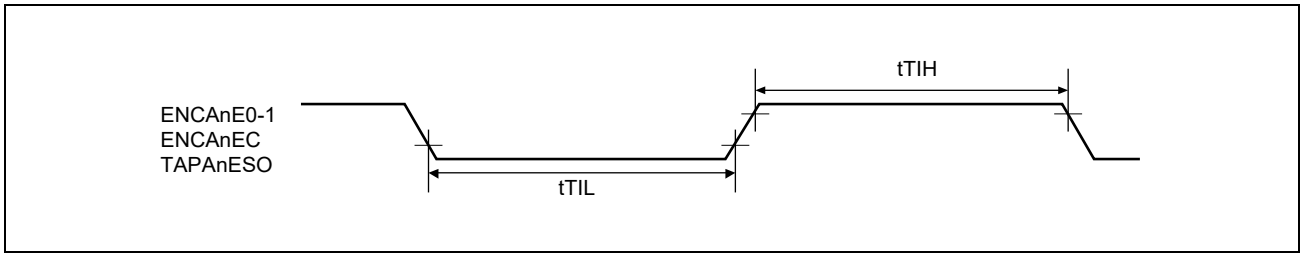


Figure 3.12 Motor Control Signals Timing

3.3.10 Timer Timing

Table 3.27 Timer Timing

Item	Symbol	Condition	Min.	Max.	Unit
Input high-level width	tTIH	TAUDnI0-15, TAUJnI0-3, ENCAnI0-1, ENCAnE0-1, ENCAnEC	1.5 × tPck	—	ns
Input low-level width	tTIL	TAUDnI0-15, TAUJnI0-3, ENCAnI0-1, ENCAnE0-1, ENCAnEC	1.5 × tPck	—	ns

Note: In case noise removal is disabled by DNF.

Note: tPck is the operating clock cycle of the timer (80 MHz clean clock).

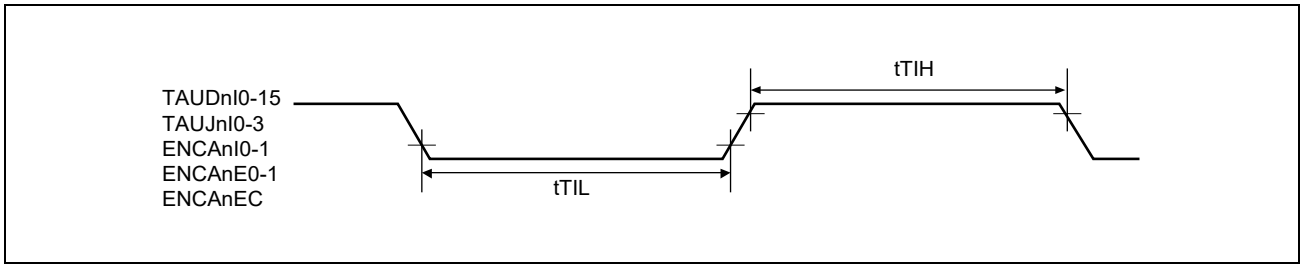


Figure 3.13 Timer Timing

3.3.11 JTAG/NEXUS Timing

Table 3.28 JTAG/NEXUS Timing

Conditions: CL = 30 pF

Item	Symbol	Condition	Min.	Max.	Unit
DCUTCK cycle time	tTCKW		50	—	ns
DCUTCK high-level width	tTCKWH		21	—	ns
DCUTCK low-level width	tTCKWL		21	—	ns
DCUTMS, DCUTDI setup time (vs. DCUTCK ↑)	tTISU		12	—	ns
DCUTMS, DCUTDI hold time (vs. DCUTCK ↑)	tTIH		12	—	ns
DCUTDO output delay time (vs. DCUTCK ↓)	tTDOD		—	tTCKW-20	ns
$\overline{\text{DCURDY}}$ output delay time (vs. DCUTCK ↓)	tRDYD		—	tTCKW-20	ns
$\overline{\text{DCUTRST}}$ low-level width	tTRSTWL		1200	—	ns
$\overline{\text{DCUTRST}}$ /DCUTCK/DCUTMS/DCUTDI input rising time	tTIR		—	12	ns
$\overline{\text{DCUTRST}}$ /DCUTCK/DCUTMS/DCUTDI input falling time	tTIF		—	12	ns

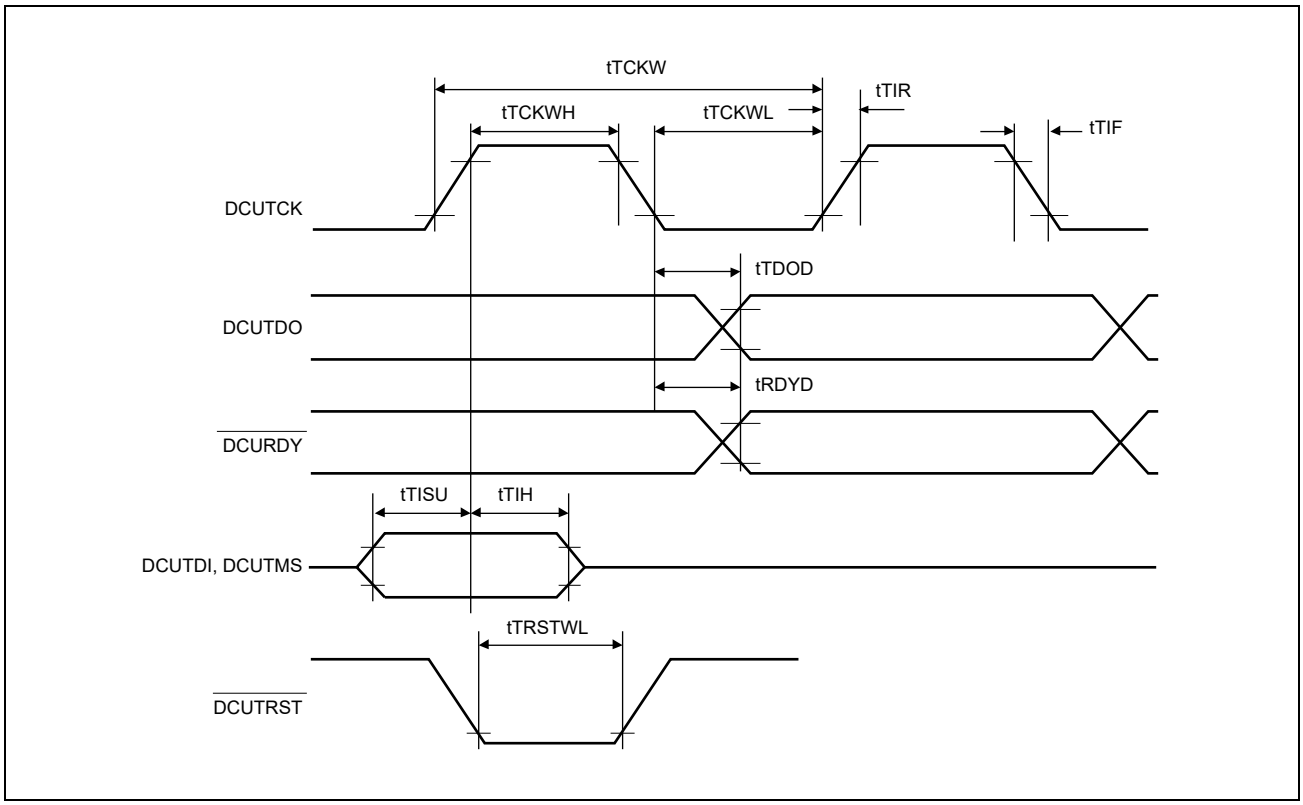


Figure 3.14 JTAG/NEXUS Timing

3.3.12 LPD (4-pin) Timing

Table 3.29 LPD (4-pin) Timing

Conditions: Tj = –40ºC to 150ºC, CL = 30 pF

Item	Symbol	Condition	Min.	Max.	Unit
LPDCLK cycle	tLPDCKW		25	—	ns
LPDCLK high-level width	tLPDCKWH		4.5	—	ns
LPDCLK low-level width	tLPDCKWL		4.5	—	ns
LPDCLK input rising time	tLPDCKR		—	8	ns
LPDCLK input falling time	tLPDCKF		—	8	ns
LPDI setup time (to LPDCLK ↑)	tLPDSU		2	—	ns
LPDI hold time (from LPDCLK ↑)	tLPDH		2	—	ns
LPDCLKOUT cycle time	tLPDCKOW		25	—	ns
LPDCLKOUT high-level width	tLPDCKOWH		4.5	—	ns
LPDCLKOUT low-level width	tLPDCKOWL		4.5	—	ns
LPDCLKOUT rising time	tLPDCKOR		—	8	ns
LPDCLKOUT falling time	tLPDCKOF		—	8	ns
LPDO output delay (from LPDCLKOUT ↑)	tLPDOD		0	12	ns

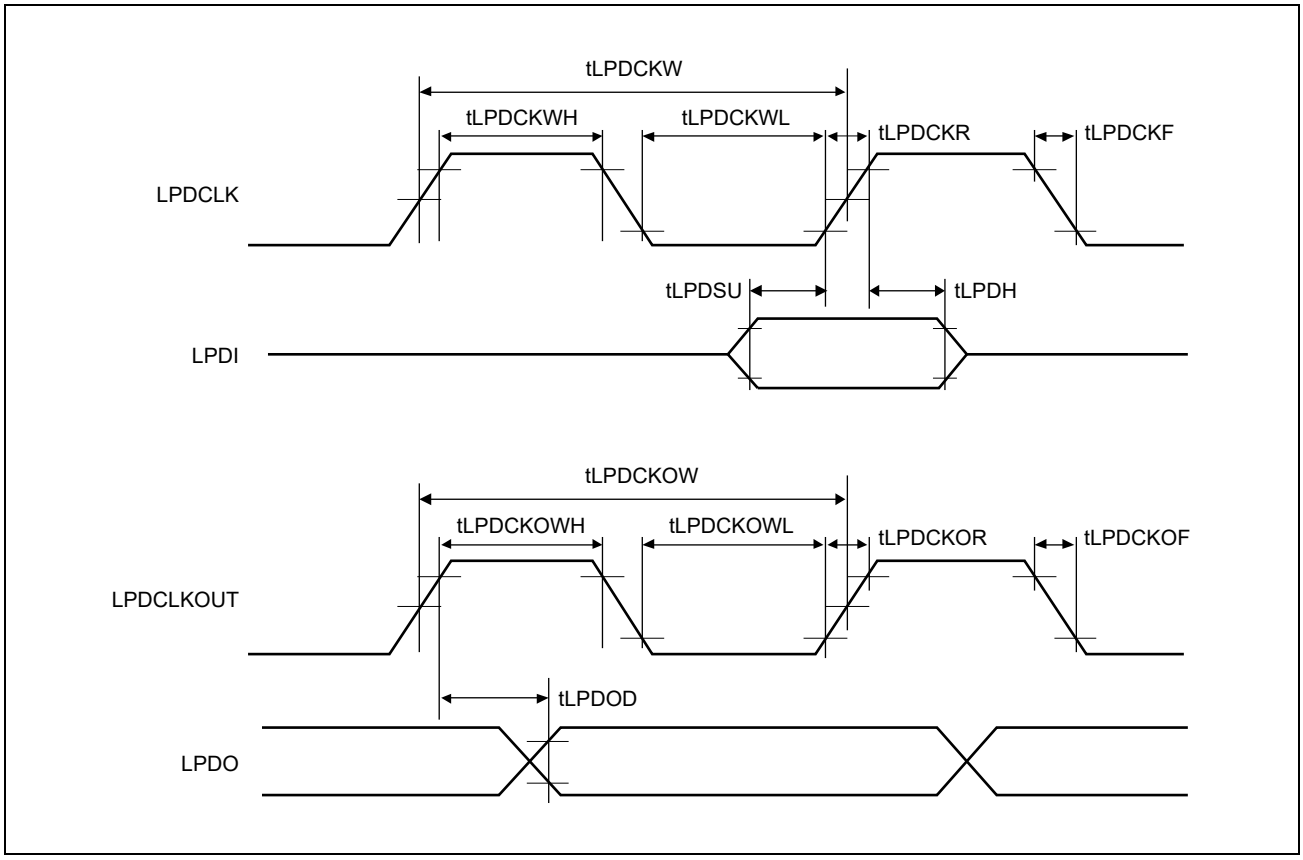


Figure 3.15 LDU 4-Wire Timing

3.3.13 AUD RAM Monitor

Table 3.30 AUD RAM Monitor Timing

Conditions: Tj = – 40ºC to 150ºC, CL = 30 pF

Item	Symbol	Min.	Max.	Unit
AUDCK cycle time (monitor mode)	tAUCKMcyc	50	—	ns
AUDCK high-level width (monitor mode)	tAUCKMH	0.4 × tAUCKMcyc	—	ns
AUDCK low-level width (monitor mode)	tAUCKML	0.4 × tAUCKMcyc	—	ns
$\overline{\text{AUDRST}}$ setup time (monitor mode, vs. AUDCK↑)	tAURSTMS	30	—	ns
$\overline{\text{AUDRST}}$ input pulse width (monitor mode)	tAURSTMW	5 × tAUCKMcyc	—	ns
Monitor data output delay time (to AUDCK ↑)	tAUDTMD	—	35	ns
Monitor data input setup time (to AUDCK ↑)	tAUDTMS	15	—	ns
Monitor data input hold time (from AUDCK ↑)	tAUDTMH	5	—	ns
$\overline{\text{AUDSYNC}}$ input setup time (vs. AUDCK ↑)	tAUDSYS	15	—	ns
$\overline{\text{AUDSYNC}}$ input hold time (vs. AUDCK ↑)	tAUDSYH	5	—	ns
AUDISR setup time	tAUDMDS	1	—	ms
AUDISR hold time	tAUDMDH	1	—	ms

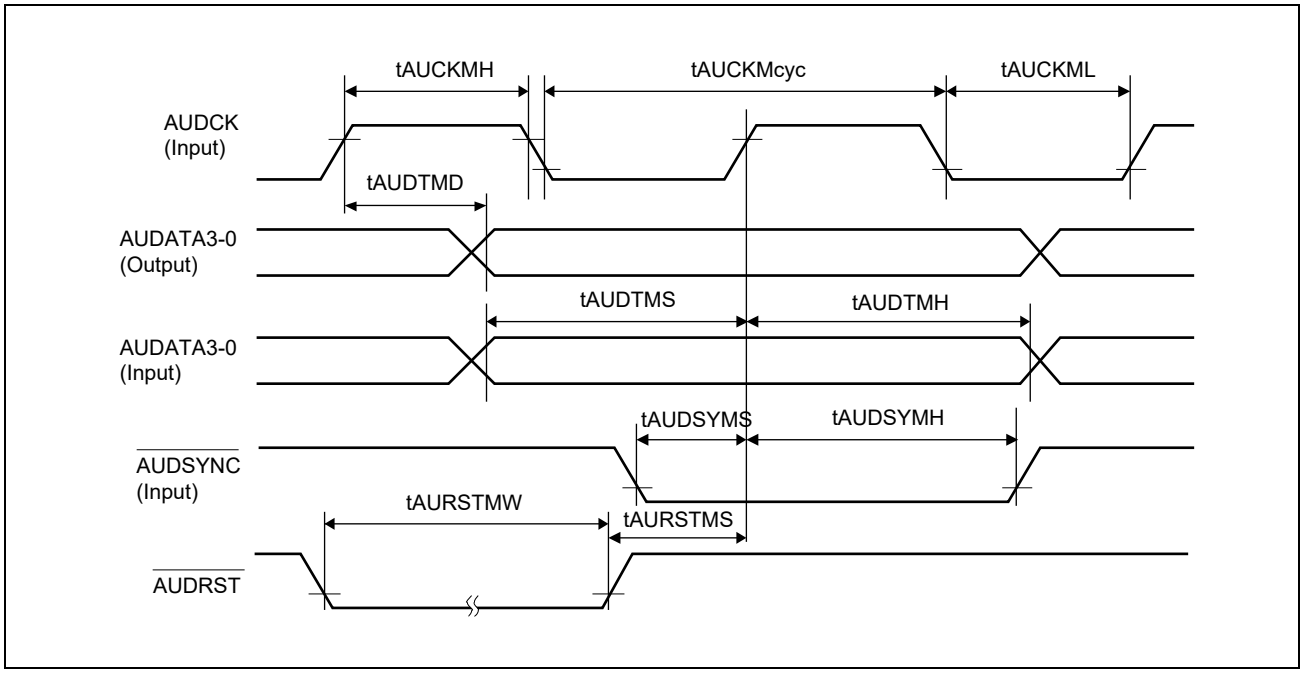


Figure 3.16 AUD RAM Monitor Timing

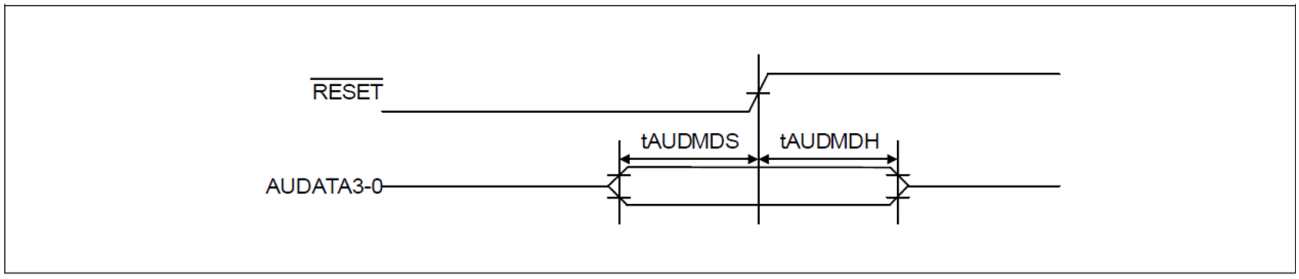


Figure 3.17 Timing to reflect settings on AUDISR

3.4 A/D Converter Characteristics

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Table 3.31 A/D Converter Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital resolution	—	—	—	12	—	bit
A/D conversion time*1	—	—	—	1	—	µs
Integral nonlinear error	—	Using T&H amplifier	—	—	±4	LSB
Offset error	—	Using T&H amplifier	—	—	±7.5	LSB
Full-scale error	—	Using T&H amplifier	—	—	±7.5	LSB
Quantization error	—	—	—	—	±0.5	LSB
Absolute error	—	—	—	—	±8.0	LSB
Self-diagnosis absolute error	—	In A/D converter self-diagnosis	—	—	±8.0	LSB
	—	In pin level self-diagnosis	—	—	±80	LSB
Analog input capacitance	—	A/D conversion standby	—	—	10	pF
	—	In sampling	—	—	20	pF
Allowable analog signal source impedance	—	—	—	—	3	kΩ
Channel T&H hold time*2	—	—	—	—	10	µs
T&H sampling time	—	—	—	—	0.45	µs
Pull-up resistance for A/D disconnection detection	—	AnVCC = 4.5V to 5.5V, ADCCnIpq = AnVSS	10	20	40	kΩ
Pull-down resistance for A/D disconnection detection	—	AnVCC = 4.5V to 5.5V, ADCCnIpq = AnVCC	10	20	40	kΩ
Input voltage range	—	Not used T&H amplifier	0	—	A0VREFH A1VREFH A2VREFH	V
	—	Using T&H amplifier	0.2	—	A0VREFH-0.2 A1VREFH-0.2 A2VREFH-0.2	V

Note 1. Conversion time for a channel, and not include T&H time.

Note 2. When the T&H circuit is in use, A/D conversion must be performed within the maximum time.

- Errors in the External Circuit of the A/D Converter

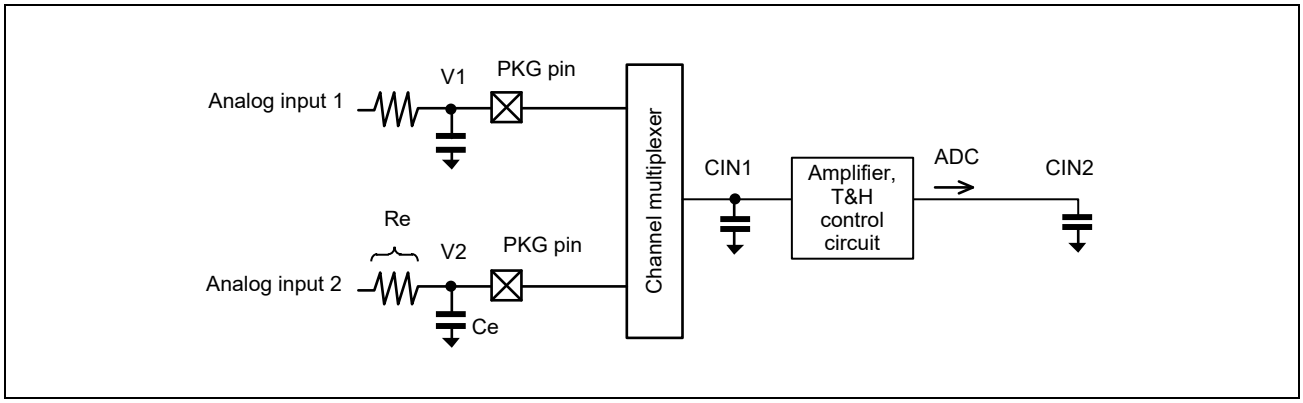
  A formula for errors in sampled values due to the external circuit of the A/D converter is given below.
  These errors will depend on the input circuit and conversion cycle. The formula given below for the errors is simplified for the calculation of sampling errors based on internal stray capacitance, amplifier offset, resistance of the signal source, and conversion cycle. This formula can also be used to calculate the effects of the signal source resistance and conversion cycle on these errors.

  The formula gives the error of analog input 2 as shown in the figure below when A/D conversion is performed in the order analog input 1 then 2.

$$Sampling\ error\ (LSB) = \left[\left(\frac{|V2 - V1| \times CIN1}{Ce + CIN1}| + \frac{|Vvfaerr| \times CIN2}{Ce + CIN2}\right) \times \frac{1}{1 - e^{-T1/(Re \times Ce)}} + \left(\frac{1}{T1} \times C1 \times V3 \times Re\right)\right] \times \frac{4096}{Vavrefh}$$

Table 3.32 Parameters of C1M-A

Item	Symbol	Reference	Unit
Common capacitance of the final stage of channel multiplexer	CIN1	1.6	pF
Common capacitance of the final stage of the amplifier and T&H control circuit	CIN2	10	pF
External capacitor on analog input pin	Ce	Depends on user board	uF
Signal source impedance	Re		kΩ
Conversion cycle of conversion pins	T1		ms
AnVREFH voltage (n = 0 to 2)	Vavrefh		V
Potential difference between V1 and V2	V2-V1	5	V
Offset voltage of amplifier and T&H control circuit	Vvfaerr	50	mV
Parasitic capacitance in channel multiplexer	C1	2	pF
|AnVCC voltage /2.5 – measured pin voltage| (n = 0 to 2)	V3	Depends on user board	V



- Values for conversion error calculated by using this formula do not include error (absolute error, etc.) specified in the A/D converter characteristics.
- This formula is a desktop formula and theoretical. When the signal source has an extremely high resistance or when the conversion cycle is too short, calculated and measured values may differ.
  Actual error depends on the capacitor, resistor, capacitance and resistance of board wiring, so please evaluate and verify the error on the user board is no greater than the value produced by this formula (Re < 1.5 MΩ and T1 ≥ 10 µs, or 1.5 MΩ ≤ Re ≤ 2 MΩ and T1 ≥ 512 µs).

3.5 R/D Converter Characteristics

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

3.5.1 RDC Conversion Performance

Table 3.33 RDC Conversion Performance (1/2)

Item	Condition		Min.	Typ.	Max.	Unit
Resolution*1			—	—	16	bit
Conversion accuracy*2	Absolute error in electrical angle signal while operation is stopped (12-bit resolution)	Angle conversion mode 0	—	—	±4	LSB
		Angle conversion mode 1	—	—	±4	
Settling time (Response for input of electric angle of 180°)	Settling range within ±8 LSB	Band 800 Hz	—	53	—	ms
		Band 1500 Hz	—	31	—	
		Band 1000 Hz	—	43	—	
		Band 500 Hz	—	85	—	
		Band 200 Hz	—	211	—	
		Automatic adjustment	—	1.9	—	
Maximum angular velocity*3 (The values in parentheses are applied to range setting as automatic adjustment)	16-bit resolution		15000 (7500)	—	—	min^{-1}
	14-bit resolution		60000 (30000)	—	—	
	13-bit resolution		120000 (60000)	—	—	
	12-bit resolution		240000 (120000)	—	—	
	11-bit resolution		480000 (240000)	—	—	
	10-bit resolution		960000 (480000)	—	—	
Maximum angular acceleration Following angular acceleration range (electrical angle)	Band 800 Hz		—	146000	—	rad/s^2
	Band 1500 Hz		—	513000	—	
	Band 1000 Hz		—	183000	—	
	Band 500 Hz		—	46000	—	
	Band 200 Hz		—	5000	—	
	Automatic adjustment		—	3000000	—	

Table 3.33 RDC Conversion Performance (2/2)

Item	Condition		Min.	Typ.	Max.	Unit
Response delay*4	Electrical angle output response delay in fixed angular velocity	Angle conversion mode 0	–0.2	—	0.20	°/10000 min^{-1}
		Angle conversion mode 1	–0.2	—	0.20	
BIST determination time*5	Obtaining the sum of squares in amplitude abnormality detection BIST (L side)		—	—	1	ms
	Obtaining the sum of squares in amplitude abnormality detection BIST (H side)		—	—	1	ms
	ADBIST		—	—	32	µs
	Angle conversion BIST (angle determination threshold is within ±16 LSB)		—	—	10	ms
	Resolver signal error detection BIST		—	—	0.5	ms
	Resolver signal cut off detection BIST		—	—	1	ms
	Conversion error BIST		—	—	10	ms
	Power short error BIST		—	—	80	µs
	Ground short error BIST		—	—	80	µs
BIST recovery time*6	All kinds of BIST		—	—	10	ms

Note 1. The resolution is changed by the setting of the maximum angular velocity select bit in the RDC3An control gain select register 1. The angle can be read with maximum 16-bit width by register access.

Note 2. It is the ability, when the waveform of analog input to RDC is ideal sign wave. RDC conversion result will defer from resolver machine angle with distortion or slippage of analog input signal or power supply voltage.

Note 3. Following angular velocity range (resolver electrical angle). It is changed by the setting of the maximum angular velocity select bit in the RDC3An control gain select register 1.

Note 4. PHI angle output from RDC is added accuracy error through analog circuit to this value. The read of PHI angle output register value with bus access needs access time. However, it does not need access time using PHI compare signal.

Note 5. It is the time to stabilize BIST determination.

Note 6. Recovery time from BIST operation to normal operation.
When the excitation frequency is under 9 kHz, BIST recovery time is maximum 15 ms.
When the conversion error determination time is set to over 10 ms, BIST recovery time is also set to over the setting value (10 ms).

3.5.2 RDC Analog Pin

Table 3.34 RDC Analog Pin Characteristics

Signal	Symbol	Item	Min.	Typ.	Max.	Unit
Signal source output*1 for resolver excitation power supply	RSO	Frequency	5	—	40	kHz
		Output voltage*2	0.38 × RVCC	0.4 × RVCC	0.42 × RVCC	VP-P
		Load impedance	10	—	—	kΩ
		Output switching*3	–40	±0	+20	%
Common voltage output for resolver excitation power supply	COM	Output voltage	0.475 × RVCC	0.5 × RVCC	0.525 × RVCC	V
		Load impedance	10	—	—	kΩ
Resolver excitation signal external input	R1E, R2E	Frequency*4, *10	5	—	40	kHz
		Input voltage range	0	—	RVCC	V
		Input voltage differential amplitude	2	—	—	VP-P
		Input impedance*11	32	40	48	kΩ
Resolver signal input	S1, S2, S3, S4	Frequency*10	5	—	40	kHz
		Input voltage range*5	—	—	—	V
		Input impedance*6	16.2	21	25.8	kΩ
		Input impedance switching*7	-40	±0	+40	%
Resolver signal monitor output	COSMNT, SINMNT	Frequency*8	5	—	40	kHz
		Output voltage*9	0.36 × RVCC	—	0.64 × RVCC	VP-P
		Load impedance	100	—	—	kΩ

Note 1. Pseudo sign wave output, 7-bit D/A output.

Note 2. The center of amplitude is COM voltage. Described values are default (±0%) of output adjustment.

Note 3. The output voltage can be adjusted in four steps of -40, -20, ±0, and +20% by adjust function.

Note 4. When the excitation frequency is over 22 kHz with resolver excitation signal external input (RDC3AnREF.EXIO = 0_B), set RDC3AnDIAG1.CVEDS = 1_B, and do not set using RD conversion error detection circuit (for high-speed rotation).

Note 5. Depends on external circuit.
Input voltage must be adjusted for COSMNT, SINMNT = 0.36 × RVCC to 0.64 × RVCC (VP-P).

Note 6. Input impedance with on-chip feed-back resistor. This is the default value (±0%).

Note 7. Can be adjusted from -40 to +40% in step of 10% by adjust function.

Note 8. Same as the frequency of resolver signal input.

Note 9. Must be adjusted within this range to keep angle conversion resolution.

Note 10. The phase error of the excitation component of the resolver excitation signal external input and the resolver signal input must be within 45º.

Note 11. When RDC3AnREF.EXIO = 0_B (i.e. the external excitation signal input is set), this impedance pulls the RSO (R1E) and COM (R2E) pins down to RVSS.

3.5.3 Error Detect Characteristics

Table 3.35 Error Detect Characteristics

Error Detect Item		Set Threshold (Default Setting)	Detect Time
Resolver signal error monitor output amplitude voltage*1	Set register RDC3AnDIAG0.EXCETH[7:0]	0.102 × (RVCC±5%) [Vp-p]	220 [µs] (typ.), 2 [ms] (max.)
Breaking of resolver signal (Direct current bias supply method) VSINMNT-VCOM or VCOSMNT-VCOM*2	The register used for setting threshold when DC resolver is selected RDC3AnDIAG0.SGBDTH[7:0]	COM + 0.35 × (RVCC±5%) [VDC]	10 [ms] (max.)
	The register used for setting threshold when VR resolver is selected RDC3AnDIAG0.SGBTH[7:0]	COM + 0.08 × (RVCC±5%) [VDC]	
R/D conversion error (over control declination) Recognition level for internal control declination (ε)*3	High side	$00CA8_H$	*4
	Low side	$7F358_H$	
Resolver signal power short error	Pins S1, S2, S3, and S4	0.9 × (RVCC±5%) [VDC]	0.08 [ms] (max.)
	Pins RSO and COM	0.8 × (RVCC±5%) [VDC]	
Resolver signal ground short error	Pins S1, S2, S3, and S4	0.1 × (RVCC±5%) [VDC]	0.08 [ms] (max.)
	Pins RSO and COM	0.2 × (RVCC±5%) [VDC]	
Sum square amplitude error Integral value of sum square of monitor output amplitude voltage (sin, cos) with an interval within the excitation period	High side	0.8 × (RVCC±5%) [Vp-p]	*5
	Low side	0.2 × (RVCC±5%) [Vp-p]	

Note 1. Determined as an error, when both of SINMNT and COSMNT become under threshold.

Note 2. Determined as an error, when DC level changed over threshold.

Note 3. Determined as over, when control declination becomes over high side threshold, or under low side threshold.

Note 4. Determined as an error, when control declination recognition rate becomes over 50% as average of period set by the EDPS [1:0] bits in the RDC3AnDIAG1 register (default is about 7.4 ms). It might not be detected, when the error continuous period is shorter than detect period.

Note 5. Dependent on the excitation frequency and amplitude error excitation period count settings.

3.6 Code Flash Characteristics

Table 3.36 Code Flash Basic Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Number of programming times*1	CWRT	Retained for 20 years *2	1000	—	—	Times
Programming temperature	TPRG	Tj	–40	—	+150	ºC
Reading temperature	TREAD	Tj	–40	—	+150	ºC

Note 1. The number of programming times is the number of erasure of each block. If the number of programming times is n (n = 1000), each block can be erased n times. For example, if 256-byte data is written 128 times to different addresses of a 32KB block and then the block is erased, the number of programming times is counted as 1. Note, however, that writing data to the same address multiple times for one erasure is not allowed (overwrite is prohibited).

Note 2. This is the case when the average Ta = 85°C. This retained period is from when the erasure of the code flash memory has been normally completed.

Table 3.37 Code Flash Programming Characteristics

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item	Condition	Block size	Min.	Typ.	Max.	Unit
Programming time	Number of programming times < 100	256 B	—	0.4*1	6*1	ms
		32 KB	—	80	360	ms
	Number of programming times ≥ 100	256 B	—	0.5*1	7.2*1	ms
		32 KB	—	96	432	ms
Erasing time*1	Number of programming times < 100	8 KB	—	39	120	ms
		32 KB		141	480	ms
	Number of programming times ≥ 100	8 KB	—	47	144	ms
		32 KB	—	169	576	ms

Note 1. Only the hardware processing time is included. Software overhead is not included.

3.7 Data Flash Characteristics

Table 3.38 Data Flash Basic Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Number of programming times*1	CWRT	Retained for 20 years*2	125000	—	—	Times
		Retained for 3 years*2	250000	—	—	Times
Programming temperature	TPRG	Tj	–40	—	+150	ºC
Reading temperature	TREAD	Tj	–40	—	+150	ºC

Note 1. The number of programming times is the number of erasure of each block. If the number of programming times is n (n = 125000), each block can be erased n times. For example, if 4 byte data is written 16 times to different addresses of a 64KB block and then the bock is erased, the number of programming times is counted as 1. Note, however, that writing data to the same address multiple times for one erasure is not allowed (overwrite is prohibited).

Note 2. This is the case when the average Ta = 85°C. This retained period is from when the erasure of the data flash memory has been normally completed.

Table 3.39 Data Flash Programming Characteristics

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V
VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V
Tj = –40ºC to 150ºC

Item	Block size	Min.	Typ.	Max.	Unit
Programming time*1	4 B	—	0.16	1.7	ms
Erasing time*1	64 B	—	1.7	10	ms
Blank checking time*1	4 B	—	—	30	µs
	64 B	—	—	100	µs

Note 1. Only the hardware processing time is included. Software overhead is not included.

3.8 Thermal Characteristics

3.8.1 Parameters

Table 3.40 Thermal Resistance of RH850/C1M-A

Package	Parameter	Estimate	Unit	Note
FPBGA1717-252	θja	20.6	ºC/ W	JESD51-9 compliant (4 layers)
	Ψjb	14.0	ºC/ W	JESD51-9 compliant (4 layers)
	Tb_inc	6.7	ºC/ W	JESD51-9 compliant (4 layers)
	Ψjt	0.22	ºC/ W	JESD51-9 compliant (4 layers)
LQFP2424-176	θja	30.0	ºC/ W	JESD51-7 compliant (4 layers)
	Ψjb	22.8	ºC/ W	JESD51-7 compliant (4 layers)
	Tb_inc	7.3	ºC/ W	JESD51-7 compliant (4 layers)
	Ψjt	0.34	ºC/ W	JESD51-7 compliant (4 layers)

Note: Thermal resistance and thermal characteristics parameters will change according to the usage environment.

3.8.2 Assumed Board

Table 3.41 JESD51-9 Compliant (4 layers)

	Board Size (mm)		
Package	X	Y	Area (mm^2)
L board	101.6	114.3	11612.88
Remaining copper rates		Thickness of conductors	
50-95-95-50%		70-35-35-70 µm	

Table 3.42 JESD51-7 Compliant (4 layers)

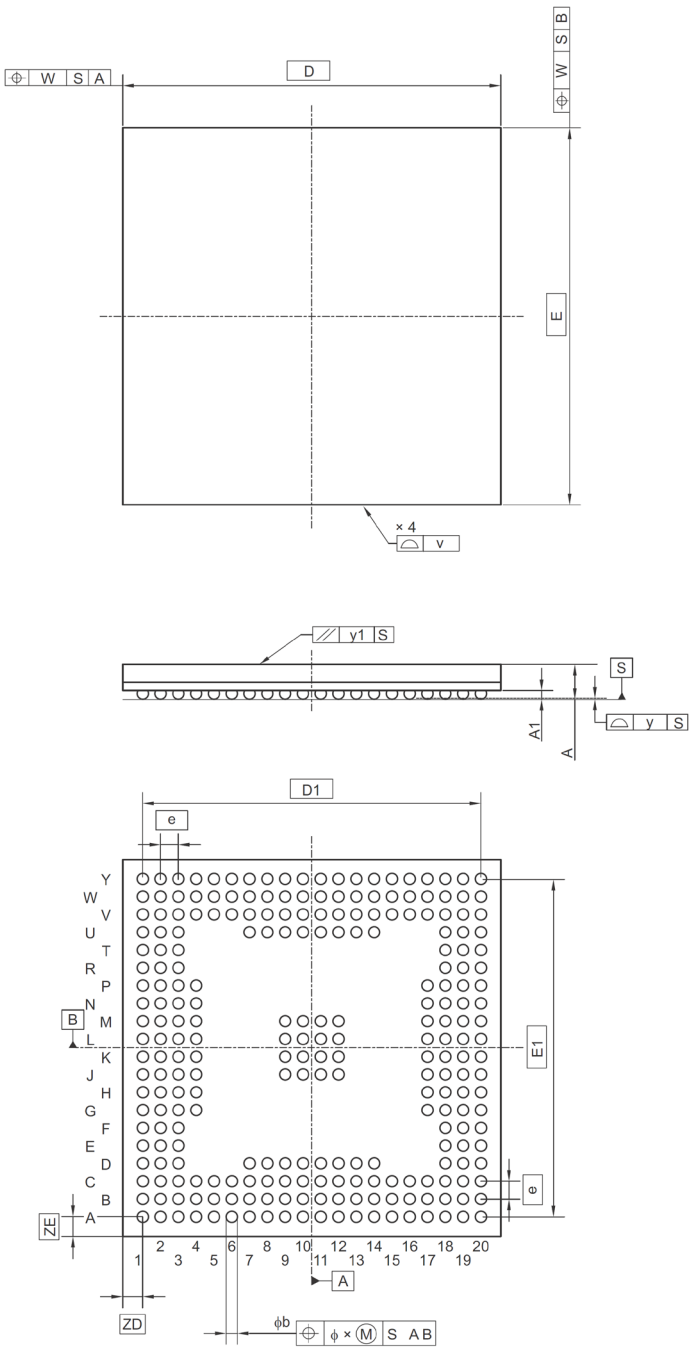
	Board Size (mm)		
Package	X	Y	Area (mm^2)
L board	76.2	114.3	8709.66
Remaining copper rates		Thickness of conductors	
50-95-95-50%		70-35-35-70 µm	

Appendix A Package Dimensions

- BGA252

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-FBGA252-17x17-0.80	PRBG0252GB-A	—	0.90

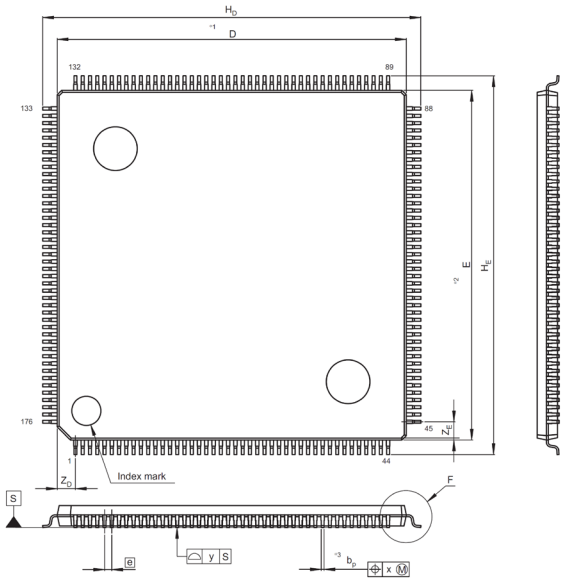
Unit: mm

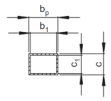


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	17.00	—
D1	—	15.20	—
E	—	17.00	—
E1	—	15.20	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	2.00
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	0.90	—
ZE	—	0.90	—

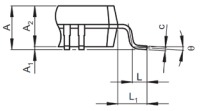
- QFP176

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025.03.31	-	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/