

READ4656J

High Drivability & High Slew Rate, Output Full Range

High Voltage, Low Power Consumption

CMOS Quad Operational Amplifier

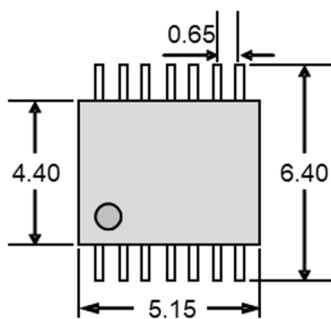
Description

The READ4656J is quad CMOS Operational Amplifier with AEC-Q100 compliant, which is the features the same performance as the Bipolar products (UPC844) about the voltage resistance (power supply voltage: 36V Max.) and high slew rate (8V/μs Typ.). This IC is the output full-range product with greatly reduced power consumption and input bias current compared to bipolar products.

Features

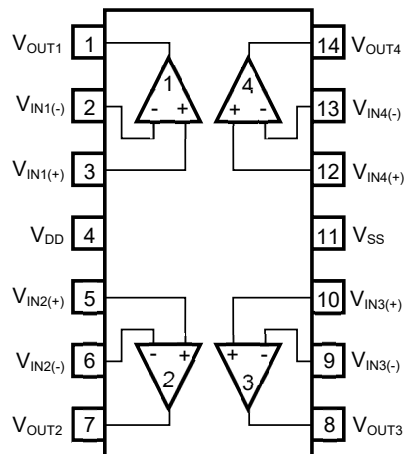
- AEC-Q100 Compliant
 - Output full range (Rail-to-Rail output)
 - Absolute Maximum Ratings
 - Power Supply Voltage $V_{DD} = -0.1$ to $+36V$
 - Operating Ambient Temperature Range $T_A = -40$ to $+125\text{ }^{\circ}C$
 - Electrical Characteristics
 - Power Supply Voltage $V_{DD} = +4.5V$ to $+32V$
 - Input Offset Voltage $V_{IO} \leq \pm 9mV$
 - Input Bias Current $I_B \leq (1pA)$
 - Supply current (per channel) $I_{DD} = 0.7\text{ mA Typ.}, 1.0\text{ mA Max.}$
(@ $V_{DD}=5.0V$ $T_A=-40^{\circ}C$ to $+125^{\circ}C$)
 - Slew Rate $SR = 8\text{ V}/\mu s$ Typ.
- () reference value of design

Product Line-up

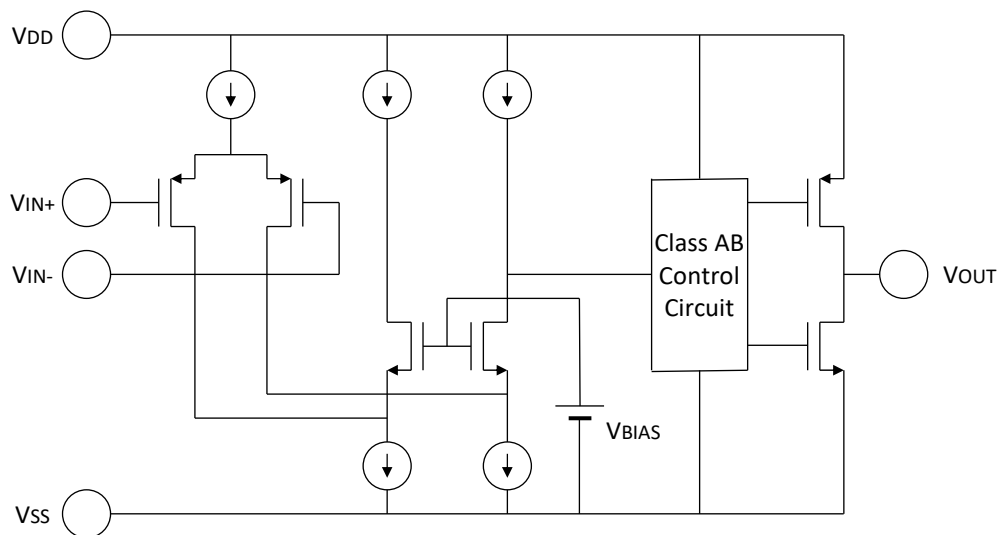
Package	TSSOP
Product Name ⁽¹⁾	READ4656JSP#GC1 READ4656JSP#HC1
Quality Level	High Quality Level
Outline	Unit : mm 

(1). The taping direction is different for GC and HC.
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

<T_A=-40 to +125 °C >

Items	Symbol	Ratings	Unit
Supply voltage Note.1	V _{DD}	-0.1 to +36	V
Differential input voltage	V _{ID}	±2	V
Input voltage Note.2	V _I	V _{SS} -0.1 to V _{DD} +0.1	V
Maximum output current	I _O	20	mA
Power dissipation Note.3	P _T	550	mW
Junction temperature	T _J	-40 to +150	°C
Operating temp. range	T _A	-40 to +125	°C
Storage temp. range	T _{stg}	-55 to +150	°C

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of V_{SS} (GND)-0.1V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm x 100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern).

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

READ4656JSP: Derate at -7.0 mW/°C when T_A > 71 °C

(Junction – ambient thermal resistance R_{th(J-A)} = 144 °C/W)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (V _{SS} = GND)	V _{DD}	+4.5		+32	V
Power Supply Voltage (Dual Supply)	V _{DD} – V _{SS}	±2.25		±16	V

Electrical Characteristics

< $T_A=25^{\circ}\text{C}$, $V_{DD}=5.0\text{V}$, $V_{SS}=\text{GND}$ >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V_{IO}		± 3	± 9	mV	
Input offset current	I_{IO}			(± 1)	pA	
Input bias current	I_B			(± 1)	pA	
Output high voltage	V_{OH}	$V_{DD}-0.3$			V	$I_L = 10\text{mA}$
Output low voltage	V_{OL}			$V_{SS}+0.3$	V	$I_L = 10\text{mA}$
Voltage gain	A_V	60	90		dB	$R_L \geq 100\text{k}\Omega$
Channel supply current	I_{DD}/ch		0.7	1.0	mA	$R_L = \infty$, $I_O = 0$
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		$V_{DD}-2$	V	
Gain bandwidth product	GBW		6		MHz	$C_L = 20\text{pF}$
Slew rate	SR		8		V/ μs	$C_L = 20\text{pF}$
Channel Separation			80		dB	$f = 20\text{ Hz to } 20\text{ kHz}$

< $T_A=25^{\circ}\text{C}$, $V_{DD,SS}=\pm 15\text{ V}$ >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V_{IO}		± 3	± 12	mV	
Input offset current	I_{IO}			(± 1)	pA	
Input bias current	I_B			(± 1)	pA	
Output high voltage	V_{OH}	$V_{DD}-0.3$			V	$I_L = 10\text{mA}$
Output low voltage	V_{OL}			$V_{SS}+0.3$	V	$I_L = 10\text{mA}$
Voltage gain	A_V	60	90		dB	$R_L \geq 100\text{k}\Omega$
Channel supply current	I_{DD}/ch		0.7	1.0	mA	$R_L = \infty$, $I_O = 0$
Common mode rejection ratio	CMRR	55	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		$V_{DD}-2$	V	
Gain bandwidth product	GBW		6		MHz	$C_L = 20\text{pF}$
Slew rate	SR		8		V/ μs	$C_L = 20\text{pF}$
Channel Separation			80		dB	$f = 20\text{ Hz to } 20\text{ kHz}$

< $T_A = -40$ to $+125^{\circ}\text{C}$, $V_{DD}=5.0\text{V}$, $V_{SS}=\text{GND}$ >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V_{IO}		± 3	± 9	mV	
Input offset current	I_{IO}		± 3	± 20	nA	
Input bias current	I_B		± 3	± 20	nA	
Output high voltage	V_{OH}	$V_{DD}-0.45$			V	$I_L = 10 \text{ mA}$
Output low voltage	V_{OL}			$V_{SS}+0.45$	V	$I_L = 10 \text{ mA}$
Voltage gain	A_V	60	90		dB	$R_L \geq 100\text{k}\Omega$
Channel supply current	I_{DD}/ch		0.7	1.0	mA	$R_L = \infty$, $I_O = 0$
Common mode rejection ratio	CMRR	50	80		dB	
Supply voltage rejection ratio	SVRR	50	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		$V_{DD}-2$	V	
Gain bandwidth product	GBW		6		MHz	$C_L = 20\text{pF}$
Slew rate	SR		8		V/ μs	$C_L = 20\text{pF}$
Channel Separation			80		dB	$f = 20 \text{ Hz to } 20 \text{ kHz}$

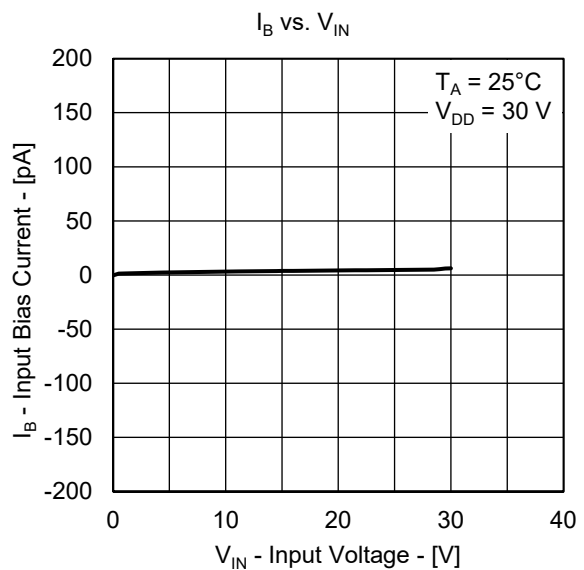
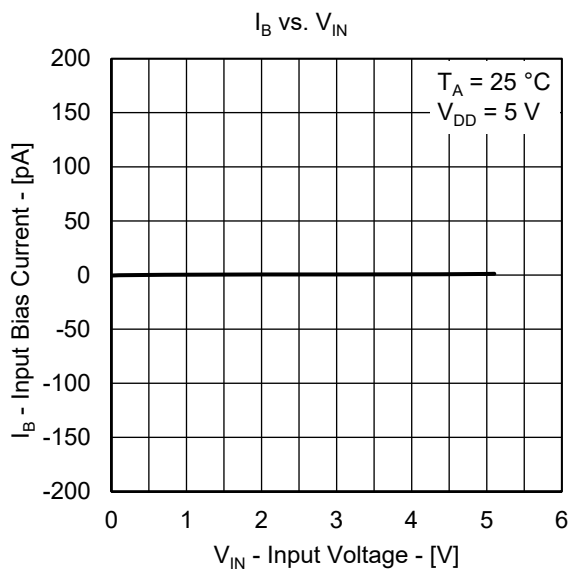
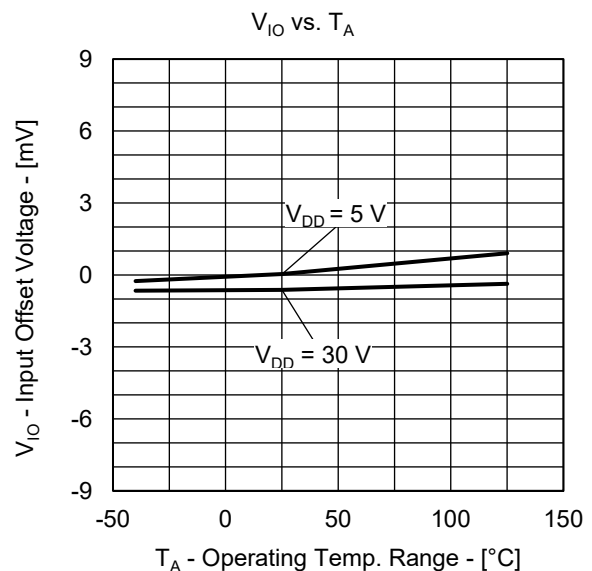
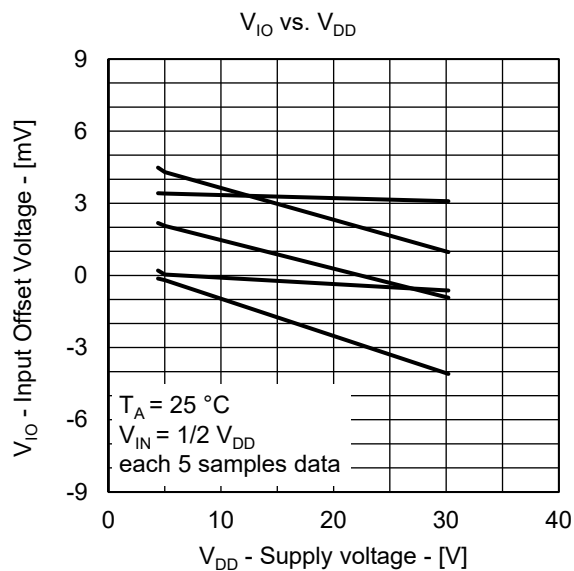
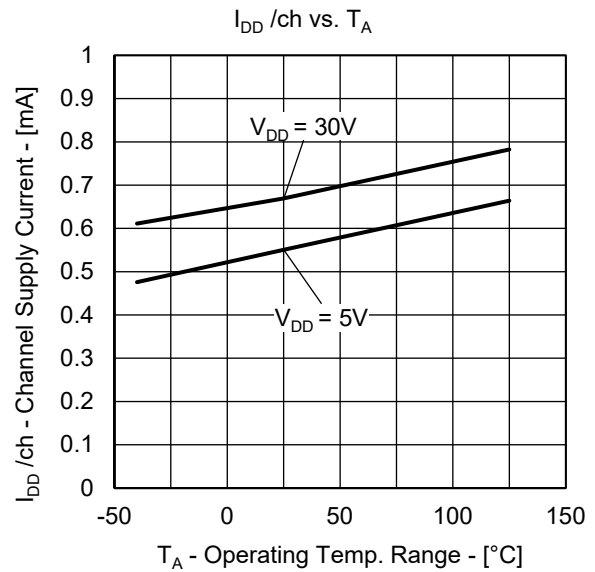
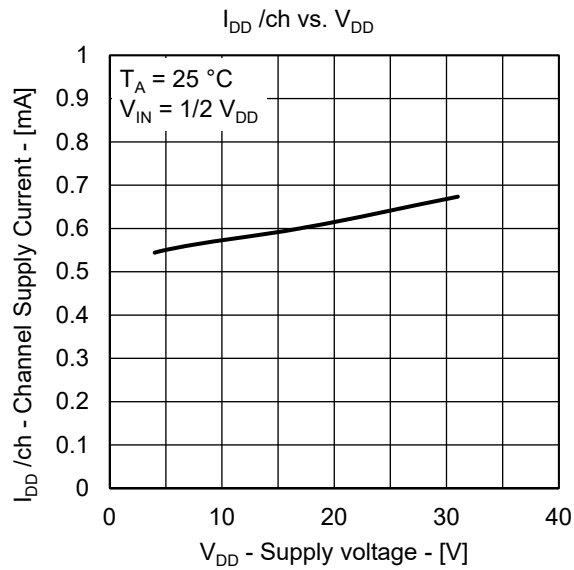
() reference value of design

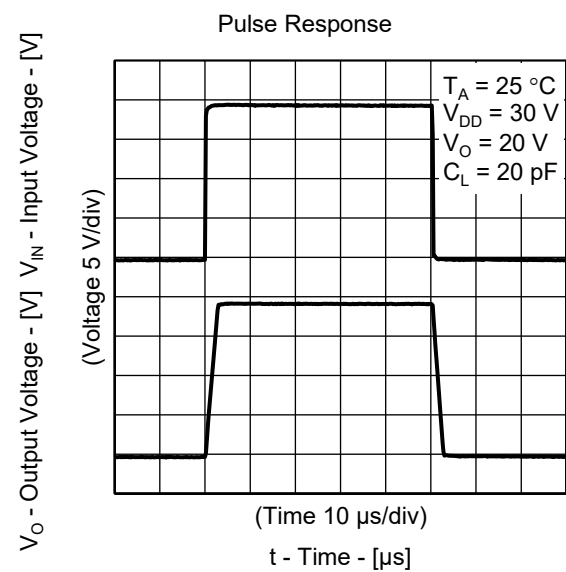
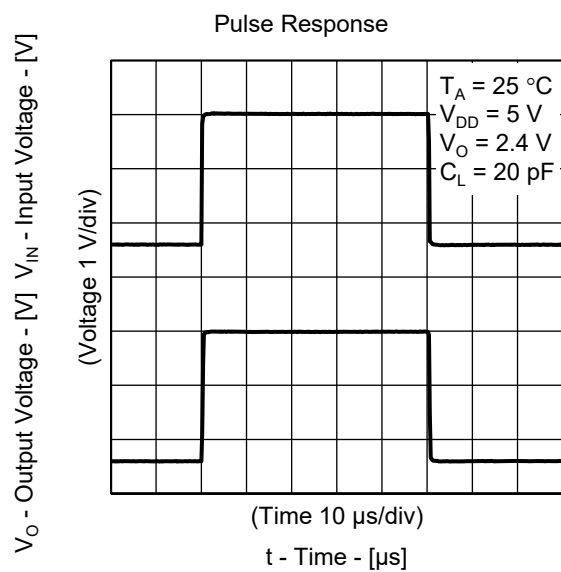
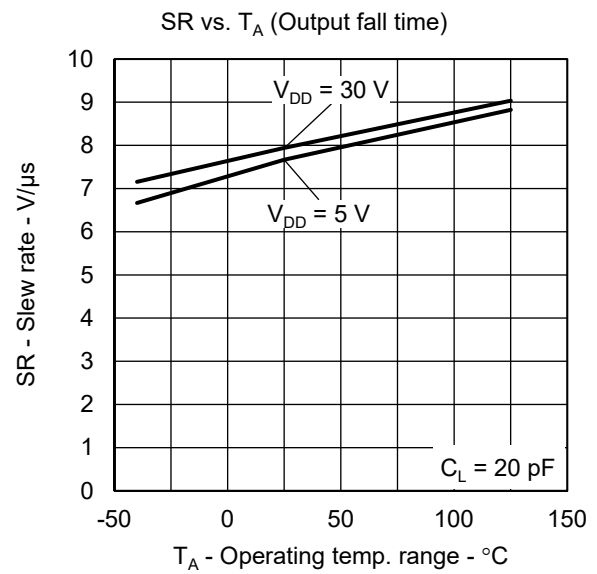
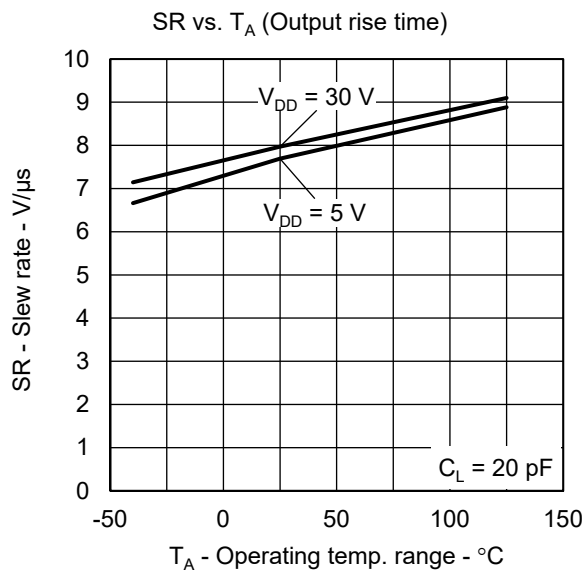
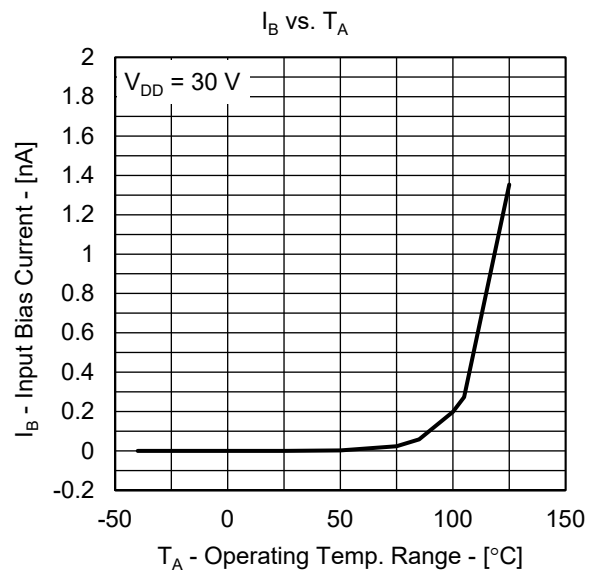
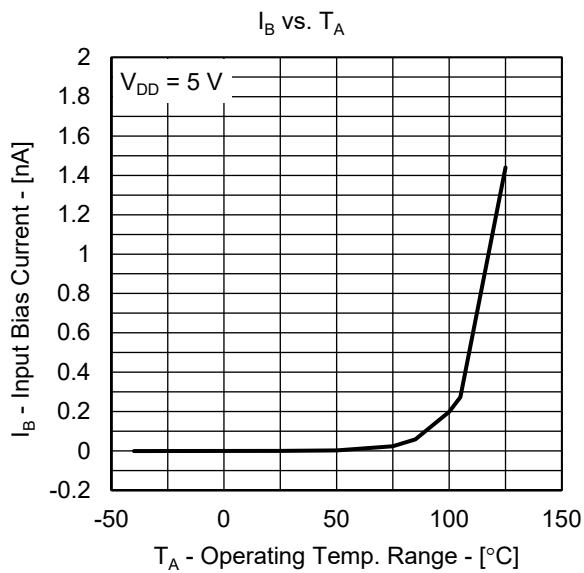
Notes

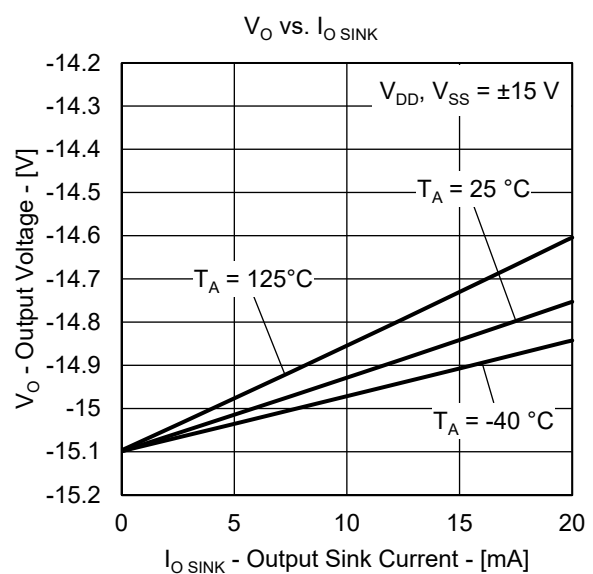
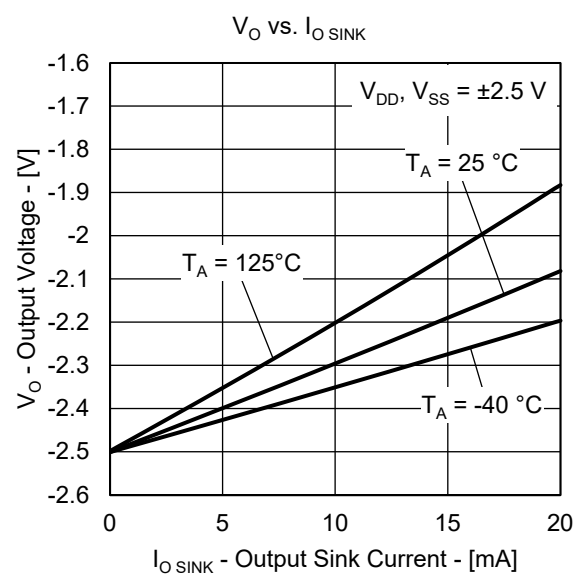
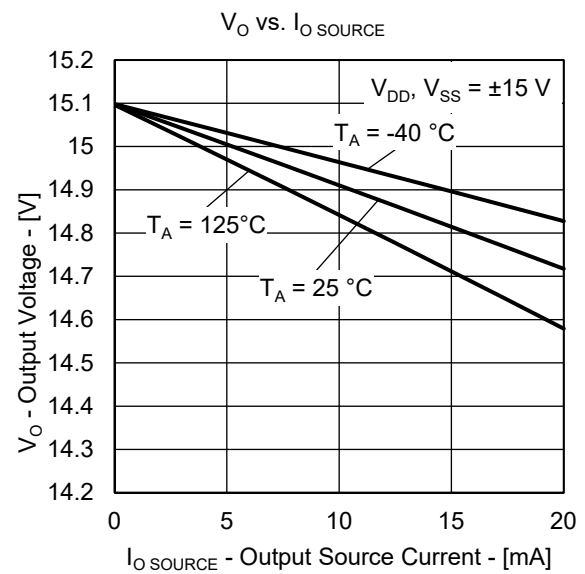
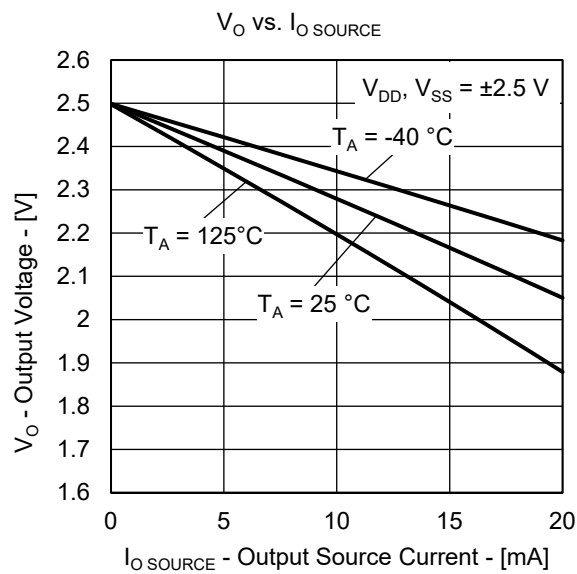
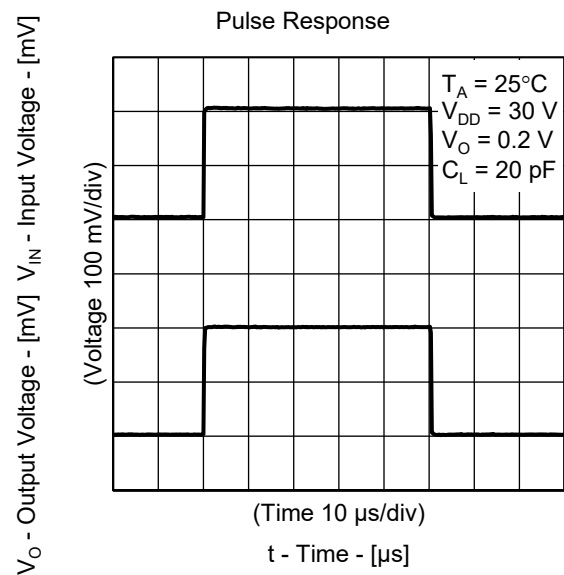
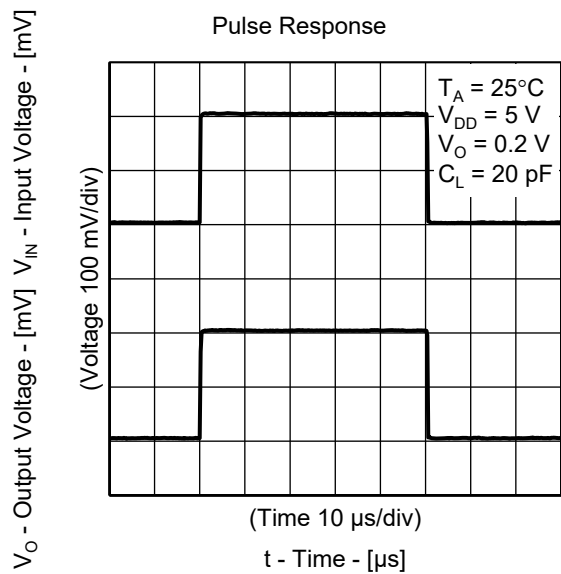
Output terminal: The over-current protection feature is not built in the output terminal of this product. Therefore, if the output is short circuit (from output to V_{DD} or from output to V_{SS}) or the forward clamp circuit using the diode at the output pin, the excessive output current may flow. Please insert the series resistor in the output pin to limit the current.

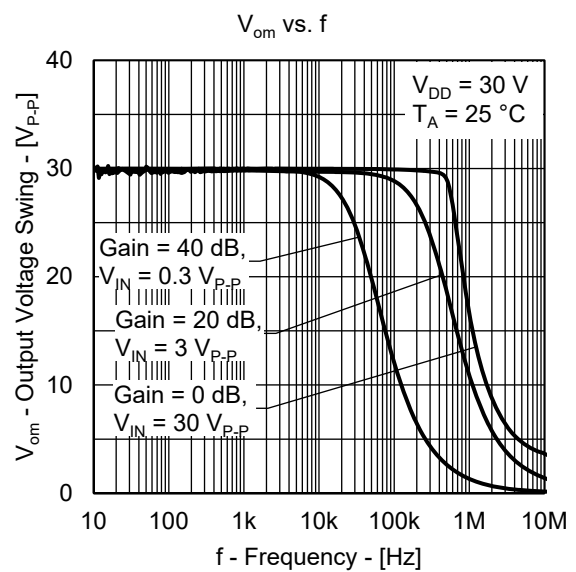
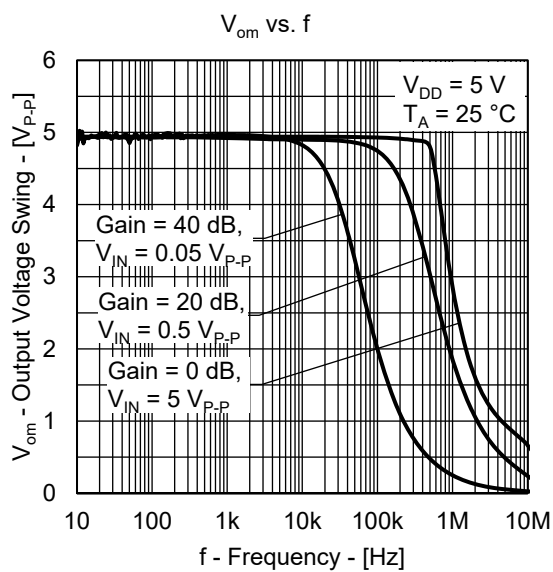
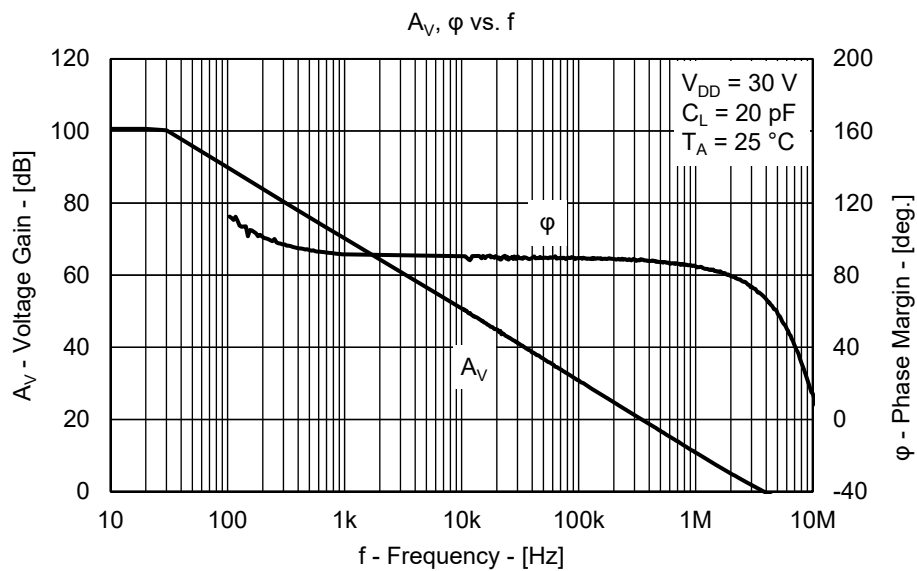
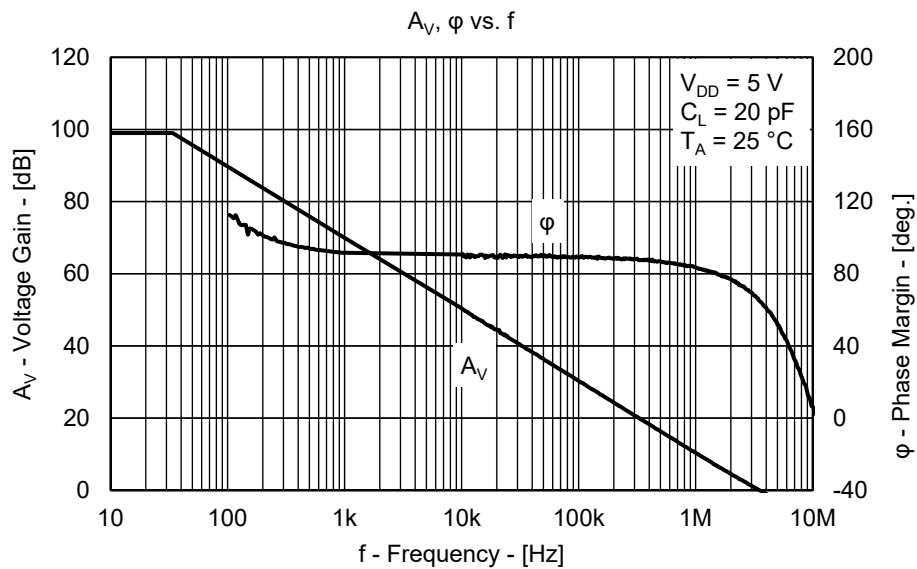
Application circuit: Please keep V_{ID} within $\pm 2\text{V}$ during stationary operation and design the closed-loop operation composed feedback system: Voltage Follower, Inverting Amplifier and Non-inverting Amplifier.

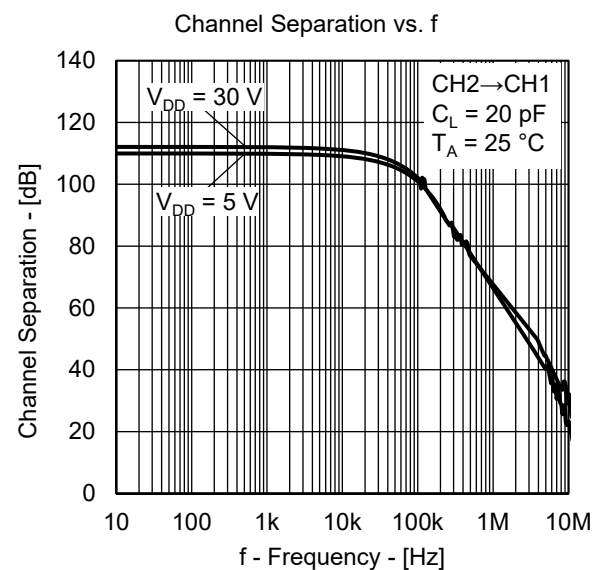
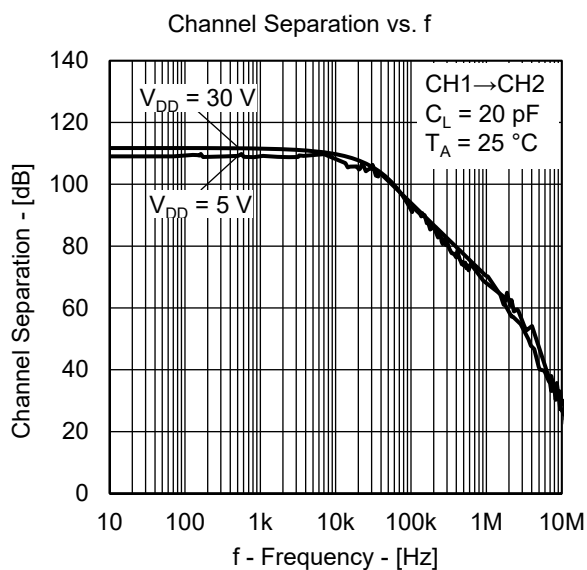
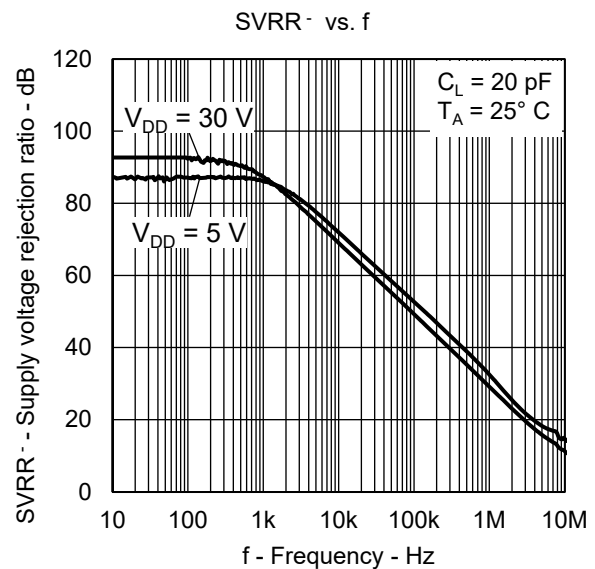
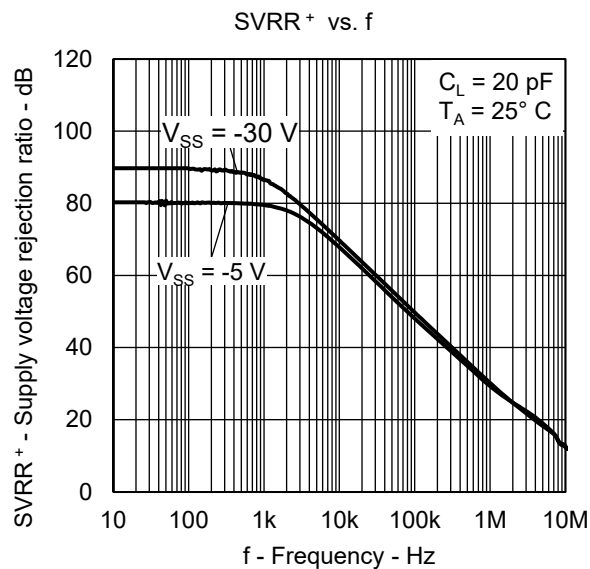
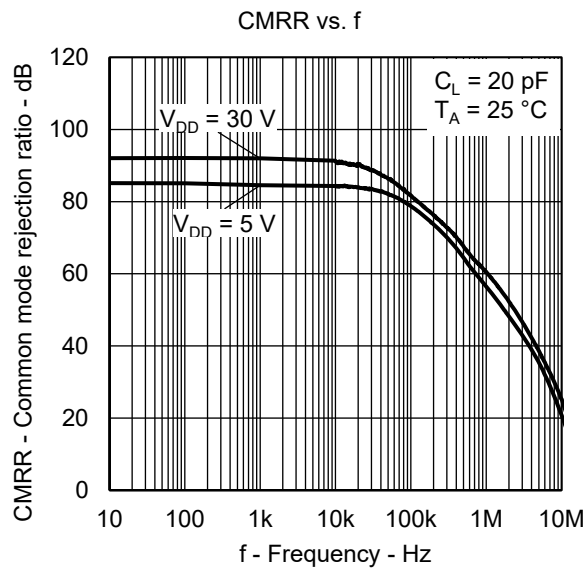
Characteristics Curve ($T_A = 25\text{ }^{\circ}\text{C}$) (Reference Value)

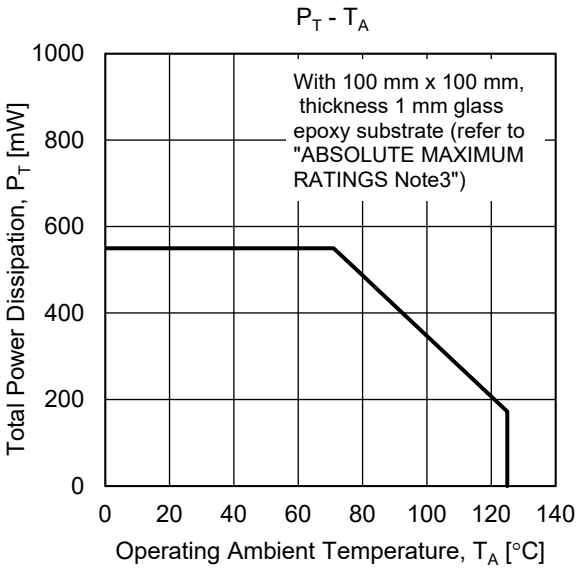










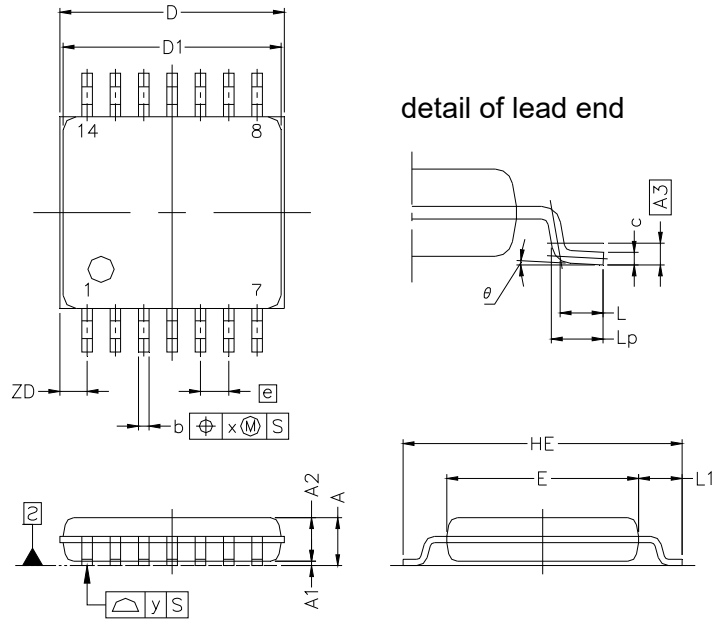


Package Dimensions

14-PIN PLASTIC TSSOP

JEITA Package Code	RENESAS Code	Previous Code	MASS(TYP.)[g]
P-TSSOP14-0225-0.65	PTSP0014JB-A	P14GR-65-9LG-1	—

Unit:mm



NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	5.15 ±0.15
D1	5.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} _{-0.05}
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.625

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(Rev.5.0-1 October 2020)

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