

# REAC842J

Low Input Offset Voltage  $V_{IO} \leq 1\text{mV} (@ -40^\circ\text{C to } +125^\circ\text{C})$

Single Power Supply, High Speed, Wide Band,

Dual Bipolar Operational Amplifier

## DESCRIPTION

The REAC842J is a single power and dual operational amplifiers which has features low input offset voltage  $V_{IO} \leq \pm 1\text{mV}$  and low input offset voltage temperature drift in  $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ .

A high speed PNP transistor is used in the circuit which improves the characteristics such as slew rate, gain-bandwidth product, stabilization of the withstand load capacitance, with no crossover distortion compared to REAC1251.

As this is a high slew rate product, it is able to provide high-speed signal amplification and can be applied to a wide range of sensor applications such as motors. Moreover, due to its small package (MSOP), mounting on the vicinity of the sensor becomes possible, which makes the board smaller and increases design freedom.

## FEATURES

AEC-Q100 Compliant

Absolute Maximum Ratings

- Power Supply Voltage -0.1 to +36 V
- Operating Ambient Temperature Range -40 °C to +125 °C

Electrical Characteristics

- Power Supply Voltage +3 V to +32 V (MIN. MAX.)
- Input Offset Voltage ( $T_A @ -40^\circ\text{C to } +125^\circ\text{C}$ )  $\pm 1\text{ mV (MAX.)}$
- Input Offset Voltage Temperature Drift  $\pm 1\ \mu\text{V}/^\circ\text{C (TYP.)}$
- Gain Bandwidth Product ( $f = 100\text{ kHz}$ ) 4 MHz (TYP.)
- Slew Rate ( $V^\pm = \pm 15\text{ V}$ ) 7 V/ $\mu\text{s (TYP.)}$
- Stability to capacitive load (Capacitive load, 1000 pF)
- Build-in phase correction circuit.
- Built-in output short-circuit protection circuit.

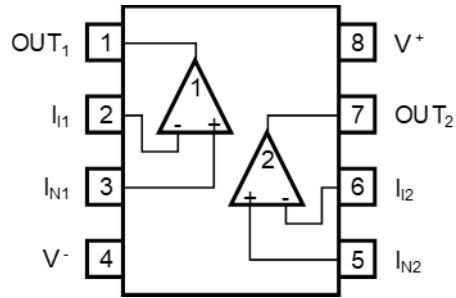
The package line-up is MSOP

## PRODUCT LINEUP

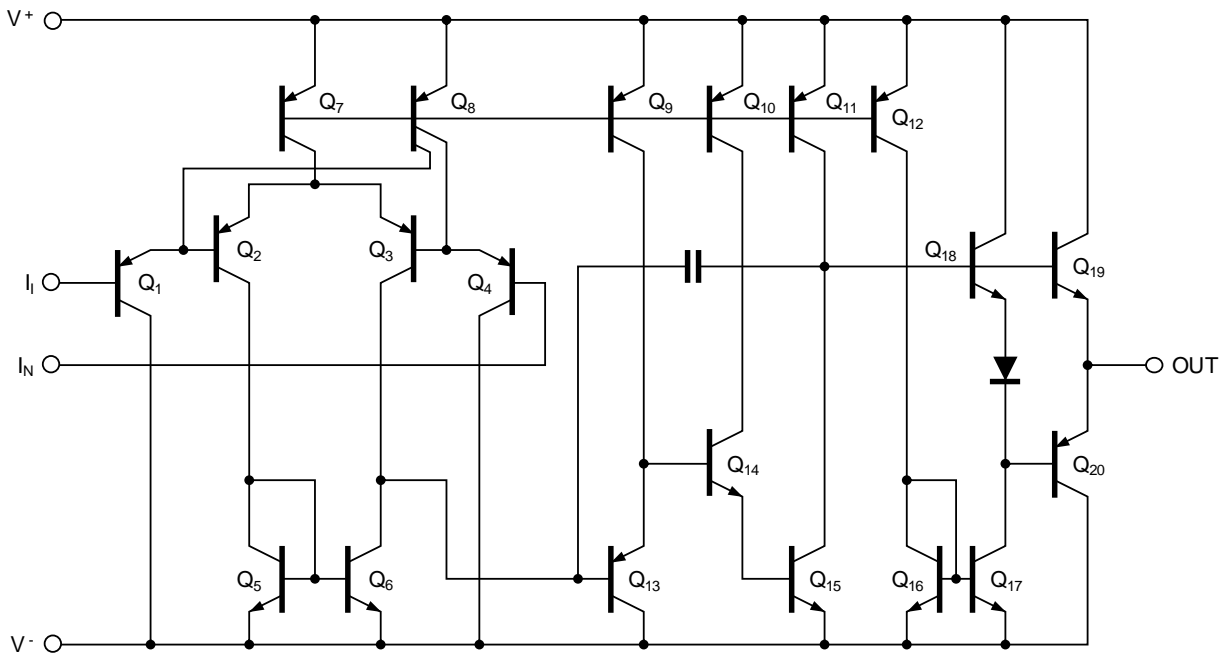
Package	SOP	MSOP
Product Name <sup>(1)</sup>	REAC842JSM#GCB REAC842JSM#HCB	REAC842JSN#GC1 REAC842JSN#HC1
Quality Level	High Quality Level	
Outline	<p style="text-align: right;">Unit : mm</p>	<p style="text-align: right;">Unit : mm</p>

(1) The taping directions are different between GC and HC. Please refer to the delivery specifications in detail.

**PIN CONFIGURATION (Marking Side)**



**EQUIVALENT CIRCUIT (1/2 CIRCUIT)**



**ABSOLUTE MAXIMUM RATINGS**(T<sub>A</sub> = -40 to +125 °C)

Parameter	Symbol	REAC842JSM	REAC842JSN	Unit
Power Supply Voltage <sup>Note 1</sup>	V <sup>+</sup> - V <sup>-</sup>	-0.1 to +36		V
Differential Input Voltage	V <sub>ID</sub>	±36		V
Input Voltage <sup>Note 2</sup>	V <sub>I</sub>	V <sup>-</sup> -0.1 to V <sup>-</sup> +36		V
Output Applied Voltage <sup>Note 3</sup>	V <sub>O</sub>	V <sup>-</sup> -0.1 to V <sup>+</sup> +0.1		V
Total Power Dissipation <sup>Note 4</sup>	P <sub>T</sub>	440		mW
Output Short Circuit Duration <sup>Note 5</sup>	t <sub>s</sub>	Indefinite		s
Operating Ambient Temperature	T <sub>A</sub>	-40 to +125		°C
Operating Junction Temperature	T <sub>J</sub>	-40 to +150		°C
Storage Temperature	T <sub>stg</sub>	-55 to +150		°C

- Notes:
- Note that reverse connections of the power supply may damage the ICs.
  - The allowable input voltage range without damaging or destructing the device. Independent to power supply voltage range.  
Do not apply voltage equivalent to V<sup>-</sup> (GND) -0.1 V or less.  
The input voltage for normal operation as operational amplifier is within the Common Mode Input Voltage Range of electrical characteristics.
  - The input voltage range that can be applied to the output pin externally without deteriorating or damaging the device characteristic.  
Note that the rating should not be exceeded including transient state such as power supply ON/OFF, etc.  
The output voltage that can be obtained as operational amplifier is within the Output Voltage Swing of electrical characteristics.
  - This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.  
Note that restrictions will be made to the following conditions for each product, and the de-rating ratio depending on the operating ambient temperature.  
REAC842JSM : Temperature condition is 50 °C or less. De-rate 4.4 mW/°C when T<sub>A</sub> > 50 °C.  
Junction - ambient thermal resistance R<sub>th(j-a)</sub> = 227 °C/W  
REAC842JSN : Temperature condition is 58 °C or less. De-rate 4.8 mW/°C when T<sub>A</sub> > 58 °C.  
Junction - ambient thermal resistance R<sub>th(j-a)</sub> = 208 °C/W
  - Please use below the Total Power Dissipation and the de-rating of Note 4.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	MIN.	MAX.	Unit
Power Supply Voltage (V <sup>-</sup> = GND)	V <sup>+</sup>	+3	+32	V
Power Supply Voltage (Dual Supply)	V <sup>±</sup>	±1.5	±16	V
Output Current	I <sub>o</sub>		±10	mA
Capacitive Load (A <sub>v</sub> = +1)	C <sub>L</sub>		1000 <sup>Note 6</sup>	pF

- Notes:
- This is the value when feedback resistor (R<sub>f</sub>) = 0.

## ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25 °C, V<sup>±</sup> = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V <sub>IO</sub>		±0.3	±1	mV	V <sub>IN</sub> = 1/2 V <sub>CC</sub> , R <sub>S</sub> ≤ 50 Ω
Input Offset Current	I <sub>IO</sub>		±6	±75	nA	
Input Bias Current <sup>Note 7</sup>	I <sub>B</sub>		75	200	nA	
Large Signal Voltage Gain	A <sub>V</sub>	25,000	1,000,000			R <sub>L</sub> ≥ 2 kΩ, V <sub>O</sub> = ±10 V
Circuit Current <sup>Note 8</sup>	I <sub>CC</sub>		4.3	6	mA	I <sub>O</sub> = 0 A
Common Mode Rejection Ratio	CMR	70	100		dB	
Supply Voltage Rejection Ratio	SVR	70	110		dB	
Output Voltage (High)	V <sub>OH1</sub>	13.7	-	-	V	R <sub>L</sub> = 10 kΩ
	V <sub>OH2</sub>	13.5	-	-	V	R <sub>L</sub> = 2 kΩ
Output Voltage (Low)	V <sub>OL1</sub>	-	-	-13.7	V	R <sub>L</sub> = 10 kΩ
	V <sub>OL2</sub>	-	-	-13.5	V	R <sub>L</sub> = 2 kΩ
Common Mode Input Voltage Range	V <sub>ICM</sub>	V <sup>-</sup>		V <sup>+</sup> -1.8	V	
Slew Rate	SR		7		V/μs	A <sub>V</sub> = +1 (Rise Edge)
Gain Bandwidth Product	GBW		4		MHz	f = 100 kHz
Channel Separation			120		dB	f = 20 Hz to 20 kHz

(T<sub>A</sub> = 25 °C, V<sup>+</sup> = +5 V, V<sup>-</sup> = GND)

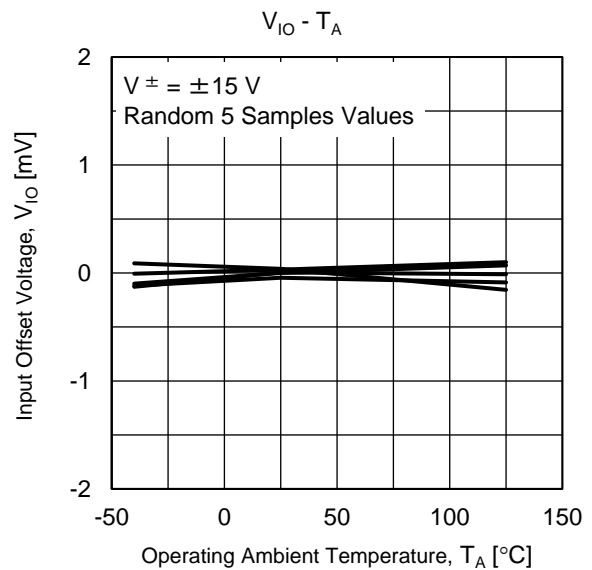
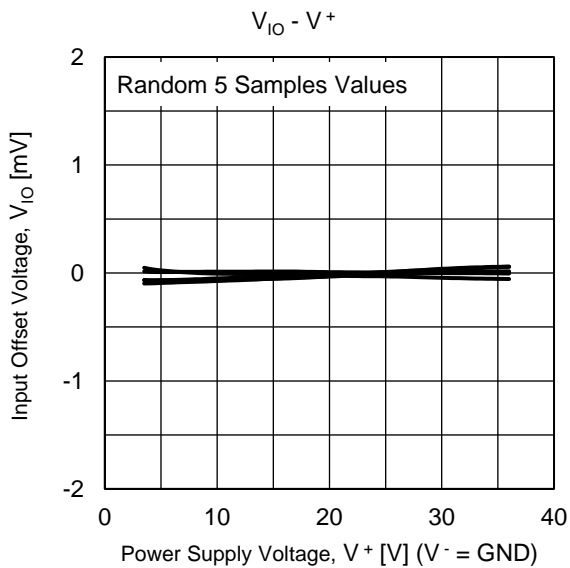
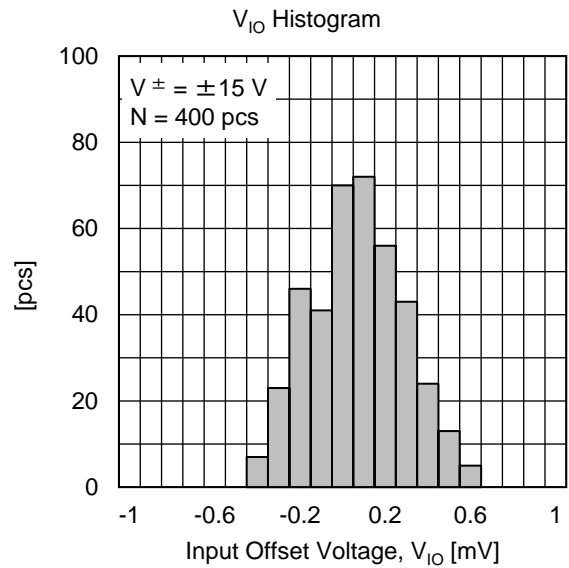
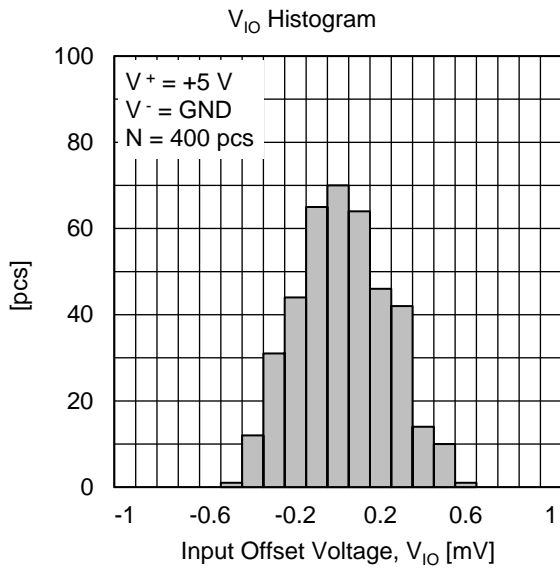
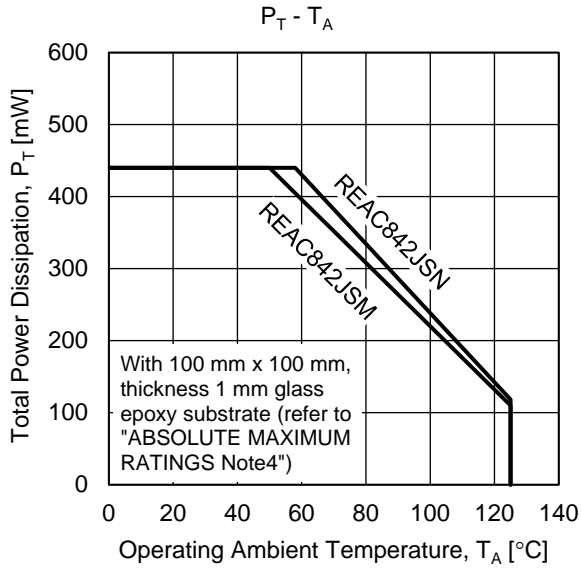
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V <sub>IO</sub>		±0.3	±1	mV	V <sub>IN</sub> = 1/2 V <sub>CC</sub> , R <sub>S</sub> ≤ 50 Ω
Input Offset Current	I <sub>IO</sub>		±6	±75	nA	
Input Bias Current <sup>Note 7</sup>	I <sub>B</sub>		75	200	nA	
Large Signal Voltage Gain	A <sub>V</sub>	25,000	600,000			R <sub>L</sub> ≥ 2 kΩ
Circuit Current <sup>Note 8</sup>	I <sub>CC</sub>		3.3	5	mA	I <sub>O</sub> = 0 A
Common Mode Rejection Ratio	CMR	70	95		dB	
Supply Voltage Rejection Ratio	SVR	70	95		dB	
Output Voltage (High)	V <sub>OH1</sub>	3.8	-	-	V	R <sub>L</sub> = 10 kΩ (Connected to GND)
	V <sub>OH2</sub>	3.7	-	-	V	R <sub>L</sub> = 2 kΩ (Connected to GND)
Output Voltage (Low)	V <sub>OL1</sub>	-	-	30	mV	R <sub>L</sub> = 10 kΩ (Connected to GND)
	V <sub>OL2</sub>	-	-	30	mV	R <sub>L</sub> = 2 kΩ (Connected to GND)
Common Mode Input Voltage Range	V <sub>ICM</sub>	0		V <sup>+</sup> -1.8	V	
Output Source Current	I <sub>O SOURCE</sub>	10	30		mA	V <sub>IN (+)</sub> = +1 V, V <sub>IN (-)</sub> = 0 V
Output Sink Current	I <sub>O SINK</sub>	10	30		mA	V <sub>IN (+)</sub> = 0 V, V <sub>IN (-)</sub> = +1 V
Slew Rate	SR		5.5		V/μs	A <sub>V</sub> = +1 (Rise Edge)

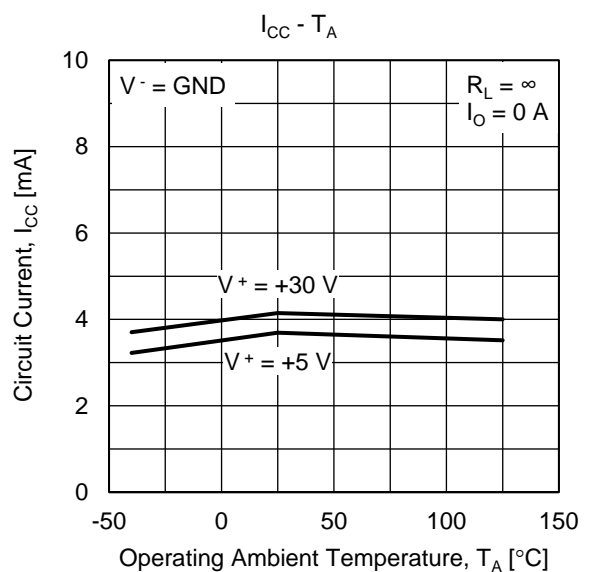
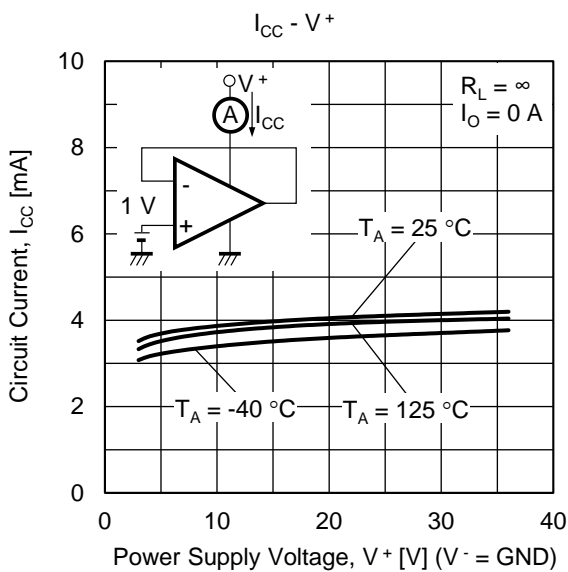
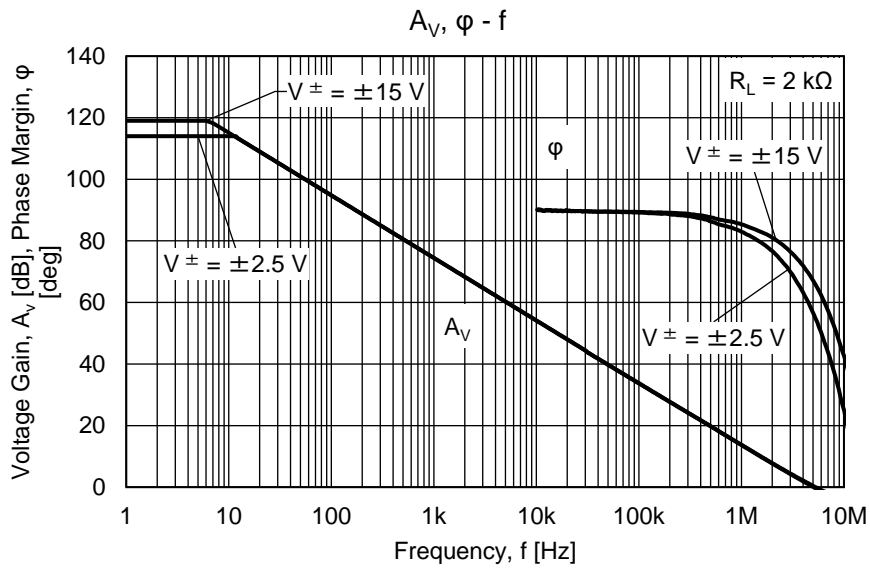
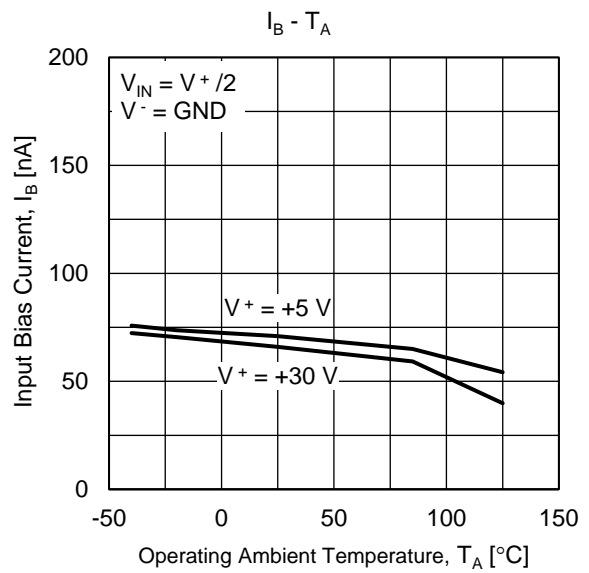
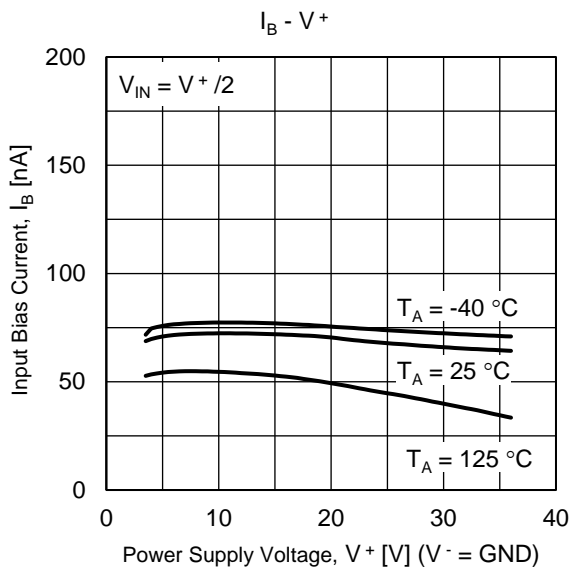
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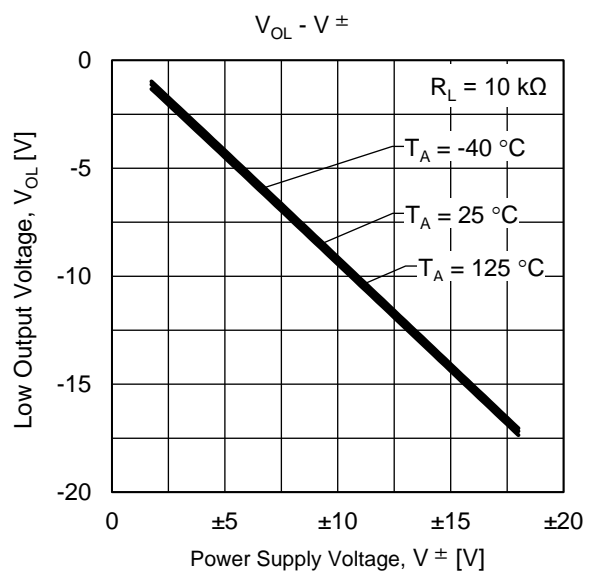
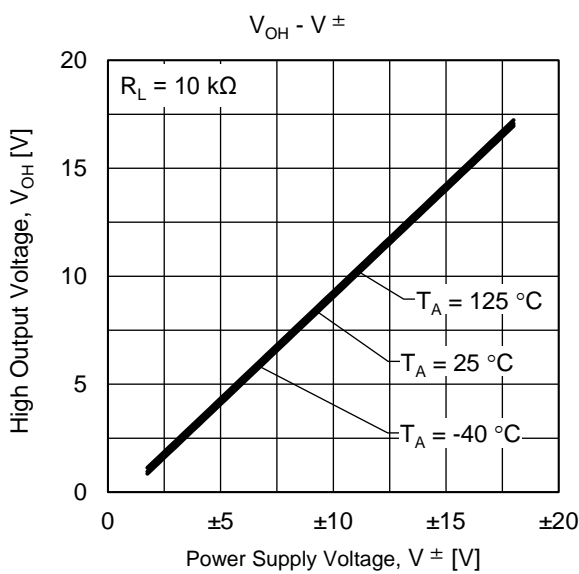
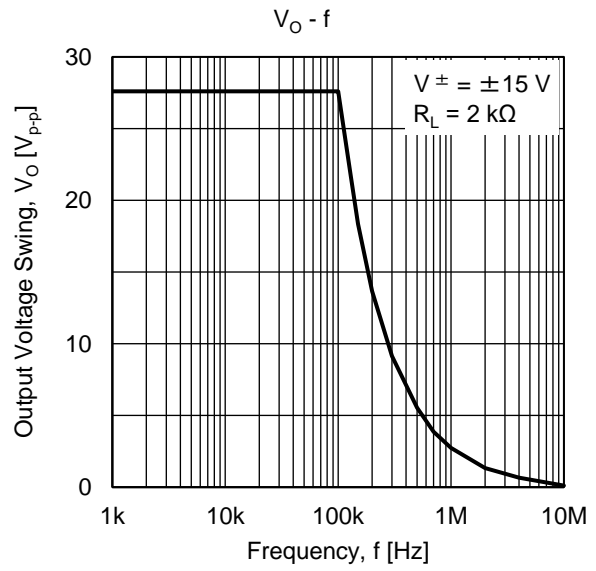
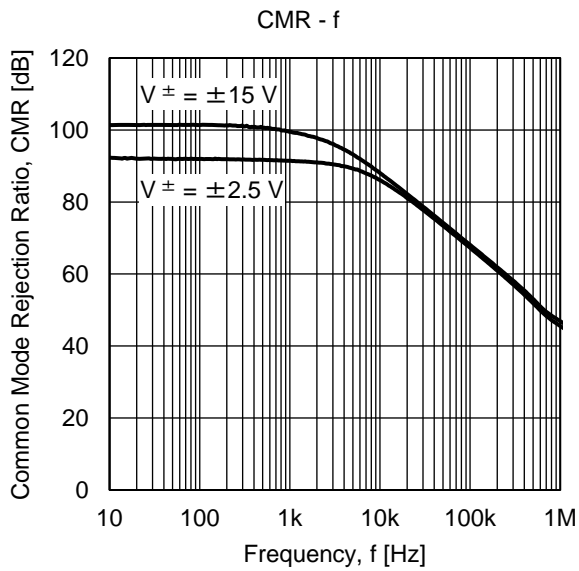
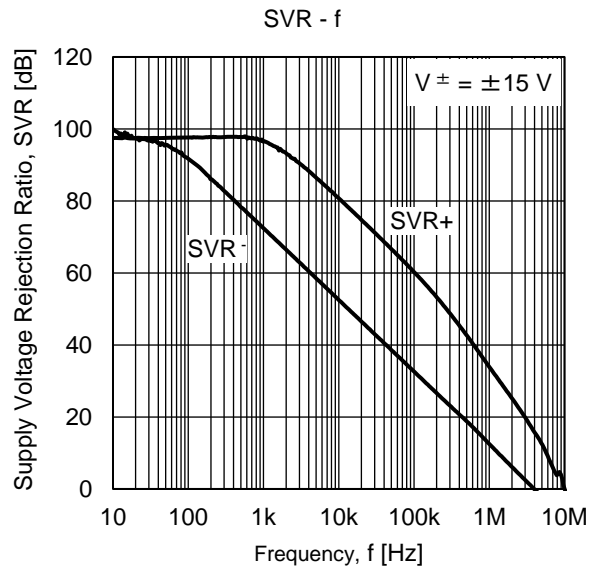
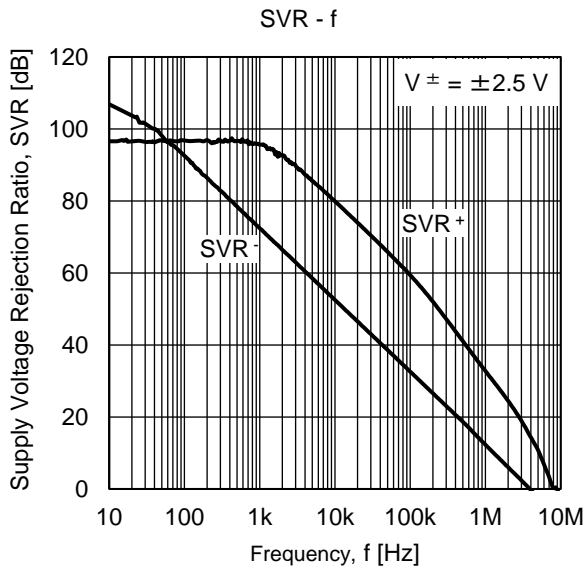
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V <sub>IO</sub>		±0.3	±1	mV	V <sub>IN</sub> = 1/2 V <sub>CC</sub> , R <sub>S</sub> ≤ 50 Ω
Input Offset Current	I <sub>IO</sub>			±90	nA	
Input Bias Current <sup>Note 7</sup>	I <sub>B</sub>			200	nA	
Large Signal Voltage Gain	A <sub>V</sub>	5,000				R <sub>L</sub> ≥ 2 kΩ
Circuit Current <sup>Note 8</sup>	I <sub>CC</sub>			6	mA	I <sub>O</sub> = 0 A
Common Mode Rejection Ratio	CMR	50			dB	
Supply Voltage Rejection Ratio	SVR	60			dB	
Output Voltage (High)	V <sub>OH1</sub>	3.7	-	-	V	R <sub>L</sub> = 10 kΩ (Connected to GND)
	V <sub>OH2</sub>	3,6	-	-	V	R <sub>L</sub> = 2 kΩ (Connected to GND)
Output Voltage (Low)	V <sub>OL1</sub>	-	-	60	mV	R <sub>L</sub> = 10 kΩ (Connected to GND)
	V <sub>OL2</sub>	-	-	60	mV	R <sub>L</sub> = 2 kΩ (Connected to GND)
Common Mode Input Voltage Range	V <sub>ICM</sub>	0		V <sup>+</sup> -2.5	V	
Output Source Current	I <sub>O SOURCE</sub>	5			mA	V <sub>IN (+)</sub> = +1 V, V <sub>IN (-)</sub> = 0 V
Output Sink Current	I <sub>O SINK</sub>	5			mA	V <sub>IN (+)</sub> = 0 V, V <sub>IN (-)</sub> = +1 V

- Notes:
7. The current flow direction of the input bias is out from the IC because the first stage of the IC composed of PNP transistor.
  8. Current flowing through the internal circuit of this IC. This current flow regardless of the channel used.

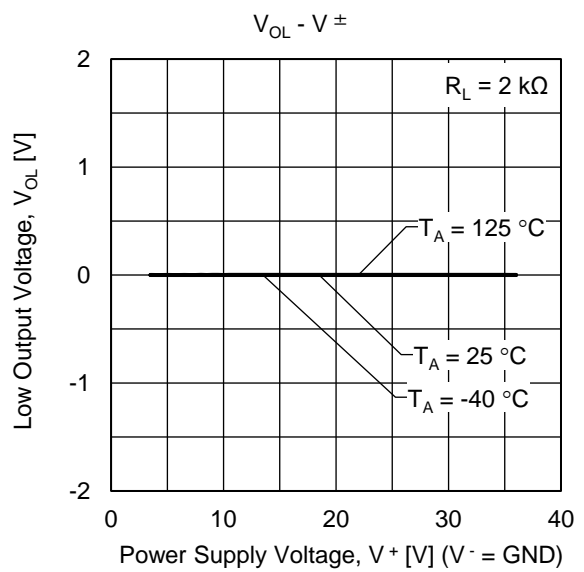
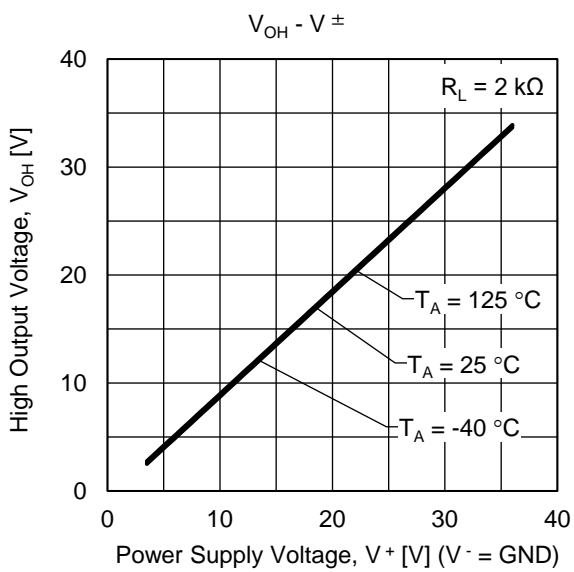
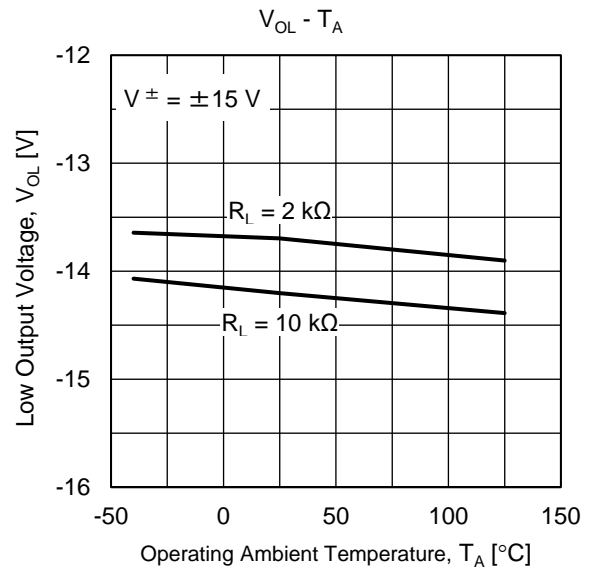
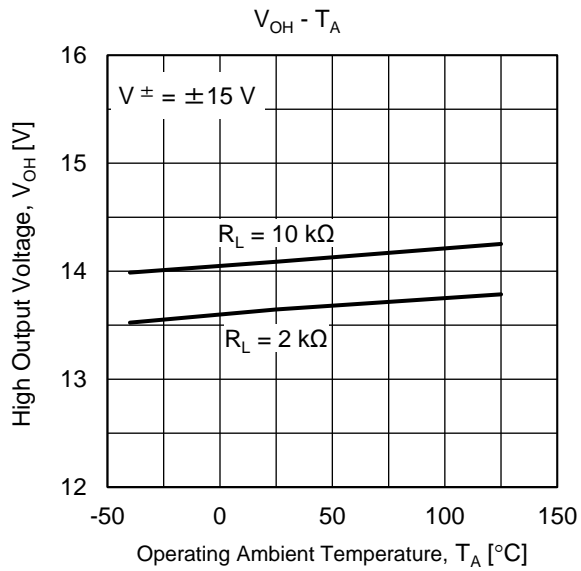
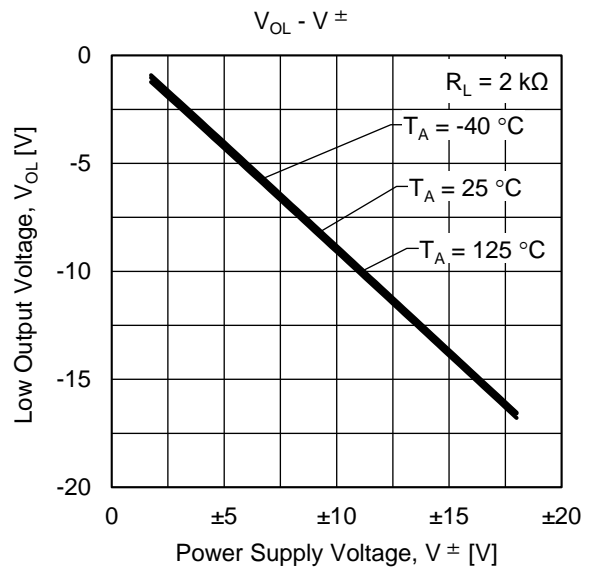
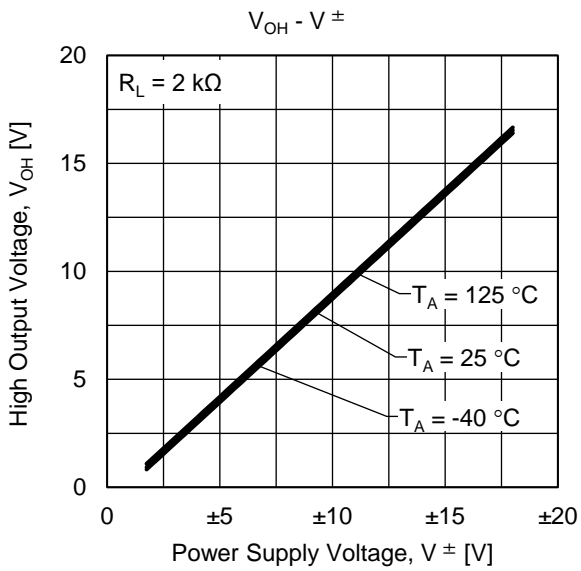
**CHARACTERISTICS CURVE ( $T_A = 25\text{ }^\circ\text{C}$ , TYP.) (REFERENCE VALUE)**

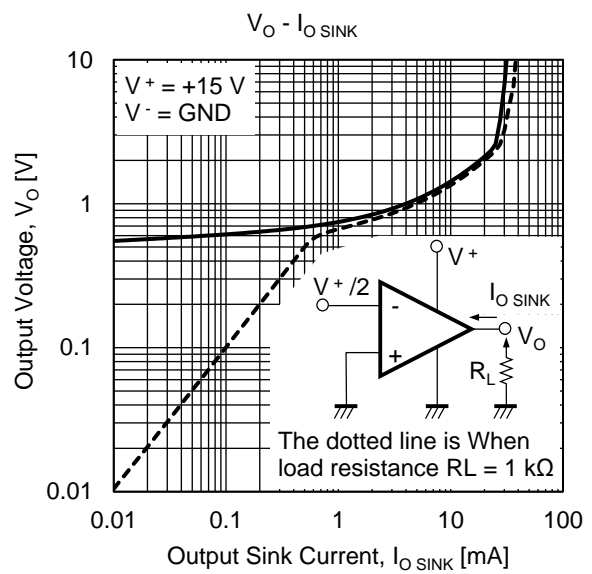
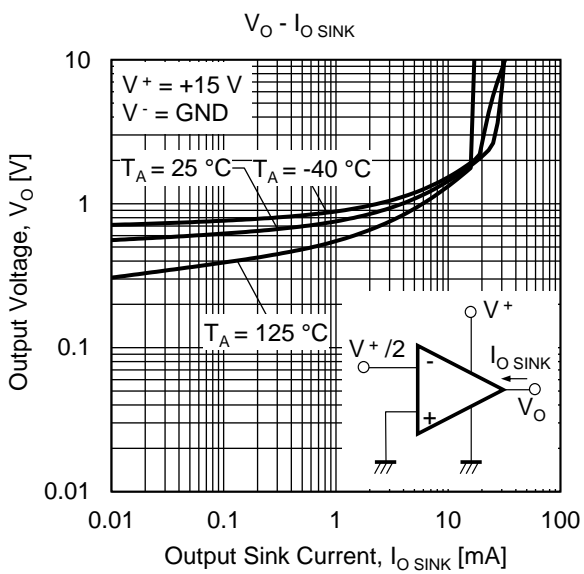
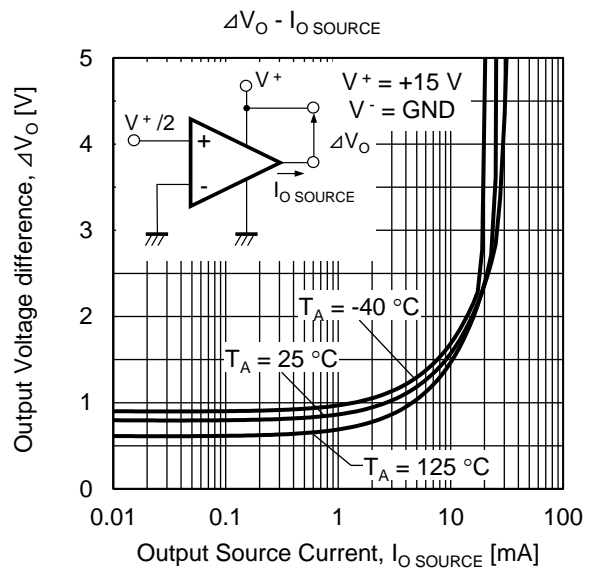
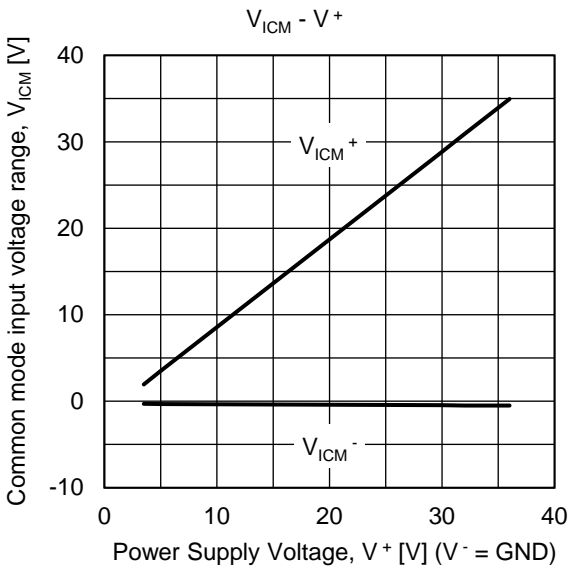
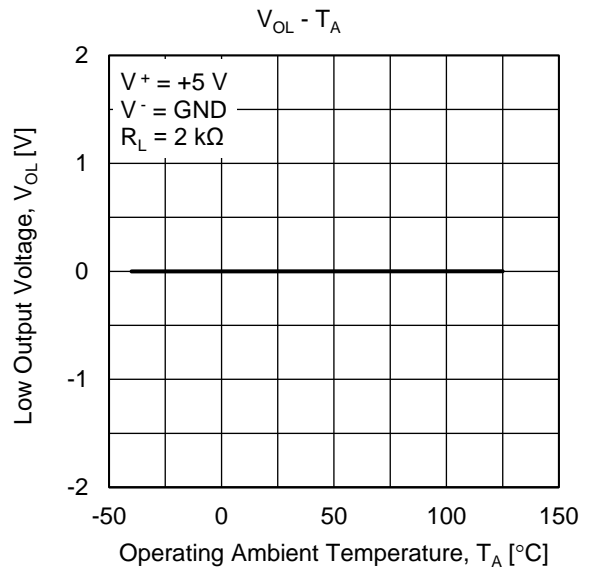
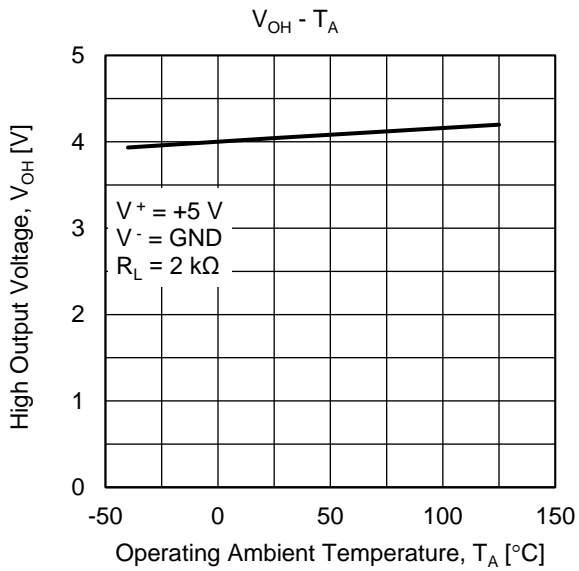


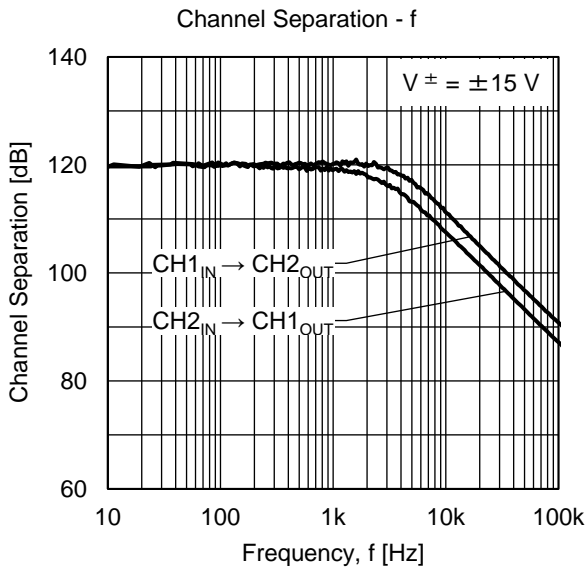
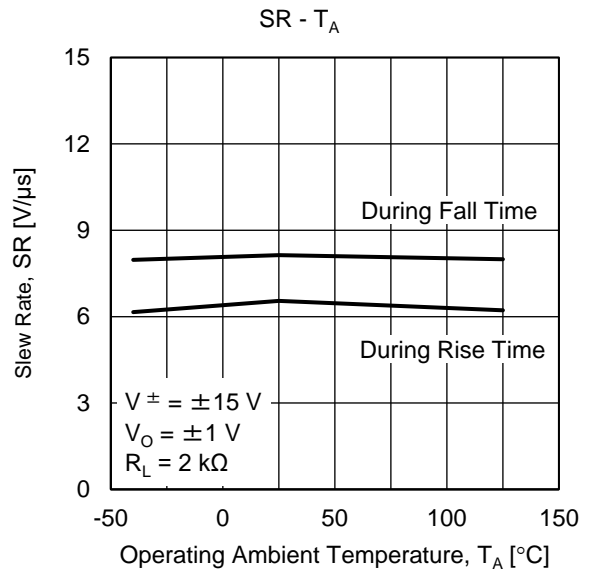
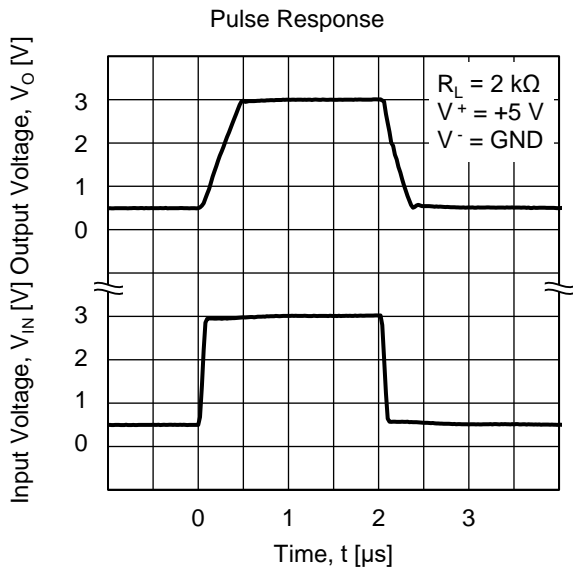








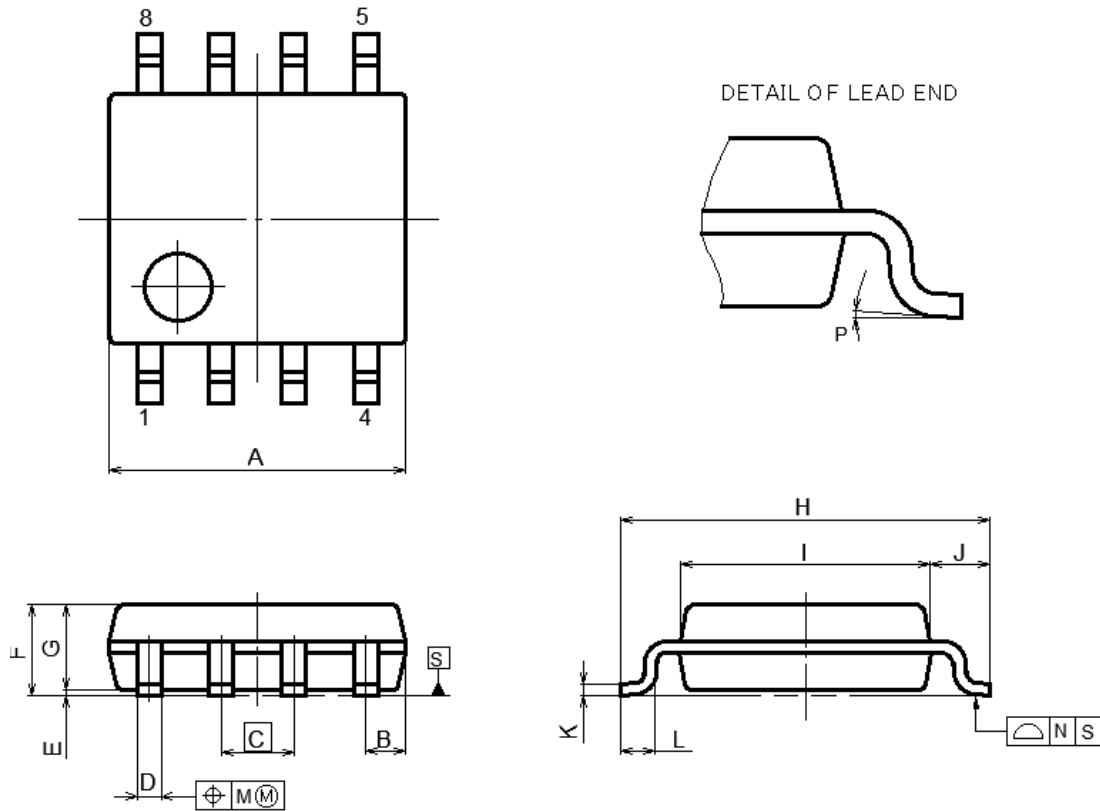




**PACKAGE DRAWINGS:**

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LSOP8-4.4x5.2-1.27	PLSP0008DE-A	0.09[g]



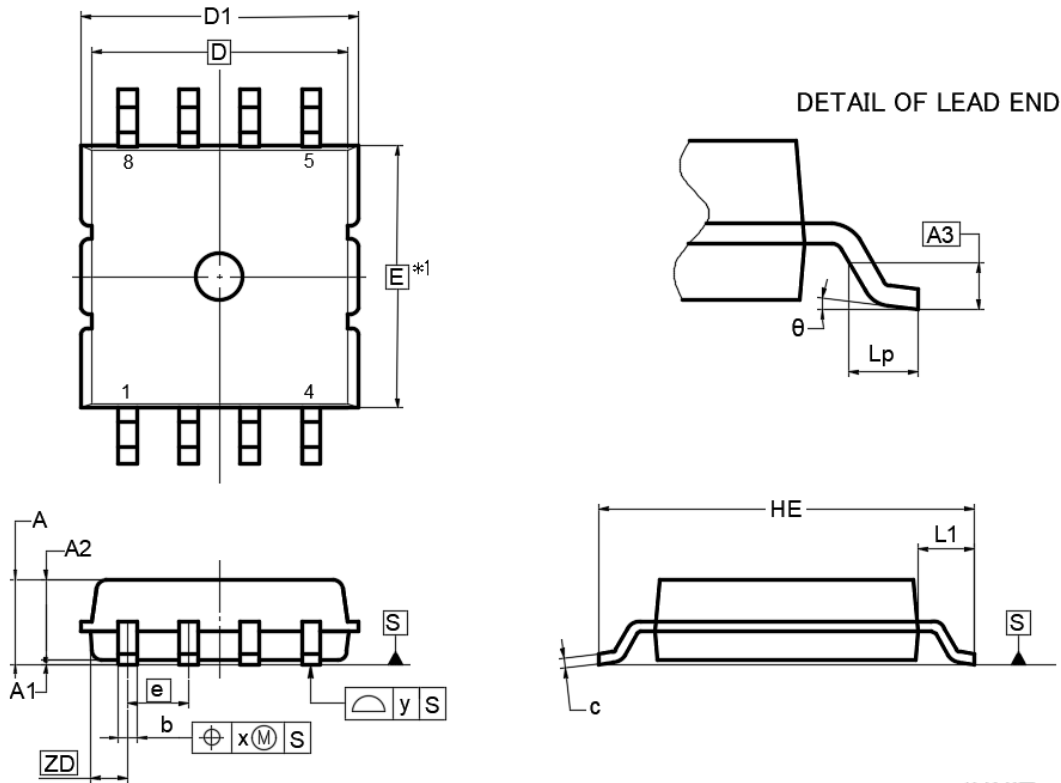
NOTE  
 EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

8-PIN PLASTIC MSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-VSSOP8-2.75x2.8-0.65	PVSP0008JA-A	—	0.02[g]



NOTE) .  
 1. DIMENSIONS "\*1"  
 DO NOT INCLUDE MOLD FLASH.  
 2. EACH LEAD CENTERLINE IS LOCATED WITHIN 0.10 MM OF  
 ITS TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

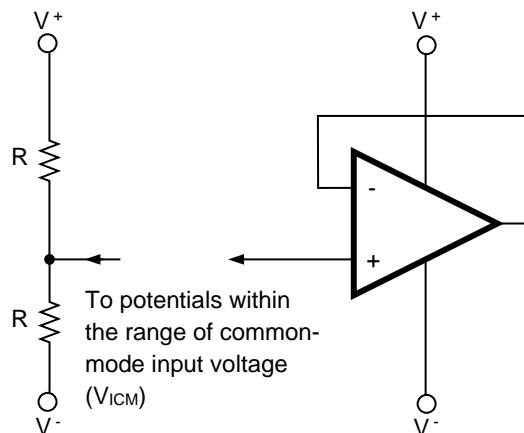
ITEM	DIMENSIONS
D	2.75
D1	2.95±0.20
E	2.80
HE	4.00±0.30
e	0.65
b	0.20 <sup>+0.10</sup> <sub>-0.05</sub>
A	1.00MAX
A1	0.05±0.05
A2	0.85±0.10
A3	0.25
L1	0.60±0.20
c	0.13 <sup>+0.10</sup> <sub>-0.05</sub>
Lp	0.37±0.12
x	0.10
y	0.10
θ	7±7°
ZD	0.50

## USE WITH PRECAUTIONS

### Managing unused circuits

If there is an unused circuit, the following connection is recommended.

#### Process example of unused circuits



Remark: In this example, an intermediate potential between  $V^+$  and  $V^-$  is applied.

### Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than  $V^-$ , or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

### Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} \text{ (TYP.) : } V^- \text{ to } V^+ - 1.8 \text{ [V] (} T_A = 25 \text{ }^\circ\text{C)}$$

During designing, do include some tolerance by considering temperature characteristics etc.

### Maximum Output Voltage

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{Om^+} \text{ (TYP.) : } V^+ - 1 \text{ [V] (} T_A = 25 \text{ }^\circ\text{C)}, V_{Om^-} \text{ (TYP.) : } V^- + 0.7 \text{ [V] (} T_A = 25 \text{ }^\circ\text{C)}$$

During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ( $V_{Om^+}$  to  $V_{Om^-}$ ) will become narrow when the output current increases.

### Output Operation

This IC will not be able to sink output current when the output voltage is  $V^- + 0.7 \text{ V}$  and below. In this case, the output voltage level can be improved to the  $V^-$  side by connecting the load resistor between the output terminal and  $V^-$  to sink the current at the load resistor. (The effect will differ depending on the flow of current in the load resistance.)

### Handling of ICs

When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

## Notice

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