RC38616/RC38412

FemtoClock™4 Radio Synchronizer and Multi-Frequency Clock Synthesizer

Description

The RC38616/RC38412 is an ultra-low phase noise radio synchronizer, multi-frequency clock synthesizer, and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with ultra-low in-band phase noise and spurious for 4G and 5G RF transceivers and with jitter below 25fs-rms for 112Gbps and 224Gbps SerDes.

Applications

- 5G radio units (RU)
- 5G distribution units (DU), switches, and routers
- Reference clock for 112Gbps and 224Gbps SerDes
- High-performance DCO for Precision Time Protocol (PTP) based clocks

Features

- Ultra-low phase noise synthesizer with jitter below 25fs RMS, 12kHz to 20MHz with 4MHz HPF
- Six independent low-phase noise sync domains
- Support for JESD204B/C/D
- Time sync block with time to digital converter (TDC), time of day (TOD) counter, and PTP clocks
- Up to 18/12 (RC38616/RC38412) clock outputs with integer dividers
  - 12/8: LVDS, HCSL (AC-LVPECL), or CML
  - 6/4: LVDS, HCSL (AC-LVPECL), or LVCMOS
- Output frequency range:
  - CML: DC to 2.5GHz
  - LVDS or HCSL: DC to 1GHz
  - LVCMOS: DC to 250MHz
- Clock inputs:
  - RC38616: Up to 6 differential or 11 single-ended
  - RC38412: Up to 4 differential or single-ended
- Operates from a 1.8V supply
- Clock inputs tolerate 1.8V input when the device is powered off, sinking less than 1mA
- CLKIN input frequency range: DC to 1GHz
- Time sync TDC supports 1PPS and PP2S inputs
- DPLLs comply with ITU-T G.8262 and G.8262.1
- DPLL input-to-output phase variation ≤ 100ps
- DCO frequency resolution < 10^{-13}
- Packages:
  - RC38616: 10 × 10 mm, 144-BGA
  - RC38412: 9 × 9 mm, 100-BGA

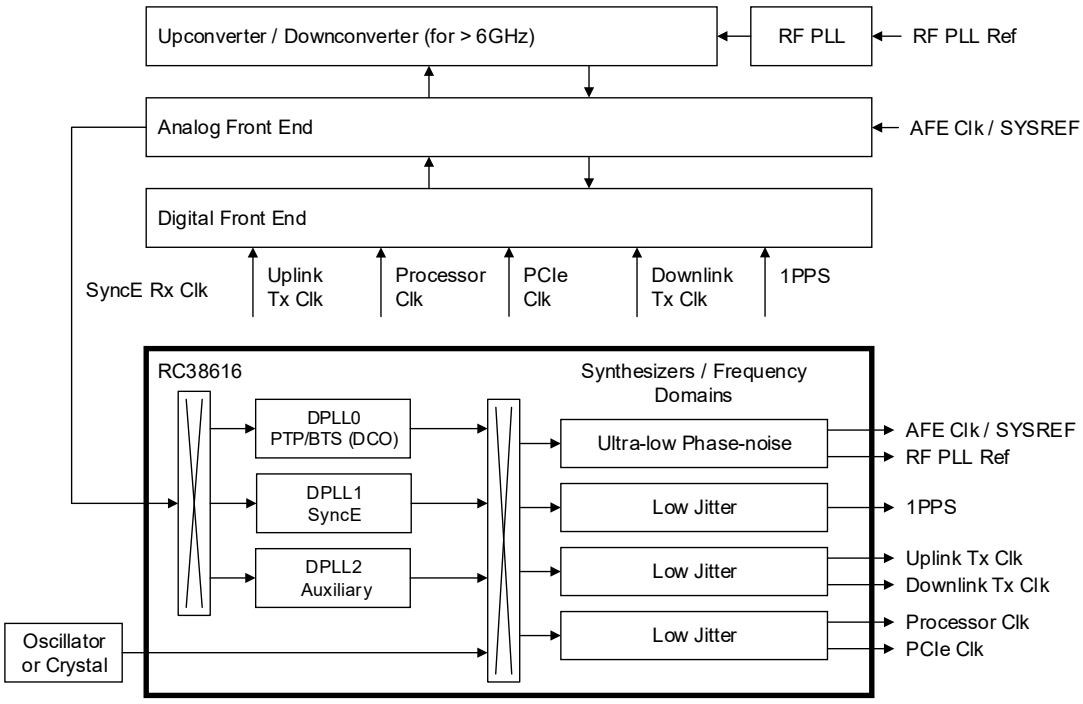


Figure 1. Typical 5G Radio Unit Use Case

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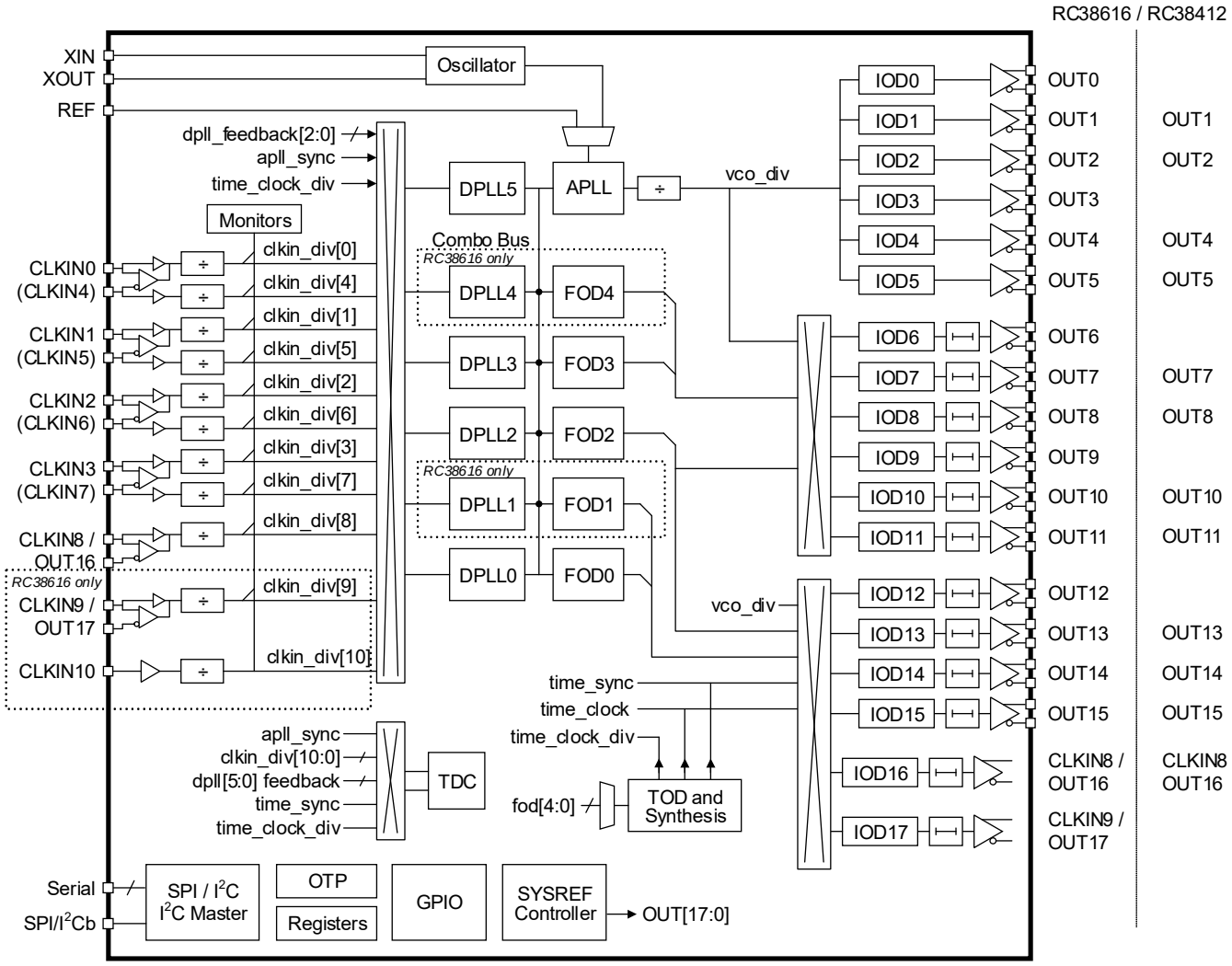


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1. Pin Information

1.1 Pin Assignments – RC38616

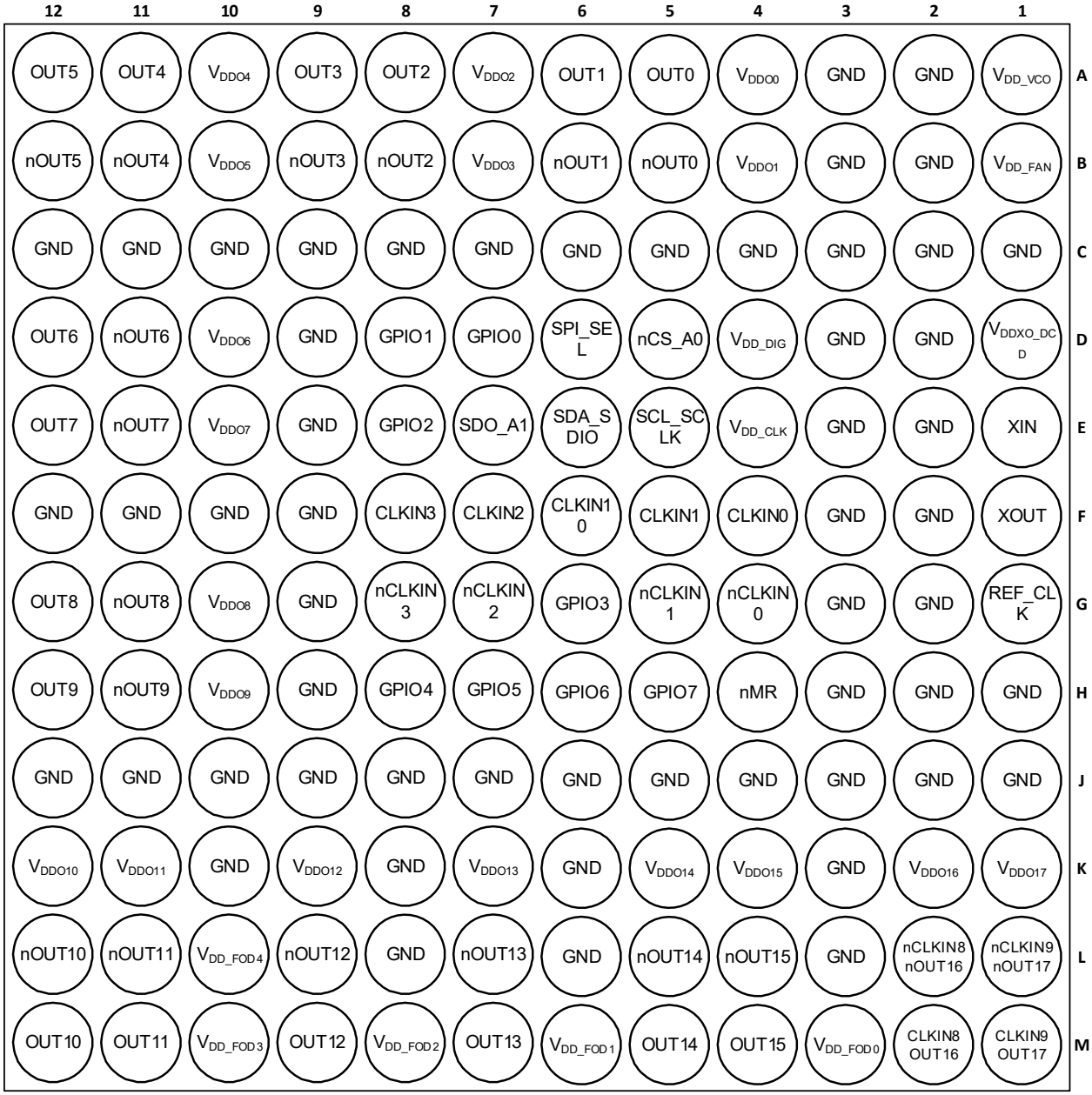


Figure 3. Pin Assignments – RC38616 (Bottom View)

1.2 Pin Descriptions – RC38616

Table 1. Pin Descriptions – RC38616

Pin Number	Pin Name	Type		Description
A1	V_{DD_VCO}	Power	-	Power supply for the VCO. 1.8V is supported.
A2	GND	Power	-	Ground reference rail.
A3	GND	Power	-	Ground reference rail.
A4	V_{DDO0}	Power	-	Power supply for OUT0/nOUT0 and IOD0. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.

Table 1. Pin Descriptions – RC38616 (Cont.)

Pin Number	Pin Name	Type		Description
A5	OUT0	O	-	Clock output 0, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A6	OUT1	O	-	Clock output 1, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A7	V_{DDO2}	Power	-	Power supply for OUT2/nOUT2 and IOD2. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
A8	OUT2	O	-	Clock output 2, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A9	OUT3	O	-	Clock output 3, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A10	V_{DDO4}	Power	-	Power supply for OUT4/nOUT4 and IOD4. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
A11	OUT4	O	-	Clock output 4, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A12	OUT5	O	-	Clock output 5, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
B1	V_{DD_FAN}	Power	-	Power supply for internal buffering to FODs and IODs. 1.8V is supported.
B2	GND	Power	-	Ground reference rail.
B3	GND	Power	-	Ground reference rail.
B4	V_{DDO1}	Power	-	Power supply for OUT1/nOUT1 and IOD1. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B5	nOUT0	O	-	Clock output 0, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B6	nOUT1	O	-	Clock output 1, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B7	VDDO3	Power	-	Power supply for OUT3/nOUT3 and IOD3. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B8	nOUT2	O	-	Clock output 2, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B9	nOUT3	O	-	Clock output 3, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B10	V_{DDO5}	O	-	Power supply for OUT5/nOUT5 and IOD5. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B11	nOUT4	O	-	Clock output 4, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B12	nOUT5	O	-	Clock output 5, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
C1	GND	Power	-	Ground reference rail.
C2	GND	Power	-	Ground reference rail.
C3	GND	Power	-	Ground reference rail.
C4	GND	Power	-	Ground reference rail.
C5	GND	Power	-	Ground reference rail.
C6	GND	Power	-	Ground reference rail.
C7	GND	Power	-	Ground reference rail.
C8	GND	Power	-	Ground reference rail.

Table 1. Pin Descriptions – RC38616 (Cont.)

Pin Number	Pin Name	Type		Description
C9	GND	Power	-	Ground reference rail.
C10	GND	Power	-	Ground reference rail.
C11	GND	Power	-	Ground reference rail.
C12	GND	Power	-	Ground reference rail.
D1	V_{DDXO_DCD}	Power	-	Power supply for XIN, XOUT, REF_CLK and the DCD block. 1.8V is supported.
D2	GND	Power	-	Ground reference rail.
D3	GND	Power	-	Ground reference rail.
D4	V_{DD_DIG}	Power	-	Power supply for digital core, nMR, serial port. 1.8V, 2.5V, and 3.3V are supported.
D5	nCS_A0	I	Pull-up	SPI mode: active-low chip select. I2C mode: address bit 0. GPIO DC electrical characteristics apply to this pin.
D6	SPI_SEL	I	Pull-up	Selects between I2C and SPI interface (default, pull-up selects SPI).
D7	GPIO0	I/O	Pull-up	General purpose input/output 0.
D8	GPIO1	I/O	Pull-up	General purpose input/output 1.
D9	GND	Power	-	Ground reference rail.
D10	V_{DDO6}	Power	-	Power supply for OUT6/nOUT6 and IOD6. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
D11	nOUT6	O	-	Clock output 6, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
D12	OUT6	O	-	Clock output 6, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
E1	XIN	I	-	Crystal oscillator input. A quartz crystal resonator, for the internal oscillator circuitry, may be connected between XIN and XOUT. Leave this pin unconnected if a crystal resonator is not used.
E2	GND	Power	-	Ground reference rail.
E3	GND	Power	-	Ground reference rail.
E4	V_{DD_CLK}	Power	-	Power supply for CLKINx buffers and the GPIOs. 1.8V is supported.
E5	SCL_SCLK	I/O	Pull-up	I2C mode: I2C interface bi-directional clock. SPI mode: serial clock. GPIO DC electrical characteristics apply to this pin.
E6	SDA_SDIO	I/O	Pull-up	I2C mode: I2C interface bi-directional serial data. SPI 3-wire mode: bi-directional serial data. SPI 4-wire mode: input serial data. GPIO DC electrical characteristics apply to this pin.
E7	SDO_A1	I/O	Pull-up	SPI 3-wire mode: unused. SPI 4-wire mode: output serial data. I2C mode: address bit 1. GPIO DC electrical characteristics apply to this pin.
E8	GPIO2	I/O		General purpose input/output 2.
E9	GND	Power	-	Ground reference rail.
E10	V_{DDO7}	Power	-	Power supply for OUT7/nOUT7 and IOD7. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
E11	nOUT7	O	-	Clock output 7, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
E12	OUT7	O	-	Clock output 7, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
F1	XOUT	O	-	Crystal oscillator output. A quartz crystal resonator, for the internal oscillator circuitry, may be connected between XIN and XOUT. Leave this pin unconnected if a crystal resonator is not used.
F2	GND	Power	-	Ground reference rail.
F3	GND	Power	-	Ground reference rail.

Table 1. Pin Descriptions – RC38616 (Cont.)

Pin Number	Pin Name	Type		Description
F4	CLKIN0	I	Pull-down	Clock reference input 0, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F5	CLKIN1	I	Pull-down	Clock reference input 1, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F6	CLKIN10	I	Pull-down	Clock reference input 10, single-ended.
F7	CLKIN2	I	Pull-down	Clock reference input 2, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F8	CLKIN3	I	Pull-down	Clock reference input 3, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F9	GND	Power	-	Ground reference rail.
F10	GND	Power	-	Ground reference rail.
F11	GND	Power	-	Ground reference rail.
F12	GND	Power	-	Ground reference rail.
G1	REF_CLK	I	-	APLL frequency reference, single ended. Leave this pin unconnected if a quartz crystal resonator is connected between XIN and XOUT.
G2	GND	Power	-	Ground reference rail.
G3	GND	Power	-	Ground reference rail.
G4	nCLKIN0	I	Pull-up	Clock reference input 0, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G5	nCLKIN1	I	Pull-up	Clock reference input 1, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G6	GPIO3	I/O		General purpose input/output 3.
G7	nCLKIN2	I	Pull-up	Clock reference input 2, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G8	nCLKIN3	I	Pull-up	Clock reference input 3, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G9	GND	Power	-	Ground reference rail.
G10	V_{DDO8}	Power	-	Power supply for OUT8/nOUT8 and IOD8. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
G11	nOUT8	O	-	Clock output 8, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
G12	OUT8	O	-	Clock output 8, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
H1	GND	Power	-	Ground reference rail.
H2	GND	Power	-	Ground reference rail.
H3	GND	Power	-	Ground reference rail.
H4	nMR	I	Pull-up	Active-low master reset.
H5	GPIO7	I/O	Pull-up	General purpose input/output 7.
H6	GPIO6	I/O	Pull-up	General purpose input/output 6.
H7	GPIO5	I/O	Pull-up	General purpose input/output 5.
H8	GPIO4	I/O	Pull-up	General purpose input/output 4.
H9	GND	Power	-	Ground reference rail.
H10	V_{DDO9}	Power	-	Power supply for OUT9/nOUT9 and IOD9. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
H11	nOUT9	O	-	Clock output 9, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.

Table 1. Pin Descriptions – RC38616 (Cont.)

Pin Number	Pin Name	Type		Description
H12	OUT9	O	-	Clock output 9, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
J1	GND	Power	-	Ground reference rail.
J2	GND	Power	-	Ground reference rail.
J3	GND	Power	-	Ground reference rail.
J4	GND	Power	-	Ground reference rail.
J5	GND	Power	-	Ground reference rail.
J6	GND	Power	-	Ground reference rail.
J7	GND	Power	-	Ground reference rail.
J8	GND	Power	-	Ground reference rail.
J9	GND	Power	-	Ground reference rail.
J10	GND	Power	-	Ground reference rail.
J11	GND	Power	-	Ground reference rail.
J12	GND	Power	-	Ground reference rail.
K1	V_{DDO17}	Power	-	Power supply for OUT17/nOUT17 and IOD17. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K2	V_{DDO16}	Power	-	Power supply for OUT16/nOUT16 and IOD16. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K3	GND	Power	-	Ground reference rail.
K4	V_{DDO15}	Power	-	Power supply for OUT15/nOUT15 and IOD15. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K5	V_{DDO14}	Power	-	Power supply for OUT14/nOUT14 and IOD14. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K6	GND	Power	-	Ground reference rail.
K7	V_{DDO13}	Power	-	Power supply for OUT13/nOUT13 and IOD13. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K8	GND	Power	-	Ground reference rail.
K9	V_{DDO12}	Power	-	Power supply for OUT12/nOUT12 and IOD12. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K10	GND	Power	-	Ground reference rail.
K11	V_{DDO11}	Power	-	Power supply for OUT11/nOUT11 and IOD11. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K12	V_{DDO10}	Power	-	Power supply for OUT10/nOUT10 and IOD10. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
L1	nCLKIN9 / nOUT17	I/O	-	Clock input mode: Clock reference input 9, differential pair. nCLKINx indicates the negative pin of a differential pair. Clock output mode: Clock output 17, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
L2	nCLKIN8 / nOUT16	I/O	-	Clock input mode: Clock reference input 8, differential pair. nCLKINx indicates the negative pin of a differential pair. Clock output mode: Clock output 16, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.

Table 1. Pin Descriptions – RC38616 (Cont.)

Pin Number	Pin Name	Type		Description
L3	GND	Power	-	Ground reference rail.
L4	nOUT15	O	-	Clock output 15, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
L5	nOUT14	O	-	Clock output 14, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
L6	GND	Power	-	Ground reference rail.
L7	nOUT13	O	-	Clock output 13, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
L8	GND	Power	-	Ground reference rail.
L9	nOUT12	O	-	Clock output 12, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
L10	V_{DD_FOD4}	Power	-	Power supply for FOD4, 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding FOD is unused. This pin must not be allowed to float.
L11	nOUT11	O	-	Clock output 11, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
L12	nOUT10	O	-	Clock output 10, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
M1	CLKIN9 / OUT17	I/O	-	Clock input mode: Clock reference input 9, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair. Clock output mode: Clock output 17, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
M2	CLKIN8 / OUT16	I/O	-	Clock input mode: Clock reference input 8, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair. Clock output mode: Clock output 16, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
M3	V_{DD_FOD0}	Power	-	Power supply for FOD0, 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding FOD is unused. This pin must not be allowed to float.
M4	OUT15	O	-	Clock output 15, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
M5	OUT14	O	-	Clock output 14, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
M6	V_{DD_FOD1}	Power	-	Power supply for FOD1 and internal buffering to the IODs for OUT12-17, 1.8V is supported.
M7	OUT13	O	-	Clock output 13, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
M8	V_{DD_FOD2}	Power	-	Power supply for FOD2, 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding FOD is unused. This pin must not be allowed to float.
M9	OUT12	O	-	Clock output 12, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
M10	V_{DD_FOD3}	Power	-	Power supply for FOD3, 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding FOD is unused. This pin must not be allowed to float.
M11	OUT11	O	-	Clock output 11, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
M12	OUT10	O	-	Clock output 10, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.

1.3 Pin Assignments – RC38412

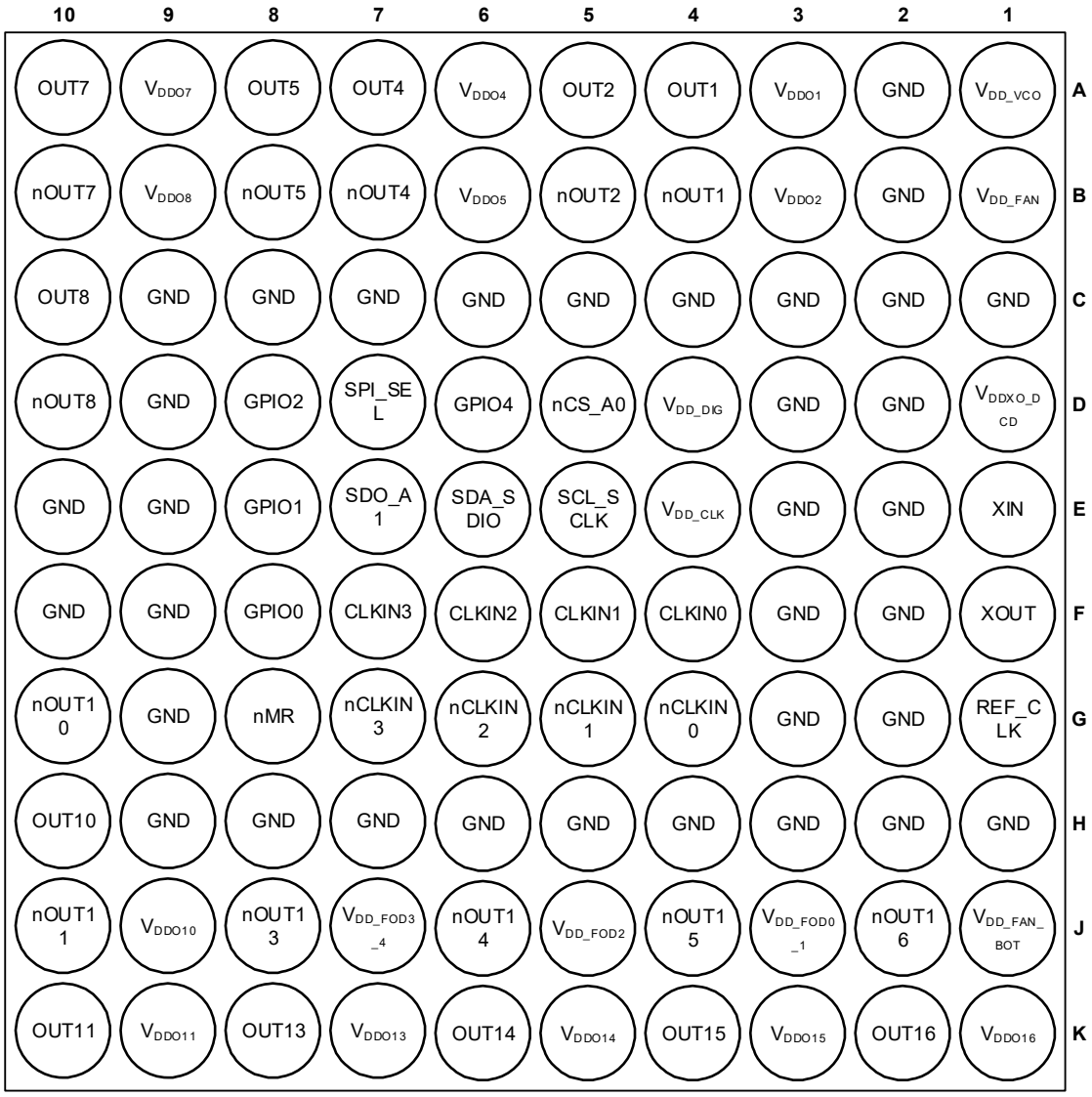


Figure 4. Pin Assignments – RC38412 (Bottom View)

1.4 Pin Descriptions – RC38412

Table 2. Pin Descriptions – RC38412

Pin Number	Pin Name	Type		Description
A1	V_{DD_VCO}	Power	-	Power supply for the VCO. 1.8V is supported.
A2	GND	Power	-	Ground reference rail.
A3	V_{DDO1}	Power	-	Power supply for OUT1/nOUT1 and IOD1. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
A4	OUT1	O	-	Clock output 0, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A5	OUT2	O	-	Clock output 2, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A6	V_{DDO4}	Power	-	Power supply for OUT4/nOUT4 and IOD4. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.

Table 2. Pin Descriptions – RC38412 (Cont.)

Pin Number	Pin Name	Type		Description
A7	OUT4	O	-	Clock output 4, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A8	OUT5	O	-	Clock output 5, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
A9	V_{DDO7}	Power	-	Power supply for OUT7/nOUT7 and IOD7. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
A10	OUT7	O	-	Clock output 7, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
B1	V_{DD_FAN}	Power	-	Power supply for internal buffering to FODs and IODs. 1.8V is supported.
B2	GND	Power	-	Ground reference rail.
B3	V_{DDO2}	Power	-	Power supply for OUT2/nOUT2 and IOD2. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B4	nOUT1	O	-	Clock output 0, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B5	nOUT2	O	-	Clock output 2, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B6	V_{DDO5}	Power	-	Power supply for OUT5/nOUT5 and IOD5. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B7	nOUT4	O	-	Clock output 4, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B8	nOUT5	O	-	Clock output 5, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
B9	V_{DDO8}	Power	-	Power supply for OUT8/nOUT8 and IOD8. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
B10	nOUT7	O	-	Clock output 7, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
C1	GND	Power	-	Ground reference rail.
C2	GND	Power	-	Ground reference rail.
C3	GND	Power	-	Ground reference rail.
C4	GND	Power	-	Ground reference rail.
C5	GND	Power	-	Ground reference rail.
C6	GND	Power	-	Ground reference rail.
C7	GND	Power	-	Ground reference rail.
C8	GND	Power	-	Ground reference rail.
C9	GND	Power	-	Ground reference rail.
C10	OUT8	O	-	Clock output 8, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
D1	V_{DDXO_DCD}	Power	-	Power supply for XIN, XOUT, REF_CLK and the DCD block. 1.8V is supported.
D2	GND	Power	-	Ground reference rail.
D3	GND	Power	-	Ground reference rail.
D4	V_{DD_DIG}	Power	-	Power supply for digital core, nMR, serial port. 1.8V, 2.5V, and 3.3V are supported.
D5	nCS_A0	I	Pull-up	SPI mode: active-low chip select. I2C mode: address bit 0. GPIO DC electrical characteristics apply to this pin.
D6	GPIO4	I/O	Pull-up	General purpose input/output 4.
D7	SPI_SEL	I	Pull-up	Selects between I2C and SPI interface (default, pull-up selects SPI).

Table 2. Pin Descriptions – RC38412 (Cont.)

Pin Number	Pin Name	Type		Description
D8	GPIO2	I/O	Pull-up	General purpose input/output 2.
D9	GND	Power	-	Ground reference rail.
D10	nOUT8	O	-	Clock output 8, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
E1	XIN	I	-	Crystal oscillator input. A quartz crystal resonator, for the internal oscillator circuitry, may be connected between XIN and XOUT. Leave this pin unconnected if a crystal resonator is not used.
E2	GND	Power	-	Ground reference rail.
E3	GND	Power	-	Ground reference rail.
E4	VDD_CLK	Power	-	Power supply for CLKINx buffers and the GPIOs. 1.8V is supported.
E5	SCL_SCLK	I/O	Pull-up	I2C mode: I2C interface bi-directional clock. SPI mode: serial clock. GPIO DC electrical characteristics apply to this pin.
E6	SDA_SDIO	I/O	Pull-up	I2C mode: I2C interface bi-directional serial data. SPI 3-wire mode: bi-directional serial data. SPI 4-wire mode: input serial data. GPIO DC electrical characteristics apply to this pin.
E7	SDO_A1	I/O	Pull-up	SPI 3-wire mode: unused. SPI 4-wire mode: output serial data. I2C mode: address bit 1. GPIO DC electrical characteristics apply to this pin.
E8	GPIO1	I/O	Pull-up	General purpose input/output 1.
E9	GND	Power	-	Ground reference rail.
E10	GND	Power	-	Ground reference rail.
F1	XOUT	O	-	Crystal oscillator output. A quartz crystal resonator, for the internal oscillator circuitry, may be connected between XIN and XOUT. Leave this pin unconnected if a crystal resonator is not used.
F2	GND	Power	-	Ground reference rail.
F3	GND	Power	-	Ground reference rail.
F4	CLKIN0	I	Pull-down	Clock reference input 0, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F5	CLKIN1	I	Pull-down	Clock reference input 1, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F6	CLKIN2	I	Pull-down	Clock reference input 2, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F7	CLKIN3	I	Pull-down	Clock reference input 3, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair.
F8	GPIO0	I/O	Pull-up	General purpose input/output 0.
F9	GND	Power	-	Ground reference rail.
F10	GND	Power	-	Ground reference rail.
G1	REF_CLK	I	Pull-down	APLL frequency reference, single ended. Leave this pin unconnected if a quartz crystal resonator is connected between XIN and XOUT.
G2	GND	Power	-	Ground reference rail.
G3	GND	Power	-	Ground reference rail.
G4	nCLKIN0	I	Pull-up	Clock reference input 0, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G5	nCLKIN1	I	Pull-up	Clock reference input 1, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G6	nCLKIN2	I	Pull-up	Clock reference input 2, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G7	nCLKIN3	I	Pull-up	Clock reference input 3, differential pair / single-ended. nCLKINx indicates the negative pin of a differential pair.
G8	nMR	I	Pull-up	Active-low master reset.

Table 2. Pin Descriptions – RC38412 (Cont.)

Pin Number	Pin Name	Type		Description
G9	GND	Power	-	Ground reference rail.
G10	nOUT10	O	-	Clock output 10, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
H1	GND	Power	-	Ground reference rail.
H2	GND	Power	-	Ground reference rail.
H3	GND	Power	-	Ground reference rail.
H4	GND	Power	-	Ground reference rail.
H5	GND	Power	-	Ground reference rail.
H6	GND	Power	-	Ground reference rail.
H7	GND	Power	-	Ground reference rail.
H8	GND	Power	-	Ground reference rail.
H9	GND	Power	-	Ground reference rail.
H10	OUT10	O	-	Clock output 10, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.
J1	$V_{DD_FAN_BOT}$	Power	-	Power supply for internal buffering to the IODs for OUT13-16. 1.8V is supported.
J2	nCLKIN8 / nOUT16	I/O	-	Clock input mode: Clock reference input 8, differential pair. nCLKINx indicates the negative pin of a differential pair. Clock output mode: Clock output 16, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J3	$V_{DD_FOD0_}1$	Power	-	Power supply for FOD0, 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding FOD is unused. This pin must not be allowed to float.
J4	nOUT15	O	-	Clock output 15, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J5	V_{DD_FOD2}	Power	-	Power supply for FOD2, 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding FOD is unused. This pin must not be allowed to float.
J6	nOUT14	O	-	Clock output 14, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J7	$V_{DD_FOD3_}4$	Power	-	Power supply for FOD3, 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding FOD is unused. This pin must not be allowed to float.
J8	nOUT13	O	-	Clock output 13, differential pair / single ended. LVDS, HCSL, or LVCMOS. nOUTx indicates the negative pin of a differential pair.
J9	V_{DDO10}	Power	-	Power supply for OUT10/nOUT10 and IOD10. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
J10	nOUT11	O	-	Clock output 11, differential pair. LVDS, HCSL, or CML. nOUTx indicates the negative pin of a differential pair.
K1	V_{DDO16}	Power	-	Power supply for OUT16/nOUT16 and IOD16. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K2	CLKIN8 / OUT16	I/O	-	Clock input mode: Clock reference input 8, differential pair / single-ended. CLKINx indicates the positive pin of a differential pair. Clock output mode: Clock output 16, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
K3	V_{DDO15}	Power	-	Power supply for OUT15/nOUT15 and IOD15. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K4	OUT15	O	-	Clock output 15, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.

Table 2. Pin Descriptions – RC38412 (Cont.)

Pin Number	Pin Name	Type		Description
K5	VDDO14	Power	-	Power supply for OUT14/nOUT14 and IOD14. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K6	OUT14	O	-	Clock output 14, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
K7	VDDO13	Power	-	Power supply for OUT13/nOUT13 and IOD13. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K8	OUT13	O	-	Clock output 13, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair.
K9	VDDO11	Power	-	Power supply for OUT11/nOUT11 and IOD11. 1.8V is supported. This pin can be tied to ground to minimize power consumption if the corresponding output is unused. This pin must not be allowed to float.
K10	OUT11	O	-	Clock output 11, differential pair. LVDS, HCSL, or CML. OUTx indicates the positive pin of a differential pair.

1.5 Input Characteristics

Table 3. Input Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
C_{IN}	Input capacitance	CLKIN/nCLKIN, REF_CLK, nMR, nCS_A0, SDO_A1, GPIOn, SPI_SEL	-	4	-	pF
		SCL_SCLK, SDA_SDIO, SDO_A1[1]			10	
R_{PU}	Input pull-up resistor	nCLKIN, nMR, nCS_A0, SDO_A1, SDA_SDIO, GPIOn, SPI_SEL, SCL_SCLK	-	54	-	kΩ
R_{PD}	Input pull-down resistor	CLKIN, nCS_A0, SDO_A1, SDA_SDIO, REF_CLK, GPIOn, SCL_SCLK				

1. UM10204r7 (I2C-bus specification and user manual) states maximum capacitance for each I/O pin is 10pF

2. Specifications

2.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{DD18}	Supply Voltage with Respect to Ground	VDD_CLK, VDDXO_DCD, VDD_VCO, VDD_FAN, VDD_FOD[4:0], VDDOx	-0.5	1.89	V
V_{DD33}	Supply Voltage with Respect to Ground	VDD_DIG	-0.5	3.63	V
V_{IN}	Input Voltage	CLKINx	-0.5	V_{DD_CLK} + 0.5	V
		GPIOx used as inputs		1.89	
		REF_CLK		3.63	
		nMR, SPI_SEL, nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO		V_{DD_DIG} + 0.5	
I_{IN}	Input Current	GPIOx used as inputs	-	±25	mA
		CLKINx		±50	
		REF_CLK		±50	
		nMR, SPI_SEL, nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO		±25	
I_{OUT}	Output Current - Continuous	OUTx, nOUTx	-	30	mA
		SDO_A1, SCL_SCLK, SDA_SDIO		25	
		GPIOx used as outputs		25	
I_{OUT}	Output Current - Surge	OUTx, nOUTx	-	30	mA
		SDO_A1, SCL_SCLK, SDA_SDIO		25	
		GPIOx used as outputs		25	
T_J	Maximum Junction Temperature		-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C
-	Human Body Model (Tested per JESD22-A114 (JS-001) Classification)		-	2000	V
-	Charged Device Model (Tested per JESD22-C101 Classification)		-	500	V

2.2 Recommended Operating Conditions

Table 5. Recommended Operating Conditions [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature		-	-	125	°C
T_A	Ambient Operating Temperature		-40	-	85	°C
T_B	Board Operating Temperature		-	-	105	°C
V_{DDx}	Supply Voltage with Respect to Ground	VDDx pins with 1.8V supply [3]	1.71	1.8	1.89	V
V_{DD_DIG}	Supply Voltage with Respect to Ground	VDD_DIG with 1.8V/2.5V/3.3V supply [4]	1.71	1.8, 2.5, 3.3	3.63	V
t_{PU}	Power-up time for all VDD to reach minimum specified voltage	Power ramps must be monotonic nMR left floating	-	-	15	ms
t_{HOLD}	Minimum time to keep nMR asserted after all power supplies have reached > 90% of nominal voltage	nMR controlled externally	25	-	-	ns

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.
3. 1.8V supply is ±5%.
4. 1.8V supply is ±5%, 2.5V supply is ±5%, 3.3V supply is ±10%

2.3 Thermal Specifications

Table 6. Thermal Specifications - JEDEC 2S2P[1]

Symbol	Parameter	Condition	Typical	Unit
Θ_{JC}[2]	Junction to case	BGA-144 package	10.1	°C/W
Θ_{JB}[3]	Junction to board		5.2	
Θ_{JA0}[4]	Junction to air, still air		22.4	
Θ_{JA1}	Junction to air, 1 m/s air flow		21.8	
Θ_{JA3}	Junction to air, 3 m/s air flow		19.7	
Θ_{JA5}	Junction to air, 5 m/s air flow		18.8	
Θ_{JC}	Junction to case	BGA-100 package	10.9	°C/W
Θ_{JB}	Junction to board		5.1	
Θ_{JA0}	Junction to air, still air		23.6	
Θ_{JA1}	Junction to air, 1 m/s air flow		22.3	
Θ_{JA3}	Junction to air, 3 m/s air flow		19.9	
Θ_{JA5}	Junction to air, 5 m/s air flow		18.7	

1. See TB379.
2. For θ_{JC}, the case temperature location is taken at the package top center.
3. For θ_{JB}, the board temp is taken on the board near the edge of the package, on a copper trace at the center of one side.
4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features.

Table 7. Thermal Specifications - Renesas 10-Layer, 10” x 10”

Symbol	Parameter	Condition	Typical	Unit
Θ_{JC}[1]	Junction to case	BGA-144 package	10.1	°C/W
Θ_{JB}[2]	Junction to board		5.2	
Θ_{JA0}[3]	Junction to air, still air		14.2	
Θ_{JC}	Junction to case	BGA-100 package	10.9	°C/W
Θ_{JB}	Junction to board		5.1	
Θ_{JA0}	Junction to air, still air		15.1	

1. For θ_{JC}, the case temperature location is taken at the package top center.
2. For θ_{JB}, the board temp is taken on the board near the edge of the package, on a copper trace at the center of one side.
3. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features.

2.4 Power Supply Noise Rejection

Table 8. Power Supply Noise Rejection [1][2][3][4]

Symbol	Parameter	Condition	Typical	Unit
PSNR	Power supply rejection ratio	VDDx = 1.8V, f_{NOISE} = 10kHz	-87	dBc
PSNR	Power supply rejection ratio	VDDx = 1.8V, f_{NOISE} = 25kHz	-85	
PSNR	Power supply rejection ratio	VDDx = 1.8V, f_{NOISE} = 50kHz	-85	
PSNR	Power supply rejection ratio	VDDx = 1.8V, f_{NOISE} = 100kHz	-84	
PSNR	Power supply rejection ratio	VDDx = 1.8V, f_{NOISE} = 500kHz	-84	
PSNR	Power supply rejection ratio	VDDx = 1.8V, f_{NOISE} = 1MHz	-79	

1. The device will meet specifications after thermal equilibrium has been reached.
2. 100mV peak-to-peak sine wave applied to any VDDO, excluding VDDO of the output being measured and excluding VDD_VCO.
3. Relative to 156.25MHz carrier frequency.
4. Measured on any differential output.

2.5 APLL Phase Jitter

Table 9. APLL Phase Jitter [1][2][3][4]

Symbol	Parameter	Condition	Typical	Maximum	Unit
$t_{JIT(\Phi)}$	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) at 100MHz	Differential output, APLL steered by DPLL5, BW = 25Hz, CLKIN = 25MHz, REF_CLK = 49.152MHz, VCO = 9.8GHz [5][6]	62	75	fs RMS
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) at 245.76MHz	Differential output, APLL steered by DPLL5, BW = 25Hz, CLKIN = 25MHz, REF_CLK = 68MHz, VCO = 9.8304GHz [5][6]	50	55	
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) at 491.52MHz		45	50	
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) at 156.25MHz	Differential output, APLL steered by DPLL5, BW = 25Hz, CLKIN = 25MHz, REF_CLK = 49.152MHz, VCO = 9.375GHz [5][7]	54	60	
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) at 312.5MHz		45	55	
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) with 4MHz high-pass-filter at 312.5MHz		25	30	
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) with 4MHz high-pass-filter at 390.625MHz		26	30	
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) with 4MHz high-pass-filter at 312.5MHz	Differential output, APLL configured as a synthesizer, REF_CLK = 62.5MHz, VCO = 9.375GHz [7]	25	30	
	Random Phase Jitter for OUT[17:0], (12kHz to 20MHz) with 4MHz high-pass-filter at 390.625MHz		22	25	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 driving the REF_CLK pin.
3. Measured after the APLL has locked and settled.
4. All outputs enabled and outputting clocks with the same frequency sourced from the APLL via integer output dividers.
5. Measured after the DPLL has locked and settled using a jitter-free and wander-free reference.
6. Using A1xx with f_{VCO} range of 9.8 to 10.35 GHz.
7. Using A2xx with f_{VCO} range of 9.25 to 9.85 GHz.

2.6 FOD Phase Jitter

Table 10. FOD Phase Jitter - Synthesizer Mode [1][2][3][4]

Symbol	Parameter	Condition	Typical	Maximum	Unit
$t_{JIT(\Phi)}$	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 155.52MHz	Differential output, FOD steered by DPLL, BW = 25Hz, CLKIN = 25MHz, REF_CLK = 68MHz, VCO = 9.8304GHz [5][6]	87	175	fs RMS
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 312.5MHz		72	110	
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 161,132,812.5Hz	Differential output, FOD steered by DPLL, BW = 25Hz, CLKIN = 25MHz, REF_CLK = 49.152MHz, VCO = 9.8GHz [5][6]	112	230	
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 156.25MHz	Differential output, FOD steered by DPLL, BW = 25Hz, CLKIN = 25MHz, REF_CLK = 68MHz, VCO = 9.8GHz [5][7]	89	160	
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 312.5MHz		69	100	
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 625MHz		67	95	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 driving the REF_CLK pin.
3. Measured after the APLL has locked and settled.
4. All OUT|17:6| enabled and outputting the same frequency sourced from the same FOD, and all OUT|5:0| disabled.
5. Measured after the DPLL has locked and settled using a jitter-free and wander-free reference.
6. Using A1xx with f_{VCO} range of 9.8 to 10.35 GHz.
7. Using A2xx with f_{VCO} range of 9.25 to 9.85 GHz.

Table 11. FOD Phase Jitter - Synchronous Mode [1][2][3][4]

Symbol	Parameter	Condition	Typical	Maximum	Unit
$t_{JIT(\Phi)}$	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 155.52MHz	Differential output, FOD directly from APLL, REF_CLK = 68MHz, VCO = 9.8304GHz	84	170	fs RMS
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 122.88MHz	Differential output, FOD directly from APLL, REF_CLK = 49.152MHz, VCO = 9.8GHz	78	140	
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 156.25MHz		82	115	
	Random Phase Jitter for OUT[17:6], (12kHz to 20MHz) at 161,132,812.5Hz		109	260	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 driving the REF_CLK pin.
3. Measured after the APLL has locked and settled.
4. All OUT|17:6| enabled and outputting the same frequency sourced from the same FOD, and all OUT|5:0| disabled.

2.7 TOD and Synthesis Phase Jitter

Table 12. TOD and Synthesis Phase Jitter [1][2][3][4][5]

Symbol	Parameter	Condition	Typical	Maximum	Unit
$t_{JIT(\Phi)}$	Random Phase Jitter (12kHz to 20MHz) for OUT[17:12] at 125MHz	Differential output, APLL steered by DPLL5, BW = 25Hz, CLKIN = 25MHz, FOD0 configured as a synthesizer / DCO from REF_CLK = 68MHz, FOD0 = 500MHz, VCO = 9.8304GHz [6]	170	300	fs RMS
	Random Phase Jitter (12kHz to 20MHz) for OUT[17:12] at 250MHz	Differential output, APLL steered by DPLL5, BW = 25Hz, CLKIN = 25MHz, FOD0 configured as a synthesizer / DCO from REF_CLK = 68MHz, FOD0 = 500MHz, VCO = 9.8304GHz [6]	167		

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 driving the REF_CLK pin.
3. Measured after the APLL has locked and settled.
4. All OUT|17:12| enabled and outputting the same frequency, and all OUT|11:0| disabled.
5. Measured after DPLL5 has locked and settled using a jitter-free and wander-free reference.
6. Measured after DPLL5 has locked and settled using a jitter-free and wander-free reference.

2.8 APLL Phase Noise

Table 13. APLL Phase Noise [1][2][3][4][5]

Symbol	Parameter	Condition	Typical	Unit
$\Phi_{SSB(10)}$	Single sideband phase noise for OUT[17:0] at 10Hz offset with 245.76MHz carrier	Differential output, APLL steered by DPLL5, BW = 25Hz, CLKIN = 25MHz from Rb timebase, REF_CLK = 68MHz, VCO = 9.8304GHz	-81	dBc/Hz
$\Phi_{SSB(100)}$	Single sideband phase noise for OUT[17:0] at 100Hz offset with 245.76MHz carrier		-96	
$\Phi_{SSB(1k)}$	Single sideband phase noise for OUT[17:0] at 1kHz offset with 245.76MHz carrier		-113	
$\Phi_{SSB(10k)}$	Single sideband phase noise for OUT[17:0] at 10kHz offset with 245.76MHz carrier		-140	
$\Phi_{SSB(100k)}$	Single sideband phase noise for OUT[17:0] at 100kHz offset with 245.76MHz carrier		-146	
$\Phi_{SSB(800k)}$	Single sideband phase noise for OUT[17:0] at 800kHz offset with 245.76MHz carrier		-153	
$\Phi_{SSB(1M)}$	Single sideband phase noise for OUT[17:0] at 1MHz offset with 245.76MHz carrier		-155	
$\Phi_{SSB(1.72M)}$	Single sideband phase noise for OUT[17:0] at 1.72MHz offset with 245.76MHz carrier		-158	
$\Phi_{SSB(10M)}$	Single sideband phase noise for OUT[17:0] at 10MHz offset with 245.76MHz carrier		-163	
$\Phi_{SSB(30M)}$	Single sideband phase noise for OUT[17:0] at 30MHz offset with 245.76MHz carrier		-164	

Table 13. APLL Phase Noise [1][2][3][4][5] (Cont.)

Symbol	Parameter	Condition	Typical	Unit
$\Phi_{SSB(10)}$	Single sideband phase noise for OUT[17:0] at 10Hz offset with 491.52MHz carrier	Differential output, APLL steered by DPLL5, BW = 25Hz, CLKIN = 25MHz from Rb timebase, REF_CLK = 68MHz, VCO = 9.8304GHz	-75	dBc/Hz
$\Phi_{SSB(100)}$	Single sideband phase noise for OUT[17:0] at 100Hz offset with 491.52MHz carrier		-90	
$\Phi_{SSB(1k)}$	Single sideband phase noise for OUT[17:0] at 1kHz offset with 491.52MHz carrier		-106	
$\Phi_{SSB(10k)}$	Single sideband phase noise for OUT[17:0] at 10kHz offset with 491.52MHz carrier		-135	
$\Phi_{SSB(100k)}$	Single sideband phase noise for OUT[17:0] at 100kHz offset with 491.52MHz carrier		-140	
$\Phi_{SSB(800k)}$	Single sideband phase noise for OUT[17:0] at 800kHz offset with 491.52MHz carrier		-148	
$\Phi_{SSB(1M)}$	Single sideband phase noise for OUT[17:0] at 1MHz offset with 491.52MHz carrier		-149	
$\Phi_{SSB(1.72M)}$	Single sideband phase noise for OUT[17:0] at 1.72MHz offset with 491.52MHz carrier		-154	
$\Phi_{SSB(10M)}$	Single sideband phase noise for OUT[17:0] at 10MHz offset with 491.52MHz carrier		-160	
$\Phi_{SSB(30M)}$	Single sideband phase noise for OUT[17:0] at 30MHz offset with 491.52MHz carrier		-161	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 driving the REF_CLK pin.
3. Measured after the DPLL and APLL have locked and settled.
4. All OUT|17:0| enabled and outputting the same frequency.
5. Measured after the DPLL has locked and settled using a jitter-free and wander-free reference.

2.9 Peak APLL Spurious Power

Table 14. Peak APLL Spurious Power [1][2][3][4][5][6]

Symbol	Parameter	Condition	Typical	Unit
Φ_{SPUR}	Peak Spurious Power 100Hz to 100MHz for OUT[17:0] with 245.76MHz carrier	Differential output, APLL steered by DPLL5, DPLL BW = 25Hz, CLKIN = 25MHz, REF_CLK = 68MHz, VCO = 9.8304GHz	-98	dBc
	Peak Spurious Power 100Hz to 100MHz for OUT[17:0] with 491.52MHz carrier		-96	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 driving the REF_CLK pin.
3. Measured after the APLL has locked and settled.
4. Measured after the DPLL has locked and settled using a jitter-free and wander-free reference.
5. All OUT|17:0| enabled and outputting the same frequency.
6. All FODs disabled.

2.10 APLL Frequency Reference AC/DC Electrical Characteristics

Table 15. APLL Frequency AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{VCO}	Analog PLL VCO Operating Frequency	A1xx	9.8	10	10.35	GHz
		A2xx	9.25	9.8304	9.85	
F_{TOL}	Frequency Tolerance [1][2][3][4]	-40°C to 85°C	-450	-	450	PPM

1. F_TOL refers to the frequency accuracy of the APLL frequency reference, either a crystal connected between XIN and XOUT, or an oscillator connected to the REF_CLK pin. The APLL can reliably lock to a reference that meets the F_TOL limits.
2. Inclusive of initial tolerance at 25°C, temperature stability, and aging.
3. The APLL frequency steering range (±F_STEER) available for a DPLL or DCO to digitally steer the APLL is determined by the following expression: F_STEER = |F_TOL| - |F_ACC|; where F_ACC is the frequency accuracy of the APLL frequency reference. For example, if the frequency accuracy of the APLL frequency reference is ±100PPM. then the APLL frequency steering range will be ±350PPM.
4. The frequency accuracy of the APLL frequency reference should be chosen to meet the free-running frequency requirements of the application, and to allow sufficient frequency steering range for a DPLL or DCO to lock the APLL to its reference and to track reference noise. For more information, see APLL Frequency Reference.

2.11 APLL Crystal (XIN) AC/DC Characteristics

Table 16. APLL Crystal Input (XIN) AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
-	Mode of oscillation		Fundamental			
f_{IN}	Input Frequency	With a quartz crystal resonator between XIN and XOUT	25	-	80	MHz
C_T	Internal crystal oscillator tuning capacitance [1]	xo_fixedcap_on = 0x0, xobuf_digcap_x1 = 0x0, xobuf_digcap_x2 = 0x0	-	7	-	pF
		xo_fixedcap_on = 0x0, xobuf_digcap_x1 = 0xF, xobuf_digcap_x2 = 0xF		10		
		xo_fixedcap_on = 0x1, xobuf_digcap_x1 = 0x0, xobuf_digcap_x2 = 0x0		11		
		xo_fixedcap_on = 0x1, xobuf_digcap_x1 = 0xF, xobuf_digcap_x2 = 0xF		15		
ESR	Equivalent Series Resistance	8pF ≤ CL ≤ 10pF	-	-	50	Ω
C_O	Shunt Capacitance		-	-	4	pF
C_L	Load Capacitance		-	8	10	pF
Drive	Drive Level [1]	CL = 8pF	-	246	-	µW
		CL = 10pF		342		
F_{ACC}	Frequency Accuracy [2]		Per Application			

1. Refers to power in the crystal (equivalent series resistance).
2. See F_TOL in APLL AC/DC Characteristics

2.12 REF_CLK AC/DC Characteristics

Table 17. APLL Reference Clock (REF_CLK) AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
F_{IN}	Input frequency	Single-ended input	25	-	100	MHz
V_{SR}	Input voltage slew rate for REF_CLK pin		0.7	-	-	V/ns
V_{IH}	Input high voltage		1.0	-	3.6	V
V_{IL}	Input low voltage		-0.3	-	0.3	V
V_{BIAS}	Bias point for the REF_CLK pin		-	0.65	-	V
I_{IH}	Input high current	VIN = V_IH (max)	-	-	23.5	µA
I_{IL}	Input low current	VIN = V_IL	-0.1	-	-	µA
$\Phi_{SSB(10)}$	Single sideband phase noise for REF_CLK at 10Hz offset with 68MHz carrier		-	-125	-	dBc/Hz
$\Phi_{SSB(100)}$	Single sideband phase noise for REF_CLK at 100Hz offset with 68MHz carrier			-142		
$\Phi_{SSB(1k)}$	Single sideband phase noise for REF_CLK at 1kHz offset with 68MHz carrier			-162		
$\Phi_{SSB(10k)}$	Single sideband phase noise for REF_CLK at 10kHz offset with 68MHz carrier			-168		
$\Phi_{SSB(100k)}$	Single sideband phase noise for REF_CLK at 100kHz offset with 68MHz carrier			-165		
$\Phi_{SSB(1M)}$	Single sideband phase noise for REF_CLK at 1MHz offset with 68MHz carrier			-171		
$\Phi_{SSB(10M+)}$	Single sideband phase noise for REF_CLK at 10M+Hz offset with 68MHz carrier			-177		

2.13 Clock Input (CLKIN/nCLKIN) AC/DC Characteristics

Table 18. Clock Input (CLKIN/nCLKIN) AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IPP}	Differential input peak-to-peak voltage [1]		0.15	-	1.2	V
V_{CMR}	Differential input common mode voltage [2]	PMOS buffer (HCSL) input	V_{IPP} / 2	0.35	V_{DD_CLK} - 1.2	V
		NMOS buffer (LVDS) input	-	-	V_{DD_CLK} - V_{IPP}	
F_{IN}	Input frequency	Differential input	-	-	1000	MHz
		Single-ended input			150	
F_{PD}	DPLL phase detector frequency [3]		0.001	-	60	MHz
I_{IH}	Differential input high current, CLKIN	VIN = VDD_CLK (max)	-	-	23.1	µA
	Differential input high current, nCLKIN				-12	
I_{IL}	Differential input low current, CLKIN	VIN = 0V	-0.1	-	-	µA
	Differential input low current, nCLKIN		-36.3			
V_{IH}	Input high voltage	VDDREF = VDD_CLK (max)	0.65 x V_{DD}	-	V_{DD} + 0.3	V

Table 18. Clock Input (CLKIN/nCLKIN) AC/DC Characteristics (Cont.)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IL}	Input low voltage	VDDREF = VDD_CLK (max)	-0.3	-	0.35 x V_{DDOx}	V
I_{IH}	Input high current	VIN = VDD_CLK (max)	-	-	150	µA
I_{IL}	Input low current	VIN = 0V	-5	-	-	µA
PW	Pulse width	Differential input	0.4	-	-	ns
		Single ended input	2			

1. Single-ended value.
2. Common mode is defined as the cross-point.
3. Internal input dividers may be used to reduce the CLKIN/nCLKIN frequency to be within the valid range.

2.14 Time Sync TDC Characteristics

Table 19. Time Sync TDC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
	Precision of the TDC		-	-	100	ps
F_{TDC}	TDC frequency [1]		1e-06	-	60	MHz
PW	Pulse width		10	-	-	ns
TDCMA	TDC Measurement Accuracy3]	REF1 = 1MHz, REF2 = 1MHz, undivided. avg_bw_shift = 6 for 63kHz decimator filter averaging.	-	0	18	ps

1. Internal input dividers must be bypassed.

2.15 Output Frequencies and Start-Up Time

Table 20. Output Frequencies and Start-Up Time

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency for Clocks OUT[11:0] sourced from APLL	CML	DC	-	2500	MHz
	Output Frequency for Clocks OUT[11:6] sourced from FOD				1000	
	Output Frequency for Clocks OUT[17:0] sourced from APLL	LVDS or HCSL			1250	
	Output Frequency for Clocks OUT[17:6] sourced from FOD				1000	
	Output Frequency for Clocks OUT[17:12] sourced from FOD	LVCMOS			250	
Δf_{OUT}	Output frequency tuning resolution	Fractional Output Divider	-	-	0.1	ppt
$t_{START-UP}$	Start-up time	Synthesizer mode [1][2]	-	6	10	ms
t_{WAIT}	Wait time after nMR de-assertion before serial port can be accessed.[3]	Load configuration from OTP	-	7	10	ms
		Load configuration from EEPROM		160	-	
		EEPROM, CRC failure[4]		580		

1. Measured from when all power supplies have reached > 90% of nominal voltage and nMR is deasserted to the first stable clock edge on the output. A stable clock is defined as one generated from a locked PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected. Includes time needed to load a configuration from internal OTP.
2. Using internal OTP. Start-up time will depend on the actual configuration used. For more information, please contact Renesas Technical Support.
3. Measured from when a GPIO configured for device_ready status is asserted.
4. Dependent on eeprom_retry_count. (default 4x).

2.16 Phase and Frequency Uncertainty

Table 21. Phase and Frequency Uncertainty [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Δt_{HS}	Output phase change using hitless reference switching		-	-	120	ps
Δf_{HO}	Initial frequency offset entering holdover	Using holdover filter with 1mHz bandwidth and allowing settling time of 1 hour	-	-	0.715	ppt
Δt_{HO}	Initial phase shift entering holdover	Using LOS monitor to disqualify	-	-	25	ps

1. The device will meet specifications after thermal equilibrium has been reached.
2. Measured after the DPLL has locked and settled using a jitter-free and wander-free reference

2.17 Output-to-Output Skew and Input-to-Output Delay

Table 22. Output-to-Output Skew and Input-to-Output Delay [1][2]

Symbol	Parameter	Condition	Maximum	Unit
t_{SK}	Output-to-output skew differential outputs	Any two outputs within the same output bank, Bank 1 [3]	35	ps
		Any two outputs within the same output bank, Bank 2 [3]	40	
		Any two outputs within the same output bank, Bank 3 [3]	40	
		Any two outputs within the same output bank, Bank 4 [3]	30	
		Any two outputs across all output banks from the same APLL or FOD source [3][4]	250	
		Any two outputs across bank 3 and 4 from the same APLL or FOD source [3][4]	115	
	Output-to-output skew LVCMOS outputs	Any two outputs within the same output bank [3][4]	70	
		Any two outputs across all output banks from the same APLL or FOD source [3][4]	160	
		Any two outputs across bank 3 and 4 from the same APLL or FOD source [3][4]	160	
t_{SK_SR}	Output-to-output skew between SYSREF and Device Clock incident edge	Differential outputs with zero phase compensation. Excluding bank 4.	50	ps
Δt_{SK}	Output-to-output skew temperature variation [3][5]	Single device, at a fixed voltage, over temperature	75	ps/°C
		Single device, over process, temperature and voltage [3][5]	80	
t_{PD}	Input-to-output delay	DPLL path to any output [5]	1	ps
Δt_{PD}	Input-to-output delay variation	For device clocks on OUT and sourced from the DPLL5/APLL, over temperature [5][6]	1	ps/°C

1. Electrical parameters are confirmed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Bank 1 refers to OUT|5:0|, Bank 2 refers to OUT|11:6|, Bank 3 refers to OUT|15:12| and Bank 4 refers to OUT|17:16|.
3. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
4. This parameter is defined in accordance with JEDEC Standard 65.
5. This parameter is measured across the full operating temperature range. The difference between the largest and smallest values is the variation.
6. Defined as the time between to output rising edge and the input rising edge that caused it.

2.18 LVCMOS Output AC/DC Characteristics

Table 23. LVCMOS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output high voltage	IOL = -2mA	V_{DDO} - 0.45	-	-	V
V_{OL}	Output low voltage [2]	IOL = 2mA	-		0.45	
V_{OH}	Output high voltage [2]	IOH = -100µA	V_{DDO} - 0.2		-	
V_{OL}	Output low voltage [2]	IOL = 100µA	-		0.2	
I_{OZ}	Output leakage current	Outputs tri-stated	-0.3	-	0.5	µA
Z_{OUTDC}	DC output impedance	At 25°C	-	25	-	Ω
Z_{OUT}	LVCMOS Output Impedance		-	30/60	-	Ω
$t_{R/F}$	Rise/Fall time, 20% to 80% of swing	out_cmos_zout = 0x0 (25 ohm)	60	210	295	ps
		out_cmos_zout = 0x1 (50 ohm)	125	225	245	
t_{DC}	Output duty cycle	From APLL, any divide ratio	47	50	51	%
		From FOD, any divide ratio	47		51	

1. Measured with outputs terminated with 50Ω to VDDO/2.
2. These values are compliant with JESD8-7A.

2.19 LVDS Output AC/DC Characteristics

Table 24. LVDS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OD}[2]	Output voltage swing [3][4]	out_boost = 0x0	330	390	440	mV
		out_boost = 0x1/0x2	390	450	510	
		out_boost = 0x3	420	495	560	
V_{OS}	Offset voltage [4]	out_boost = 0x0	1.15	1.2	1.25	
		out_boost = 0x1/0x2	1.05	1.15	1.23	
		out_boost = 0x3	0.96	1.12	1.22	
ΔV_{OS}	Change in V_{OS} between complementary output states [4]	out_boost = any	-	-	50	mV
t_R	Rise time, 20% to 80% of swing	out_boost = any	82	-	193	ps
t_F	Fall time, 20% to 80% of swing		198		332	
t_{DC}	Output duty cycle	From APLL, even IOD divide	49	50	51	%
		From APLL, odd IOD divide ≥ 3	49		51	
		From APLL with IOD divide = 1	47		54	
		From FOD, even IOD divide	49		51	
		From FOD, odd IOD divide ≥ 3	49		51	
		From FOD with IOD divide = 1	47		54	

1. Terminated with 100Ω across OUTx and nOUTx, out_pull_down = 0x0, out_pull_up = 0x0.
2. V_{OD} corresponds to the differential output voltage (V_T) defined in TIA/EIA-644-A.
3. Single-ended measurement.
4. Tested at 10MHz.

2.20 HCSL Output AC/DC Characteristics – Externally Terminated

Table 25. HCSL Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{HIGH}	Output high voltage	out_boost = any	-	-	1200	V
V_{LOW}	Output low voltage	out_boost = any	-65	-	-	
EDGERATE	Output edge rate	out_boost = any	0.5	-	4.6	V/ns
V_{OVS}	Output voltage swing [2][3]	out_boost = 0x0	685	800	880	mV
		out_boost = 0x1/0x2	800	945	1075	
		out_boost = 0x3	790	1020	1200	
ΔV_{CROSS}	Variation of V_{CROSS} [4] over all rising clock edges [3]	out_boost = any	-	-	100	mV
$t_{R/F}$	Rise/Fall time, 20% to 80% of swing	out_hcsl_fast_edge = 0x0, out_boost = Any	110	-	315	ps
		out_hcsl_fast_edge = 0x1, out_boost = Any	90	-	260	
t_{DC}	Output duty cycle	From APLL, even IOD divide	49	50	51	%
		From APLL, odd IOD divide ≥ 3	49		51	
		From APLL with IOD divide = 1	47		54	
		From FOD, even IOD divide	49		51	
		From FOD, odd IOD divide ≥ 3	49		51	
		From FOD with IOD divide = 1	47		54	

1. Terminated with 50Ω to ground on each of OUTx and nOUTx, out_pull_down = 0x0, out_pull_up = 0x0.
2. Single-ended measurement.
3. Tested at 10MHz.
4. Nominal crossing point voltage, V_{CROSS},is approximately V_{OVS}/2.

2.21 HCSL Output AC/DC Characteristics – Internally Terminated

Table 26. HCSL Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{HIGH}	Output high voltage	out_boost = any	-	-	600	V
V_{LOW}	Output low voltage	out_boost = any	-10	-	-	
EDGERATE	Output edge rate	out_boost = any	1.2	-	5.4	V/ns
V_{OVS}	Output voltage swing [2][3]	out_boost = 0x0	345	400	425	mV
		out_boost = 0x1/0x2	415	475	515	
		out_boost = 0x3	460	545	605	
ΔV_{CROSS}	Variation of V_{CROSS} [4] over all rising clock edges [3]	out_boost = any	-	-	100	mV
$t_{R/F}$	Rise/Fall time, 20% to 80% of swing	out_hcsl_fast_edge = 0x0, out_boost = Any	45	-	125	ps
		out_hcsl_fast_edge = 0x1, out_boost = Any	40	-	115	
t_{DC}	Output duty cycle	From APLL, even IOD divide	49	50	51	%
		From APLL, odd IOD divide ≥ 3	49		51	
		From APLL with IOD divide = 1	47		54	
		From FOD, even IOD divide	49		51	
		From FOD, odd IOD divide ≥ 3	49		51	
		From FOD with IOD divide = 1	47		54	

1. Internally terminated with 50Ω to ground on each of OUTx and nOUTx, out_pull_down = 0x1, out_pull_up = 0x0.
2. Single-ended measurement.
3. Tested at 10MHz.
4. Nominal crossing point voltage, V_{CROSS},is approximately V_{OVS}/2.

2.22 CML Output AC/DC Characteristics – Externally Terminated

Table 27. CML Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{CM}	Output common-mode voltage		-	V_{DD} - 435	-	mV
V_{OD}	Differential output voltage[2][3]	out_boost = 0x0	700	800	870	
		out_boost = 0x1/0x2	785	900	1005	
		out_boost = 0x3	825	950	1095	
$t_{R/F}$	Rise/Fall time, 20% to 80% of swing	out_boost = Any	202	235	277	ps
t_{DC}	Output duty cycle	From APLL, even IOD divide	49	50	51	%
		From APLL, odd IOD divide ≥ 3	49		51	
		From APLL with IOD divide = 1	43		53	
		From FOD, even IOD divide	49		51	
		From FOD, odd IOD divide ≥ 3	49		51	
		From FOD with IOD divide = 1	43		53	

1. Terminated with 50Ω to VDDOx on each of OUTx and nOUTx, out_pull_down = 0x0, out_pull_up = 0x0.
2. Single-ended measurement.
3. Tested at 10MHz.

2.23 CML Output AC/DC Characteristics – Internally Terminated

Table 28. CML Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{CM}	Output common-mode voltage		-	V_{DD} - 235	-	mV
V_{OVS}	Differential output voltage[2][3]	out_boost = 0x0	345	390	425	mV
		out_boost = 0x1/0x2	400	450	495	mV
		out_boost = 0x3	425	485	545	mV
$t_{R/F}$	Rise/Fall time, 20% to 80% of swing	out_boost = Any	55	75	110	ps
t_{DC}	Output duty cycle	From APLL, even IOD divide	49	50	51	%
		From APLL, odd IOD divide ≥ 3	49		51	
		From APLL with IOD divide = 1	44		53	
		From FOD, even IOD divide	49		51	
		From FOD, odd IOD divide ≥ 3	49		51	
		From FOD with IOD divide = 1	44		53	

1. Internally terminated with 50Ω to VDDOx on each of OUTx and nOUTx, out_pull_down = 0x0, out_pull_up = 0x1.
2. Single-ended measurement.
3. Tested at 10MHz.

2.24 SYSREF Output AC/DC Characteristics

Table 29. SYSREF Output AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency for SYSREF [1]		0.001	-	62.5	MHz
Φ_{REF}	SYSREF delay circuit range		0	-	3*sysref_period	ns
t_{PD}	SYSREF propagation delay	SYSREF input trigger to output (Φ_REF = 0)	-	-	sysref_period	ns

1. Must be an integer divisor of the associated device clock frequency.

2.25 Power Supply Current

Table 30. Power Supply Current [1]

Symbol	Parameter	Condition	Typical	Maximum	Unit
I_{DD_CLK}	Supply current for VDD_CLK	Per single-ended input	25	-	mA
I_{DD_CLK}	Supply current for VDD_CLK	Per differential input	33	-	mA
I_{DDXO_DCD}	Supply current for VDDXO_DCO	VDDXO_DCD = 1.89V	42	-	mA
I_{DD_VCO}	Supply current for VDD_VCO	VDD_VCO = 1.89V	163	-	mA
I_{DD_DIG}	Supply current for VDD_DIG	VDD_DIG = 1.89V, All FODs off (IDD_FODDIGBASE)	43	-	mA
I_{DD_DIG}	Supply current for VDD_DIG	VDD_DIG = 1.89V, Current adder for one FOD at 100MHz (IDD_PERFODDIG)	62	-	mA
I_{DD_DIG}	Supply current for VDD_DIG	VDD_DIG = 1.89V, Current adder for one FOD per 10MHz over 100MHz (IDD_FODDIGPERMHZ)	66	-	mA
I_{DD_FAN}	Supply current for VDD_FAN	VDD_FAN = 1.89V	160	-	mA
I_{DD_FODx}	Supply current for VDD_FODx [2]	VDD_FODx = 1.89V, Current with the FOD off (IDD_FODBASE)	4	-	mA
I_{DD_FODx}	Supply current for VDD_FODx [2]	VDD_FODx = 1.89V, Current adder for the FOD at 100MHz (IDD_PERFOD)	33	-	mA
I_{DD_FODx}	Supply current for VDD_FODx [2]	VDD_FODx = 1.89V, Current adder for the FOD per 10MHz over 100MHz (IDD_FODPERMHZ)	37	-	mA
I_{DDOx}	Supply current for VDDOx [2]	LVCMOS, one output	14	-	mA
I_{DDOx}	Supply current for VDDOx [2]	LVCMOS, two outputs	27	-	mA
I_{DDOx}	Supply current for VDDOx [2]	LVDS, out_boost = any	10	-	mA
I_{DDOx}	Supply current for VDDOx [2]	HCSL, out_boost = any, externally terminated	12	-	mA
I_{DDOx}	Supply current for VDDOx [2]	HCSL, internally terminated	28/31/33	-	mA
I_{DDOx}	Supply current for VDDOx [2]	CML, out_boost = any, externally terminated	10	-	mA
I_{DDOx}	Supply current for VDDOx [2]	CML, internally terminated	26/28/29	-	mA
I_{DDOx}	Supply current for VDDOx [2]	Output disabled	3	4	mA

1. Internal dynamic switching current at maximum f_{OUT} is included, unless otherwise noted.
2. Measured with outputs unloaded.

2.26 GPIO and nMR DC Electrical Characteristics

Table 31. GPIO, Serial Port, and nMR Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage [2][3][4]	GPIO[4:0], nMR	0.65 x V_{DD}	-	V_{DD} + 0.3	V
V_{IH}	Input low voltage [2]		-0.3		0.4 x V_{DD}	
V_{OH}	Output high voltage [2][3]	GPIO[4:0], IOH = -2mA	V_{DDOx} - 0.45		V_{DDOx} + 0.3	
V_{OL}	Output low voltage [2]	GPIO[4:0], IOL = 2mA	-		0.45	
V_{OH}	Output high voltage [2][3]	GPIO[4:0], IOH = -100µA	V_{DDOx} - 0.2		V_{DDOx} + 0.3	
V_{OL}	Output low voltage [2]	GPIO[4:0], IOL = 100µA	-		0.2	
V_{OL}	Output low voltage [2]	GPIO[4:0] open-drain, IOL = 4mA	-0.5		0.3 x V_{DD}	

1. Input specifications refer to signals GPIO, when acting as inputs. Output specifications refer to signals GPIO, when acting as outputs.
2. These values are compliant with JESD8-7A.
3. VDDOx refers to the supply powering the GPIO. For VDD pin mapping, see GPIO VDD Pin Assignments.
4. VDD refers to the supply powering the GPIO, Serial Port, and nMR.

2.27 I2C Bus Target Timing Diagram

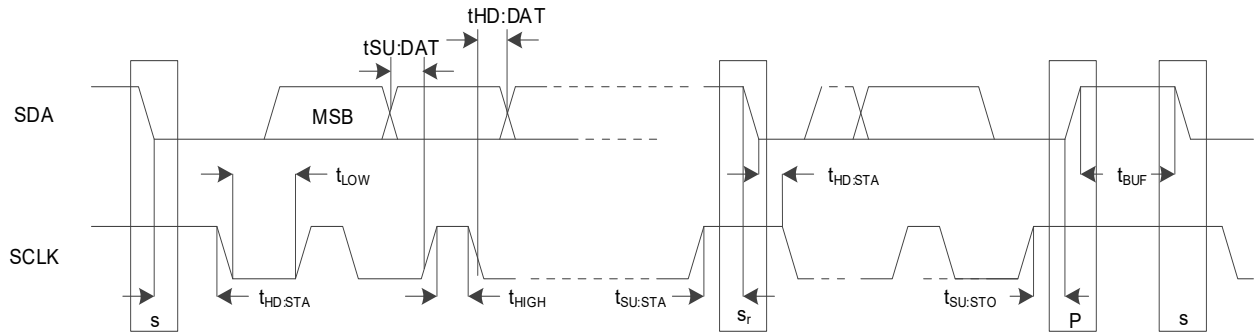


Figure 5. I2C Bus Target Timing Diagram

2.28 I2C Bus Target Timing

Table 32. I2C Bus Timing

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCL}	SCL clock frequency		10	1000	kHz
$t_{HD;STA}$	Hold time after (REPEATED) START Condition		0.26	-	µs
t_{LOW}	Clock low period		0.5	-	
t_{HIGH}	Clock high period		0.26	-	
$t_{SU;STA}$	REPEATED START Condition setup time		0.26	-	
$t_{HD;DAT}$	Data hold time [1]		0	-	
$t_{SU;DAT}$	Data setup time		0.05	-	
$t_{SU;STO}$	STOP condition setup time		0.26	-	
t_{BUF}	Bus free time between STOP and START Condition		0.5	-	
$t_{VD;DAT}$	Data valid time [2]		-	0.45	
$t_{VD;ACK}$	Data valid acknowledge time [3]		-	0.45	

1. t_HD:DAT is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
2. Time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
3. Time for Acknowledgment signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

2.29 I2C Bus AC/DC Electrical Characteristics

Table 33. I2C Bus AC/DC Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{IL}	Low-level input voltage for SCL_SCLK and SDA_nCS		-0.5	0.3 x V_{DD_DIG}	V
V_{IH}	High-level input voltage for SCL_SCLK and SDA_nCS		0.6 x V_{DD_DIG}	-	
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.05 x V_{DD_DIG}	-	
V_{OL}	Low-level output voltage for SCL_SCLK and SDA_nCS	IOL = 4mA	-	0.4	
t_{SPIKE}	Noise spike suppression time [2]	i2c_spike_fltr = 0x3	-	50	ns
I_{IN}	Input leakage current per pin [3]		-	2	µA

1. VOH is governed by the VPUP, the voltage rail to which the pull-up resistors are connected.
2. Device rejects noise spikes of a duration up to the maximum specified value.
3. See CMOS GPIO, Serial Port, and nMR Common Electrical Characteristics in Table 25.

2.30 SPI Target Timing Diagrams

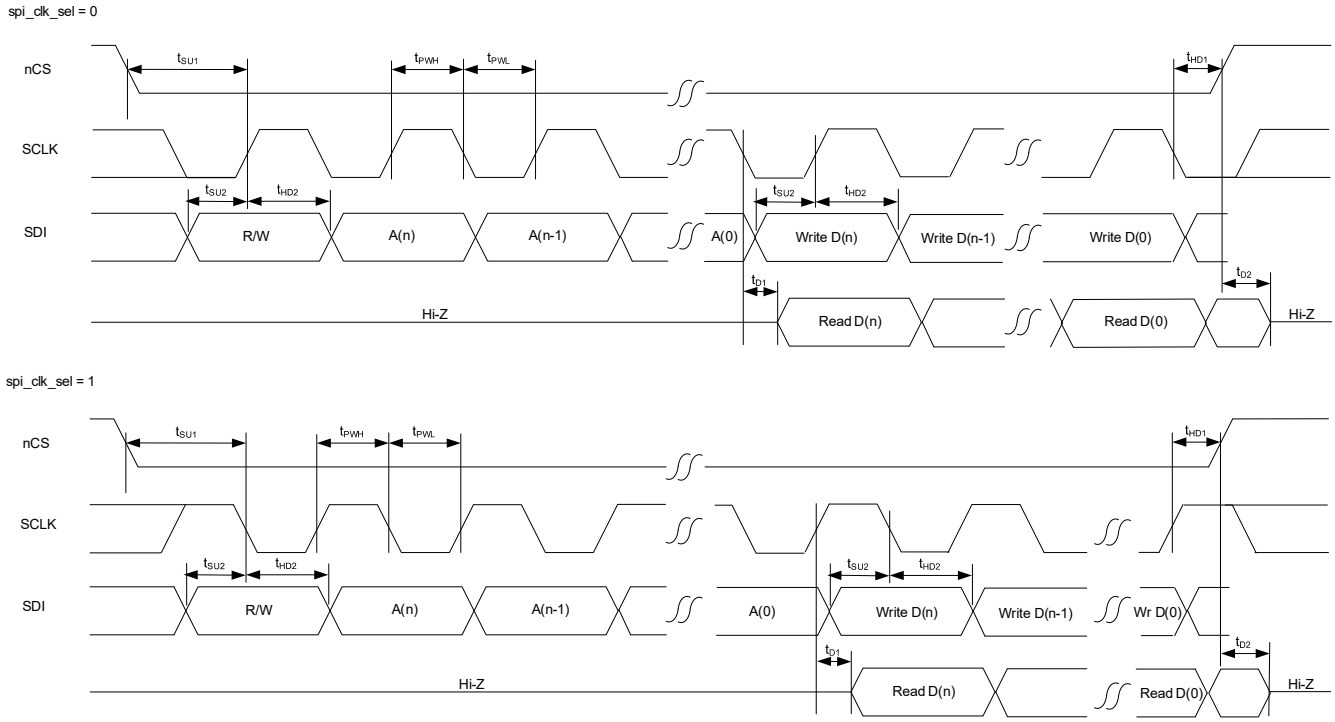


Figure 6. SPI Timing Diagrams

2.31 SPI Target Timing

Table 34. SPI Target Timing

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{MAX}	Maximum operating frequency		0.1	20 (read) 50 (write)	MHz
t_{PWH}	SCLK pulse width high		14	-	ns
t_{PWL}	SCLK pulse width low		14	-	
t_{SU1}	nCS setup time to SCLK rising or falling edge		10	-	
t_{HD1}	nCS hold time from SCLK rising or falling edge		2	-	
t_{SU2}	SDIO setup time to SCLK rising or falling edge		4	-	
t_{HD2}	SDIO hold time from SCLK rising or falling edge		3	-	
t_{D1}	Read data valid time from SCLK rising or falling edge		4.7	7.4	
t_{D2}	SDIO read data Hi-Z time from CS high [1]		-	14.5	

1. This is the time until the device releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

2.32 Temperature Sensor Characteristics

Table 35. Temperature Sensor Characteristics (T_J = -10 °C to +150 °C, unless otherwise specified) [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_{ACC}	Temperature sensor accuracy	Referenced to ideal transfer, normalized at +90 °C. Includes device-to-device variation and quantization error (±1 LSB).	-2.5	-	2.5	°C
T_{RES}	Temperature measurement resolution [2][3]	LSB size of reported temperature code.	-	2.5	-	°C
T_{SLOPE}	Temperature transfer slope [4]	Ideal conversion gain	-	2.5	-	°C/LSB
T_{OFF}	Temperature offset error	Relative to ideal transfer characteristic, referenced at > +30 °C	-	-	±2.5	°C

1. The on-chip temperature sensor reports die temperature, not ambient temperature.
2. Temperature is derived from a 6-bit SAR ADC output (ts_adc_dac_val_sts).
3. See Programming Guide for conversion transfer function.
4. Measurement step size is fixed at 2.5°C; no interpolation is performed between codes.

3. Functional Description

3.1 Overview

The RC38616/RC38412 is an ultra-low phase noise radio synchronizer, multi-frequency clock synthesizer, and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with ultra-low, in-band phase noise and spurious for 4G and 5G RF transceivers and with jitter below 25fs-rms for 112Gbps and 224Gbps SerDes.

The device has up to six independent time domains, each with its own digital PLL / digitally controlled oscillator (DPLL/DCO). An ultra-low phase noise analog PLL (APLL) is the clock synthesizer for one time domain, and fractional output dividers (FOD) are the synthesizers for the other five time domains. See Figure 2 for a block diagram of the device.

The device supports up to 11 clock inputs. CLKIN[3:0] are differential clock inputs that can each be configured as two single-ended clock inputs for up to 8 clock inputs (CLKIN[7:0]). CLKIN[9:8] use bi-directional pairs of pins, each bi-directional pair be configured as a differential clock input or as a differential clock output. The positive leg of each bi-directional pair can be configured as a single ended clock input. CLKIN[10] is a single-ended clock input. The differential clock inputs can operate at frequencies up to 1GHz, and the single-ended clock inputs can operate at frequencies up to 250MHz.

The RC38616 provides up to 18 differential clock outputs. OUT[11:0] can be configured as LVDS, HCSL (AC-LVPECL), or CML outputs. OUT[15:12] can be configured as LVDS or HCSL (AC-LVPECL) outputs, or they can each be configured as two LVCMOS outputs. When OUT[17:16] are used as outputs, they can be configured as LVDS or HCSL (AC-LVPECL) outputs, or they can each be configured as two LVCMOS outputs. The LVDS and HCSL (AC-LVPECL) outputs can operate at frequencies up to 1GHz, the CML outputs can operate at frequencies up to 2.5GHz, and the LVCMOS outputs can operate at frequencies up to 250MHz.

3.2 APLL Frequency Reference

The RC38616/RC38412 requires an analog PLL (APLL) frequency reference. The APLL frequency reference must support the phase noise, frequency accuracy, and frequency stability requirements of the intended application.

The APLL frequency reference can be implemented using an external crystal resonator connected between the XIN and XOUT pins and the device oscillator circuitry. Alternatively, the APLL frequency reference can be an external oscillator connected to the REF pin.

If a crystal resonator is used for the APLL frequency reference, the resonant frequency must be in the range 25MHz to 80MHz. If an external oscillator is used, it must provide a low-phase noise clock with frequency in the range 25MHz to 100MHz. For APLL frequency reference requirements, see APLL Frequency Reference AC/DC Electrical Characteristics.

For all applications, the phase noise of the APLL frequency reference, after filtering by the APLL, is the minimum phase noise that will appear on all clocks output by the device.

The accuracy of the APLL frequency reference determines the frequency accuracy of the reference monitors and free-running clocks. In these cases, the stability of the frequency reference determines the holdover stability of the DPLL and it affects the lowest filtering bandwidth the DPLL can support.

The accuracy of the APLL frequency reference determines the frequency accuracy of the free-running clocks. In these cases, the stability of the frequency reference determines the stability of the DCO clocks when a source of synchronization is not available, and it affects the lowest filtering bandwidth that a filtering algorithm can support.

The accuracy of the frequency reference should be chosen to meet the free-running frequency accuracy requirements of the application (see Table 36 for examples) and to allow sufficient APLL frequency steering range for DPLL[5]/DCO[5] to lock the APLL to its reference and to track reference noise.

For applications where a System DPLL is used, the frequency stability and accuracy of the System DPLL reference can override the frequency stability and accuracy of the APLL frequency reference for DPLL/DCOs connected to the System DPLL by the Combo Bus.

The available APLL frequency steering range ($\pm F_{STEER}$) is determined by the following expression: $F_{STEER} = |F_{TOL}| - |F_{ACC}|$; where F_{ACC} is the accuracy of the APLL frequency reference. See APLL Frequency Reference AC/DC Electrical Characteristics for the value of F_{TOL} and for additional information.

Table 36. Recommended Free-Running Frequency Accuracy by Application

Application	Recommended Free-Running Frequency Accuracy (PPM)
PCIe Free-running clock synthesizer	±100
Most Ethernet types Jitter attenuator or free-running clock synthesizer	±100
800GBASE-xR8, 10GBASE-T Jitter attenuator or free-running clock synthesizer	±50
100GBASE-ZR, 10GBASE-W Jitter attenuator or free-running clock synthesizer	±20
ITU-T G.8262, G.8262.1 SEC, EEC, OEC, eSEC, eEEC, eOEC	±4.6
ITU-T G.8273.2, G.8273.3 T-BC, T-TSC, T-BC-A, T-TSC-A, T-BC-P, T-TSC-P	±4.6

3.3 Analog PLL

The internal APLL has a bandwidth of approximately 1MHz, it locks to the APLL frequency reference, and synthesizes an ultra-low phase noise clock of virtually any frequency from 9.80GHz to 10.35GHz, or from 9.25GHz to 9.85GHz, depending on the version of the device. The APLL inherits the fractional frequency offset (FFO) of the APLL frequency reference and this determines the free-run frequency accuracy of the device. The APLL is the primary synthesizer for DPLL5 and its FFO can be steered by DPLL5.

The APLL output clock is pre-divided by 2, 3, 5, or 7 and is available to the integer output dividers (IOD).

For the RC38412, the pre-divided APLL clock is available directly to IOD[5:4][2:1]; it is also available via cross-connect to IOD[11:10][8:7] and IOD[16:13]. The undivided APLL clock is supplied to FOD[3][2][0].

For the RC38616, the pre-divided APLL clock is available directly to IOD[5:0]; it is also available via cross-connect to IOD[11:6] and IOD[17:12]. The undivided APLL clock is supplied to FOD[4:0].

3.4 Integer Output Dividers

Each IOD divides its input clock by a programmable 23-bit integer value.

3.5 Fractional Output Dividers

The FODs divide the APLL clock to synthesize low phase noise clocks with programmable frequencies. The FODs support integer division, rational division (that is, M/N), and fractional division with 1 part per trillion frequency resolution. The FOD output clocks are available via cross-connect to IOD[11:6] and IOD[17:12].

When configured for fractional division, the FODs can operate as DCOs, and they can cancel digital frequency adjustments made to the APLL via the Combo Bus so that their output frequencies are virtually unaffected by digital steering of the APLL. The frequency steering range of the FODs is ±244PPM.

3.6 Divider Synchronization

For each DPLL, the feedback divider is synchronized with the IODs selected to divide the output of its synthesizer. For DPLL5, the synthesizer is considered to be the VCO after the pre-divider, for DPLL[4:0] the synthesizer is considered to be FOD[4:0] respectively.

3.7 Clock Inputs

3.7.1 Clock Input Dividers

Each CLKIN[x] is connected to a programmable 20-bit integer divider that can be bypassed for divide by 1. The signals output by the input dividers (clkin_div[x]) must have a frequency ≤ 33MHz to be acceptable by the DPLLs.

3.7.2 Reference Monitors

All clkin_div[x] can be continually monitored for loss of signal and for frequency offset per user-programmed thresholds.

3.8 Digital PLLs

3.8.1 DPLL Reference Selection Mux

All clock inputs CLKIN[10:0] are available as references for all DPLLs. The DPLLs can lock to reference frequencies from 1kHz to 33MHz; clock inputs with frequencies above 33MHz must be divided using the internal reference dividers. Each DPLL steers its respective synthesizer (APLL or FOD) using digital frequency control words via the Combo Bus. The DPLLs support loop filter settings from 1mHz to 1kHz.

A DPLL in DCO mode does not lock to an input reference and its frequency is steered by external software instead.

Each DPLL operates in any of five states: Free-run, Acquire, Normal, Holdover, and Hitless Switch.

3.8.2 DPLL Free-Run State

In the Free-run state, a DPLL does not generate frequency control words and its respective synthesizer operates based on the frequency reference, and, if so configured, on information from other channels via the Combo Bus.

3.8.3 DPLL Acquire State

In the Acquire state, a DPLL tracks the selected qualified reference with the acquisition bandwidth and damping factor settings until the DPLL declares lock. The acquisition bandwidth and damping factor can be configured to accelerate the locking process. When a DPLL achieves lock it automatically transitions to the Normal state.

3.8.4 DPLL Normal State

In the Normal state, a DPLL tracks the selected reference with the normal locking bandwidth and damping factor settings. The normal bandwidth and damping factor can be configured to meet the filtering requirements of the intended application. In the Normal state, the long-term FFO of the DPLL synthesizer output clocks is the same as the long-term FFO of the reference and no cycle slips will occur.

3.8.5 DPLL Holdover State

In the Holdover state, a DPLL outputs digital frequency control words based on data acquired while in the Normal state so that its synthesizer outputs accurate frequencies when a reference is not provided to the DPLL. While a DPLL is in the Holdover state, its synthesizer operates based on the frequency reference, the DPLL holdover data, and, if so configured, on information from other channels via the Combo Bus.

3.8.6 DPLL Hitless Switch State

In the Hitless Switch state, the DPLL enters Holdover and measures the phase offset between the selected reference and the DPLL feedback clock. The measured phase offset is stored by the DPLL and is used to minimize the phase transient at the output of the DPLL when it locks to the new reference.

3.9 DPLL External Feedback

In some applications it is useful to use an external feedback path from the synthesizer to the DPLL. The DPLL reference selection multiplexer can select one of the external references for use as the feedback clock for the DPLL. When external feedback is used, the feedback clock must have the same frequency as the selected DPLL reference.

3.10 DPLL Reference Switching

The active reference for a DPLL is determined by forced selection or by automatic selection based on user-programmed priorities, locking allowances, reference monitors, revertive and non-revertive settings, and GPIO LOS inputs.

A DPLL will act to close phase differences between the selected reference and the feedback clock. A step change in the phase difference can occur when a new reference is selected while the DPLL is in the Acquire state or the Normal state, or when the DPLL exits the Holdover state and enters the Acquire state. The resulting phase transient is filtered by the DPLL loop filter and the phase slope limiter, and there will not be any instantaneous phase steps or glitches on the device outputs.

3.10.1 Hitless Reference Switching

Hitless reference switching causes a DPLL to ignore the phase difference between the newly selected reference and the DPLL feedback clock; the DPLL will track the FFO of the newly selected reference.

When hitless reference switching is enabled – and a DPLL is in the Acquire state or the Normal state, and the selected reference is changed – the DPLL enters the Holdover state and measures the phase offset between the newly selected reference and the DPLL feedback clock. The measured phase offset is stored and is subtracted from later phase offsets measured by the DPLL phase detector. The DPLL then enters the Acquire state.

When the DPLL is in the Holdover state due to a reference failure or any other reason, hitless reference switching can be used when entering the Acquire state.

3.10.2 Aligned Reference Switching

Hitless reference switching does not allow a deterministic phase relationship to exist between the DPLL reference and its output clocks. When a deterministic phase relationship is needed, hitless reference switching should not be enabled so that the DPLL can align its output clocks with the DPLL reference.

3.11 Clock Output Enable

The RC38616/RC38412 enables and disables clock outputs synchronously to ensure there are no runt pulses during clock output enable and disable operations.

Clock output enables can be controlled by software using the global_oe and out_driver_en register fields. Alternatively, GPIOs can be assigned the clock output enable function using the oe_source_sel and gpio_func register fields. For more information, see the *RC38616/RC38412 Programming Guide*.

When a GPIO is assigned an output enable function it should be configured with gpio_resync = 0x0 and gpio_deglitch_bypass = 0x1. This disables GPIO resynchronization and bypasses the GPIO deglitcher ensuring lowest latency. When so configured, the maximum time delay from the time the voltage level on a GPIO input changes state until the clock output is enabled or disabled is 13ns plus four periods of the output clock.

3.12 SYSREF

The RC38616/RC38412 includes a fully integrated SYSREF controller supporting JESD204B/C/D applications. SYSREF generation is deterministic, phase-aligned to device clocks, and scalable across multiple devices using SYSREF group topologies.

3.12.1 Device Clocks

- Any OUT[x] can be independently configured to output a device clock
- Device clocks are continuous clocks with a deterministic phase relationship to SYSREF
- Supported device clock frequencies include (but are not limited to): 122.88MHz, 153.6MHz, 184.32MHz, 245.76MHz, 307.2MHz, 368.64MHz, 491.52MHz, 614.4MHz, 737.28MHz, and 983.04MHz

3.12.2 SYSREF Outputs

- Any OUT[x] can be independently configured to output SYSREF
- SYSREF frequencies are integer divisors of the associated device clock, with frequencies up to 16.384MHz
- SYSREF outputs:
  - Are continuous clocks that start and stop under control of the SYSREF controller
  - Have a deterministic phase relationship to the associated device clock
  - Start and stop without generating runt pulses
  - Support LVDS signaling
  - Stop toggling with P = Low and N = High

3.12.3 SYSREF Event Types

The device supports the following SYSREF event types:

- Continuous SYSREF – SYSREF toggles continuously between a start trigger and a stop trigger
- Counted SYSREF – SYSREF toggles for a programmed number of SYSREF periods (1 to 255) after a start trigger
- Continuous Pulse/Pause SYSREF – SYSREF toggles for a programmable pulse interval followed by a programmable pause interval, repeating until a stop trigger is received. Pulse and pause durations are independently programmable from 1 to 255 SYSREF periods.
- Omitted Pulse SYSREF – SYSREF toggles continuously between a start trigger and a stop trigger with an omitted pulse transmitted within 1UI of an omitted pulse SYSREF trigger (see 3.12.4.1).

All SYSREF outputs operate using the same SYSREF event type, selected via a programmable SYSREF event type number.

3.12.4 SYSREF Triggers

SYSREF events can be initiated and controlled using multiple trigger sources:

- GPIO transitions (level- or edge-sensitive)
- Register bit transitions
- Time of Day (TOD) compare events
- Omitted pulse detection on a designated CLKIN
- Synchronous clock enable of SYSREF_CLK outputs (SYSREF group operation)

Any SYSREF event can be stopped by a register write, independent of the selected stop trigger source.

3.12.5 Omitted Pulse SYSREF Trigger

The RC38616/RC38412 supports omitted pulse SYSREF triggering, where a missing clock edge on a designated CLKIN is used as a SYSREF trigger source.

- Omitted pulse detection is performed using a configurable monitor
- Detection of an omitted pulse generates a maskable interrupt
- Omitted pulse SYSREF triggering operates deterministically when the CLKIN frequency is an integer divisor of SYSREF_CLK
- For start only SYSREF events, a single omitted pulse acts as a SYSREF start trigger
- For start/stop SYSREF events, successive omitted pulses act as start and stop triggers

- When an omitted pulse is detected on a reference used by a DPLL:
  - The DPLL remains locked and in the normal state
  - No phase error is introduced into the DPLL loop

3.12.6 SYSREF Phase Alignment

- By default, all device clocks and SYSREF outputs are phase aligned
- The output phase of any device clock or SYSREF can be independently adjusted using integrated output delay elements

3.13 Time Sync

The RC38616/RC38412 includes a Time Sync block that enables external software to monitor and control phase and time alignment of the device with external signals and devices.

The time of day (TOD) and Synthesis block synthesizes a time clock with a frequency from 10MHz to 250MHz. The block includes a 60-bit addressable TOD accumulator that counts time clock pulses and generates sync pulses with a frequency from 0.5Hz to 8kHz. The phase of the time sync pulses can be controlled by external software without disturbing the time clock. Any one of the FODs can be used to control the frequency of time clock. The time clock and time sync signals are available on any of OUT[17:12].

A time-to-digital converter (TDC) is provided to make precision phase and time comparisons between external signals, between internal signals, or between internal and external signals with frequencies between one-time-event and 33MHz. Internal signals available to the TDC are the time clock, time sync, and the DPLL feedback clocks. The precision of the TDC is better than 100ps.

3.14 Status and Control

All control and status registers are accessed through a 1MHz I^2C or 20MHz SPI target (slave) microprocessor interface. The device can automatically load a configuration from internal one time programmable (OTP) memory. Alternatively, the I^2C host (master) interface can automatically load a configuration from an external EEPROM after reset.

For more information about the device's registers, contact Renesas Technical Support.

4. Applications Information

4.1 Power Considerations

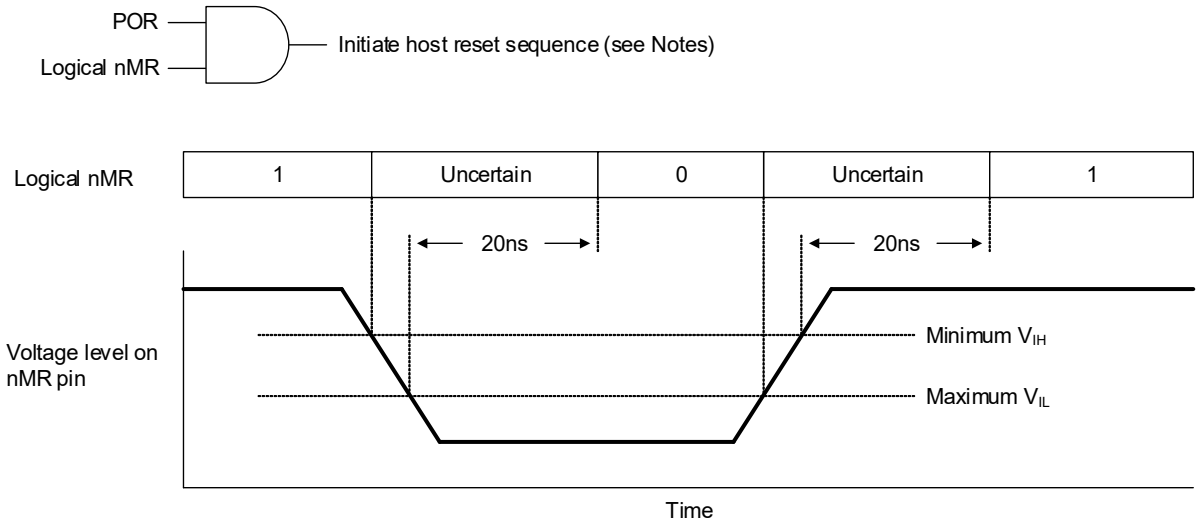
There are no power supply sequencing requirements; however, if V_{DDOx} or V_{DD_CLK} reach 90% of V_{DD} nominal after V_{DD_DIG} then a soft reset or a host (master) reset must be initiated to ensure the input dividers and output dividers are synchronized.

For power and current consumption calculations, see the Renesas IC Toolbox (RICBox) software tool.

4.2 Power-On Reset and Reset Controller

Upon power-up, an internal power-on reset (POR) signal is asserted 20ms after the V_{DDXO}, V_{DD_DCD}, and V_{DDD33_DIG} supplies all reach 90% of V_{DD} nominal. The first host reset sequence is initiated when POR is asserted and the voltage level on the nMR pin is high.

After the first host reset sequence is initiated, another host reset sequence can be initiated by taking the voltage level on the nMR pin low and then high while POR remains asserted (see Figure 7). To ensure a host reset sequence is initiated, the voltage level on the nMR pin must be held low for at least 20ns before transitioning high. To ensure deterministic behavior, voltage level transitions on the nMR pin must be monotonic between minimum V_{IH} and maximum V_{IL} (see GPIO and nMR DC Electrical Characteristics).



Notes:
- Requires 1 from logical nMR for the first host reset sequence
- Requires 0 to 1 transition from logical nMR after the first host reset sequence has been initiated

Figure 7. Host Reset Sequence Initiation

The nMR pin has an internal pull-up to VDD_DIG that can be left to float, or it can optionally be externally pulled high or low. If nMR is high when the internal POR is asserted, the reset controller will initiate a host reset sequence. If nMR is low when the internal POR is asserted, the reset controller will not initiate a host reset sequence until nMR is taken high.

During the host reset sequence all clock outputs are initially disabled and will be enabled during the reset sequence at a point depending on the out_startup bits. Disabled differential outputs will have OUTx = low and nOUTx = high. Disabled LVCMOS outputs with cmos_same_phase = 1 will have OUTx = low and nOUTx = low. Disabled LVCMOS outputs with cmos_same_phase = 0 will have OUTx = low and nOUTx = high.

The serial ports are accessible when the device_ready_sts register bit is set to 0x1. Any GPIO can be configured to indicate the state of the device_ready_sts register bit by setting the associated gpio_func register field to 0x18. When a reset sequence completes, the rst_done_sts register bit is set to 0x1.

When a configuration is loaded from EEPROM, the voltage level on the nMR pin must be held high from the time a host reset sequence is initiated until after the EEPROM transactions have completed, as indicated when the device_ready_sts bit is set to 1. Any GPIO can be configured to indicate the state of the device_ready_sts bit.

4.3 Recommendations for Unused Input and Output Pins

4.3.1 CLKIN/nCLKIN Pins

Unused CLKIN/nCLKIN pins should be left to float. Renesas recommends that CLKIN/nCLKIN inputs that are connected but not used, should not be driven with active signals.

4.3.2 LVCMOS Control Pins

LVCMOS control pins have internal pull-up resistors. Additional 1kΩ pull-up resistors can be added but are not required.

4.3.3 LVCMOS Output Pins

Unused LVCMOS outputs must be left to float. Renesas recommends that no trace should be attached. Unused LVCMOS outputs should be configured to a high-impedance state to prevent noise generation.

4.3.4 Differential Output Pins

Unused differential outputs must be left to float. Renesas recommends that no trace should be attached. Both sides of a differential output pair should be either left to float or terminated.

4.4 Overdriving the Crystal Interface

When overdriving the crystal interface, the XOUT pin is left to float and the XIN input is overdriven by an AC coupled LVCMOS driver, or by one side of an AC coupled differential driver. The XIN pin is internally biased to 0.6V. The voltage swing on XIN should be between 0.5V peak-to-peak and 1.2V peak-to-peak, and the slew rate should not be less than 0.2V/ns.

Figure 8 shows a 1.8V or 2.5V LVCMOS driver overdriving the XIN pin. For V_{DD} = 1.8V, considering the output impedance of the driver (R_O), the values of the series resistance (R_S) and R_1 should be chosen so that the voltage swing on XIN will be below 1.2V peak-to-peak. For V_{DD} = 2.5V the sum of the output impedance of the driver (R_O) and the series resistance (R_S) can be made higher than R_1 so that the voltage swing on XIN will be below 1.2V peak-to-peak.

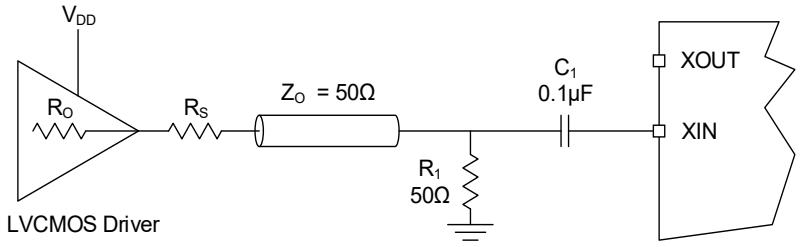


Figure 8. LVCMOS Driver to Crystal Input Interface

Figure 9 shows one side of an LVPECL driver overdriving the XIN pin.

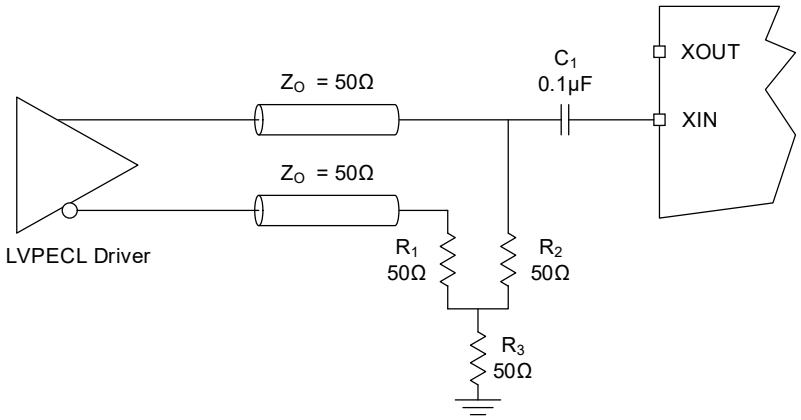


Figure 9. LVPECL Driver to Crystal Input Interface

4.5 Differential Output Termination

The RC38616/RC38412 programmable differential clock outputs support LVDS, HCSL, and CML. Receivers that support LVDS, HCSL, or CML can be direct-coupled with RC38616/RC38412 outputs. Differential receiver types other than LVDS, HCSL, or CML can be AC-coupled.

The RC38616/RC38412 differential clock outputs support selectable internal termination resistors as shown in Figure 10. The value of resistors R_{O1}, R_{O2}, R_{O3}, and R_{O4} is 50Ω.

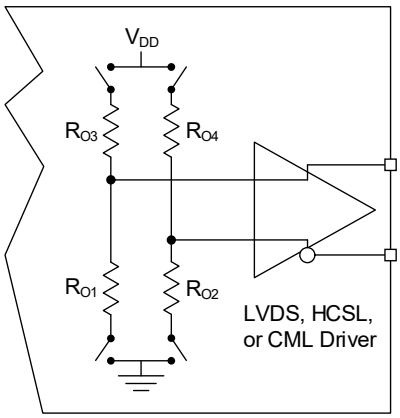


Figure 10. Internal Termination Resistors for Differential Drivers

Note: Some receivers are equipped with internal terminations that can include the following: trace termination, voltage biasing, and AC-coupling. Consult with the receiver specifications to determine if the termination components shown in this section are needed.

4.5.1 Direct-Coupled HCSL Termination

For HCSL receivers, RC38616/RC38412 clock outputs should be configured for HCSL, and the devices should be direct-coupled. The RC38616/RC38412 supports several programmable HCSL voltage swing options.

Figure 11 shows an HCSL driver direct-coupled with an HCSL receiver and configured for internal source termination. The RC38616/RC38412 supports source termination, with an internal 50Ω resistors to ground at the transmitter. Resistor R_1 is optional and is used to improve impedance matching. If R_1 is used, it will reduce the amplitude at the receiver by 50%, this can be mitigated by adjusting the output amplitude of the driver.

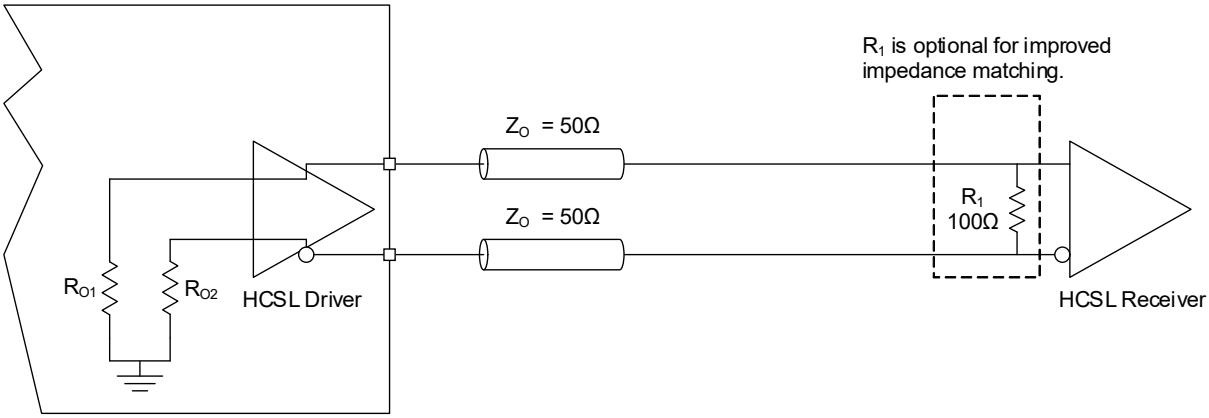


Figure 11. HCSL Source Termination Using Internal Termination

Figure 12 shows an HCSL driver direct-coupled with an HCSL receiver using end termination.

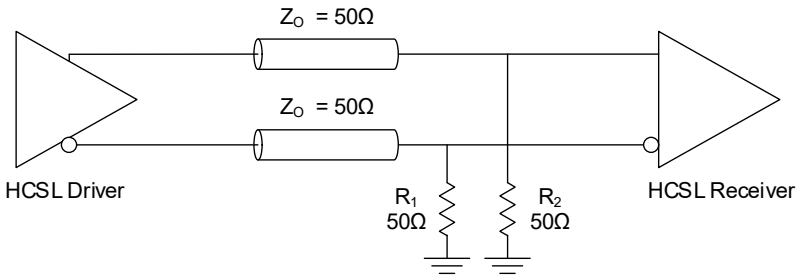


Figure 12. HCSL End Termination

4.5.2 Direct-Coupled LVDS Termination

For LVDS receivers, RC38616/RC38412 clock outputs should be configured for LVDS, and should be direct-coupled. The device supports several programmable LVDS voltage swing and common mode options.

Figure 13 shows an LVDS driver direct-coupled with an LVDS receiver. The recommended value for the termination resistor (R_1) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of the transmission line. To avoid transmission-line reflection issues, R_1 should be surface-mounted and placed as close to the receiver as practical.

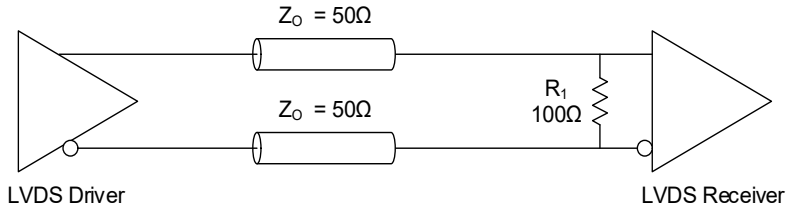


Figure 13. LVDS Termination

4.5.3 Direct-Coupled CML Termination

For CML receivers, RC38616/RC38412 clock outputs should be configured for CML, and should be direct-coupled. The device supports several programmable CML voltage swing options.

Figure 14 shows a CML driver direct-coupled with a CML receiver.

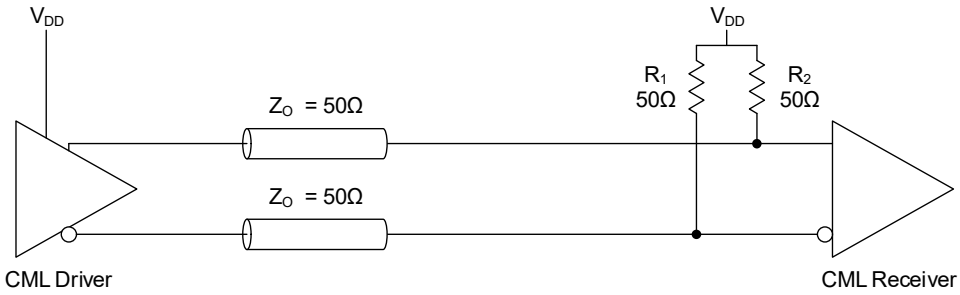


Figure 14. Direct-Coupled CML Termination

4.5.4 AC-Coupled Differential Termination

For AC-coupled differential terminations, the RC38616/RC38412's clock outputs should be configured for HCSL and the HCSL driver should be configured with a voltage swing appropriate for the receiver. The device supports several programmable HCSL voltage swing options.

Figure 15 shows an HCSL driver configured for internal termination and AC-coupled with a differential receiver with external termination resistors and biasing. Resistors R_1, R_2, R_3, and R_4 should be selected to provide the appropriate bias voltage for the receiver. Consult receiver specifications for input swing and bias requirements. An optional resistor (R_5) can be used to improve impedance matching. If R_5 is used, it will reduce the amplitude at the receiver by 50%; this can be mitigated by adjusting the output amplitude of the driver.

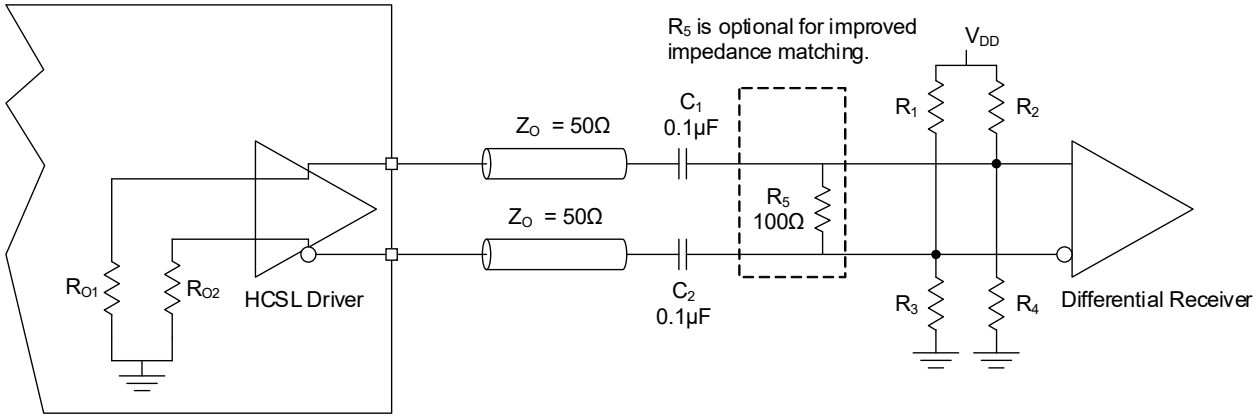


Figure 15. AC-Coupled Differential Termination

For more information on AC-coupling, see Renesas application note AN-953, *Quick Guide - Output Terminations*.

4.5.5 AC-Coupled LVPECL (AC-LVPECL) Termination

AC-coupling should be used for LVPECL receivers.

For AC-coupled LVPECL (AC-LVPECL) terminations, the RC38616/RC38412 clock outputs should be configured for HCSL. The device supports several programmable HCSL voltage swing options and it should be configured as appropriate for the receiver and termination scheme. Consult receiver specifications for input swing and bias requirements.

Figure 16 shows an HCSL driver configured for internal termination driving an AC-LVPECL receiver with internal termination resistors and biasing.

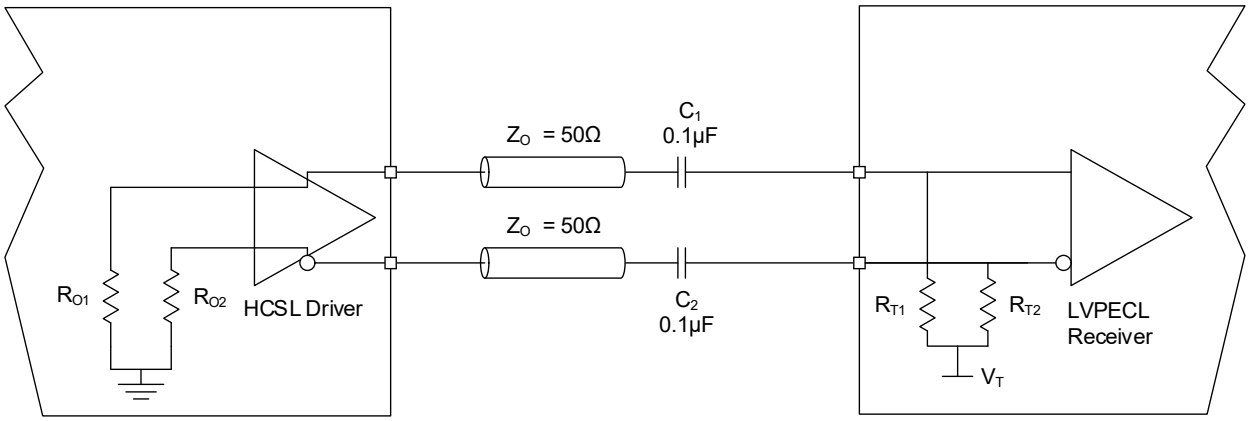


Figure 16. AC-LVPECL Termination for LVPECL Receiver with Internal Termination Resistors and Biasing

For more information on AC-coupling, see Renesas application note AN-953, *Quick Guide - Output Terminations*.

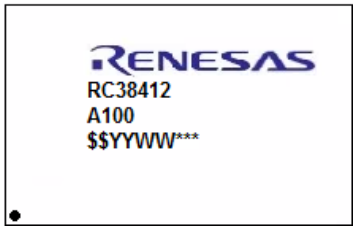
5. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

6. Marking Diagrams



- Lines 1 and 2: part number
- Line 3:
  - "$$" indicates the mark code
  - "YWW" indicates the last digit of the year and work week the part was assembled
  - "***" indicates the last three characters of assembly lot



- Lines 1 and 2: part number
- Line 3:
  - "$$" indicates the mark code
  - "YYWW" indicates the last two digits of the year and work week the part was assembled
  - "***" indicates the last three characters of assembly lot

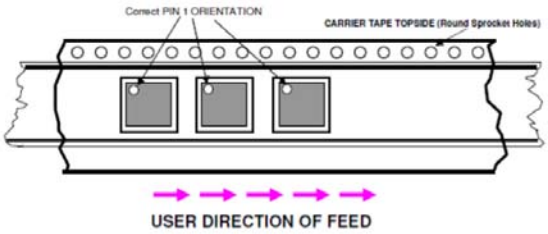
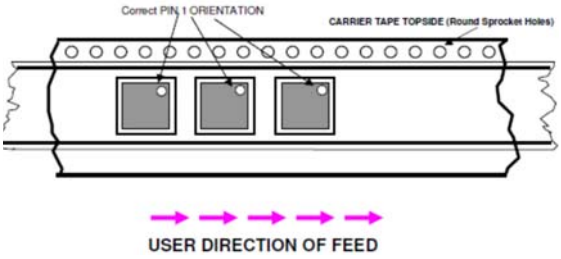
7. Ordering Information

Table 37. Ordering Information

Part Number [1][2]	Package Description	Carrier Type	Temperature Range [3]
RC38616AyxxGBB#HC0	144-BGA, 10 × 10 mm	Tape, Pin 1 orientation: EIA-481-C	-40 to +105°C
RC38616AyxxGBB#KC0	144-BGA, 10 × 10 mm	Tape, Pin 1 orientation: EIA-481-D/E	
RC38616AyxxGBB#BC0	144-BGA, 10 × 10 mm	Tray	
RC38412Ayxxzzz#HC0	100-BGA, 9 × 9 mm	Tape, Pin 1 orientation: EIA-481-C	-40 to +105°C
RC38412Ayxxzzz#KC0	100-BGA, 9 × 9 mm	Tape, Pin 1 orientation: EIA-481-D/E	
RC38412Ayxxzzz#BC0	100-BGA, 9 × 9 mm	Tray	

1. Replace "y" in the part number with "1" for VCO frequency range 9.8GHz to 10.35GHz, or "2" for VCO frequency range 9.25GHz to 9.85GHz.
2. Replace "xx" in the part number with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use "00" for unprogrammed parts.
3. Temperature range refers to board temperature.

Table 38. Pin 1 Orientation in Tape and Reel Packaging

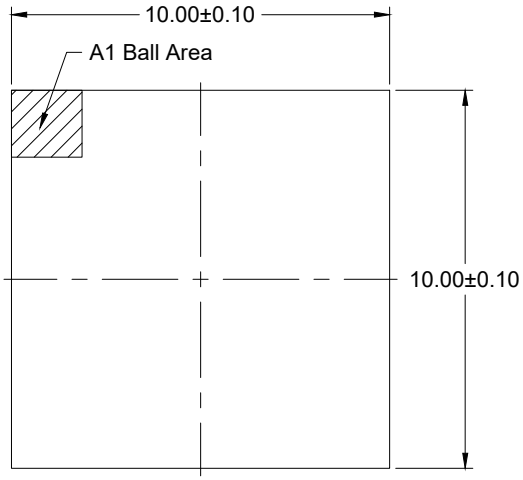
Part Number Suffix	Pin 1 Orientation	Illustration
HC0	Quadrant 1 (EIA-481-C)	
KC0	Quadrant 2 (EIA-481-D/E)	

8. Revision History

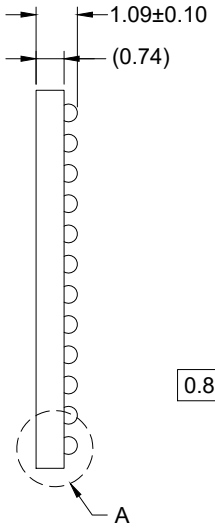
Revision	Date	Description
1.00	Oct 2, 2026	Initial release

Package Outline Drawing

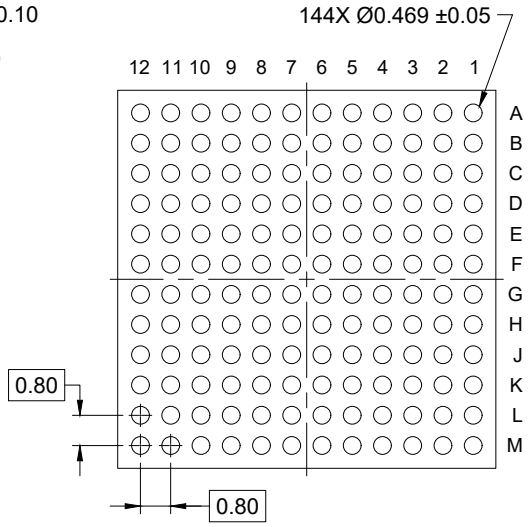
PSC-5141-01
BT0144AA
144-BGA 10.00 x 10.00 x 1.09 mm Body, 0.80 mm Pitch
Rev.00, May 19, 2025



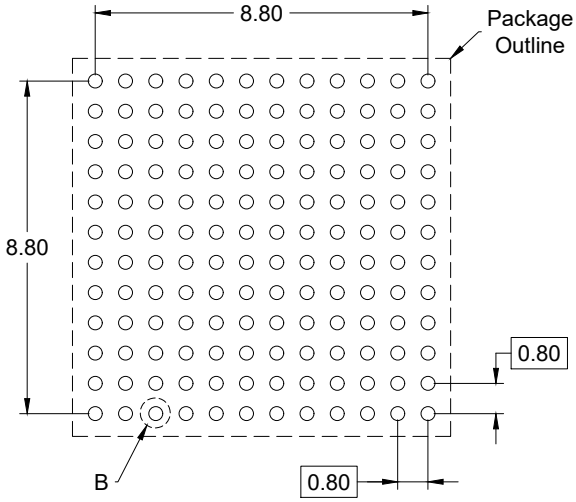
TOP VIEW



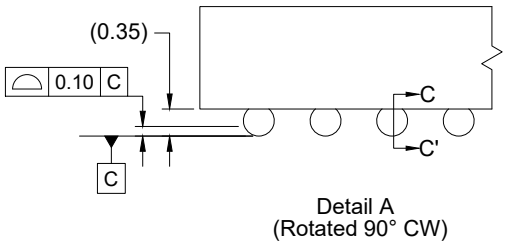
SIDE VIEW



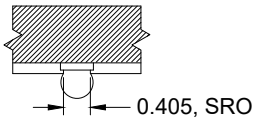
BOTTOM VIEW



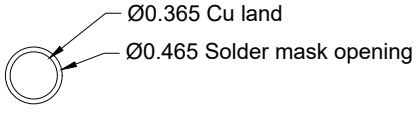
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)



Detail A
(Rotated 90° CW)



Section C-C'



Detail B

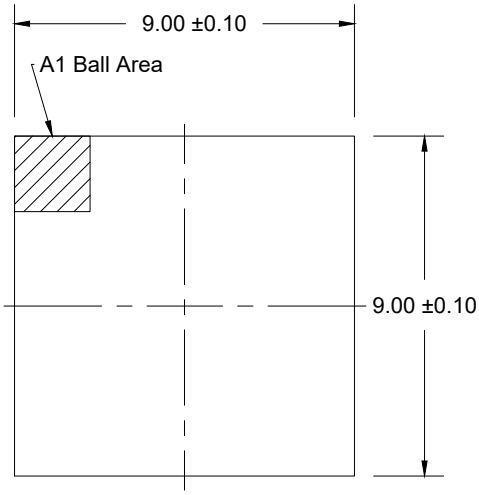
NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solderball diameter is Ø0.45 mm.

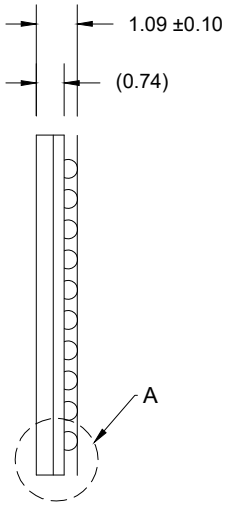
© Renesas Electronics Corporation

Package Outline Drawing

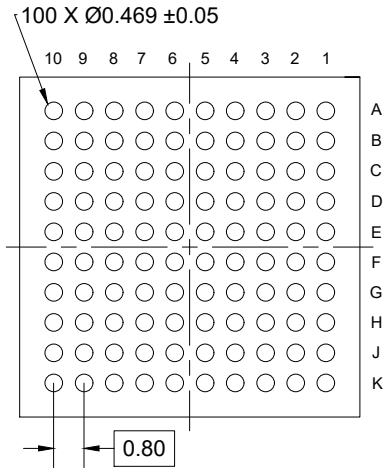
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100-BGA 9.00 x 9.00 x 1.09 mm Body, 0.80 mm Pitch
PSC-4959-01, Revision: 01, Date Created: Mar 14, 2023



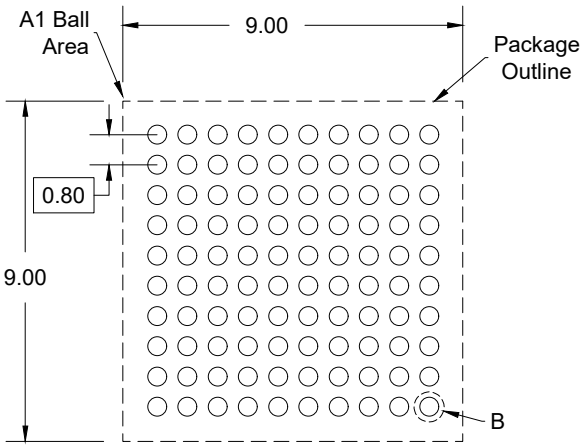
TOP VIEW



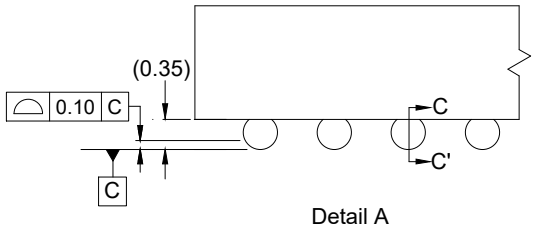
SIDE VIEW



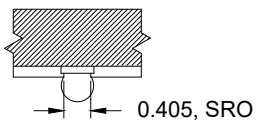
BOTTOM VIEW



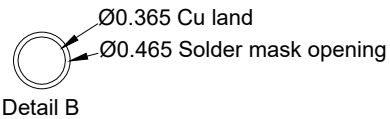
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)



Detail A
(Rotated 90° CW)



Detail C - C'



Detail B

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solderball diameter is Ø0.45 mm.

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