RC22312, RC22308

FemtoClock™ 3 Multi-Frequency Clock Synthesizer

Description

The RC22312/RC22308 is an ultra-low phase noise multi-frequency clock synthesizer and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with 25fs RMS jitter supporting 112Gbps and 224Gbps SerDes.

Applications

- Clock synthesis for:
  - 112Gbps and 224Gbps SerDes
  - 100 / 200 / 400 / 800 / 1600 Gbps Ethernet PHYs
- Switches and routers
- Medical imaging
- Test and measurement

Features

- Jitter 25fs RMS, 12kHz to 20MHz with 4MHz HPF
- Output frequency range:
  - 4kHz to 1GHz for differential outputs
  - 4kHz to 250MHz for single-ended outputs
- Up to 12 HCSL (AC-LVPECL) or LVDS outputs with independent integer dividers; differential outputs can be configured as two single-ended outputs
- DCO frequency resolution < 10^{-13}
- Factory programmable internal OTP
- RC22312
  - 12 outputs
  - 9 × 9 mm, 64-VFQFPN
- RC22308
  - 8 outputs
  - 7 × 7 mm, 48-VFQFPN
- Operating voltage: 1.8V
  - Serial ports support 1.8V or 3.3V
- Operating temperature:
  - -40°C to 85°C ambient
  - -40°C to 105°C board

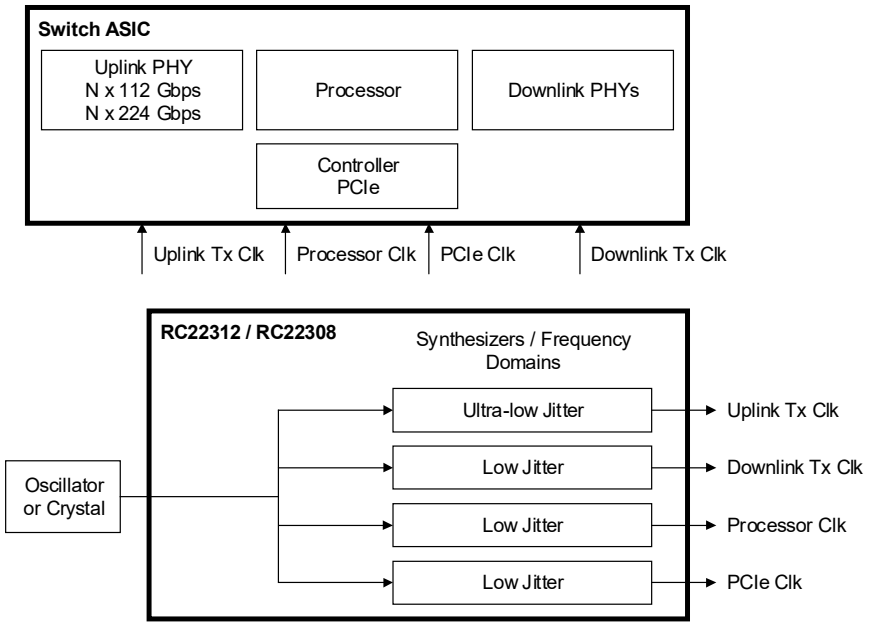

Figure 1. Typical Wireline Infrastructure Use Case

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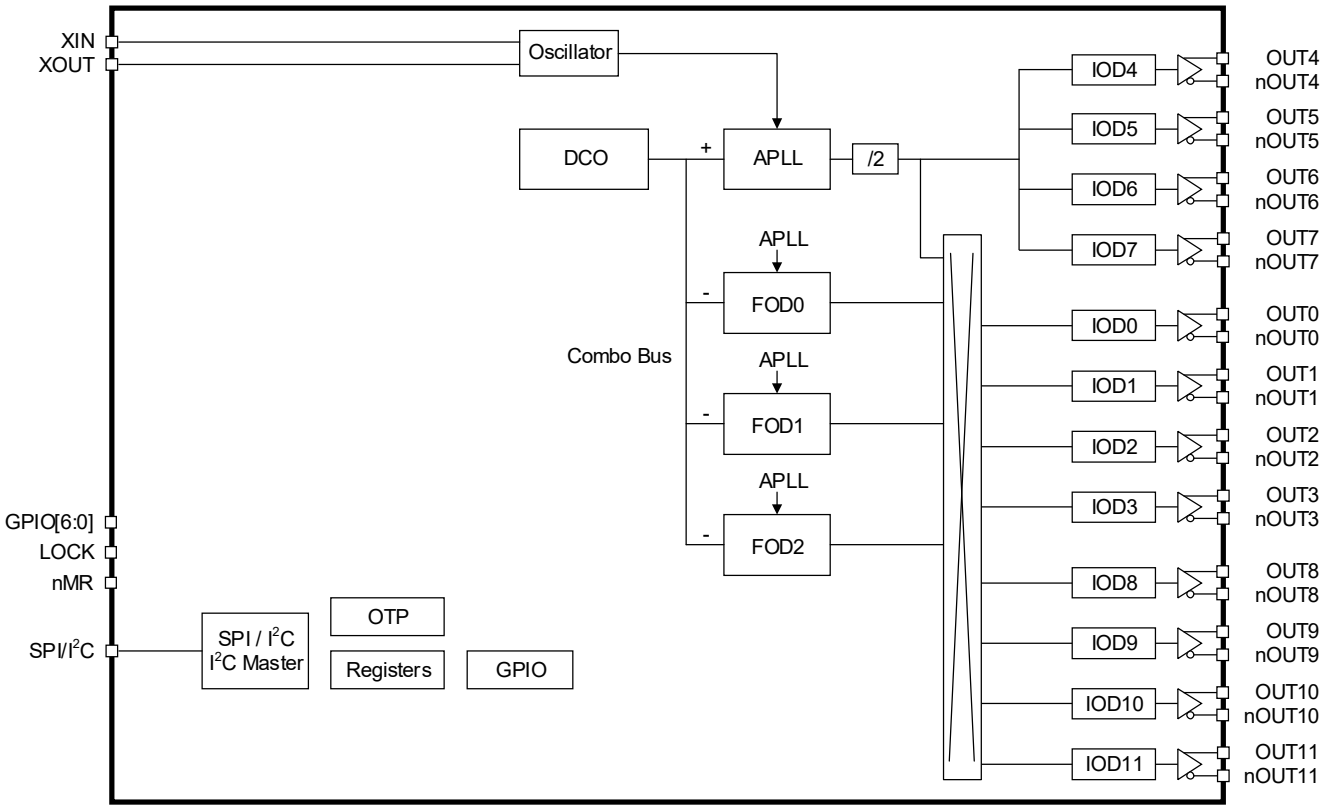

Figure 2. RC22312 Block Diagram

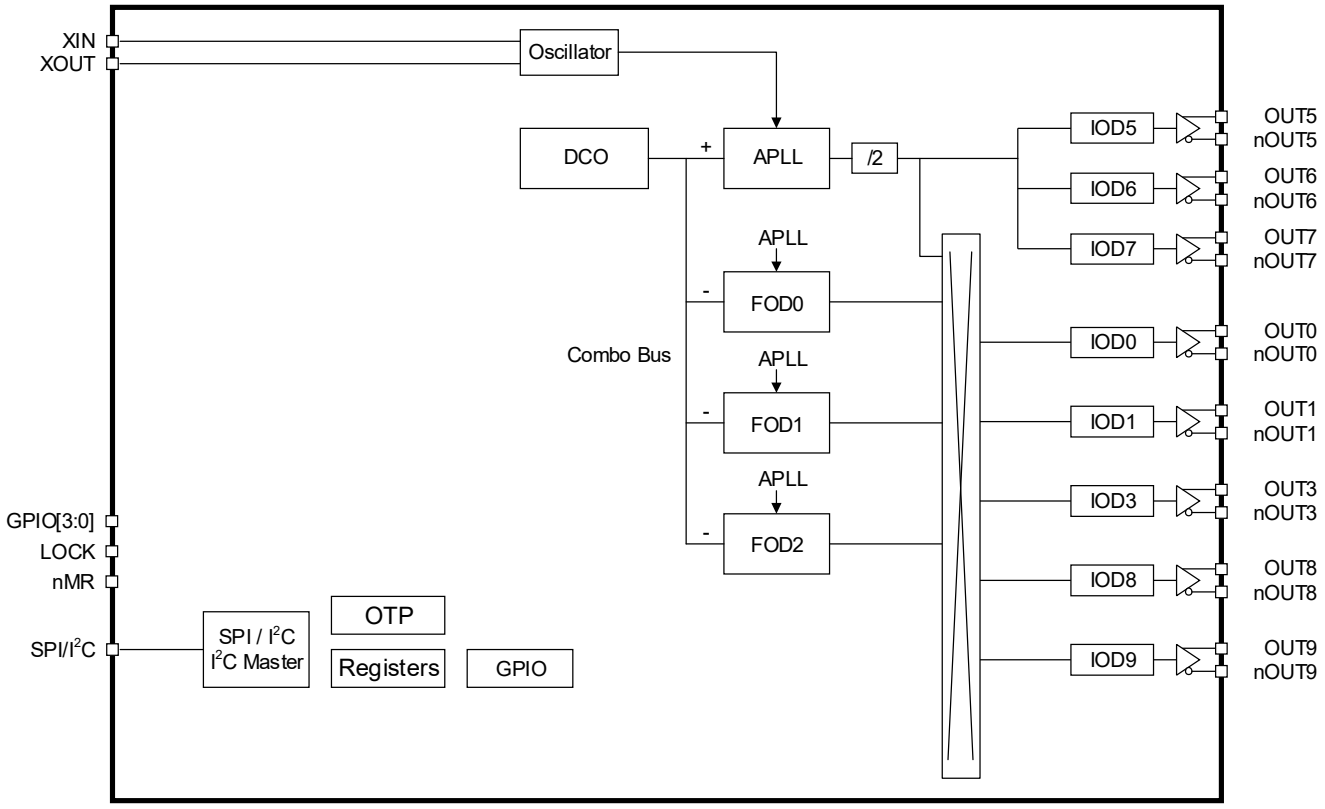

Figure 3. RC22308 Block Diagram

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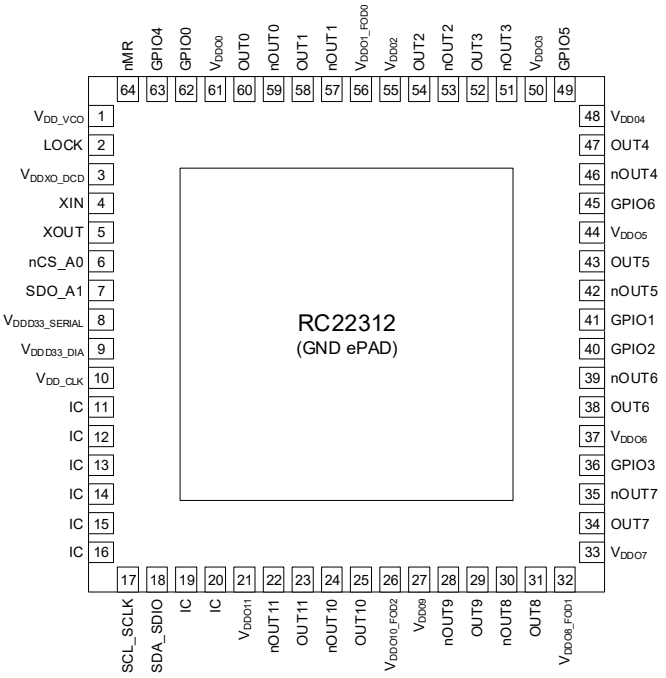
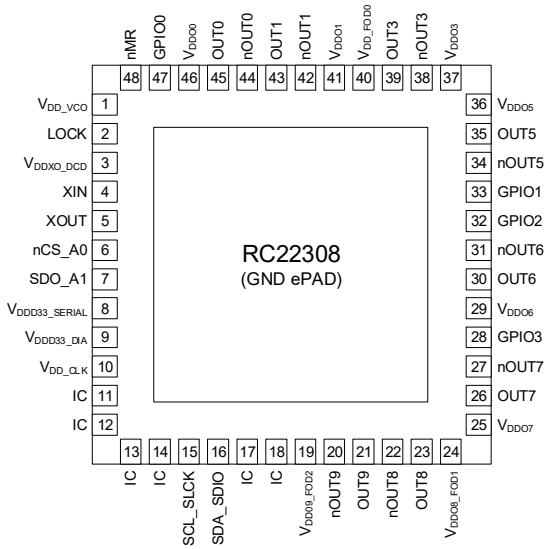
Top View
(9 × 9 mm, 0.5mm lead pitch)



Top View
(7 × 7 mm, 0.5mm lead pitch)



1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number		Type	Description
	RC22312	RC22308		
XIN	4	4	I	Crystal oscillator / xCXO input.
XOUT	5	5	O	Crystal oscillator output.
OUT0	60	45	O	Clock output, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair. nOUTx indicates the negative pin of a differential pair.
nOUT0	59	44	O	
OUT1	58	43	O	
nOUT1	57	42	O	
OUT2	54	-	O	
nOUT2	53	-	O	
OUT3	52	39	O	
nOUT3	51	38	O	
OUT4	47	-	O	Clock output, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair. nOUTx indicates the negative pin of a differential pair.
nOUT4	46	-	O	
OUT5	43	35	O	
nOUT5	42	34	O	
OUT6	38	30	O	
nOUT6	39	31	O	
OUT7	34	26	O	
nOUT7	35	27	O	

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Number		Type	Description
	RC22312	RC22308		
OUT8	31	23	O	Clock output, differential pair / single ended. LVDS, HCSL, or LVCMOS. OUTx indicates the positive pin of a differential pair. nOUTx indicates the negative pin of a differential pair.
nOUT8	30	22	O	
OUT9	29	21	O	
nOUT9	28	20	O	
OUT10	25	-	O	
nOUT10	24	-	O	
OUT11	23	-	O	
nOUT11	22	-	O	
nMR	64	48	I	Active-low master reset. The V_{DDO0} pin must be powered to ensure proper operation.
nCS_A0	6	6	I	I2C mode: address bit 0. SPI mode: active-low chip select.
SCL_SCLK	17	15	I/O	I^2C Mode: I^2C interface bi-directional clock. SPI Mode: serial clock.
SDA_SDIO	18	16	I/O	I^2C mode: I^2C interface bi-directional serial data. SPI 3-wire mode: bi-directional serial data. SPI 4-wire mode: input serial data.
SDO_A1	7	7	I/O	I^2C mode: address bit 1. SPI 3-wire mode: unused. SPI 4-wire mode: output serial data.
GPIO0	62	47	I/O	General purpose input/output.
GPIO1	41	33	I/O	
GPIO2	40	32	I/O	
GPIO3	36	28	I/O	
GPIO4	63	-	I/O	
GPIO5	49	-	I/O	
GPIO6	45	-	I/O	
LOCK	2	2	O	Lock indicator. This pin is GPIO8 with gpio_func default = 0x1B (APLL lock).
V_{DD_CLK}	10	10	Power	Power supply for CLKINx buffers, dividers, muxes, and the TDC. 1.8V is supported.
V_{DD_VCO}	1	1	Power	Power supply for the VCO. 1.8V is supported.
V_{DDD33_DIA}	9	9	Power	Power supply for digital core, digital in FODs, and digital in the APLL. 1.8V and 3.3V are supported. 1.8V is recommended for lowest power consumption during normal operation.
V_{DDD33_SERIAL}	8	8	Power	Power supply for serial port. 1.8V and 3.3V are supported.
V_{DDO0}	61	46	Power	Power supply for OUT0/nOUT0, IOD0, GPIO0, GPIO4, and nMR. 1.8V is supported.
V_{DDO1_FOD0}	56	-	Power	Power supply for OUT1/nOUT1, IOD1, and FOD0. 1.8V is supported.
V_{DDO1}	-	41	Power	Power supply for OUT1/nOUT1 and IOD1. 1.8V is supported.
V_{DD_FOD0}	-	40	Power	Power supply for FOD0. 1.8V is supported.
V_{DDO2}	55	-	Power	Power supply for OUT2/nOUT2 and IOD2. 1.8V is supported.
V_{DDO3}	50	37	Power	Power supply for OUT3/nOUT3, IOD3, and GPIO5. 1.8V is supported.
V_{DDO4}	48	-	Power	Power supply for OUT4/nOUT4, IOD4, and GPIO6. 1.8V is supported.
V_{DDO5}	44	36	Power	Power supply for OUT5/nOUT5, IOD5 and GPIO1. 1.8V is supported.
V_{DDO6}	37	29	Power	Power supply for OUT6/nOUT6, IOD6, and GPIO2. 1.8V is supported.
V_{DDO7}	33	25	Power	Power supply for OUT7/nOUT7, IOD7, and GPIO3. 1.8V is supported.
V_{DDO8_FOD1}	32	24	Power	Power supply for OUT8/nOUT8, IOD8, and FOD1. 1.8V is supported.
V_{DDO9}	27	-	Power	Power supply for OUT9/nOUT9 and IOD9. 1.8V is supported.

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Number		Type	Description
	RC22312	RC22308		
V_{DDO9_FOD2}	-	19	Power	Power supply for OUT9/nOUT9, IOD9, FOD2, and FOD calibration. For theRC22308, the V_{DDO9_FOD2} pin must be powered if “any” of the FODs are used. 1.8V is supported.
V_{DDO10_FOD2}	26	-	Power	Power supply for OUT10/nOUT10, IOD10, FOD2, and FOD calibration. For theRC22312, the V_{DDO10_FOD2} pin must be powered if “any” of the FODs are used. 1.8V is supported.
V_{DDO11}	21	-	Power	Power supply for OUT11/nOUT11 and IOD11. 1.8V is supported.
V_{DDXO_DCD}	3	3	Power	Power supply for the analog reference and the LOCK output. 1.8V is supported.
IC	15	13	I	Internal connection, leave to float.
IC	16	14	I	
IC	13	11	I	
IC	14	12	I	
IC	11	-	I	
IC	12	-	I	
IC	19	17	I	
IC	20	18	I	
V_{SS}	ePad	ePad	Power	Device ePad. Must be connected to ground.

Table 2. Input Characteristics

Symbol	Parameter		Condition	Minimum	Typical	Maximum	Unit
C_{IN}	Input capacitance	nMR, nCS_A0, SDO_A1, GPIOx, SCL_SCLK, SDA_SDIO	-	-	4	-	pF
R_{PULLUP}	Input pull-up resistor	nMR	-	-	98	-	kΩ
		nCS_A0, SDO_A1, GPIOx	-	-	53	-	
$R_{PULLDOWN}$	Input pull-down resistor	nCS_A0, SDO_A1, GPIOx	-	-	53	-	kΩ

2. Specifications

2.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{DD33}	Supply Voltage with Respect to Ground	V_{DDD33_Serial}, V_{DDD33_DIA}	-0.5	3.63	V
V_{DD18}	Supply Voltage with Respect to Ground	V_{DD_CLK}, V_{DDXO_DCD}, V_{DD_VCO}, V_{DD05_FOD0}, V_{DDO6_FOD1}, V_{DDO9_FOD2}	-0.5	1.89	V
V_{IN}	Input Voltage	XIN [1]	-0.5	1.32	V
		GPIOx used as inputs, nMR [2]	-0.5	V_{DDOx} + 0.3	
		nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO	-0.5	3.63	
I_{IN}	Input Current	GPIOx used as inputs, nMR	-	±25	mA
		nCS_A0, SDO_A1, SCL_SCLK, SDA_SDIO	-	±25	
I_{OUT}	Output Current - Continuous	OUTx, nOUTx	-	30	mA
		LOCK, SDO_A1, SCL_SCLK, SDA_SDIO	-	25	
		GPIOx used as outputs	-	25	
	Output Current - Surge	OUTx, nOUTx	-	60	mA
		LOCK, SDO_A1, SCL_SCLK, SDA_SDIO	-	50	
		GPIOx used as outputs	-	50	
T_J	Maximum Junction Temperature	-	-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C
-	Human Body Model (Tested per JESD22-A114 (JS-001) Classification)	-	-	2000	V
-	Charged Device Model (Tested per JESD22-C101 Classification)	-	-	250	V

1. This limit only applies when XIN is overdriven by an external oscillator. No limit is implied when connected directly to a crystal.
2. V_{DDOx} refers to the supply powering the GPIO or nMR. For V_{DD} pin mapping, see Pin Assignments.

2.2 Thermal Resistance

Table 4. Thermal Resistance

Package	Symbol	Conditions [1]	Typical Value	Unit
NDG48	Θ_{JC}	Junction to case	17.5	°C/W
	Θ_{JB}	Junction to base	1.0	
	Θ_{JA0}	Junction to air, still air	20.0	
NDG64	Θ_{JC}	Junction to case	13.1	°C/W
	Θ_{JB}	Junction to base	1.0	
	Θ_{JA0}	Junction to air, still air	20.0	

1. ePad soldered to board.

2.3 Recommended Operating Conditions

Table 5. Recommended Operating Conditions [1][2]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature	-	-	-	125	°C
T_A	Ambient Operating Temperature	-	-40	-	85	°C
V_{DDx}	Supply Voltage with Respect to Ground	V_{DD} pins with 1.8V supply	1.71	1.8	1.89	V
		V_{DD} pins with 3.3V supply	3.135	3.3	3.465	V
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage	Power ramps must be monotonic	-	-	10	ms

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.

2.4 APLL Phase Jitter

Table 6. APLL Phase Jitter [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[11:0] differential, APLL configured as synthesizer, XIN = 62.5MHz, VCO = 10.625GHz	156.25MHz	-	51	60	fs RMS
		312.5MHz	-	47	56	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the APLL has locked and settled.
4. All outputs enabled and generating clocks with the same frequency sourced from the APLL via integer output dividers.

2.5 FOD Phase Jitter

Table 7. FOD Phase Jitter [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{JIT}(\Phi)$	Random Phase Jitter (12kHz to 20MHz), OUT[3:0] and OUT[11:8] differential, APLL configured as a synthesizer, XIN = 60MHz, VCO = 10.86GHz	106.25MHz	-	100	165	fs RMS
		212.5MHz	-	82	97	
		425MHz	-	75	101	
		156.25MHz	-	100	165	
		312.5MHz	-	79	115	
		625MHz	-	68	97	

1. The device will meet specifications after thermal equilibrium has been reached.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the crystal interface.
3. Measured after the APLL has locked and settled.
4. All outputs enabled and generating clocks with the same frequency sourced from the same FOD.

2.6 Power Supply Noise Rejection

Table 8. Power Supply Noise Rejection [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
PSNR	Power supply rejection ratio V_{DDx} = 1.8V [2][3][4]	f_{NOISE} = 10kHz	-	-125	-	dBc
		f_{NOISE} = 25kHz	-	-127	-	
		f_{NOISE} = 50kHz	-	-117	-	
		f_{NOISE} = 100kHz	-	-99	-	
		f_{NOISE} = 250kHz	-	-92	-	
		f_{NOISE} = 500kHz	-	-80	-	
		f_{NOISE} = 1MHz	-	-81	-	

1. The device will meet specifications after thermal equilibrium is reached.
2. 100mV peak-to-peak sine wave applied to any V_{DDO}, excluding V_{DDO} of the output being measured and excluding V_{DD_VCO}.
3. Relative to 156.25MHz carrier frequency.
4. Measured on any differential output.

2.7 Crystal Oscillator Input and APLL AC/DC Electrical Characteristics

Table 9. Crystal Oscillator Input and Analog PLL AC/DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
-	Mode of oscillation	-	Fundamental			-
f_{IN}	Input Frequency	Using a crystal with APLL in Integer mode [1]	25	-	80	MHz
		Over-driving crystal interface, with APLL in Integer mode[1]	25	-	150	
		Using a crystal, with APLL not in Integer mode [2]	25		73	
		Over-driving crystal interface, with APLL not in Integer mode [2]	25		63	
V_{BIAS}	Bias point for XIN	Over-driving XIN input	-	0.6	-	V
V_{IVS}	Input voltage swing for XIN	Over-driving XIN input	0.6	-	1.2	V
C_T	Internal crystal oscillator tuning capacitance	xobuf_digicap_x1 = 0x0 xobuf_digcap_x2 = 0x0	-	8	-	pF
		xobuf_digicap_x1 = 0xF xobuf_digcap_x2 = 0xF	-	11.5[3]	-	
f_{VCO}	Analog PLL VCO Operating Frequency		9.7	-	10.75	GHz
F_{TOL}	Frequency Tolerance [4][5][6][7]	-40°C to 85°C	-450	-	450	PPM

1. APLL configured with integer_mode = 0x1. Note this configuration does not permit the APLL to be steered by the DCO.
2. APLL configured with integer_mode = 0x0, apll_fb_div_frac ≠ 0x0.
3. Capacitance increases by 0.25pF for each step of both xobuf_digicap_x1 and xobuf_digicap_x2.
4. F_{TOL} refers to the frequency accuracy of the Device Frequency Reference, either a crystal connected between XIN and XOUT, or an oscillator connected to XIN and overdriving the crystal interface. The APLL can reliably lock to a frequency reference that meets the F_{TOL} limits.
5. Inclusive of initial tolerance at 25°C, temperature stability, and aging.
6. The APLL frequency steering range ($\pm F_{STEER}$) available for a DCO to digitally steer the APLL is determined by the following expression: $F_{STEER} = |F_{TOL}| - |F_{ACC}|$; where F_{ACC} is the frequency accuracy of the device frequency reference. For example, if the frequency accuracy of the Device Frequency Reference is ±100PPM. then the APLL frequency steering range will be ±350PPM.
7. The frequency accuracy of the device frequency reference should be chosen to meet the free-running frequency requirements of the application, and to allow sufficient frequency steering range for a DCO to lock the APLL to its reference and to track reference noise. For more information, see Device Frequency Reference.

2.8 Recommended Crystal Characteristics

Table 10. Recommended Crystal Characteristics

Symbol	Parameter [1]	Condition	Minimum	Typical	Maximum	Unit
ESR	Equivalent Series Resistance	8pF ≤ C_L ≤ 12pF	-	-	50	Ω
C_O	Shunt Capacitance	-	-	-	4	pF
C_L	Load Capacitance	-	-	8	12	pF
Drive	Drive Level [2]	C_L = 8pF	-	-	160	µW
		C_L = 12pF	-	-	290	
F_{TOL}	Frequency Tolerance	-	See F_{TOL} in Table 9 and Device Frequency Reference			-

1. Specified by the crystal manufacturer.
2. Refers to power delivered by the oscillator circuit and dissipated in the crystal. The crystal must tolerate this drive level.

2.9 Output Frequencies and Start-Up Time

Table 11. Output Frequencies and Start-Up Time

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency for Clocks Sourced from the APLL	Differential Output	0.004	-	1000	MHz
		LVCMOS Output	0.004	-	250	
Δf_{OUT}	Output frequency tuning resolution	Fractional Output Divider	-	-	0.1	PPT
$t_{Start-up}$	Start-up time [1][2]	Synthesizer mode	-	-	9.9	ms

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected. Includes time needed to load a configuration from internal OTP.
2. Start-up time will depend on the actual configuration used. For more information, please contact Renesas Technical Support.

2.10 Output-to-Output Skew

Table 12. Output-to-Output Skew [1][2][3]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-output skew differential outputs [4][5]	Any two outputs within the same output bank	-	20	50	ps
		Any two outputs across all output banks from the same APLL or FOD source	-	40	70	ps
		Any two outputs across all output banks from different APLL or FOD sources	-	50	80	ps
	Output-to-output skew LVCMOS outputs [4][5]	Any two outputs within the same output bank	-	40	70	ps
		Any two outputs across all output banks from the same APLL or FOD source	-	60	90	ps
		Any two outputs across all output banks from different APLL or FOD sources	-	80	100	ps
Δt_{SK}	Output-to-output skew temperature variation [4]	Single device, at a fixed voltage, over temperature	-	0.30	2	ps/°C
	Output-to-output skew variation outputs [4]	Single device, over process, temperature, and voltage	-	2	4	ps

1. The device will meet specifications after thermal equilibrium has been reached.

2. Output bank 1 refers to OUT[3:0], output bank 2 refers to OUT[7:4], and output bank 3 refers to OUT[11:8].
3. Measured across the full operating temperature range.
4. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
5. This parameter is defined in accordance with JEDEC Standard 65.

2.11 LVCMOS Output AC/DC Characteristics

Table 13. LVCMOS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output high voltage [2]	I_{OH} = -2mA	V_{DDO} - 0.45	-	-	V
V_{OL}	Output low voltage [2]	I_{OL} = 2mA	-	-	0.45	V
V_{OH}	Output high voltage [2]	I_{OH} = -100µA	V_{DDO} - 0.2	-	-	V
V_{OL}	Output low voltage [2]	I_{OL} = 100µA	-	-	0.2	V
I_{OZ}	Output leakage current	Outputs tri-stated	-5	-	5	µA
Z_{OUTDC}	DC output impedance	At 25°C	-	46	-	Ω
t_R/t_F	Rise/Fall time 20% to 80%	-	133	200	310	ps
t_{DC}	Output duty cycle	-	45	50	55	%

1. Measured with outputs terminated with 50Ω to $V_{DDO}/2$.
2. These values are compliant with JESD8-7A.

2.12 LVDS Output AC/DC Characteristics

Table 14. LVDS Output AC/DC Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OD}	Output voltage swing [2]	out_cnf_lvds_amp = 0x0	156	377	526	mV
		out_cnf_lvds_amp = 0x1	336	456	594	mV
V_{OS}	Offset voltage	out_lvds_cm_voltage = 0x1	775	900	1025	mV
		out_lvds_cm_voltage = 0x2	875	1000	1125	
		out_lvds_cm_voltage = 0x3	975	1100	1225	
ΔV_{OS}	Change in V_{OS} between complimentary output states	-	5	20	50	mV
t_R/t_F	Rise/fall time 20% to 80%	out_cnf_lvds_amp = 0x0	73	125	190	ps
		out_cnf_lvds_amp = 0x1	80	135	200	
t_{DC}	Output duty cycle	-	45	50	55	%

1. Outputs terminated with 100Ω across OUTx and nOUTx.
2. Single-ended measurement.

2.13 HCSL Output AC/DC Characteristics

Table 15. HCSL Output AC/DC Characteristics [1]

Symbol	Parameter		Condition	Minimum	Typical	Maximum	Unit
V_{OVS} [2]	Output voltage swing	HCSL Mode (Amplitude boost off)	out_cnf_hcsl_swing = 0x0	177	213	248	mV
			out_cnf_hcsl_swing = 0x1	227	266	305	mV
			out_cnf_hcsl_swing = 0x2	271	321	370	mV
			out_cnf_hcsl_swing = 0x3	314	374	433	mV
			out_cnf_hcsl_swing = 0x4	358	430	500	mV
			out_cnf_hcsl_swing = 0x5	401	482	564	mV
			out_cnf_hcsl_swing = 0x6	447	537	626	mV
			out_cnf_hcsl_swing = 0x7	495	589	683	mV
			out_cnf_hcsl_swing = 0x8	550	641	733	mV
			out_cnf_hcsl_swing = 0x9	608	692	777	mV
			out_cnf_hcsl_swing = 0xA	657	742	827	mV
			out_cnf_hcsl_swing = 0xB	713	789	865	mV
			out_cnf_hcsl_swing = 0xC	752	834	915	mV
			out_cnf_hcsl_swing = 0xD	767	875	983	mV
			out_cnf_hcsl_swing = 0xE	778	913	1047	mV
			out_cnf_hcsl_swing = 0xF	789	946	1102	mV
		HCSL Mode (Amplitude boost on)	out_cnf_hcsl_swing = 0xF	812	1085	1359	mV
t_R/t_F	Rise/fall time 20% to 80%	out_cnf_hcsl_swing = Any		105	161	225	ps
t_{DC}	Output duty cycle			47	50	52	%

1. Outputs terminated with 50Ω to GND on each OUTx and nOUTx pin.
2. Peak-to-peak output voltage swing on each OUTx and nOUTx pin.

2.14 Power Supply Current

Table 16. Power Supply Current [1]

Symbol	Parameter	Condition	Typical	Maximum	Unit
I_{DDD33_SERIAL}	Supply current for V_{DDD33_SERIAL}	-	0.5	1	mA
I_{DDXO_DCD}	Supply current for V_{DDXO_DCO}	V_{DDXO_DCD} = 1.89V	45	86	mA
I_{DD_VCO}	Supply current for V_{DD_VCO}	V_{DD_VCO} = 1.89V	230	260	mA
I_{DDD33_DIA}	Supply current for V_{DDD33_DIA}	V_{DDD33_DIA} = 1.89V or 3.465V All FODs off $I_{DD\_FODDIGBASE}$	52	69	mA
		V_{DDD33_DIA} = 1.89V or 3.465V Current adder for one FOD at 120MHz $I_{DD\_PERFODDIG}$	7	11	
		V_{DDD33_DIA} = 1.89V or 3.465V Current adder for one FOD per 100MHz over 120MHz $I_{DD\_FODDIGPERMHZ}$	1	2	

Table 16. Power Supply Current [1] (Cont.)

Symbol	Parameter	Condition		Typical	Maximum	Unit
$I_{DD\_FODxADD}$ [2]	Supply current adder for V_{DDO1_FOD0}, V_{DD_FOD0}, V_{DDO8_FOD1}, V_{DDO9_FOD2}, V_{DDO10_FOD2}	V_{DDOx_FODx} = 1.89V Current adder with FOD off. $I_{DD\_FODBASE}$		0.02	0.1	mA
		V_{DDOx_FODx} = 1.89V Current adder with FOD at 120MHz. I_{DD_PERFOD}		34	38	
		V_{DDOx_FODx} = 1.89V Current adder for FOD per 100MHz over 120MHz. $I_{DD\_FODPERMHZ}$		0.9	1.3	
	Supply current adder for V_{DDO9_FOD2}, V_{DDO10_FOD2}	V_{DDOx_FODx} = 1.89V Current adder for FOD calibration with any FOD on.		7.7	8.8	
I_{DDOx} [3]	Supply current for V_{DDOx}	HCSL mode (Amplitude boost off)	out_cnf_hcsl_swing = 0x0	20	29	mA
			out_cnf_hcsl_swing = 0x1	21	31	
			out_cnf_hcsl_swing = 0x2	22	33	
			out_cnf_hcsl_swing = 0x3	23	34	
			out_cnf_hcsl_swing = 0x4	24	36	
			out_cnf_hcsl_swing = 0x5	25	38	
			out_cnf_hcsl_swing = 0x6	26	39	
			out_cnf_hcsl_swing = 0x7	27	40	
			out_cnf_hcsl_swing = 0x8	28	41	
			out_cnf_hcsl_swing = 0x9	29	41	
			out_cnf_hcsl_swing = 0xA	30	41	
			out_cnf_hcsl_swing = 0xB	31	41	
			out_cnf_hcsl_swing = 0xC	32	41	
			out_cnf_hcsl_swing = 0xD	33	42	
			out_cnf_hcsl_swing = 0xE	34	45	
			out_cnf_hcsl_swing = 0xF	35	47	
I_{DDOx} [3]	Supply current for V_{DDOx}	HCSL mode (Amplitude boost on)	out_cnf_hcsl_swing = 0xF	42	59	mA
I_{DDOx} [3]	Supply current for V_{DDOx}	LVDS mode	out_cnf_lvds_amp = 0x0	18	30	mA
			out_cnf_lvds_amp = 0x1	27	35	
I_{DDOx} [3]	Supply current for V_{DDOx}	LVCMOS mode	One output	26	33	mA
			Two outputs	35	42	
I_{DDOx} [3]	Supply current for V_{DDOx}	Output powered down [4][5][6]		4	7	mA
		Output Hi-Z		14	19	
		Output disabled		14	19	

1. Internal dynamic switching current at maximum f_{OUT} is included, unless otherwise noted.
2. Added to supply current for V_{DDO1_FOD0}, V_{DD_FOD0}, V_{DDO8_FOD1}, V_{DDO9_FOD2}, V_{DDO10_FOD2} according to the conditions for the FOD supplied by the pin.
3. Values do not include $I_{DD\_FODxADD}$.
4. OUT[11:0] are powered down by setting: out_en_bias = 0x0, out_dis_state = 0x3, and out_driver_en = 0x0.
5. IOD[3:0] and IOD[11:8] are powered down by setting: iod_apll_vco_fanout_en = 0x0, iod_mux_sel = 0x7, and iod_enable = 0x0.
6. IOD[7:4] are powered down by setting: iod_apll_vco_fanout_en = 0x0 and iod_enable = 0x0.

2.15 GPIO and Serial Port DC Electrical Characteristics

Table 17. GPIO and Serial Port DC Electrical Characteristics [1][2][3][4]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	-	0.77 × V_{DDx}	-	V_{DDx} + 0.3	V
V_{IL}	Input low voltage	-	-0.3	-	0.31 × V_{DDx}	V
V_{OH}	Output high voltage	I_{OH} = -2mA	V_{DDx} - 0.45	-	V_{DDx} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2mA	-	-	0.45	V
V_{OH}	Output high voltage	I_{OH} = -100µA	V_{DDx} - 0.2	-	V_{DDX} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 100µA	-	-	0.2	V

1. Applies to GPIOx, nMR, nCS_A0, SCL_SCLK, SCA_SDIO, and SDO_A1.
2. Input specifications refer to pins acting as inputs, output specifications refer to pins acting as outputs.
3. V_{DDx} refers to the V_{DDOx} or V_{DDD33_SERIAL} supply powering the GPIO or serial port (see Pin Assignments).
4. Values are compliant with JESD8-7A.

2.16 CMOS GPIO and Serial Port Common Electrical Characteristics

Table 18. CMOS GPIO Common Electrical Characteristics [1][2][3]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{IL}	Input leakage current	Does not include input pull-up/pull-down resistor current. V_{IL} = 0V, V_{IH} = V_{DDX}	-15	-	15	µA
R_P	Pull-up/pull-down resistor	If enabled	-	53	-	kΩ

1. Applies to GPIOx, nMR, nCS_A0, SCL_SCLK, SCA_SDIO, and SDO_A1.
2. Input specifications refer to pins acting as inputs, output specifications refer to pins acting as outputs.
3. V_{DDx} refers to the V_{DDOx} or V_{DDD33_SERIAL} supply powering the GPIO or serial port (see Pin Assignments).

2.17 I²C Bus Slave Timing Diagram

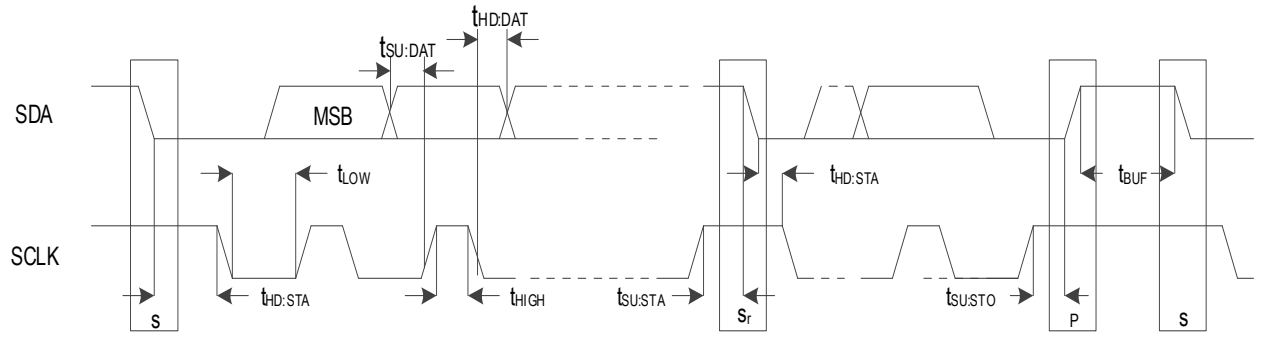


Figure 4. I²C Bus Slave Timing Diagram

2.18 I²C Bus Slave Timing Characteristics

Table 19. I²C Bus Slave Timing Characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCL}	SCL clock frequency	-	10	1000	kHz
$t_{HD:STA}$	Hold time after (REPEATED) START Condition	-	0.26	-	µs
t_{LOW}	Clock low period	-	0.5	-	µs
t_{HIGH}	Clock high period	-	0.26	-	µs
$t_{SU:STA}$	REPEATED START Condition setup time	-	0.26	-	µs
$t_{HD:DAT}$	Data hold time	-	0	-	ns
$t_{SU:DAT}$	Data setup time	-	50	-	ns
$t_{SU:STO}$	STOP condition setup time	-	0.26	-	µs
t_{BUF}	Bus free time between STOP and START Condition	-	0.5	-	µs
t_{SPIKE}	Noise spike suppression time [1]	i2c_spike_fltr = 0x3	-	50	ns

1. Device rejects noise spikes of a duration up to the maximum specified value.

2.19 I²C Bus AC/DC Electrical Characteristics

Table 20. I²C Bus AC/DC Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	High-level input voltage for SCL_SCLK and SDA_nCS	-	0.8 × V_{DDD33}	-	-	V
V_{IL}	Low-level input voltage for SCL_SCLK and SDA_nCS	-	-	-	0.3 × V_{DDD33}	V
V_{HYS}	Hysteresis of Schmitt trigger inputs	-	0.05 × V_{DDD33}	-	-	V
V_{OL}	Low-level output voltage for SCL_SCLK and SDA_nCS	I_{OL} = 2mA	-	-	0.4	V
I_{IN}	Input leakage current per pin	-	[2]	-	[2]	µA

1. VOH is governed by the VPUP, the voltage rail to which the pull-up resistors are connected.
2. See CMOS GPI/GPIO Common Electrical Characteristics in Table 18.

2.20 SPI Slave Timing Diagrams

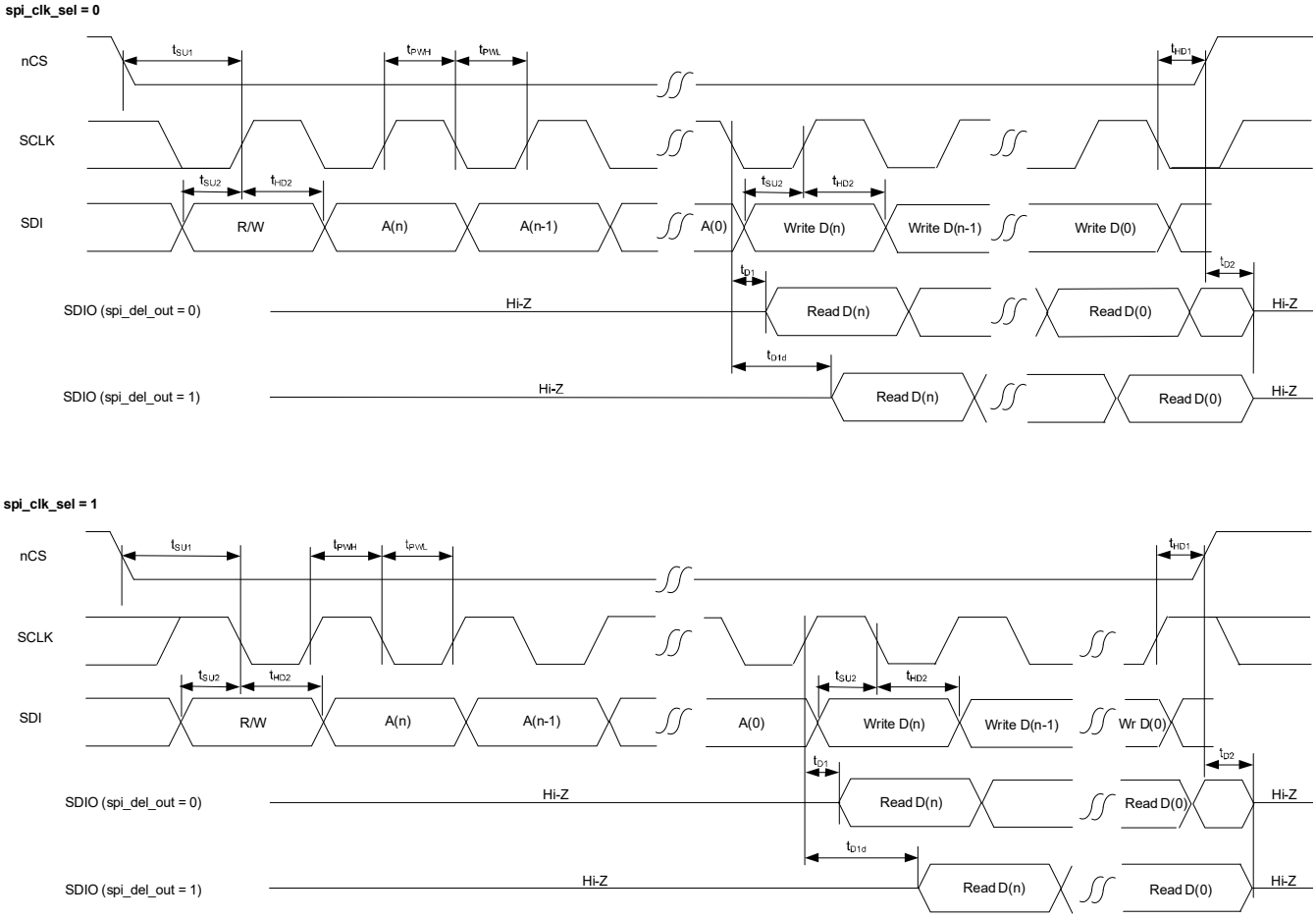


Figure 5. SPI Slave Timing Diagrams

2.21 SPI Slave Timing Characteristics

Table 21. SPI Slave Timing Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{MAX}	Maximum operating frequency	0.1	-	20	MHz
t_{PWH}	SCLK pulse width high	14	-	-	ns
t_{PWL}	SCLK pulse width low	14	-	-	ns
t_{SU1}	nCS setup time to SCLK rising or falling edge	10	-	-	ns
t_{HD1}	nCS hold time from SCLK rising or falling edge	2	-	-	ns
t_{SU2}	SDIO setup time to SCLK rising or falling edge	4	-	-	ns
t_{HD2}	SDIO hold time from SCLK rising or falling edge	3	-	-	ns
t_{D1}	Read data valid time from SCLK rising or falling edge	4.7	-	7.4	ns
t_{D2}	SDIO read data Hi-Z time from CS high [1]	0	-	14.5	ns

1. This is the time until the device releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

3. Functional Description

3.1 Overview

The RC22312/22308 is an ultra-low phase noise multi-frequency synthesizer and digitally controlled oscillator (DCO). This flexible, low-power device outputs clocks with 50fs RMS (12kHz to 20MHz) jitter supporting SerDes operating at rates up to 112Gbps and 25fs RMS (12kHz to 20MHz with 4MHz high pass filter) supporting SerDes operating at 224Gbps.

The RC22312 has 12 differential clock outputs, see Figure 2. The RC22308 has eight differential clock outputs, see Figure 3. Both devices provide a DCO with an ultra-low phase noise analog PLL (APLL) based clock synthesizer and three fractional output divider (FOD) based clock synthesizers.

The differential outputs can be configured as LVDS or HCSL (AC-LVPECL). When configured for LVDS or HCSL (AC-LVPECL), the differential outputs can operate at frequencies up to 1GHz. Each differential output can be configured as two LVCMOS outputs that can operate at frequencies up to 250MHz.

3.2 Device Frequency Reference

The RC22312, RC22308 requires a device frequency reference. The frequency reference must support the phase noise, frequency accuracy, and frequency stability requirements of the intended application.

The frequency reference can be implemented using an external crystal resonator connected between the XIN and XOUT pins and the device oscillator circuitry. Alternatively, an external oscillator can be connected to the XIN pin to overdrive the internal oscillator circuitry.

If a crystal resonator is used for the frequency reference, the resonant frequency must be from 25MHz to 80MHz. If an external oscillator is used, it must provide a low-phase noise clock with frequency from 25MHz to 150MHz. For frequency reference requirements, see Table 9 and Table 10.

For all applications, the phase noise of the frequency reference, after filtering by the APLL, is the minimum phase noise that will appear on all clocks output by the device.

For DCO and synthesizer applications, the accuracy of the frequency reference determines the frequency accuracy of the free-running clocks. For DCO applications, the stability of the frequency reference determines the stability of the DCO clocks when a source of synchronization is not available, and it affects the lowest filtering bandwidth that a filtering algorithm can support.

The accuracy of the frequency reference should be chosen to meet the free-running frequency accuracy requirements of the application (see Table 22 for examples) and to allow sufficient APLL frequency steering range for a DCO to lock the APLL to its reference and to track reference noise.

The available APLL frequency steering range ($\pm F_{STEER}$) is determined by the following expression: $F_{STEER} = |F_{TOL}| - |F_{ACC}|$; where F_{ACC} is the accuracy of the frequency reference. For the value of F_{TOL} and for additional details, see Table 9.

Table 22. Recommended Free-Running Frequency Accuracy by Application

Application	Recommended Free-Running Frequency Accuracy (PPM)
PCIe Free-running clock synthesizer	±100
Most Ethernet types Free-running clock synthesizer	±100
800GBASE-xR8, 10GBASE-T Free-running clock synthesizer	±50
100GBASE-ZR, 10GBASE-W Free-running clock synthesizer	±20

3.3 Analog PLL

The internal APLL locks to the device oscillator and synthesizes an ultra-low phase noise clock of virtually any frequency between 9.70GHz and 10.75GHz.

The APLL is the primary synthesizer for the DCO and its fractional frequency offset (FFO) can be steered by the DCO.

The APLL output clock is pre-divided by 2 and is available to the integer output dividers (IOD). The pre-divided APLL clock is available directly to IOD[7:4]; it is also available via cross-connect to IOD[3:0] and IOD[11:8]. The undivided APLL clock is supplied to FOD[2:0].

3.4 Integer Output Dividers

Each IOD divides its input clock by a programmable 21-bit integer value.

3.5 Fractional Output Dividers

The FODs divide the APLL clock to synthesize low phase noise clocks with programmable frequencies from 120MHz to 700MHz. The FODs are capable of integer division, rational division (i.e., M/N), and fractional division with 1 part per trillion frequency resolution. The FOD output clocks are available, via cross-connect, to IOD[3:0] and IOD[11:8].

When configured for fractional division, the FODs can operate as DCOs with steering range of ±244PPM. The FODs can be configured to cancel frequency adjustments made by the DCO to the APLL via the Combo Bus so that their output frequencies are virtually unaffected by the DPLL.

3.6 Divider Synchronization

The IODs are synchronized. The rising edges of clocks from these dividers will be aligned for every Nth rising edge of the APLL clock, where N is the lowest common multiple of the accumulated divide ratios along the paths from the APLL to the divider outputs.

Consider the following example: The APLL is operating at 10GHz. The pre-divider supplies a 5GHz clock to IOD1 and IOD2. IOD1 uses a divide ratio of 40 to produce a 125MHz clock and IOD2 uses a divide ratio of 625,000 to produce an 8kHz clock. In this example, the lowest common multiple of the divisors along the three paths is 625,000. Therefore the outputs of IOD1 and IOD2 will be aligned once for every 625,000 edges of the 10GHz clock. In other words, the 8kHz and the 125MHz clocks will be aligned for every edge of the 8kHz output clock.

3.7 Clock Output Enable

The RC22312, RC22308 enables and disables clock outputs synchronously to ensure there are no runt pulses during clock output enable and disable operations.

Clock output enables can be controlled by software using the global_oe and out_driver_en register fields. Alternatively, GPIOs can be assigned the clock output enable function using the oe_source_sel and gpio_func register fields. For more information, see the *RC22312, RC22308 Programming Guide*.

When a GPIO is assigned an output enable function it should be configured with gpio_resync = 0x0 and gpio_deglitch_bypass = 0x1; this disables GPIO resynchronization and bypasses the GPIO deglitcher ensuring lowest latency. When so configured, the maximum time delay from the time the voltage level on a GPIO input changes state until the clock output is enabled or disabled is 14ns plus 4 periods of the output clock.

3.8 Status and Control

All control and status registers are accessed through a 1MHz I^2C or 20MHz SPI slave microprocessor interface. The device can automatically load a configuration from internal one time programmable (OTP) memory. Alternatively, the I^2C master interface can automatically load a configuration from an external EEPROM after reset.

Note: For registers information, contact Renesas Technical Support.

4. Applications Information

4.1 Power Considerations

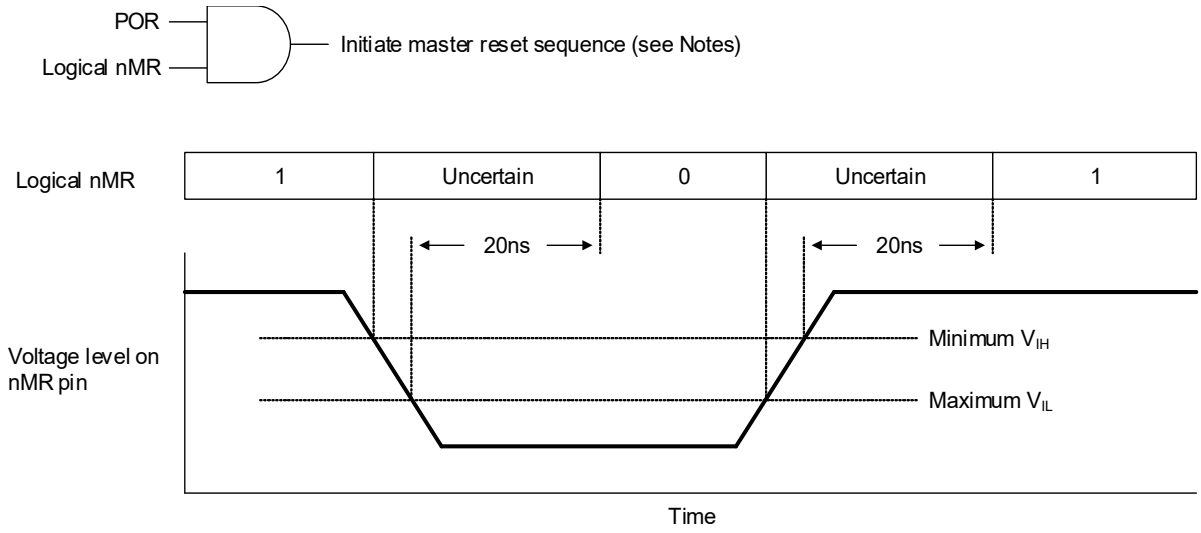
There are no power supply sequencing requirements; however, if V_{DDOx} or V_{DD_CLK} reach 90% of V_{DD} nominal after the later of V_{DD_VCO} or V_{DDD33_DIA} then a soft reset or a master reset must be initiated to ensure the output dividers are synchronized.

For power and current consumption calculations, see the Renesas IC Toolbox (RICBox) software tool.

4.2 Power-On Reset and Reset Controller

Upon power-up, an internal power-on reset (POR) signal is asserted 5ms after both the V_{DDXO_DCD} and V_{DDD33_DIA} supplies reach 90% of V_{DD} nominal. The first master reset sequence is initiated when POR is asserted and the voltage level on the nMR pin is high.

After the first master reset sequence is initiated, another master reset sequence can be initiated by taking the voltage level on the nMR pin low and then high while POR remains asserted (see Figure 6). To ensure a master reset sequence is initiated, the voltage level on the nMR pin must be held low for at least 20ns before transitioning high. To ensure deterministic behavior, voltage level transitions on the nMR pin must be monotonic between minimum V_{IH} and maximum V_{IL} (see Table 17).



Notes:
- Requires 1 from logical nMR for the first master reset sequence
- Requires 0 to 1 transition from logical nMR after the first master reset sequence has been initiated

Figure 6. Master Reset Sequence Initiation

The nMR pin has an internal pull-up that can be left to float, or it can optionally be externally pulled high or low. If nMR is high when the internal POR is asserted, the reset controller will initiate a master reset sequence. If nMR is low when the internal POR is asserted, the reset controller will not initiate a master reset sequence until nMR is taken high.

During the master reset sequence, all clock outputs are optionally disabled depending on the value of the out_startup register field. Disabled outputs behave according to the associated out_dis_state register field.

The serial ports are accessible when the device_ready_sts register bit is set to 0x1. Any GPIO can be configured to indicate the state of the device_ready_sts register bit by setting the associated gpio_func register field to 0x18. When a reset sequence completes, the rst_done_sts register bit is set to 0x1.

When a configuration is loaded from EEPROM, the voltage level on the nMR pin must be held high from the time a master reset sequence is initiated until after the EEPROM transactions have completed, as indicated when the device_ready_sts register bit is set to 0x1.

4.3 Recommendations for Unused Input and Output Pins

4.3.1 LVCMOS Control Pins

LVCMOS control pins have internal pull-up resistors. Additional 1kΩ pull-up resistors can be added but are not required.

4.3.2 LVCMOS Output Pins

Unused LVCMOS outputs must be left to float; Renesas recommends that no trace should be attached. Unused LVCMOS outputs should be configured to a high-impedance state to prevent noise generation.

4.3.3 Differential Output Pins

Unused differential outputs must be left to float; Renesas recommends that no trace should be attached. Both sides of a differential output pair should be either left to float or terminated.

4.4 Overdriving the Crystal Interface

When overdriving the crystal interface, the XOUT pin is left to float and the XIN input is overdriven by an AC coupled LVCMOS driver, or by one side of an AC coupled differential driver. The XIN pin is internally biased to 0.6V. The voltage swing on XIN should be between 0.5V peak-to-peak and 1.2V peak-to-peak, and the slew rate should not be less than 0.6V/ns.

Figure 7 shows an LVCMOS driver overdriving the XIN pin. For this implementation, the voltage swing at XIN will equal $V_{DD} \times R_1 / (R_O + R_S + R_1)$. The values of V_{DD}, R_S, and R_1 should be selected so that the voltage swing at XIN is below 1.2V peak-to-peak.

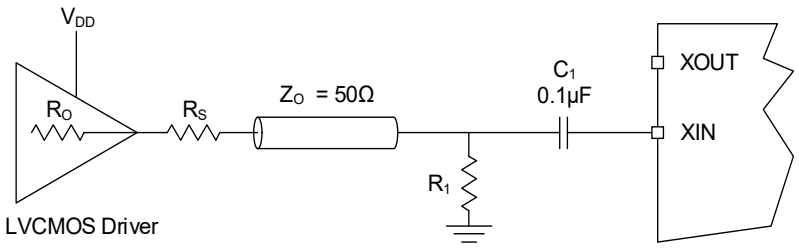


Figure 7. LVCMOS Driver to Crystal Input Interface

Figure 8 shows one side of an LVPECL driver overdriving the XIN pin.

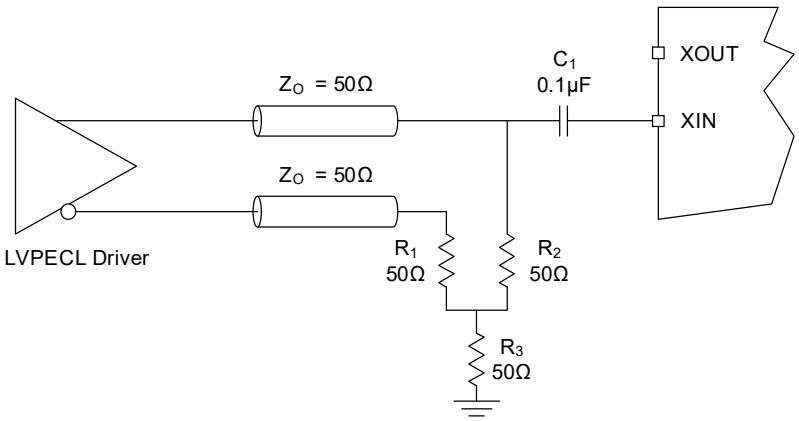


Figure 8. LVPECL Driver to Crystal Input Interface

4.5 Differential Output Termination

The RC22312, RC22308 programmable differential clock outputs support HCSL and LVDS. Receivers that support HCSL or LVDS can be direct-coupled with RC22312, RC22308 outputs. Differential receiver types other than HCSL or LVDS can be AC-coupled.

The RC22312, RC22308 HCSL clock outputs support selectable internal termination resistors as shown in Figure 9. The value of resistors $R_{O1\ and}$ R_{O2} is 50Ω.

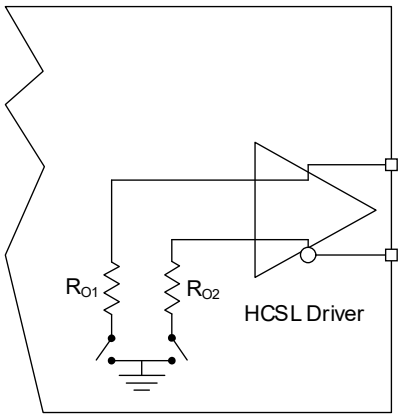


Figure 9. Internal Termination Resistors for Differential Drivers

Note: Some receivers are equipped with internal terminations that can include the following: trace termination, voltage biasing, and AC-coupling. Consult with the receiver specifications to determine if the termination components shown in this section are needed.

4.5.1 Direct-Coupled HCSL Terminations

For HCSL receivers, RC22312, RC22308 clock outputs should be configured for HCSL, and the devices should be direct-coupled. The RC22312, RC22308 supports a wide range of programmable HCSL voltage swing options.

Figure 10 shows an HCSL driver direct-coupled with an HCSL receiver and configured for internal termination. The RC22312, RC22308 supports source termination, with internal 50Ω resistors to ground at the transmitter. Resistor R_1 is optional and is used to improve impedance matching. If R_1 is used, it will reduce the amplitude at the receiver by 50% – this can be mitigated by adjusting the output amplitude of the driver.

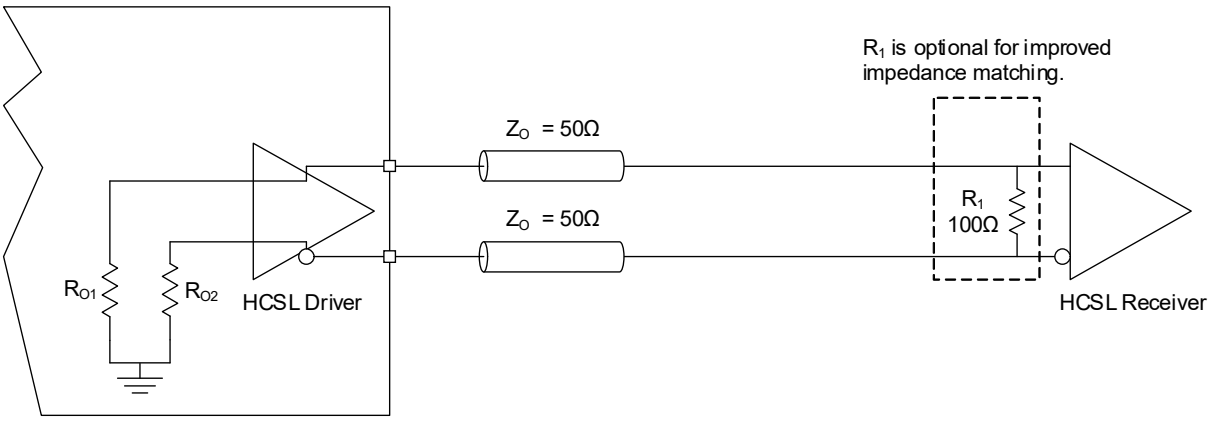


Figure 10. HCSL Internal Termination

Figure 11 shows an HCSL driver direct-coupled with an HCSL receiver and configured for external termination. If the HCSL receiver has an internal 100Ω termination resistor then it will reduce the signal amplitude at the receiver by 50% – this can be mitigated by adjusting the output amplitude of the driver.

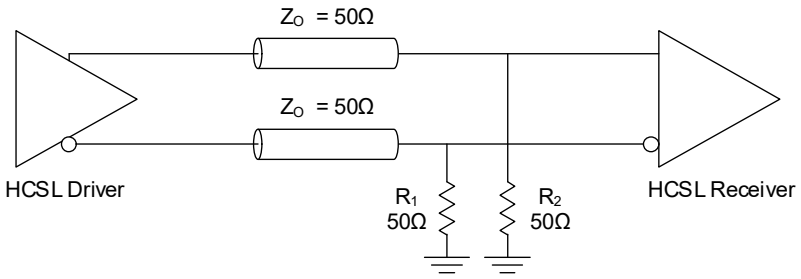


Figure 11. HCSL External Termination

For alternative termination schemes, see HCSL Terminations in *Quick Guide - Output Terminations* located on the RC32312/RC32308 product page, or contact Renesas for support.

4.5.2 Direct-Coupled LVDS Termination

For LVDS receivers, RC22312, RC22308 clock outputs should be configured for LVDS, and should be direct-coupled. The RC22312, RC22308 supports several programmable LVDS voltage swing and common mode options.

Figure 12 shows an LVDS driver direct-coupled with an LVDS receiver. The recommended value for the termination resistor (R_1) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of the transmission line. To avoid transmission-line reflection issues, R_1 should be surface-mounted and placed as close to the receiver as practical.

For alternative termination schemes, see LVDS Terminations in *Quick Guide - Output Terminations* located on the RC32312/RC32308 product page, or contact Renesas for support.

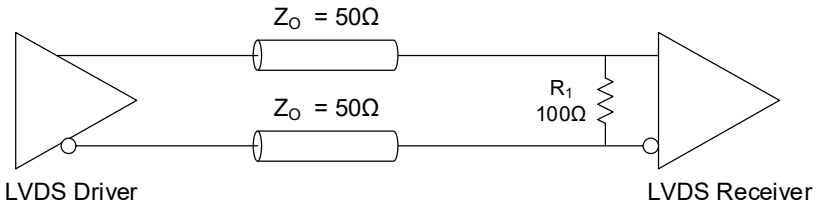


Figure 12. LVDS Termination

4.5.3 AC-Coupled Differential Termination

For AC-coupled differential terminations, the RC22312, RC22308 clock outputs should be configured for HCSL and the HCSL driver should be configured with a voltage swing appropriate for the receiver. The RC22312, RC22308 supports several programmable HCSL voltage swing options.

Figure 13 shows an HCSL driver configured for internal termination and AC-coupled with a differential receiver with external termination resistors and biasing. Resistors R_1, R_2, R_3, and R_4 should be selected to provide the appropriate bias voltage for the receiver. Consult receiver specifications for input swing and bias requirements. An optional resistor (R_5) can be used to improve impedance matching. If R_5 is used, it will reduce the amplitude at the receiver by 50%; this can be mitigated by adjusting the output amplitude of the driver.

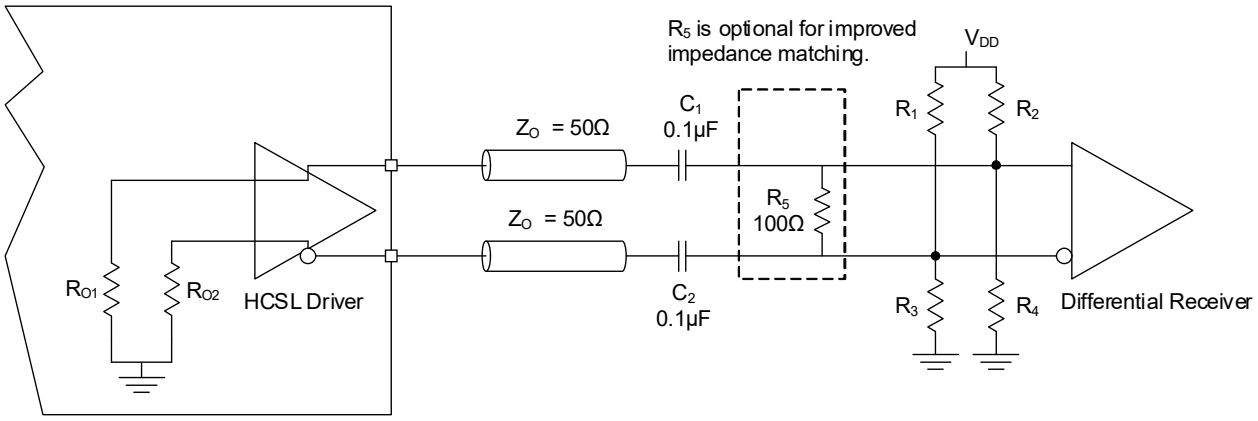


Figure 13. AC-Coupled Differential Termination

For more information on AC-coupling, see Renesas application note AN-953, *Quick Guide - Output Terminations*.

4.5.4 AC-Coupled LVPECL (AC-LVPECL) Termination

AC-coupling should be used for LVPECL receivers. For AC-coupled LVPECL (AC-LVPECL) terminations, the RC22312, RC22308 clock outputs should be configured for HCSL. The RC22312, RC22308 supports several programmable HCSL voltage swing options and it should be configured as appropriate for the receiver and termination scheme. Consult receiver specifications for input swing and bias requirements.

Figure 14 shows an HCSL driver configured for internal termination driving an AC-LVPECL receiver with internal termination resistors and biasing.

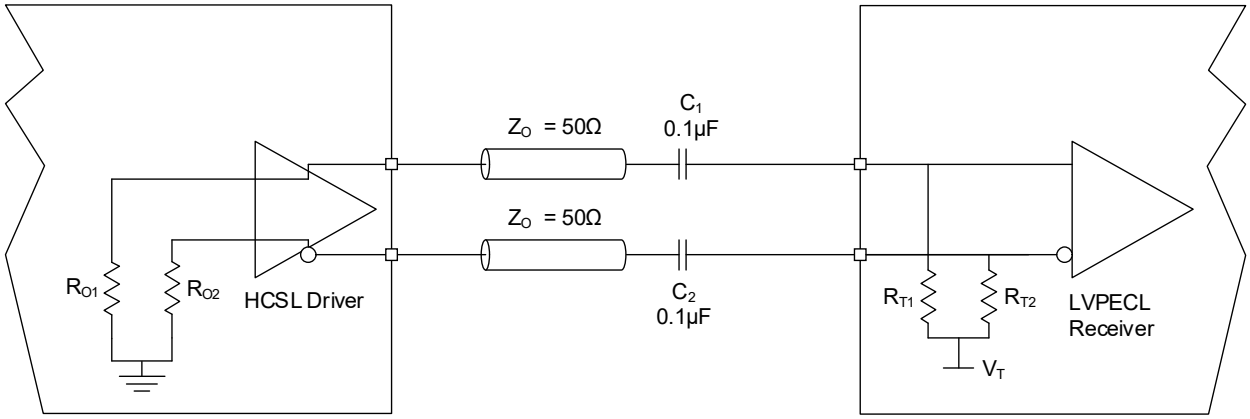


Figure 14. AC-LVPECL Termination for LVPECL Receiver with Internal Termination Resistors and Biasing

For more information on AC-coupling, see Renesas application note AN-953, *Quick Guide - Output Terminations*.

5. Package Outline Drawings

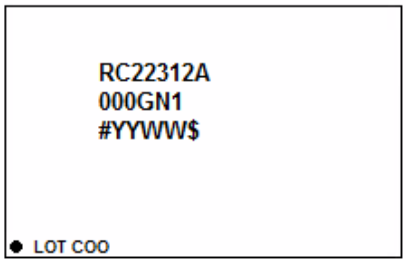
The package outline drawings are located at the end of this document. The package information is the most current data available.

6. Device ID Register

Device	Device_ID (Base Address 0x02)
RC22308	0x85C1
RC22312	0x85C2

7. Marking Diagram

- Lines 1 and 2 are the part number.
- Line 3:
  - "#" denotes the stepping number.
  - "YYWW" denotes the last two digits of the year and the work week the part was assembled.
  - "$" denotes the mark code.



- Lines 1 and 2 are the part number.
- Line 3:
  - "#" denotes the stepping number.
  - "YYWW" denotes the last two digits of the year and the work week the part was assembled.
  - "$" denotes the mark code.

8. Ordering Information

Part Number [1]	Package Description	Carrier Type	Temperature Range
RC22308AxxxGNE#KB0	48-VFQFPN, 7 × 7 mm	Tape	-40 to +85°C
RC22308AxxxGNE#BB0	48-VFQFPN, 7 × 7 mm	Tray	
RC22312AxxxGN1#KB0	64-VFQFPN, 9 × 9 mm	Tape	-40 to +85°C
RC22312AxxxGN1#BB0	64-VFQFPN, 9 × 9 mm	Tray	

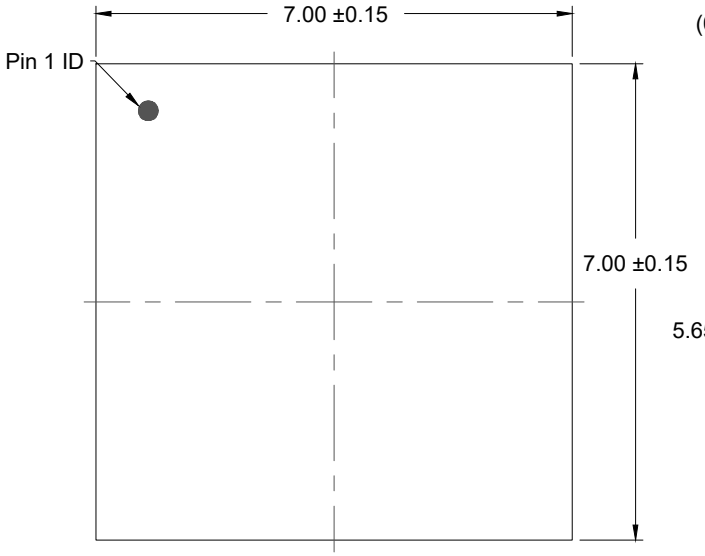
1. Replace "xxx" in the part number with the desired preprogrammed configuration code provided by Renesas in response to a custom configuration request or use "000" for unprogrammed parts.

9. Revision History

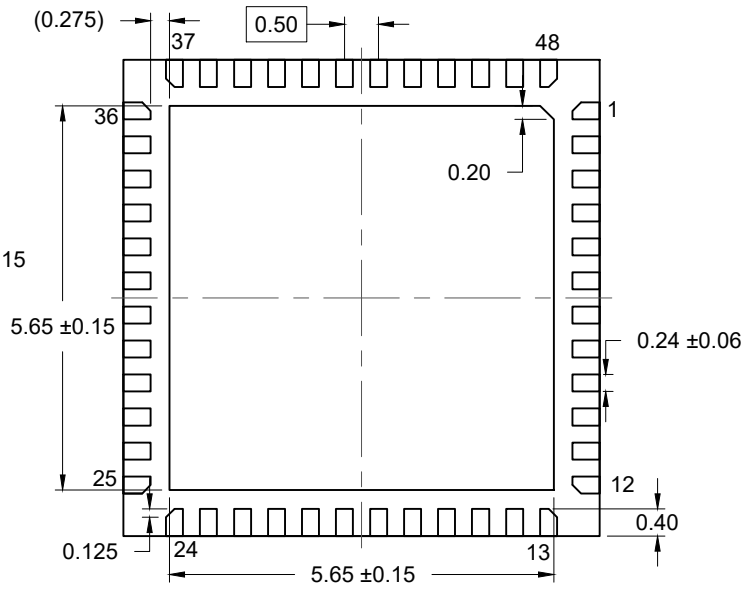
Revision	Date	Description
1.15	Dec 19, 2024	▪ Changed the maximum time delay number in Clock Output Enable to 14ns from 13ns.
1.14	Dec 16, 2024	▪ Added Clock Output Enable.
1.13	Oct 11, 2024	▪ Updated footnote 2 in Table 14. ▪ Complete other minor changes.
1.12	Aug 27, 2024	▪ Updated the minimum and maximum values for “Load Capacitance” in Table 10. Also added a footnote to the parameter. ▪ Updated the footnote associated with “Drive Level” in Table 10.
1.11	Jul 9, 2024	▪ Updated Table 21.
1.10	Jul 5, 2024	▪ Updated the description of V_{DDO9_FOD2} and V_{DDO10_FOD2} in Table 1. ▪ Updated the following specification tables: Table 9, Table 10, Table 15, Table 16, Table 19, and Table 21. ▪ Updated Device Frequency Reference. ▪ Updated AC-Coupled Differential Termination. ▪ Added AC-Coupled LVPECL (AC-LVPECL) Termination. ▪ Completed other minor changes.
1.09	May 17, 2024	▪ Updated the nMR, nCS_A0, SCL_SCLK, SDA_SDIO, and SDO_A1 pins in Table 1. ▪ Updated Table 17 and Table 18.
1.08	Apr 9, 2024	▪ Completed minor changes.
1.07	Apr 2, 2024	▪ Updated Figure 2 and Figure 3.
1.06	Mar 28, 2024	▪ Updated Figure 2, Figure 3, and Figure 5.
1.05	Mar 15, 2024	▪ Updated the nMR, nCS_A0, SCL_SCLK, SDA_SDIO and SDO_A1 pins in Table 1. ▪ Updated footnote 1 in Table 18. ▪ Updated Power-On Reset and Reset Controller section. ▪ Updated footnotes 3 and 4 and added footnote 5 in Table 15. ▪ Moved Soft Reset section to the *RC22312, RC22308 Programming Guide*. ▪ Completed other minor changes.
1.04	Feb 28, 2024	▪ Updated the description of the LOCK pin in Table 1. ▪ Updated the frequency tolerance values in Table 9. ▪ Updated footnotes 1 and 2 in Table 15. ▪ Updated Power Considerations. ▪ Added two new sections, Power-On Reset and Reset Controller and Soft Reset. ▪ Updated the slew rate in Overdriving the Crystal Interface.
1.03	Jan 24, 2024	▪ Updated Table 5 and Table 15. ▪ Updated the second paragraph of Overdriving the Crystal Interface.
1.02	Dec 6, 2023	▪ Updated Table 8 and Table 9. ▪ Updated the second paragraph of Overdriving the Crystal Interface.
1.01	Nov 21, 2023	▪ Updated the footnotes in Table 6. ▪ Reformatted Table 7 and updated its footnotes. ▪ Updated the footnotes in Table 8. ▪ Separated Table 8 into Table 9 and Table 9. ▪ Updated the footnotes in Table 11 to Table 12. ▪ Updated Table 13 to Table 15 and their footnotes.
1.00	Oct 20, 2023	Initial release.

Package Outline Drawing

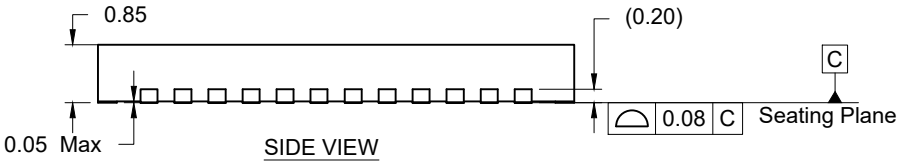
PSC-4203-01
NLG48P1
48-VFQFPN 7.0 x 7.0 x 0.85 mm Body, 0.5mm Pitch
Rev.04, Date Created: Mar 21, 2025



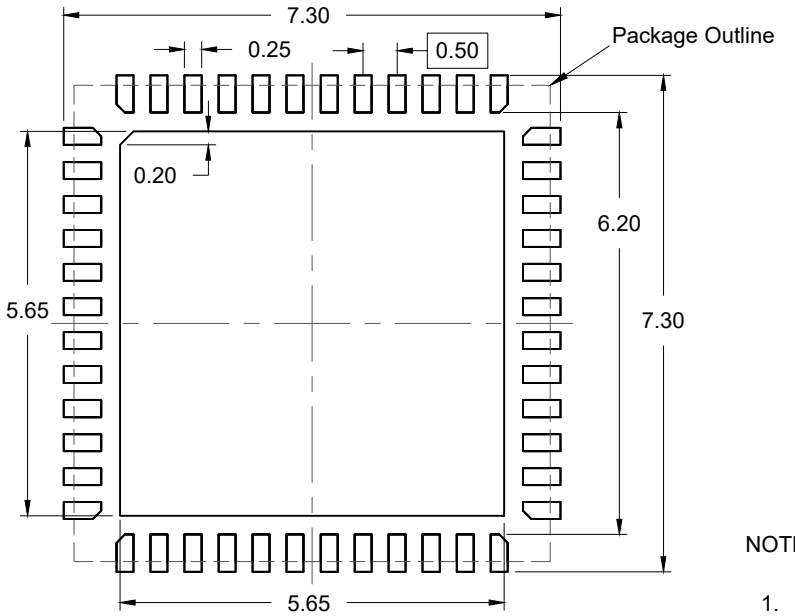
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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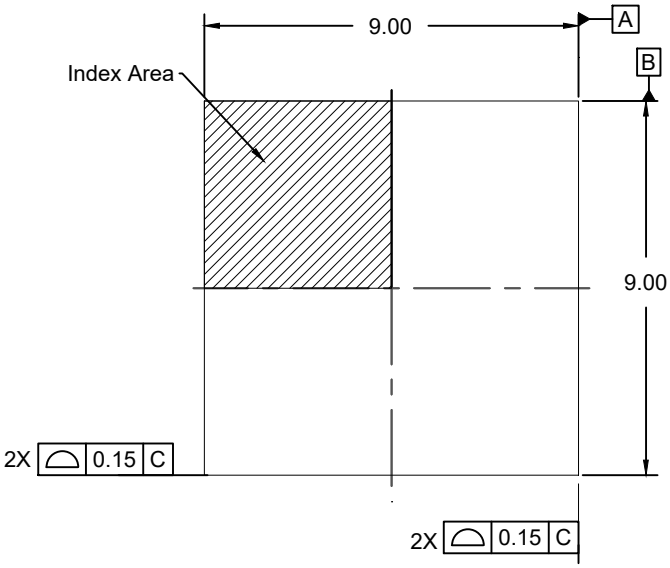
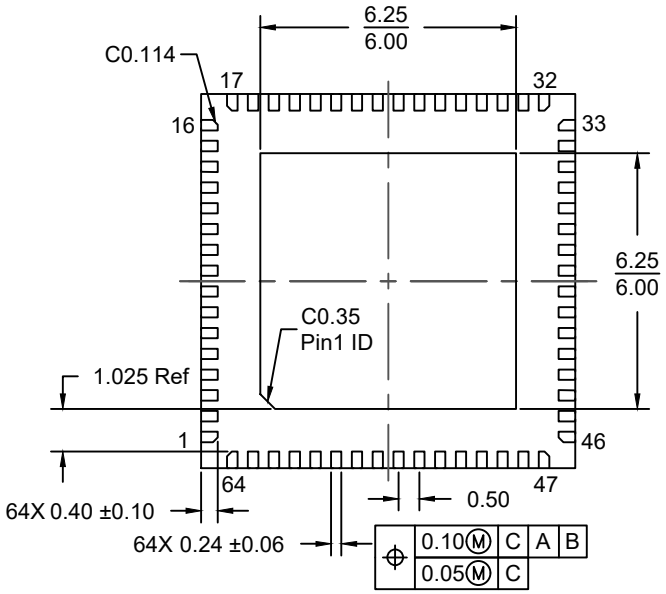
Package Outline Drawing

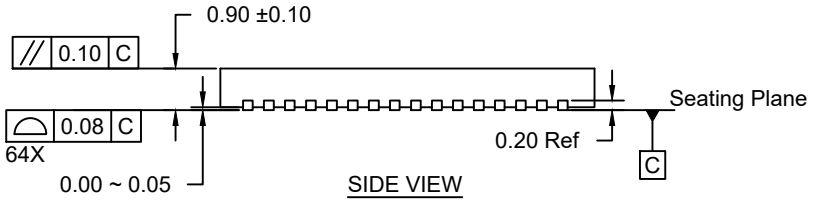
Package Code: NLG64P2
64-VFQFPN 9.0 x 9.0 x 0.9 mm Body, 0.50mm Pitch
PSC-4147-02, Revision: 03, Date Created: Jun 23, 2022



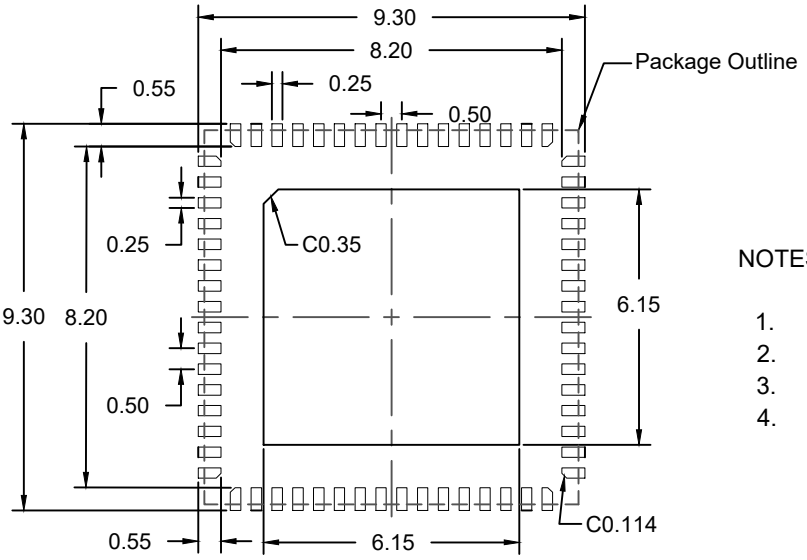
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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