RBE034N15R1SZQ4

REXFET-1 N-Channel Power MOSFET

150 V - 200 A - 3.4 mΩ - TOLL

Description

The RBE034N15R1SZQ4 N-channel power MOSFET features REXFET-1 split-gate technology and is offered in a TOLL package. The TOLL package features compact and optimal thermal performance. Renesas' REXFET-1 split gate technology is suitable for applications requiring low RDS(on) and switching capability for high-power and high-frequency applications.

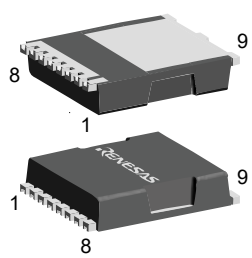
Features

- Standard level gate drive voltage: $V_{GS(th)}$ = 2.2 to 3.7 V
- Super low on-state resistance: $R_{DS(on)}$ = 3.4 mΩ MAX.
- Low input capacitance
- Low thermal resistance
- 100% Avalanche tested
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

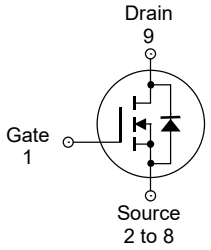
Application

Motor Control, Energy Infrastructure, Industrial Automation, DC-DC Power Conversion, Power Tools, Robotics

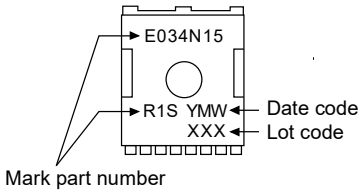
Outline



TOLL



Equivalent circuit



Marking Specification

Absolute Maximum Ratings

(T_J = 25 °C unless otherwise noted.)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	150	V
Gate to Source Voltage	V_{GSS}	±20	V
Continuous Drain Current	$I_{D(Tc = 25°C)}$ Note 2,7	±200	A
	$I_{D(Tc = 100°C)}$ Note 2,7	±148	A
Pulsed Drain Current	$I_{D(pulse)}$ Note 1,2,3,7	±800	A
Power Dissipation	P_D Note 1,7	366	W
Operating and Storage Temperature	T_J, T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} Note 4,5	75	A
Single Avalanche Energy	E_{AS} Note 4,5	421	mJ

Thermal Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ Note 7	—	—	0.41	°C/W
Junction to Ambient Thermal Resistance	$R_{th(j-a)}$ Note 6,7	—	—	40	°C/W

Electrical Characteristics

(T_J = 25 °C unless otherwise noted.)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 150 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.2	—	3.7	V	V_{DS} = V_{GS}, I_D = 250 μA
Drain to Source On-state Resistance	$R_{DS(on)}$	—	2.8	3.4	mΩ	V_{GS} = 10 V, I_D = 100 A
Input Capacitance	C_{iss}	—	6200	—	pF	V_{DS} = 75 V, V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{oss}	—	2100	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	37	—	pF	
Gate resistance	R_g	—	4.4	—	Ω	—
Turn-on Delay Time	$t_{d(on)}$	—	30	—	ns	V_{DD} = 75 V, I_D = 50 A V_{GS} = 10 V R_G = 5 Ω
Rise Time	t_r	—	20	—	ns	
Turn-off Delay Time	$t_{d(off)}$	—	95	—	ns	
Fall Time	t_f	—	20	—	ns	
Total Gate Charge	Q_g	—	86	—	nC	V_{DD} = 75 V, I_D = 50 A V_{GS} = 10 V
Gate to Source Charge	Q_{gs}	—	30	—	nC	
Gate to Drain Charge	Q_{gd}	—	15	—	nC	
Gate Plateau Voltage	$V_{plateau}$	—	5.0	—	V	
Output Charge	Q_{oss}	—	255	—	nC	V_{DS} = 75 V, V_{GS} = 0 V
Body Diode Forward Voltage	$V_{F(S-D)}$	—	0.87	1.5	V	I_F = 100 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	120	—	ns	I_F = 50 A, V_{GS} = 0 V d_i/d_t = 100 A/μs
Reverse Recovery Charge	Q_{rr}	—	400	—	nC	

Notes:

1. T_C = 25 °C
2. Value is limited by overall system design including PCB.
3. $P_W \leq 10$ μs
4. L = 100 μH, V_{DD} = 50 V, R_G = 25 Ω
5. Refer to the typical characteristics curve for I_{AS} and $E_{AS.}$ (Figure. 5, 6)
6. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)
7. Defined by design. Not subject to production test.

Typical Characteristics

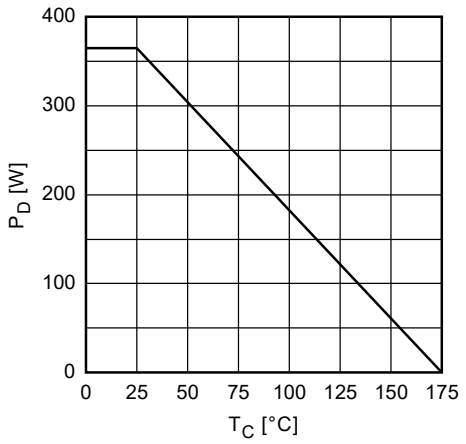


Figure 1. Power Dissipation vs. Case Temperature

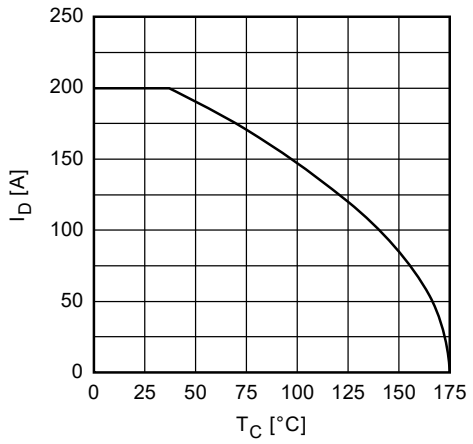


Figure 2. Drain Current vs. Case Temperature

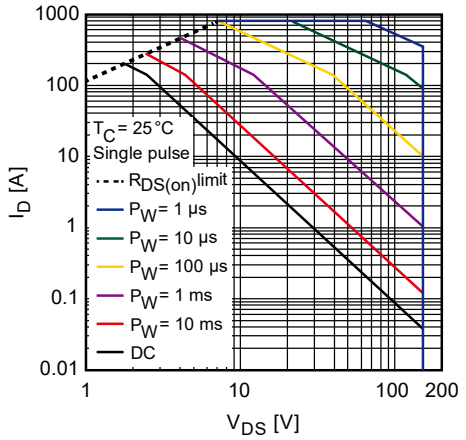


Figure 3. Foward Bias Safe Operating Area

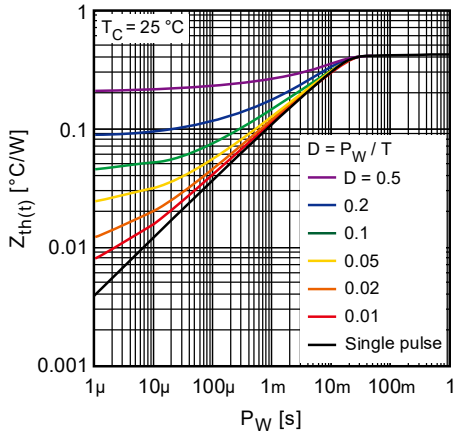


Figure 4. Transient Thermal Impedance vs. Pulse Width

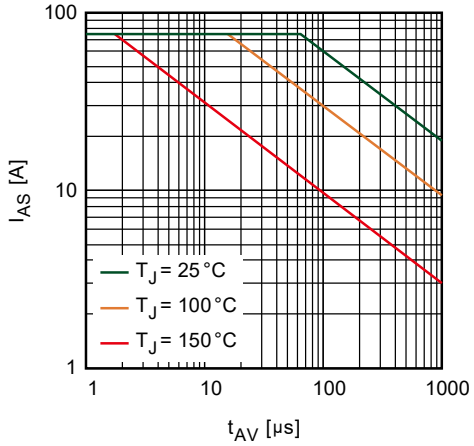


Figure 5. Avalanche Current Characteristics

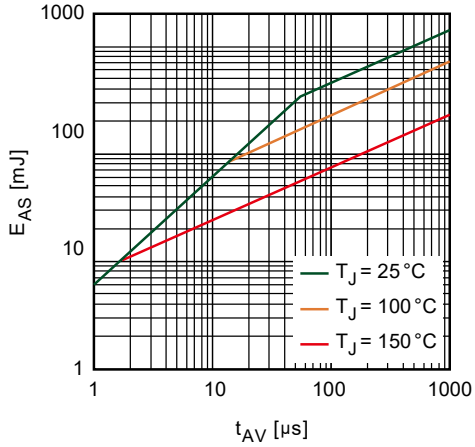


Figure 6. Avalanche Energy Characteristics

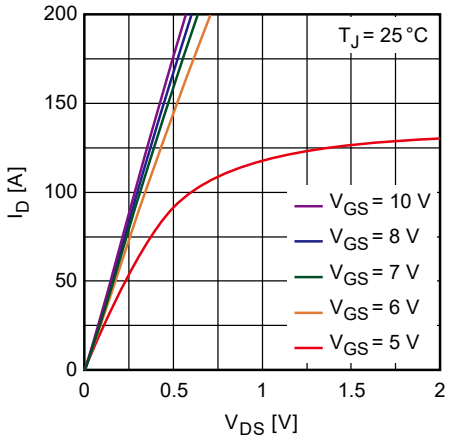


Figure 7. Typical Output Characteristics

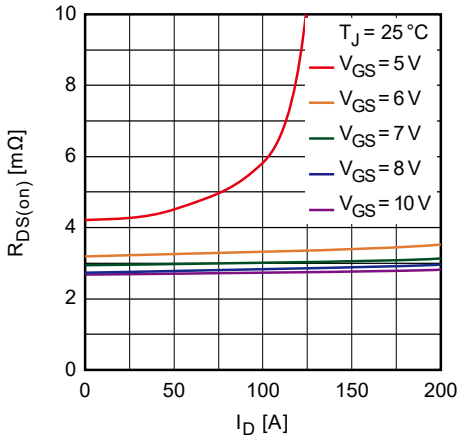


Figure 8. Drain to Source On-state Resistance vs. Drain Current

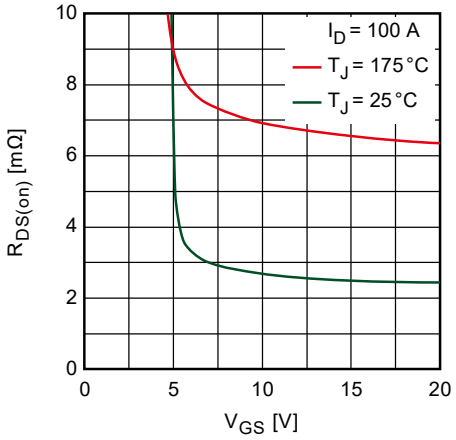


Figure 9. Drain to Source On-state Resistance vs. Gate to Source Voltage

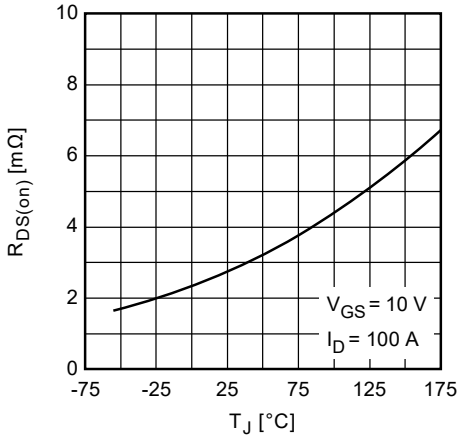


Figure 10. Drain to Source On-state Resistance vs. Junction Temperature

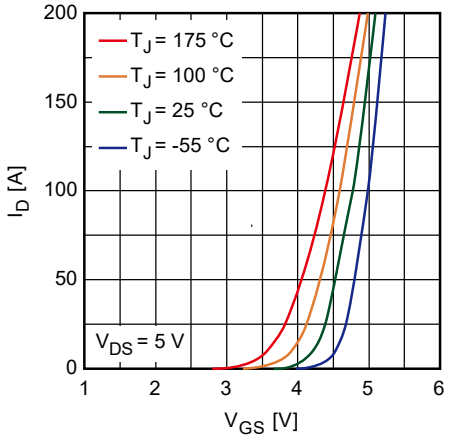


Figure 11. Typical Transfer Characteristics

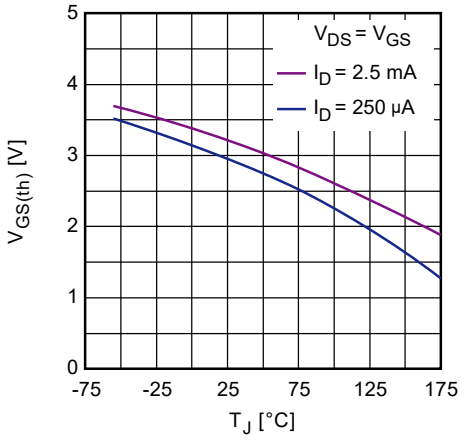


Figure 12. Gate to Source Threshold Voltage vs. Junction Temperature

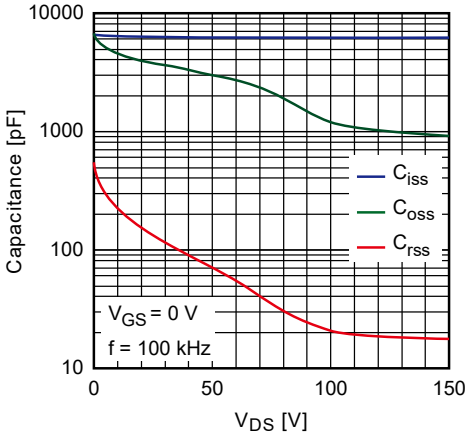


Figure 13. Capacitances vs. Drain to Source Voltage

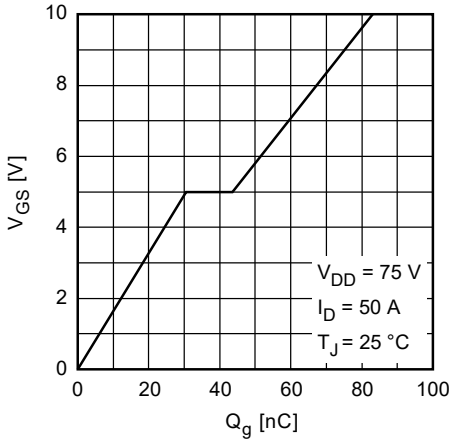


Figure 14. Dynamic Input/Output Characteristics

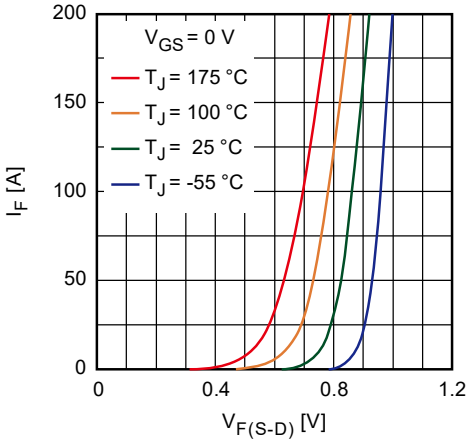


Figure 15. Source to Drain Diode Forward Voltage

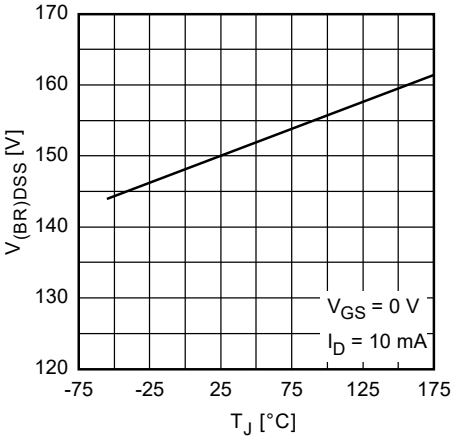


Figure 16. Drain to Source Breakdown Voltage vs. Junction Temperature

Test Circuits

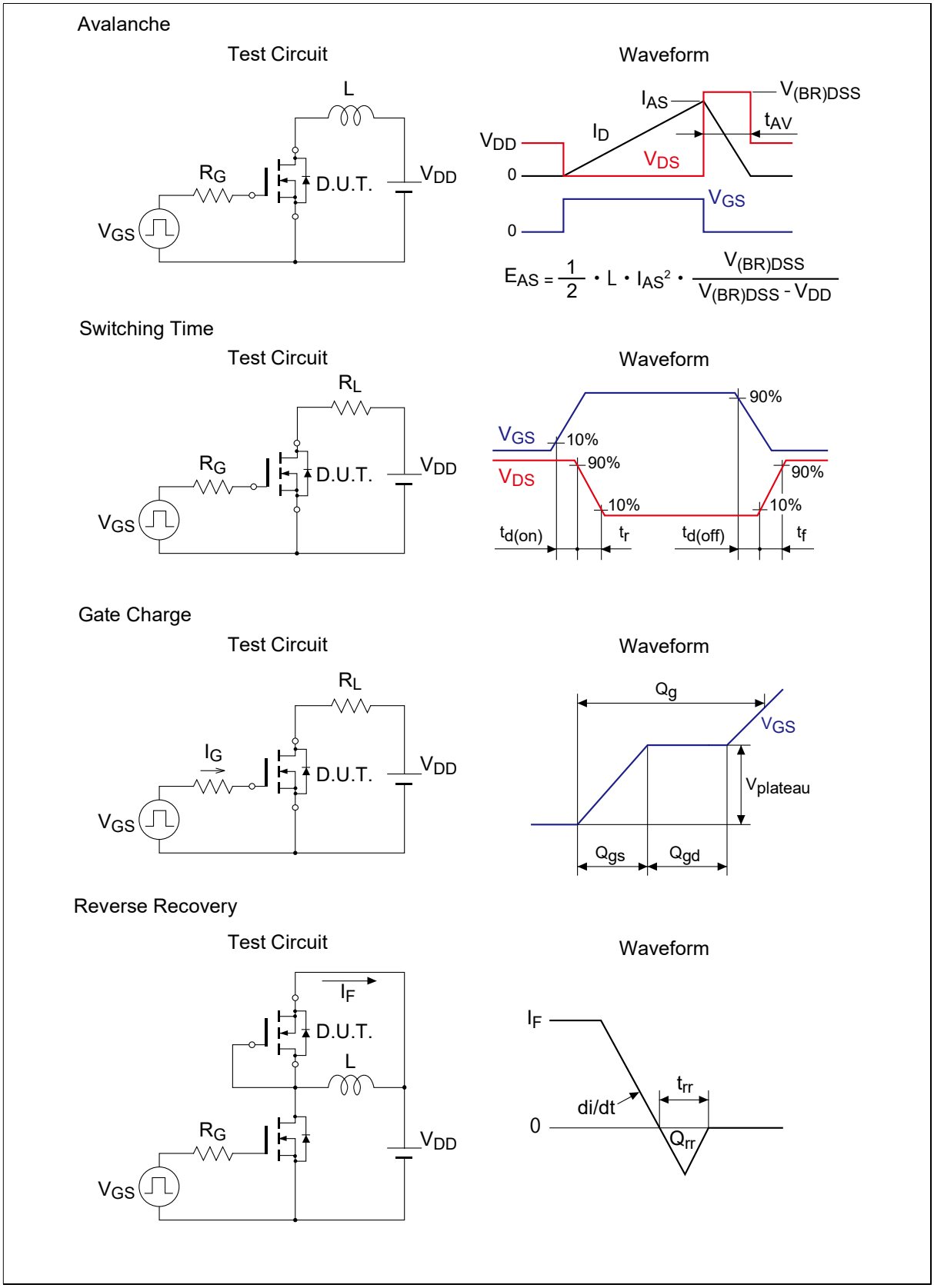
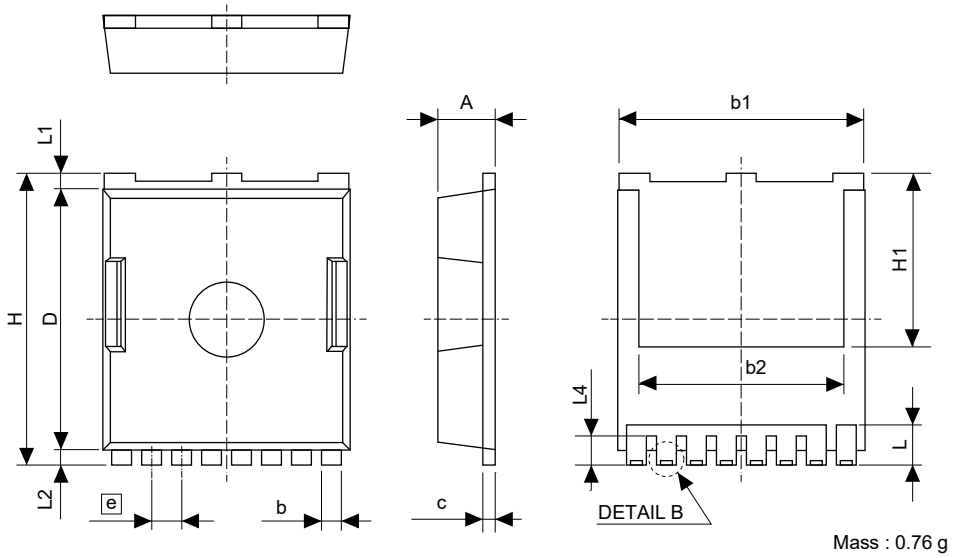
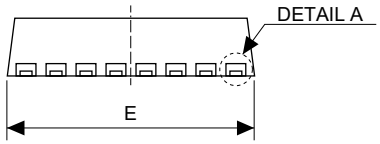
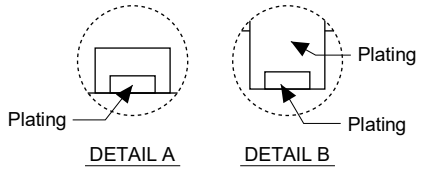


Figure 17. Test Circuits and waveforms

Package Dimensions





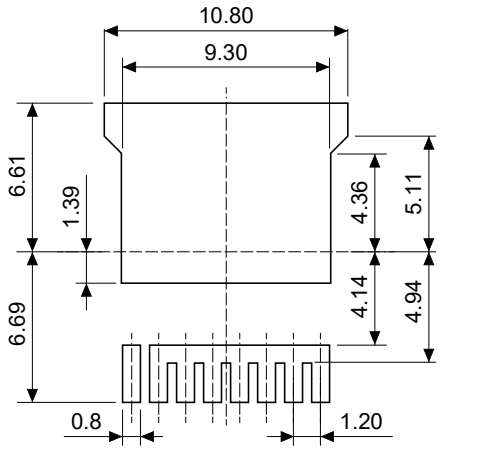


Wettable flank structure

SYMBOL	DIMENSION (mm)		
	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.65	0.80	0.95
b1	9.65	9.80	9.95
b2	8.00	8.20	8.40
c	0.40	0.50	0.60
D	10.18	10.38	10.58
E	9.70	9.90	10.10
e	1.20BSC		
H	11.48	11.68	11.88
H1	6.65	6.95	7.25
L	1.40	1.60	1.80
L1	0.60	0.70	0.80
L2	0.45	0.60	0.75
L4	1.00	1.15	1.30

Figure 18. Package Outline – TOLL

Mount pad



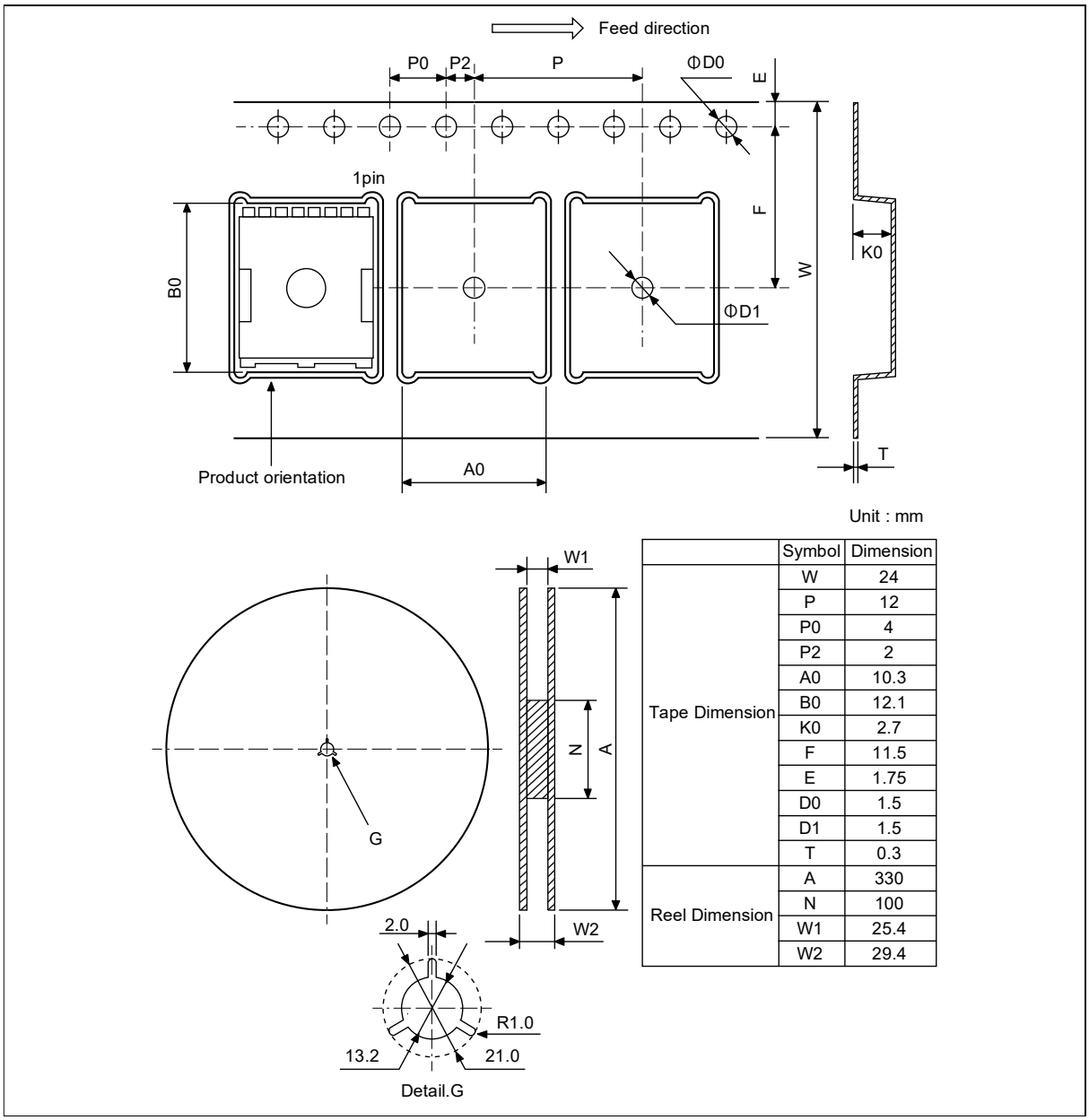
Unit : mm

Figure 19. Mount Pad Information

Ordering Information

Part No.	Packing	Quantity
RBE034N15R1SZQ4#GB0	Taping	2000 pcs/reel

Packing Specification



	Symbol	Dimension
Tape Dimension	W	24
	P	12
	P0	4
	P2	2
	A0	10.3
	B0	12.1
	K0	2.7
	F	11.5
	E	1.75
	D0	1.5
	D1	1.5
	T	0.3
Reel Dimension	A	330
	N	100
	W1	25.4
	W2	29.4

Figure 20. Packing Information

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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