

RBA500N10EHWT-2UA01

REXFET-1 N-Channel Power [MOSFET](#)

100V – 500A – 0.65mΩ– Chip

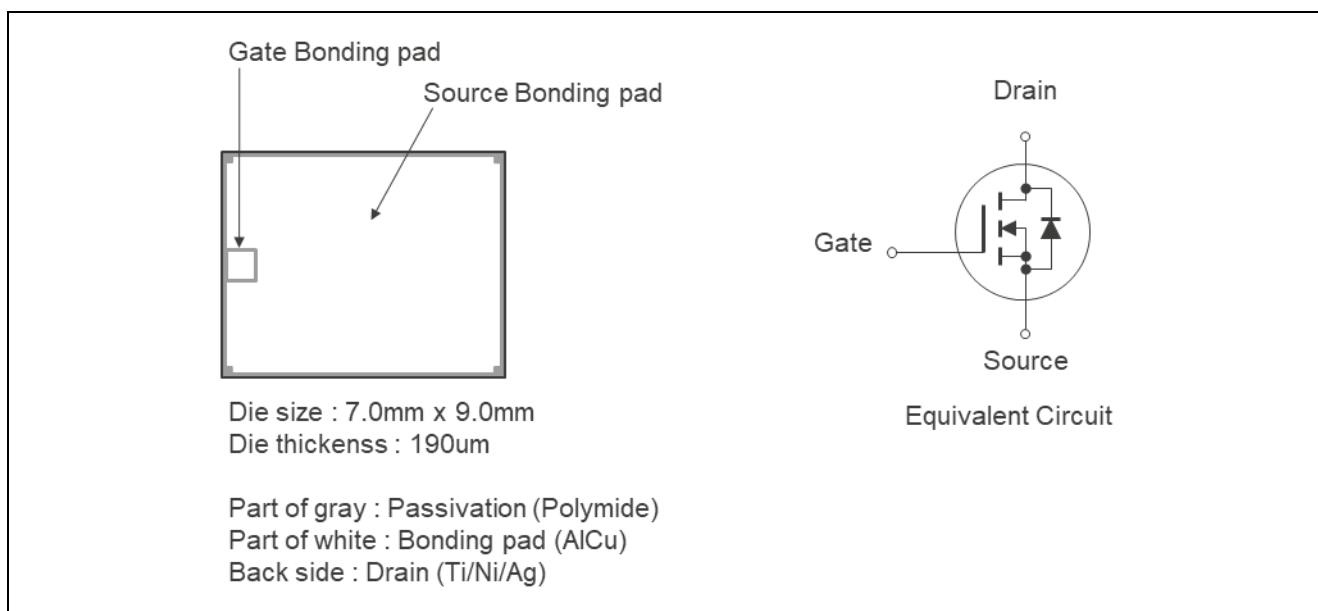
Description

This product is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Standard level gate drive voltage : $V_{GS(th)} = 2.0\sim 4.0V$
- Super Low on-state resistance : $R_{DS(on)} = 0.65m\Omega$ Max.
- Low input capacitance
- Designed for automotive application and AEC Q101 (HTRB, HTGB) qualified.

Outline



Absolute Maximum Ratings

(T_j=25°C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DSS}	100	V
Gate to Source Voltage	V _{GSS}	+20 / -10	V
Drain Current (DC)	I _{D(DC)} ^{Notes1}	±500	A
Junction Temperature	T _j	175	°C

Notes 1. T_c=25 °C, T_{ch}≤175°C

Value is limited by overall system design including PCB.

Defined by design. Not subject to production test.

Electrical Characteristics 1

The characteristic items specified in this table guarantee the electrical characteristics in the chip state but do not the characteristic fluctuations or characteristic defects that occur in the processes after assembling.

(T_j=25°C unless otherwise notice.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	—	—	10	μA	V _{DS} = 100 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}	—	—	±3	μA	V _{GS} = +20 / -10 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250 μA

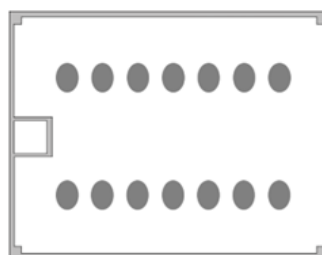
Electrical Characteristics 2

Reference data. Defined by design. Not subject to production test.

(T_j=25°C unless otherwise notice.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to Source On-state Resistance	R _{DS(on)} ^{Notes2}	—	0.54	0.65	mΩ	V _{GS} = 10 V, I _D = 250A
Input Capacitance	C _{iss}	—	34000	—	pF	V _{DS} = 50 V V _{GS} = 0 V f = 100 kHz
Output Capacitance	C _{oss}	—	8700	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	250	—	pF	
Gate resistance	R _g	—	2.0	—	Ω	
Turn-on Delay Time	t _{d(on)}	—	220	—	ns	V _{DD} = 50 V, I _D = 100A V _{GS} = 10 V R _G = 10 Ω
Rise Time	t _r	—	300	—	ns	
Turn-off Delay Time	t _{d(off)}	—	550	—	ns	
Fall Time	t _f	—	270	—	ns	
Total Gate Charge	Q _g	—	450	—	nC	V _{DD} = 50 V V _{GS} = 10 V I _D = 250 A
Gate to Source Charge	Q _{gs}	—	180	—	nC	
Gate to Drain Charge	Q _{gd}	—	80	—	nC	
Body Diode Forward Voltage	V _{F(S-D)} ^{Notes2}	—	0.85	1.7	V	I _F = 250 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	190	—	ns	I _F = 250 A, V _{GS} = 0 V di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}	—	850	—	nC	

Notes 2. This is the estimated value of the chip excluding package resistance when mounted at the source bonding wire position shown in the figure below.

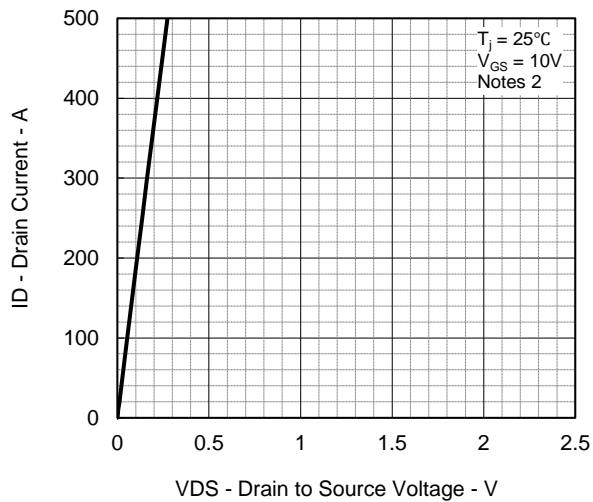


Bonding wire x 7 , two stitch bonding

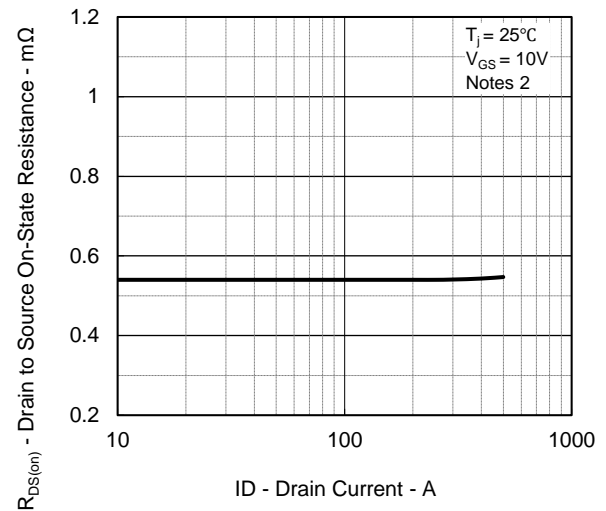
● Bonding position

Typical Characteristics

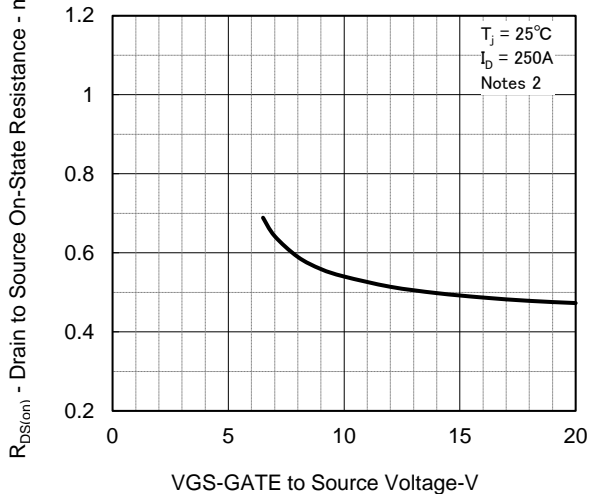
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



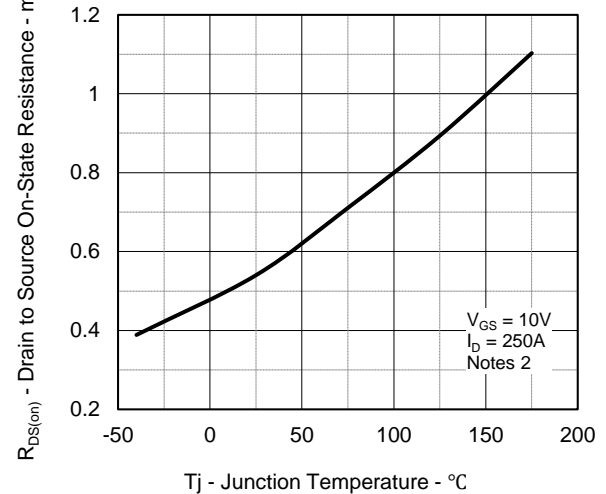
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



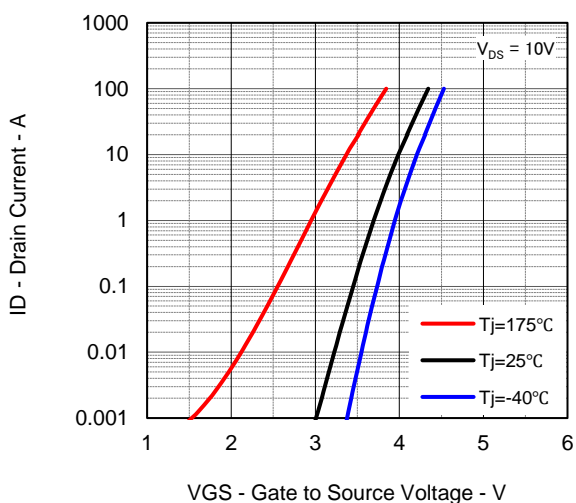
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



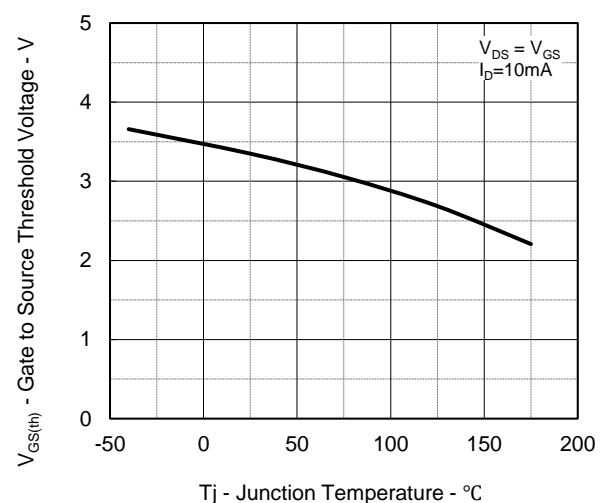
DRAIN TO SOURCE ON-STATE RESISTANCE vs. JUNCTION TEMPERATURE



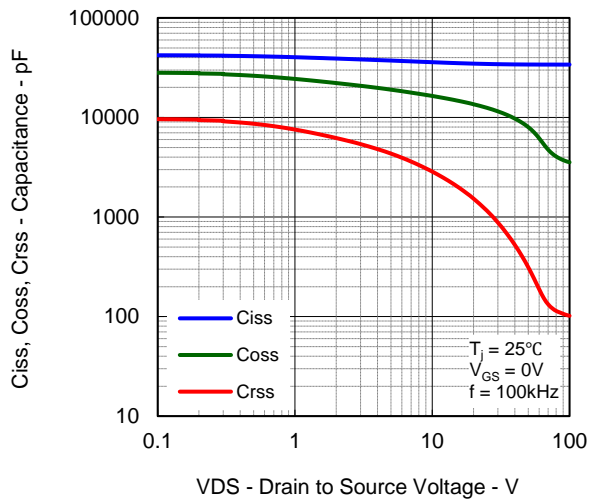
FORWARD TRANSFER CHARACTERISTICS



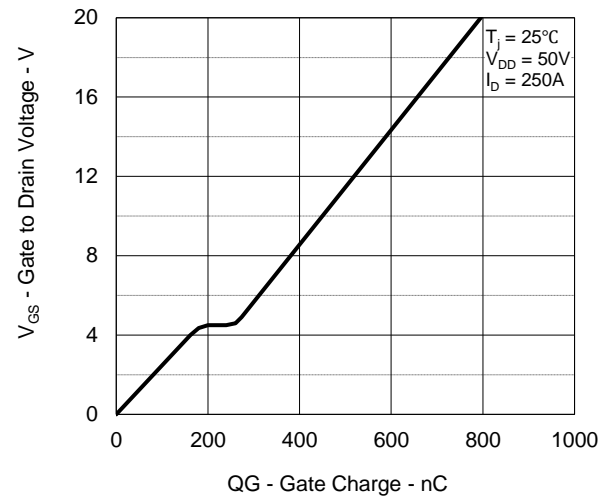
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE



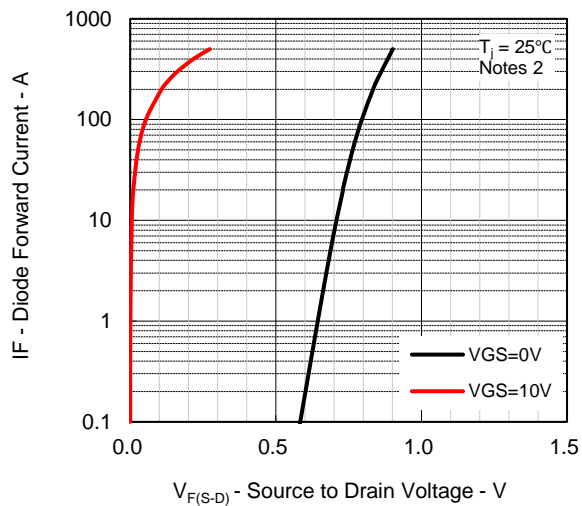
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



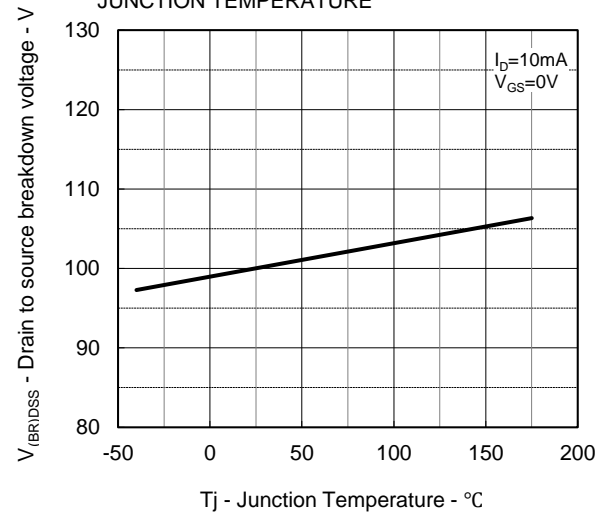
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



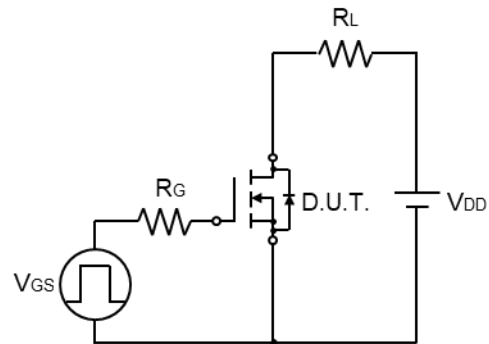
DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE



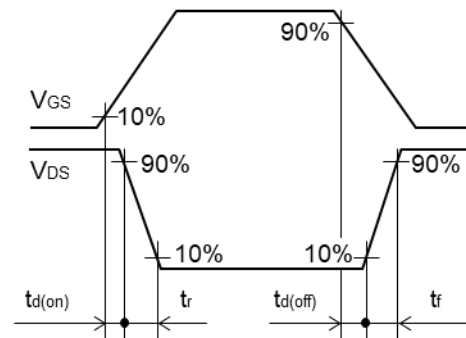
Test Circuit

Switching Time

Test Circuit

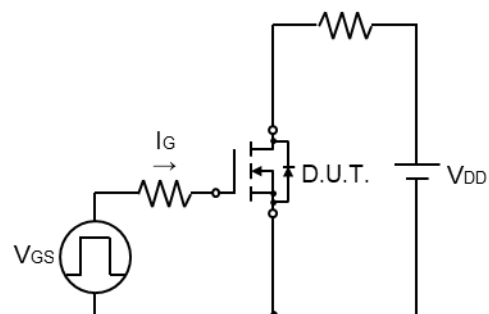


Waveform

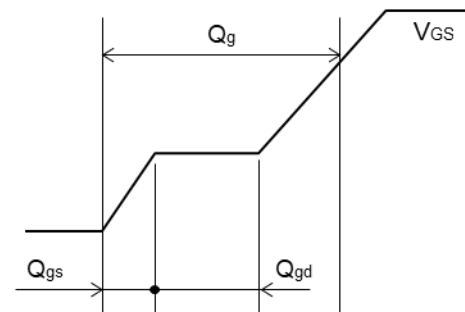


Gate Charge

Test Circuit

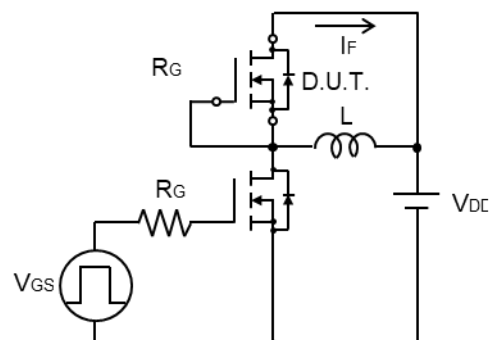


Waveform

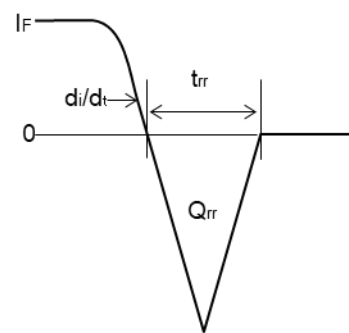


Reverse Recovery

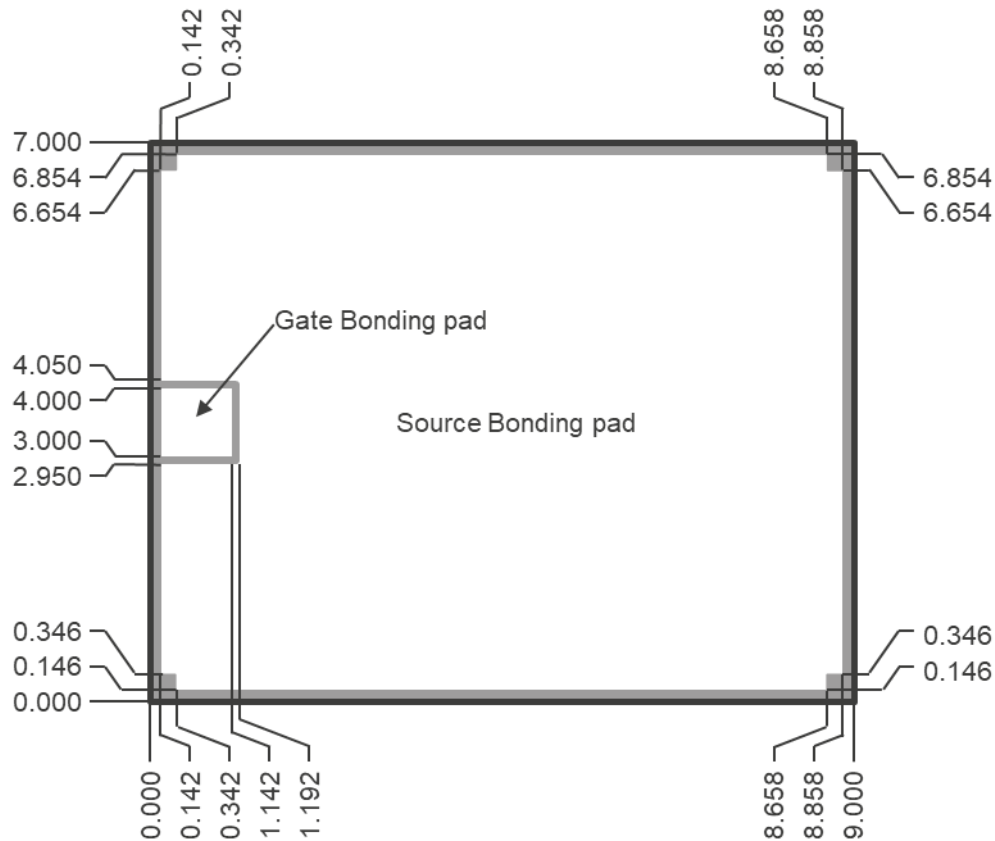
Test Circuit



Waveform



Chip Dimensions



Unit : mm

Die size : 7.0mm x 9.0mm

Die thickness : 190um

Part of gray : Passivation (Polymide)

Part of white : Bonding pad (AlCu)

Back side : Drain (Ti/Ni/Ag)

Recognition, target and any other patterns which are not related to MOSFET operation, may be changed without notice.

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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