

RBA100N04DANS-4UB02

N-Channel Power [MOSFET](#)

40V - 100A - 2.0mΩ

Description

The RBA100N04DANS-4UB02 is an AEC-Q101 qualified N-channel power MOSFET featuring low RDS(on) and low input capacitance for high-speed switching and low power loss. It uses a Renesas SO8-FL 5 x 6 mm² flat-lead, copper-clip package, supporting high current with excellent thermal performance, durability, and reliability, making it ideal for automotive applications such as power management, motor drives, and e-fuse.

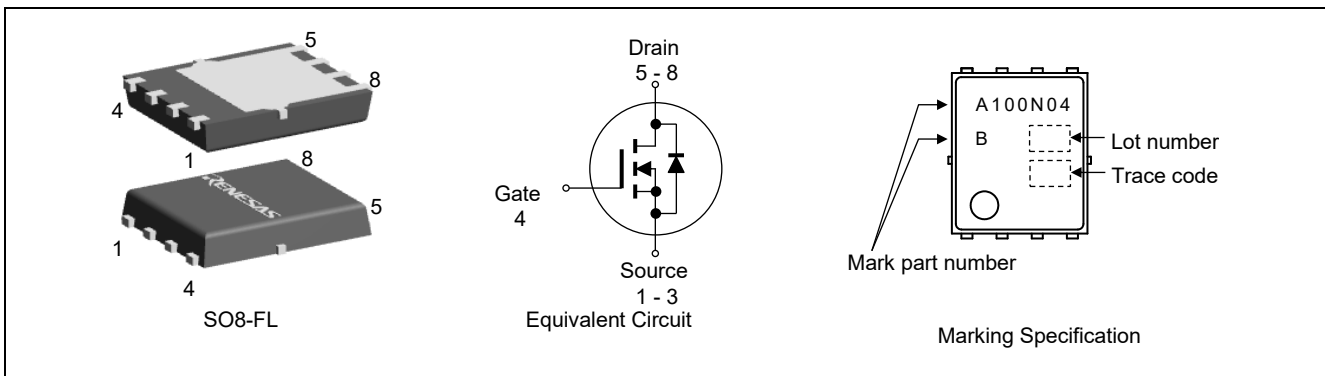
Features

- Standard-level gate drive voltage: $V_{GS(th)} = 2.0\sim 4.0V$
- Super low on-state resistance: $R_{DS(on)} = 2.0m\Omega$ Max.
- Low input capacitance
- Low thermal resistance
- 100% Avalanche tested
- AEC-Q101 qualified
- Production Part Approval Process (PPAP) capable
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

Application

- 12V/24V load EPS, ABS, BMS, e-fuse, etc.

Outline



Absolute Maximum Ratings

($T_j = 25\text{ }^\circ\text{C}$ unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	40	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$ <small>Note 1,2,5</small>	± 100	A
Drain Current (pulse)	$I_{D(pulse)}$ <small>Note 1,3,5</small>	± 300	A
Power Dissipation	P_D <small>Note 1,5</small>	100	W
Junction Temperature	T_j	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 175	$^\circ\text{C}$
Single Avalanche Current	I_{AS} <small>Note 4</small>	41	A
Single Avalanche Energy	E_{AS} <small>Note 4</small>	168	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ ^{Note 5}	1.5	°C/W
Junction to Ambient Thermal Resistance	$R_{th(j-a)}$ ^{Note 5,6}	50	°C/W

Electrical Characteristics

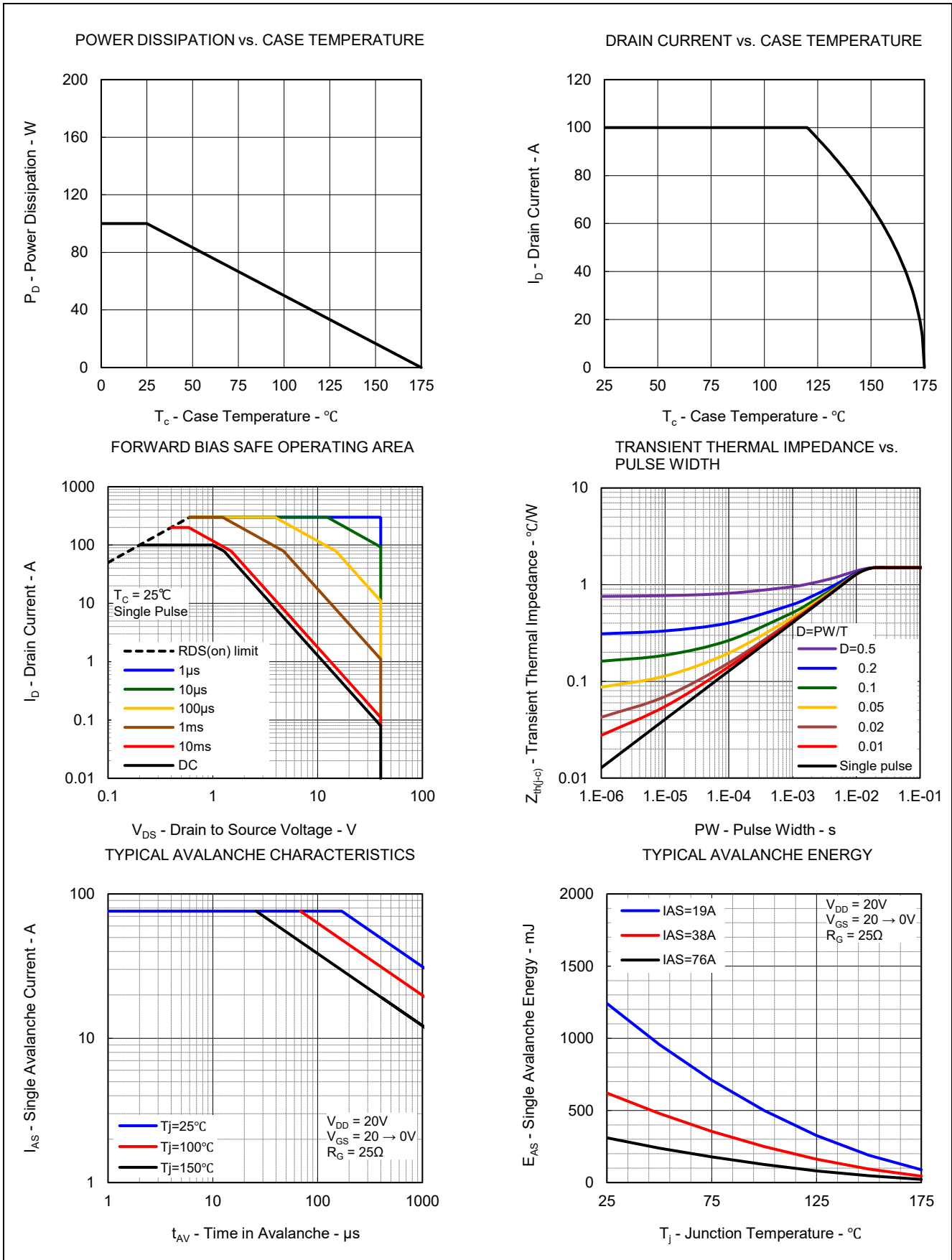
(T_j = 25 °C unless otherwise notice.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 40 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}	—	—	±100	nA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250 μA
Drain to Source On-state Resistance	R _{DS(on)}	—	1.76	2.0	mΩ	V _{GS} = 10 V, I _D = 50 A
Input Capacitance	C _{iSS}	—	4160	—	pF	V _{DS} = 25 V V _{GS} = 0 V f = 1 MHz
Output Capacitance	C _{oss}	—	450	—	pF	
Reverse Transfer Capacitance	C _{rSS}	—	335	—	pF	
Gate Resistance	R _g	—	1.7	—	Ω	
Turn-on Delay Time	t _{d(on)}	—	29	—	ns	V _{DD} = 20 V, I _D = 50 A V _{GS} = 10 V R _G = 5 Ω
Rise Time	t _r	—	31	—	ns	
Turn-off Delay Time	t _{d(off)}	—	71	—	ns	
Fall Time	t _f	—	25	—	ns	
Total Gate Charge	Q _g	—	83	—	nC	V _{DD} = 20 V V _{GS} = 10 V I _D = 50 A
Gate to Source Charge	Q _{gs}	—	21	—	nC	
Gate to Drain Charge	Q _{gd}	—	24	—	nC	
Gate Plateau Voltage	V _{plateau}	—	5.0	—	V	
Output Charge	Q _{oss}	—	24	—	nC	V _{DD} = 20 V, V _{GS} = 0 V
Body Diode Forward Voltage	V _{F(S-D)}	—	0.83	1.5	V	I _F = 50 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	47	—	ns	I _F = 50 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	—	60	—	nC	di/dt = 100 A/μs

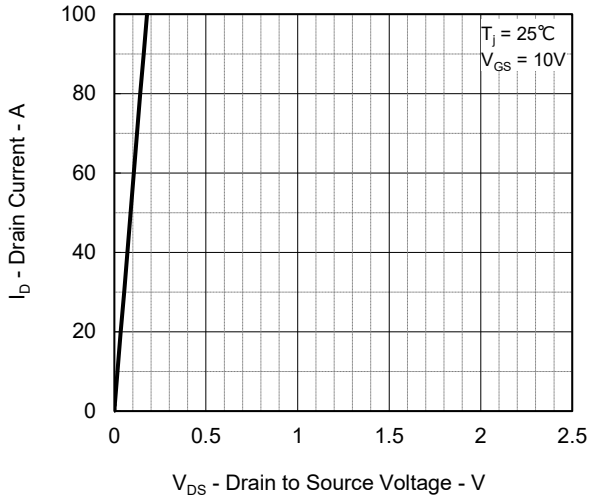
Note 1. T_c = 25°C

2. Value is limited by overall system design including PCB.
3. PW ≤ 10 μs, Duty Cycle ≤ 1%
4. L = 100 μH, V_{DD} = 20 V, V_{GS} = 20 → 0 V, R_G = 25 Ω
5. Defined by design. Not subject to production test.
6. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)

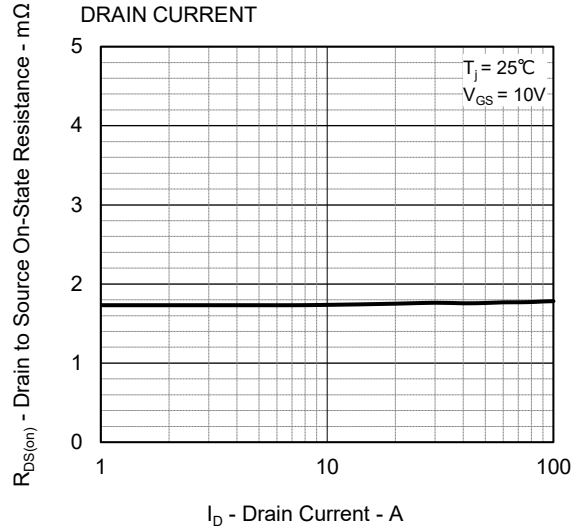
Typical Characteristics



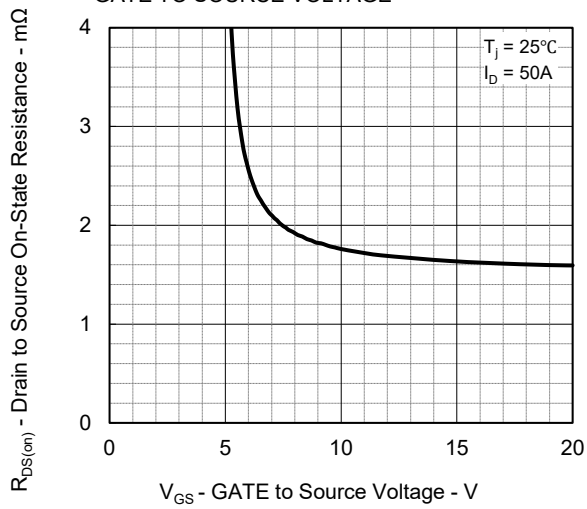
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



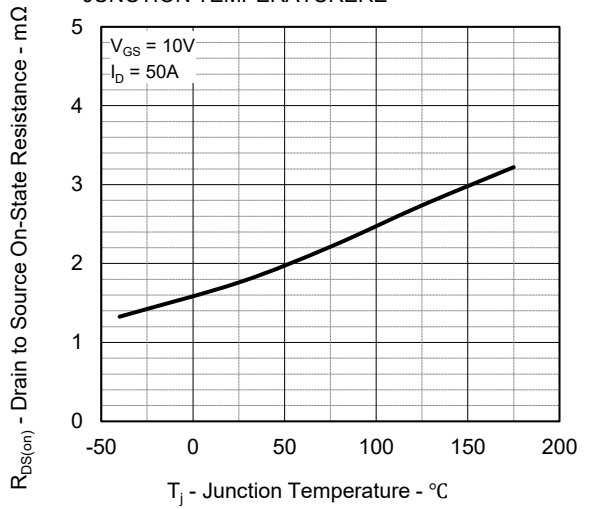
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



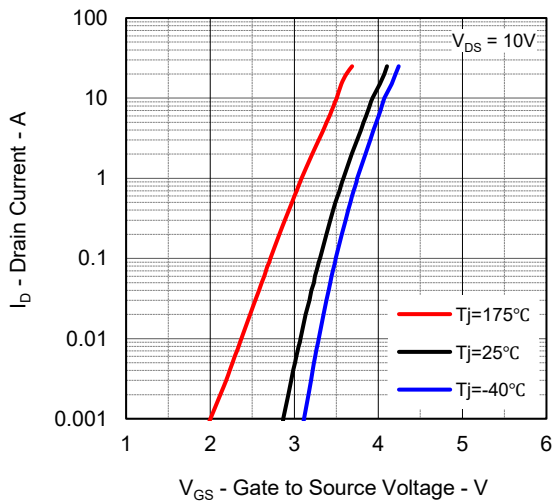
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



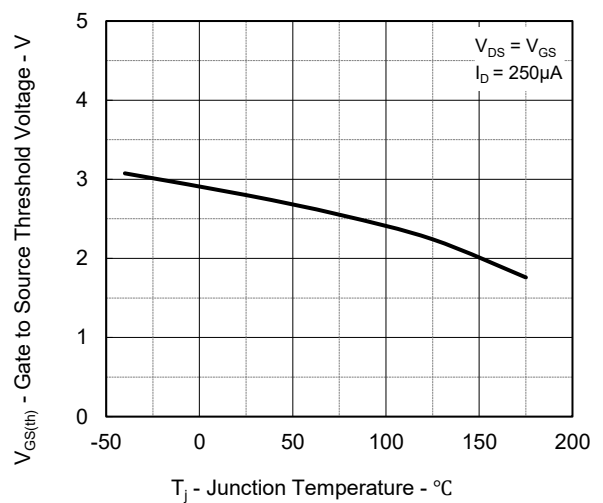
DRAIN TO SOURCE ON-STATE RESISTANCE vs. JUNCTION TEMPERATURE



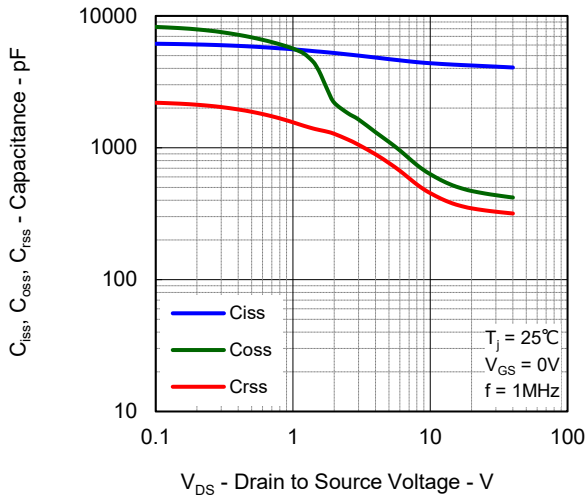
FORWARD TRANSFER CHARACTERISTICS



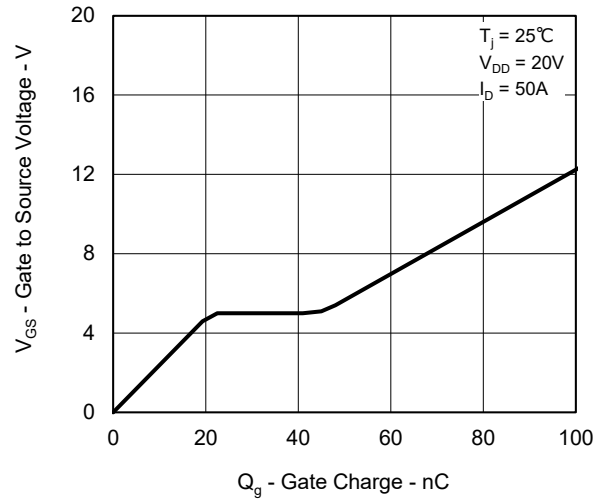
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE



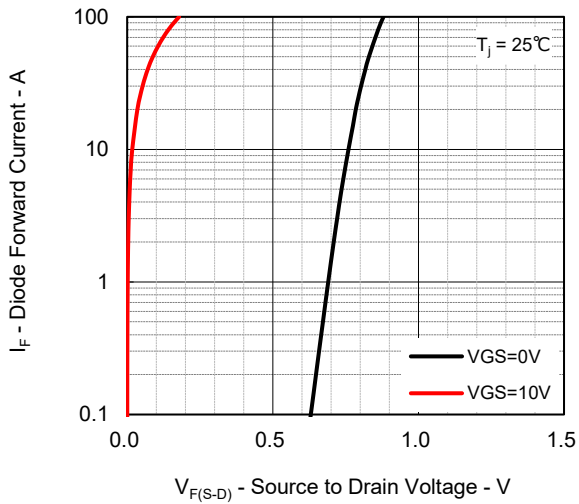
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



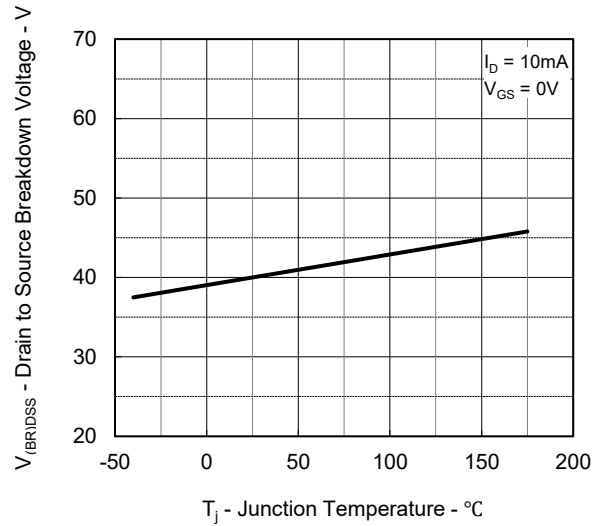
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

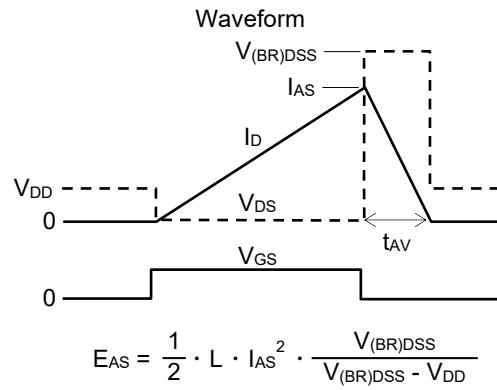
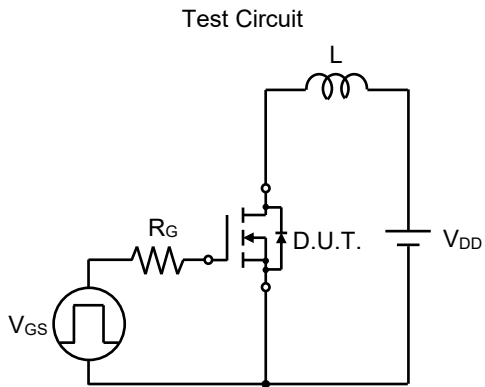


DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE

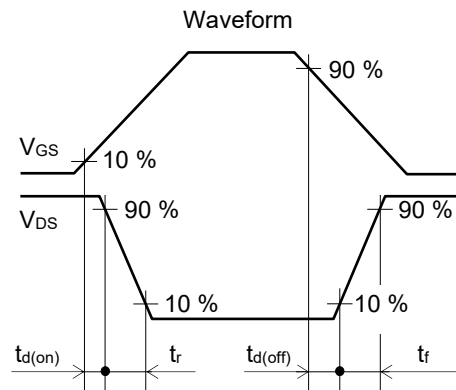
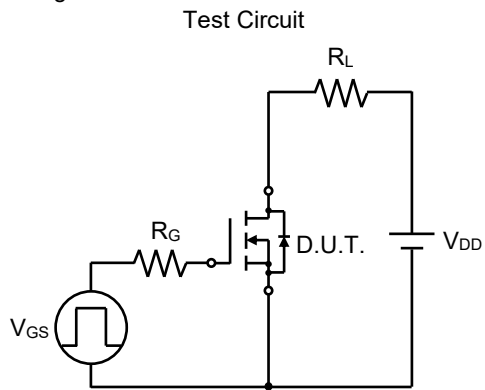


Test Circuit

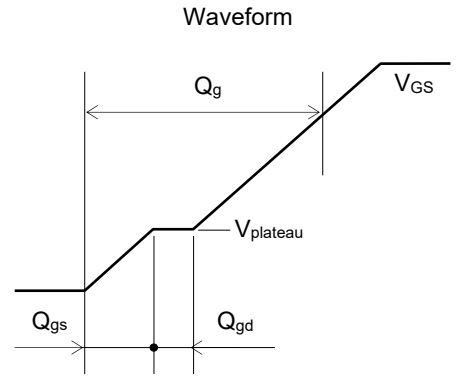
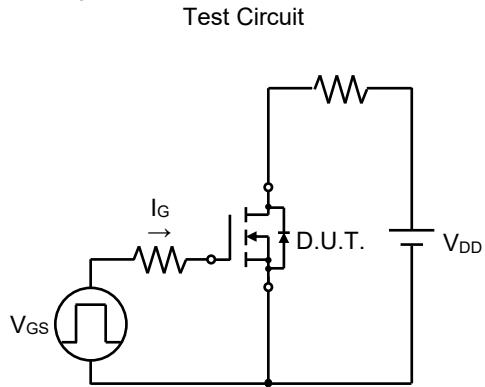
Avalanche



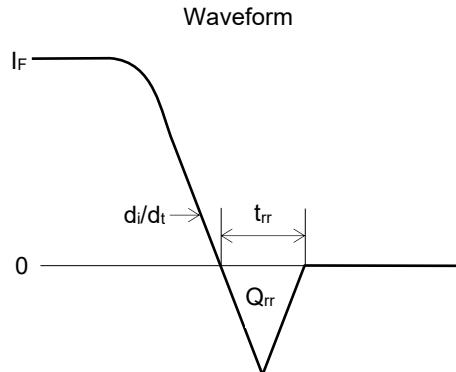
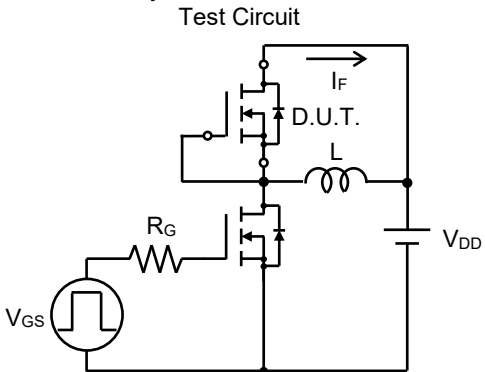
Switching Time



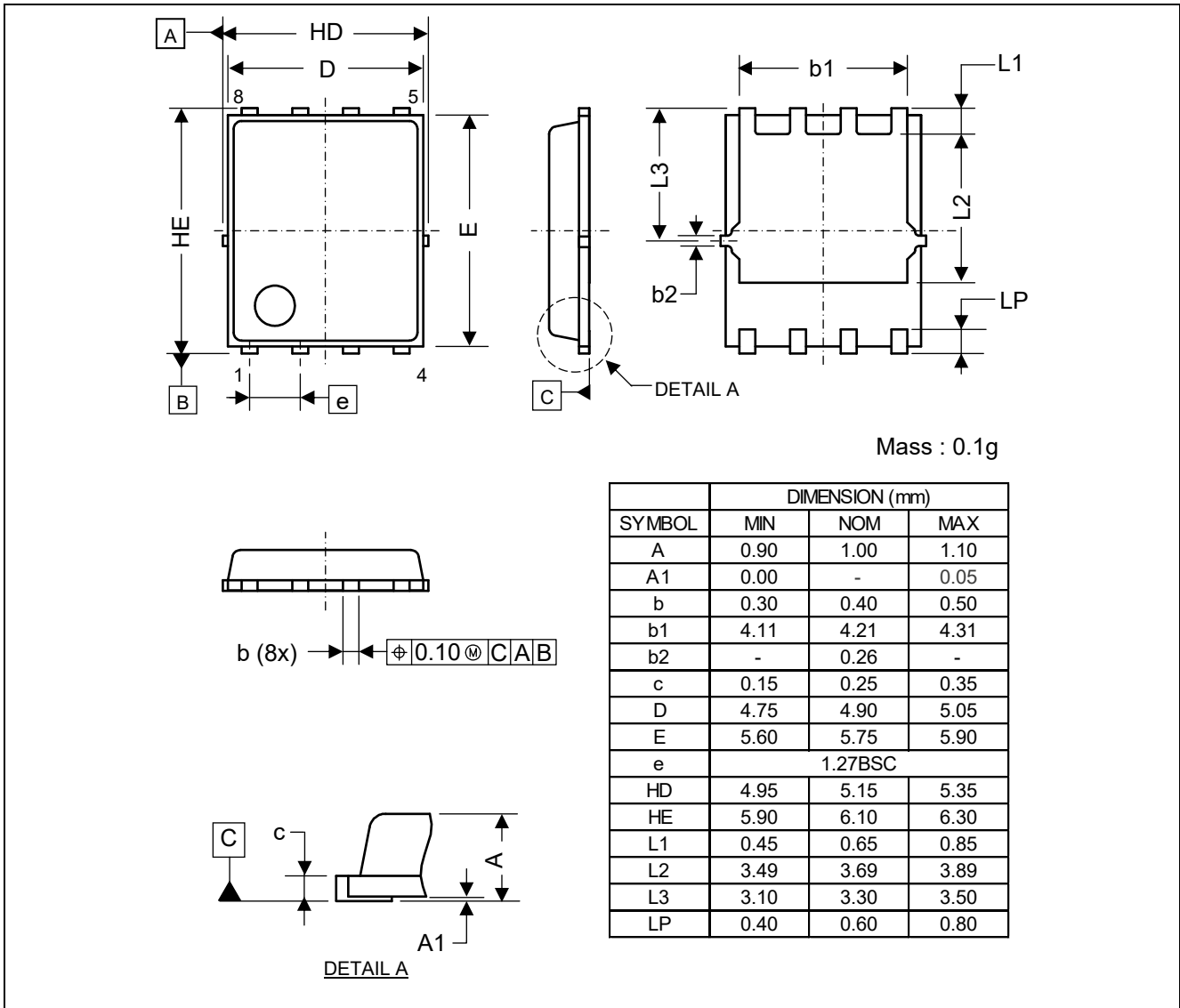
Gate Charge



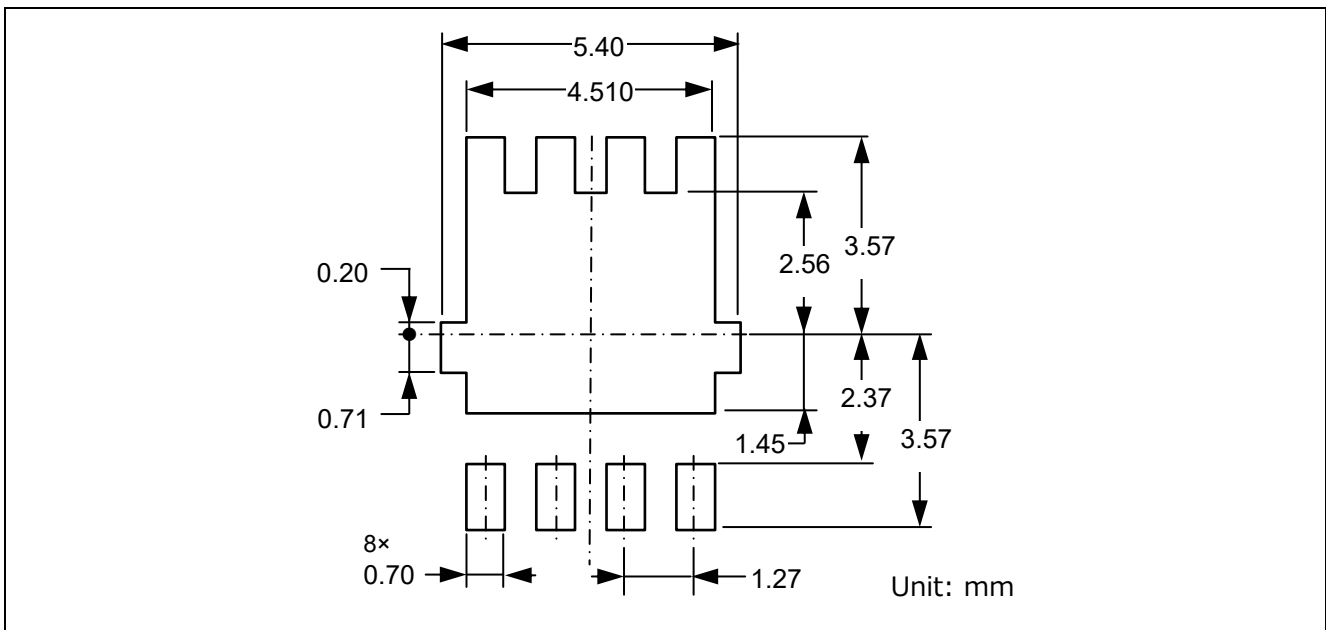
Reverse Recovery



Package Dimensions



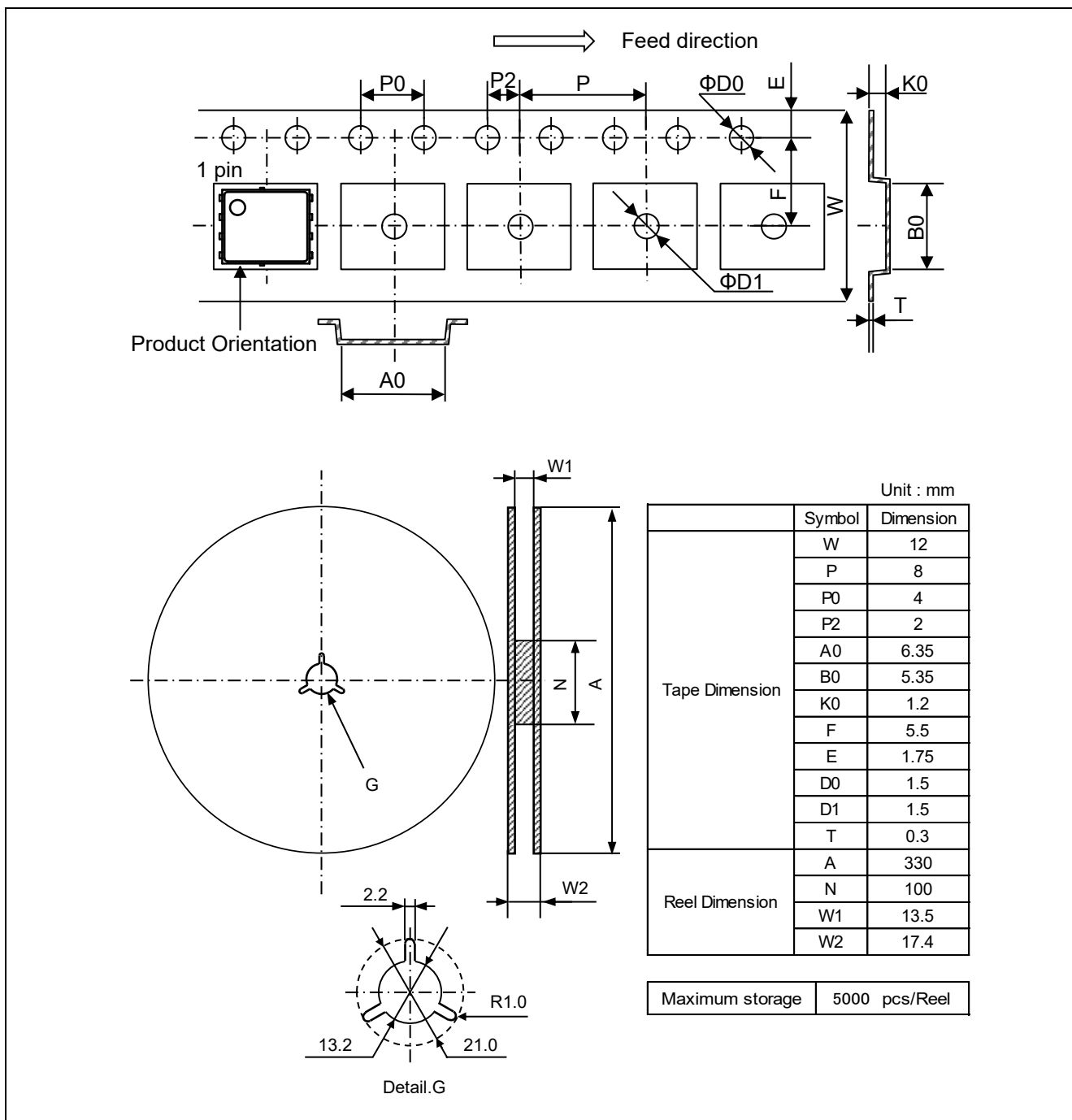
Mount Pad



Ordering Information

Part No.	Packing	Quantity
RBA100N04DANS-4UB02#HB0	Taping	5000pcs/reel

Packing Specification



Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook.

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