RAJ2930104AGM

Gate Driver IC for IGBTs and SiC MOSFETs

Description

The RAJ2930104AGM is a gate driver IC for IGBT and SiC MOSFET gate-drive in high voltage inverter applications. Integrated 3750 V_{RMS} micro-isolators provide data transfer with high voltage isolation between the primary circuit (MCU side) and the secondary circuit (IGBT side). In addition, it boasts superior CMTI (Common Mode Transient Immunity) performance over 150 V/ns, providing reliable communication and increased noise immunity while meeting the high voltages and fast switching speeds required in inverter systems.

This device contains gate drive circuit, miller clamp circuit, and soft turn-off circuit as well as several types of protection circuits such as over-current detection.

Part Number	Package	Body Size
RAJ2930104AGM	SOP16	7.5 mm x 10.3 mm

Features

- On-chip micro isolator (Isolated circuit)
  - High voltage isolation: 3750 V_{RMS}, 1 min
  - High Common Mode Transient Immunity (CMTI): over 150 V/ns
- High output gate drive circuit
  - Gate drive output peak current (Source / Sink): 10 A typ. / 10 A typ.
  - On-chip active miller clamp
  - Soft turn-off function
- Various on-chip protection circuits
  - Over-current detection by current sense: 0.7 V typ.
  - On-chip Under-Voltage Lockout Circuit (UVLO)
    - VCC1 (5 V system): 4.1 V typ.
    - VCC2 (15 V system): 10 V typ.
  - Fault alarm outputs on FOB pin and the latched fault status can be reset by RSTB pin
- Operating temperature: -40 °C to 125 °C (Junction temperature: 150 °C max)
- AEC-Q100 Qualified (Grade 1)

Applications

- Traction inverters for EV / HEV in automotive applications
- DC-DC converters for EV / HEV in automotive applications
- On-board charger for EV in automotive applications
- Inverters and converters for industrial instruments and so on

Note: The information contained in this document is the one that was obtained when the document was issued and may be subject to change.

Contents

Figures

Tables

1. Pin Information

1.1 Pin Assignments

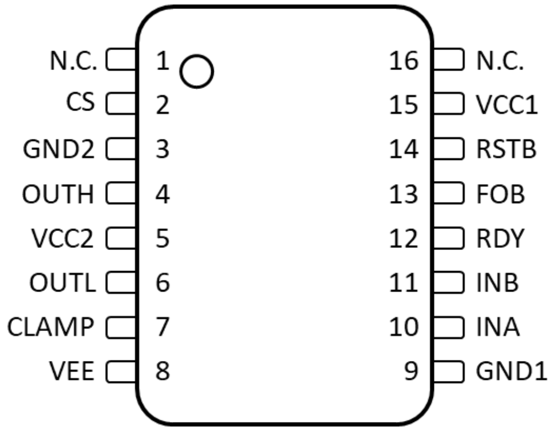


Figure 1. Pin assignments

1.2 Pin Descriptions

Table 1. Pin assignment and functions

Pin Number	Pin Name	I/O	Description
1	N.C.	-	Non-connection Pin can be applied in either open or VEE connection.
2	CS	I	Current sense input.
3	GND2	P	Secondary side GND. Connect to IGBT emitter.
4	OUTH	O	Gate drive output (Positive).
5	VCC2	P	Secondary power supply input (15 V typ).
6	OUTL	O	Gate drive output (Negative).
7	CLAMP	I/O	Active miller clamp input/output.
8	VEE	P	Negative power supply input. Connect to GND2 for unipolar supply application.
9	GND1	P	Primary side GND.
10	INA	I	Non-inverted gate drive input.
11	INB	I	Inverted gate drive input.
12	RDY	O	Power-good output.
13	FOB	O	Inverted fault output (L level output at error).
14	RSTB	I	Reset input. Apply a low pulse to reset fault (FOB) latch.
15	VCC1	P	Primary side power supply input (5 V typ)
16	N.C.	-	Non-connection Pin can be applied in either open or GND1 connection.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Min	Max	Unit
VCC1 – GND1	VCC1	–0.3	6	V
VCC2 – GND2	VCC2	–0.3	36	V
VEE – GND2	VEE	–17.5	0.3	V
VCC2 – VEE	V_{MAX}	–0.3	36	V
Digital inputs	INA, INB, RSTB	GND1–0.3	VCC1+0.3	V
Reference to GND2	CS	GND2–0.3	VCC2+0.3	V
Outputs	OUTH, OUTL, CLAMP	VEE–0.3	VCC2+0.3	V
Peak source current	I_{OUTH}	-15		A
Peak sink current	I_{OUTL}		15	A
Digital outputs	RDY, FOB	GND1–0.3	VCC1+0.3	V
FOB, and RDY pin input current	I_{FOB}, I_{RDY}		20	mA
Junction temperature range	T_J	-40	150	°C
Storage temperature range	T_{STG}	-55	150	°C
Slew rate of VCC1 for no destruction	VCC1SR1		20	V/µs
Slew rate of VCC2 for no destruction	VCC2SR1		20	V/µs
Slew rate of VEE for no destruction	VEESR1	-20		V/µs

2.2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
VCC1 – GND1	VCC1	4.5	5.5	V
VCC2 – GND2	VCC2	12.5	33	V
VCC2 – VEE	VMAX	12.5	33	V
VEE – GND2	VEE	-16.5	0	V
Reference to GND1, high level input voltage	INA, INB, RSTB	0.7×VCC1	VCC1	V
Reference to GND1, low level input voltage		0	0.3×VCC1	V
Ambient temperature	T_A	-40	125	°C
Junction temperature	T_J	-40	150	°C
Slew rate of VCC1 for no change parameters	$VCC1_{SR2}$		0.5	V/µs
Slew rate of VCC2 for no change parameters	$VCC2_{SR2}$		0.5	V/µs
Slew rate of VEE for no change parameters	VEE_{SR2}	-0.5		V/µs

2.3 ESD Specifications

Parameter	Symbol	Condition	Typical Value	Unit
Electrostatic discharge	V(ESD)	Human Body Model (HBM), per AEC Q100-002	±2000	V
		Charged Device Model (CDM), per AEC Q100-011	±750 (Corner pins) ±500 (Other pins)	V

2.4 Thermal Specifications

Parameter	Symbol	Value	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$[1][4]	64.9	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$[3][4]	27.8	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$[2][4]	33.4	°C/W
Junction-to-top characterization parameter	ψ_{JT}[1][4]	9.4	°C/W
Junction-to-board characterization parameter	ψ_{JB}[1][4]	31.8	°C/W

1. $R_{\theta JA}$, ψ_{JT}, ψ_{JB}: Based on JESD51-2 environment, JESD51-7 test board (4-layer board)
2. $R_{\theta JB}$: Based on JESD51-8 environment
3. $R_{\theta JC(top)}$: Based on MIL-STD-883 method 1012.1 described in JESD51-12
4. These thermal parameters were obtained by simulation and these figures are reference values.

2.5 Power Ratings

Parameter	Symbol	Conditions	Value	Unit
Maximum power dissipation (both sides)	P_D	VCC1 = 5 V, VCC2-GND2 = 20 V, GND2-VEE = 5 V, INA / INB = 5 V, 150 kHz, 50% Duty Cycle for 10 nF load, T_A = 25 °C, T_J = 150 ℃	1926	mW
Maximum power dissipation by transmitter side	P_{D1}		20	mW
Maximum power dissipation by receiver side	P_{D2}		1906	mW

2.6 Insulation Specifications

Parameter	Symbol	Conditions	Value	Unit
Withstand isolation voltage	V_{ISO}[1]	V_{TEST} = V_{ISO} = 3750 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 4500 V_{RMS}, t = 1 s (100% production)	3750	V_{RMS}
Maximum isolation working voltage	V_{IOWM}[2]	AC voltage (sine wave) Time Dependent Dielectric Breakdown (TDDB) test	970	V_{RMS}
		DC voltage	1375	V_{DC}
Insulation resistance, input to output	R_{IO}[2]	V_{IO} = 500 V, T_S = 150°C	≥ 10^9	Ω

1. Refer to UL 1577
2. Refer to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01

2.7 Safety Limiting Values

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Safety input, output, or supply current	I_S	$R_{θJA}$ = 64.9°C/W, V_{CC2} = 15 V, V_{EE} = 5 V, T_J = 150°C, T_A = 25°C			96	mA
		$R_{θJA}$ = 64.9°C/W, V_{CC2} = 20 V, V_{EE} = 5 V, T_J = 150°C, T_A = 25°C			77	mA
Safety input, output, or total power	P_S	$R_{θJA}$ = 64.9°C/W, V_{CC2} = 20 V, V_{EE} = 5 V, T_J = 150°C, T_A = 25°C			1926	mW
Safety temperature	T_S				150	°C

For electrical characteristics, the external circuit of the gate driver is shown in Figure 2.
RON = ROFF = 0 Ω and CL = 100 pF unless otherwise noted.

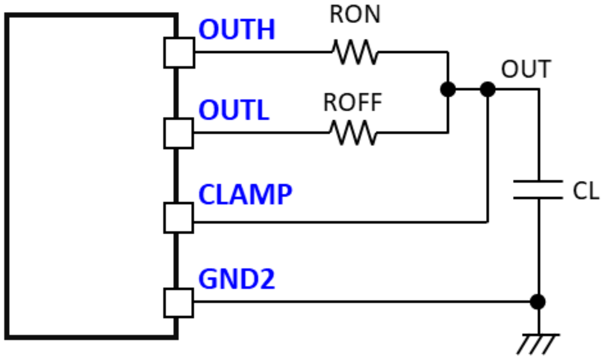


Figure 2. External circuit of the gate driver

2.8 Electrical Specifications

VCC1 = 5 V, VCC2 - GND2 = 20 V, GND2 – VEE = 0 V, CL = 100 pF, -40 °C < T_J < 150 °C unless otherwise noted.

Table 2. Electrical characteristics (1/5)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC1 UVLO THRESHOLD AND DELAY						
VCC1–GND1	V_{VCC1_ON}		3.9	4.2	4.5	V
	V_{VCC1_OFF}		3.8	4.1	4.4	V
	V_{VCC1_HYS}			0.1		V
VCC1 UVLO on delay to output high	$t_{VCC1+ \text{ to } OUT}$	INA = VCC1, INB = GND1	15	30	60	µs
VCC1 UVLO off delay to output low	$t_{VCC1- \text{ to } OUT}$	VCC1 > 3.6V	5	10	25	µs
VCC1 UVLO on delay to RDY high	$t_{VCC1+ \text{ to } RDY}$	RSTB = VCC1	15	30	60	µs
VCC1 UVLO off delay to RDY low	$t_{VCC1- \text{ to } RDY}$		5	10	25	µs

Table 3. Electrical characteristics (2/5)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC2 UVLO THRESHOLD AND DELAY						
VCC2–GND2	V_{VCC2_ON}		10	11	12	V
	V_{VCC2_OFF}		9	10	11	V
	V_{VCC2_HYS}			1.0		V
VCC2 UVLO on delay to output high	$t_{VCC2+ \text{ to } OUT}$	INA= VCC1, INB = GND1 SR of VCC2 = 10 mV/µs		10	20	µs
VCC2 UVLO off delay to output low	$t_{VCC2- \text{ to } OUT}$			5	15	µs
VCC2 UVLO on delay to RDY high	$t_{VCC2+ \text{ to } RDY}$	RSTB = FOB=High SR of VCC2 = 10 mV/µs		10	20	µs
VCC2 UVLO off delay to RDY low	$t_{VCC2- \text{ to } RDY}$			10	20	µs
VCC1, VCC2 QUIESCENT CURRENT						
VCC1 quiescent current	I_{VCC1Q}	OUTH = High, f_S = 0 Hz	1.45	2	3.2	mA
		OUTL = Low, f_S = 0 Hz	1.45	2	3.2	mA
VCC2 quiescent current	I_{VCC2Q}	OUTH = High, f_S = 0 Hz	2.0	4	5.9	mA
		OUTL = Low, f_S = 0 Hz	2.0	3.7	5.3	mA
LOGIC INPUTS — INA, INB and RSTB						
Input high threshold	V_{INH}	VCC1 = 5 V	0.7×VCC1			V
Input low threshold	V_{INL}	VCC1 = 5 V			0.3×VCC1	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input threshold hysteresis	V_{IN_HYS}	VCC1 = 5 V		0.12×VCC1		V

VCC1 = 5 V, VCC2 - GND2 = 20 V, GND2 – VEE = 0 V, CL = 100 pF, -40 °C < T_J < 150 °C unless otherwise noted.

Table 4. Electrical characteristics (3/5)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOGIC INPUTS —INA, INB and RSTB						
Input pins pull-down resistance	R_{IND}	INA = VCC1 RSTB = VCC1		55		kΩ
Input pins pull-up resistance	R_{INU}	INB = GND1		55		kΩ
INA, INB and RSTB deglitch (ON and OFF) filter time	t_{INFIL}	f_S = 50 kHz	28	40	60	ns
Deglitch filter time to reset FOB	t_{RSTFIL}		1.0	-	8.0	us
GATE DRIVER STAGE						
Peak source current	I_{OUTH}	CL = 0.18 μF, f_S = 1 kHz		-10		A
Peak sink current	I_{OUTL}			10		A
Output pull-up resistance	R_{OUTH}	I_{OUTH} = -0.1 A		2.5		Ω
Output pull-down resistance	R_{OUTL}	I_{OUTL} = 0.1 A		0.3		Ω

Table 5. Electrical characteristics (4/5)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ACTIVE PULL-DOWN						
Output active pull-down on OUTL	V_{OUT_PD}	I_{OUTL} = 1 A (IOUTL(typ)x0.1), VCC2 = OPEN			2.5	V
INTERNAL ACTIVE MILLER CLAMP						
Miller clamp threshold voltage	$V_{CLAMPTH}$	Reference to VEE	1.5	2	2.5	V
Output low clamp voltage	V_{CLAMP}	I_{CLAMP} = 1 A		VEE + 0.5		V
Output low clamp current	I_{CLAMP}	CLAMP = 0 V, VEE = -2.5 V		4		A
Miller clamp pull-down resistance	R_{CLAMP}	I_{CLAMP} = 0.2 A		0.6		Ω
Miller clamp ON delay time	t_{DCLAMP}	CL = 1.8 nF		15	50	ns
SHORT CIRCUIT CLAMPING						
OUTH-VCC2	V_{CLP_OUTH}	I_{OUTH} = 500 mA, t_{CLP} = 10 μs		0.8	1.0	V
OUTL-VCC2	$V_{CLP-OUTL}$	I_{OUTL} = 500 mA, t_{CLP} = 10 μs		1.55	1.8	V
CLAMP-VCC2	$V_{CLP-CLAMP}$	I_{CLAMP} = 20 mA, t_{CLP} = 10 μs		0.9		V

VCC1 = 5 V, VCC2 - GND2 = 20 V, GND2 – VEE = 0 V, CL = 100 pF, -40 °C < T_J < 150 °C unless otherwise noted.

Table 6. Electrical characteristics (5/5)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OVER CURRENT PROTECTION WITH CURRENT SENSE						
CS pull-down current	I_{DCHG}	CS = 1 V		40		mA
CS detection threshold	V_{CSTH}		0.63	0.7	0.77	V
CS output low voltage	V_{CSL}	ICS = 5 mA, Reference to GND2		0.13		V
CS fault deglitch filter	t_{CSFIL}		50	140	230	ns
CS propagation delay to OUTL 90%	t_{CSOFF}		60	220	300	ns
CS to FOB low delay	t_{CSFOB}		60	400	1600	ns
INTERNAL SOFT TURN-OFF						
Soft turn-off current on fault conditions	I_{STO}	OUTL = VEE + 8 V	250	400	570	mA
FOB AND RDY REPORTING						
VCC1 and VCC2 UVLO RDY low minimum holding time	t_{RDYHLD}		0.20		1	ms
Output mute time on fault	$t_{FOBMUTE}$	Reset fault through RSTB	0.20		1	ms
Open drain low output voltage	V_{ODL}	IODON = 5 mA			0.3	V
COMMON MODE TRANSIENT IMMUNITY						
Common-mode transient immunity	CMTI		150			V/ns

VCC1 = 5 V, VCC2 - GND2 = 20 V, GND2 – VEE = 0 V, CL = 100 pF, -40 °C <T_J<150 °C unless otherwise noted

Table 7. Switching characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Propagation delay time – high to low	t_{PDHL}	CL = 100 pF	30	70	140	ns
Propagation delay time – low to high	t_{PDLH}	CL = 100 pF	30	70	140	ns
Pulse width distortion $\|t_{PDHL} – t_{PDLH}\|$	PWD				30	ns
Part-to-part skew	t_{sk-pp}	Rising or falling propagation delay difference due to process deviation			50	ns
Driver output rise time	t_r	CL = 10 nF		33		ns
Driver output fall time	t_f	CL = 10 nF		27		ns
Maximum switching frequency	f_{Smax}			1		MHz

Table 8. Thermal shutdown characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal shutdown temperature	T_{TSD}		150	175	200	°C
Thermal shutdown recover temperature	T_{TSDREC}		120	150	180	°C
Thermal shutdown hysteresis temperature	T_{TSDHYS}		15	25	35	°C

3. Typical Performance Graphs

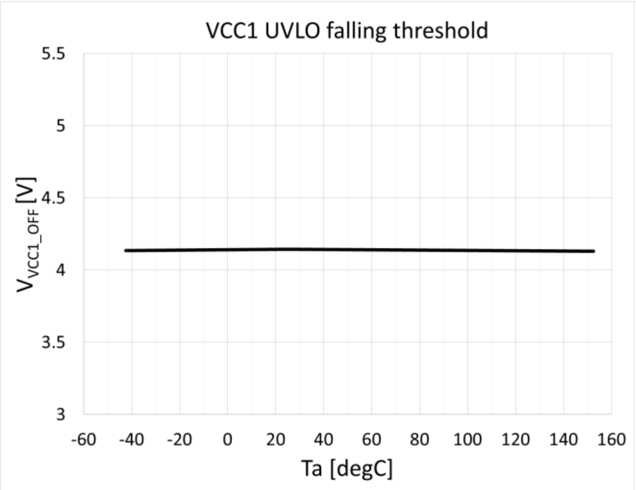


Figure 3. VCC1 UVLO falling threshold

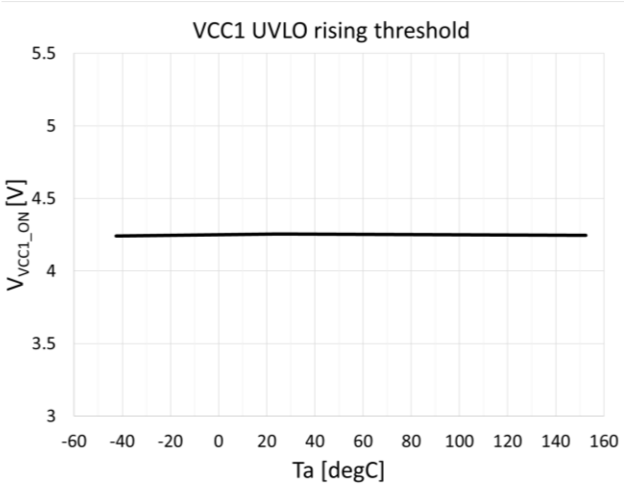


Figure 4. VCC1 UVLO rising threshold

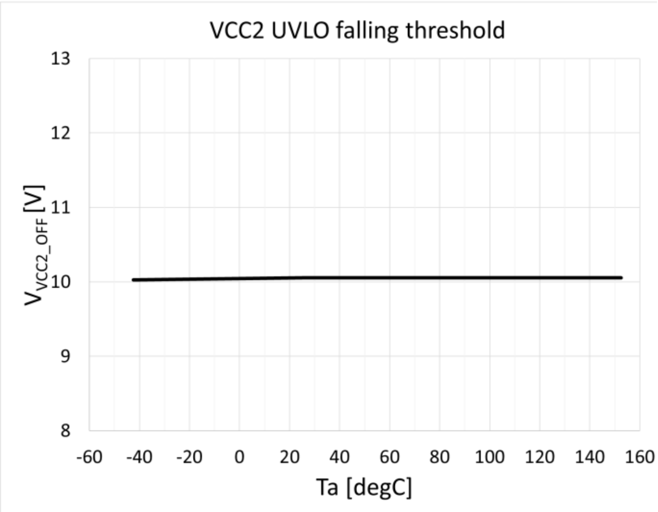


Figure 5. VCC2 UVLO falling threshold

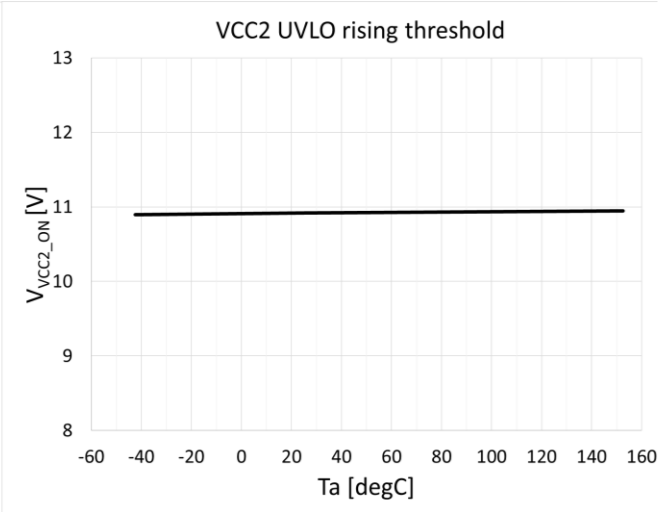


Figure 6. VCC2 UVLO rising threshold

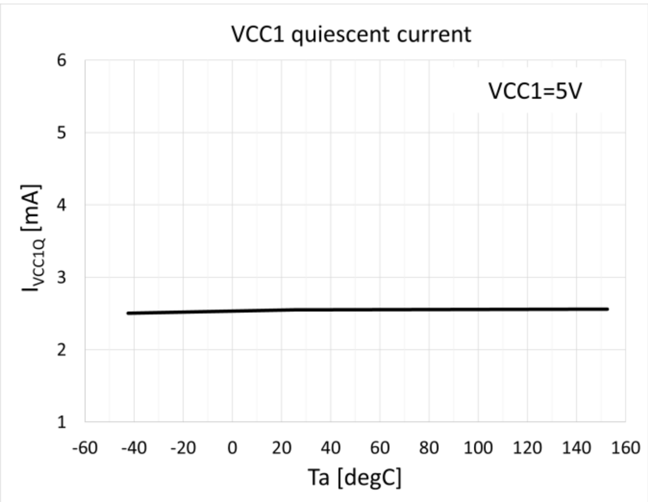


Figure 7. VCC1 quiescent current

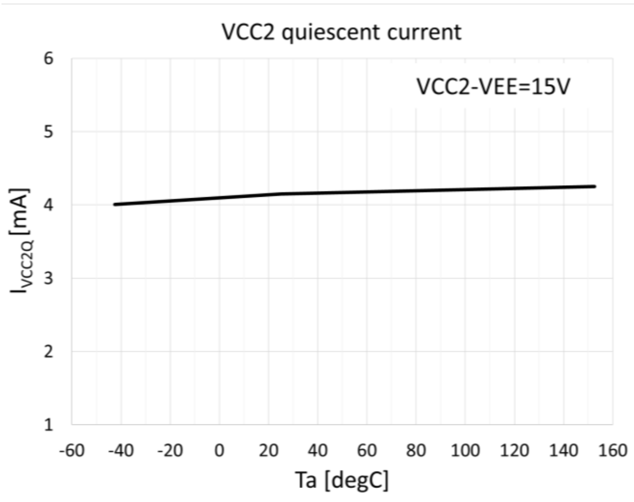


Figure 8. VCC2 quiescent current

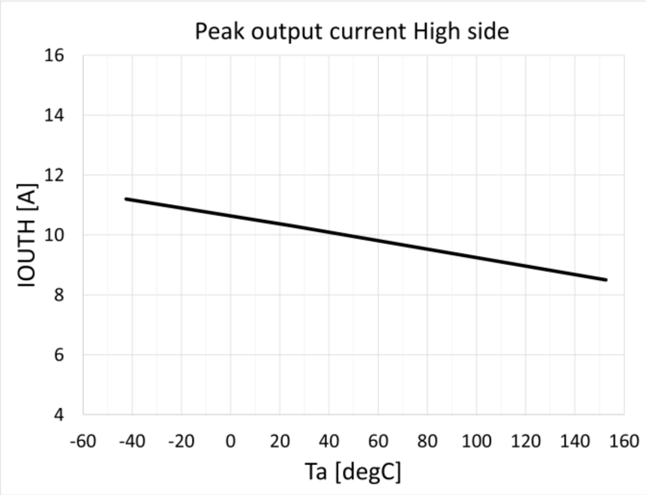


Figure 9. Peak output current high side

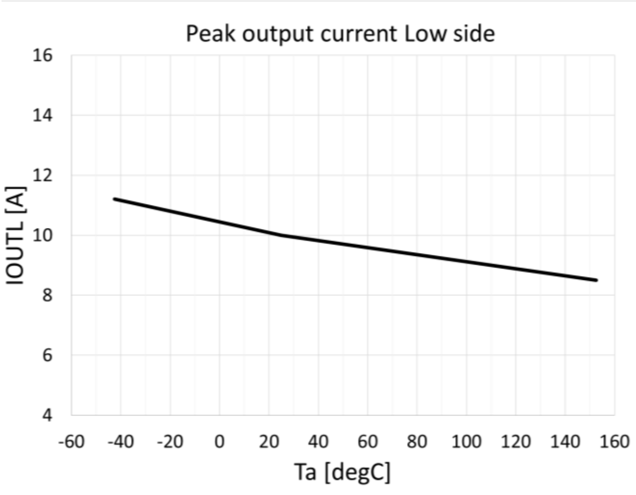


Figure 10. Peak output current low side

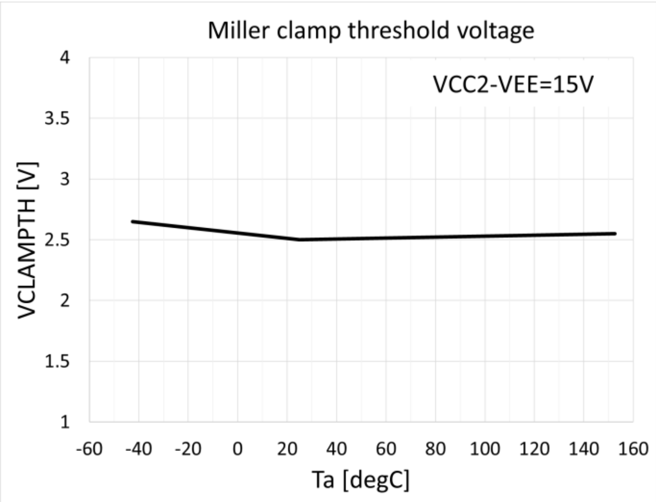


Figure 11. Miller clamp threshold voltage

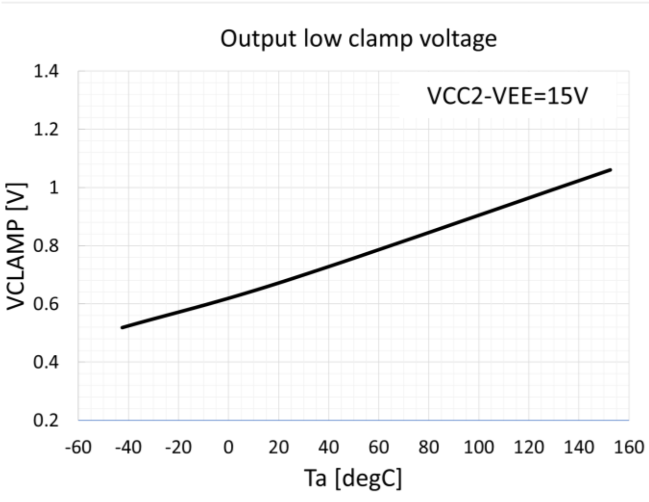


Figure 12. Output low clamp voltage

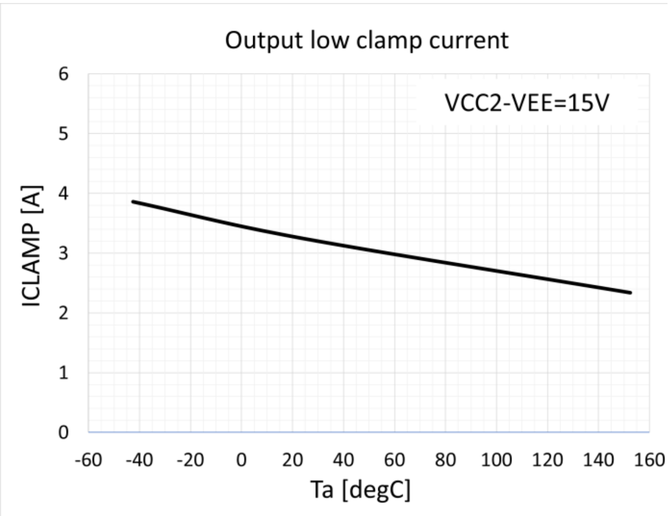


Figure 13. Output low clamp current

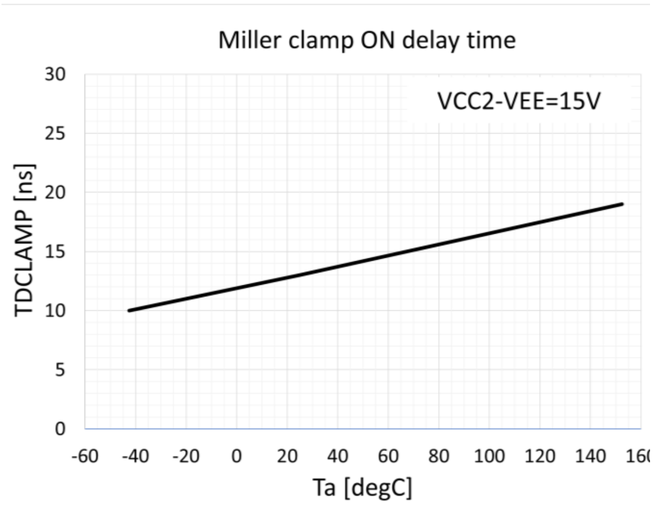


Figure 14. Miller clamp on delay time

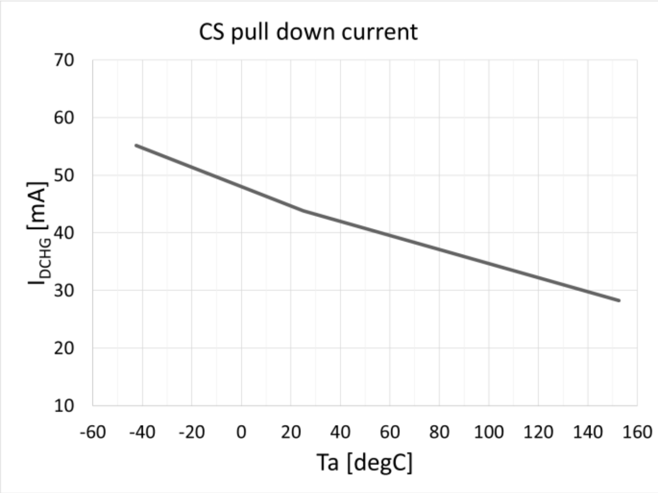


Figure 15. CS Pull-down current

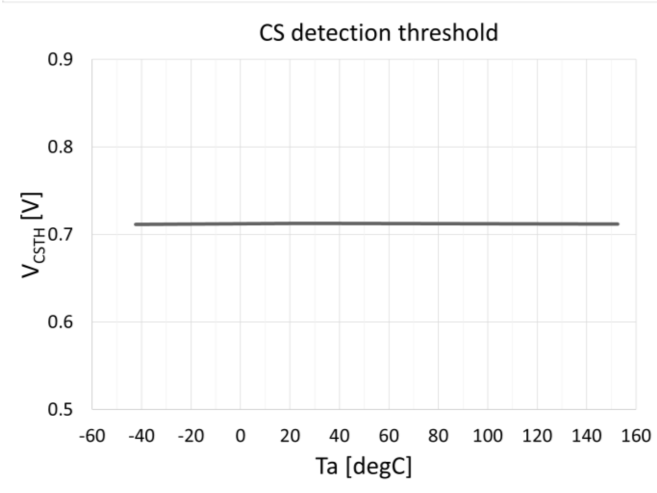


Figure 16. CS detection threshold

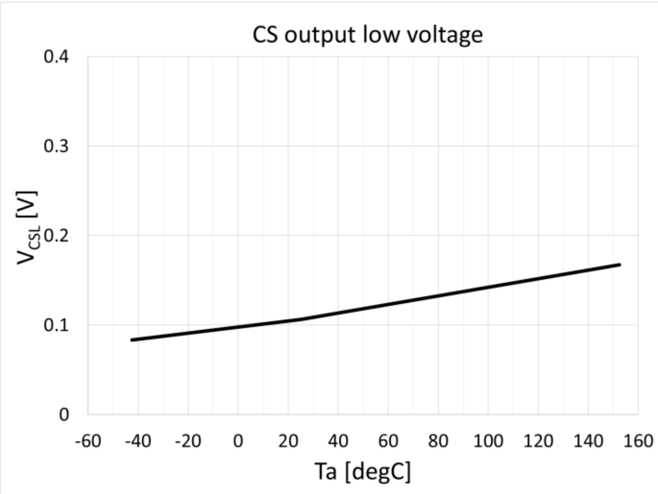


Figure 17. CS output low voltage

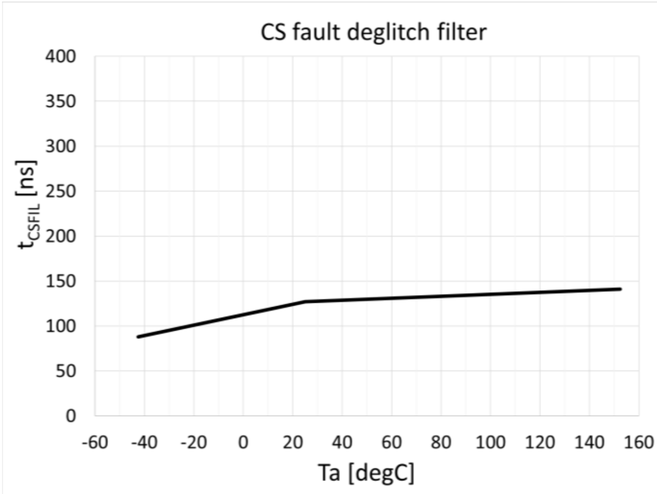


Figure 18. CS fault deglitch filter

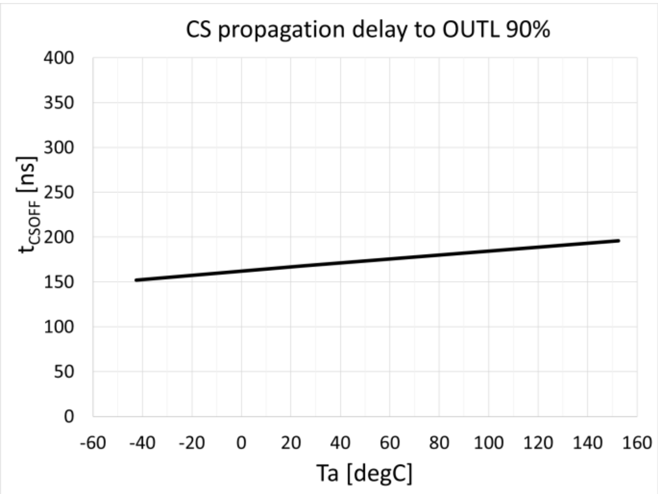


Figure 19. CS propagation delay to OUTL 90%

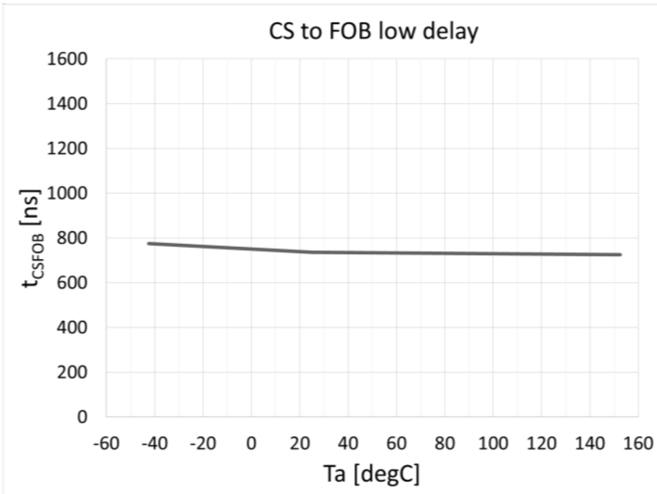


Figure 20. CS to FOB low delay

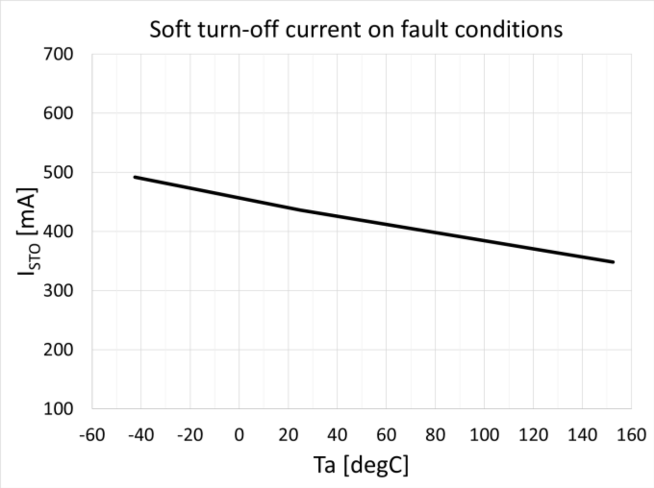


Figure 21. Soft turn-off on fault conditions

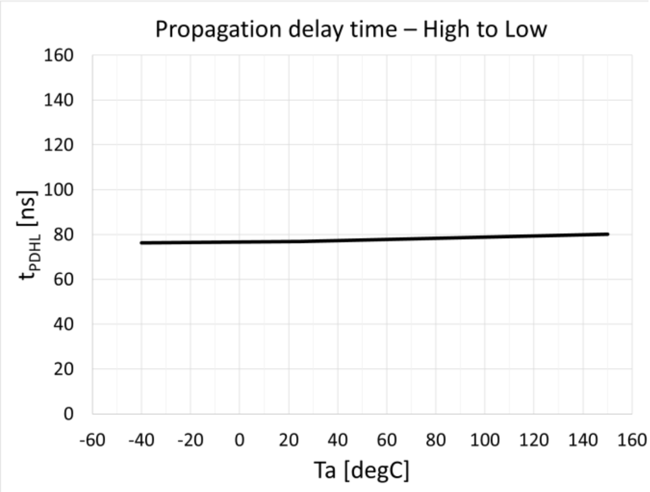


Figure 22. Propagation delay time - high to low

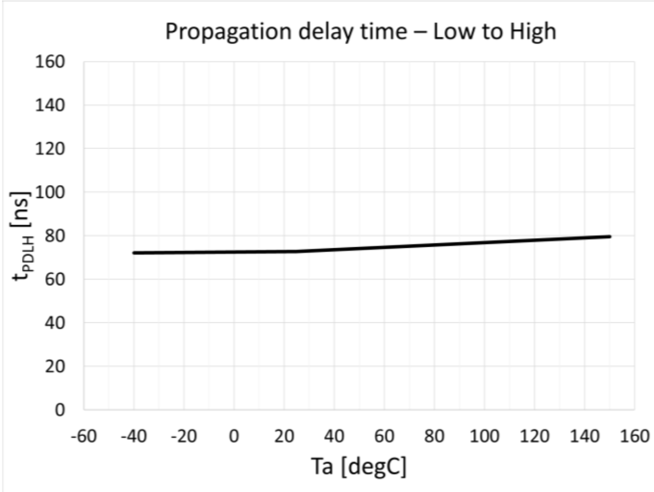


Figure 23. Propagation delay time - low - to high

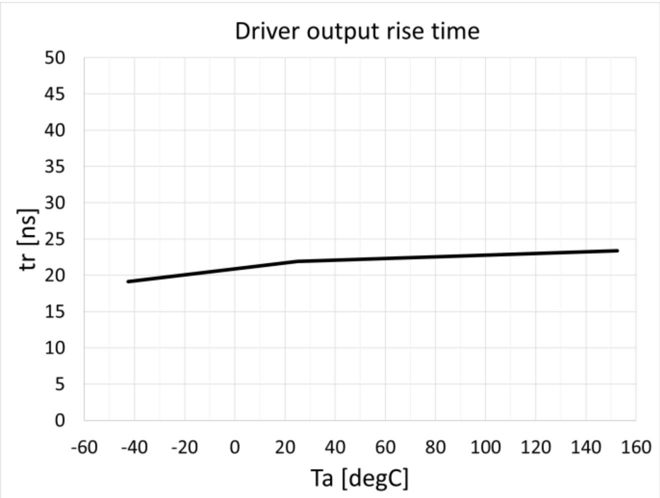


Figure 24. Driver output rise time

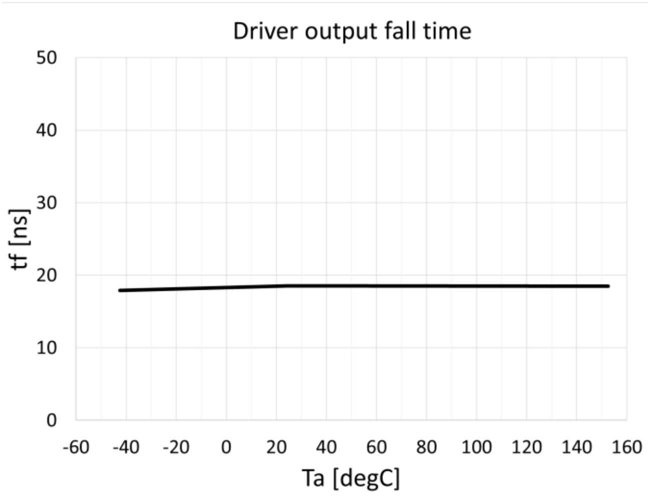


Figure 25. Driver output fall time

Table 9. Function table

		Supply			Input				Output			
No.	**State**	**VCC1**	**VCC2**	**VEE**	**Latched fault[1]**	**RSTB**	**INA**	**INB**	**RDY**	**FOB**	**OUTH/ OUTL**	**CLAMP**
1	VCC1 UVLO	PD	PU	PU	X	X	X	X	Low	HiZ	Low	Low
2	VCC2 UVLO	PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low
3	VCC2 Open	PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ
4	Current Sense and TSD	PU	PU	PU	Yes	X	X	X	HiZ	Low	Soft turn-off	Low
5	Reset	PU	PU	PU	No	Low	X	X	HiZ	HiZ	Low	Low
6	Normal operation	PU	PU	PU	No	High	Low	X	HiZ	HiZ	Low	Low
7		PU	PU	PU	No	High	X	High	HiZ	HiZ	Low	Low
8		PU	PU	PU	No	High	High	High	HiZ	HiZ	Low	Low
9		PU	PU	PU	No	High	High	Low	HiZ	HiZ	High	HiZ

1. Latched fault is reset at rise edge of RSTB.

PU: Power Up (VCC1 ≥ 4.5 V, VCC2 ≥ 12 V); PD: Power Down (3.2 V ≤ VCC1 ≤ 3.8 V, VCC2 ≤ 9 V); X: Irrelevant; HiZ: High Impedance

To drive the power devices, the following methods are recommended (See Table 13):

1. Fix the INA to L and use the INB to drive the power device.
2. Fix the INB to H and use the INA to drive the power device.
3. Make the INA and INB in a opposite phases to drive the power device.

Table 10. Recommended drive method

#	INA	INB	OUTH/OUTL	Power Device State
1	L	X	L	OFF
2	X	H	L	OFF
3	H	L	H	ON

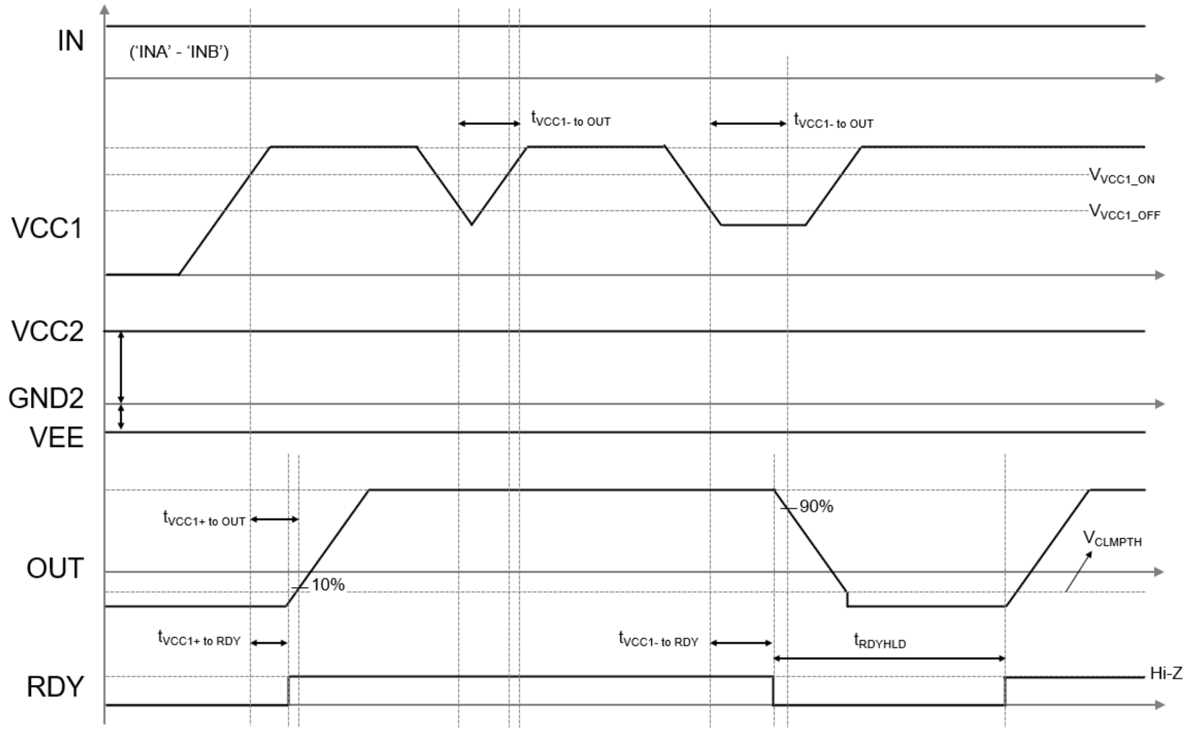


Figure 26. VCC1 UVLO protection timing diagram

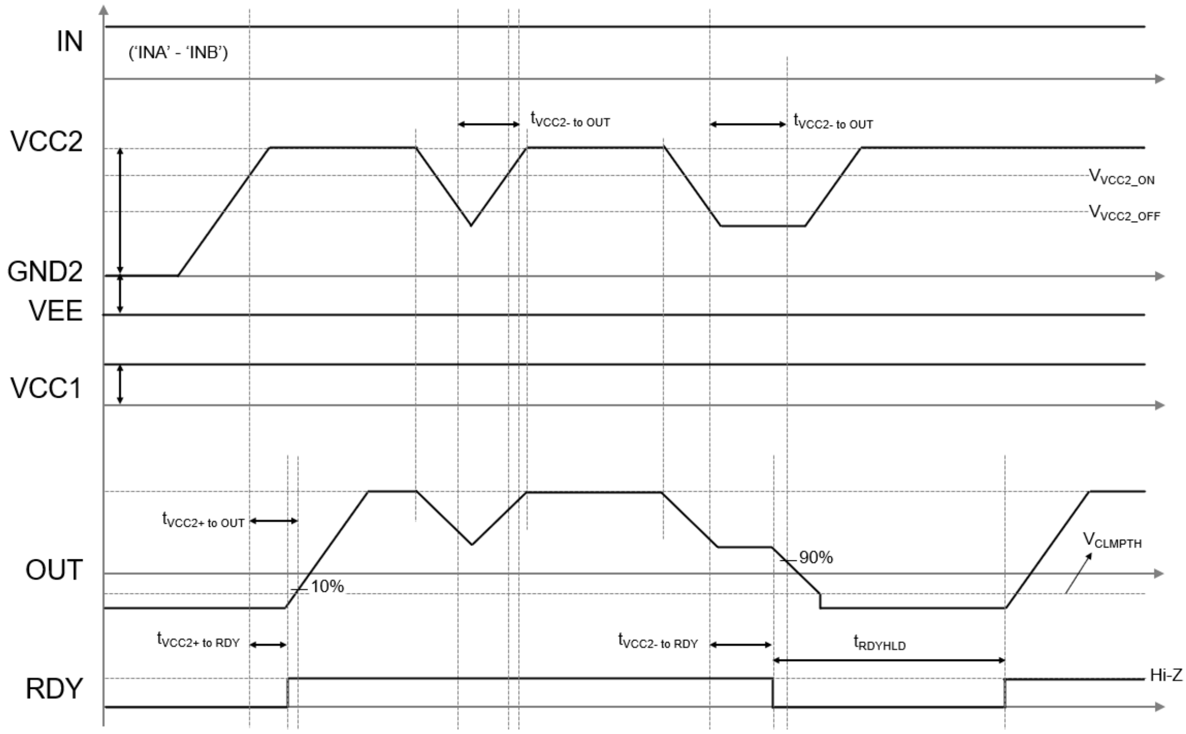


Figure 27. VCC2 UVLO protection timing diagram

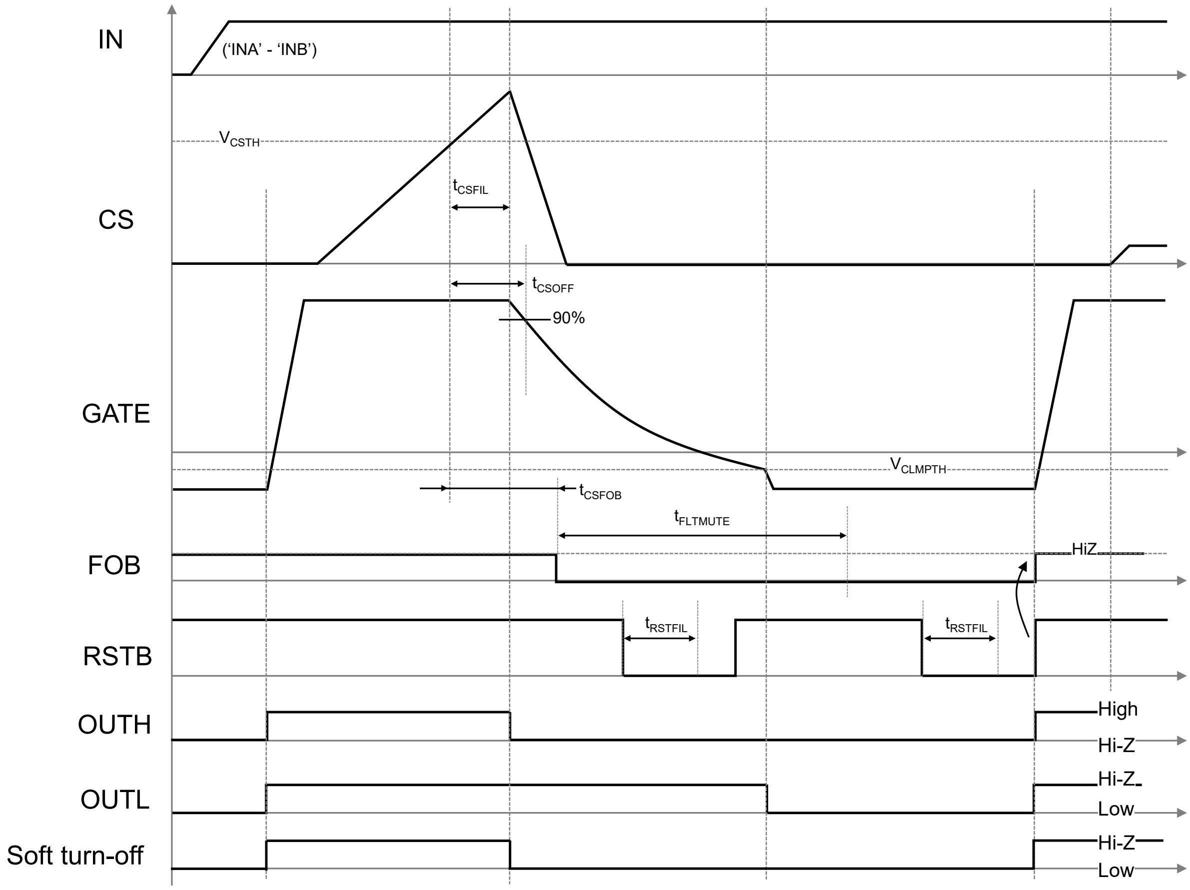


Figure 28. Timing diagram of current sense protection with soft turn-off during turn-on transition

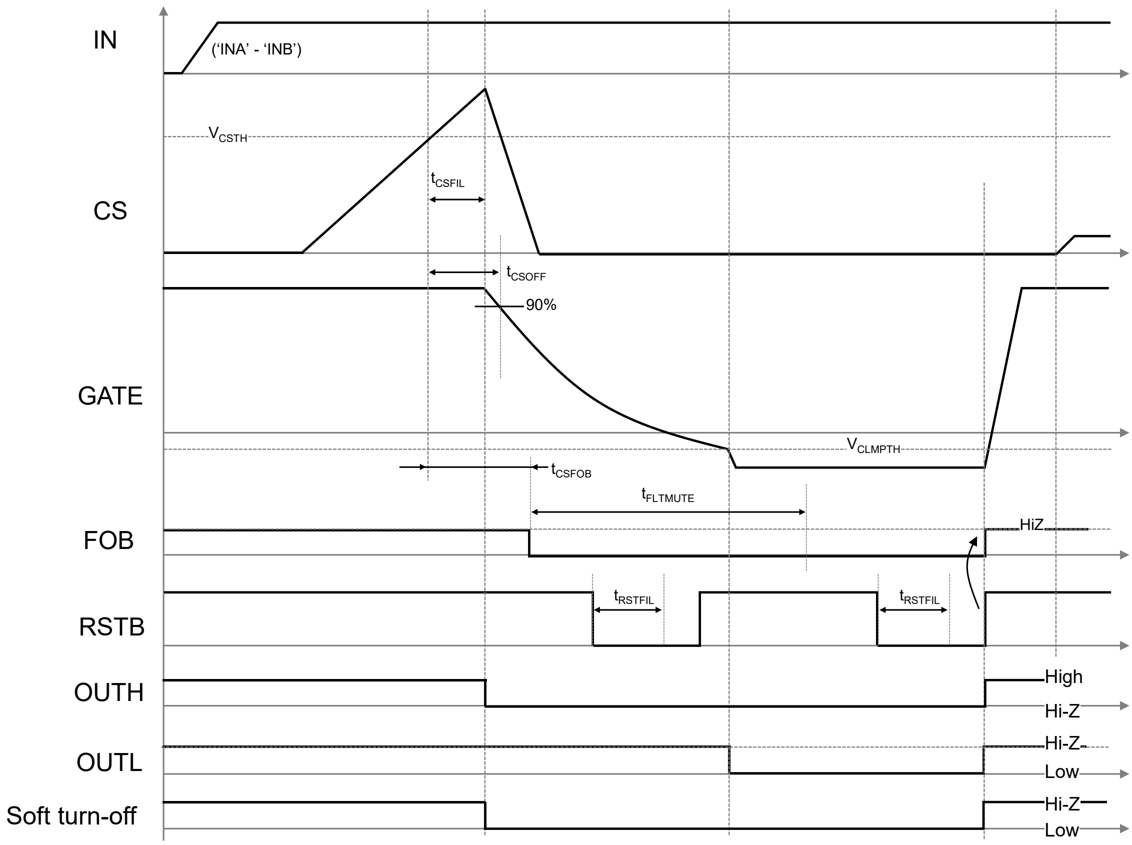


Figure 29. Timing diagram of current sense protection with soft turn-off while power device is on

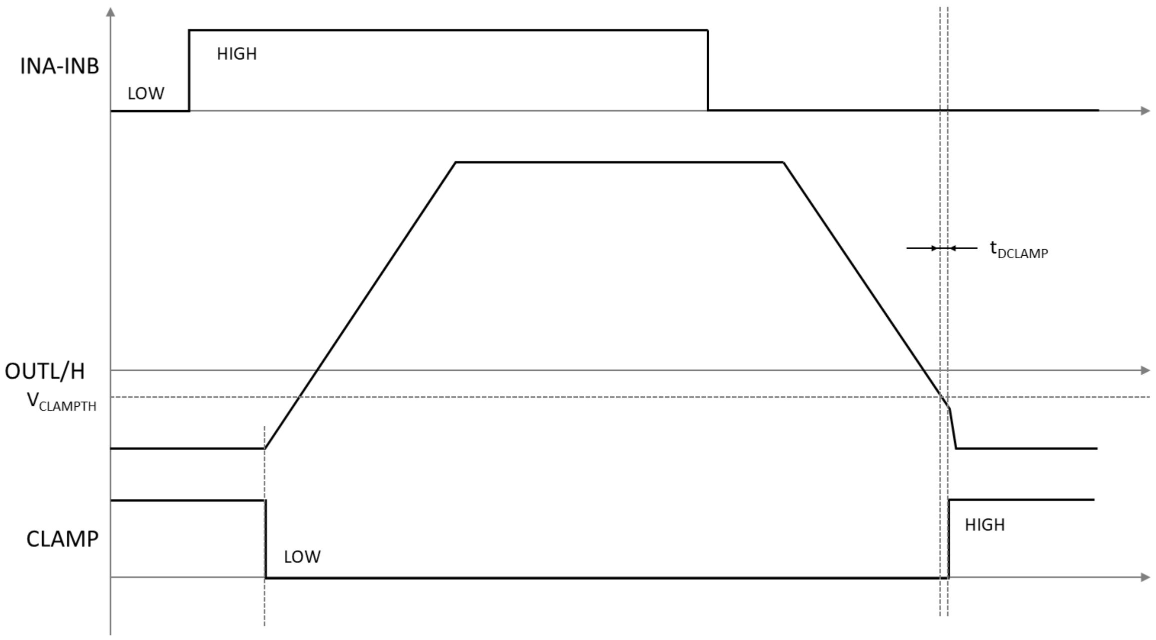


Figure 30. Timing diagram of active miller clamp

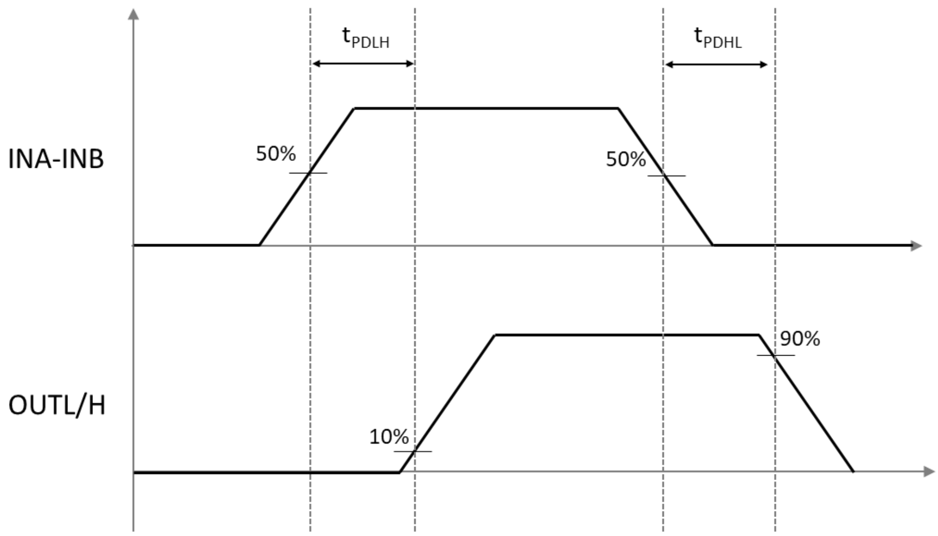


Figure 31. Timing diagram of propagation delay time

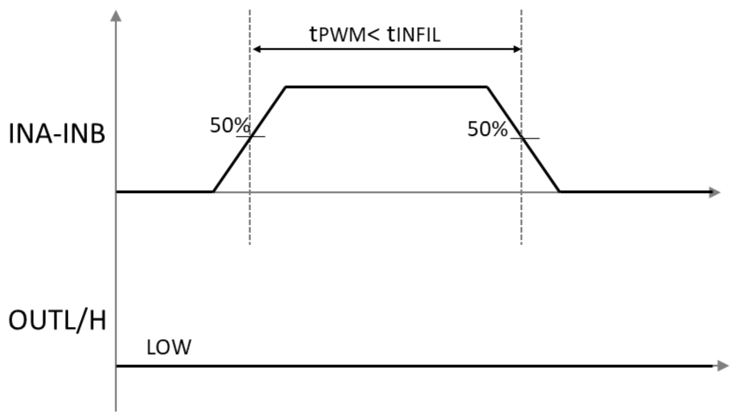


Figure 32. Timing diagram of on deglitch filter

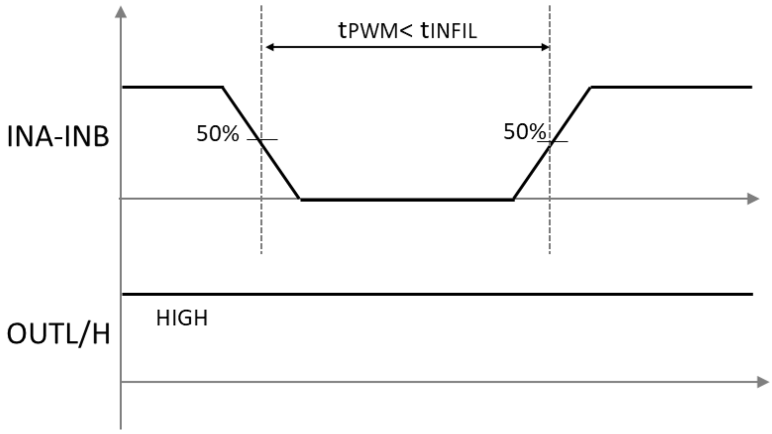


Figure 33. Timing diagram of off deglitch filter

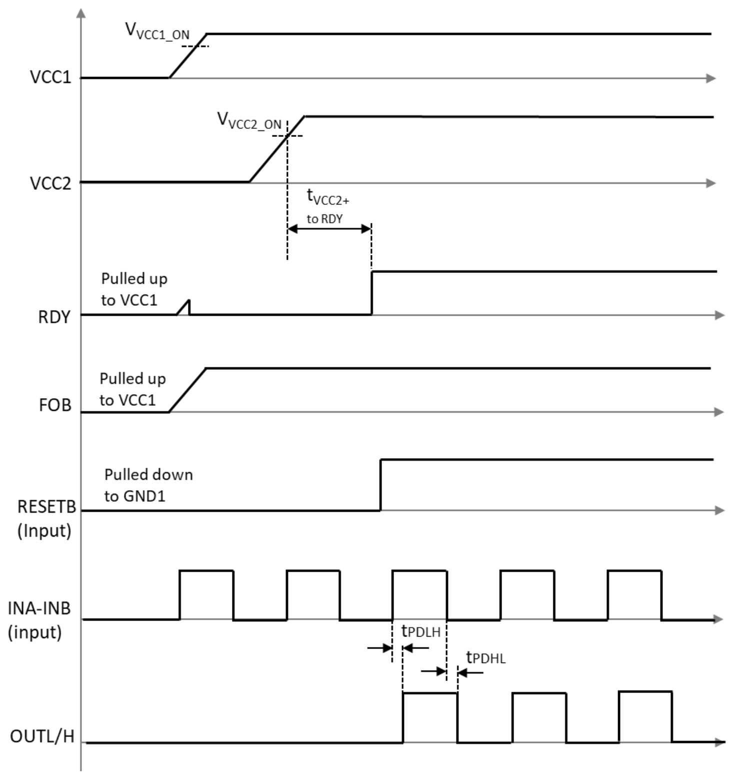


Figure 34. Timing diagram of power-up sequence

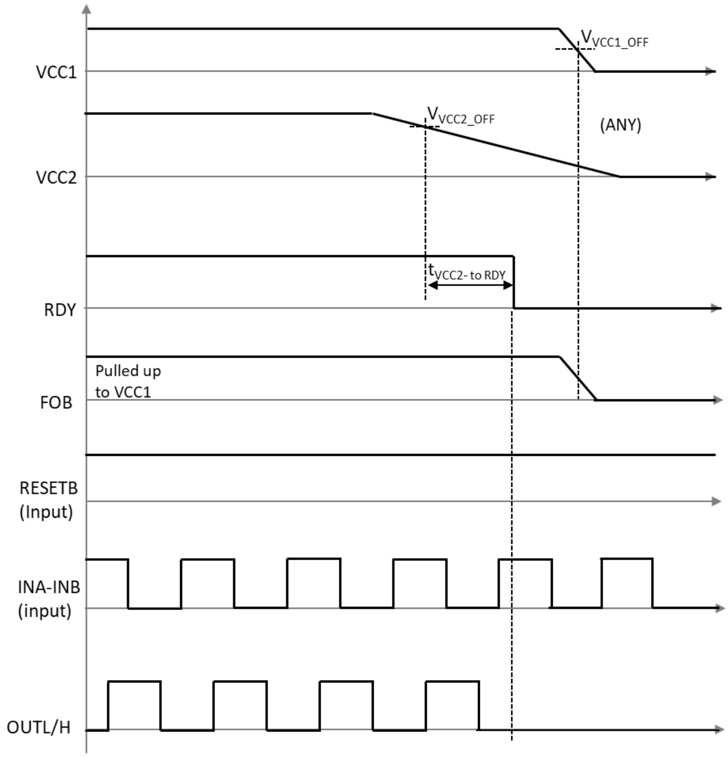


Figure 35. Timing diagram of power-down sequence

4. Functional description

The internal block of the RAJ2930004AGM is shown in figure 36.

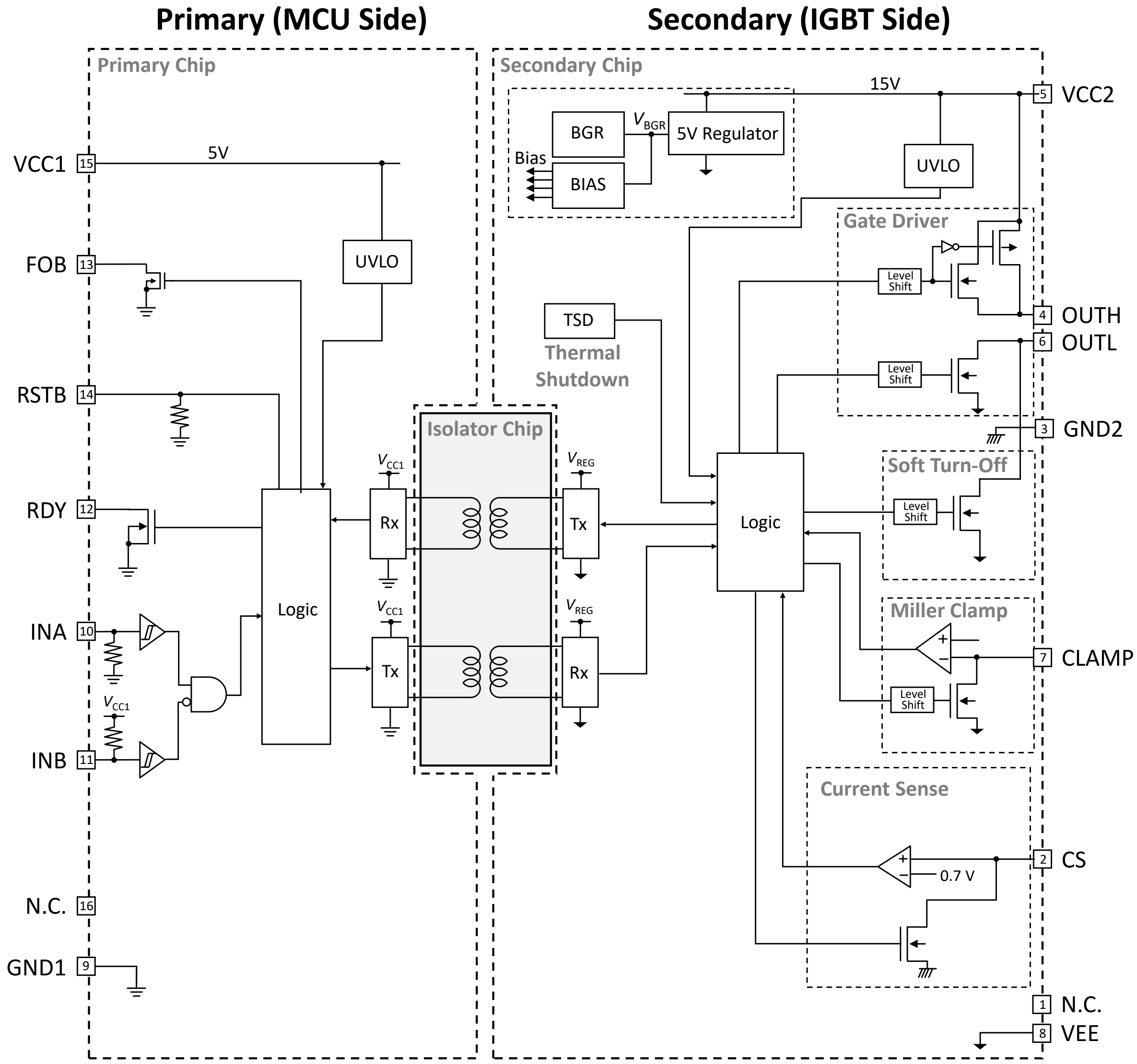


Figure 36. Internal block diagram

4.1 Gate Driver

4.1.1 Features

- The gate driver charges or discharges the IGBT gate pins.
- Gate drive output peak current (Source/Sink): 10 A (Typ)/10 A (Typ).
- Since the high-side gate drive output pin OUTH and the low-side gate drive output pin OUTL are independent of each other, the slew rates of the rise and fall of the gate voltage can be separately adjusted using the external resistors (RGH and RGL).
- The soft turn-off is the feature to lower the gate voltage of the IGBT gradually and turn it off when any of the following abnormal states are detected on the secondary circuit: DESAT or TSD.
- Switching operation can be resumed by RSTB when the abnormal states that caused soft turn-off returns to normal.
- Active pull-down resistance can clamp the OUTL pin to VEE when VCC2 is open. (Figure 38)
- Short circuit clamping diodes can clamp the OUTH/OUTL/CLAMP pins to VCC2 + V_f when the short circuit event occurs and the current input to the pins. (Figure 39)

4.1.2 Block Diagram

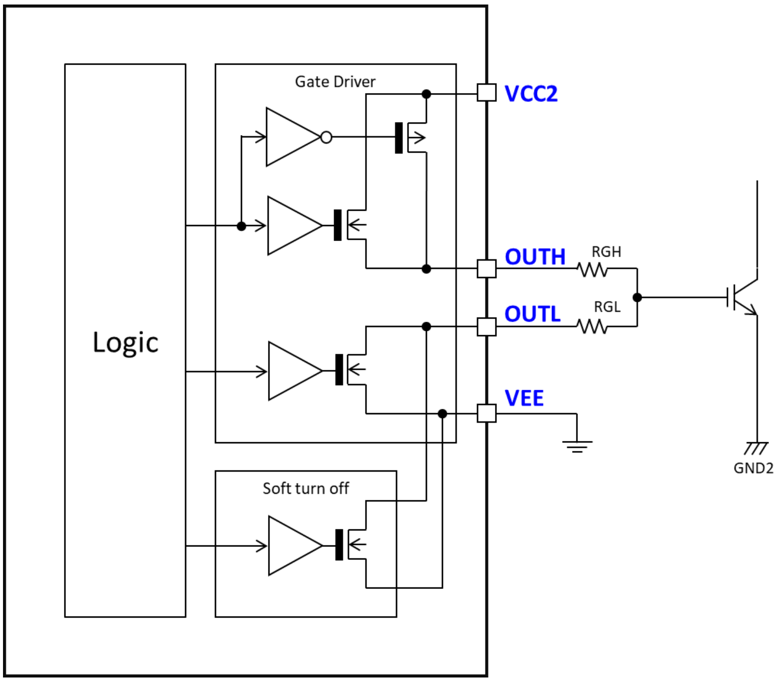


Figure 37. Block diagram of gate DRIVER

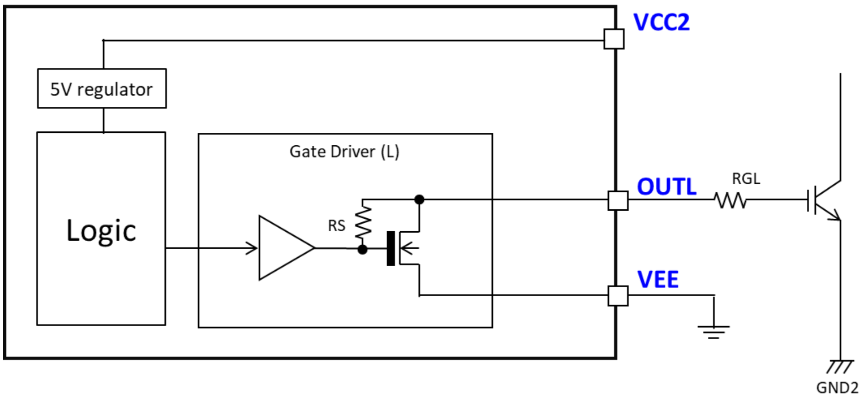


Figure 38. Block diagram of active pull-down

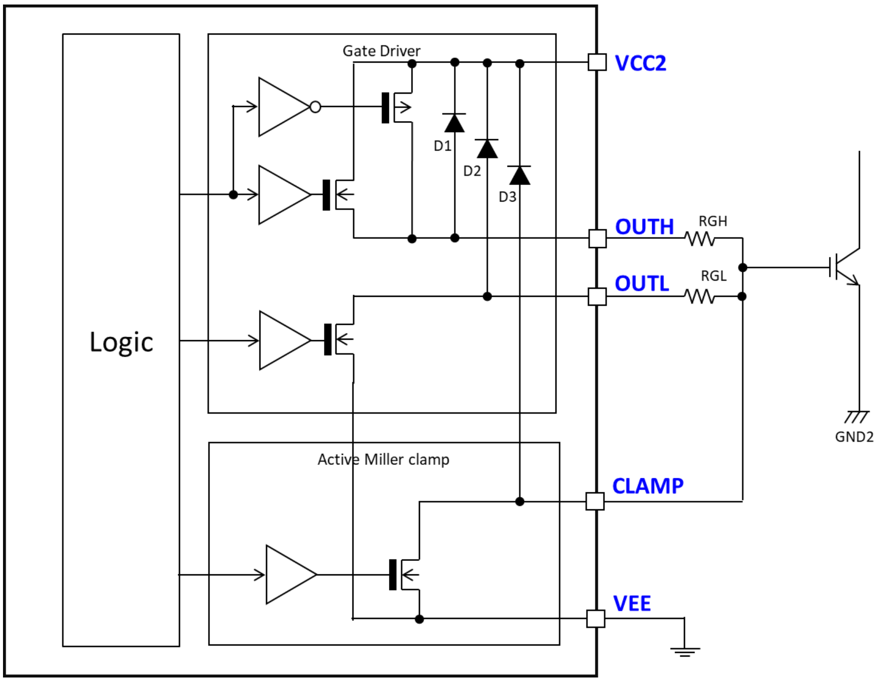


Figure 39. Block diagram of short circuit clamping

4.2 Active Miller Clamp

4.2.1 Features

- The active miller clamp is the feature to prevent the self turn-on of the IGBT due to the coupling capacitance between the IGBT gate and collector.
- If the CLAMP pin voltage falls below VCLAMP (2.0 V typ.) while the input signal to turn off the IGBT is applied to the INA or INB pin, the IGBT gate is short-circuited to the VEE pin with low resistance.

4.2.2 Block Diagram

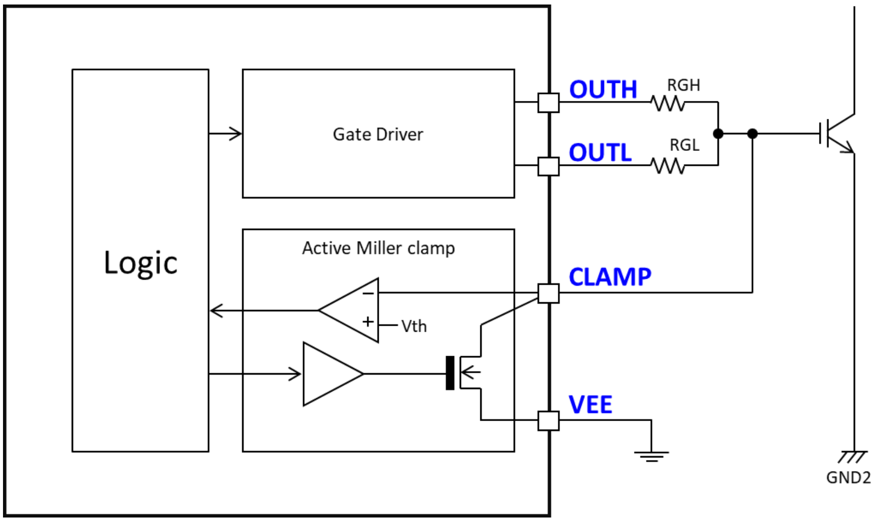


Figure 40. Block diagram of active miller clamp

4.3 UVLO

4.3.1 Features

- The primary circuit is equipped with a UVLO that detects a voltage drop of VCC1, and the UVLO turns off the IGBT (this is a normal turn-off operation different from a soft turn-off) when the VCC1 voltage drops below 4.1 V. At this time, the low level is output to the RDY pin of the primary circuit.
- The secondary circuit is equipped with a UVLO that detects the voltage drop of VCC2 and a UVLO that detects the voltage drop of VREG (output from 5 V regulator). The IGBT is turned off if the VCC2 voltage drops below 10 V or the VREG voltage drops below 4.1 V. At this time, the low level is output to the RDY pin of the primary circuit.

4.3.2 Block Diagram

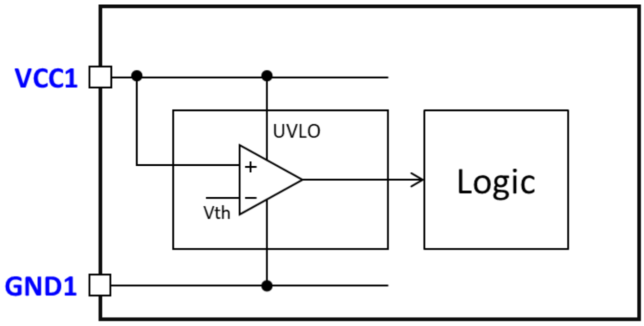


Figure 41. Block diagram of UVLO on primary chip

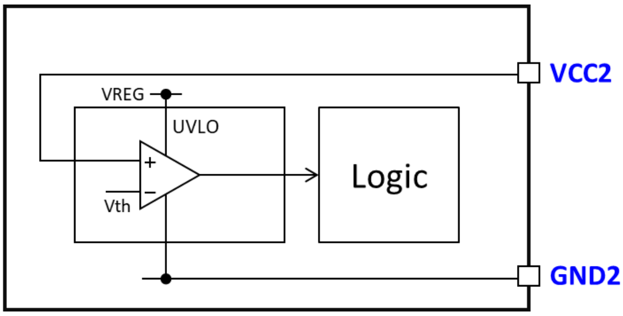


Figure 42. Block diagram of UVLO on secondary chip

4.4 Current Sense Protection

4.4.1 Features

- This feature turns off the output from the gate driver if the over-current is detected by current sense.
- The IGBT is soft turned-off if the voltage applied to the CS pin rises beyond the threshold voltage 0.7 V ± 10% when the IGBT is in the on-state. At this time, the low level is output to the FOB pin of the primary circuit.

4.4.2 Block Diagram

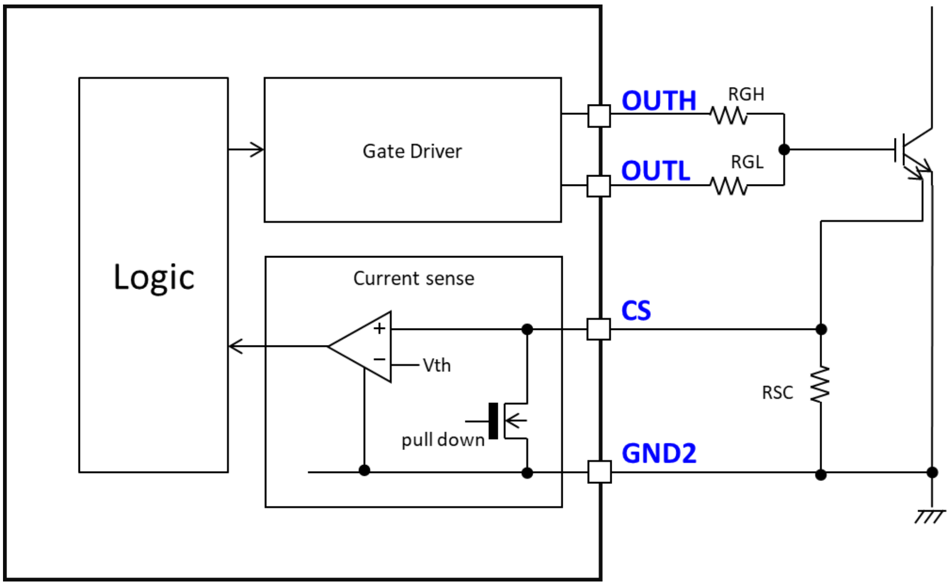


Figure 43. Block diagram of current sense

4.5 Isolation

4.5.1 Features

- On-chip micro isolator (Isolated circuit)
- High voltage isolation: 3750 V_{RMS}, 1 min
- High CMTI: over 150 kV/μs

4.5.2 Block Diagram

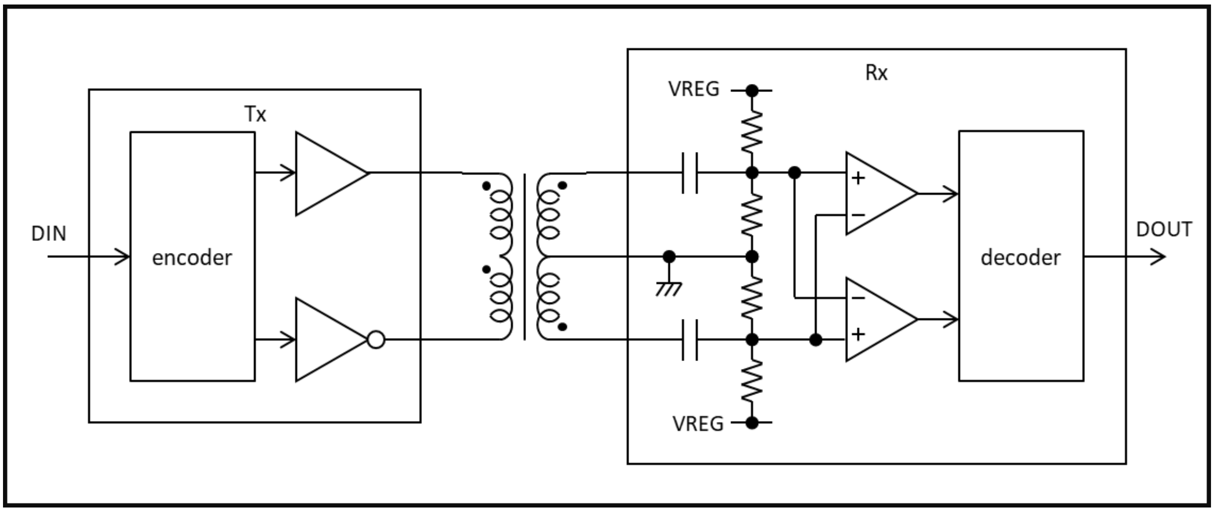


Figure 44. Block diagram of isolation

4.6 Thermal Shut Down (TSD)

4.6.1 Features

- This feature turns off the IGBT to prevent the damage on the IGBT due to malfunctioning of the IC when an extraordinary over-heat (175 °C TYP) is detected in the IC (TSD). Switching operation can be resumed by RSTB when IC's junction temperature is below the TSD recover temperature (typical hysteresis is 25 °C).

- Temperature sense diode is placed near the OUTH pin that tends to be heated in the IC. The IGBT is soft turned off if the temperature of the driver transistor in the IC exceeds a threshold value due to the overload or the increased ambient temperature. At this time, the low level is output to the FOB pin of the primary circuit.

4.6.2 Block Diagram

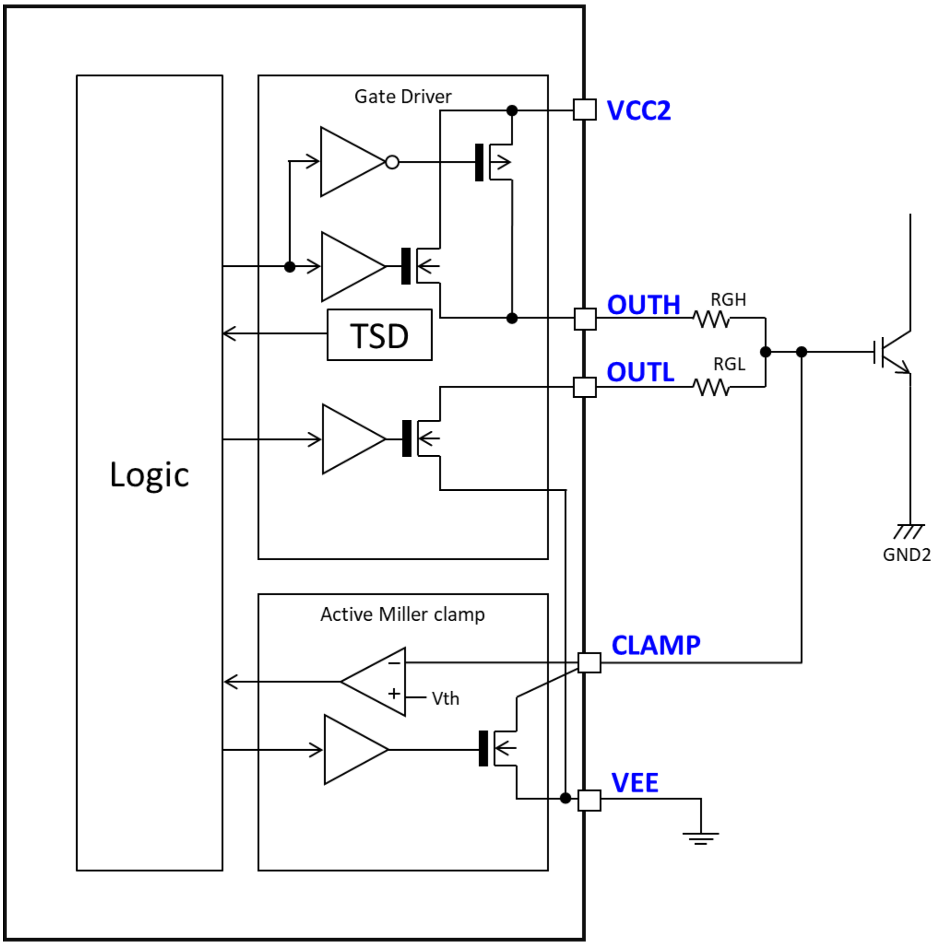


Figure 45. Block diagram of thermal shut down

4.7 Internal Regulator, Reference Voltage

4.7.1 Features

- For primary chip, supply voltage of internal circuit is supplied from external pin.
- For secondary chip, supply voltage of internal circuit is supplied from on-chip 5 V regulator.

4.7.2 Block Diagram

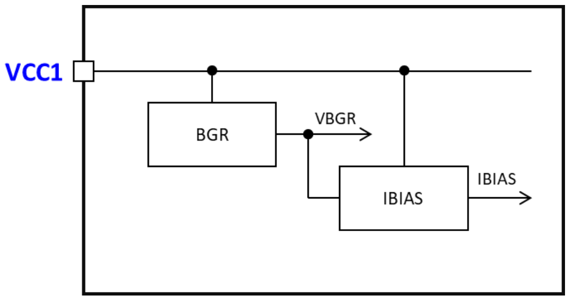


Figure 46. Block diagram of reference voltage on primary chip

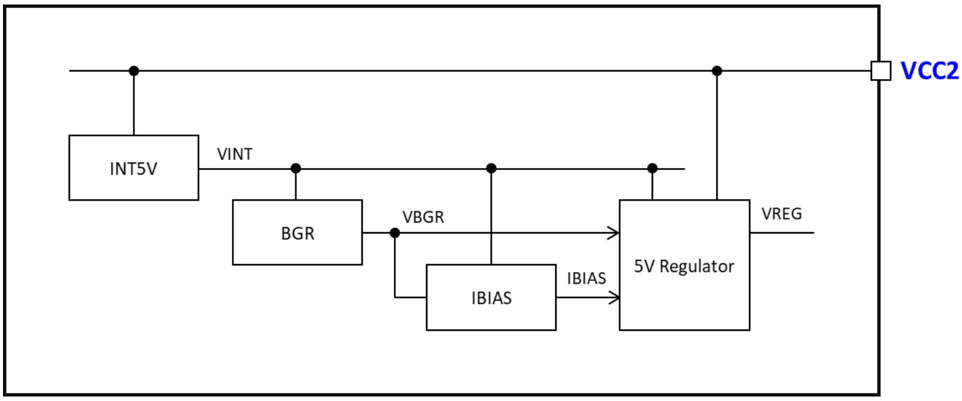


Figure 47. Block diagram of internal regulator and reference voltage on secondary chip

5. Example of Application Diagram

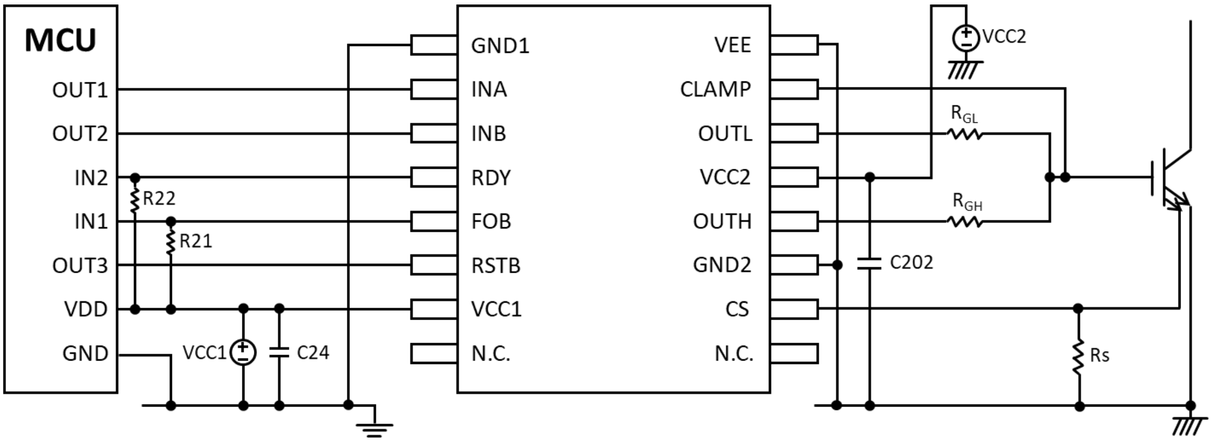


Figure 48. Simplified application diagram for IGBT

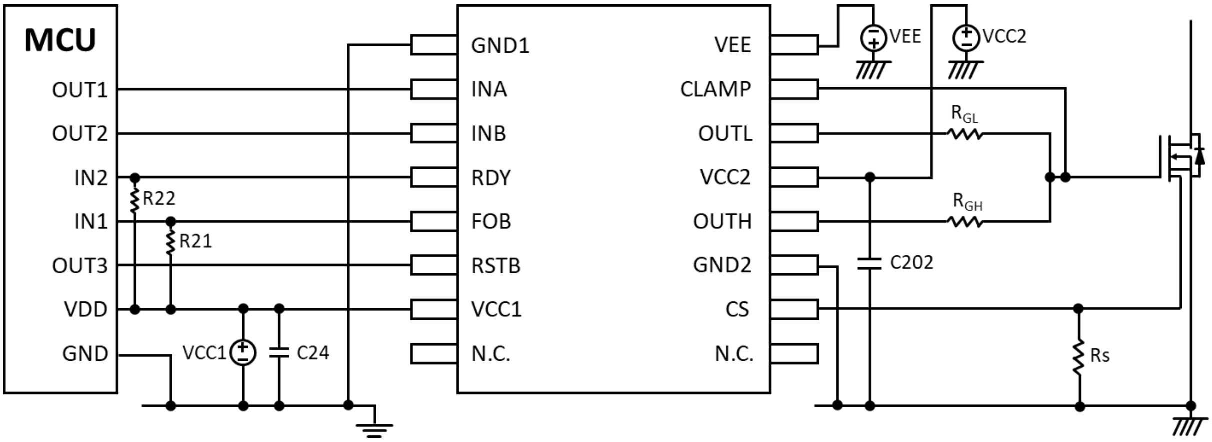


Figure 49. Simplified application diagram for SiC MOSFET

Table 11. Specifications of external components

Component	Specification
R21	5 kΩ/5%
R22	5 kΩ/5%
C24	0.1 µF/10%
C202	1 µF/10%
RGL(1)	5.1 Ω/5%
RGH(1)	5.1 Ω/5%
RS	2.0 Ω/5%

The type and unit price of the component (resistor RG) may differ depending on the specifications of the IGBT (gate charge, gate-emitter peak voltage, etc.). The rated power PG of the resistor RG connected to the IGBT can be calculated by equations 1 and 2.

$$P_{\mathrm{G}} = I_{\mathrm{G}}^2 R \quad (1)$$

$$I_{\mathrm{G}} = f_{\mathrm{C}} \times \left(\left|+Q_g\right| + \left|-Q_g\right|\right) \quad (2)$$

fc: Switching Frequency

$+Q_g$: Charge amount from 0 V to + V_{GE}

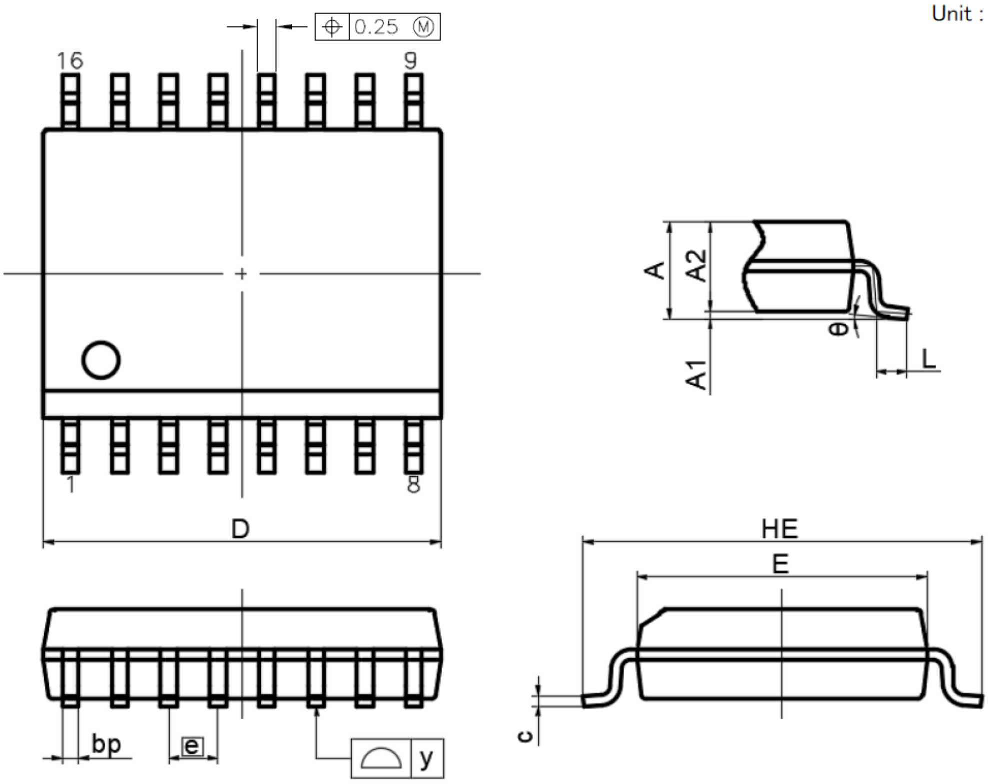
$-Q_g$: Charge amount from $-V_{GE}$ to 0 V

6. Package

Outline drawing SOP (PRSP0016DR-A)	RDK-G-001717-2
	Renesas Electronics Corporation

JEITA Package code	RENESAS code	MASS(TYP.) [g]
P-SOP16 7.5×10.3-1.27	PRSP0016DR-A	0.44[g]

Unit : mm



Reference Symbol	Dimension Millimeters		
	Min	Non	Max
D	10.15	—	10.41
E	7.44	—	7.59
A2	2.24	—	—
HE	10.01	—	10.63
A2	—	—	2.64
A1	0.10	—	0.29
bp	0.33	—	0.51
c	0.23	—	0.32
θ	0°	—	8°
e	—	1.27	—
y	—	—	0.10
L	0.51	—	1.02

7. Revision History

Revision	Date	Description
01.01	Jan 26.2026	Applied unified Renesas format.
01.00	Jun 8. 2024	Initial release.