RAA489108

Buck-Boost Narrow VDC Battery Charger with SMBus Interface Supporting USB PD EPR

The RAA489108 is a buck-boost Narrow Output Voltage DC (NVDC) charger. The RAA489108 provides NVDC charging, system bus regulation, and protection features for tablets, Ultrabooks, notebooks, power banks, and any USB-C interface platform. The advanced Renesas R3™ technology provides high light-load efficiency and fast transient response.

In Charging mode, the RAA489108 accepts input power from a wide range of DC power sources (such as conventional AC/DC charger adapters, USB PD ports, and travel adapters) and safely charges battery packs with up to 4-series cell Li-ion batteries.

As an NVDC topology charger, the RAA489108 also regulates the system output to a narrow DC range for stable system bus voltage. System power can be provided from the adapter, battery, or a combination of both. The RAA489108 can operate with only a battery, only an adapter, or with both connected. For Intel IMVP compliant systems, the RAA489108 includes PSYS (system power monitor) functionality, which provides an analog signal representing total platform power consumption. The PSYS output connects to a wide range of Renesas IMVP core regulators to provide an IMVP compliant power domain function.

The RAA489108 supports reverse buck, reverse boost, or reverse buck-boost operation to the input port from 2-cell to 4-cell batteries.

The RAA489108 provides SMBus/I^{2}C serial communication that enables programming of many critical parameters to deliver a customized solution.

Features

- Buck-boost NVDC charger for 2, 3, or 4-cell Li-ion batteries
- Input voltage range: 3.9V to 30V (no dead zone)
- System output voltage: 2.4V to 18.304V
- Autonomous charging option (automatic completion of charging)
- Pass-Through mode in forward direction
- System power monitor PSYS output, IMVP compliant
- Up to 1MHz switching frequency
- Adapter current and battery current monitor (AMON/BMON)
- PROCHOT# open-drain output, IMVP compliant
- Trickle charging of depleted battery
- Ideal diode control in Turbo mode
- Reverse buck, boost, and buck-boost operation from battery
- Two-level adapter current limit available
- Battery Ship mode option
- SMBus and auto-increment I^{2}C compatible
- 4×4 32 Ld TQFN package compatible with the ISL9238 family of parts

Applications

- 2-cell to 4-cell tablets, Ultrabooks, notebooks, power banks, and any USB-C interface portable device requiring batteries

Contents

1. Overview

1.1 Typical Application Diagrams

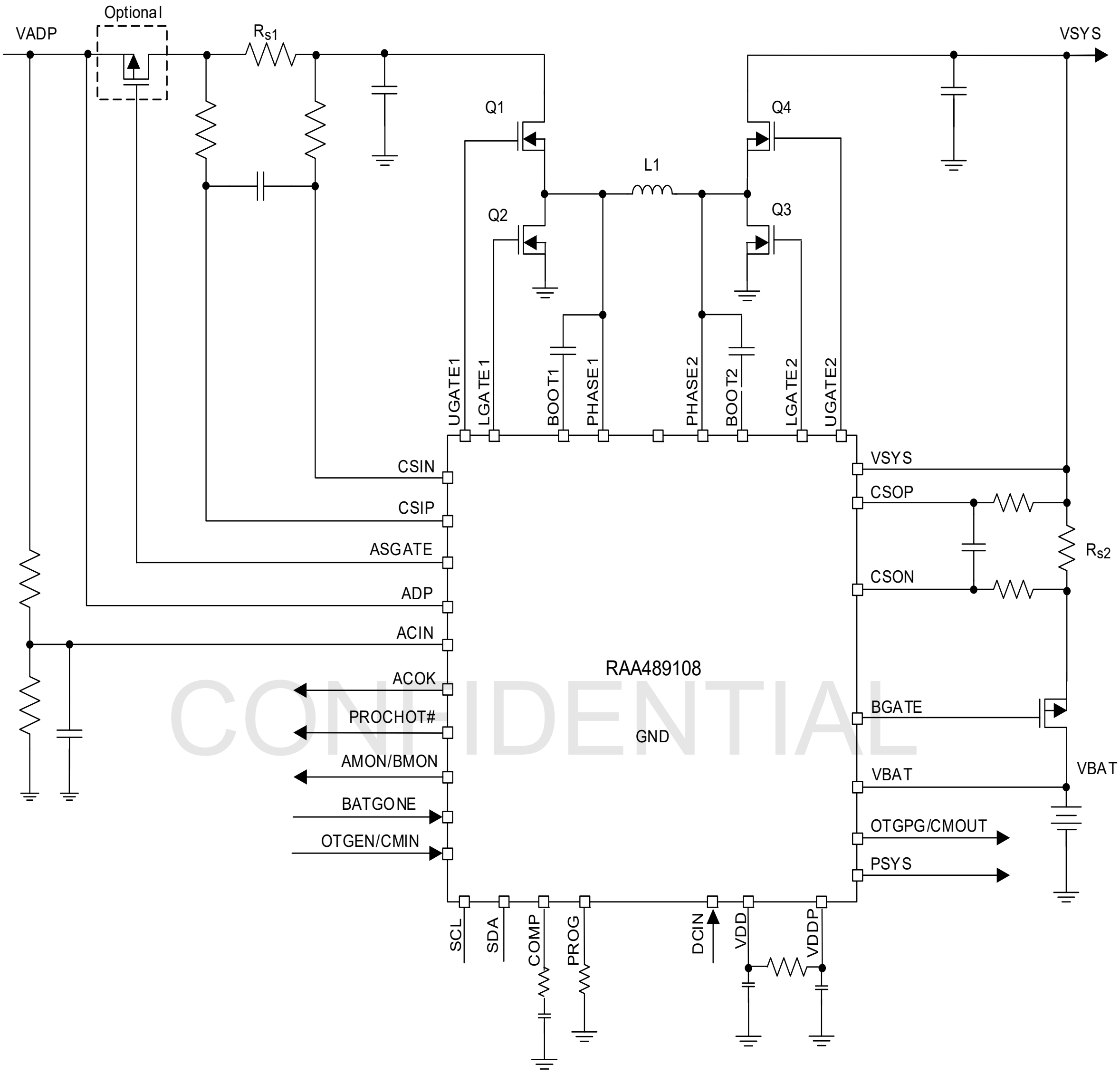


Figure 1. Typical Application Circuit

1.2 Block Diagram

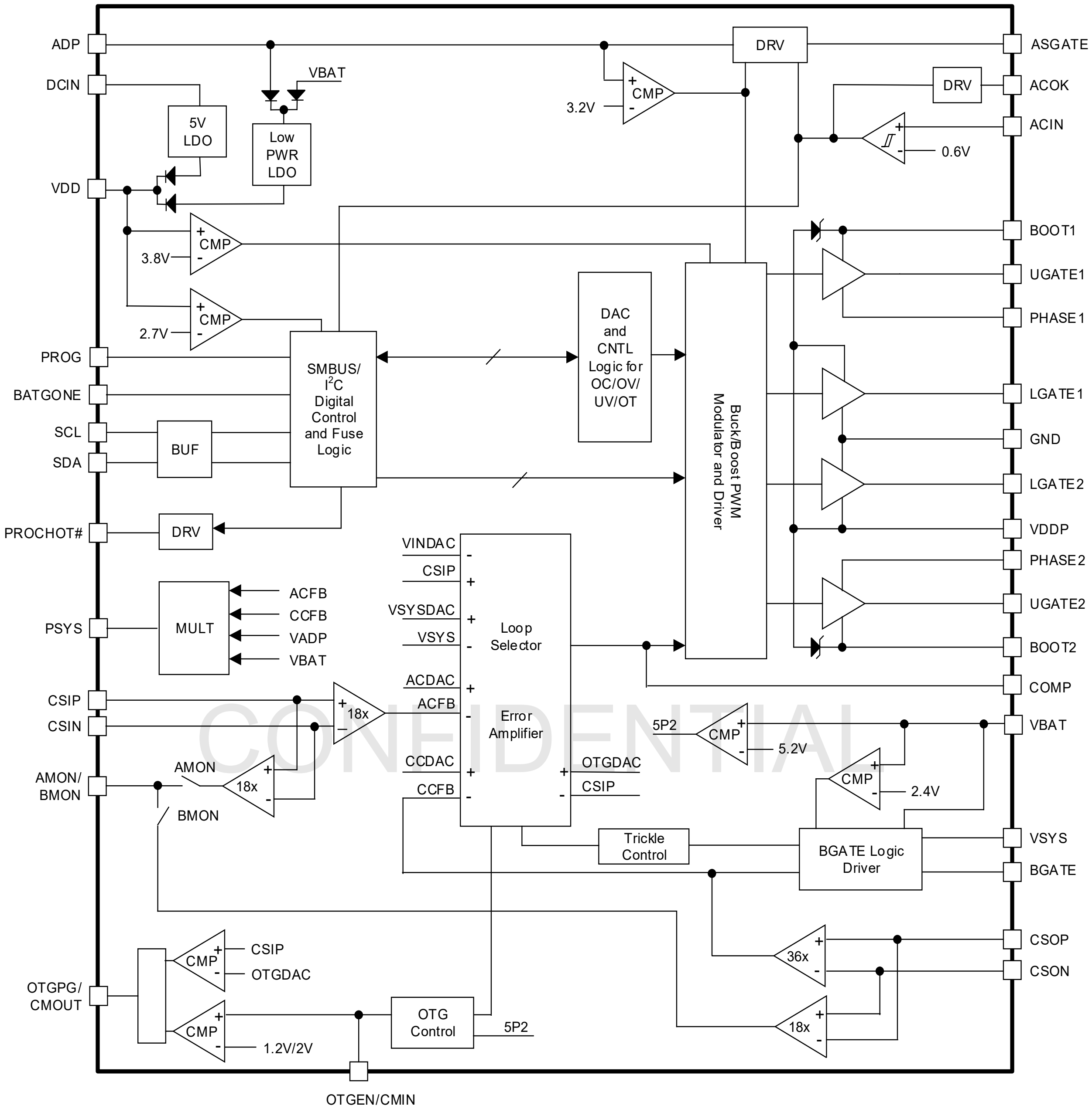
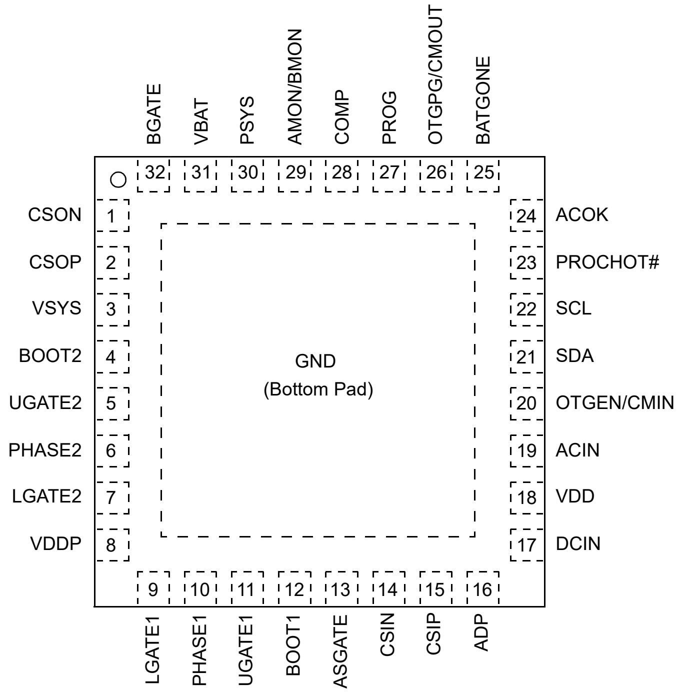


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
Bottom Pad	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. GND should also be used as the thermal pad for heat dissipation.
1	CSON	Battery current sense negative input. Connect to the battery current resistor negative input. Place a ceramic capacitor between CSOP and CSON to provide differential mode filtering.
2	CSOP	Battery current sense positive input. Connect to the battery current resistor positive input. Place a ceramic capacitor between CSOP and CSON to provide differential mode filtering.
3	VSYS	Provides feedback voltage for MaxSystemVoltage regulation.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins. Connect a 0.47µF bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain, and one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to the VDD pin through a 4.7Ω resistor and connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

Pin Number	Pin Name	Description
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain, and one terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins. Connect a 0.47µF bootstrap capacitor, which must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.
13	ASGATE	Gate drive output to the P-channel adapter FET. The use of ASGATE FETs is optional. If they are not used, leave the ASGATE pin floating.
14	CSIN	Adapter current sense negative input.
15	CSIP	Adapter current sense positive input. The modulator also uses the CSIP pin for sensing input voltage in forward mode and output voltage in reverse mode.
16	ADP	Adapter input used to sense adapter voltage. ASGATE is turned on when the adapter voltage is higher than 3.2V. The ADP pin also provides one of the two internal low power LDO inputs.
17	DCIN	Internal LDO input that provides power to the IC. Connect a diode OR from the adapter and system outputs. Bypass DCIN with an MLCC capacitor. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7µF DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 30V.
18	VDD	Internal LDO output that provides the bias power for the internal analog and digital circuit. Connect a 2.2µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V. If VDD is pulled below 2V for more than 1ms, the RAA489108 resets all the SMBus register values to their defaults.
19	ACIN	Adapter voltage sense. Use a resistor divider externally to detect adapter voltage. The adapter voltage is valid if the ACIN pin voltage is greater than 0.6V.
20	OTGEN/ CMIN	Input pin. OTG function enable pin, stand-alone comparator input pin. When the OTG function is enabled and the general purpose comparator is disabled, pulling this pin high can activate the OTG function. When the general purpose comparator is enabled, this pin is the general purpose comparator input.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
23	PROCHOT#	Open-drain output. Pulled low when ACHOT, DCHOT, or Low_VSYS are detected. IMVP compliant. Send an SMBus command to pull low with OTGCURRENT, BATGONE, ACOK, and the general purpose comparator (see Table 15).
24	ACOK	Adapter presence indicator output to indicate the adapter is ready.
25	BATGONE	Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high forces the BGATE FET to turn off in any circumstances.
26	OTGPG/ CMOUT	Open-drain output. OTG function output power-good indicator or the stand-alone comparator output. When the OTG function is enabled, this signal is low if the OTG output voltage is not within the regulation window. When the OTG function is not used, this signal is the general purpose comparator output. GP comparator must be disabled for OTGPG to function as expected.

Pin Number	Pin Name	Description
27	PROG	A resistor from the PROG pin to GND sets the following configurations: ▪ Default number of the battery cells in series: 2-, 3-, or 4-cell ▪ Default switching frequency: 733kHz or 1MHz ▪ Default adapter current limit value: 0.476A or 1.5A ▪ Autonomous Charging mode: Enabled or disabled See Table 27 for programming options.
28	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
29	AMON/ BMON	Adapter current, OTG output current, battery charging current, or battery discharging current monitor output. ▪ V_{AMON} = 18x (V_{CSIP} - V_{CSIN}) for adapter current monitor ▪ $V_{OTGCMON}$ = 18x (V_{CSIN} - V_{CSIP}) for OTG output current monitor ▪ $V_{BMON\_DISCHARGING}$ = 18x (V_{CSON} - V_{CSOP}) for battery discharging current monitor ▪ $V_{BMON\_CHARGING}$ = 36x (V_{CSOP} - V_{CSON}) for battery charging current monitor
30	PSYS	Current source output that indicates the platform power consumption. PSYS gain = 0.979µA/W (default) or 0.489µA/W
31	VBAT	Battery voltage sensor. Used for trickle charging detection and Ideal Diode mode control. Connect an optional ceramic capacitor >1µF from VBAT to GND. The VBAT pin is also one of the two internal low power LDO inputs.
32	BGATE	Gate drive output to the P-channel FET connecting the system and the battery. This pin can go high to disconnect the battery, or low to connect the battery or operate in Linear mode to regulate the trickle charge current during trickle charge.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Units
CSIP, CSIN, DCIN, ADP, ASGATE	-0.3	+36	V
DCIN - VDD	-0.3	+31	V
PHASE1	GND - 0.3	+36	V
PHASE1	GND - 2 (<20ns)	+36	V
BOOT1, UGATE1	GND - 0.3	VDDP+36	V
PHASE2	GND - 0.3	24	V
PHASE2	GND - 2 (<20ns)	24	V
BOOT2, UGATE2	GND - 0.3	VDDP+24	V
LGATE1, LGATE2	GND - 0.3	+6.5	V
LGATE1, LGATE2	GND - 2 (<20ns)	+6.5	V
VBAT, VSYS, CSOP, CSON, BGATE	-0.3	+24	V
VDD, VDDP	-0.3	+6.5	V
COMP	-0.3	+6.5	V
AMON/BMON, PSYS	-0.3	+6.5	V
OTGEN, BATGONE	-0.3	+6.5	V
ACIN, PROCHOT#	-0.3	+6.5	V
SCL, SDA	-0.3	+6.5	V
BOOT1 - PHASE1, BOOT2 - PHASE2	-0.3	+6.5	V
CSIP - CSIN, CSOP - CSON	-0.3	+0.3	V
OTGPG, PROCHOT#, ACOK		2	mA

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2017)	2	kV
Charged Device Model (Tested per JS-002-2018)	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Recommended Operating Conditions

Parameter		Minimum	Maximum	Unit
Ambient Temperature	RAA489108ARGNP	-10	+100	°C
	RAA489108A3GNP	-40	+100	°C
Junction Temperature	RAA489108ARGNP	-10	+125	°C
	RAA489108A3GNP	-40	+125	°C
Adapter Voltage		+4	+30	V

3.4 Thermal Specifications

Package Description	Thermal Resistance (Typical)	
	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
32 Ld TQFN Package	37	2

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature Range (T_J)	-10	+125	
Storage Temperature Range (T_S)	-65	+175	°C
Pb-Free Reflow Profile	See TB493		

3.5 Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
UVLO/ACOK						
VADP UVLO Rising	VADP_UVLO_r	-	**3.05**	3.3	**3.7**	V
VADP UVLO Hysteresis[2]	VADP_UVLO_h	-	-	600	-	mV
V_{BAT} UVLO Rising	VBAT_UVLO_r	-	**2.30**	2.45	**2.65**	V
V_{BAT} UVLO Hysteresis	VBAT_UVLO_h	-	-	400	-	mV
V_{BAT} 5P2V Rising	VBAT_5P2_r	-	**5.03**	5.20	**5.85**	V
V_{BAT} 5P2V Hysteresis	VBAT_5P2_h	-	-	500	-	mV
VDD 2P7 POR Falling, SMBus and BGATE/BMON Active Threshold	VDD_2P7_f	-	**2.5**	2.7	**2.9**	V
VDD 2P7 POR Hysteresis[2]	VDD_2P7_h	-	-	150	-	mV

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
VDD 3P8 POR Rising, Modulator and Gate Driver Active	VDD_3P8_r	-	**3.6**	3.8	**3.9**	V
VDD 3P8 POR Hysteresis	VDD_3P8_h	-	-	150	-	mV
ACIN Rising	ACIN_r	-	**0.58**	0.6	**0.615**	V
ACIN Hysteresis	ACIN_h	-	-	50	-	mV
Linear Regulator						
VDD Output Voltage	VDD	6V < V_{DCIN} < 30V	4.5	5.0	5.5	V
VDD Dropout Voltage	VDD_dp	<35mA, V_{DCIN} = 4V	-	-	**200**	mV
VDD Overcurrent Threshold	VDD_OC	ARGNP Junction Temperature: -10 to +125°C A3GNP Junction Temperature: -40 to +125°C	**85**	115	**155**	mA
Battery Current	I_{BAT1}	Battery only, BGATE on, PSYS OFF, BMON OFF, V_{BAT} = 16.8V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}$	-	24	**50**	µA
	I_{BAT2}	Battery only, BGATE on, PSYS OFF, BMON ON, V_{BAT} = 16.8V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}$	-	74	-	
	I_{BAT3}	Battery only, BGATE on, PSYS ON, BMON OFF, V_{BAT} = 16.8V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}$	-	930	**1155**	

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Adapter Current Regulation, R_{s1} = 20mΩ						
Adapter Current Accuracy		CSIP - CSIN = 100mV	-	5	-	A
			-2	-	**2**	%
		CSIP - CSIN = 80mV	-	4	-	A
			-2	-	**2**	%
		CSIP - CSIN = 60mV	-	3	-	A
			-2.1	-	**2.1**	%
		CSIP - CSIN = 50mV	-	2.5	-	A
			-2.2	-	**2.2**	%
		CSIP - CSIN = 40mV	-	2	-	A
			-2.5	-	**2.5**	%
		CSIP - CSIN = 30mV	-	1.5	-	A
			-3.5	-	**3.5**	%
		CSIP - CSIN = 20mV	-	1	-	A
			-5	-	**5**	%
		CSIP - CSIN = 10mV	-	0.5	-	A
			-10	-	**10**	%
		CSIP - CSIN = 5mV	-	0.25	-	A
			-20	-	**20**	%
Adapter Current PROCHOT# Threshold R_{s1} = 20mΩ	$I_{ADP\_HOT\_TH10}$	ACProchot = 0x1580H (5.504A)	-	5.504	-	A
			-1.5	-	**1.5**	%
		ACProchot = 0x0A8H (2.688A)	-	2.688	-	A
			-3	-	**3**	%
		ACProchot = 0x0800H (2.048A)	-	2.048	-	A
			-4	-	**4**	%
		ACProchot = 0x0400H (1.024A)	-	1.024	-	A
			-6	-	**6**	%
System Voltage Regulation						
Maximum System Voltage Accuracy		MaxSystemVoltage for 2-cell (8.4V) Ambient Temperature: -10°C to +100°C	**-0.6**	-	**0.6**	%
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V) Ambient Temperature: -10°C to +100°C	**-0.5**	-	**0.5**	
		MaxSystemVoltage for 2-cell (8.4V) Ambient Temperature: -40°C to +100°C	**-0.7**	-	**0.7**	
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V) Ambient Temperature: -40°C to +100°C	**-0.5**	-	**0.5**	

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Minimum System Voltage Accuracy		VDAC = 5V to 14V	**-3**	-	**3**	%
Input Voltage Regulation Accuracy		Input Voltage Register = 4.096V	**3.92**	-	**4.18**	V
Charge Current Regulation, R_{s2} = 10mΩ (Limits apply across temperature range of 0°C to +85°C)						
Charge Current Accuracy		V_{CSOP} - V_{CSON} = 60mV	-	6	-	A
			-2.5	-	**2.5**	%
		V_{CSOP} - V_{CSON} = 50mV	-	5	-	A
			-2.75	-	**2.75**	%
		V_{CSOP} - V_{CSON} = 40mV	-	4	-	A
			-3	-	**3**	%
		V_{CSOP} - V_{CSON} = 30mV	-	3	-	A
			-3.5	-	**3.5**	%
		V_{CSOP} - V_{CSON} = 20mV	-	2	-	A
			-4	-	**4**	%
		V_{CSOP} - V_{CSON} = 10mV	-	1	-	A
			-6	-	**6**	%
		V_{CSOP} - V_{CSON} = 5mV	-	0.5	-	A
			-12	-	**12**	%
BGATE Clamp						
VSYS - VBGATE ON	-	Charging enabled	**7.45**	8.30	**9.05**	V
VSYS - VBGATE OFF	-	Charging disabled	-	0	-	V
ASGATE Clamp						
VADP - VASGATE ON	-	-	-	10	-	V
VADP - VASGATE OFF	-	-	-	0	-	V
Trickle Charging Current Regulation, R_{s2} = 10mΩ (Limits apply across temperature range of 0°C to +85°C)						
Trickle Charge Current Accuracy	-	Trickle, 512mA	**456**	512	**567**	mA
		Trickle, 256mA	**200**	256	**300**	
		Trickle, 128mA	**75**	128	**170**	
		Trickle, 64mA	**16**	64	**105**	
Fast Charge to Trickle Charge Threshold	-	V_{SYS} - V_{BGATE}	**4.5**	5.05	**5.6**	V
Trickle Charge to Fast Charge Threshold Hysteresis	-	V_{SYS} - V_{BGATE}	**50**	130	**290**	mV
Fast Charge to Trickle Charge BGATE Threshold	-	V_{SYS} > 7V, V_{FB} >> V_{REF}	-	1.15	-	V

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Trickle Charge to Fast Charge BGATE Threshold Hysteresis	-	V_{SYS} > 7V, V_{FB} >> V_{REF}	-	50	-	mV
Ideal Diode Mode						
Entering Ideal Diode Mode VSYS Voltage Threshold	-	BGATE off, VSYS falling V_{VBAT} - V_{CSON}	**100**	150	**200**	mV
Exiting Ideal Diode Mode Battery Discharging Current Threshold	-	R_{s2} = 10mΩ	**100**	200	**290**	mA
Exiting Ideal Diode Mode Battery Charging Current Threshold	-	R_{s2} = 10mΩ	**50**	130	**215**	mA
BGATE Source	-	V_{SYS} - V_{BGATE} = 2V, charging disabled	**4**	6	**10**	mA
BGATE Sink	-	V_{BGATE} - V_{GND} = 2V, charging enabled	**20**	30	**40**	µA
BGATE Sink[2]	-	V_{BGATE} - V_{GND} = 2V, in Ideal Diode mode	-	6	-	mA
AMON/BMON						
Input Current Sense Amplifier, R_{s1} = 20mΩ						
CSIP/CSIN Input Voltage Range	-	-	**4**	-	**30**	V
Forward AMON Gain	-	-	-	17.97	-	V/V
Forward AMON Accuracy V_{AMON} = 17.97 x (V_{CSIP} - V_{CSIN})	-	V_{CSIP} - V_{CSIN} = 100mV (5A), CSIP = 5V,28V	**-2**	-	**2**	%
		V_{CSIP} - V_{CSIN} = 20mV (1A), V_{CSIP} = 5V, 28V	**-5**	-	**5**	
		V_{CSIP} - V_{CSIN} = 10mV (0.5A), V_{CSIP} = 5V, 28V	**-10**	-	**10**	
		V_{CSIP} - V_{CSIN} = 2mV (0.1A), V_{CSIP} = 5V, 28V	**-40**	-	**40**	
Reverse AMON Gain	-	-	-	17.9	-	V/V
Reverse AMON Accuracy V_{AMON} = 17.9 x (V_{CSIP} - V_{CSIN})	-	V_{CSIN} - V_{CSIP} = 80mV (4A), V_{CSIP} = 5V, 28V	**-3**	-	**3**	%
		V_{CSIN} - V_{CSIP} = 20mV (1A), V_{CSIP} = 5V, 28V	**-6.8**	-	**6.8**	
		V_{CSIN} - V_{CSIP} = 10mV (0.5A), V_{CSIP} = 5V, 28V	**-12.5**	-	**12.5**	
		V_{CSIN} - V_{CSIP} = 5.12mV (0.256A), CSIP = 5V, 28V	**-25**	-	**25**	
AMON Minimum Output Voltage	-	V_{CSIP} - V_{CSIN} = 0V	-	-	**30**	mV

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Discharge Current Sense Amplifier, R_{s2} = 10mΩ						
BMON Gain (Battery Discharging)	-	-	-	17.97	-	V/V
BMON Accuracy $V_{BMON} = 17.97×(V_{CSON} - V_{CSOP})$	-	$V_{CSON} - V_{CSOP}$ = 100mV (10A), V_{CSON} = 8V	**-2.5**	-	**2.5**	%
		$V_{CSON} - V_{CSOP}$ = 20mV (2A), V_{CSON} = 8V	**-7.0**	-	**4.0**	
		$V_{CSON} - V_{CSOP}$ = 10mV (1A), V_{CSON} = 8V	**-10.5**	-	**5.5**	
		$V_{CSON} - V_{CSOP}$ = 6mV (0.6A), V_{CSON} = 8V	**-18**	-	**12**	
Charge Current Sense Amplifier, R_{s2} = 10mΩ (Limits apply across the temperature range of 0°C to +85°C)						
BMON Gain (Battery Charging)	-	-	-	35.78	-	V/V
BMON Accuracy $V_{BMON} = 35.78 \times (V_{CSOP} - V_{CSON})$	-	$V_{CSOP} - V_{CSON}$ = 60mV (6A), V_{CSON} = 8V	**-3**	-	**3**	%
		$V_{CSOP} - V_{CSON}$ = 40mV (4A), V_{CSON} = 8V	**-4**	-	**4**	
		$V_{CSOP} - V_{CSON}$ = 10mV (1A), V_{CSON} = 8V	**-9**	-	**9**	
		$V_{CSOP} - V_{CSON}$ = 5mV (0.5A), V_{CSON} = 8V	**-25**	-	**25**	
BMON Minimum Output Voltage	-	$V_{CSOP} - V_{CSON}$ = 0V	-	-	**31**	mV
Discharging Current PROCHOT# Threshold, R_{s2} = 10mΩ	$I_{DIS\_HOT\_TH}$	DCProchot# = 2.048A	**1.77**	2.08	**2.39**	A
Discharging Current PROCHOT# Threshold, Battery Only, R_{s2} = 10mΩ	$I_{DIS\_HOT\_TH}$	DCProchot# = 12A	**10.8**	13.5	**17**	A
		DCProchot# = 6A	**5.2**	6.5	**8**	A
AMON/BMON Source Resistance[2]	-	-	-	-	**5**	Ω
AMON/BMON Sink Resistance[2]	-	-	-	-	**5**	Ω
BATGONE and OTGEN						
High-Level Input Voltage	-	-	**0.9**	-	-	V
Low-Level Input Voltage	-	-	-	-	**0.4**	V
Pull-Down Current	-	BATGONE and OTGEN = 5V	-	5	-	µA
PROCHOT#						
PROCHOT# Debounce Time	-	Control2 register Bit[10:9] = 11	**0.85**	1	**1.15**	ms
		Control2 register Bit[10:9] = 10	**425**	500	**575**	µs
PROCHOT# Duration Time	-	Control2 register Bit[8:6] = 000	**8.5**	10	**11.5**	ms
		Control2 register Bit[8:6] = 001	**17**	20	**23**	
Low VSYS PROCHOT# Trip Threshold	$V_{LOW\_VSYS\_HOT}$	Control1 register Bit[1:0] = 00	**5.8**	6.0	**6.2**	V
		Control1 register Bit[1:0] = 01	**6.1**	6.3	**6.5**	
		Control1 register Bit[1:0] = 10	**6.4**	6.6	**6.8**	
		Control1 register Bit[1:0] = 11	**6.7**	6.9	**7.1**	

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
PSYS[2]						
PSYS Output Current R_{s1} = 20mΩ R_{s2} = 10mΩ	I_{PSYS} Control3 Bit[9] = 0 I_{PSYS} = 0.979µA/W × Power + 2.45µA	V_{CSIP} = 28V, V_{CSIP} - V_{CSIN} = 40mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = -10mV	**-5**	-	**5**	%
	I_{PSYS} Control3 Bit[9] = 1 I_{PSYS} = 0.489µA/W ×Power	V_{CSIP} = 28V, V_{CSIP} - V_{CSIN} = 80mV, V_{BAT} = 12V, V_{CSOP} - V_{CSON} = -20mV	**-5**	-	**5**	
Maximum PSYS Output Voltage	V_{PSYS_MAX}	-	**3**	-		V
OTG						
OTG Voltage	-	OTGVoltage register = 5.004V	**4.9**	5.03	**5.15**	V
OTG Current	-	OTGCurrent register = 512mA, (OTGVoltage = 5.004V, 12V)	**435**	512	**600**	mA
		OTGCurrent register = 1024mA, (OTGVoltage = 5.004V, 12V)	**922**	1024	**1126**	
		OTGCurrent register = 1536mA, (OTGVoltage = 5.004V, 12V)	**1420**	1536	**1657**	
		OTGCurrent register = 3072mA, (OTGVoltage = 5.004V, 12V)	**2924**	3072	**3225**	
		OTGCurrent register = 4096mA, (OTGVoltage = 5.004V, 12V)	**3975**	4096	**4250**	
General Purpose Comparator						
General Purpose Comparator Rising Threshold	-	Reference = 1.2V	**1.11**	1.2	**1.32**	V
		Reference = 2V	**1.93**	2	**2.05**	
General Purpose Comparator Hysteresis	-	Reference = 1.2V	-	45	-	mV
		Reference = 2V	-	45	-	
Protection						
VSYS Absolute Overvoltage Rising Threshold	-	-	22.5	23.5	24	V
VSYS Absolute Overvoltage Hysteresis	-	-	-	0.35	-	V
VSYS Overvoltage Rising Threshold	-	MaxSystemVoltage register value = 8.4V	**8.92**	9.15	**9.38**	V
VSYS Overvoltage Hysteresis	-	MaxSystemVoltage register value = 8.4V	**270**	400	**530**	mV

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
VSYS UV Falling Threshold	-	Control6 register Bit[2:0] = 001	-	3	-	V
		Control6 register Bit[2:0] = 010	-	3.9	-	V
		Control6 register Bit[2:0] = 011	-	4.8	-	V
		Control6 register Bit[2:0] = 100	-	5.7	-	V
		Control6 register Bit[2:0] = 101	-	6.6	-	V
		Control6 register Bit[2:0] = 110	-	7.5	-	V
		Control6 register Bit[2:0] = 111	-	8.4	-	V
VSYS OK Threshold	-	-	**0.45**	0.6	**0.75**	V
VSYS OK Source Current	-	-	-	10	-	mA
Over-Temperature Threshold[2]	-	-	**140**	150	**160**	°C
Adapter Overvoltage Rising Threshold	-	-	**32.2**	33.3	**33.95**	V
Adapter Overvoltage Hysteresis	-	-	**390**	590	**760**	mV
Adapter Low Threshold	-	Control5 register Bit[7:6] = 00	-	7.2	-	V
		Control5 register Bit[7:6] = 01	-	7.8	-	V
		Control5 register Bit[7:6] = 10	-	9	-	V
		Control5 register Bit [7:6] = 11	-	9.6	-	V
OTG Undervoltage Falling Threshold	-	OTG voltage = 5.004V	**2.85**	3.2	**3.65**	V
OTG Overvoltage Rising Threshold	-	OTG voltage = 5.004V	**6.4**	6.8	**7.2**	V
Oscillator						
Oscillator Frequency, Digital Core Only	-	-	**0.85**	1	**1.15**	MHz
Digital Debounce Time Accuracy[2]	-	-	**-15**	-	**15**	%
Miscellaneous						
Switching Frequency Accuracy	-	COMP > 1.7V and not in period stretching	**-15**	-	**15**	%
Battery Learn Mode Auto-Exit Threshold	-	MinSystemVoltage = 5.376V Control1 register Bit[13] = 1	**5.05**	5.35	**5.7**	V
Battery Learn Mode Auto-Exit Hysteresis[2]	-	MinSystemVoltage = 5.376V Control1 register Bit[13] = 1	-	330	-	mV
ADP Discharge Current	-	ADP = 5V to 32V	-	15	-	mA
VSYS Discharge Current	-	VSYS = 5V to 18V	-	10	-	mA
SMBus						
SDA/SCL Input Low Voltage	-	-	-	-	**0.6**	V

Operating conditions: ADP = CSIP = CSIN = 5V and 28V, VSYS = VBAT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C (ARGNP) or -40 to +125°C (A3GNP) unless otherwise specified.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
SDA/SCL Input High Voltage	-	-	**1.3**	-	-	V
SDA/SCL Input Bias Current	-	-	-	-	**1**	µA
SDA, Output Sink Current	-	SDA = 0.4V	**4**	-	-	mA
SMBus Frequency	f_{SMB}	-	**10**	-	**400**	kHz
Gate Driver[2]						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current	-	800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2	-	A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current	-	350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8	-	A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current	-	800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2	-	A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current	-	300	**450**	mΩ
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5	-	A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current	-	800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2	-	A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current	-	300	**450**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5	-	A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current	-	800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2	-	A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current	-	300	**450**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**2.3**	3.5	-	A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$	-	**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$	-	**10**	20	**40**	ns
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$	-	**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$	-	**10**	20	**40**	ns

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Values or limits established by characterization and are not production tested.

3.6 SMBus Timing Specification

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
SMBus Frequency	F_{SMB}	-	10	-	400	kHz
Bus Free Time	t_{BUF}	-	4.7	-	-	µs
Start Condition Hold Time from SCL	$t_{HD:STA}$	-	4	-	-	µs
Start Condition Set-Up Time from SCL	$t_{SU:STA}$	-	4.7	-	-	µs
Stop Condition Set-Up Time from SCL	$t_{SU:STO}$	-	4	-	-	µs
SDA Hold Time from SCL	$t_{HD:DAT}$	-	300	-	-	ns
SDA Set-Up Time from SCL	$t_{SU:DAT}$	-	250	-	-	ns
SCL Low Period	t_{LOW}	-	4.7	-	-	µs
SCL High Period	t_{HIGH}	-	4	-	-	µs
SMBus Inactivity Timeout	-	Maximum charging period without a SMBus Write to MaxSystemVoltage or ChargeCurrent register	-	175	-	s

1. Limits established by characterization and are not production tested.

3.7 Gate Driver Timing Diagrams

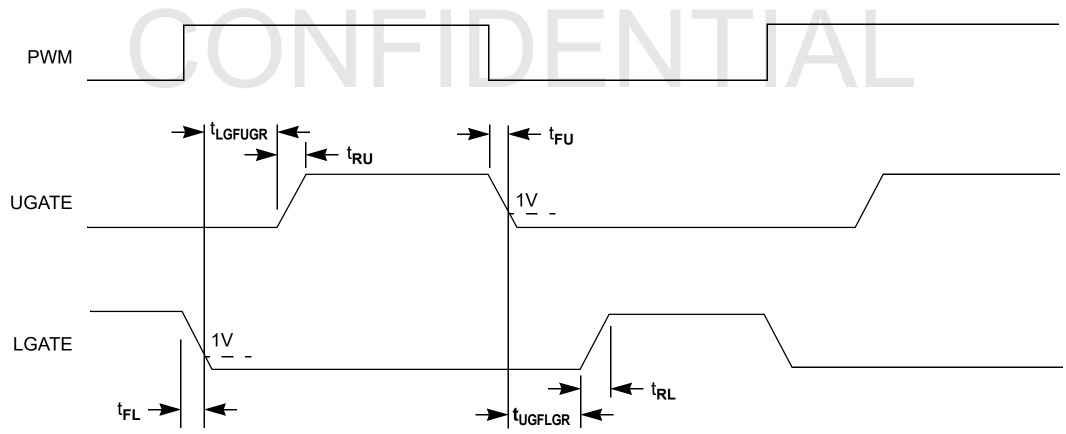


Figure 3. Gate Driver Timing Diagram

4. Typical Performance

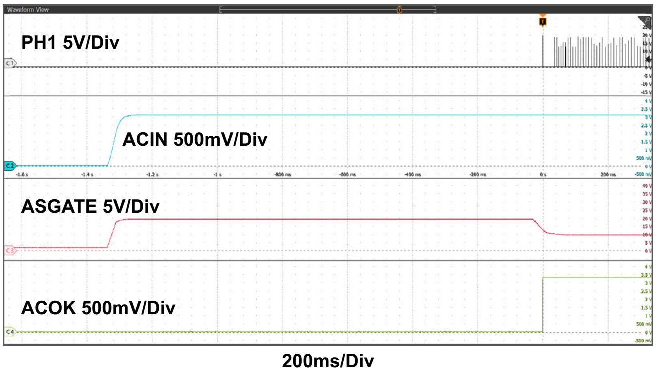


Figure 4. Adapter Insertion, V_{ADP} = 20V, V_{BAT} = 11V, ChargeCurrent = 0A

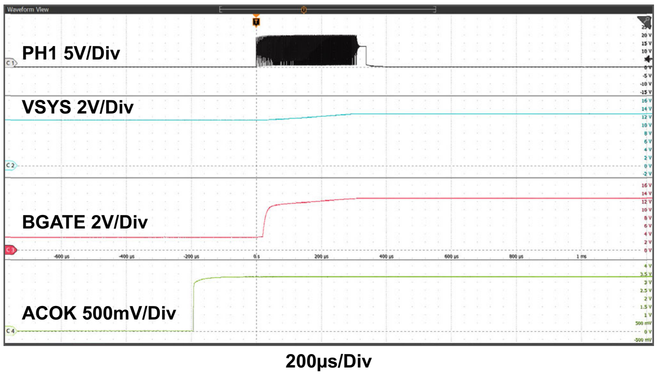


Figure 5. Adapter Insertion, V_{ADP} = 20V, V_{BAT} = 11V, ChargeCurrent = 0A (Figure 4 Zoomed In)

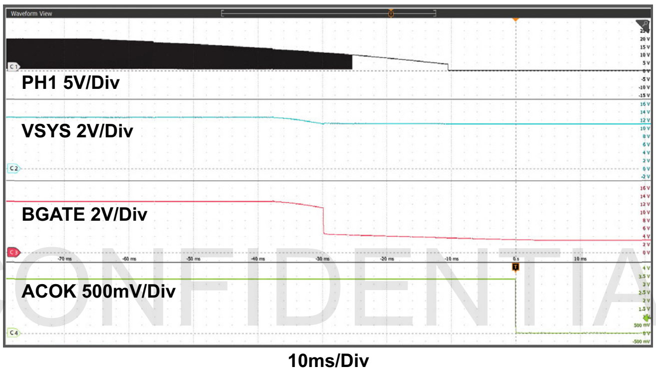


Figure 6. Adapter Removal, V_{ADP} = 20V, V_{BAT} = 11V, ChargeCurrent = 0A

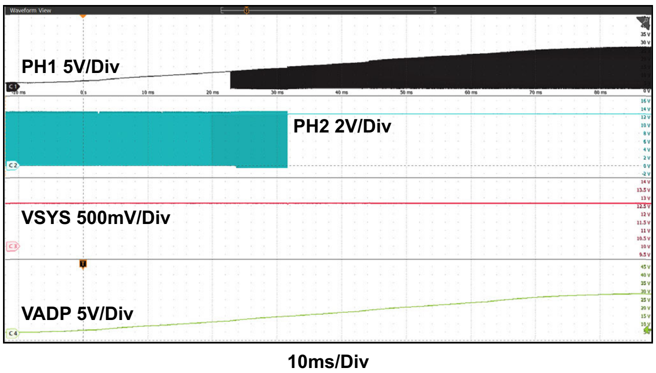


Figure 7. Adapter Voltage Ramps Up, Boost -> Buck-Boost -> Buck Operation Mode Transition

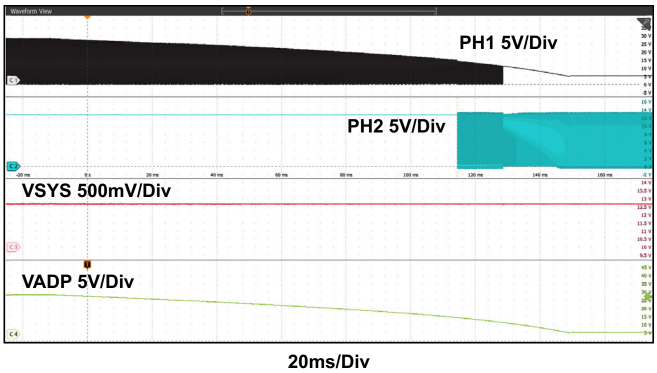
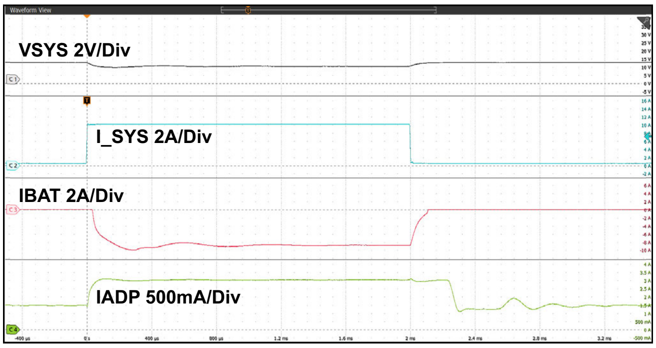
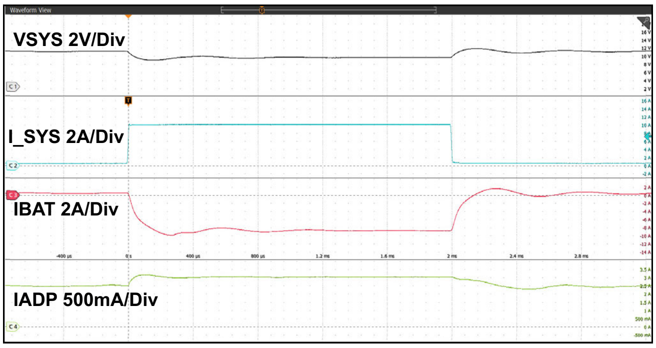


Figure 8. Adapter Voltage Ramps Down, Buck -> Buck-Boost -> Boost Operation Mode Transition



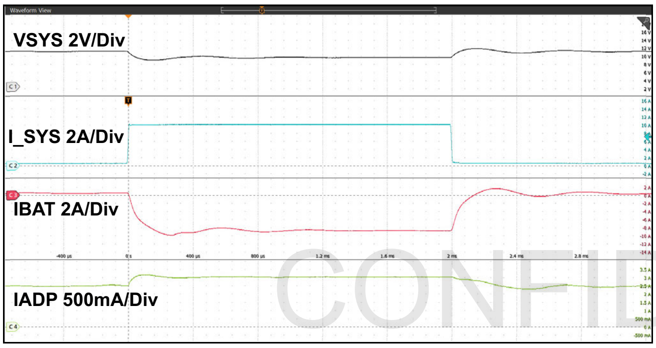
400µs/Div

Figure 9. Boost Mode, Output Voltage Loop to Adapter Current Loop Transition. V_{ADP} = 5V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 0.5A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0A

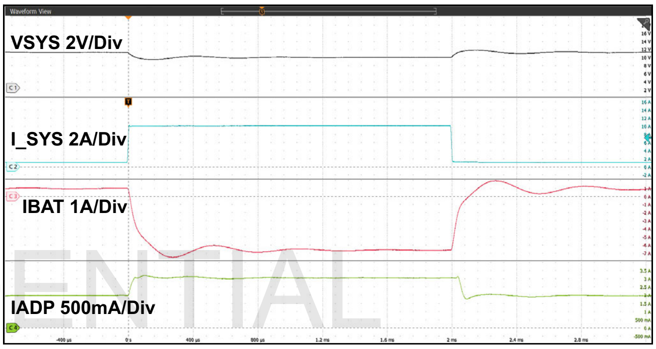


400µs/Div

Figure 10. Boost Mode, Charging Current Loop to Adapter Current Loop Transition. V_{ADP} = 5V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 0.5A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0.5A



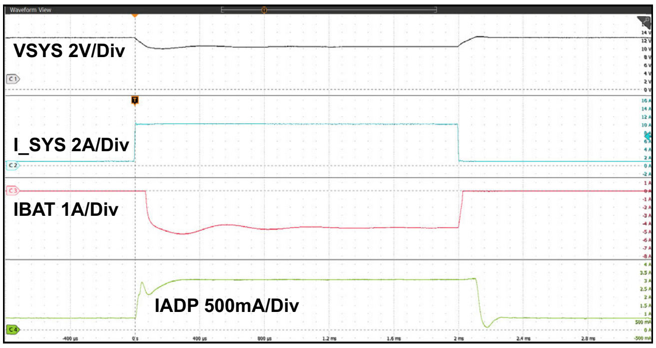
400µs/Div



400µs/Div

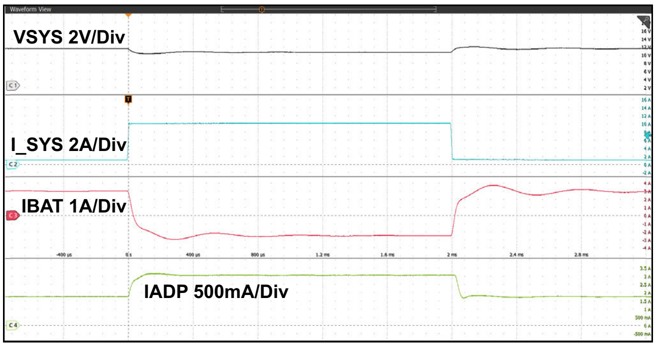
Figure 11. Buck-Boost Mode, Output Voltage Loop to Adapter Current Loop Transition. V_{ADP} = 12V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0A

Figure 12. Buck-Boost Mode, Charging Current Loop to Adapter Current Loop Transition. V_{ADP} = 12V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 1A



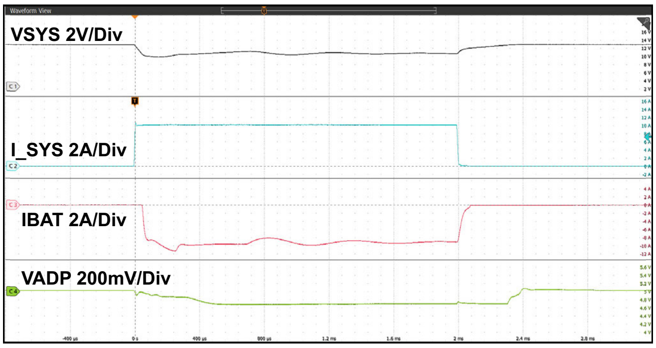
400µs/Div

Figure 13. Buck Mode, Output Voltage Loop to Adapter Current Loop Transition. V_{ADP} = 28V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 0A



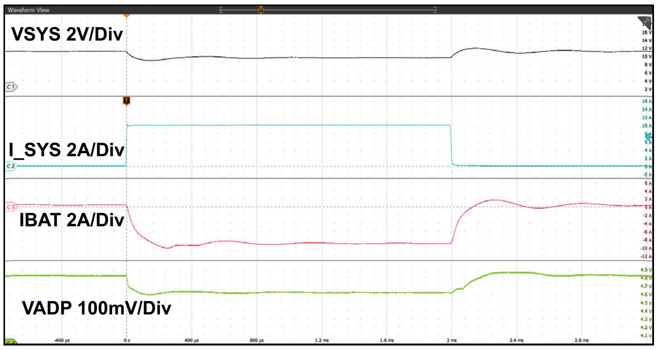
400µs/Div

Figure 14. Buck Mode, Charging Current Loop to Adapter Current Loop Transition. V_{ADP} = 28V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, System Load 1A to 10A Step, AdapterCurrentLimit = 3A, ChargeCurrent = 3A



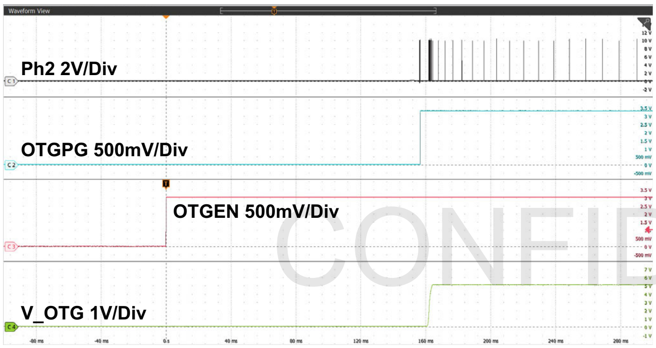
400µs/Div

Figure 15. Boost Mode, Output Voltage Loop to Input Voltage Loop Transition. V_{ADP} = 5.004V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, VINDAC = 4.608V, System Load 0A to 10A Step, ChargeCurrent = 0A



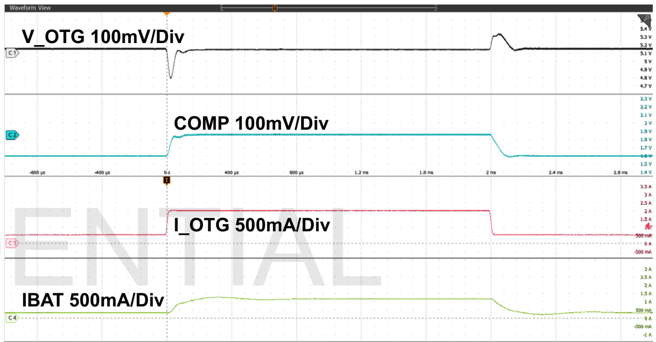
400µs/Div

Figure 16. Boost Mode, Charging Current Loop to Input Voltage Loop Transition. V_{ADP} = 5.004V, MaxSystemVoltage = 12.576V, V_{BAT} = 11V, VINDAC = 4.608V, System Load 0A to 10A Step, ChargeCurrent = 0.5A



40ms/Div

Figure 17. OTG Mode Enable, OTG Enable 150ms Debounce Time



400µs/Div

Figure 18. OTG Mode 0.5A to 2A Transient Load, OTG Voltage = 5.12V

5. General SMBus Architecture

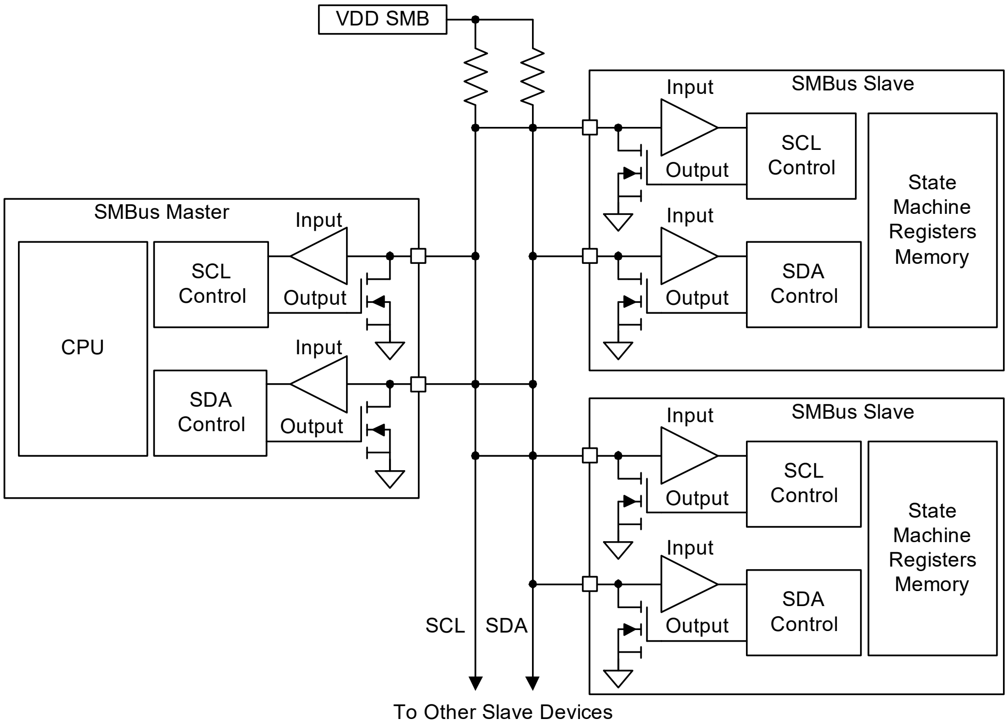


Figure 19. General SMBus

5.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 20.

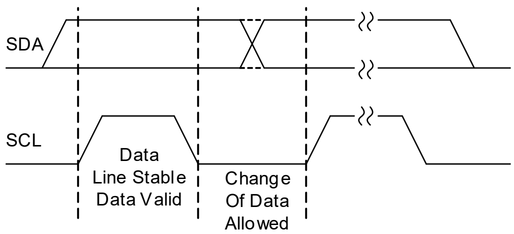


Figure 20. Data Validity

5.2 START and STOP Conditions

In Figure 21, the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

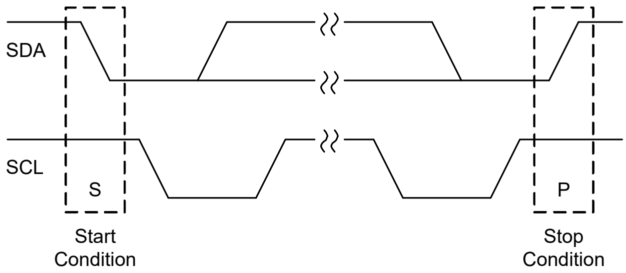


Figure 21. Start and Stop Waveforms

5.3 Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and a R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line LOW to acknowledge (see Figure 22). Both the master and the slave use the ACK bit to acknowledge receipt of register addresses and data.

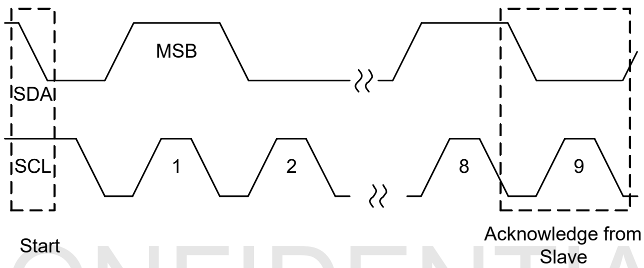


Figure 22. Acknowledge On The SMBus

5.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition followed by seven bits of slave address (0001001) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line LOW for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is 1 indicating a not acknowledge condition.

When the control byte is sent and the RAA489108 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the RAA489108 which register the master writes or reads. See Table 1 for register details. When the RAA489108 receives a register address byte, it responds with an acknowledge.

5.5 Byte Format

Every byte on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO Byte data is transferred before the HI Byte data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

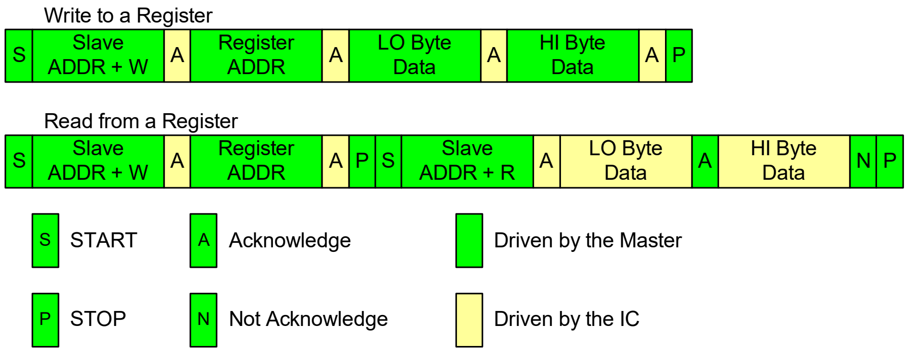


Figure 23. SMBus Read and Write Protocol

5.6 SMBus and I²C Compatibility

The RAA489108 SMBus minimum input logic high voltage is 1.3V, so it is compatible with I^2C with pull-up power supplies higher than 1.3V.

The RAA489108 SMBus registers are 16 bits, so it is compatible with 16-bit I^2C or 8-bit I^2C with auto-increment capability.

6. SMBus Commands

The RAA489108 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification. The RAA489108 uses the SMBus Read-word and Write-word protocols (see Figure 23) to communicate with the host system and a smart battery. The RAA489108 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ as follows:

The Read and Write address for the RAA489108 is:

- Read address = 0b00010011 (0X13H)
- Write address = 0b00010010 (0X12H)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The information in this datasheet is based on current sensing resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ unless otherwise specified.

Table 1. Register Summary

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
ChargeCurrentLimit	0x14	R/W	11	[12:2] 11-bit, LSB size 4mA, total range 6080mA with 10mΩ R_{S2}	0A
MaxSystemVoltage	0x15	R/W	12	[14:3] 12-bit, LSB size 8mV, total range 18.304V	8.384V for 2-cell 12.576V for 3-cell 16.768V for 4-cell
Control7	0x36	R/W	3	[7], [1:0] 3-bit, configures various charger options	0x0000h
Control6	0x37	R/W	8	[7:0] 8-bit, configures various charger options	0x0000h or 0x0003h[1]
Control5	0x38	R/W	16	Configures various charger options	0x0000h
Control0	0x39	R/W	16	Configures various charger options	0x0000h

Table 1. Register Summary (Cont.)

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
Information1	0x3A	R	16	Indicates various charger statuses	0x0000h
AdapterCurrentLimit2	0x3B	R/W	11	[12:2] 11-bit, LSB size 4mA, total range 6080mA with 20mΩ R_{S1}	1500mA
Control1	0x3C	R/W	16	Configures various charger options	0x0000h
Control2	0x3D	R/W	16	Configures various charger options	0x0000h
MinSystemVoltage	0x3E	R/W	6	[13:8] 6-bit, LSB size 256mV, total range 13.824V	5.12V for 2-cell 7.68V for 3-cell 10.24V for 4-cell
AdapterCurrentLimit1	0x3F	R/W	11	[12:2] 11-bit, LSB size 4mA, total range 6080mA with 20mΩ R_{S1}	Set by PROG pin
Revision ID	0x44	R	8	Revision ID register - Read only	0x00h
ACProchot#	0x47	R/W	6	[12:7] Adapter current PROCHOT# threshold Default 3.072A, 128mA resolution for 20mΩ R_{s1}.	3.072A
DCProchot#	0x48	R/W	6	[13:8] Battery discharging current PROCHOT# threshold Default 4.096A, 256mA resolution for 10mΩ R_{s2}.	4.096A
OTG Voltage	0x49	R/W	12	[14:3] 12-bit, LSB size 18mV, total range 32.256V OTG mode voltage reference	5.004V
OTG Current	0x4A	R/W	6	[12:5] 8-bit, LSB size 32mA, total range 4.096A OTG mode maximum current limit	0.512A
V_{IN} Voltage	0x4B	R/W	6	[13:8] 6-bit, LSB size 512mV, total range 27.648V V_{IN} loop voltage reference	4.096V
Control3	0x4C	R/W	16	Configures various charger options	0x0000h or 0x0080h[2]
Information2	0x4D	R	16	Indicates various charger statuses	0x0000h
Control4	0x4E	R/W	16	Configures various charger options	0x0000h
Information3	0x90	R	1	[1] 1-bit, indicates pass-through mode status	0x0000h
Manufacturer ID	0xFE	R	8	Manufacturer ID register – 0x49 - Read only	0x0049h
Device ID	0xFF	R	8	Device ID register - Read only	0x001Ch

1. When inserting the battery for the first time, VSYS UV by default is 000 = Disabled. When inserting the adapter, VSYS UV threshold by default is 011 = 4.8V.
2. Control3 Bit[7] is set by PROG pin, see Table 27.

6.1 Setting the Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0x14H) using the Write-word protocol shown in Figure 23 and the data format shown in Table 2 for a 10mΩ R_{s2} or Table 3 for a 5mΩ R_{s2}.

The RAA489108 limits the charging current by limiting the CSOP-CSON voltage. By using the recommended current sense resistor values R_{s1} = 20mΩ and R_{s2} = 10mΩ, the LSB of the register translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register and the maximum value is clamped at 6080mA for R_{s2} = 10mΩ.

The ChargeCurrentLimit register is reset to 0x0000H after POR. To set the battery charging current value, write a non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its content.

Table 2 shows the conditions to enable fast charging according to the ChargeCurrentLimit register setting.

Table 2. ChargeCurrentLimit Register 0x14H (11-Bit, 4mA Step, 10mΩ Sense Resistor)

Bit	Description
[1:0]	Not used
[2]	0 = Add 0mA of charge current limit. 1 = Add 4mA of charge current limit.
[3]	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
[4]	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
[5]	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
[6]	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
[7]	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
[8]	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
[9]	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
[10]	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
[11]	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
[12]	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
[13:15]	Not used
Maximum	[12:2] = 10111110000, 6080mA

Table 3. ChargeCurrentLimit Register 0x14H (11-Bit, 8mA Step, 5mΩ Sense Resistor)

Bit	Description
[1:0]	Not used
[2]	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
[3]	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
[4]	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
[5]	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
[6]	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
[7]	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
[8]	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
[9]	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
[10]	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
[11]	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
[12]	0 = Add 0mA of charge current limit. 1 = Add 8192mA of charge current limit.
[13:15]	Not used
Maximum	[12:2] = 10111110000, 12160mA

6.2 Setting the Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0x3FH) and/or AdapterCurrentLimit2 command (0x3BH) using the Write-word protocol shown in Figure 23 and the data format shown in Table 4 for a 20mΩ R_{s1} or Table 5 for a 10mΩ R_{s1}.

The RAA489108 limits the adapter current by limiting the CSIP-CSIN voltage. By using the recommended current sense resistor values, the LSB of the register always translates to 4mA of adapter current. Any adapter current limit command is accepted, but only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers and the maximum value is clamped at 6080mA for R_{s1} = 20mΩ.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.5A or keeps the value that is written to it previously if the battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content.

To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0x3BH) command using the Write-word protocol shown in Figure 23 and the data format shown in Table 4 for a 20mΩ R_{s1} or Table 5 for a 10mΩ R_{s1}.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. See Current Monitor for detailed operation instructions.

Table 4. AdapterCurrentLimit1 Register 0x3FH and AdapterCurrentLimit2 Register 0x3BH (11-Bit, 4mA Step, 20mΩ Sense Resistor)

Bit	Description
[1:0]	Not used
[2]	0 = Add 0mA of adapter current limit. 1 = Add 4mA of adapter current limit.
[3]	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
[4]	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
[5]	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
[6]	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
[7]	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
[8]	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
[9]	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
[10]	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
[11]	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
[12]	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
[13:15]	Not used
Maximum	[12:4] = 10111110000, 6080mA

Table 5. AdapterCurrentLimit1 Register 0x3FH and AdapterCurrentLimit2 Register 0x3BH (11-Bit, 8mA Step, 10mΩ Sense Resistor)

Bit	Description
[1:0]	Not used
[2]	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
[3]	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
[4]	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
[5]	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.

Table 5. AdapterCurrentLimit1 Register 0x3FH and AdapterCurrentLimit2 Register 0x3BH (11-Bit, 8mA Step, 10mΩ Sense Resistor)

Bit	Description
[6]	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
[7]	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
[8]	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
[9]	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
[10]	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
[11]	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
[12]	0 = Add 0mA of adapter current limit. 1 = Add 8192mA of adapter current limit.
[13:15]	Not used
Maximum	[12:4] = 10111110000, 12160mA

6.3 Setting the Two-Level Adapter Current Limit Duration

For a two-level adapter current limit, write the 16-bit AdapterCurrentLimit1 and AdapterCurrentLimit2 registers (0x3F and 0x3B) using the Write-word protocol shown in Figure 23 and the data format shown in Table 4 or Table 5. Additionally, set time durations for the AdapterCurrentLimit1 and AdapterCurrentLimit2 levels using, respectively, the T1 and T2 fields of Control5 (0x38) as shown in Table 6. The two-level adapter current functionality is enabled using Control Register 2 (0x3D) Bit[12]. See Current Monitor for detailed operation instructions.

Table 6. Control5 0x38H

Bit	Description
[2:0] T1	000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5ms 110 = 0.1ms 111 = 0ms
[10:8] T2	000 = 10µs (default) 001 = 100µs 010 = 500µs 011 = 1ms 100 = 300µs 101 = 750µs 110 = 2ms 111 = 10ms

6.4 Setting the Maximum Charging Voltage or System Regulating Voltage

To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command (0x15H) using the Write-word protocol shown in Figure 23 and the data format shown in Table 7.

The valid range of MaxSystemVoltage is 8mV to 18.304V. The MaxSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register and the maximum value is clamped at 18.304V. The RAA489108 accepts a 0V command, but the register value does not change.

The MaxSystemVoltage register sets the battery full charging voltage limit. The MaxSystemVoltage register setting is also the system bus voltage regulation point when the battery is absent, or if the battery is present but is not in Charging mode. See System Voltage Regulation and Trickle Charging for details.

The VSYS pin senses the battery voltage for maximum charging voltage regulation. The VSYS pin is also the system bus voltage regulation sense point.

Table 7. MaxSystemVoltage Register 0x15H (8mV Step)

Bit	Description
[2:0]	Not used
[3]	0 = Add 0mV of charge voltage. 1 = Add 8mV of charge voltage.
[4]	0 = Add 0mV of charge voltage. 1 = Add 16mV of charge voltage.
[5]	0 = Add 0mV of charge voltage. 1 = Add 32mV of charge voltage.
[6]	0 = Add 0mV of charge voltage. 1 = Add 64mV of charge voltage.
[7]	0 = Add 0mV of charge voltage. 1 = Add 128mV of charge voltage.
[8]	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
[9]	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
[10]	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
[11]	0 = Add 0mV of charge voltage. 1 = Add 2048mV of charge voltage.
[12]	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
[13]	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
[14]	0 = Add 0mV of charge voltage. 1 = Add 16384mV of charge voltage.
[15]	Not used
Maximum	[15:3] = 100011110000, 18304mV

6.5 Setting the Minimum System Voltage

To set the minimum system voltage, write a 16-bit MinSystemVoltage command (0x3EH) using the Write-word protocol shown in Figure 23 and the data format shown in Table 8.

The valid range of MinSystemVoltage is 256mV to 13.824V. The MinSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register. The MinSystemVoltage register value should be set lower than the MaxSystemVoltage register value and the maximum value of the MinSystemVoltage is clamped at 13.824V.

The MinSystemVoltage register sets the battery voltage threshold for entry and exit of Trickle Charging mode and for entry and exit of Learn mode. The VBAT pin senses the battery voltage to compare with the MinSystemVoltage register setting. See Battery Learn Mode for details.

The MinSystemVoltage register setting provides the system regulation voltage when the RAA489108 is in Trickle Charging mode. The VSYS pin is the system voltage regulation sense point in Trickle Charging mode. See System Voltage Regulation and Trickle Charging" for details.

Table 8. MinSystemVoltage Register 0x3EH

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
[9]	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
[10]	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
[11]	0 = Add 0mV of charge voltage. 1 = Add 2048mV of charge voltage.
[12]	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
[13]	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
[15:14]	Not used
Maximum	[13:8] = 110110, 13824mV

6.6 Setting the PROCHOT# Threshold for Adapter Overcurrent Conditions

To set the PROCHOT# assertion threshold for adapter overcurrent conditions, write a 16-bit ACProchot# command (0x47H) using the Write-word protocol shown in Table 23 and the data format shown in Table 9. By using the recommended current sense resistor values, the LSB of the register translates to 128mA of adapter current. The ACProchot# register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 6400mA for R_{s1} = 20mΩ.

After POR, the ACProchot# register is reset to 0x0C00H. The ACProchot# register can be read back to verify its content.

If the adapter current exceeds the ACProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit[10:9] and latches on for the minimum time programmed by Control2 register Bit[8:6].

Table 9. ACProchot# Register 0x47H (20mΩ Sensing Resistor, 128mA Step)

Bit	Description
[6:0]	Not used
[7]	0 = Add 0mA of ACProchot# threshold. 1 = Add 128mA of ACProchot# threshold.
[8]	0 = Add 0mA of ACProchot# threshold. 1 = Add 256mA of ACProchot# threshold.
[9]	0 = Add 0mA of ACProchot# threshold. 1 = Add 512mA of ACProchot# threshold.
[10]	0 = Add 0mA of ACProchot# threshold. 1 = Add 1024mA of ACProchot# threshold.
[11]	0 = Add 0mA of ACProchot# threshold. 1 = Add 2048mA of ACProchot# threshold.
[12]	0 = Add 0mA of ACProchot# threshold. 1 = Add 4096mA of ACProchot# threshold.
[15:13]	Not used
Maximum	[12:7] = 110010, 6400mA

6.7 Setting the PROCHOT# Threshold for the Battery Over Discharging Current Condition

To set the PROCHOT# signal assertion threshold for the battery over discharging current condition, write a 16-bit DCProchot# command (0x48H) using the Write-word protocol shown in Figure 23 and the data format shown in Table 10. By using the recommended current sense resistor values, the LSB of the register translates to 256mA of adapter current. The DCProchot# register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 12.8A for R_{s2} = 10mΩ.

After POR, the DCProchot# register is reset to 0x1000H. The DCProchot# register can be read back to verify its content.

If the battery discharging current exceeds the DCProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit[10:9] and latches on for the minimum time programmed by Control2 register Bit[8:6].

In Battery Only mode and Low Power mode, the DCProchot# threshold is set by Control0 register Bit[4:3] and Control7 Bit[1], which provide a total of eight options.

In Battery Only mode, the DCProchot# function works only when PSYS is enabled, because enabling PSYS activates the internal comparator reference. The Information register 0x3A Bit[15] indicates whether the internal comparator reference is active. When the adapter is present, the internal comparator reference is always active.

Table 10. DCProchot# Register 0x48H (10mΩ Sensing Resistor, 256mA Step)

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mA of DCProchot# threshold. 1 = Add 256mA of DCProchot# threshold.
[9]	0 = Add 0mA of DCProchot# threshold. 1 = Add 512mA of DCProchot# threshold.
[10]	0 = Add 0mA of DCProchot# threshold. 1 = Add 1024mA of DCProchot# threshold.
[11]	0 = Add 0mA of DCProchot# threshold. 1 = Add 2048mA of DCProchot# threshold.
[12]	0 = Add 0mA of DCProchot# threshold. 1 = Add 4096mA of DCProchot# threshold.
[13]	0 = Add 0mA of DCProchot# threshold. 1 = Add 8192mA of DCProchot# threshold.
[15:14]	Not used.
Maximum	[13:8] = 110010, 12800mA

6.8 Setting the PROCHOT# Debounce Time and Duration Time

Control2 register Bit[10:9] configures the PROCHOT# signal debounce time before its assertion for ACProchot# and DCProchot#. The low system voltage PROCHOT# has a fixed debounce time of 8µs.

Control2 register Bit[8:6] configures the minimum duration of the PROCHOT# signal when asserted.

6.9 Setting the Control Registers

The Control0, Control1, Control2, Control3, Control4, Control5, Control6 and Control7 registers configure the RAA489108 operation. To change certain functions or options after POR, write control commands to any of the following control registers using the Write-word protocol shown in Figure 23 and the data format shown in Table 11 (0x39H), Table 12 (0x3CH), Table 13 (0x3DH), Table 14 (0x4CH), Table 15 (0x4EH), Table 16 (0x38H), Table 17 (0x37H), and Table 18 (0x36H).

- 16-bit control command to the Control0 register (0x39H)
- 16-bit control command to the Control1 register (0x3CH)
- 16-bit control command to the Control2 register (0x3DH)
- 16-bit control command to the Control3 register (0x4CH)
- 16-bit control command to the Control4 register (0x4EH)
- 16-bit control command to the Control5 register (0x38H)
- 8-bit control command to the Control6 register (0x37H)
- 3-bit control command to the Control7 register (0x36H)

Table 11. Control0 Register 0x39H

Bit	Bit Name	Description
[15:13]	Forward Buck Phase Comparator Threshold Offset	Bit[15:13] adjusts the phase comparator threshold offset for the forward buck mode. 000 = 0mV (default) 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[12:10]	Forward Buck-boost, Forward Boost, and Reverse Boost Phase Comparator Threshold Offset	Bit[12:10] adjusts the phase comparator threshold offset for the forward buck-boost, forward boost, and reverse boost modes. 000 = 0mV (default) 001 = 0.5mV 010 = 1mV 011 = 1.5mV 100 = -2mV 101 = -1.5mV 110 = -1mV 111 = -0.5mV
[9,8,0]	Reverse Buck and Reverse Buck-boost Phase Comparator Threshold Offset	Bit[9,8,0] adjusts the phase comparator threshold offset for the reverse buck and reverse buck-boost modes. 000 = 0mV (default) 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[7]	SMBus Timeout	Bit[7] enables or disables the charger timeout function. If the adapter is present and the RAA489108 does not receive a write command to the MaxSystemVoltage(0x15h) or ChargeCurrentLimit(0x14h) register within the time set by Control3 register Bit[12:11], RAA489108 terminates charging. After the timeout occurs, writing the MaxSystemVoltage(0x15h) or ChargeCurrentLimit(0x14h) register re-enables charging. 0 = Enable the SMBus timeout function (default) 1 = Disable the SMBus timeout function
[6:5]	High-Side FET Short Detection Threshold	Bit[6:5] configures the high-side FET short detection phase node voltage threshold while the low-side FET turns on. 00 = 800mV (default) 01 = 500mV 10 = 600mV 11 = 400mV

Table 11. Control0 Register 0x39H (Cont.)

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[4:3]</td><td>DCProchot# Threshold in Battery Only Low Power Mode</td><td>Control7[1] and Control0[4:3] configure the battery discharging current DCProchot# threshold in battery only Low Power mode as indicated by Information1 register 0x3A Bit[15]. If PSYS is enabled, the battery discharge current DCProchot# threshold is instead set by the DCProchot# register 0x48 setting.
<table>
<tr><th>Control7[1]</th><th>Control0[4:3]</th><th>R_{s2} = 20mΩ (A)</th><th>R_{s2} = 10mΩ (A)</th><th>R_{s2} = 5mΩ (A)</th></tr>
<tr><td>0 (default)</td><td>00 (default)</td><td>6</td><td>12</td><td>24</td></tr>
<tr><td>0</td><td>01</td><td>5</td><td>10</td><td>20</td></tr>
<tr><td>0</td><td>10</td><td>4</td><td>8</td><td>16</td></tr>
<tr><td>0</td><td>11</td><td>3</td><td>6</td><td>12</td></tr>
<tr><td>1</td><td>00</td><td>2.5</td><td>5</td><td>10</td></tr>
<tr><td>1</td><td>01</td><td>2</td><td>4</td><td>8</td></tr>
<tr><td>1</td><td>10</td><td>1.5</td><td>3</td><td>6</td></tr>
<tr><td>1</td><td>11</td><td>1</td><td>2</td><td>4</td></tr>
</table></td></tr>
<tr><td>[2]</td><td>Input Voltage Regulation Loop</td><td>Bit[2] enables or disables the input voltage regulation loop.
0 = Enable the input voltage regulation loop (default)
1 = Disable the input voltage regulation loop</td></tr>
<tr><td>[1]</td><td>Force Buck Mode</td><td>Bit[1] disables or enables Force Buck mode. If the Force Buck mode bit is enabled, the Buck-Boost window narrows.
0 = Disable Force Buck mode (default)
1 = Enable Force Buck mode</td></tr>
</table>

Table 12. Control1 Register 0x3CH

Bit	Bit Name	Description
[15:14]	General Purpose Comparator Assertion Debounce Time	Bit[15:14] configures the general purpose comparator assertion debounce time. 00 = 2µs (default) 01 = 12µs 10 = 2ms 11 = 5s
[13]	Exit Learn Mode Option	Bit[13] provides the option to Exit Learn mode when the battery voltage is lower than the MinSystemVoltage register setting. 0 = Stay in Learn mode even if V_{BAT} < MinSystemVoltage register setting (default) 1 = Exit Learn mode if V_{BAT} < MinSystemVoltage register setting
[12]	Learn Mode	Bit[12] enables or disables Battery Learn mode. 0 = Disable Battery Learn mode (default) 1 = Enable Battery Learn mode To enter Learn mode, the BATGONE pin must be low, that is, the battery must be present.
[11]	OTG Function	Bit[11] enables or disables the OTG function. 0 = Disable the OTG function (default) 1 = Enable the OTG function
[10]	Audio Filter	Bit[10] enables or disables the audio filter function. 0 = Disable the audio filter function (default) 1 = Enable the audio filter function

Table 12. Control1 Register 0x3CH (Cont.)

Bit	Bit Name	Description
[9:8]	Switching Frequency	Bit[9:8] configures the switching frequency and overrides the switching frequency set by the PROG pin. 00 = Switching frequency set by the PROG pin (default) 01 = 839kHz 10 = 723kHz 11 = 635kHz
[7]	Not Used	Not used
[6]	Turbo	Bit[6] enables or disables Turbo mode. When the turbo function is enabled, the BGATE FET turns on in Turbo mode. See Table 26 for the BGATE ON/OFF truth table. 0 = Enable Turbo mode (default) 1 = Disable Turbo mode
[5]	AMON/BMON Function	Bit[5] enables or disables the current monitor function AMON and BMON. 0 = Enable AMON/BMON (default) 1 = Disable AMON/BMON Bit[5] is only valid in Battery Only mode. When the adapter is present, AMON/BMON is automatically enabled and Bit[5] becomes invalid.
[4]	AMON or BMON	Bit[4] selects AMON or BMON as the AMON/BMON pin output. 0 = AMON (default) 1 = BMON
[3]	PSYS	Bit[3] enables or disables the system power monitor PSYS function. 0 = Disables the PSYS function (default) 1 = Enables the PSYS function
[2]	VSYS	Bit[2] enables or disables the buck-boost charger switching VSYS output. When disabled, the RAA489108 stops switching and forces the BGATE FET on. 0 = Enables VSYS output (default) 1 = Disables VSYS output
[1:0]	Low_VSYS_Prochot# Reference	Bit[1:0] configures the Low_VSYS_Prochot# assertion and supplemental mode activation threshold. 00 = 6.0V (default) 01 = 6.3V 10 = 6.6V 11 = 6.9V

Table 13. Control2 Register 0x3DH

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[15:14]</td><td>Trickle Charging Current</td><td>Bit[15:14] configures the charging current in Trickle Charging mode.
00 = 256mA (default)
01 = 128mA
10 = 64mA
11 = 512mA</td></tr>
<tr><td>[13]</td><td>OTG Function Enable Debounce Time</td><td>Control2 Bit[13] and Control 3 Bit[0] configures the OTG function debounce time from when the RAA489108 receives the OTG enable command.
<table>
<tr><th>Control2[13]</th><th>Control3[0]</th><th>OTG Start-Up Delay</th></tr>
<tr><td>0 (default)</td><td>0 (default)</td><td rowspan="2">1.3s</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>150ms</td></tr>
<tr><td>1</td><td>1</td><td>1ms</td></tr>
</table></td></tr>
<tr><td>[12]</td><td>Two-Level Adapter Current Limit Function</td><td>Bit[12] enables or disables the two-level adapter current limit function.
0 = Disables the current limit function (default)
1 = Enables the current limit function</td></tr>
<tr><td>[11]</td><td>Adapter Insertion to Switching Debounce</td><td>Bit[11] configures the debounce time from adapter insertion to when ACOK is asserted high.
0 = 1.3s (default)
1 = 150ms
After VDD POR, for the first time the adapter is plugged in, the ASGATE turn-on delay is always 150ms, regardless of the Bit[11] setting. This bit sets the ASGATE turn-on delay only after ASGATE turns off at least one time when VDD is above its POR value and the Bit[11] default is 0 for 1.3s.</td></tr>
<tr><td>[10:9]</td><td>Prochot# Debounce</td><td>Bit[10:9] configures the PROCHOT# debounce time before its assertion for ACProchot# and DCProchot#. The Low_VSYS_Prochot# has a fixed 8µs debounce time.
00: 7µs (default)
01: 100µs
10: 500µs
11: 1ms</td></tr>
<tr><td>[8:6]</td><td>Prochot# Duration</td><td>Bit[8:6] configures the minimum duration of the PROCHOT# signal when asserted.
000 = 10ms (default)
001 = 20ms
010 = 15ms
011 = 5ms
100 = 1ms
101 = 500µs
110 = 100µs
111 = 0s</td></tr>
<tr><td>[5]</td><td>ASGATE in OTG Mode</td><td>Bit[5] turns the ASGATE FET on or off in OTG mode.
0 = Turn on ASGATE in OTG mode (default)
1 = Turn off ASGATE in OTG mode</td></tr>
<tr><td>[4]</td><td>CMIN Reference</td><td>Bit[4] configures the general purpose comparator reference voltage.
0 = 1.2V (default)
1 = 2V</td></tr>
</table>

Table 13. Control2 Register 0x3DH (Cont.)

Bit	Bit Name	Description
[3]	General Purpose Comparator	Bit[3] enables or disables the general purpose comparator. 0 = Enable the general purpose comparator (default) 1 = Disable the general purpose comparator
[2]	CMOUT Polarity	Bit[2] configures the general purpose comparator output polarity when asserted. The comparator reference voltage is connected at the inverting input node. 0 = CMOUT is High when CMIN is higher than reference (default) 1 = CMOUT is Low when CMIN is higher than reference
[1]	Not Used	Not Used
[0]	Pass-Through Mode	Bit[0] enables or disables Pass-Through mode. 0 = Disable Pass-Through mode (default) 1 = Enable Pass-Through mode

Table 14. Control3 Register 0x4CH

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description7</th></tr>
<tr><td>[15]</td><td>Reread PROG Pin Resistor</td><td>Bit[15] specifies whether to reread the PROG pin resistor.
0 = Reread PROG pin resistor (default)
1 = Do not reread PROG pin resistor</td></tr>
<tr><td>[14]</td><td>Reload ACLIM When Adapter Is Plugged In</td><td>Bit[14] specifies whether to reload the AdapterCurrentLimit1 register set by the PROG pin resistor.
0 = Reload the AdapterCurrentLimit1 register (default)
1 = Do not reload the AdapterCurrentLimit1 register</td></tr>
<tr><td>[13]</td><td>Autonomous Charging Termination Time</td><td>Bit[13] configures the autonomous charging termination time.
0 = 20ms (default)
1 = 200ms</td></tr>
<tr><td>[12:11]</td><td>Charger Timeout</td><td>Bit[12:11] configures the SMBus charger timeout time.
00 = 175s (default)
01 = 87.5s
10 = 43.75s
11 = 5s</td></tr>
<tr><td>[10]</td><td>BGATE OFF</td><td>Bit[10] configures the BGATE operation between normal and force off.
0 = Normal BGATE operation (default)
1 = Force BGATE MOSFET off</td></tr>
<tr><td>[9]</td><td>PSYS Gain</td><td>Bit[9] configures the system power monitor PSYS output gain.
0 = 0.979µA/W (default)
1 = 0.489µA/W</td></tr>
<tr><td>[8]</td><td>Exit IDM Timer</td><td>Control7[7] and Control3[8] configure the Ideal Diode mode exit timer when the battery discharge current is less than 200mA.
<table>
<tr><th>Control3 [8]</th><th>Control7 [7]</th><th>IDM Timer</th></tr>
<tr><td>0 (default)</td><td>0 (default)</td><td>40ms</td></tr>
<tr><td>0</td><td>1</td><td>5ms</td></tr>
<tr><td>1</td><td>0</td><td>80ms</td></tr>
<tr><td>1</td><td>1</td><td>1ms</td></tr>
</table></td></tr>
</table>

Table 14. Control3 Register 0x4CH (Cont.)

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description7</th></tr>
<tr><td>[7]</td><td>Autonomous Charging Mode</td><td>Bit[7] enables or disables the Autonomous Charging mode.
0 = Enable Autonomous Charging mode
1 = Battery charging current control through SMBus (default)</td></tr>
<tr><td>[6]</td><td>AC and CC Feedback Gain</td><td>Bit[6] configures AC and CC feedback gain for high current.
0 = Ideal (default)
1 = x0.5</td></tr>
<tr><td>[5]</td><td>Input Current Limit Loop</td><td>Bit[5] enables or disables the input current limit loop.
0 = Enable input current limit loop (default)
1 = Disable input current limit loop</td></tr>
<tr><td>[4]</td><td>Input Current Limit Loop when BATGONE = 1</td><td>Bit[4] enables or disables the input current limit loop when BATGONE = 1.
0 = Enable input current limit loop when BATGONE = 1 (default)
1 = Disable input current limit loop when BATGONE = 1</td></tr>
<tr><td>[3]</td><td>AMON/BMON Direction</td><td>Bit[3] configures the AMON/BMON direction.
0 = Adapter current monitor/battery charging current monitor (default)
1 = OTG output current monitor/battery discharging current monitor</td></tr>
<tr><td>[2]</td><td>Digital Reset</td><td>Bit[2] resets all SMBus register values to the POR default value.
0 = Idle (default)
1 = Reset</td></tr>
<tr><td>[1]</td><td>Buck-Boost Stretch CCM Period</td><td>Buck-boost stretch CCM period (T2 TIME). See Control4 Bit[8] in Table 15.
<table>
<tr><th>Control3[1]</th><th>Control4[8]</th><th>T2 Time</th></tr>
<tr><td>0</td><td>0</td><td>0.6x (default)</td></tr>
<tr><td>0</td><td>1</td><td>1x</td></tr>
<tr><td>1</td><td>0</td><td>3x</td></tr>
<tr><td>1</td><td>1</td><td>2x</td></tr>
</table></td></tr>
<tr><td>[0]</td><td>OTG Start-Up Delay</td><td>Control2 Bit[13] and Control 3 Bit[0] configures the OTG function debounce time from when the RAA489108 receives the OTG enable command.
<table>
<tr><th>Control2[13]</th><th>Control3[0]</th><th>OTG Start-Up Delay</th></tr>
<tr><td>0 (default)</td><td>0 (default)</td><td rowspan="2">1.3s</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>150ms</td></tr>
<tr><td>1</td><td>1</td><td>1ms</td></tr>
</table></td></tr>
</table>

Table 15. Control4 Register 0x4EH

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[15:14]</td><td>Dither Enable</td><td>Bit[15:14] disables or selects the switching frequency dithering function.
00 = Disable dither (default)
01 = Dither 100 - 102%
10 = Dither 100 - 104%
11 = Dither 100 - 106%</td></tr>
<tr><td>[13]</td><td>ADP Side Discharge</td><td>Bit[13] enables or disables the ADP side discharge function. Typical 15mA.
0 = Disable ADP side discharge function (default)
1 = Enable ADP discharge function</td></tr>
<tr><td>[12]</td><td>VSYS Sink</td><td>Bit[12] enables or turns on the discharge FET to pull down the VSYS.
0 = Disable, 10mA sink turned off (default)
1 = Enable, 10mA sink turned on</td></tr>
<tr><td>[11]</td><td>BGATE Tri-state</td><td>Bit[11] enables or disables the BGATE tri-state function.
0 = Disable BGATE tri-state (default)
1 = Enable BGATE tri-state</td></tr>
<tr><td>[10]</td><td>Buck-Boost Min T3 Time</td><td>Bit[10] selects the minimum T3 time when in the buck-boost mode.
0 = Long (default)
1 = Short</td></tr>
<tr><td>[9]</td><td>Buck-Boost T2 time in DCM</td><td>Bit[9] selects the buck-boost T2 time in the discontinuous-conduction mode (DCM).
0 = Reduced T2 time (increases switching frequency in DCM) (default)
1 = Normal T2 time</td></tr>
<tr><td>[8]</td><td>Buck-Boost Stretch CCM Period</td><td>Buck-Boost stretch CCM period (T2 TIME). See Control3 Bit[1] in Table 14.
Control3[1] Control4[8]<table><tr><th>Control3[1]</th><th>Control4[8]</th><th>T2 Time</th></tr><tr><td>0</td><td>0</td><td>0.6x (default)</td></tr><tr><td>0</td><td>1</td><td>1x</td></tr><tr><td>1</td><td>0</td><td>3x</td></tr><tr><td>1</td><td>1</td><td>2x</td></tr></table></td></tr>
<tr><td>[7]</td><td>OTGCURRENT PROCHOT#</td><td>Bit[7] enables or disables PROCHOT# trigger with OTGCURRENT.
0 = Disable PROCHOT# trigger with OTGCURRENT (default)
1 = Enable PROCHOT# trigger with OTGCURRENT</td></tr>
<tr><td>[6]</td><td>BATGONE PROCHOT#</td><td>Bit[6] enables or disables PROCHOT# trigger with BATGONE.
0 = Disable PROCHOT# trigger with BATGONE (default)
1 = Enable PROCHOT# trigger with BATGONE</td></tr>
<tr><td>[5]</td><td>ACOK PROCHOT#</td><td>Bit[5] enables or disables PROCHOT# trigger with ACOK.
0 = Disable PROCHOT# trigger with ACOK (default)
1 = Enable PROCHOT# trigger with ACOK</td></tr>
<tr><td>[4]</td><td>Comparator PROCHOT#</td><td>Bit[4] enables or disables PROCHOT# trigger with General Purpose Comparator rising.
0 = Disable PROCHOT# trigger with General Purpose Comparator rising (default)
1 = Enable PROCHOT# trigger with General Purpose Comparator rising</td></tr>
</table>

Table 15. Control4 Register 0x4EH (Cont.)

Bit	Bit Name	Description
[3:2]	ACOK falling or BATGONE Rising Debounce	Bit[3:2] configures the debounce time from ACOK falling or BATGONE rising to PROCHOT# trip. 00 = 2µs (default) 01 = 25µs 10 = 125µs 11 = 250µs
[1]	PROCHOT# Clear	Bit[1] clears PROCHOT#. 0 = Idle (default) 1 = Clear PROCHOT#
[0]	PROCHOT# Latch	Bit[0] manually resets PROCHOT#. 0 = PROCHOT# signal auto-clear (default) 1 = Latch PROCHOT# low when tripped

Table 16. Control5 Register 0x38H

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Descriptions</th></tr>
<tr><td>[15]</td><td>T_SUP Multiplier (T_SUPM)</td><td>Bit[15] sets the supplemental mode period (T_SUPM) multiplier.
0 = 2x (default)
1 = 1x</td></tr>
<tr><td>[14]</td><td>T_SUP</td><td>Bit[14] sets the supplemental buck mode period (T_SUP).
0 = 6 (default)
1 = 10</td></tr>
<tr><td>[13:12]</td><td>R_SUP</td><td>Bit[13:12] sets the supplemental mode R_r buffer and R_r resistance. Works only when supplemental mode enabled (Control5 Bit[3] = 1)
<table>
<tr><th>Bits[13:12]</th><th>V_{ref} (V)</th><th>R_r(Ω)</th></tr>
<tr><td>00 (default)</td><td>1.35</td><td>1.35M</td></tr>
<tr><td>01</td><td>1.2</td><td>1.35M</td></tr>
<tr><td>10</td><td>1.2</td><td>2.7M</td></tr>
<tr><td>11</td><td>0</td><td>2.7M</td></tr>
</table></td></tr>
<tr><td>[11]</td><td>Adapter Low</td><td>Bit[11] enables or disables the adapter low threshold.
0 = Disable the adapter low threshold (Supplemental mode 1: Charger follows specifications for Intel's V_{MIN} Support Mechanism 1) (default)
1 = Enable the adapter low threshold (Supplemental mode 2: Charger follows specifications for Intel's V_{MIN} Support Mechanism 2)</td></tr>
<tr><td>[10:8]</td><td>Two-Level ACLIM T2 Time</td><td>Bit[10:8] sets the T2 time corresponding to AdapterCurrentLimit2 when two-level adapter current limit function is enabled.
000 = 10µs (default)
001 = 100µs
010 = 500µs
011 = 1ms
100 = 300µs
101 = 750µs
110 = 2ms
111 = 10ms</td></tr>
</table>

Table 16. Control5 Register 0x38H

Bit	Bit Name	Descriptions
[7:6]	Adapter Low Threshold	Bit[7:6] sets the adapter low threshold value. 00 = 7.2V (default) 01 = 7.8V 10 = 9V 11 = 9.6V
[5]	OTGPG PROCHOT# at OTG startup in Supplemental Mode	Bit[5] disables OTGPG PROCHOT# at OTG startup in supplemental mode. 0 = Enable (default) 1 = Disable
[4]	GM_SUP	Bit[4] sets the supplemental mode loop gain. 0 = 1x (default) 1 = 2x
[3]	Supplemental Mode	Bit[3] enables or disables supplemental mode. 0 = Disable (default) 1 = Enable
[2:0]	Two-Level ACLIM T1 Time	Bit[2:0] sets the T1 time corresponding to AdapterCurrentLimit1 when two-level adapter current limit function is enabled. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5ms 110 = 0.1ms 111 = 0ms

Table 17. Control6 Register 0x37H

Bit	Bit Name	Description
[15:8]	Not Used	Not used
[7]	Turn off BGATE at VSYSOV	Bit[7] configures the BGATE behavior during VSYSOV 0 = No action (default) 1 = Turn off BGATE
[6]	Charge Current and Maximum System Voltage Slew Rate (1 LSB/clk)[1]	Bit[6] enables or disables the charger current and maximum system voltage slew rate control. 0 = Disable the charger current and maximum system voltage slew rate control (default) 1 = Enable the charger current and maximum system voltage slew rate control
[5]	OTG Undervoltage and Overvoltage	Bit[5] enables or disables the OTG undervoltage and overvoltage protection 0 = Enable OTG undervoltage and overvoltage protection (default) 1 = Disable OTG undervoltage and overvoltage protection
[4]	Clear CMOUT Latch Data	Bit[4] can clear the current CMOUT data when it is set to 1. The CMOUT latch data can be read from Bit[4] when Control6[3] = 0 (CMOUT Latch is enabled). 0 = Do not clear CMOUT latch data (default) 1 = Clear CMOUT latch data

Table 17. Control6 Register 0x37H

Bit	Bit Name	Description
[3]	CMOUT Latch	Bit[3] enables or disables the CMOUT latch function. This bit also applies to OTGPG. 0 = Enable the CMOUT latch function (default) 1 = Disable the CMOUT latch function
[2:0]	VSYS Undervoltage Threshold[2]	Bits[2:0] set VSYS under voltage threshold. 000 = Disable 001 = 3.0V 010 = 3.9V 011 = 4.8V (default) 100 = 5.7V 101 = 6.6V 110 = 7.5V 111 = 8.4V

1. Typical values of 1LSB/clk slew rate: 8mV/µs for system voltage, and 4mA/µs for charging current with 10mΩ sense resistor, and 18mV/µs for OTG voltage.
2. When inserting the battery for the first time, VSYS UV by default is 000 = Disabled. When inserting the adapter, VSYS UV threshold by default is 011 = 4.8V.

Table 18. Control7 Register 0x36H

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>[15:8]</td><td>Not Used</td><td>Not Used</td></tr>
<tr><td>[7]</td><td>Exit IDM Timer</td><td>Control7[7] and Control3[8] configure the Ideal Diode mode exit timer when the battery discharge current is less than 200mA.
<table>
<tr><th>Control3[8]</th><th>Control7[7]</th><th>IDM Timer</th></tr>
<tr><td>0 (default)</td><td>0 (default)</td><td>40ms (default)</td></tr>
<tr><td>0</td><td>1</td><td>5ms</td></tr>
<tr><td>1</td><td>0</td><td>80ms</td></tr>
<tr><td>1</td><td>1</td><td>1ms</td></tr>
</table>
</td></tr>
<tr><td>[6:2]</td><td>Not Used</td><td>Not Used</td></tr>
<tr><td>[1]</td><td>Battery Only DCProchot# Threshold</td><td>Refer to the description of Control0[4:3] in Table 11.</td></tr>
<tr><td>[0]</td><td>VSYS ABS OV</td><td>VSYS ABS OV
0 = Enabled (default)
1 = Disabled</td></tr>
</table>

6.10 OTG Voltage Register

The OTG Voltage register contains SMBus readable and writable OTG mode output regulation voltage references. The default is 5.004V. This register accepts any voltage command, but only the valid register bits are written to the register and the maximum value is clamped at 32.256V.

Table 19. OTG Voltage Register 0x49H

Bit	Description
[2:0]	Not Used
[3]	0 = Add 0mV of OTG voltage 1 = Add 18mV of OTG voltage
[4]	0 = Add 0mV of OTG voltage 1 = Add 36mV of OTG voltage
[5]	0 = Add 0mV of OTG voltage 1 = Add 72mV of OTG voltage
[6]	0 = Add 0mV of OTG voltage 1 = Add 144mV of OTG voltage
[7]	0 = Add 0mV of OTG voltage 1 = Add 288mV of OTG voltage
[8]	0 = Add 0mV of OTG voltage 1 = Add 576mV of OTG voltage
[9]	0 = Add 0mV of OTG voltage 1 = Add 1152mV of OTG voltage
[10]	0 = Add 0mV of OTG voltage 1 = Add 2304mV of OTG voltage
[11]	0 = Add 0mV of OTG voltage 1 = Add 4608mV of OTG voltage
[12]	0 = Add 0mV of OTG voltage 1 = Add 9216mV of OTG voltage
[13]	0 = Add 0mV of OTG voltage 1 = Add 18432mV of OTG voltage
[14]	0 = Add 0mV of OTG voltage 1 = Add 36864mV of OTG voltage
[15]	Not used
Maximum	32256mV

6.11 OTG Current Register

The OTG Current register contains SMBus readable and writable OTG current limits. The default is 512mA. This register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 4096mA for R_{s1} = 20mΩ.

Table 20. OTG Current 0x4AH

Bit	Description
[4:0]	Not used
[5]	0 = Add 0mA of OTG current 1 = Add 32mA of OTG current
[6]	0 = Add 0mA of OTG current 1 = Add 64mA of OTG current
[7]	0 = Add 0mV of OTG current 1 = Add 128mA of OTG current

Table 20. OTG Current 0x4AH

Bit	Description
[8]	0 = Add 0mV of OTG current 1 = Add 256mA of OTG current
[9]	0 = Add 0mV of OTG current 1 = Add 512mA of OTG current
[10]	0 = Add 0mV of OTG current 1 = Add 1024mA of OTG current
[11]	0 = Add 0mV of OTG current 1 = Add 2048mA of OTG current
[12]	0 = Add 0mV of OTG current 1 = Add 4096mA of OTG current
[15:13]	Not used
Maximum	4096mA

6.12 Input Voltage Register

The Input Voltage register contains SMBus readable and writable input voltage limits. The default is 4.096V. This register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 27.648V.

Table 21. Input Voltage Register 0x4BH

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mV of input voltage 1 = Add 512mV of input voltage
[9]	0 = Add 0mA of input voltage 1 = Add 1024mV of input voltage
[10]	0 = Add 0mV of input voltage 1 = Add 2048mV of input voltage
[11]	0 = Add 0mV of input voltage 1 = Add 4096mV of input voltage
[12]	0 = Add 0mV of input voltage 1 = Add 8192mV of input voltage
[13]	0 = Add 0mV of input voltage 1 = Add 16384mV of input voltage
[15:14]	Not used
Maximum	27648mV

6.13 Information Register

The Information register contains SMBus readable information about manufacturing and Operating modes. Table 22, Table 23, and Table 24 identify the bit locations of the information available.

Table 22. Information1 Register 0x3AH

Bit	Description
[3:0]	Not used
[4]	Bit[4] indicates whether the Trickle Charging mode is active. 0 = Trickle Charging mode is not active 1 = Trickle Charging mode is active
[9:5]	Not used
[10]	Bit[10] indicates whether the Low_VSYS_Prochot# is tripped. 0 = Low_VSYS_Prochot# is not tripped 1 = Low_VSYS_Prochot# is tripped
[11]	Bit[11] indicates whether DCProchot# is tripped. 0 = DCProchot# is not tripped 1 = DCProchot# is tripped
[12]	Bit[12] indicates whether ACProchot#/OTGCURRENTProchot# is tripped. 0 = ACProchot#/OTGCURRENTProchot# is not tripped 1 = ACProchot#/OTGCURRENTProchot# is tripped
[14:13]	Bit[14:13] indicates the active control loop. 00 = MaxSystemVoltage control loop is active 01 = Charging current loop is active 10 = Adapter current limit loop is active 11 = Input voltage loop is active
[15]	Bit[15] indicates whether the internal reference circuit is active. Bit[15] = 0 indicates that the RAA489108 is in Low Power mode. 0 = Reference is not active 1 = Reference is active

Table 23. Information2 Register 0x4DH

Bit	Description
[4:0]	Program Resister read out Battery cell number Switching frequency Adapter current limit
[7:5]	Bit[7:5] indicates the RAA489108 operation mode. 001 = Boost Mode 010 = Buck Mode 011 = Buck-Boost Mode 101 = OTG Boost Mode 110 = OTG Buck Mode 111 = OTG Buck-Boost Mode

Table 23. Information2 Register 0x4DH (Cont.)

Bit	Description
[11:8]	Bit[11:8] indicates the RAA489108 state machine status. 0000 = OFF 0001 = BATTERY 0010 = ADAPTER 0011 = ACOK 0100 = VSYS 0101 = CHARGE 0110 = ENOTG 0111 = OTG 1000 = ENLDO5 1001 = Not Applicable 1010 = TRIM/ENCHREF 1011 = ACHRG 1100 = CAL 1101 = AGON/AGONTG 1110 = WAIT/PSYS 1111 = ADPPSYS
[12]	Bit[12] indicates the BATGONE pin status. 0 = Battery is present 1 = No battery
[13]	Bit[13] indicates the general purpose comparator output after debounce time. 0 = Comparator output is low 1 = Comparator output is high
[14]	Bit[14] indicates the ACOK pin status. 0 = No adapter 1 = Adapter is present
[15]	Not used

Table 24. Information3 Register 0x90H

Bit	Description
[15:2]	Not used
[1]	Bit[1] indicates the Pass-Through Mode (PTM) status. 0 = PTM is inactive 1 = PTM is active
[0]	Not used

7. Modulator Information

7.1 RAA489108 Buck-Boost Charger Modes of Operation

The RAA489108 buck-boost charger drives an external N-channel MOSFET bridge made of two transistor pairs as shown in Figure 24. The first pair, Q1 and Q2, is a buck arrangement with the transistor center tap connected to an inductor input as is the case with a buck converter. The second transistor pair, Q3 and Q4, is a boost arrangement with the transistor center tap connected to the output of the inductor as is the case with a boost converter. This arrangement supports bucking from a voltage input higher than the battery and also boosting from a voltage input lower than the battery.

Table 25. Operation Mode

Mode	Q1	Q2	Q3	Q4
Buck	Control FET	Sync. FET	OFF	ON
Boost	ON	OFF	Control FET	Sync. FET
Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET
OTG Buck	ON	OFF	Sync. FET	Control FET
OTG Boost	Sync. FET	Control FET	OFF	ON
OTG Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET
Pass-Through	ON	OFF	OFF	ON

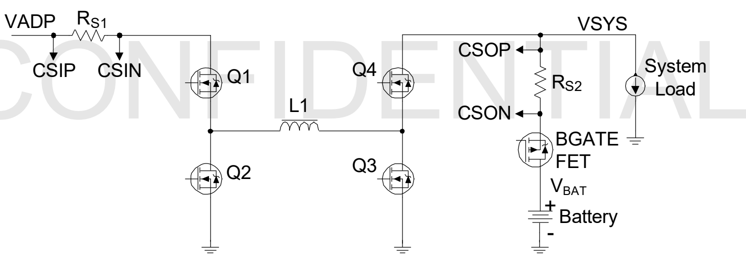


Figure 24. Buck-Boost Charger Topology

The RAA489108 optimizes the Operation mode transition algorithm by comparing the input and output voltage ratio and the load condition. When the adapter voltage V_{ADP} is rising and is higher than 90% of the system bus voltage VSYS, the RAA489108 transitions from Boost mode to Buck-Boost mode. If V_{ADP} is higher than 114% of VSYS, the RAA489108 forcedly transitions from Buck-Boost mode to Buck mode at any circumstance. At heavier loads, the mode transition point changes accordingly to accommodate the duty cycle change due to the power loss on the charger circuit.

When the adapter voltage V_{ADP} is falling and is lower than 108% of the system bus voltage VSYS, the RAA489108 transitions from Buck mode to Buck-Boost mode. If V_{ADP} is lower than 86% of VSYS, the RAA489108 transitions from Buck-Boost mode to Boost mode.

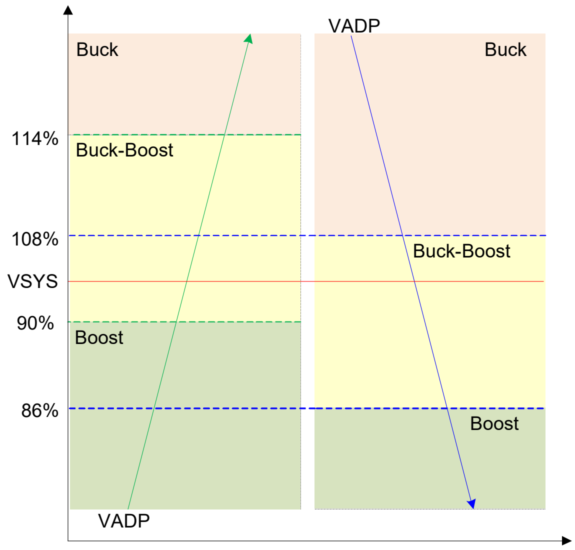


Figure 25. Operation Mode

When the Force Buck Mode is enabled by setting the Control0 Bit[1] to 1, the RAA489108 operates in Buck mode instead of Buck-Boost mode when VADP is 480mV higher than VSYS. Force Buck mode has a 240mV hysteresis window, so the RAA489108 operates in Buck-Boost mode when VADP is lower than VSYS + 240mV.

7.2 USB On-the-Go (USB OTG)

When the On-the-Go (OTG) function is enabled with the SMBus command and OTGEN pin, and if the battery voltage V_{BAT} is higher than 5.2V, the RAA489108 operates in OTG mode and one bit controls ASGATE. BATGONE must be low to enable OTG mode.

When the OTG function is enabled with the SMBus command and OTGEN pin and if the battery voltage V_{BAT} is higher than 5.2V, the RAA489108 operates in Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode.

When the RAA489108 receives the command to enable the OTG function, it starts switching after the 1.3s or 150ms debounce time set by Control2 register Bit[13]. When the OTG output voltage reaches to the OTG output voltage set by register 0x49 Bit[14:3], OTG power-good OTGPG asserts to high. Control2 register Bit[5] can also be used to turn the ASGATE FET off to cut off the OTG output.

Before OTG mode starts switching, the CSIP pin voltage needs to drop below the OTG output overvoltage protection threshold (OTG Voltage DAC(0x49h) + 100mV) first. The CSIP pin is the output sensing point in OTG mode.

The default OTG output voltage is 5.004V. The OTG Voltage register 0x49h configure the OTG output voltage.

The default OTG output current is 512mA when R_{s1} is 20mΩ. The OTG Current register 0x4Ah can be used to adjust the OTG output current limit.

The RAA489108 includes the OTG output undervoltage and overvoltage protection functions. The UVP threshold is OTG output voltage -1.8V and the OVP threshold is OTG output voltage +1.8V.

When UV is detected, the RAA489108 de-asserts OTGPG. After 32ms, it stops switching and turns off ASGATE. It resumes switching after the 1.3s or 150ms debounce time set by Control2 register Bit[13].

When OV is detected, the RAA489108 de-asserts OTGPG. It resumes switching when the OTG voltage drops below the OTG Voltage DAC value specified at 0x49.

BATGONE must be low to enable OTG mode.

7.3 Pass-Through Mode

The Pass-Through Mode (PTM) is enabled or disabled with Control2 register Bit[0]. When the Pass-Through mode control bit is enabled, REF ramps to the input voltage and the switcher continues switching until the output voltage is within ±150mV of the input (adapter) voltage. When the regulating voltage is within the 300mV window to the input voltage, the latch is set to stop switching. Q1 and Q4 are set on while Q2 and Q3 are turned off. When the PTM is enabled, all protections are still active. The following methods can be used to exit Pass-Through mode.

- Unprogram Control2 register Bit[0]. The REF ramps to the DAC and switching resumes
- Enable adapter OV triggers
- Ideal DE mode is enabled or the battery discharge current is higher than 300mA
- VSYS absolute OV triggers

Before entering Pass-Through mode, it is recommended to:

1. Ensure CV mode operation.
2. Enable slew rate Ctrl6[6] = 1
3. Change Vsysmax DAC to the value as close to VADP as possible.

When Q1 and Q4 are latching on to enter Pass-Through mode, the current limit loop turns on for more than 1ms.

7.4 Modulator Control Loops

Figure 26 shows the modulator's four main control loops. Each loop has a DAC register to provide settings as needed for each system.

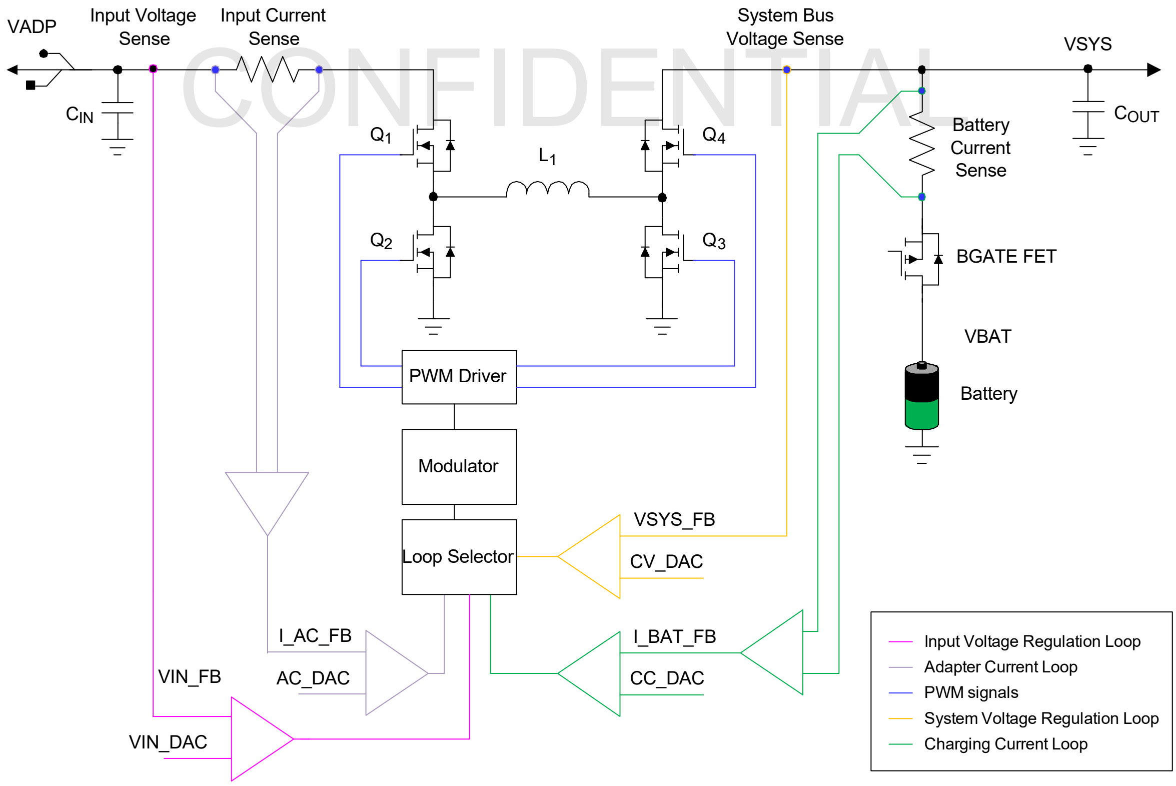


Figure 26. Charger Control Loops

7.4.1 Adapter Current Loop and Two-Level Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command to register address 0x3FH and, optionally, an AdapterCurrentLimit2 command to register address 0x3BH using the Write-word protocol for a 20mΩ R_{s1}. See Table 1 for the DAC summary of values.

The RAA489108 limits the adapter current by limiting the CSIP - CSIN voltage. By using the recommended current sense resistor values, the LSB of the register translates to 4mA of adapter current. Any adapter current limit command is accepted; however, only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers and the maximum value is clamped.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.5A or keeps the value that is written to it previously if the battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content. By default, the two level adapter current limit is disabled.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit[12]and the t1, t2 settings are configured by the Control5 register. When the two-level adapter current limit function is disabled, only the AdapterCurrentLimit1 value is used as the adapter current limit and AdapterCurrentLimit2 value is ignored.

In a real system, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The RAA489108 uses a two-level adapter current limit to fully take advantage of the surge capability of the adapter and minimize the power drawn from the battery.

Figure 27 shows the two SMBus programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current is less than 100mA lower than the AdapterCurrentLimit1 register setting. It starts at AdapterCurrentLimit2 for duration t2, then changes to AdapterCurrentLimit1 for duration t1 before repeating the pattern. These parameters can set the adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. This operation maximizes battery life.

The AdapterCurrentLimit1 register value can be higher or lower than the AdapterCurrentLimit2 value.

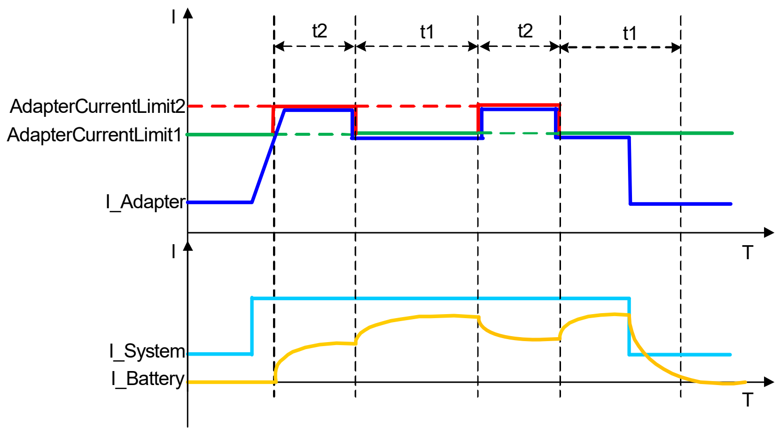


Figure 27. Two-Level Adapter Current Limit

7.4.2 USB-PD On-the-Go Output Current

The OTG output current regulation register DAC (Table 1) contains the SMBus readable and writable current that the current sense loop tries to regulate. This loop reuses the input current sense amplifier. If you are using the USB-PD Programmable Power Supply, this is the current limit loop. *Note:* The OTG_UV needs to be disabled (see Control6 Bit[5] in Table 17). This register accepts any current command, but only the valid register bits are written to the register. The maximum value is clamped.

7.4.3 Input Voltage Regulation Loop

7.4.3.1 Adapter Support Voltage

The input voltage regulation register DAC (Table 1) contains the SMBus readable and writable input voltage limit at which the input voltage loop tries to regulate when the input voltage is dropping. When the ADP is browning out or weak, the input voltage can droop and the input voltage loop tries to regulate to this setting by reducing battery charging current and then system power to try to hold up the input voltage. The system voltage may start to drop if the input power is not high enough to support the system.

This register accepts any current command but only the valid register bits are written to the register. The maximum value is clamped.

7.4.3.2 USB-PD On-the-Go Output Voltage

The OTG output voltage regulation register DAC (Table 1) contains the SMBus readable and writable voltage that the voltage loop tries to regulate. This loop reuses the input voltage sense amp.

This register accepts any current command, but only the valid register bits are written to the register. The maximum value is clamped.

7.4.4 System Voltage Regulation and Trickle Charging

This loop works with two different voltage settings, MaxSystemVoltage and MinSystemVoltage.

If the battery is absent, the BGATE is turned off (no charging) with the presence of battery the system voltage is regulated to the same setting as the MaxSystemVoltage DAC(0x15h). To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command to register address 0x15H using the Write-word protocol shown in Figure 23 and the data format shown in Table 7.

The RAA489108 supports trickle charging to overly discharged batteries. It can activate the trickle charging function when the battery voltage is lower than MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode.

To enable Trickle Charging, set the ChargeCurrent register to a non-zero value. To disable trickle charging, set the ChargeCurrent register to 0. See Table 26 for trickle charging control logic.

The trickle charging current can be programmed to be 512mA, 256mA, 128mA, or 64mA (with 10mΩ R_{s2}) through SMBus Control2 register Bit[15:14] as shown in Table 13.

In Trickle Charging mode, the RAA489108 regulates the trickle charging current through the buck-boost switcher. Another independent control loop controls the BGATE FET so that the system voltage is maintained at the voltage set in the MinSystemVoltage register. The VSYS pin is the system voltage sensing point in Trickle Charging mode.

When the battery voltage is charged to the MinSystemVoltage register value, the RAA489108 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting.

7.4.5 Charging Current Loop

This loop uses the charge current DAC (see Table 2) to set the fast charging current limit. To set it, write a 16-bit ChargeCurrentLimit command to register address 0x14H (Table 1).

The RAA489108 limits the charging current by limiting the CSOP - CSON voltage. Therefore, the charge current is dependent of the R_{s2} resistor value. For example, if the current sense resistor R_{s2} is halved, the regulated charge current doubles. By using the current sense resistor values R_{s1} = 20mΩ and R_{s2} = 10mΩ, the LSB of the register translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register.

7.4.5.1 Reverse Mode Discharge Current

When the charger is in reverse mode of operation (OTG, Supplemental mode), there is a discharge current limit loop that is set by 2xCharge Current limit register (0x14). This discharge current limit loop is in addition to the voltage regulation loop set by the OTG Voltage register and the current limit loop set by the OTG Current register. The discharge current limit loop is disabled when charge current limit (0x14h) is zero. When the charge current is a non-zero value, the charger limits the battery discharge current to be less than the discharge current, which is set by 2xCharge current limit register setting. This function can be used to limit inrush current from the battery when the OTG Voltage ramps up or down (in addition to the slew rate function).

7.4.6 Turbo Mode Support

Turbo mode refers the system drawing more power than the power rating of the adapter.

If the adapter current reaches the AdapterCurrentLimit1 register set value (or the AdapterCurrentLimit2 register set value, if the two-level adapter current limit function is enabled), or the adapter input voltage drops to the Input Voltage Regulation Reference set by Input Voltage DAC register (0x4B), the RAA489108 limits the input power by regulating the adapter current at the AdapterCurrentLimit1/2 register set value, or by regulating the adapter voltage at the Input Voltage Regulation Reference point.

In Turbo mode, the system bus voltage VSYS drops automatically or the charging current drops automatically to limit the adapter input power. If the VSYS pin voltage is 150mV lower than the VBAT pin voltage, the BGATE FET turns on so that the battery supplies the rest of the power required by the system.

If the RAA489108 detects 150mA charging current or if the battery discharging current is less than 200mA for longer than 40ms or 80ms, it turns off BGATE and exits Turbo mode. The Turbo mode exit timer can be configured through Control3 register 0x4C Bit[8]. See Table 26 for BGATE control logic.

Table 26. BGATE On/Off Truth Table

Turbo (Control Bit)	ChargeCurrent Register	BGATE On/Off	
0 = Enable 1 = Disable	**0 = Zero 1 = Nonzero**	**System Load Not In Turbo Mode Range**	**System Load in Turbo Mode Range**
0	0	OFF	ON
0	1	ON for fast charge; Trickle charge is enabled	ON
1	0	OFF	OFF
1	1	ON for fast charge; Trickle charge is enabled	ON

7.5 R3 Modulator

The RAA489108 uses the patented Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 28 conceptually shows the R3 modulator circuit, and Figure 29 shows the operation principles in steady state.

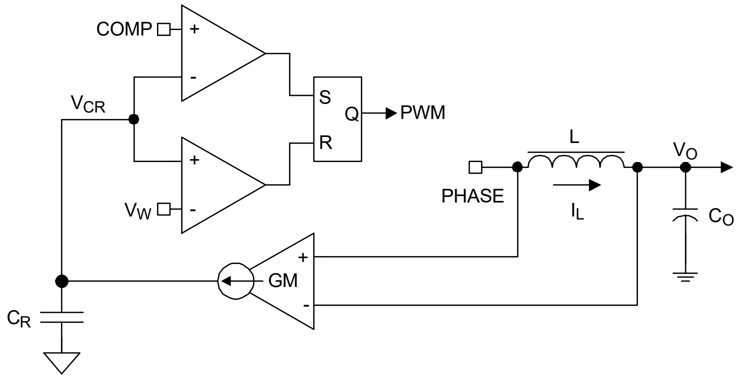


Figure 28. R3 Modulator

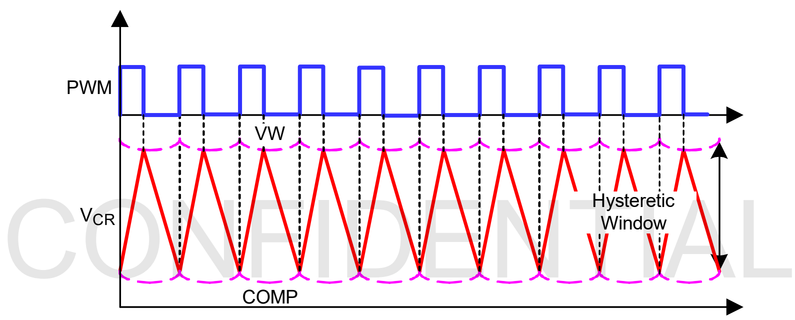


Figure 29. R3 Modulator Operation Principles In Steady State

A fixed voltage window (VW window) exists between VW and COMP. The modulator charges the ripple capacitor C_R with a current source equal to $g_m(V_{IN}-V_O)$ during PWM on-time and discharges the ripple capacitor C_R with a current source equal to g_mV_O during PWM off-time, where g_m is a gain factor. The C_r voltage V_{CR} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr}, which is large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulator.

Figure 30 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently temporarily, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

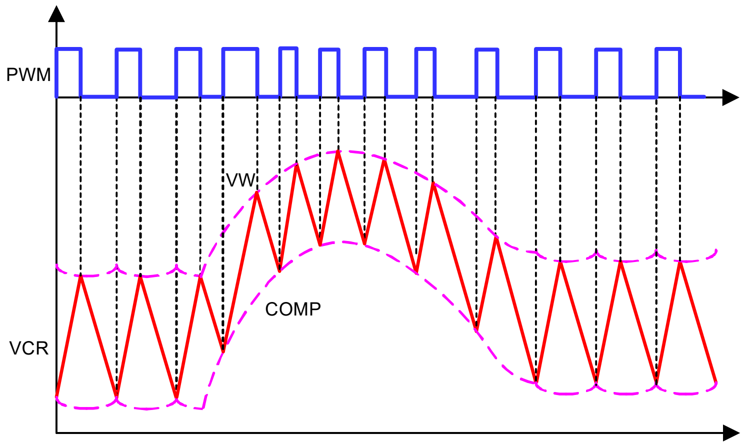


Figure 30. R3 Modulator Operation Principles In Dynamic Response

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, which emulates a diode. As shown in Figure 31, when LGATE is on, the low-side MOSFET carries current and creates negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

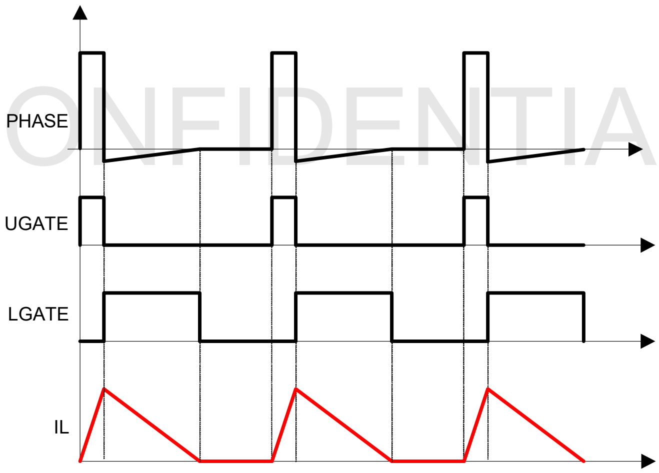


Figure 31. Diode Emulation

If the load current is light enough, as Figure 31 shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A, and the regulator is in Continuous Conduction Mode (CCM) although the controller is in DE mode.

Figure 32 shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, so the inductor current triangle is the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to mimic the inductor current. The COMP voltage takes longer to reach V_{CR}, which naturally stretches the switching period. The inductor current triangles move farther apart from each other so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

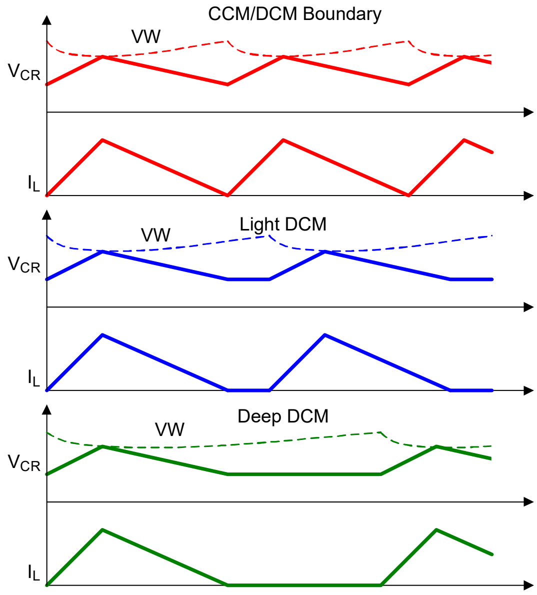


Figure 32. Period Stretching

8. Application Information

8.1 Soft-Start

The RAA489108 includes a low power LDO with nominal 4.6V output, with an input OR-ed from the VBAT and ADP pins. The RAA489108 also includes a high power LDO with nominal 5V output, with an input from the DCIN pin that connects to both the adapter and the system bus through an external OR-ing diode circuit. Both LDO outputs are tied to the VDD pin to provide the bias power and gate drive power for the RAA489108. The VDDP pin is the RAA489108 gate drive power supply input. Use an R-C filter to generate the VDDP pin voltage from the VDD pin voltage.

When V_{DD} > 2.7V, the digital block is activated and the SMBus register is ready to communicate with the master controller.

When VADP > 3.2V, after the 1.3s or 150ms debounce time set by Control2 register Bit[11] (the ASGATE turn on delay is always 150ms the first time the adapter is plugged in after VDD POR), ASGATE starts turning on with 10µA of sink current.

Use a voltage divider from the adapter voltage to set the ACIN pin voltage. The RAA489108 monitors the ACIN pin voltage to determine the presence of the adapter. When V_{DD} > 3.8V, the ACIN pin voltage exceeds 0.6V, and ASGATE is fully turned on, the RAA489108 allows the external circuit to pull up the ACOK pin. When ACOK is asserted, the RAA489108 starts switching.

The ACOK is an open-drain output pin that indicates the presence and readiness of the adapter to supply power to the system bus. The RAA489108 actively pulls ACOK low in the absence of the adapter.

Before ASGATE turns ON, the RAA489108 sources 10µA of current out of the PROG pin and reads the pin voltage to determine the PROG resistor value. The PROG resistor programs the configurations of the RAA489108.

In Battery Only mode, the RAA489108 enters Low Power mode if only the battery is present. V_{DD} is 5V from the low power LDO to minimize power consumption.

8.2 Programming Charger Option

The resistor from the PROG pin to GND programs the default number of battery cells in series, the default switching frequency, the default AdapterCurrentLimit1 register value, and the autonomous charging function. The AdapterCurrentLimit2 register default value is 1.5A. Table 27 shows the programming options.

Table 27. PROG Pin Programming Options

PROG-GND Resistance (kΩ)			Cell Number	Default Switching Frequency (Hz)	Autonomous Charging	Default ACLimit1 Reg (A)
Min	Typ. 1%	Max				
42.7	43.2	43.7	2	733k	Yes	1.5
51.7	52.3	52.9		733k	Yes	0.476
61.2	61.9	62.6		1M	No	0.476
70.6	71.5	72.4		1M	No	1.5
81.5	82.5	83.5		733k	No	1.5
92.0	93.1	94.2		733k	No	0.476
104	105	106	3	733k	No	0.476
116	118	120		733k	No	1.5
131	133	135		1M	No	1.5
145	147	149		1M	No	0.476
160	162	164		733k	Yes	0.476
176	178	180		733k	Yes	1.5
194	196	198	4	733k	Yes	1.5
212	215	218		733k	Yes	0.476
234	237	240		1M	No	0.476
258	261	264		1M	No	1.5
284	287	290		733k	No	1.5
312	316	320		733k	No	0.476

The RAA489108 uses the default number of cells in series as Table 27 shows and sets the default MaxSystemVoltage register value and default MinSystemVoltage register value accordingly.

The switching frequency can be changed through SMBus Control1 register Bit[9:8] after POR. See the SMBus Control1 register programming table (Table 12) for a detailed description.

Before ASGATE turns on, the RAA489108 sources 10µA of current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise can pollute the PROG pin voltage and cause incorrect readings. If noise is a concern, connect a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor RC time constant should be less than 40µs so the PROG pin voltage can rise to steady state before the RAA489108 reads it.

If the RAA489108 is powered up from the battery, it does not read the PROG resistor unless PSYS is enabled through SMBus Control1 register Bit[3]. Whenever PSYS is enabled in Battery Only mode, the RAA489108 reads the PROG pin resistor and resets the configuration to the default.

When the adapter is plugged in, the RAA489108 resets the AdapterCurrentLimit1 register to the default by reading the PROG pin resistor if it was not read before, or by loading the previous readings.

If PSYS is not enabled, the RAA489108 resets the MaxSystemVoltage register and MinSystemVoltage register to their default values according to the PROG pin cell number setting. If PSYS is enabled, the RAA489108 keeps the values in these two registers.

By default, the adapter current sensing resistor R_{s1} is 20mΩ and the battery current sensing resistor R_{s2} is 10mΩ. Using this R_{s1} = 20mΩ and R_{s2} = 10mΩ option results in a 4mA/LSB correlation in the SMBus current commands.

If the R_{s1} and R_{s2} values are different from this R_{s1} = 20mΩ and R_{s2} = 10mΩ option, the SMBus command needs to be scaled accordingly to obtain the correct current. Smaller current sense resistor values reduce power loss while larger current sense resistor values give better accuracy.

If different current sensing resistors are used, the R_{s1}:R_{s2} ratio should be kept as 2:1 so that the PSYS output can be scaled accordingly to reflect the total system power correctly.

The information in this datasheet is based on current sensing resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ unless specified otherwise.

8.3 Autonomous Charging Mode

Autonomous Charging mode can be enabled or disabled through the programming charging option resistor or SMBus Control3 register Bit[7]. When Autonomous Charging mode is enabled, this mode can also be disabled by writing to the SMBus ChargeCurrentLimit or MaxSystemVoltage command.

The RAA489108 enters Autonomous Charging mode when the battery voltage is lower than MaxSystemVoltage - 200mV per cell for 1ms of debounce time and the BGATE MOSFET is on.

In Autonomous Charging mode, the RAA489108 starts to charge the battery with 2A (with R_{S2} = 10mΩ), the PROCHOT# pin (Autonomous Charging mode indication pin) is pulled down to GND, and the 175s charging timeout timer is disabled. The RAA489108 exits from Autonomous Charging mode when the battery charging current is less than 200mA (with R_{S2} = 10mΩ) for 20ms or 200ms in CV loop. This autonomous charging termination time can be set by Control3 register Bit[13]. The RAA489108 re-enters Autonomous Charging mode when the battery voltage is discharged below MaxSystemVoltage - 200mV per cell. When the RAA489108 stays in Autonomous Charging mode for 12hrs, which means the battery charging current is higher than 200mA and the battery cannot be charged to MaxSystemVoltage for 12hrs, the RAA489108 stops charging the battery and exits Autonomous Charging mode.

8.4 Battery Ship Mode

The RAA489108 supports Battery Ship mode. When Control3 register Bit[10] is 1, the BGATE MOSFET stays off for Battery Ship mode.

Battery Ship mode sets the lowest power state for the IC. Ship mode can only be entered from Battery Only mode. To achieve the lowest power, several analog functions must be disabled. Many are disabled by default and do not need to be written, but all are listed for completeness. However, the power level can be customized for the system.

- Control1 0x3C
  - Bit[5] = 1 Disable IMON
  - Bit[3] = 0 Disable PSYS
- Control2 0x3D
  - Bit[3] = 1 Disable GP Comparator
- Control3 0x4C
  - Bit[10] = 1 Force BGATE Off
- Control 5 0x38
  - Bit[3] = 0 Disable Supplemental mode

To exit Battery Ship mode, use the SMBus to change the control bits.

8.5 Diode Emulation Operation

In Diode Emulation (DE) mode, the RAA489108 uses a phase comparator to monitor the PHASE node voltage during the low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the RAA489108 can lose DE ability. To prevent this, the RAA489108 uses a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the RAA489108 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

8.6 Battery Learn Mode

Use Battery Learn mode to supply the system power from the battery even when the adapter is plugged in, such as calibration of the battery fuel gauge.

The RAA489108 enters Battery Learn mode when it receives the SMBus Control command. When entering Battery Learn mode, the RAA489108 turns on the BGATE FET.

In Battery Learn mode, the RAA489108 turns on BGATE and keeps ASGATE on but turns off the buck-boost switcher regardless of whether the adapter is present.

The three ways of exiting Battery Learn mode are:

- Receive the Battery Learn mode exit command through SMBus
- The battery voltage is less than MinSystemVoltage register setting (according to the Control1 register Bit[12] setting)
- The BATGONE pin voltage goes from logic LOW to HIGH

In all these cases, the RAA489108 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

8.7 Charger Timeout

The RAA489108 includes a timer to ensure the SMBus master is active and to prevent overcharging the battery. The RAA489108 terminates charging by turning off the BGATE FET if the charger has not received a write command to the MaxSystemVoltage or ChargeCurrent register within 175s (SMBus Control3 register Bit[12:11] = 00). Charger timeout time can be configured through SMBus Control3 register Bit[12:11]. When charging is terminated by the timeout, the ChargeCurrent register retains its value instead of resetting to zero. If a timeout occurs, the MaxSystemVoltage or ChargeCurrent register must be written to re-enable charging.

The RAA489108 allows you to disable the charger timeout function through SMBus Control0 register Bit[7] as Table 11 shows.

8.8 Supplemental Power Support Mode

Supplemental power mode (also known as Intel VMIN Active mode or VAP) allows the use of the unattached input bias capacitor to store energy and release it to the system during a high power demand. In this mode, the IC uses OTG mode to fill the input capacitance to store energy. When a large power event drops the VSYS voltage below the Low_VSYS_Prochot# level (set by Control1 Bit[1:0]), it quickly uses the stored energy and begins to buck from the input capacitance to hold up the VSYS node voltage.

Supplemental mode is designed to temporarily support the VSYS rail, because impedance from the battery pack (including battery impedance) to VSYS causes a drop during increased current loads. Set the OTGV voltage register 0x49H (Table 1) to the highest tolerable voltage on the input capacitance to store the maximum available energy.

If the adapter low threshold is disabled (Control5 Bit[11] = 0 Supplemental mode 1: Charger follows specifications for Intel's V_{MIN} Support Mechanism 1), low VSYS (lower than the Low_VSYS_Prochot# threshold) causes PROCHOT# to let the processor know to throttle the power request. If the adapter low threshold is enabled (Control5 Bit[11] = 1 Supplemental mode 2: Charger follows specifications for Intel's V_{MIN} Support Mechanism 2), PROCHOT# asserts when both the Low_VSYS_Prochot# threshold and adapter low threshold are reached. Use Control5 Bit[7:6] to configure the adapter low threshold.

Note: Many capacitors reduce their total capacitance with higher applied voltage. Using the recommend maximum input capacitor of 150µF, the stored capacitor energy momentarily supplements the power provided by the battery under this condition.

During the OTG mode switching operation to fill the input capacitance, the battery discharge current should be limited to prevent an undesired PROCHOT warning during the charging of the input capacitor. The current used to refill the input cap is the value of the discharge current set by register 0x14H (Table 1) minus the system load.

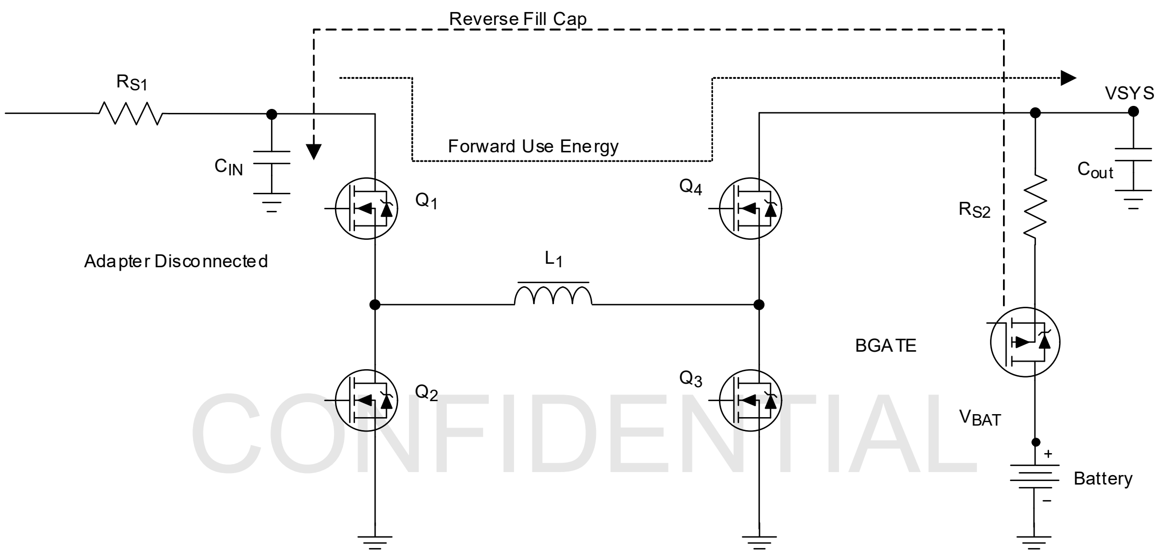


Figure 33. Supplemental Mode Energy Flow

Because the GPCOMP is shared with the same pin OTGEN, there is some logic to control whether it is supplemental support or OTG mode.

- If GPCOMP is enabled (Control2[3] = 0), only OTG can be enabled. The OTG function register bit (Control1[11]), supplemental mode bit (Control5[3], and the OTGEN pin become don't care conditions.
- If GPCOMP is disabled (Control2[3] = 1), supplemental mode is disabled (Control5[3] = 0), the OTG function register bit is enabled (Control1[11]), the OTGEN pin is enabled (Pin 26), and OTG can be enabled.
- If GPCOMP is disabled (Control2[3] = 1), the supplemental mode register bit is enabled (Control5[3] = 1), the OTGEN register bit is low (Control1[11] = 0), the OTGEN pin is high, and supplemental mode can be enabled.

The function must be set up and armed. Figure 34 and Table 28 describe the logical function.

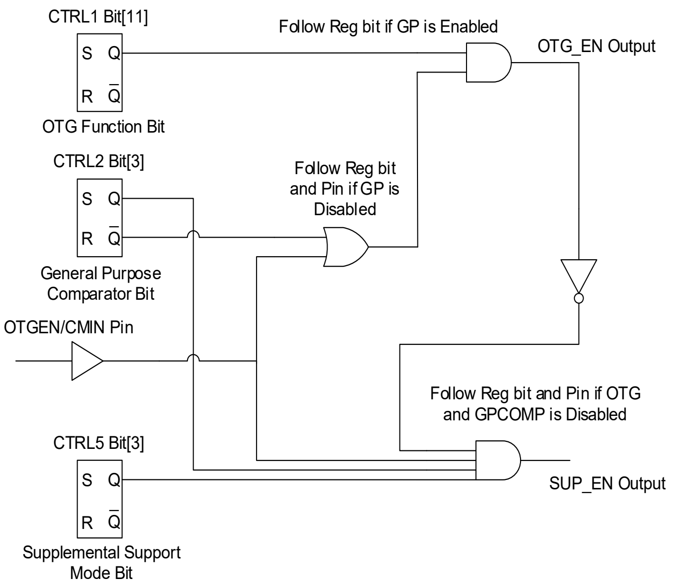


Figure 34. Simplified Control Logic for OTG and Supplemental Mode

Table 28. Control Logic Truth Table for OTG and Supplemental Mode

Inputs				Outputs	
External Pin OTGEN/CMIN	**CTRL5 Bit[3] Supplemental Mode**	**CTRL2 Bit[3] GP Comparator**	**CTRL1 Bit[11] OTG Function**	**Logic Control Signal**	**Logic Control Signal**
	1 - SUP 0 - OTG	**1 - Disable 0 - Enable**	**1 -Enable 0 - Disable**	**OTG Mode (OTG_EN)**	**Supplemental Mode (SUP_EN)**
0	1	1	0	0	0
0	1	1	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
1	1	1	0	0	1
1	1	1	1	1	0
1	0	1	0	0	0
1	0	1	1	1	0
x	x	0	0	0	0
x	x	0	1	1	0

8.9 Monitoring

8.9.1 Current Monitor

The RAA489108 provides an adapter current monitor/OTG current monitor or a battery charging current monitor/battery discharging current monitor through the AMON/BMON pin. The AMON output voltage is 18x (CSIP - CSIN) and 18x (CSIN - CSIP) voltage. The BMON output voltage is 18x (CSON - CSOP) and 36x (CSOP - CSON) voltage.

The AMON and BMON functions can be enabled or disabled through SMBus Control1 register Bit[5]. AMON or BMON can be selected through SMBus Control1 register Bit[4] and the AMON/BMON direction can be configured through SMBus Control3 register Bit[3] as Table 12 shows.

8.9.2 PSYS Monitor

The RAA489108 PSYS pin provides a measure of the instantaneous power consumption of the entire platform. The PSYS pin outputs a current source described by Equation 1.

(EQ. 1) $$I_{PSYS} = K_{PSYS} \times (V_{ADP} \times I_{ADP} + V_{BAT} \times I_{BAT})$$

K_{PSYS} is based on the current sensing resistor R_{s1} = 20mΩ and R_{s2} = 10mΩ. V_{ADP} is the adapter voltage in V, I_{ADP} is the adapter current in A, V_{BAT} is the battery voltage, and I_{BAT} is the battery discharging current. When the battery is discharging, I_{BAT} is a positive value; when the battery is being charged, I_{BAT} is a negative value. The battery voltage V_{BAT} is detected through the CSON pin to maximize the power monitor accuracy in NVDC configuration Trickle Charge mode.

The R_{s1} to R_{s2} ratio must be 2:1 for valid power calculation. If the resistance values are higher (or lower) than the suggested values mentioned previously, K_{PSYS} is proportionally higher (or lower). As an example, if R_{s1} = 10mΩ and R_{s2} = 5mΩ, the output current is half that above for the same power. If the PSYS information is not needed, any R_{s1}:R_{s2} ratio is acceptable.

The PSYS gain can be configured through SMBus Control3 register Bit[9]. The default PSYS gain is set to 0.979µA/W and a 0.489µA/W PSYS gain option is available.

The PSYS information includes the power loss of the charger circuit and the actual power delivered to the system. The resistor R_{PSYS} connected between the PSYS pin and GND converts the PSYS information from current to voltage.

PSYS accuracy limits and a typical accuracy scan are shown in Figure 35.

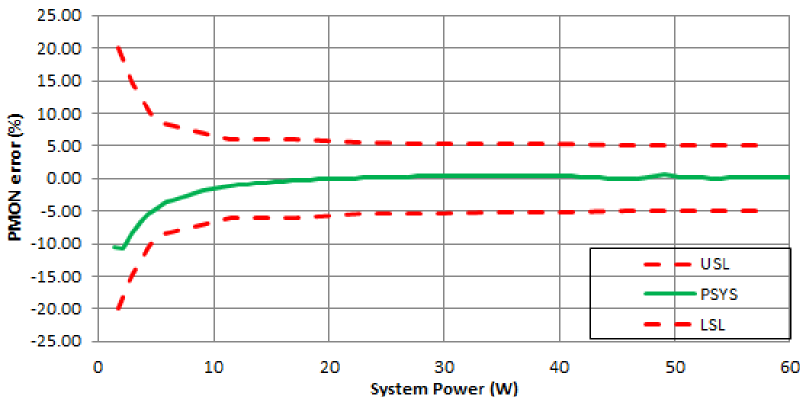


Figure 35. PSYS Accuracy and Limits

The PSYS function can be enabled or disabled through SMBus Control1 register Bit[3] as shown in Table 12.

In Battery Only mode, the PSYS function cannot work if the battery voltage is less than 5.2V.

8.10 Stand-Alone Comparator

The RAA489108 includes a general purpose stand-alone comparator. The OTGEN/CMIN pin is the comparator input. The internal comparator reference is connected to the inverting input of the comparator and can be configured as 1.2V or 2V through SMBus Control2 register Bit[4]. The comparator output is the OTGPG/CMOUT pin. The output polarity can be configured through the SMBus register bit when the comparator is tripped.

- When Control2 register Bit[2] = 0 for normal comparator output polarity, CMOUT = High if CMIN > Reference; CMOUT = Low if CMIN < Reference.
- When Control2 register Bit[2] = 1 for inversed comparator output polarity, CMOUT = Low if CMIN > Reference; CMOUT = High if CMIN < Reference.

By default in Battery Only mode, the stand-alone comparator is enabled. This comparator can be enabled/disabled in Battery Only mode using Control 2 Bit[3]. In Battery Only mode, the reference is set to 1.2V only.

Table 29 shows the OTG mode and the stand-alone comparator truth table.

Table 29. OTG and Comparator Truth Table

				Description
Control1 Register 0x3C	Control2 Register 0x3D	PIN-2O	PIN-26	
Bit[11] OTG Function Enable/Disable	Bit[3] Comparator Enable/Disable	OTGEN/CMIN	OTGPG/CMOUT	
0	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT	OTG function is disabled. Comparator is enabled.
0	1	X	X	Both the OTG function and comparator are disabled.
1	0	Comparator Input Pin CMIN	Comparator Output Pin CMOUT	Both the OTG function and comparator are enabled. OTG function is enabled when V_{BAT} > 5.2V and Control1 register Bit[11] = 1 without OTG power-good pin indication. The device is in OTG mode while Information1 register 0x3A Bit[6:5] = 11.
1	1	OTG Enable Input Pin OTGEN	OTG Power-Good Indication Pin OTGPG	Comparator is disabled. OTG function is enabled when V_{BAT} > 5.2V and ENOTG pin = High and Control1 register Bit[11] = 1.

8.11 Protections

8.11.1 Adapter Overvoltage Protection

If the ADP pin voltage exceeds 33.3V for more than 10µs, an adapter overvoltage condition occurs. The RAA489108 turns off the ASGATE MOSFETs to isolate the adapter from the system, de-asserts the ACOK signal by pulling it low, and stops switching. BGATE turns on for the battery to support the system load. When the ADP voltage drops below 32.78V from more than 100µs, it starts to turn on ASGATE and start switching.

8.11.2 System Overvoltage Protection

The RAA489108 provides system rail overvoltage protection. If the system voltage VSYS is 800mV higher than MaxSystemVoltage register set value, it declares the system overvoltage and stops switching. It resumes switching without the 1.3s or 150ms debounce when VSYS drops 400mV below the system overvoltage threshold.

The RAA489108 provides VSYS absolute overvoltage protection. The absolute overvoltage rising threshold is 23.5V; if the system voltage VSYS is higher than 23.5V, it stops switching. When the VSYS drops to lower than 23.15V, it starts switching again.

8.11.3 System Voltage Rail Short Protection

The RAA489108 has a system rail short protection (VSYSOK) to prevent powering on the system rail into a short-circuit before switching starts. When the VSYS voltage is below 0.6V, the RAA489108 sources 10mA current from VDDP to charge VSYS before switching can start.

From VSYSOK (VSYS rail short protection) beginning to switching start in VSYS state, the parts must go through multiple startup and initialization transition states, including turning on A-FET. This initialization transition duration may or may not take longer than VSYS voltage is charged above 0.6V using a 10mA source by the VSYSOK function. If this initialization transition duration is longer than the duration of charging VSYS above 0.6V, the charger must wait until the transition duration is completed before switching starts, and vice versa.

Conversely, the duration of charging VSYS above 0.6V, which depends on the leakage current and capacitance value at VSYS, varies per individual system design. If users would like to estimate the duration in a worst-case scenario, Renesas recommends testing their design to determine the following:

- If the initialization transition duration is longer than the duration of charging VSYS above 0.6V, one may add a 30% margin (considering ±5% clock tolerance) to estimate the duration.
- If the initialization transition duration is shorter than the duration of charging VSYS above 0.6V, one can check the tolerance of the VSYS capacitance or leakage current from VSYS downstream circuitry and then add a reasonable margin, such as 40% (considering ±20% cap tolerance), to estimate the duration.

After switching starts, the charger enters the Fault state if VSYS drops below 0.6V again at any time. After entering the Fault state, the charger stops switching and turns off ASGATE, and tries to start again with 1.3s or 150ms debounce time (configured by Control 2[11]).

For RAA489108 startup without battery pack present, Renesas recommends checking total system loading on VSYS, zero load preferred, and ensure it does not exceed the worse-case value, VSYS loading <19.8µA for VSYS <0.6V.

8.11.4 System Voltage Undervoltage Protection (for Short-Circuit Protection)

The charger has a fixed undervoltage protection on the system side that can be configured using Control 6[2:0].

When inserting the battery for the first time, VSYS UV by default is 000 = Disabled. When inserting the adapter, VSYS UV threshold by default is 011 = 4.8V. When the VSYS voltage falls to the VSYS UV threshold set by Control 6[2:0], there is a 100ms debounce before the charger enters FAULT state. After entering FAULT state, there is no switching and charger tries to start switching again after 1.3s (configurable by Control 2[11]).

8.11.5 Over-Temperature Protection

The RAA489108 stops switching for self protection when the junction temperature exceeds +140°C. When the temperature falls below +120°C and after a 100µs delay, the RAA489108 resumes switching.

8.12 Selecting the Power Source

The RAA489108 automatically selects the adapter and/or the battery as the source for system power.

The BGATE pin drives a P-channel MOSFET gate that connects/disconnects the battery from the system and the switcher.

The ASGATE pin drives a pair of back-to-back common source PFETs to connect/disconnect the adapter from the system and the battery. Use of the ASGATE pin is optional.

When the battery voltage V_{BAT} is higher than 2.4V and the adapter voltage V_{ADP} is less than 3.2V, the RAA489108 operates in Battery Only mode. During Battery Only mode, the RAA489108 turns on the BGATE FET to connect the battery to the system. In Battery Only mode, the RAA489108 consumes very low power (less than 20µA). The battery discharging current monitor BMON can be turned on during this mode to monitor the battery discharging current. If the battery voltage V_{BAT} is higher than 5.2V, the system power monitor PSYS function also can be turned on during this mode to monitor system power.

In Battery Only mode, the USB OTG function can be enabled when the battery voltage V_{BAT} is higher than 5.2V. See the Features for details.

When the adapter voltage V_{ADP} is more than 3.2V, the RAA489108 turns on ASGATE. If VDD is higher than 3.8V, the RAA489108 enters Forward Buck, Forward Boost, or Forward Buck-Boost mode depending on the adapter and system voltage VSYS duty cycle ratio. The system bus voltage is regulated at the voltage set on the MaxSystemVoltage register. If the charge current register is programmed (non-zero), the RAA489108 charges the battery either in Trickle Charging mode or Fast Charging mode, as long as BATGONE is low.

9. General Application Information

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following sections. In addition to this guide, Renesas provides complete reference designs that include schematics, bill of materials, and example board layouts.

9.1 Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 2:

(EQ. 2) $$D = \frac{V_{OUT}}{V_{IN}}$$

The output inductor peak-to-peak ripple current is written by Equation 3:

(EQ. 3) $$I_{P-P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L}$$

A typical step-down DC/DC converter has an I_{P-P} of 20% to 40% of the maximum DC output load current for a practical design. The value of I_{P-P} is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 4 where I_{LOAD} is the converter output DC current.

(EQ. 4) $$P_{COPPER} = I_{LOAD}^2 \cdot DCR$$

The copper loss can be significant, so select DCR carefully. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written by Equation 5 and Equation 6:

(EQ. 5) $$\Delta V_{ESR} = I_{P-P} \cdot ESR$$

(EQ. 6) $$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

9.2 Selecting the Input Capacitor

The important parameters for input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and that are capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 36 is a graph of the input capacitor RMS ripple current that is normalized relative to output load current. The graph is also a function of duty cycle and is adjusted for converter efficiency.

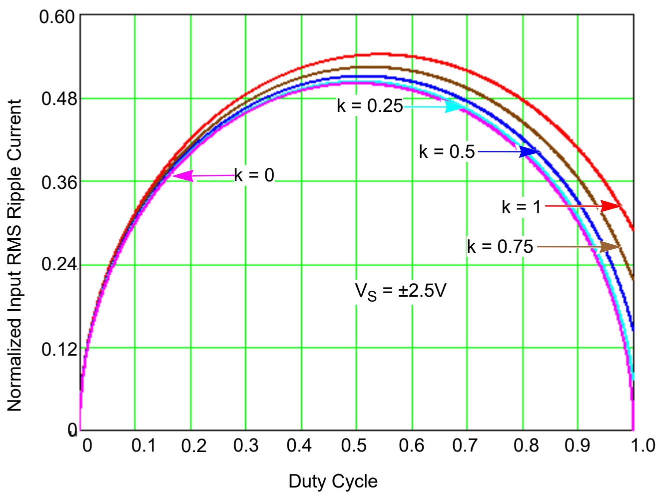


Figure 36. Normalized RMS Input Current at EFF = 1

The normalized RMS ripple current calculation is written by Equation 7:

(EQ. 7)
$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1-D) + \frac{D \cdot k^2}{12}}}{I_{MAX}}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to peak ripple amplitude expressed as a ratio of I_{MAX} (0 to 1)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written by Equation 8:

(EQ. 8)
$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

9.3 Selecting the Switching Power MOSFET

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds both the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs that are optimized for DC/DC converter applications are readily available. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately VIN - VOUT, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. *Note:* This is an optimal configuration of MOSFET selection for low duty cycle applications ($D < 50\%$). For higher output, low input voltage solutions, a more balanced MOSFET selection for high-side and low-side devices may be needed.

The power loss of the Low-Side (LS) MOSFET can be assumed to be conductive only and is written by Equation 9:

(EQ. 9)
$$P_{CON\_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)\_LS} \cdot (1-D)$$

The conduction loss of the High-Side (HS) MOSFET is written by Equation 10:

(EQ. 10)
$$P_{CON\_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)\_HS} \cdot D$$

The switching loss of the HS MOSFET is written by Equation 11:

(EQ. 11)
$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{SWON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{SWOFF} \cdot f_{SW}}{2}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- $t_{SW(ON)}$ is the time required to drive the device into saturation
- $t_{SW(OFF)}$ is the time required to drive the device into cut-off

9.4 Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 12:

(EQ. 12) $$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}}$$

where:

- Q_g is the total gate charge required to turn on the high-side MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on.

As an example, suppose the HS MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF is sufficient. Use an X7R or X5R ceramic capacitor. Renesas recommends using a bootstrap capacitor of 0.47µF (25V), which has an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance.

9.5 Switching Power MOSFET Gate Capacitance

The RAA489108 includes an internal 5V LDO output at the VDD pin, which can be used to provide the switching MOSFET gate driver power through the VDDP pin with an RC filter. The 5V LDO output overcurrent protection threshold is 85mA, minimal (check EC table for the accurate value). When selecting the switching power MOSFET, consider the MOSFET gate capacitance carefully to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, the gate drive current can be estimated by Equation 13:

(EQ. 13) $$I_{driver} = Q_g \bullet f_{SW}$$

where:

- Q_g is the total gate charge, which can be found in the MOSFET datasheet
- f_{SW} is the switching frequency

Renesas recommends using a 2.2µF (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

9.6 DCIN Filter

An RC filter is connected at the DCIN pin. Renesas recommends connecting a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7µF DCIN capacitor to GND, which has an effective capacitance higher than 0.4µF at 28V.

9.7 Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike can damage the ASGATE MOSFET or the RAA489108 pins connecting to the adapter connector node. One low cost solution is to add an R-C snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 37. A practical value of the R-C snubber is 2.2Ω to 2.2µF, while the appropriate values and power rating should be carefully characterized based on the actual design. Renesas does not recommend adding a pure capacitor at the adapter connector node, which can cause an even larger voltage spike due to the adapter cable or the adapter current path parasitic inductance.

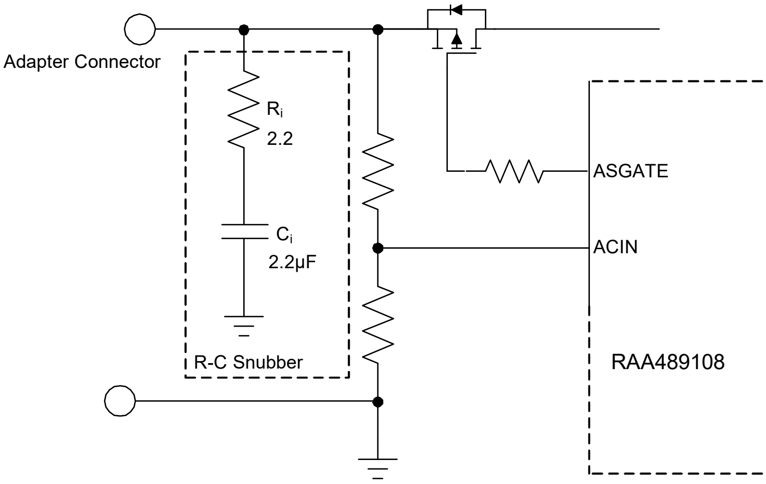
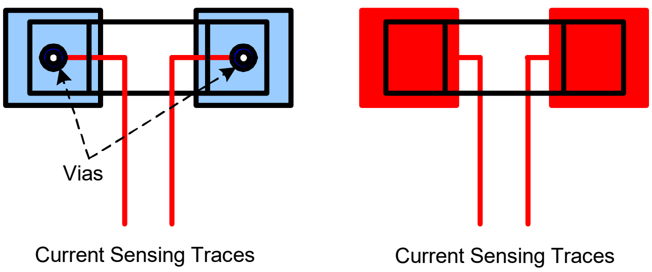


Figure 37. Adapter Input R-C Snubber Circuit

10. Layout

Pin Number	Pin Name	Layout Guidelines
Bottom Pad 33	GND	Connect this ground pad to the ground plane through a low impedance path. Use at least five vias to connect to the PCB ground planes to ensure sufficient thermal dissipation directly under the IC.
1	CSON	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current sensing resistor to the IC. Place the differential mode and common-mode RC filter components in the general proximity of the controller.
2	CSOP	Route the current sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
3	VSYS	This signal pin provides feedback for the system bus voltage. Place the optional RC filter in the general proximity of the controller. Run a dedicated trace from the system bus to the pin and do not route near the switching traces. Do not share the same trace with the signal routing to the DCIN pin OR diodes and the CSOP trace.
4	BOOT2	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide traces. Avoid any sensitive analog signal traces from crossing over or getting close.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Layout Guidelines</th></tr>
<tr><td>5</td><td>UGATE2</td><td rowspan="2">Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close. Route the PHASE2 trace to the high-side MOSFET source pin instead of general copper.

Place the IC close to the gate terminals of the switching MOSFETs and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs.

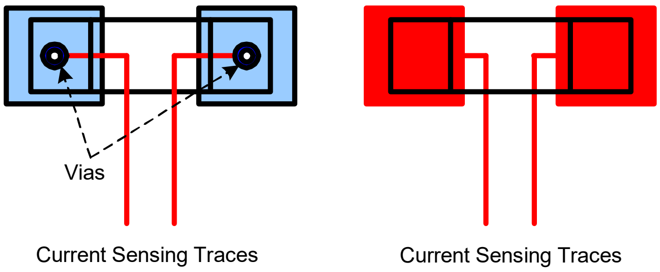
Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source, and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection.

Place the inductor terminal to the switching high-side MOSFET source and low-side MOSFET drain terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.</td></tr>
<tr><td>6</td><td>PHASE2</td></tr>
<tr><td>7</td><td>LGATE2</td><td>Switching pin. Run the LGATE2 trace in parallel with the UGATE2 and PHASE2 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close.</td></tr>
<tr><td>8</td><td>VDDP</td><td>Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to the VDD pin with sufficient width.</td></tr>
<tr><td>9</td><td>LGATE1</td><td>Switching pin. Run the LGATE1 trace in parallel with the UGATE1 and PHASE1 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close.</td></tr>
<tr><td>10</td><td>PHASE1</td><td rowspan="2">Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal traces from crossing over or getting close. Route the PHASE1 trace to the high-side MOSFET source pin instead of general copper.

Place the IC close to the gate terminals of the switching MOSFETs and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs.

Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source, and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection.

Place the inductor terminal to the switching high-side MOSFET source and low-side MOSFET drain terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area big enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.</td></tr>
<tr><td>11</td><td>UGATE1</td></tr>
<tr><td>12</td><td>BOOT1</td><td>Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficient wide trace. Avoid any sensitive analog signal traces from crossing over or getting close.</td></tr>
<tr><td>13</td><td>ASGATE</td><td>Run this trace with sufficient width in parallel fashion with the ADP pin trace.</td></tr>
</table>

Pin Number	Pin Name	Layout Guidelines
14	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Route the current sensing traces through vias to connect the center of the pads or route the traces into the pads from the inside of the current sensing resistor. The following drawings show the two preferred ways of routing current sensing traces. 
15	CSIP	
16	ADP	Run this trace with sufficient width in parallel fashion with the ASGATE pin trace.
17	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller. Run the VADP trace and VSYS trace to the OR diodes with sufficient width.
18	VDD	Place the RC filter connecting with the VDDP pin in the general proximity of the controller. Run the trace connecting to the VDDP pin with sufficient width.
19	ACIN	Place the voltage divider resistors and the optional decoupling capacitor in the general proximity of the controller.
20	OTGEN/CMIN	No special consideration.
21	SDA	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
22	SCL	
23	PROCHOT#	Digital pin, open-drain output. No special consideration.
24	ACOK	
25	BATGONE	Digital pin. Place the 100kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller.
26	OTGPG/ CMOUT	Digital pin, open-drain output. No special consideration.
27	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.
28	COMP	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
29	AMON/BMON	No special consideration. Place the optional RC filter in the general proximity of the controller.
30	PSYS	Signal pin, current source output. No special consideration.
31	VBAT	Place the optional R-C filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC.
32	BGATE	Use sufficient width trace from the IC to the BGATE MOSFET gate. Place the capacitor from BGATE to ground close to the MOSFET.

11. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

12. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type[3]	Temp. Range
RAA489108ARGNP#AA0	489108 ARGNPA	32 Ld 4x4 TQFN	L32.4x4D	Tube	-10 to +100°C
RAA489108ARGNP#HA0				Reel, 6k	
RAA489108A3GNP#AA0	489108 A3GNPA			Tube	-40 to +105°C
RAA489108A3GNP#HA0				Reel, 6k	
RTKA489108DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA489108 product page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

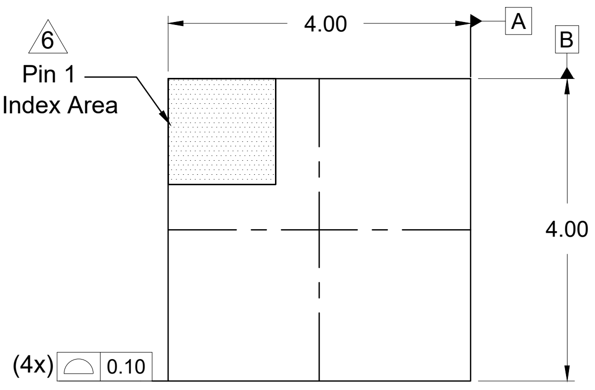
13. Revision History

Rev.	Date	Description
1.05	Mar 14, 2025	Updated IMVP8 to IMVP. Updated POD L32.4x4D to the latest version; changes are as follows: ▪ Converted to the new format ▪ Corrected typos on notes ▪ Added four dimensions to the Land Pattern
1.04	Oct 27, 2023	Added Evaluation Board to Ordering Information.
1.03	Sep 1, 2023	Minor update to Soft-Start section.
1.02	May 11, 2023	Updated Table 11 Bit [12:10]. Updated Table 14 Bits [8] and [4]. Updated the USB On-the-Go (USB OTG) section. Updated the System Voltage Rail Short Protection section.
1.01	Feb 1, 2023	Updated Pins 12 and 31 description. Updated the BMON Accuracy on page 14 minimum specification from -16 to -25 and the maximum from 16 to 25. Updated Switching Power MOSFET Gate Capacitance section.
1.00	Jan 13, 2023	Initial release

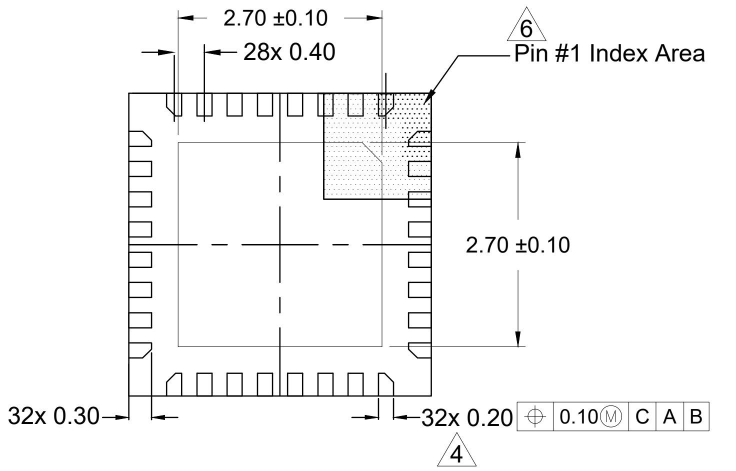
Package Outline Drawing

32 Lead Thin Quad Flat No-Lead Plastic Package

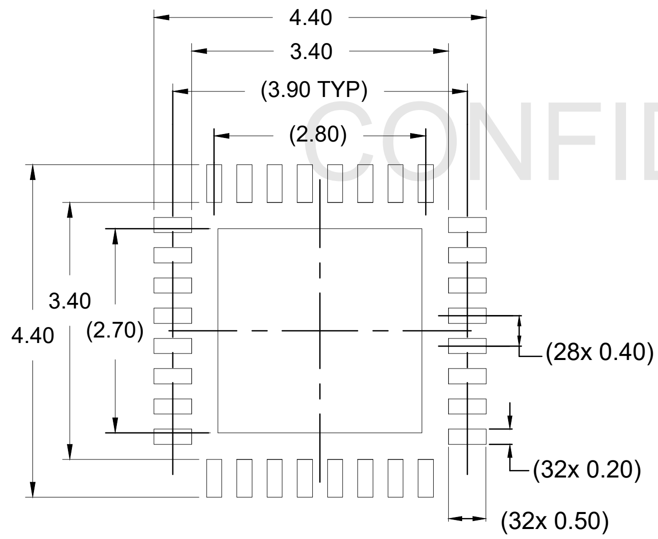
POD Number L32.4x4D, Revision No: 03, Date Created: Sept 11, 2024



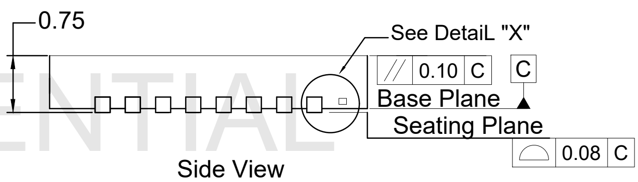
Top View



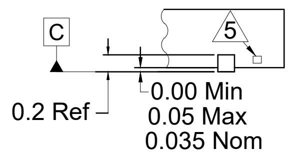
Bottom View



Typical Recommended Land Pattern



Side View



Detail "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.