RAA2P3500

Single Coil High-Speed Inductive Position Sensor IC with SPI, UART, and Incremental/UVW Interfaces

RAA2P3500 is a high-speed magnet-free, inductive position sensor IC that can be used for high-speed absolute and incremental position sensing in automotive, industrial, medical, and consumer applications.

It operates on the principle of eddy currents to detect the position of a simple metallic target that is moving above a set of coils, comprising one transmitter coil and two receiver coils.

The RAA2P3500 is equipped with:

- 14-bit SPI interface
- 14-bit High-speed UART interface (up to 2 Mbit/s)
- 12/14-bit Incremental interfaces ABI and Step/Direction
- UVW interface
- AB (Step/Dir) 12/14-bit + PWM output
- AB (Step/Dir) 12/14-bit + SENT interface

The RAA2P3500 is developed according to ISO26262 for implementation in safety-relevant systems up to ASIL C. It can also be used in ASIL D system-level requirements according to ASIL Decomposition rules (ISO 26262:2018, Part 9, Clause 5”) or proper risk analysis by the system integrator.

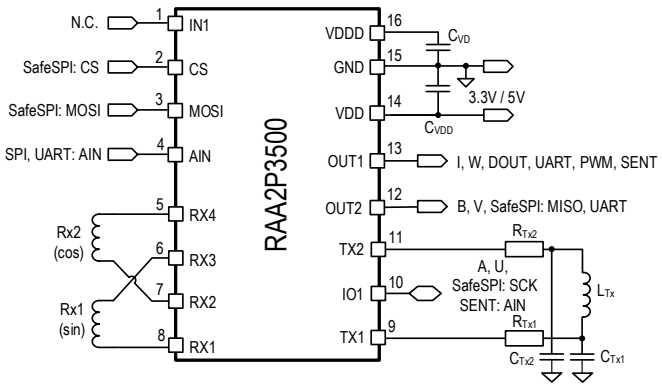


Figure 1. Application circuit example

Features

- Cost-effective; no magnet required
- Immune to magnetic stray fields; no shielding required
- Suitable for harsh environments and extreme temperatures
- Seven user-selectable incremental output modes
- True-power-on position information, obtained by digital interfaces (SafeSPI, UART), PWM/SENT or with ABI with fast incremental start-up burst
- Programmable through UART interface and SafeSPI protocols
- Nonvolatile memory enables multiple programming options
- Single IC supports on-axis and off-axis rotation, linear motion, and arc motion sensing
- Adaptable to any full-scale angle range through coil design
- High accuracy: ≤ 0.1% full scale (with ideal coils), enabling sensor solutions up to 11-bit electrical accuracy
- Overvoltage and reverse polarity protection: ±18 V on both supply and output pins
- Supply voltage programmable for 3.3 V ±0.3 V or 5.0 V±0.5 V
- Qualified for automotive application use from −40°C to +160°C ambient temperature
- 48 bits nonvolatile user ID memory space
- Small 16-TSSOP package (4.4 mm×5.0 mm)

Applications

Rotor position detection for brushless DC motors with digital interfaces, adaptable to any pole pair count.

Available Support

Renesas provides application modules that demonstrate RAA2P3500 rotary position sensing applications.

Contents

Figures

Tables

Terms and Definitions

ABI	ABI quadrature interface
AC	Alternating Current
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
APB	Advanced Peripheral Bus
BLDC	Brushless Direct Current
CDM	Charged-Device Model
CORDIC	Coordinate Rotation Digital Computer
CPHA	SPI Clock Phase
CPOL	SPI Clock Polarity
CS	Chip Select
CRC	Cyclic Redundancy Check

DC	Direct Current
DP	Discontinuity Point
ECU	Electronic Control Unit
EMC	Electromagnetic compatibility
ESD	Electrostatic Discharge
FDM	Failure Detection Mechanisms
FSM	Finite-State Machine
GND	Ground
FSM	Finite State Machine
HK	House Keeping
I/O	Input/Output
I2C	Inter-Integrated Circuit Interface
IC	Integrated Circuit
ID	Identification
LC	Resonant Inductor-Capacitor Circuit
LF	Low Frequency
LPF	Low Pass Filter
LSB	Least Significant Bit
MCU	Micro Controller Unit
MISO	Master In Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Bit
MUX	Multiplexer
NVM	Non-Volatile Memory
OD	Open Drain
PCB	Printed Circuit Board
PP	Push-Pull
RF	Radio Frequency
RX	Receiver
SCL	I2C Clock
SDA	I2C Data
TSSP	Thin Shrink Small Outline Package
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter
UVW	UVW Motor Commutation Interface

1. Pin Assignments and Descriptions

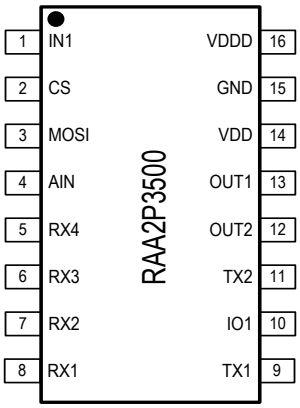


Figure 2. RAA2P3500 pinout

Table 1. Pin description, RAA2P3500

Pin number	Name	Type	Description
1	IN1	Digital Input	SPI: Not used Incremental/UVW: Not used UART: Not used
2	CS		SPI: Chip Select input (active low) Incremental/UVW: Not used UART: Optional address pin strapping input ADR0
3	MOSI		SPI: MOSI Data input Incremental/UVW: Not used UART: Optional address pin strapping input ADR1
4	AIN	Analog Input	Auxiliary analog (12-bit) input for external analog signal, readable over SPI, SENT, and UART interface
5	RX4	Sensor Input	Receiver coil (COS_P)
6	RX3		Receiver coil (SIN_P)
7	RX2		Receiver coil (COS_N)
8	RX1		Receiver coil (SIN_N)
9	TX1	Transmitter Output	Connect the transmitter coil between the TX1 and TX2 pins, using series resistors R_{Tx1} and R_{Tx2}. The resonant frequency is adjusted with capacitors C_{Tx1} and C_{Tx2} from each coil terminal to GND
10	IO1	Digital I/O	SPI: SCK clock input Incremental/UVW: A, Step, U UART: Not used
11	TX2	Transmitter Output	See description of pin #9 (TX1)
12	OUT2	Digital Output	SPI: MISO output Incremental/UVW: B, Direction, V UART: TxD
13	OUT1	Digital I/O	SPI: Digital output Incremental/UVW: Index, W, SENT, PWM UART: Bi-directional TxD/RxD SENT: Data output Single-wire programming interface

Pin number	Name	Type	Description
14	VDD	Supply	External supply voltage (3.3 V or 5 V)
15	GND	Supply	Common ground connection
16	VDDD	Supply	Internally regulated digital supply voltage

2. Specification

2.1 Absolute Maximum Ratings

The absolute maximum ratings listed in Table 2 are stress ratings only. Stresses greater than those listed in Table 2 can cause permanent damage to the device. Functional operation of the RAA2P3500 at the absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions could affect device reliability. All voltage levels refer to GND.

Table 2. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Units
V_{VDDmax}	External supply voltage: VDD	Continuous	-18	18	V
V_{IO1}	Digital Input Pin Voltage				
V_{OUT2}	Digital I/O Pin Voltage				
V_{OUT1}	Analog/Digital Output Pin voltage				
V_{RX1}	Sensor Receiver coil input pin Voltage (RX1)	Continuous	-12	12	V
V_{RX2}	Sensor Receiver coil input pin Voltage (RX2)				
V_{RX3}	Sensor Receiver coil input pin Voltage (RX3)				
V_{RX4}	Sensor Receiver coil input pin Voltage (RX4)				
V_{DIN}	Digital Input Pin Voltage				
V_{ADR0}	Digital Input Pin Voltage				
V_{ADR1}	Digital Input Pin Voltage				
V_{AIN}	Analog Input Pin Voltage				
V_{Tx1}	Transmitter Output pin (TX1) Voltage	Continuous	-0.3	5.5	V
V_{Tx2}	Transmitter Output pin (TX2) Voltage				
$V_{VDDDmax}$	Internal digital supply voltage, VDDD	VDDD is internally regulated with an external capacitor to GND. No other connection to external voltages.	-0.3	2.0	V
T_{AMB}	Ambient temperature		-40	160	ºC
T_J	Junction temperature		-40	170	ºC
T_{STOR}	Storage temperature	Unmounted units must be limited to 10 hours at temperatures above 125°C to prevent pre-aging.	-55	160	ºC
R_{THJA}	Thermal resistance junction to ambient: 16-TSSOP package	Velocity = 0 m/s with 2s2p PCB test board (JEDEC 51-2, JEDEC 51-7)		89.5	K/W
R_{THJC}	Thermal resistance junction to case: 16-TSSOP package	Junction to top of package		38.38	K/W

2.2 ESD Ratings

Table 3. ESD ratings

Symbol	Parameter	Conditions	Max	Units
V_{ESD_OUT}	ESD tolerance for pins with potential external cable connection: ▪ OUT1 ▪ VDD, VSS ▪ Human Body Model: 100 pF / 1.5 kΩ	According to AEC-Q100-002 classification 3A	±4	kV
V_{ESD}	ESD tolerance for all other pins not listed under V_{ESD_OUT} Human Body Model: 100 pF / 1.5 kΩ	According to AEC-Q100-002 classification 2	±2	kV
V_{CDM}	ESD tolerance for all pins: Charged-Device Model (CDM)	According to AEC-Q100-011 classification C2B	±750	V

2.3 Operating Conditions

All Min/Max specification limits are guaranteed by design, production testing, and/or statistical characterization. Conditions: T_{AMB} = −40°C to 160°C unless otherwise specified. C_{VDD} = 470 nF, C_{VDDD} = 100 nF.

Typical values are based on characterization results at default measurement conditions and are informative only.

Table 4. Electrical characteristics, 5 V and 3.3 V modes

Symbol	Parameter	Description	Min	Typ	Max	Units
V_{VDD5}	Supply voltage, 5 V mode		4.5	5.0	5.5	V
$V5_{UV}$	Under-voltage detection level, 5 V mode	An under-voltage alarm is created if VDD falls below this limit	3.95	4.1	4.45	V
$V5_{OV}$	Overvoltage detection level, 5 V mode	An overvoltage alarm is created if VDD rises above this limit	5.55	6.15	6.5	V
V_{VDD3}	Supply voltage, 3.3 V mode		3.0	3.3	3.6	V
$V3_{UV}$	Under-voltage detection level, 3.3 V mode	An under-voltage alarm is created if VDD falls below this limit	2.7	2.8	2.98	V
$V3_{OV}$	Overvoltage detection level, 3.3 V mode	An overvoltage alarm is created if VDD rises above this limit	3.65	3.85	4.04	V
$V_{VDD\_TH\_H}$	Power-on reset (POR), high threshold	Power-on reset (POR): the device is activated when VDD increases above this threshold		2.61	2.7	V
$V_{VDD\_TH\_L}$	Power-on reset (POR), low threshold	The device is deactivated when VDD decreases below this threshold	2.3	2.38		V
$V_{VDD\ POR\_HYST}$	Power-on reset hysteresis		200	250	300	mV
$t_{stup\ PE}$	Start-up times	Power-on reset (POR) to valid output signal, programming enabled			5	ms
$t_{stup\ PL}$		Power-on reset (POR) to valid output signal, programming locked			3	ms
$t_{stup\ cmd}$	Command timeout time	Time to wait before sending first command	1.5			ms

Symbol	Parameter	Description	Min	Typ	Max	Units
t_{ProgEn}	Programming window enable time	Timeout window after POR, in which a first programming enable command must be sent			5	ms
p_{rogun}	Programming window unlock time	Timeout window after programming enable in which a second unlock command must be completely sent (Note 1)			75	ms
V_{VDDD}	Digital supply voltage	Internally regulated. Connect capacitor C_{VDDD} = 100 nF from VDDD to GND.	1.75	1.8	1.85	V
I_{AUXIN}	Auxiliary Input on VDDD maximum external load current	VDDD must be connected to a capacitor C_{VDDD}	0		1	mA
$I_{SHORT\ VDDD}$	VDDD short circuit current limitation		18.5	27	40	mA
I_{CC}	Current consumption	Without coils, no load	10	15	20	mA
C_{VDDD}	Capacitor from VDDD pin to GND		100			nF
C_{VDD}	Capacitor from VDD pin to GND	Nominal value	100	470		nF

Note 1 Device configuration according to the *RAA2P3500 Programming Manual*.

Table 5. Position resolution and update rate

Symbol	Parameter	Description	Min	Typ	Max	Units
RES_{UART}	Position Resolution UART interface			14		
RES_{SPI}	Resolution of calculated position over SafeSPI interface			14		bits
RES_{INC_BIN}	Position Resolution Incremental Interfaces (ABI, Step/Dir)	Binary Mode Counts per 1 coil period (programmable)		512 1024 2048 4096		cpr
RES_{INC_DEC}		Decimal Mode Counts per 1 coil period (programmable)		500 1000 2000 4000		cpr
RES_{PWM}	Position Resolution PWM, SENT Interface		12		14	
Acc (Note 3)	Position Accuracy SPI, UART, ABI (12-Bit), Step-Dir (12-bit), UVW, PWM, SENT	Ambient temperature, nominal supply	−0.1		0.1	%FS
		Over temperature and supply range	−0.2		0.2	%FS
t_{POS}	Position refresh rate	Internal refresh rate of position information	2		3	µs

Note 1 Device configuration according to the *RAA2P3500 Programming Manual*.

Note 2 Accuracy specifications can be further improved with linearization, see Section 4.

Note 3 “% FS” = percent of full scale = accuracy in % per period, where 100% is the angle range of one electrical period. For rotary multi-period designs, one electrical period = 360° (one full turn) divided by the number of periods per turn. For example, a 4-periodic coil design (4 × 90°) has a typical mechanical accuracy of ±0.1% per 90° = ±0.09°

Table 6. Non-volatile memory parameters (Note 1)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Data retention	Qualified according to JEDEC 22-A117	15 at T_J = 100°C			Years
	Over product lifetime		>100 at T_J = 25°C		
Write temperature	Allowed ambient temperature range for read and write access	−40		135	°C
Read temperature		−40		160	ºC
Endurance (Note 2)	Over product lifetime			1000	NVM Write Cycles
Read Cycles		5x 10^{11}	1x 10^{12}		NVM Read events

Note 1 Guaranteed by memory supplier.

Note 2 Verified number of program/erase cycles. Qualified with 2000 cycles.

Table 7. LC oscillator specifications

Symbol	Parameter	Description	Min	Typ	Max	Units
f_{LC}	Excitation frequency	LC oscillator frequency is determined by external components L and C.	2		5.5	MHz
R_{Peq}	Equivalent parallel resistance of the LC resonant circuit		250			Ω
V_{TX_PP}	LC oscillator amplitude at VDD = 5.0 V ±10%	Peak-to-peak voltage; pins TX1 vs. TX2; all modes. Adjustable by coil current.			8.8	Vpp
	LC oscillator amplitude at VDD = 3.3 V ±10%				2* V_{VDD3}	
I_{LC}	Programmable transmitter coil drive current	T_{AMB} = −40 to +160°C	0	Note 1	16	mA
R_{Tx1}, R_{Tx2}	LC oscillator series resistors	Depending on coil design and excitation frequency (f_{LC})		10		Ω

Note 1 The required transmitter coil current is determined by the equivalent parallel resistance of the LC circuit, depending on coil design.

Table 8. Receiver coils front-end specifications

Symbol	Parameter	Description	Min	Typ	Max	Units
V_{RX}	RX coil amplitude	Differential coil input	5		200	mV_{pp}
A_{IN_mm}	Maximum amplitude mismatch correction	Programmable gain mismatch correction of RX coil signals (SIN and COS)			15	%
$A_{IN\_OFFS\_RANGE\%}$	Input offset correction range	Differential input offsets of sine or cosine signal, percentage of transmitter coil amplitude.	−0.2		0.2	%
D_{OFFSET}	Coil input offset temperature drift	Over temperature range T_{AMB}	−2.5		2.5	%
C_{RX1} to C_{RX4}	Receiver input filter capacitors	For improved EMC immunity		220		pF
$Noise_{SP}$		V_{RX} = 50 mV			0.1	° el. rms

Symbol	Parameter	Description	Min	Typ	Max	Units
	Signal path noise level	V_{RX} = 5 mV Device configuration according to the programming manual			0.5	° el. rms

2.4 Interface Pin Characteristics

Table 9. UART interface

Symbol	Parameter	Description	Min	Typ	Max	Units
V_{OL_UART}	Output low voltage	3 mA sink current, VDD = 3.0 to 5.5 V OUT1 pin 13 OUT2 pin 12	0		0.4	V
V_{OH_UART}	Output high voltage	3 mA source current, VDD = 3.0 to 5.5 V OUT1 pin 13 OUT2 pin 12 (Push-Pull condition)	0.8 × VDD		VDD	V
$I_{OUT2\ lim\ thr}$	OUT2 current limitation threshold	OUT2 pin 12	8			mA
$I_{OUT2\ sc\ lim}$	OUT2 output short current limitation (Note 1)	OUT2 pin 12 Short to VDD, GND VDD = 3.0V to 5.5 V Open Drain mode	14		26	mA
$I_{OUT1\ lim\ thr}$	OUT1 current limitation threshold	OUT1 pin 13	35			mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation (Note 2)	OUT1 pin 13 Short to VDD, GND VDD = 3.0 to 5.5 V Push-pull mode	28			mA
$I_{OUT1\ sc\ lim}$	Output short current limitation (Note 2)	OUT1 pin 13 Short to VDD, GND VDD = 3.0 V to 5.5 V Open Drain Mode	28		56	mA
V_{IL_UART}	OUT1 low level input voltage	VDD = 5 V	-0.3		0.2 × VDD	V
		VDD = 3.3 V	-0.3		0.3 × VDD	V
V_{IH_UART}	OUT1 high level input voltage	VDD = 5 V	0.7 × VDD		VDD + 0.3	V
		VDD = 3.3 V	0.7 × VDD		VDD + 0.3	V

Note 1 With OUT2 drive strength set to "00" and OUT2 drive strength for open drain disabled. (out2_io1_drv = "00").

Note 2 With digital mode configuration (out1_drv = "10").

Table 10. SPI interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOL	Output low voltage	3 mA sink current VDD = 3.0 V to 5.5 V OUT2 pin 12	0		0.4	V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOH	Output high voltage	3 mA source current VDD = 3.0 V to 5.5 V OUT2 pin 12	0.8 × VDD		VDD	V
VOH_{SPI3}	Output high voltage	3 mA source current VDD = 3.3 V ±10% SafeSPI mode Pin OUT2	V_{VDD} − 0.4		V_{VDD}	V
$I_{OUT2\ lim\ thr}$	OUT2 current limitation threshold	OUT2 pin 12	8			mA
$I_{OUT2\ sc\ lim}$	OUT2 output short current limitation Note 1	OUT2 pin 12 Short to VDD, GND VDD = 3.0 V to 5.5 V	33		70	mA
t_{rf}	Output rising edge, push/pull mode. MISO (SafeSPI) pin	Load capacitance 60 pF Output voltage rising from 10% to 90%, 5 V			55	ns
t_{rf}	Output falling edge, push/pull mode. MISO (SafeSPI) pin	Load capacitance 60 pF Output voltage falling from 90% to 10%, 5 V			55	ns

Note 1 With OUT2 drive strength set to "00" and OUT2 drive strength for open drain disabled. (out2_io1_drv = "00").

Note 2 With digital mode configuration (out1_drv = "10").

Table 11. PWM interface

Symbol	Parameter	Description	Min	Typ	Max	Units
$I_{IO1\ lim\_thr\ PWM}$	IO1 current limitation threshold	Pin 10 (IO1) in overload condition	6			mA
$I_{IO1\ sc\ lim\ PWM}$	IO1 Output short current limitation (Note 2)	Pin 10 (IO1) Short to VDD/GND VDD = 3.3 V, 5 V	32		70	mA
DC_{PWM}	PWM duty cycle	Normal operation	5.56		94.44	%
DC_{PWM_DHI}	PWM duty cycle	Diagnostic low mode		2.78		%
DC_{PWM_DLO}	PWM duty cycle	Diagnostic high mode		97.24		%
ft_{PWM}	PWM frequency tolerance		−5		5	%
t_{PWM_r}	PWM output rising edge, push-pull mode	Load capacitance 4.7 nF Output voltage rising from 10% to 90% at 5 V			5	us
t_{PWM_f}	PWM output falling edge, push-pull mode	Load capacitance 4.7 nF Output voltage falling from 90% to 10% at 5 V			5	us

Note 1 With digital mode configuration (out1_drv = "10").

Note 2 With OUT2 fast configuration (out2_io1_drv = "11").

Table 12. Incremental interfaces

Symbol	Parameter	Description	Min	Typ	Max	Units
f_{inc}	Single channel Pulse Rate	ABI Step/Dir interfaces			2	MHz

Symbol	Parameter	Description	Min	Typ	Max	Units
V_{OH_inc}	Output high voltage ABI -Step/Dir	3 mA source current, VDD = 3.0 to 5.5 V Pin 13 (OUT1) Pin 12 (OUT2) Pin 10 (IO1)	0		0.4	V
V_{OL_inc}	Output low voltage ABI -Step/Dir	3 mA sink current, VDD = 3.0 to 5.5 V Pin 13 (OUT1) Pin 12 (OUT2) Pin 10 (IO1)	0.8 × VDD		VDD	V
$I_{OUT2\ IO1\ lim\ thr}$	Current limitation threshold A, B/Step, Dir pins	Pin 12 (OUT2) Pin 10 (IO1) in overload condition	6			mA
$I_{OUT2\ IO1\ sc\ lim}$	Output short current limitation (Note 1) A, B/Step, Dir pins	Pin 12 (OUT2) Pin 10 (IO1) Short to VDD/GND VDD = 3.3 V, 5 V	32		70	mA
$I_{OUT1\ lim\ thr}$	Current limitation threshold (Note 1) Index pin	Pin 13 (OUT1) in overload condition	35			mA
$I_{OUT1\ sc\ lim}$	Output short current limitation (Note 1) Index pin	Pin 13 (OUT1) Short to VDD/GND VDD = 3.3 V, 5 V	28		58	mA
t_{r_local}	Output rising edge embedded applications	Load capacitance 60 pF Output voltage rising from 10% to 90% VDD = 3.0 to 5.5 V			55	ns
$t_{f\ local}$	Output falling edge, embedded applications	Load capacitance 60 pF Output voltage falling from 90% to 10% VDD = 3.0 to 5.5 V			55	ns
$t_{r\ remote}$	Output rising edge remote applications	Load capacitance 4.7 nF Output voltage rising from 10% to 90% VDD = 3.0 to 5.5 V			4	µs
$t_{f\ remote}$	Output falling edge remote applications	Load capacitance 4.7 nF Output voltage falling from 90% to 10% VDD = 3.0 to 5.5 V			4	µs

Note 1 With digital mode configuration (out1_drv = "10").

Table 13. SENT interface

Symbol	Parameter	Description	Min	Typ	Max	Units
V_{OL_SENT} (Note 3)	Output low voltage	3 mA sink current, VDD = 4.5 to 5.5 V OUT1 pin 13	0		0.5	V
V_{OH_SENT} (Note 3)	Output high voltage	3 mA source current, VDD = 4.5 to 5.5 V OUT1 pin 13	4.1		5.5	V
$I_{OUT1\ lim\ thr}$	OUT1 current limitation threshold (Note 1)	OUT1 pin 13 in overload condition	55			mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation (Note 1)	OUT1 pin 13 Short to VDD, GND	40		91	mA

Symbol	Parameter	Description	Min	Typ	Max	Units
		VDD = 4.5 to 5.5 V Push-pull mode				
t_{OVL}	Overload shutdown debounce time	Duration of overload condition, before output is shut off		2		ms
$I_{DOUT\ lim\ thr}$	DOUT current limitation threshold (Note 2)	OUT2 pin 12 in overload condition	8			mA
$I_{DOUT\ lim\ thr}$	DOUT output short current limitation (Note 2)	OUT2 pin 12	33		70	mA
C_{input}	Parasitic input capacitance from ESD protection				0.1	nF
I_{SUP} (Note 3)	Average current consumption from Receiver 5 V supply over one message				50	mA
I_{GND} (Note 3)	Average current through Ground line over one message				50	mA
$I_{SUP\ RIPPLE}$ (Note 3)	Peak-to-peak variation in supply current consumption over one message at frequency up 30 kHz				9	mA
T_{Fall} (Note 3)	Falling time, tick time = 3 µs From V_{TH} = 3.8 V to V_{TL} = 1.1 V	$I_{SUP} \le 20$ mA			6.5	µs
		20 mA ≤ I_{SUP} < 50 mA			5	µs
T_{Rise} (Note 3)	Rising time, tick time = 3 µs From V_{TL} = 1.1 V to V_{TH} = 3.8 V				18	µs
ΔT_{Fall} (Note 3)	Edge to Edge Jitter with static environment for any pulse period tick time = 3 µs				0.1	µs
R_{Tau1}	Input filter resistor (first stage)		448	560	672	Ω
C_{Tau1}	Input filter capacitor (first stage)		1.54	2.2	2.86	nF
Tau_1	Input filter time first stage time constant defined by RTau1 and CTau1		0.74		1.73	µs
$R_{PULL-UP}$	Input Pull-up resistor		10		55	kΩ
R_F	Input filter resistor (second stage)		4			kΩ
C_F	Input filter capacitor (second stage)	Determined by TAU2 requirement				nF
R_V	Voltage divider, adjusting SENT output level to MCU input level	Optional, depends on MCU input level				kΩ
Tau_2	Input filter time second stage time constant defined by RV, RF, and CF		0.6		1.4	µs

Note 1 With SENT mode configuration (out1_drv = "11").

Note 2 With out2_io1_drv = "11".

Note 3 Refer to SENT Standard SAE J2716 Standard (Rev. April 2016).

3. Detailed Description

3.1 Overview

The RAA2P3500 sensor IC consists of one transmitter coil and one pair of receiver coils, which are typically designed as traces on a printed circuit board. The receiver coils are designed as two wire loops with anti-serial connection. The “sine” coil and the “cosine” coil are shifted by 90 electrical degrees. A metal target is placed above the coil arrangement.

When the IC drives an AC current into the transmitter coil, it generates an alternating magnetic field. This magnetic field induces secondary voltages in the receiver coils. Without a target, the induced voltages in the loops of the receiver coils cancel each other out, resulting in a net receiver voltage of zero.

When a metal target is placed above the coils, the magnetic field generates eddy currents on its surface. These eddy currents create a counter magnetic field, reducing the total flux density underneath. This leads to a reduction in the voltage induced in the receiver coil areas underneath the target, creating an imbalance in the anti-serial coil segment voltages.

The IC demodulates, offsets, and corrects the amplitude of the signals from the two receiver coils with a 90° electrical phase shift design, which generates sine and cosine shaped voltages as the target is moving.

The RAA2P3500 IC amplifies, rectifies, and filters the receiver voltages, converting them into digital representation with an ADC. The digital sine and cosine signals are converted into a 0°to 360° absolute position. The signal accuracy can be further enhanced through a 2-dimentional,16-point linearization process.

The position can be read over SPI, UART, SENT or Incremental interfaces: ABI, Step-Dir, UVW.

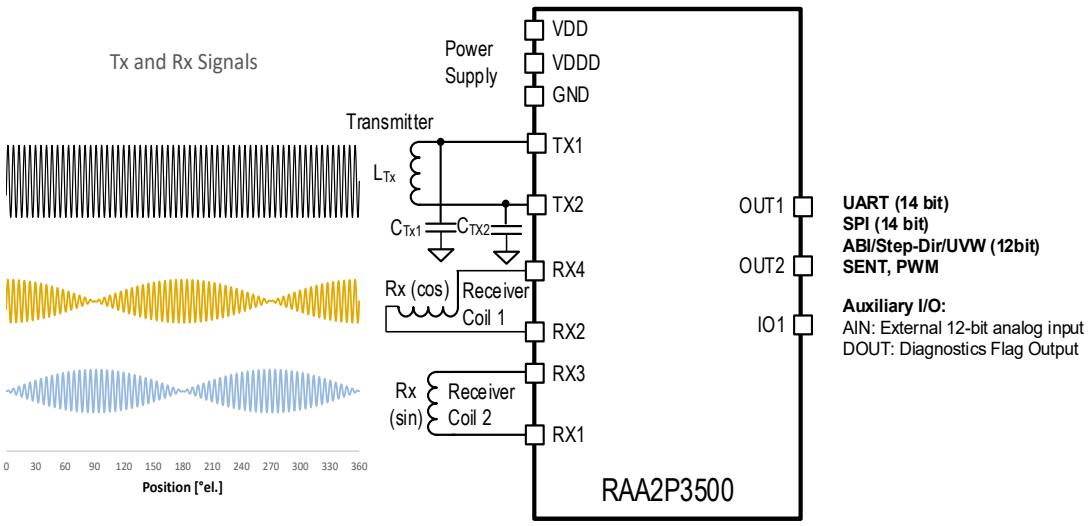


Figure 3. RAA2P3500 input/output signals

3.2 Block Diagram

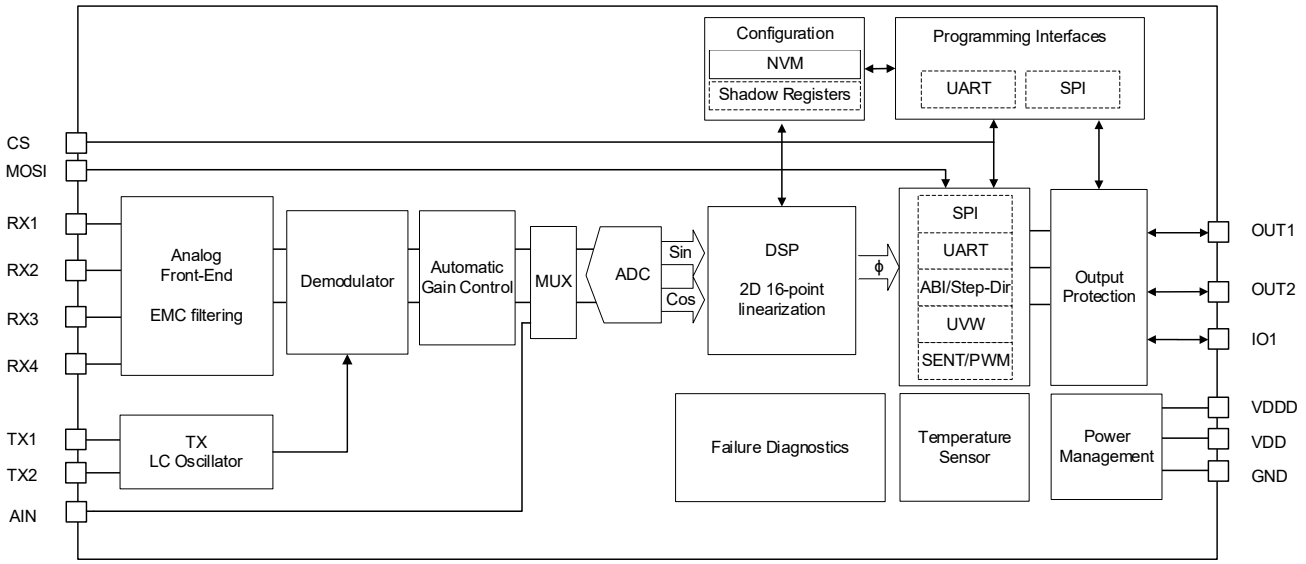


Figure 4. Block diagram

The main building blocks include:

- Analog front-end: Input filter, offset, and gain control for the receiver signals.
- Demodulator: Converting RF modulated position signal to LF demodulated raw sine and cosine signals.
- Automatic Gain Control: Automatically adjusts the raw sine and cosine signal levels.
- High Speed ADC: Converts raw signals into digital format for further digital signal processing.
- Digital signal processing: Conversion of digital sine and cosine raw signals into synchronized absolute position information for both channels.
- 2D 16-point linearization: up to 16 two-dimensional linearization points with freely programmable X- and Y-coordinates for each point (X= Position input, Y= Position output).
- Post processing, clamping, signal integrity checks. Decoding of Channel information and other diagnostics info into the selected output format (SPI, UART, Incremental).
- TX Oscillator: Generation of the transmitter coil signal.
- Temperature sensor: internal temperature sensor, used for chip diagnostics.
- Protection: All outputs are fully protected against overvoltage, reverse polarity, and short circuit, enabling direct connection of a cable to these outputs, eliminating the need for additional line driver ICs.
- Power Management: The chip operates with supply voltages in a wide range from 3.0 to 5.5 V. External capacitors are required for the supply voltage VDD, and an internally regulated digital power supply, VDDD. All other supplies, such as the supply for the analog circuits, do not need any external capacitor.
- Programming interface: via one-wire UART interface or SPI interface.
- Configuration, NVM: Nonvolatile, storage of factory and user-programmable settings. User configuration parameters may be programmed multiple times.
- On-chip diagnostics: Internal diagnosis of critical blocks.
- Auxiliary I/O include, AIN (12-bit analog input for external analog signals), DOUT (Diagnostic Output) accessible over serial interfaces.

3.3 LC Oscillator

The transmitter circuit of the RAA2P3500, generating the required RF magnetic field for operating the sensor is determined by an external parallel LC circuit as shown in the application circuit.

To ensure low emission of harmonics, the capacitive part of the LC circuit is split into two capacitors C_{Tx1} and C_{Tx2} of equal value and two series resistors R_{Tx1} and R_{Tx2} are added as shown Figure 5.

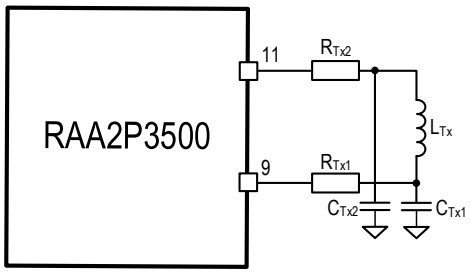


Figure 5. TX LC oscillator

3.3.1 Parallel LC Resonator Calculations

A resonator, comprising an inductor (L) and a capacitor (C) in parallel, is essential for generating specific frequencies in RF applications. Accurate calculations of the equivalent parallel resistance (R-Peq) ensure proper resonator function. In the RAA2P3500 transmitter circuit, this resonator minimizes harmonic emissions.

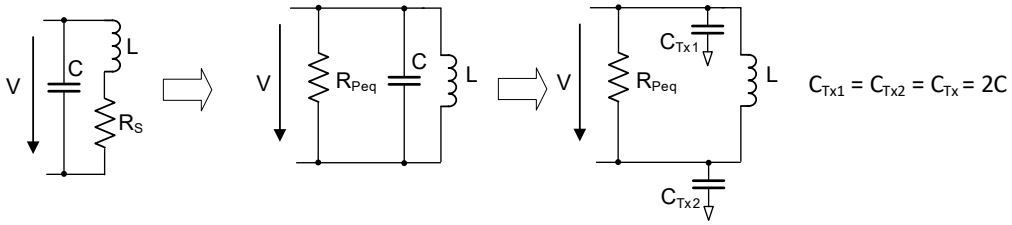


Figure 6. Parallel resonator circuit

Equivalent parallel resistance from Coil series resistance:

$$R_{Peq} = \frac{1}{R_S} \times \frac{L}{C} \tag{1}$$

For $C_{Tx1} = C_{Tx2} = C_{Tx} = 2C$:

$$R_{Peq} = \frac{1}{R_S} \times \frac{2 \times L}{C_{Tx}} \tag{2}$$

Equivalent parallel resistance from Quality factor Q:

$$R_{Peq} = Q \times \sqrt{\frac{L}{C}} = Q \times \sqrt{\frac{2L}{C_{Tx}}} \tag{3}$$

Ideal LC Oscillator frequency with split Tx capacitors C_{Tx}:

$$f_{TX} = \frac{1}{2\pi\sqrt{L\frac{C_{Tx}}{2}}} \tag{4}$$

Oscillator frequency with split Tx capacitor C_{Tx} and coil series resistor R_s:

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{R_S}{L}\right)^2} \tag{5}$$

Oscillator frequency with split Tx capacitor C_{Tx} and equivalent parallel resistor R_{Peq}:

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{2}{R_{Peq}C_{Tx}}\right)^2} \tag{6}$$

Coil quality factor:

$$Q = R_{Peq}\sqrt{\frac{C}{L}} = \frac{1}{R_S}\sqrt{\frac{L}{C}} \quad (7)$$

$$Q = \omega\frac{L}{R_S} = 2\pi f_{TX}\frac{L}{R_S} \quad (8)$$

Where:

- R_{Peq}: Equivalent parallel resistance of the LC circuit at the transmitter frequency in Ohms
- R_S: Serial resistance of the transmitter coil at the transmitter frequency in Ohms
- f_{Tx}: Resonant circuit frequency in Hertz, 1/s
- L: Resonant circuit coil impedance in Henry
- C: Resonant circuit capacitance in Farad
- C_{Tx1}, C_{Tx2}: Capacitance of the split capacitors in Farad
- Q: Resonant circuit quality factor (unitless)
- ω: Angular frequency $2*\pi*f_{Tx}$ in Hertz, 1/s

3.4 Coil Design

Figure 7 shows an example of a linear motion sensor with one transmitter coil (transmitter loop) and two receiver coils (Sin loop and Cos loop). Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

$$\text{VCos Loop1} = \text{-VCos Loop2} \quad (9)$$

If no target is present, the secondary voltages cancel each other:

$$\text{VCos} = \text{VCos Loop1} - \text{VCos Loop2} = 0\ \text{V} \quad (10)$$

With a target placed above the coils, the secondary voltage induced in the covered area is lower than the secondary voltage without a target above it.

$$\text{VCos Loop1} \neq \text{-VCos Loop2} \quad (11)$$

This creates an imbalance of the secondary voltage segments, and thus, a secondary voltage ≠ 0 V is generated, depending on the location of the target.

$$\text{VCos} = \text{VCos Loop1} - \text{VCos Loop2} \neq 0\ \text{V} \quad (12)$$

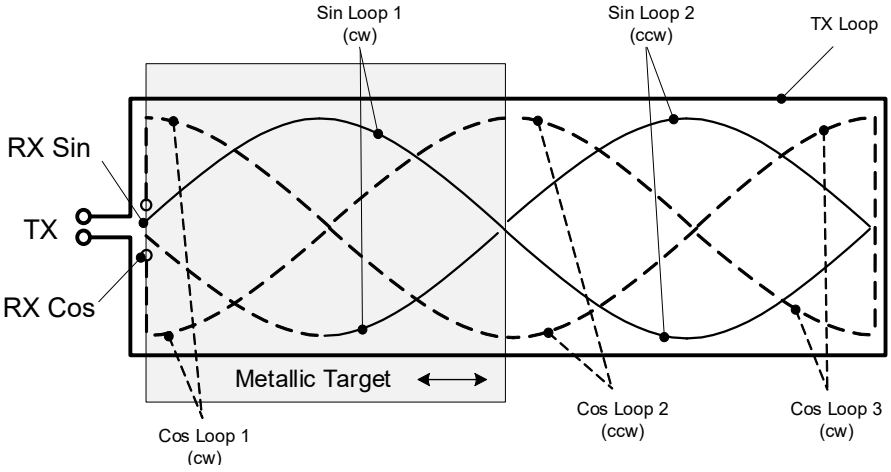


Figure 7. Coil design for a linear motion sensor

The same principles shown for the linear motion sensor can be applied to a rotary sensor as shown in Figure 8.

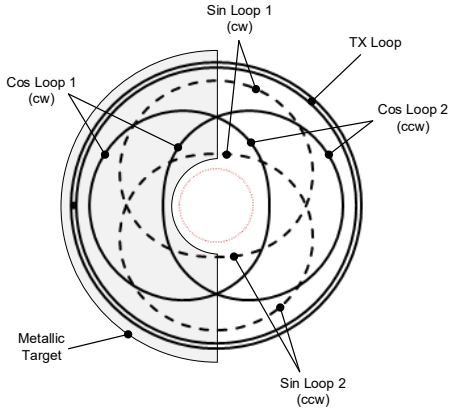


Figure 8. Coil design for a 360° rotary sensor

3.4.1 Multi-Periodic Coil Design Application Examples

Applying the same fundamental design principles, coils with multiple periods per turn can be designed. Multi-periodic designs improve mechanical accuracy compared to single-periodic coil designs. For example, a 4-periodic coil design (4 × 90°) improves mechanical accuracy by a factor of 4. Consequently, for angular designs, requiring < 360° movement range, coil designs with multiple periods are recommended. These designs not only improve mechanical accuracy but are also more robust against mechanical target misalignment and tilt.

3.4.2 Electrical versus Mechanical Degrees

The RAA2P3500 converts the movement of a target across a single period of the receiver coil into a precise electrical signal. This conversion spans the full angular range from 0°to 360°, producing a digital output ranging from 0 to (2^N-1) LSBs. The position output is thus absolute over a full turn of 360 mechanical degrees.
As illustrated in Figure 9, the single-periodic coil design establishes a direct 1:1 relationship between electrical and mechanical domains as the following:

- Coil Period: 360° electrical
- Mechanical Range: 360° mechanical
- Conversion Factor: 1:1 (1°el. = 1° mechanical)

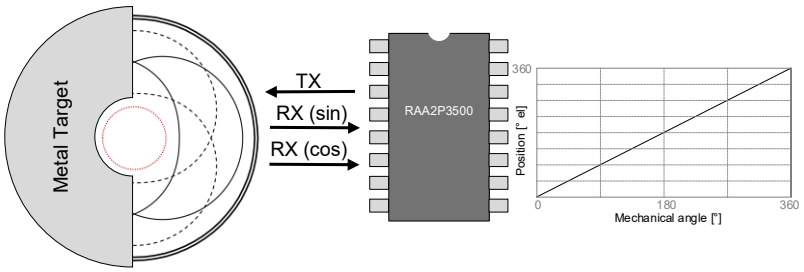


Figure 9. Coil design using 1-periodic coil

As shown in Figure 10, a coil design with four receiver coil periods within a single full mechanical turn, results in four electrical rotations for every complete mechanical turn and provides the following advantages in accuracy and resolution.

Higher Resolution: Position output resolution increases proportionally with period count by:

$$\text{Mechanical Resolution} = \text{Sensors\_Periods} * \text{Electrical Resolution} \quad (13)$$

In this configuration one electrical degree (°el) equals 0.25 mechanical degrees (°). The provided output resolution is four times higher compared to the single-periodic design.

Improved accuracy: Mechanical error is reduced by the period factor.

$$Mechanical\ Error = \frac{Electrical\ Error}{Sensor\ Periods} \quad (14)$$

This configuration is particularly well-suited for:

- Multi-pole motors requiring precise commutation
- Limited-range applications (<180° mechanical travel)
- Systems demanding high-resolution incremental feedback

Select the number of periods based on application requirements to optimize measurement performance. Proper period selection is critical for achieving maximum system accuracy.

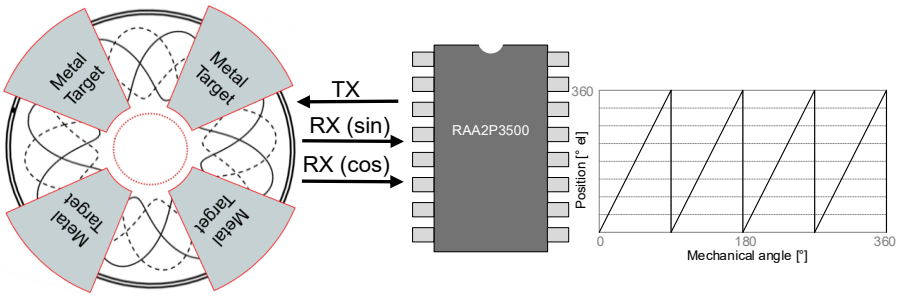


Figure 10. Coil design using 4-periodic coil

4. Linearization

The RAA2P3500 offers a very flexible linearization feature to enhance sensor accuracy. The linearization algorithm is applied digitally after an angle calculation. The linearization is performed with 12-bits resolution over a 360° electrical range (el.). Up to 16 programmable linearization points can be positioned within a grid of 0.088° in both X (position) and Y (expected output) directions.

Figure 11 shows an example of the impact of linearization, showing that the total error is significantly reduced.

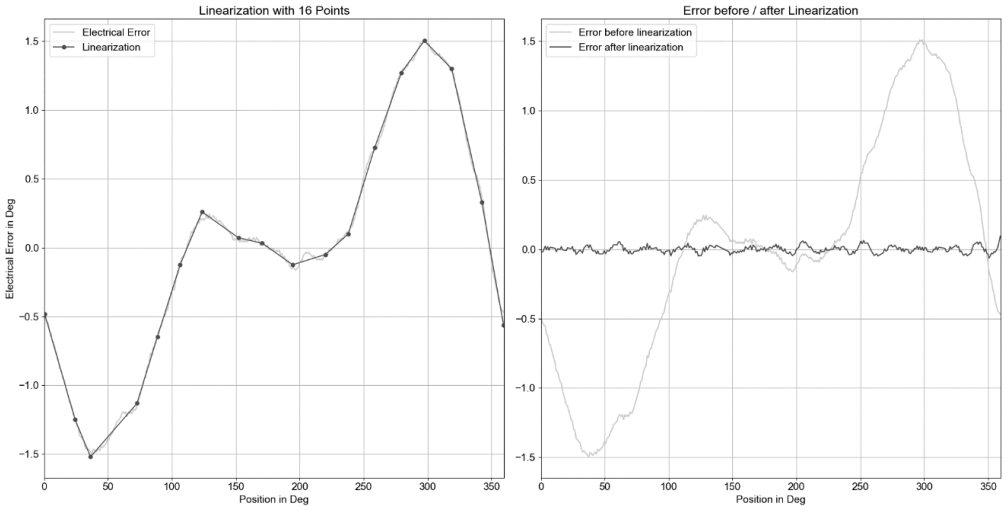


Figure 11. Example of 16-point linearization

Table 14. Linearization parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
N_{P_Lin}	Number of linearization points				16	
$Grid_{LIN}$	Placement grid of linearization points	In X and Y		0.088		°el
Res_{Lin}	Resolution of linearization transfer function	X and Y coordinates		12		bits

Note 1 The slope of each segment (ΔY/ΔX) is automatically calculated from the X and Y parameters of adjacent linearization points. If two adjacent points are positioned with a slope outside the specified range (see Table 14), the slope is reset to 0 to prevent an overflow of the calculated slope value.

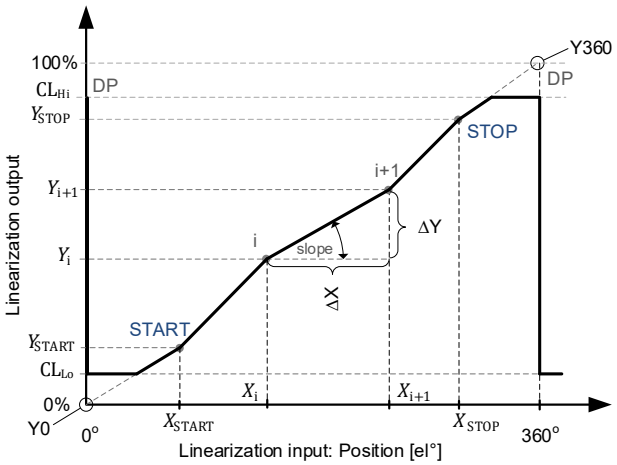


Figure 12. Linearization transfer function parameters

Table 15. Linearization parameter settings

Parameter	Description	Programming options	Resolution
P_{Lin}	Number of linearization options	0,2,4,6,8,16	
D_P	Discontinuity point, zero position transition from 0°/360°	0° to <360° el.	0.088°el. per LSB
X_{Start}	Mechanical start position, first linearization point		
Y_{Start}	Expected output at XStart, first linearization point		
X_i	Mechanical position of linearization point (i = 1 to 16, including start and stop)		
Y_i	Expected output at linearization point (i = 1 to 16 including start and stop)		
X_{Stop}	Mechanical end position, last linearization point		
Y_{Stop}	Expected output at XStop, last linearization point		
CL_{Hi}	Output Clamping level, high	0% to 100% VDD	12 bits (VDD/4096) per LSB
CL_{Lo}	Output Clamping level, low		
Y0	Position at DP, start value at X = 0°	0°/360° el.	
Y360	Position at DP, stop value at X = 360°	0°/360° el.	

5. Interfaces

The RAA2P3500 offers SafeSPI, UART, ABI/Step-Dir, and SENT. A summary of the maximum speed for each high-speed interface is shown in Table 16.

Table 16. Interfaces overview

Interface	Number of I/f wires	Resolution	Features	Other options
SafeSPI	4	14 bits	Interface Speed: 10 MHz Fastest Position Update rate: 3.9 µs	Analog Input (pin 4)
UART	1 or 2	14 bits	Interface Speed: 2 MHz Fastest Position update rate: 15 µs	Analog Input (pin 4)
UVW	3	6 - 48 counts per period	600 krpm	1-8 programmable pole pairs per period
ABI	3	9-12	max. edge rate = 8 MHz: speed ≤600 krpm at 9 bit 468 krpm at 10 bit 234 krpm at 11 bit 117 krpm at 12 bit	Binary and decimal based resolutions Analog Input (pin 4) (SENT)
AB + PWM				
AB + SENT				
Step/Direction + Index				
Step/Direction + PWM				
Step/Direction + SENT				

5.1 SafeSPI Interface

The SafeSPI Serial Peripheral Interface for Automotive Safety is an open standard based on the de-facto Serial Peripheral Interface (SPI) industry standard. RAA2P3500 was developed according to SafeSPI specification ver. 1.0. Further details can be found at: https://safespi.org.

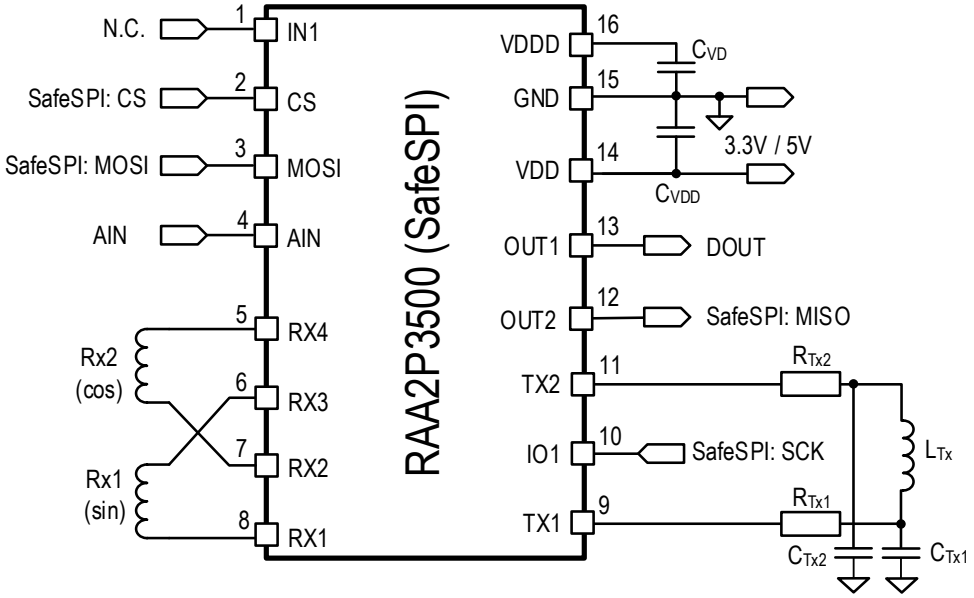


Figure 13. Safe SPI – input/output pins

The RAA2P3500 supports the following features:

- Command frame according to SafeSPI standard.
- Out-Of-Frame communication protocol.
- Data read is frozen/latched on the rising edge of CS.
- Multi-slave configuration with dedicated chip selects.
- 32-bit frame format, 16-bit data per frame.
- Frame starts with MSB first.
- Supports Burst Write mode.
- Programmable Clock phase CPHA
- Programmable Clock polarity CPOL
- Operation on both 3.0–3.3 V (as specified in SafeSPI standard) and 4.5 V–5.5 V supply voltage.

Data transfer over the SafeSPI interface is controlled by the Chip Select (CS) signal. While the CS signal is at high level, incoming data is not accepted at the data input MOSI (Master-Out-Slave-In) and the data output MISO (Master-In-Slave-Out) remains in high impedance state.

A low signal at the Chip Select signal (CS) activates the SafeSPI interface. Data can be transferred from the SafeSPI Master to the SafeSPI Slave and vice versa. The Serial Clock (SCK) represents the master clock signal. This clock determines the data transfer speed. All receiving and sending data is synchronized with this clock.

Commands are transmitted from the master to the slave through the MOSI line and the SPI Slave returns its response through the MISO line. See Figure 14 for diagrams.

5.1.1 Timing Specifications

Table 17. SafeSPI output user programming options

SafeSPI interface programming parameter	Number of options	Programming option
SCK Clock polarity: CPOL	2	0: clock which idles at 0, and each cycle consists of a pulse of 1

SafeSPI interface programming parameter	Number of options	Programming option
		1: clock which idles at 1, and each cycle consists of a pulse of 0.
SCK Clock phase: CPHA	2	0: Output data is latched on the trailing edge of the preceding clock cycle, while the input data captures the data on the leading edge of the clock cycle. 1: Output data is latched on the leading edge of the preceding clock cycle, while the input data captures the data on the trailing edge of the clock cycle.

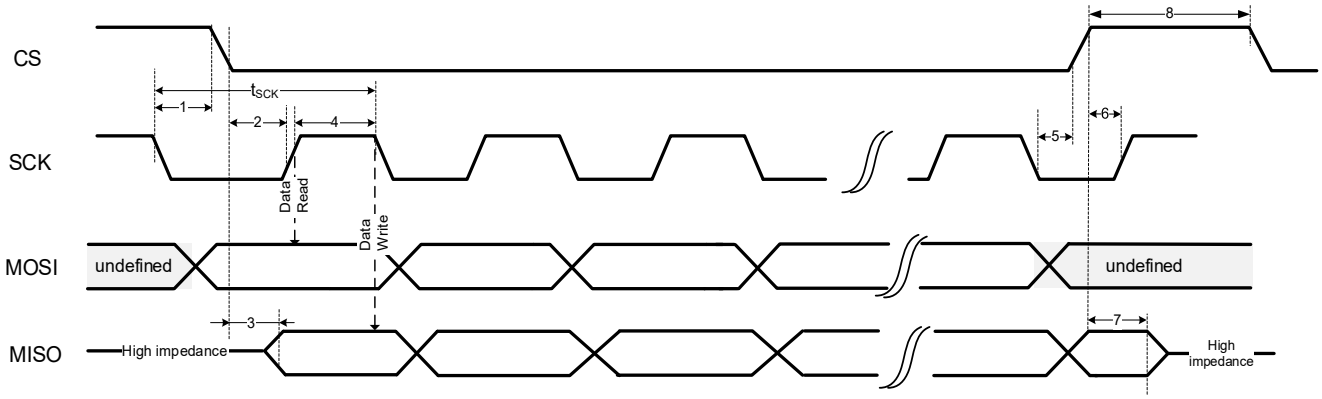


Figure 14. Safe SPI timing diagram for mode 0 (CPOL = 0; CPHA = 0)

The incoming data is received by a rising edge and transmitted by a falling edge of clock signal SCK.

For CPOL and CPHA parameters, see Table 17.

The incoming data is received on the rising edge and transmitted on the falling edge of the clock signal SCK.

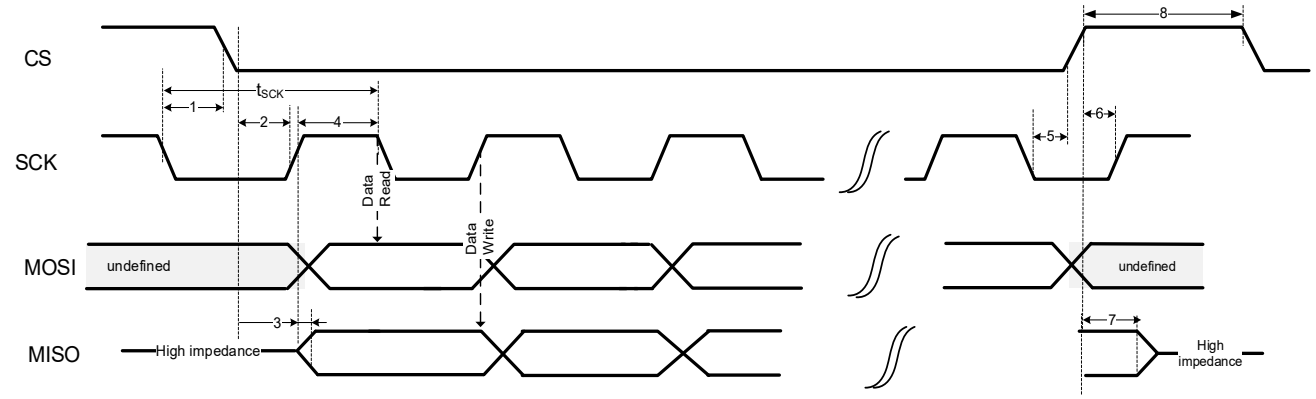


Figure 15. Safe SPI timing diagram for mode 0 (CPOL = 0; CPHA = 1)

The incoming data is received by a falling edge and transmitted by a rising edge of clock signal SCK.

For CPOL and CPHA parameters, see Table 17.

Table 18. SafeSPI timing requirements

Symbol		Parameter	Min	Typ	Max	Units
1	$t_{sck\_dis\_lo}$	SCK disable lead time, time between the falling edge of SCK and falling edge of CS	10			ns
2	$t_{sck\_en\_hi}$	SCK enable lead time, time between the falling edge of CS and rising edge of SCK	40			ns
3	$t_{MISO\_valid\_lo}$	MISO data valid time, time between the falling edge of CS and the start of MISO operation			40	ns
4	t_{SCK_hi}	SCK high time, time between rising edge and falling edge of SCK	40			ns

Symbol		Parameter	Min	Typ	Max	Units
5	$t_{SCK\_en\_lo}$	SCK enable lag time, time between the falling edge of SCK and rising edge of CS	20			ns
6	$t_{SCK\_dis\_hi}$	SCK disable lag time, time between the rising edge of CS and rising edge of SCK	10			ns
7	t_{MISO_dis}	MISO data disable lag time, time between the rising edge of CS and disabling of MISO data			50	ns
8	t_{CS_hi}	Sequential transfer delay	700			ns
f_{SCK}		SCK clock frequency		10	12.5	MHz
n_{Fps}		Frame rate (32-bit frame + t_{CS_hi})		256.4	306.7	kFrames/second

5.1.2 SafeSPI Frame

5.1.2.1 SafeSPI Out-of-Frame Logical Layer

The Out-of-Frame communication protocol ensures simultaneous data reading and command broadcasting in parallel. The response from the SafeSPI slave (the RAA2P3500) is always synchronized with the subsequent command frame of the Master.

For example, while the Master transmits Command #2 over the MOSI line, it simultaneously receives the response from Command #1 over the MISO line.

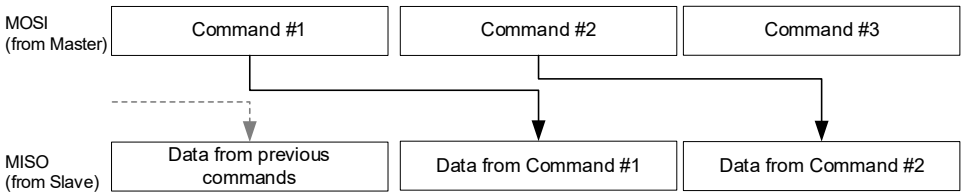


Figure 16. Out-of-frame communication

5.1.2.2 SafeSPI Protocol

The SafeSPI data frame consists of 32 bits. MSB is transmitted first.

5.1.2.3 SafeSPI Master Commands

The master initiates communication over the MOSI line. The interface supports various read and write operations determined by a 3-bit command field as the following:

- Sensor Read (0b000): reads the linearized, speed compensated 14-bit position.
- Read from register (0b001): specifies the register address to read from, see Table 20 for examples.
- Write to register (0b010): two frames are required for register write: the first frame contains the address, and the second frame contains the data to be written to that address.
- Write Burst to registers (0b011): performs a sequence of write commands on contiguous registers.

Table 19. SafeSPI commands

Command [2:0]	SafeSPI command
0b000	Sensor Read (Position)
0b001	Read from Register/Set Address
0b010	Write Register
0b011	Burst Write
0b1xx	Undefined (error)

5.1.2.4 SafeSPI Response Slave to Master

Response sequence by the Slave over the MISO line is the following:

- D: 1-bit data identifier, which defines whether the response contains sensor data (D= 1) or not (D=0).
- SA: 10-bit Slave Address uniquely identifying the content of the response data (Sensor Data [15:0]). Only the 3 MSBs are used in the RAA2P3500, the remaining 7 bits are not assigned (N/A).
- S1: status bit (S1, MSB) indicating the status of the sensor, see Table 21.
- Data [15:0]: 16 bits of data, which can be either sensor data (identified by D=1) or other data (identified by D=0), as requested in the previous frame. See Table 20 for examples.
- S0: the second status bit (S0, LSB) indicating the status of the sensor, see Table 21 for status descriptions.
- CRC: 3-bit cyclic redundancy check.

Table 20 shows an abstract of the main registers that are accessible through the SafeSPI interface. A comprehensive list of all accessible registers is provided in *RAA2P3500 Programming Manual*, available on request from Renesas Electronics.

5.1.2.5 Sensor Read

With Sensor Data Read, you can obtain the 14-bit compensated position information by transmitting two 32-bit SafeSPI frames. When the D bit is set to 1 (indicating Sensor Data), the sensor's response is received on the MISO output during the second frame, as shown in Figure 18.

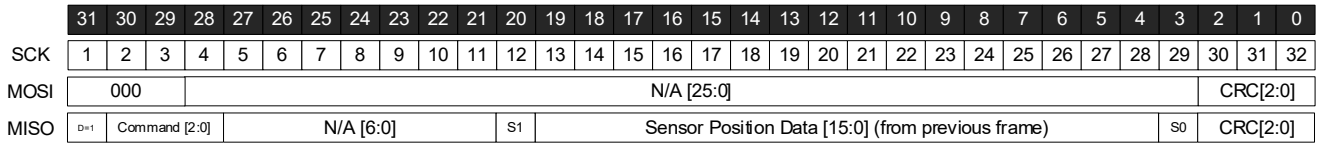


Figure 17. SafeSPI frame for reading sensor data

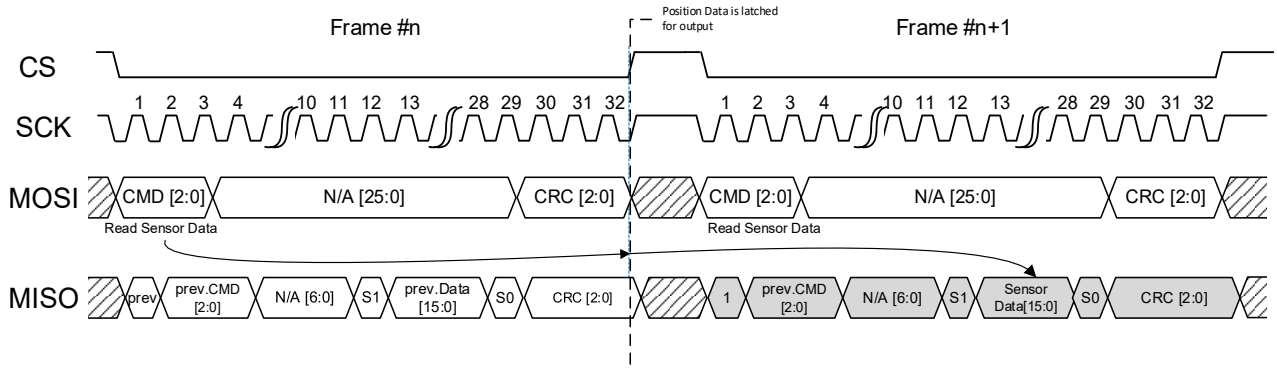


Figure 18. SafeSPI signal diagram for reading sensor data (CPHA = 0)

5.1.2.6 Register Data Read

Register Data Read allows users to access internal register information using two 32-bit SafeSPI frames. When the D bit is set to 0 (indicating Register Read), the sensor's response is received on the MISO output during the second frame, as shown in Figure 20. The available registers are listed in Table 20.

Table 20. SafeSPI available register data

Address	Type of data	Length [bits]	R/W	Note
0x0276	Raw Position Data	16	R	Raw Position after angle calculation
0x026A	Linearized position	14	R	Position after angle calculation + linearization
0x026E	Speed compensated position	14	R	Position after angle calculation + linearization + speed compensation (correction of speed related propagation delay) This register is also read by the “read sensor” command

Address	Type of data	Length [bits]	R/W	Note
0x02A2	Interpolated Position	14	R	Position after angle calculation + linearization + speed compensation (correction of speed related propagation delay) + position interpolation
0x0282	Turns counter	12	R	±2048 turns; increments/decrements at every zero-crossing of the position data. Counter is reset after Power-on-reset
0x0286	Chip internal temperature	8	R	Internal temperature sensor, measuring the junction temperature of the chip
0x0296	Analog input	13	R	Voltage at pin AIN
0x0298	VDDD voltage	13	R	Measurement of the VDDD reference voltage, for external temperature measurement using an NTC
0x0270	Signal magnitude	14	R	Magnitude of input signal: sqrt (V_{sin}^2 + V_{cos}^2)
0x027A	Sine raw data	13+1	R	Raw data of sine coil inputs after AGC + inversion bit
0x027C	Cosine raw data	13+1	R	Raw data of cosine coil inputs after AGC + inversion bit
0x029E	DOUT FLAG output	1	R/W	Control of digital FLG output by writing 0/1 into a register
0x0264	Customer ID 0	16	R	Customer ID information
0x0266	Customer ID 1	16	R	Customer ID information
0x0268	Customer ID 2	16	R	Customer ID information

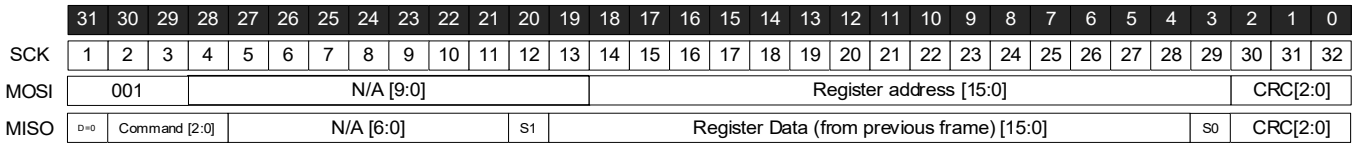


Figure 19. SafeSPI frame for reading register data

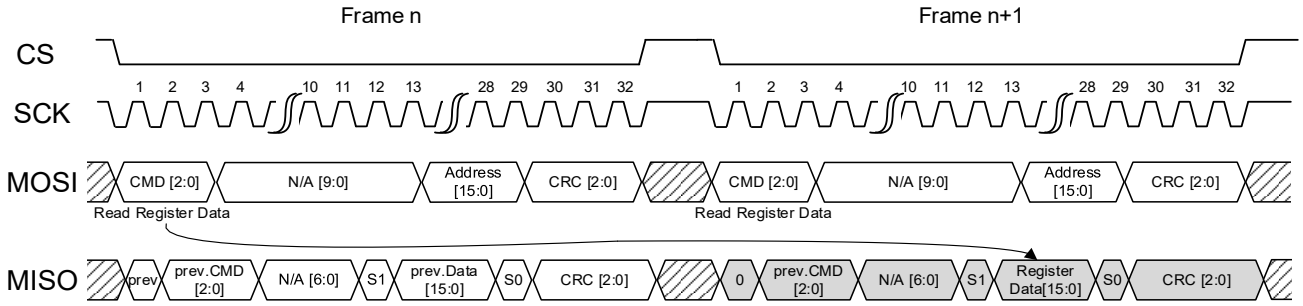


Figure 20. SafeSPI signal diagram for reading register data (CPHA = 0)

5.1.2.7 Register Data Write

The Register Data Write function allows users to write on internal registers using two 32-bit SafeSPI frames. When the D bit is set to 0, the first frame includes the address, and the second frame contains the data, as shown in Figure 22.

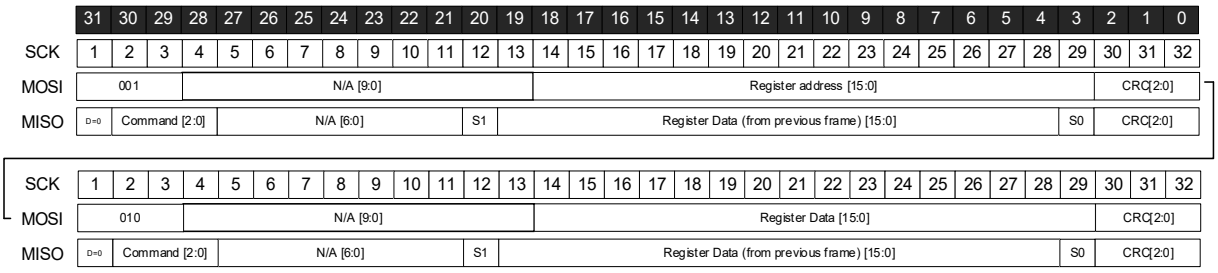


Figure 21. SafeSPI frame for writing register data

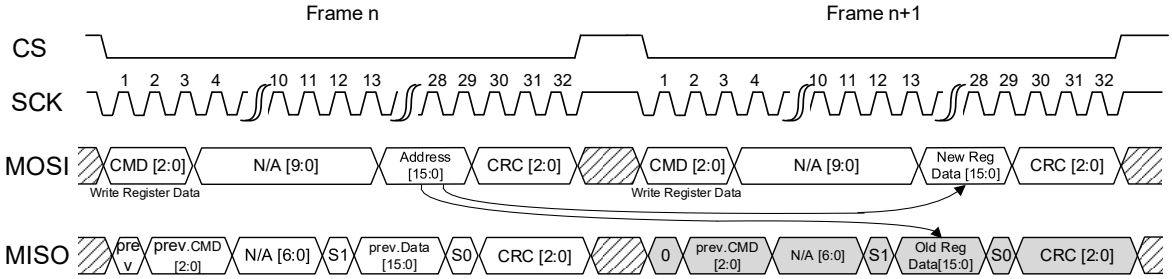


Figure 22. SafeSPI signal diagram for writing register data (CPHA = 0)

5.1.2.8 Register Data Burst Write

The RAA2P3500 supports Burst Write mode, which facilitates rapid consecutive register writes. In this mode, the register address automatically increments with each frame, allowing the master to efficiently write data to the memory.

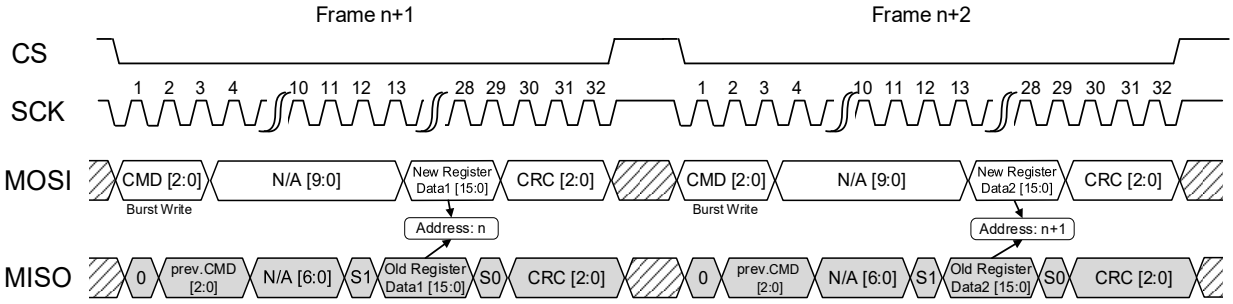


Figure 23. SafeSPI signal diagram for burst writing register data (CPHA = 0)

Table 21. SafeSPI status bit indication

Status bit S1	Status bit S0	Status indication
0	0	Valid sensor data
0	1	Sensor is in error state
1	0	Sensor is in programming mode
1	1	Sensor is in initialization state. Data [15:0] still contains data

5.1.2.9 CRC Protection

The Cyclic Redundancy Check (CRC) is calculated over bits 31:3 using the polynomial of $x^3 + x + 1$ (binary 1011). The initial value is set to 0xb101, and value is 0xb000. For more information, see *RAA2P3500 Programming Manual*.

5.2 Incremental Interfaces

The RAA2P3500 includes incremental and BLDC motor commutation interfaces such as ABI, Step/Direction, and UVW, making it ideal for replacing optical and magnetic encoders in industrial applications. All incremental interfaces utilize three channels on OUT1, OUT2 and IO1 pins, as shown in Figure 24.

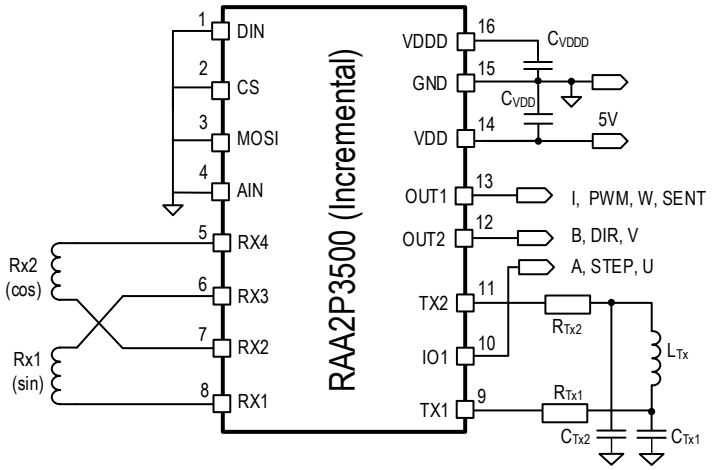


Figure 24. Incremental interfaces input/output pins

Table 22. Incremental interfaces user programming options

Parameter		Number of options	Programming options	
Incremental mode		7	ABI, AB+PWM, AB+SENT, Step/Direction+Index, Step/Direction+PWM, Step/Direction+SENT, UVW	
Index pulse length		2	For ABI and Step/Direction mode: 1 LSB, 3 LSBs	
Index position		4	For ABI and Step/Direction mode	
Interpolation factors	Base	12	Binary	Decimal
	Pulses per period [el.]		128/256/512/1024	125/250/500/1000
	Counts per period [el.]		512/1024/2048/4096	500/1000/2000/4000
UVW pulses per period [el.]		8	1, 2, 3, 4, 5, 6, 7, 8	
Startup counter burst mode		5	Burst generator enabled/disabled If enabled: Frequency of startup burst generator	
Startup counter wait time		4	If enabled: Wait time for burst generator after POR	
Delay compensation		2	Enable/Disable	

5.2.1 ABI Interface

The ABI interface uses two quadrature channels, A and B, which toggle with a 50% duty cycle. The I (Index) signal provides a pulse once per revolution, marking the zero-angle position. Each cycle of channels A and B generates four unique states.

Counting up or down occurs at each edge of channels A and B, resulting in four count increments or decrements per pulse. Consequently, the number of counts per period is four times the number of pulses per period. The counting direction of the receiving counter depends on the state of the channels at each edge (see Figure 25). In clockwise rotation, a rising edge of channel A occurs when channel B is low, whereas in counterclockwise rotation, the rising edge of channel A occurs when channel B is high.

The RAA2P3500 device also allows for programmable reversal of rotational direction, enabling easy adaptation to different requirements.

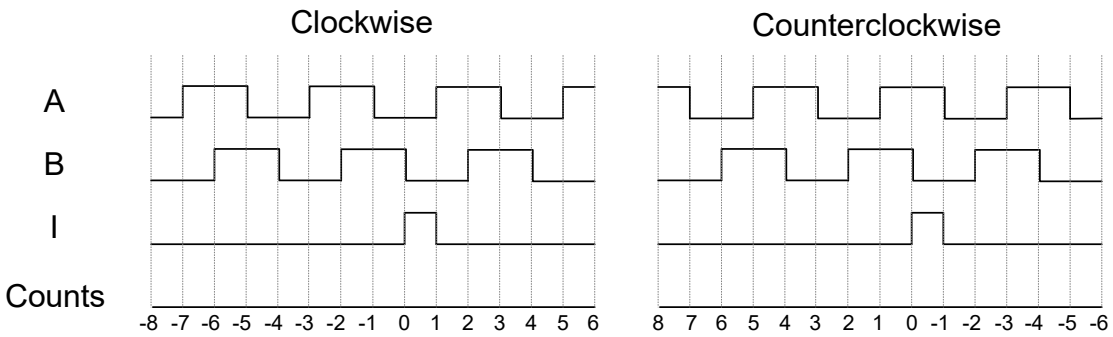


Figure 25. ABI protocol

5.2.2 Step/Direction

The RAA2P3500 can be configured for the Step/Direction protocol. In this protocol, one pin (Step) delivers one pulse per count, while the other (Direction) is held high or low to indicate the rotational direction. As a result, the Step pin outputs double the number of pulses compared to A pin in ABI mode.

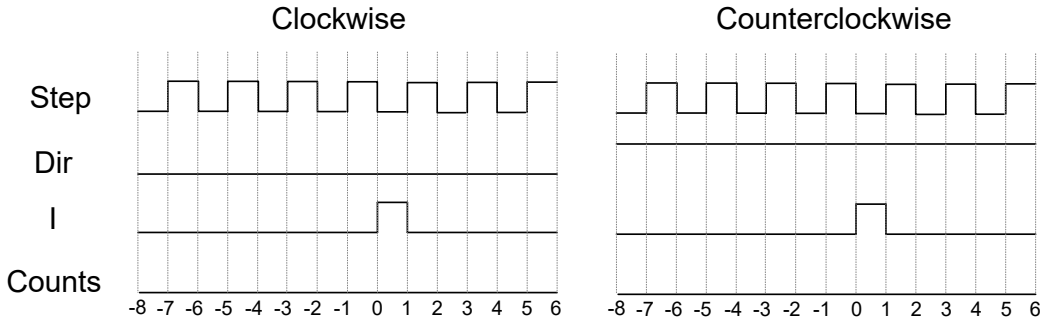


Figure 26. Step/Direction protocol

5.2.3 UVW Motor Commutation Interface

The UVW interface is designed to replace the simple block commutation scheme used in brushless DC motors that employ three discrete magnetic switches. It works as an incremental interface, providing three channels with one pulse per period, each channel phase shifted by 120° electrically (see Figure 27).
In normal operation, this interface can exhibit six states. The two states that do not occur during normal operation are UVW = 000 and UVW = 111. These two states are reserved for diagnostic indication.

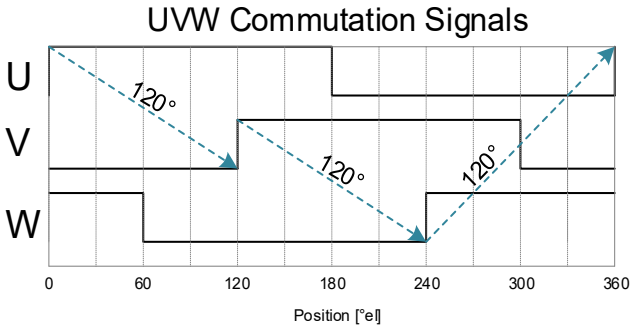


Figure 27. UVW decoding scheme within one electrical period

The sequence of three-phase shifted UVW signals appears once per electrical phase of the e-motor. For motors with n-pole-pairs, the sequence repeats n times per mechanical turn. The number of UVW pulses per electrical period is programmable from 1 to 8.
Multi-periodic coil designs offer flexibility to match the number of pole pairs on the motor with an equivalent number of periods in the coil design. For example, a four-pole pair motor can be matched with the following:

- a four periodic coil design with 1 UVW pulse per period
- a one periodic coil design with 4 UVW pulses per period

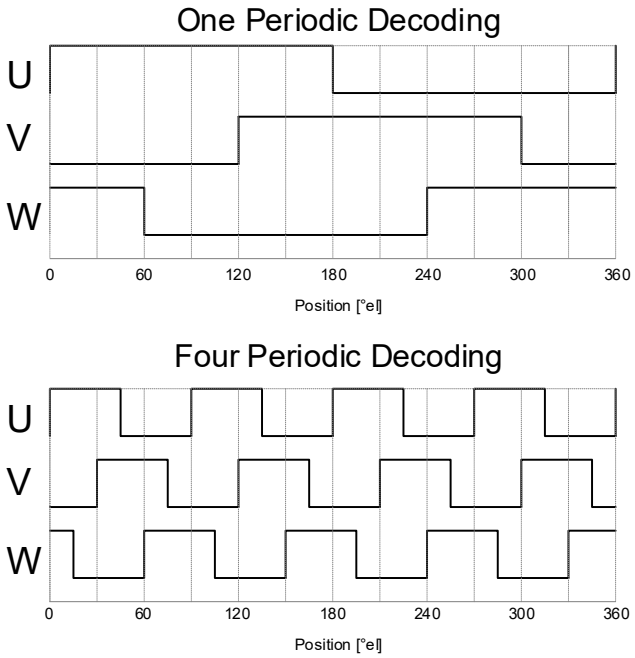


Figure 28. Decoding examples for 1 and 4 pulses per period

5.2.4 Interpolation Factor/Resolution

The incremental interfaces for the RAA2P3500 device offer four interpolation settings (9-bit,10-bit,11-bit,12-bit) in both binary and decimal formats. The interpolation factor is the number of counts per electrical period. "Pulses per period" denote the pulses generated on one channel during a single electrical period (360° el.). These settings determine the counts per electrical period, which must be multiplied by the number of primary coil periods to get the total counts per mechanical period.

5.2.5 Maximum Speed

The maximum rotation speed is defined by the maximum output pulse rate at channels A and B, which is 2 MHz. Additionally, the maximum rotation speed is influenced by the interpolator resolution and the number of pole pairs of the coil. In addition, the maximum rotation speed is constrained by the maximum input frequency, which is 10 kHz (600 000 rpm) as shown in Table 23.

Table 23. Maximum speed

Interpolation factor, resolution	Maximum counts per revolution	Maximum electrical speed [rpm]	Maximum pulse rate, outputs A and B	Maximum edge rate
9-bit	512	600 000	2 MHz	8 MHz
10-bit	1024	468 000		
11-bit	2048	234 000		
12-bit	4096	117 000		

For UVW mode, the interpolation factor must be set to 12-bit, offering a maximum speed of up to 117 krpm (both electrical and mechanical), regardless of the pole pair (pulses per period) setting as shown in Table 24.

Table 24. UVW maximum speed

Pulses per period	Maximum electrical and mechanical speed	Maximum pulse rate, outputs U, W and W
1	117 000 rpm	1.95 kHz
2		3.9 kHz
3		5.85 kHz
4		7.8 kHz
5		9.75 kHz

Pulses per period	Maximum electrical and mechanical speed	Maximum pulse rate, outputs U, W and W
6		11.7 kHz
7		13.65 kHz
8		15.6 kHz

Note 1 Note: the maximum mechanical speed is determined by dividing the maximum electrical speed by the number of periods per turn for the specific coil design. For example, a coil design with 5 periods and 10-bit interpolation has a maximum speed of 468 krpm/5 = 93600 rpm.

5.2.6 Index Pulse

Encoders' incremental interfaces send an index pulse to indicate their zero position. The receiver uses this pulse to synchronize and subsequently utilizes the A/B and Step/Direction signals to track of the position accurately. To support a variety of receivers, this pulse is programmable in both width and position.
Two programmable options are available for the index pulse width: either a duration of 1 count or 3 counts. Additionally, there are four programmable options for the index pulse position (index_cfg). Each configuration defines the resulting diagnostic state as described in Table 25.

Table 25. ABI index configurations

Index pulse position	ABI Diagnostic state	Step/Direction Diagnostic state
A = 0, B = 0	A = 1, B = 1, I = 1	Step = 1, Dir = X , I = 1
A = 1, B = 1	A = 0, B = 0, I = 1	Step = 0, Dir = X , I = 1
A = 0, B = 1	A = 0, B = 0, I = 1	Step = 1, Dir = X , I = 1
A = 1. B = 0	A = 0, B = 1, I = 1	Step = 0, Dir = X, I = 1

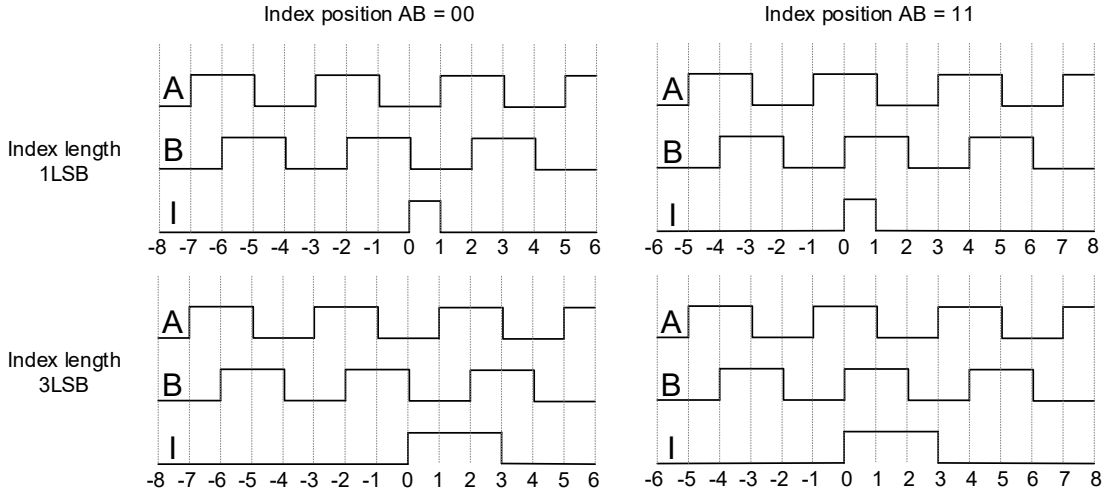


Figure 29. ABI index position and length configurations

The index configuration defines the diagnostic state indication. The unique combination of the three signals in diagnostic mode ensures that it does not occur during normal operation.

5.2.7 True-Power-On Absolute Position Information

Incremental interfaces lack the capability to deliver absolute position information immediately upon power-up.

At power-up, the absolute position remains unknown if the measured object, such as a motor, is stationary. Motion is required to detect the first index and calculate the position accurately.

RAA2P3500 can calculate the absolute position internally and provides it over the incremental interface after power-up, before any rotation starts. This is implemented by sending an artificial burst of pulses. (see Figure 30).

After a programmable wait time, an index pulse is generated to reset the external counter at the receiving end, followed by a series of AB pulses that indicate the absolute position. The frequency of this pulse train is programmable, ensuring synchronization of the counter at the receiving end with the correct absolute position.

The rotor must remain stationary during the initial pulse train sequence. This feature can be enabled or disabled by user programming.

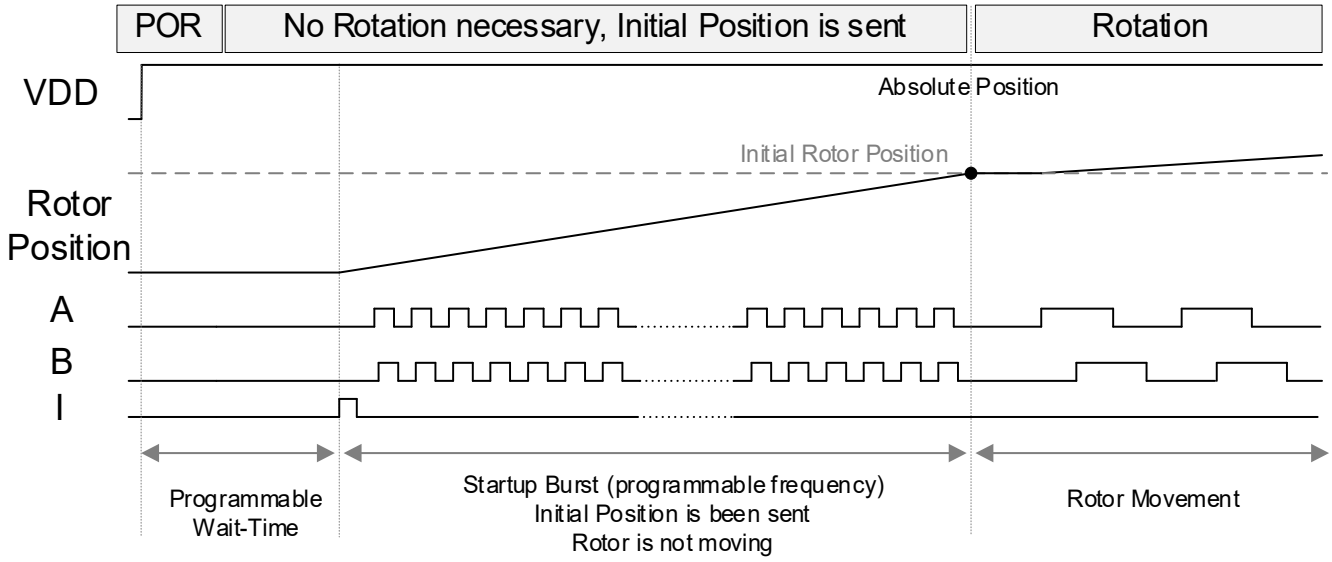


Figure 30. ABI true-power-on burst delivering absolute position at startup without rotation

5.2.7.1 True Power-On with AB + PWM Mode

In AB+PWM mode, the index output is replaced with a PWM output, allowing users to determine the exact position during start-up based on the PWM output. Once the measured object begins to move, the position can be calculated from the pulses of the A and B outputs. The PWM signal is available in a wide frequency range, see Table 29 for details.

5.2.7.2 True Power-On with SD + PWM Mode

In addition to the AB+PWM mode, a 3-wire mode with Step/Direction, and PWM is available. This versatile setup ensures precise position control and flexibility in various applications.

5.2.7.3 True Power-on with AB + SENT Mode

In this 3-wire mode, the index output is replaced by a SENT output. The absolute position at start-up can be read from the SENT output. When the measured object is moving, the position is obtained from the pulses of the A and B outputs, and the status information can be read independently from the SENT output.

5.2.7.4 True Power-on with SD + SENT Mode

Like the AB+SENT mode as described in section 5.2.7.3, a 3-wire mode with Step + Direction + SENT is available.

5.2.8 Incremental Output Programming Options

Table 26, Table 27, and Table 28 summarize the user programmable options for the various incremental output options of the RAA2P3500.

Table 26. Incremental interface user programming options

Incremental interface programming parameter		Number of options	Programming options	
Incremental mode		7	ABI, AB+PWM, AB+SENT, Step/Direction + Index, S/D+PWM, S/D + SENT, UVW	
Index pulse width		2	1/3 LSB	
Index position		4	Index pulse at: A=B=00/A=B=11	
	Base:	12	Binary	Decimal

Incremental interface programming parameter		Number of options	Programming options	
Interpolation factors:	Pulses per period [el.]		128/256/512/1024	125/250/500/1000
	Counts per period [el.]		512/1024/2048/4096	500/1000/2000/4000
UVW pulses per period [el.]		8	1/2/3/4/5/6/7/8	
Delay compensation		2	Enable/Disable	

Table 27. PWM output user programming options (for AB+PWM and Step/Direction + PWM modes)

PWM interface programming parameter	Number of options	Programming option
PWM frequency	7	100/200/500/1000/1500/3000/4000 Hz
PWM output mode	2	Push-pull/Open-drain
PWM polarity	2	Low/High
PWM resolution	2	12 -bit (all PWM frequencies)/14-bit (PWM frequencies from 100-1000 Hz)

Table 28. SENT output user programming options (for AB+SENT and Step/Direction + SENT modes)

SENT programming parameter	Number of options	Programming option
SENT tick time	1024	0.02 to 16 µs
SENT fast channel frame	8	Selection of fast channel frame formats
SENT pause pulse	3	No pause, fixed length pauses, constant frame length
Serial message protocol	3	Disabled, 16 or 32 messages (see *RAA2P45xx Datasheet* for further details)
CRC calculation method	2	As defined by SENT Standard SAE-J2716, Apr2016: “recommended” or “legacy” calculation method

5.3 PWM interface (AB + PWM, Step/Direction + PWM)

The PWM interface can be used in combination with the incremental A + B or Step/Direction outputs to provide the absolute position, replacing the Index output. It can either be configured as push-pull or open drain output on pin 13 as shown in Figure 31. The PWM interface can be configured for push/pull or open drain output.

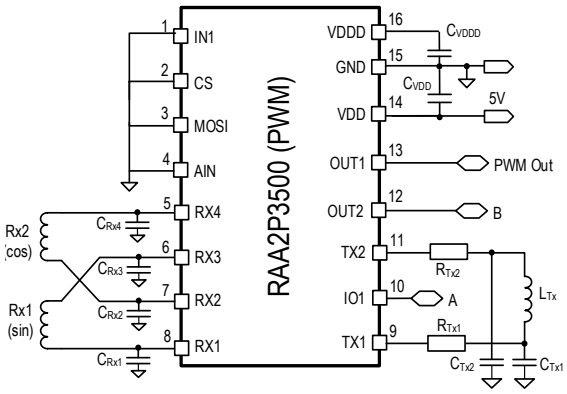


Figure 31. AB + PWM configuration

Table 29. PWM interface user programming options

Incremental interface programming parameter	Number of options	Programming option
PWM frequency	8	109, 219, 547, 1094, 1641, 2188, 3282, or 4376 Hz
PWM output mode	2	Push-pull or open-drain
PWM polarity	2	Position information is either active low or active high
PWM resolution	2	12 -bit (all PWM frequencies) or 14-bit (PWM frequencies from 109-1094 Hz)
Diagnostic mode indicated by PWM signal	3	Disabled Diagnostic mode enabled with low duty cycle Diagnostic mode enabled with high duty cycle

The 12-bit PWM signal frame is composed of a 256 LSB high level header, followed by the 12-bit Position Data ranging from 0 to 4095 LSBs. This is marked by a high-level section and a corresponding low-level section ensuring a total of 4095 LSBs. The frame concludes with a 256 LSB low-level trailer as shown in Figure 32.

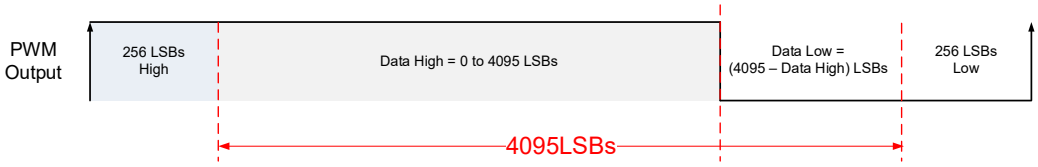


Figure 32. 12-bit PWM signal in normal operation

The minimum 12-bit duty cycle can be calculated with Position data = 0 LSB High, 4095 LSBs low:

$$DC_{min} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{256}{256 + (4095 + 256)} = 5.557\% \quad (15)$$

The maximum 12-bit duty cycle can be calculated with Position data = 4096 LSBs High, 0 LSBs low:

$$DC_{max} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{256 + 4095}{(256 + 4095) + 256} = 94.443\% \quad (16)$$

The 14-bit PWM signal frame shown in Figure 33 is structured similarly as the 12-bit PWM signal frame shown in Figure 32, with the key difference being an increased resolution by a factor of 4.

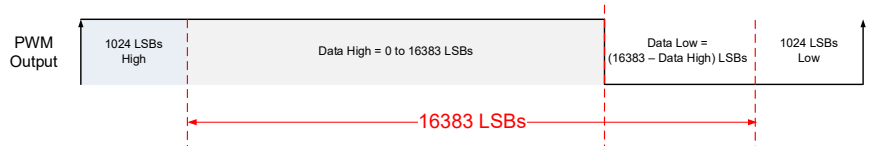


Figure 33. 14-bit PWM signal in normal operation

The minimum 14-bit duty cycle can be calculated with Position data = 0 LSB High, 16383 LSBs low:

$$DC_{min} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{1024}{1024 + (16383 + 1024)} = 5.556\% \quad (17)$$

The maximum 14-bit duty cycle can be calculated with Position data = 16384 LSBs High, 0 LSBs low:

$$DC_{max} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{1024 + 16383}{(1024 + 16383) + 1024} = 94.44\% \quad (18)$$

5.3.1 PWM Diagnostics Mode

In PWM Diagnostics mode, the duty cycle is forced to a range normally not given in normal operation. This mode can be configured for:

- Diagnostic low mode, see Figure 34 and Figure 36
- Diagnostic high mode, see Figure 35 and Figure 37

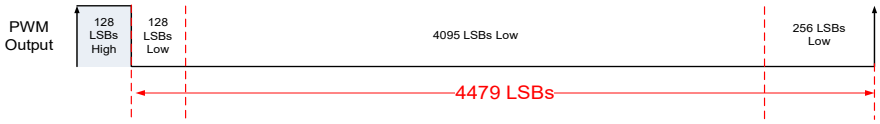


Figure 34. 12-bit PWM signal in Diagnostic low mode

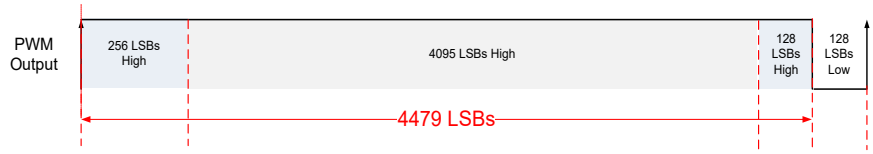


Figure 35. 12-bit PWM signal in Diagnostic high mode

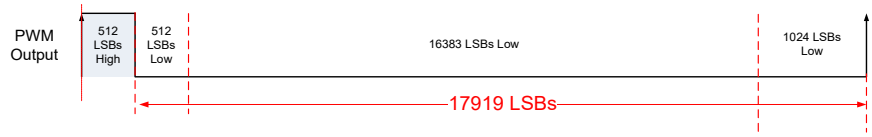


Figure 36. 14-bit PWM signal in Diagnostic low mode

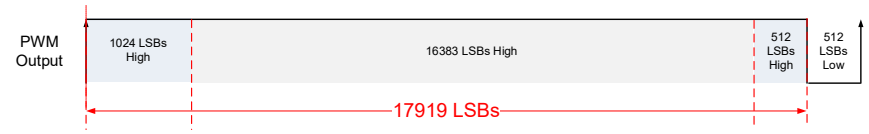


Figure 37. 14-bit PWM signal in Diagnostic high mode

5.4 SENT Interface (AB + SENT, Step/Direction + SENT)

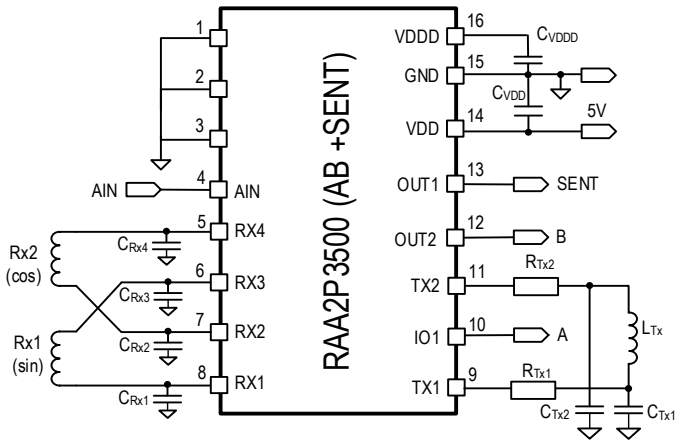


Figure 38. SENT interface input/output pins

The sensor is equipped with a SENT interface compliant with SAE J2716 Standard (Rev. April 2016). The key features are:

- Configurable tick time (1.5 µs, 3 µs, 6 µs with pulse shaping output, down to 0.1 µs with push-pull output).
- Configurable pause pulse.
- Support Enhanced Serial message with 8-bits ID and 12-bits data.
- Eight different fast channel configurations.
- Serial message cycle length is selectable between 16 or 32 messages.
- Signal shaping for reduced EMI.

Table 30. SENT interface user programming options

SENT programming parameter	Number of options	Programming option
SENT tick time	1024	0.02 to 16 µs Note: <1.5 µs tick time in push-pull mode only
SENT fast channel frame	8	see Table 33
SENT pause pulse	3	No pause, fixed length pauses, Constant frame length, see Table 32
Serial message protocol	3	Disabled, 16 or 32 messages (see Table 34 and Table 35)
CRC calculation method	2	As defined by SENT Standard SAE-J2716, Apr2016: “recommended” or “legacy” calculation method

5.4.1 SENT Protocol Frame

The SENT protocol frame consists of a fixed-length synch pulse (LOW period of 5 ticks followed by a HIGH period of 51 ticks), followed by a status nibble, 6 data nibbles, and a CRC nibble. An optional pause pulse can be programmed to adjust the SENT frame to a fixed length of 270 ticks.

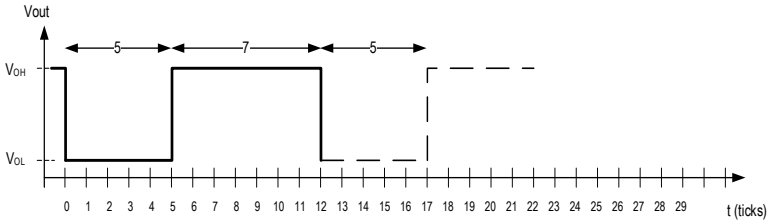


Figure 39. SENT nibble output for value = 0_{DEC}

For transmitting a nibble with the 0 value, 12 clock ticks are required: a fixed LOW period of 5 ticks followed by a HIGH period of 7 ticks.

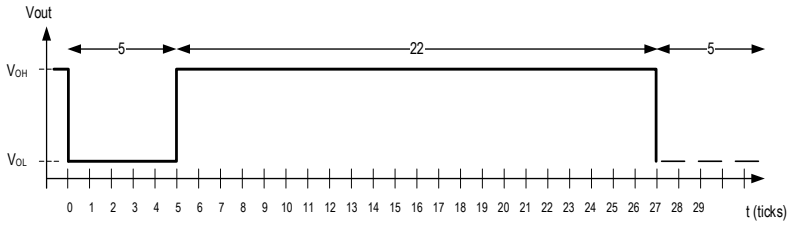


Figure 40. SENT nibble output for value = 15_{DEC}

For transmitting a nibble with the value 15_{DEC} (1111_{BIN}, F_{HEX}), 27 clock ticks are required: a fixed LOW period of 5 ticks followed by a HIGH period of 22 ticks.

The total time for one nibble can be calculated as with the following equation:

$$t_{NIBBLE} = t_{TICK}*(12 + x) \quad (19)$$

Where:

- x = the nibble decimal value = 0 to 15.
- t_{TICK} = the length of one tick, which is programmable.

Table 31. SENT tick counts

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Number of ticks	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27

The tick time can be programmed in a wide range from 0.02 to 16 µs, see Table 30.

Table 32 lists examples for the most common tick times, 1.5 µs, 3.0 µs, and 6.0 µs.

Table 32. SENT Tick time programming options

SENT tick time t_{TICK}	SENT frame length without pause pulse		SENT frame length with pause pulse (programmable)	
	Total frame length (min 154 ticks)	Total frame length (max 270 ticks)	Constant frame minimum = 282 ticks	Constant frame maximum = 922 ticks
1.5 µs	231 µs	405 µs	423 µs	1383 µs
3.0 µs	462 µs	810 µs	846 µs	2766 µs
6.0 µs	924 µs	1620 µs	1692 µs	5532 µs

5.4.1.1 Operation and Frame Format

The SENT transmitter controller supports both fast channel message and serial message formats.

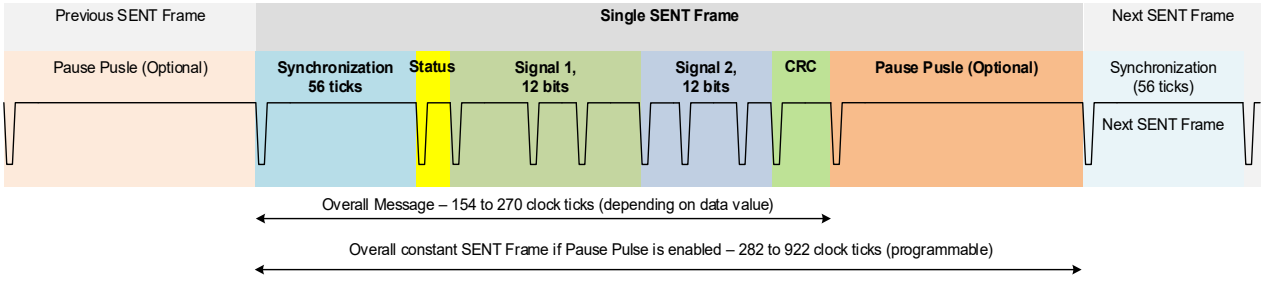


Figure 41. SENT typical frame

Several fast channel modes are available, combining primary and analog inputs with turns counter (Table 33).

Table 33. SENT fast channel frame options

SENT fast channel frame									
Nibble #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**SAE J2716 reference:**
Programming Option:	Status	Signal 1 (12-bit)			Signal 2 (12-bit)			CRC	
Option 0: Secure Angle Sensor	Status	12-bit MSB position data (Receiver coils) MSN → LSN			8-bit rolling counter		4-bit inverted MSB	CRC	H.4: 12+8+4 bits
Option 1: Dual Throttle Sensor		12-bit MSB position data (Receiver coils) MSN → LSN			12-bit analog input LSN → MSN				H.1: 12+12 bits
Option 2: Dual Throttle Sensor		14-bit MSB position data MSN → LSN			10-bit analog input LSN → MSN				14+10 bits
Option 5: Position (14bit) + turns counter (10LSBs)		14-bit position data (Receiver coils) MSN → LSN			10 LSBs turns counter (Receiver coils) LSN → MSN				H.6: 14+10 bits

Note 1 The internally calculated resolution is always 14 bits at 360°. For options 0 and 1, where 12-bits position data are selected, the 12 MSBs of the 14-bit position data are transmitted.

Note 2 Turns counter functionality counts the number of electrical periods that have been detected on the receiver coils. This information is decoded in a 12-bit register and stored in an internal register also SENT.

Note 3 The status nibble bits S[3:2] contain the enhanced serial message and are constat zero if the enhanced serial message is disabled. S[0] contains the temporary diagnostic state of the IC. S[1] is zero.

5.4.1.2 Enhanced Serial Message

The enhanced serial protocol message format consists of an 8-bit ID and 12-bit data with 6-bit CRC per frame. In addition, two sets of serial protocol messages are programmable: 16 frames or 32 frames.

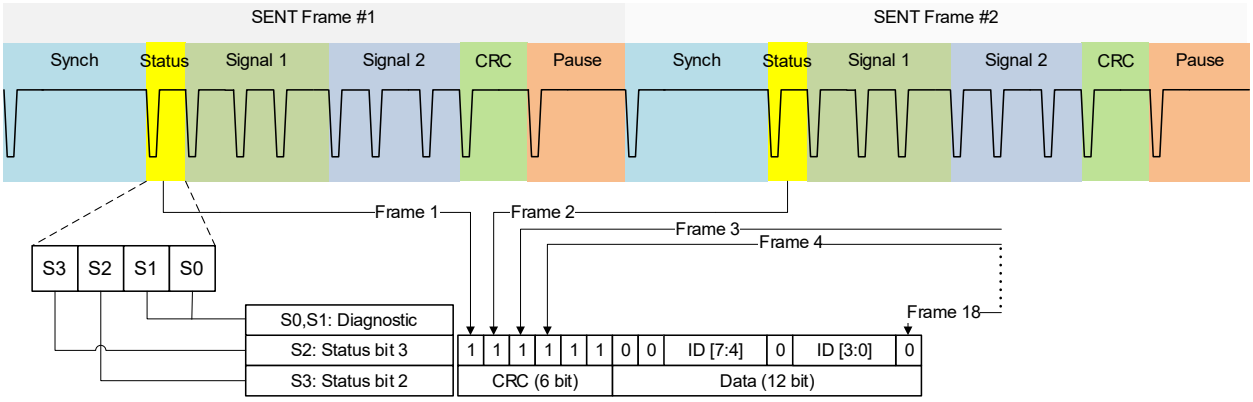


Figure 42. Enhanced serial protocol message format

Table 34. SENT 12-bit enhanced serial protocol data (data frames 1 - 16)

Frame #	ID (8-bit)	Description	Source data (12-bit)
1	01 Hex	Diagnostic Status 1	Mapped to internal status registers: irq_sts0[11:0]
2	03 Hex	Ch1, Ch 2 sensor type	Sensor type according to SENT specification: cust_id2[15:8]
3	05 Hex	Manufacturer Code	Manufacturer Code for RENESAS
4	06 Hex	SENT Standard Revision	04 = SENT Revision 4 J2716 APR2016
5	83 Hex	Diagnostic Status 2	Mapped to internal status registers: irq_sts0[15:12], irq_sts1[7:0]
6	23 Hex	Chip temperature	Internal temperature register: chip_temp
7	29 Hex	Sensor ID #1	USER_ID0: cust_id0[11:0]
8	2A Hex	Sensor ID #2	USER_ID1: cust_id1[7:0], USER_ID0: cust_id0[15:12]
9	84 Hex	Diagnostic Status 3	Mapped to internal status registers irq_sts2[3:0], irq_sts1[15:8]
10	90 Hex	OEM ID #1	Product ID [7:0] bits: prod_id
11	88 Hex	ADC raw SIN data	Rx Coil's ADC raw sine data, 11MSBs out of 13-bits and bit denoting inversion adc_raw_sin[13:2]
12	16 Hex	Turns Counter	12-bit Turns counter angle1_turns
13	85 Hex	Diagnostic Status 4	Mapped to internal status registers: irq_sts2[15:4]
14	80 Hex	Reserved	Reserved
15	81 Hex	Reserved	Reserved
16	89 Hex	ADC raw COS data	Rx Coil's ADC raw cosine data, 11MSBs out of 13-bits and bit denoting inversion adc_raw_cos[13:2]

Table 35. SENT 12-bit enhanced serial protocol data (data frames 17-32)

Frame #	ID (8-bit)	Description	Source data (12-bit)
17	86 Hex	Diagnostic Status 5	Mapped to internal status registers irq_sts3[11:0]
18	17 Hex	Reserved	Reserved
19	10 Hex	Reserved	Reserved

Frame #	ID (8-bit)	Description	Source data (12-bit)
20	12 Hex	AGC setting	Coil AGC: angle1_gain
21	87 Hex	Diagnostic Status 6	Mapped to internal status registers: irq_sts3[15:12]
22	1C Hex	Analog Input	Analog input, 12 MSBs out of 13-bits: adc_hk_ana_in[12:1]
23	1D Hex	Analog reference voltage (VDDD)	Analog input reference (VDDD) 12 MSBs out of 13-bits: adc_hk_vdda_ref[12:1]
24	18 Hex	Reserved	Reserved
25	01 Hex	Diagnostic Status 1	Mapped to internal status registers: irq_sts0[11:0]
26	91 Hex	OEM ID#2	0x632 (ASCII coded “RA”)
27	2B Hex	Sensor ID #3	cust_id2[3:0], cust_id1[15:8]
28	2C Hex	Sensor ID #4	cust_id2[7:4]
29	82 Hex	Reserved	Reserved
30	92 Hex	OEM ID#3 (optional)	0x4A1 (ASCII coded “A2”)
31	93 Hex	OEM ID#4 (optional)	0x430 (ASCII coded “P0”)
32	94 Hex	OEM ID#5 (optional)	0x410 (ASCII coded "00")

5.4.2 SENT Load Circuits

Load circuit components are shown in Figure 43 for the legacy SENT interface and Figure 44 for the recommended SENT interface. All components are specified according to specification SAE J2716 – APR2016, see With digital mode configuration (out1_drv = "10").
Table 13.

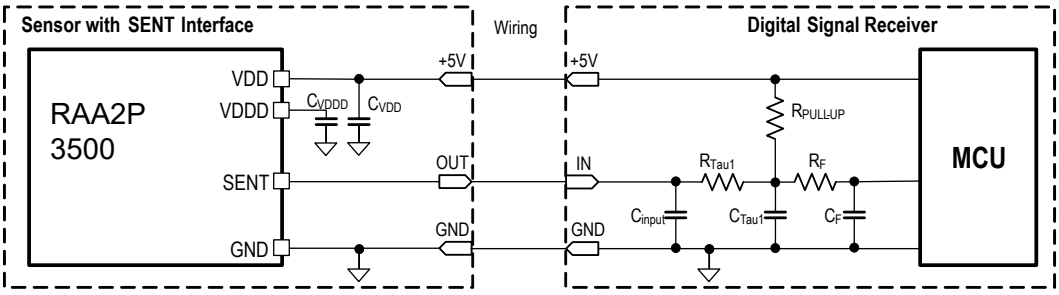


Figure 43. Legacy SENT interface load circuit

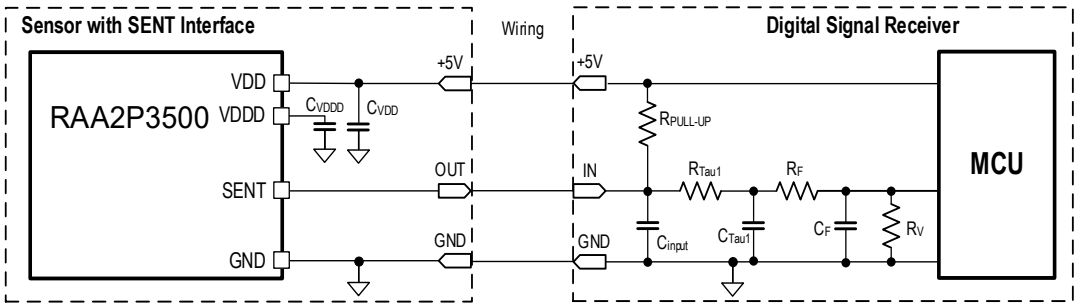


Figure 44. Recommended SENT interface load circuit

5.5 High Speed UART interface

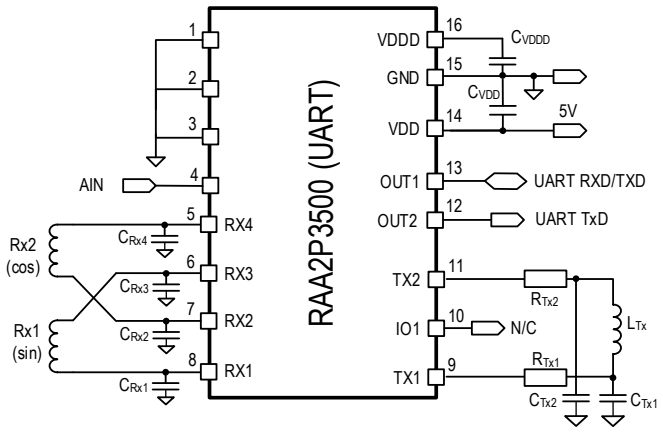


Figure 36. UART interface with input/output pins

The UART interface is utilized as a one-wire programming interface and serves as primary back-end interface in the following modes:

- single wire bidirectional
- dual wire unidirectional
- dual wire differential bidirectional

NOTE
All UART modes operate in half duplex data transmission.

Table 37. UART operating modes

Operating mode	OUT1 (Pin 13)	OUT2 (Pin 12)
Single-Wire Bidirectional	RxD/TxD	Not Used
Dual-Wire Unidirectional	RxD	TxD
Dual-Wire Differential Bidirectional	RxD/TxD complementary	TxD

Table 38. UART interface user programming options

UART programming parameter	Number of options	Programming option
UART output drive	2	Open drain or push-pull
UART slave address	4	2 LSBs of general slave address
UART Baud rate (Note 1)	6	{9600, 57600, 115200, 230400,1M,2M} bit/s
UART operation mode	3	Single wire bidirectional Dual wire unidirectional Dual wire differential bidirectional
UART error warnings	7	Baud rate, framing, CRC errors

Note 1 Maximum data rate may be reduced by external capacitive and resistive loads when open drain configuration is used.

5.5.1 Single Wire Bidirectional UART

In Single Wire UART mode the device communicates with the ECU using only OUT1 pin which could be configured in push-pull or open drain mode. This mode can be used in a point-to-point connection where one device is interfaced only to an ECU (Figure 45) or implementing a multi-slave single bidirectional wire connection. (Figure 46).

In Open Drain mode, one Master can address up to four sensors over a single wire, one sensor at a time. Sensors are identified by their slave address, stored in the NVM or by address pin strapping.

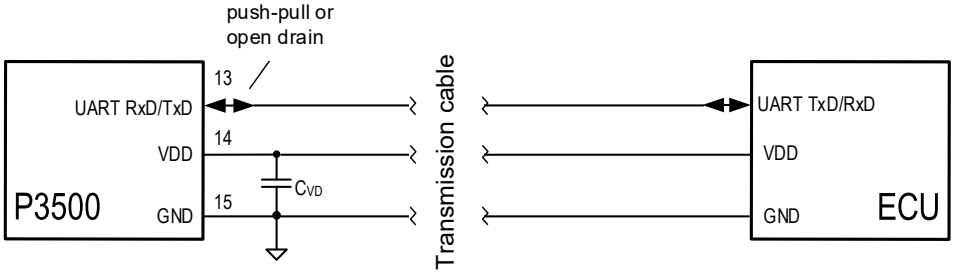


Figure 45. UART point-to-point single-wire bidirectional connection

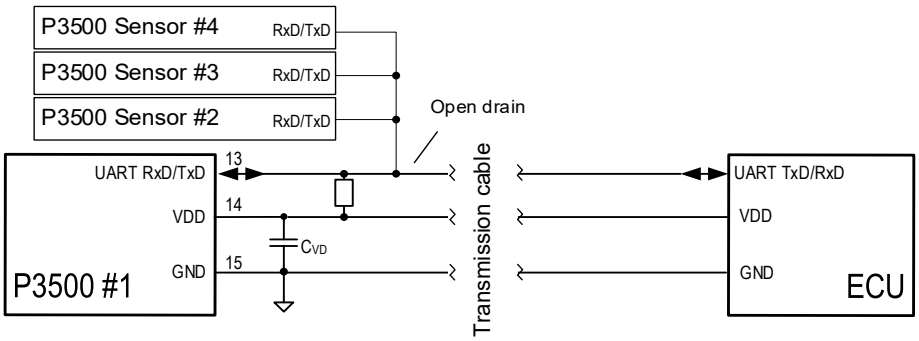


Figure 46. UART multi-slave single-wire bidirectional connection

5.5.2 Dual-Wire Differential Bidirectional UART with Pseudo-Differential TX

In Dual-Wire UART mode, the device uses both OUT1/OUT2 pins to communicate. A point-to-point connection could be implemented similarly to what shown in Figure 45. This communication mode uses OUT1 as single-wire transceiver.

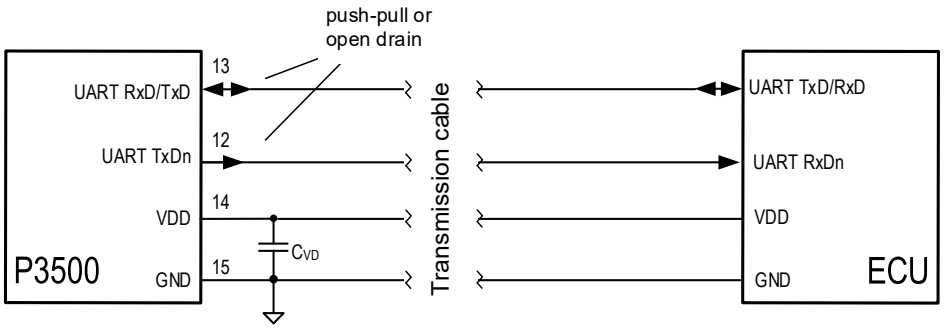


Figure 47. UART 2-wire point-to-point connection with pseudo-differential TX

In addition, OUT2 (pin #12) is used as transmitter and OUT1 (pin#13) is used to transmit and receive but it is carrying an inverted information of the transmitted data, creating a pseudo differential signal for safer data transmission. While receiving, OUT1 is kept in HIGH state.

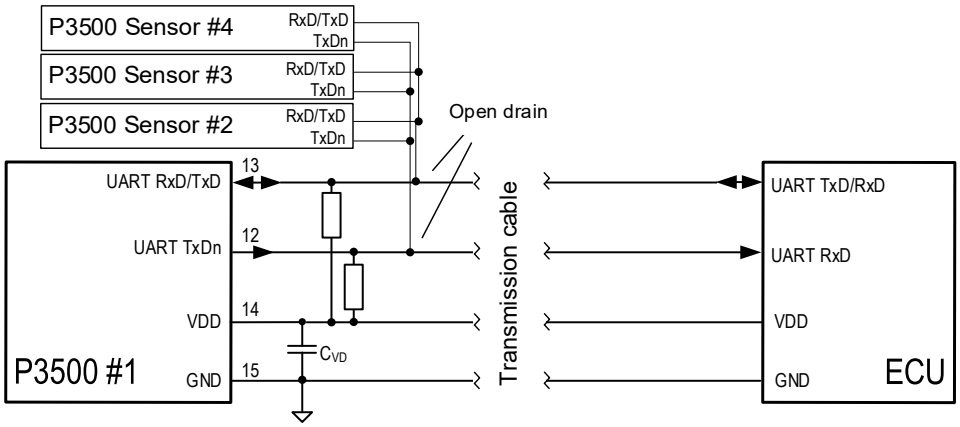


Figure 48. UART 2-wire connection with pseudo-differential TX and multiple slaves

In Pseudo-Differential mode, with open drain configuration, one Master can address up to four sensors, one sensor at a time. Sensors are identified by their slave address, stored in the NVM or by address pin strapping.

5.5.3 Dual Wire Unidirectional UART

This dual wire mode uses separate, unidirectional lines for transmitting and receiving. The transmitter may be configured for both push-pull or open-drain output. Push-pull mode is recommended for achieving data rates up to 2 Mbit/s. In open-drain mode, data rates may be limited, depending on the capacitive load on the transmission cable and the resistance of the pull-up resistor.

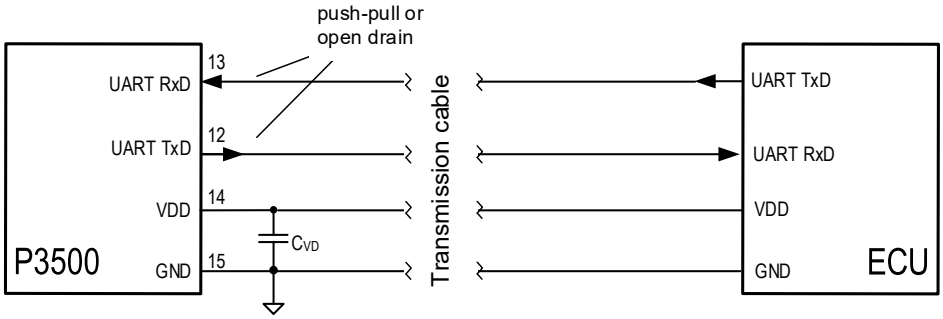


Figure 49. UART 2-wire unidirectional connection

In Dual-Wire Unidirectional mode, one Master can address up to four sensors, one sensor at a time. The sensors get identified by their slave address in the NVM or by address pin strapping. Note that for parallel connection of several sensors on the same line, the transmitter output (TxD) must be configured for open drain output.

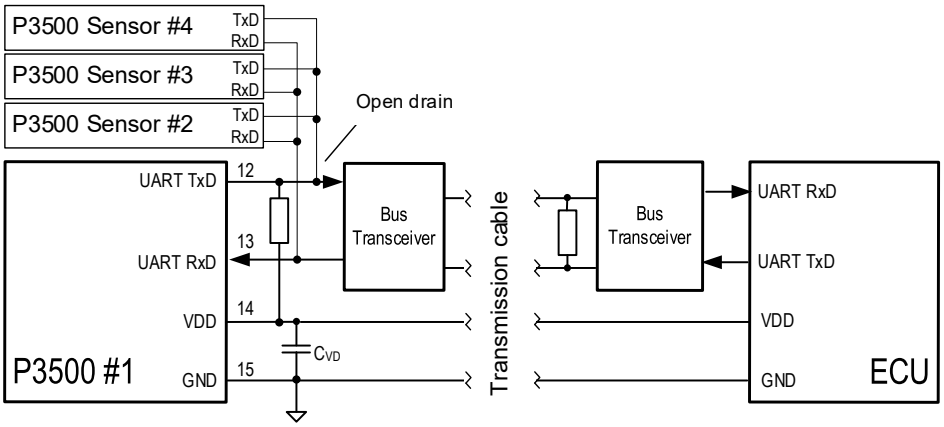


Figure 50. UART 2-wire unidirectional connection with multiple slaves and bus transceivers

The transmission cable can be extended with external bus transceiver circuits as shown in, providing extra robustness and low capacitive load for the UART TxD output pin, achieving high data rates up to 2 Mbit/s.

5.5.4 UART Address Pin Strapping

The two least significant bits (LSBs) of the RAA2P3500 UART's slave address can be set either through programming or by hardware pin strapping.

In Pin Strapping mode, two pins set the address:

- Pin #2: ADR0 - Address bit 0
- Pin #3: ADR1 - Address bit 1

5.5.5 UART Operating Commands

The RAA2P3500 provides 3 UART operating modes:

- 16-bit register write (Figure 51)
- 16-bit register read (Figure 52)
- Fast read mode of two registers within one frame with 12, 14, or 16 bits of data per register.

5.5.5.1 Gap Time between Messages

A minimum pause (gap) time is implemented between the messages to ensure the controller goes to idle before next communications. Minimum time for each UART baud rate configuration is shown in Table 39.

Table 39. UART wait time between measurements

UART baud rate [bits/s]	Min gap time [bits]
9600, 57600, 115200, 230400	10
1M, 2M	12

5.5.5.2 UART Register Write

This mode writes one register per frame. Each frame contains 8 bytes, with each byte including a start and stop bit, totaling 8x10 bits. A short wait (GAP) time is required between frames. All bytes are written by the Master and sent to the chip.

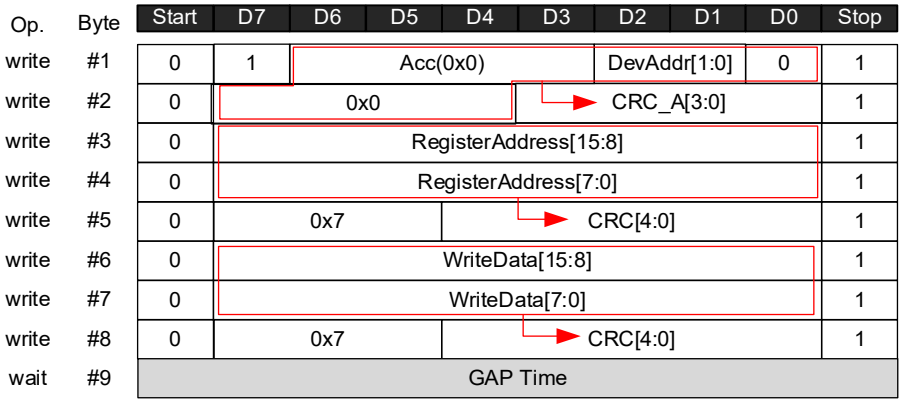


Figure 51. UART register write mode

Figure 51 shows the Write Frame structure where:

- *Acc*: Access type 0x0 for register write.
- *DevAddr*: The device address if several sensors are connected in parallel, it defines their slave address (0x1-0x3). The default is 0x0.
- *RegisterAddress*: The target register.
- *WriteData*: The data to be written.
- *CRC, CRC_A*: Cyclic redundancy check.

5.5.5.3 UART Register Read

In read mode, the device reads one register per frame. The first five bytes are sent from the Master to the chip, while bytes six to eight are read from the chip by the UART in read access mode. In all modes, the bit order is MSB to LSB. The read frame contains eight bytes, each with a start and stop bit, totalling 8x10 bits. A short wait (GAP) time required between each frame.

During data read operations, the Master must add an additional wait bit when switching from sending to receiving data due to the generation of the differential start and stop bits. This results in each frame containing either 91 bits (for data rates up to 230.4 kbit/s) or 93 bits (for 1Mbit and 2Mbit data rates).

In register read mode, an additional wait bit must be added at the end of byte five before the chip can start transmitting data (start bit of byte six). The *ReadData* content is latched at the stop bit of byte five.

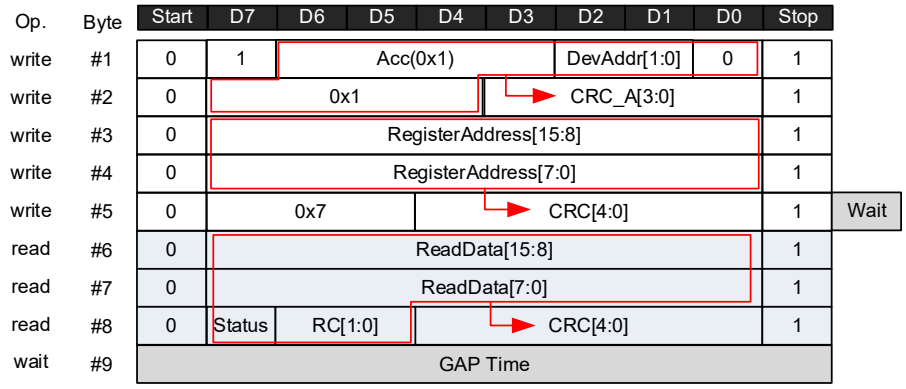


Figure 52. Register read mode frame

Figure 52 shows the Read Frame structure where:

- *Acc*: Access type 0x1 for register read.
- *DevAddr*: the device address if several sensors are connected in parallel, it defines their slave address (0x1-0x3) Default value is 0x0.
- *RegisterAddress*: the target register.
- *ReadData*: the data contents of the target register.
- *CRC, CRC_A*: cyclic redundancy check.
- *Status*: 1 bit status flag information of the sensor (0: normal operation, 1: error)
- *RC*: rolling counter, a counter that increments with each frame and wraps around 0 when overflowing.
- Wait: 1 bit wait time for master before receiving data (in pseudo-differential mode only).

5.5.5.4 UART fast two-register read

This mode facilitates the efficient reading of a defined subset of two registers per frame. The first two bytes of the frame specify which subset of the predefined registers is to be read, defined by a 4-bit access code, The access type is set on the Acc1 and Acc2 bitfields (see Table 40). The read data for the first register is contained in bytes three to five, and for the second register, it is in with bytes six to eight.

Table 40. UART Fast Access mode

Acc Type1/2	Byte#3/Byte#6	Byte#4/Byte#7		Byte#5/Byte#8		
2	Sensor Data[11:4]	Sensor Data[3:0]	RC[5:2]	S	RC[1:0]	CRC[4:0]
4	Sensor Data[13:6]	Sensor Data[5:0]	RC[3:2]	S	RC[1:0]	CRC[4:0]
7	Chip Temperature	0x0	RC[5:2]	S	RC[1:0]	CRC[4:0]
8	Analog input [12:5]	Analog input [4:0]	0 RC[3:2]	S	RC[1:0]	CRC[4:0]
11 = 0xB	IRQ Status 0 [15:8]	IRQ Status 0 [7:0]		S	RC[1:0]	CRC[4:0]
12 = 0xC	IRQ Status 1 [15:8]	IRQ Status 1 [7:0]		S	RC[1:0]	CRC[4:0]

Acc Type1/2	Byte#3/Byte#6	Byte#4/Byte#7	Byte#5/Byte#8		
13 = 0xD	IRQ Status 2 [15:8]	IRQ Status 2 [7:0]	S	RC[1:0]	CRC[4:0]
14 = 0xE	IRQ Status 3 [15:8]	IRQ Status 3 [7:0]	S	RC[1:0]	CRC[4:0]
15 = 0xF	IRQ Status 4 [15:8]	IRQ Status 4 [7:0]	S	RC[1:0]	CRC[4:0]

Note 1 RC: Rolling counter.

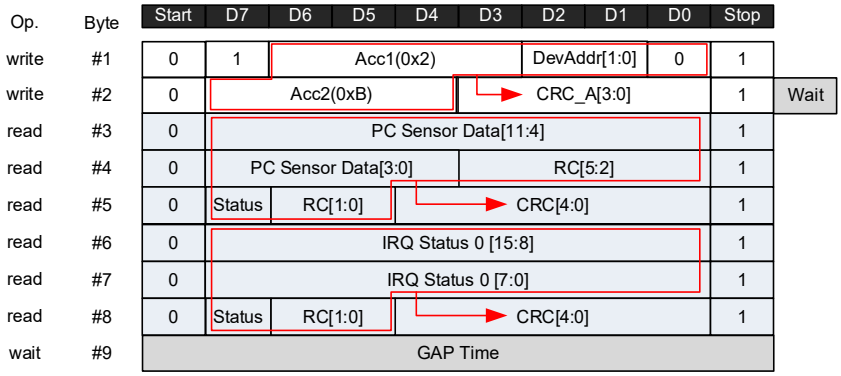


Figure 53. UART fast read mode example with different access codes

Figure 53 shows the frame structure, an example of reading 12-bit primary coil sensor data (Acc1 = 0x2) and 16-bit IRQ status 0 (Acc2 = 0xB), the frame bitfield are:

- *Acc1, Acc2*: Access code: 0x2 to 0xF (see Table 40)
- *DevAddr*: Device address: (default = 0x0. If several sensors are connected in parallel, it defines their slave address (0x1-0x3).
- *CRC*, *CRC_A*: Cyclic redundancy check.
- *Status*: 1 bit status flag information of the sensor (0: normal operation, 1: error)
- *ReadData*: the data answer from the IC are the PC Sensor Data + RC for Byte #3 and #4 according to ACC1=0x2, while for ACC2=0xB the device provides IRQ_Status on Byte#6 and #7. (see Table 40). The ReadData is latched at the stop bit of Byte#2 for Acc1, and at the stop bit of Byte#5 for Acc2.
- *RC*: Rolling counter, a counter that increments with each frame and wraps around 0 when overflowing
- *Wait*: 1 bit wait time for master before receiving data (in pseudo-differential mode only)

In Fast Read mode, an additional wait bit must be added at the end of byte #2 before the chip can begin transmitting data.

5.5.5.5 UART Fast Read Mode with Same Access Code

Reading the same register twice provides two results from the same input at different sampling timestamps. For example, the primary coil sensor data can be read twice (see Figure 54). The first reading (Acc1= 0x2) is sampled at the end of byte two, while the second reading (Acc2 = 0x2) is sampled at the end of byte five. This results in an interval of 30 bits between the two samples in the UART clock (3 bytes, including start and stop bits).

By repeating this sequence, users can obtain two samples within a 92-bit frame. The timeframe between consecutive sample is 30 UART clock cycles, which equates to 15 µs at 2 M/s Baud-rate. The time interval between each frame is 46 µs at the same Baud-rate.

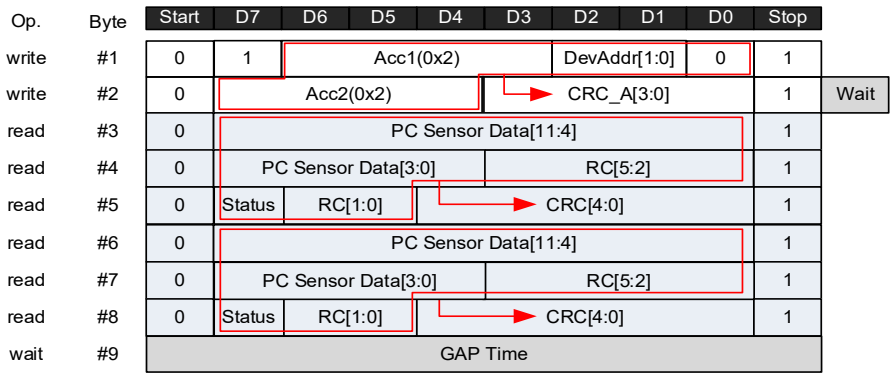


Figure 54. UART fast read mode of the same register

Table 41 shows a summary of the UART interface speed, depending on the selected Baud rate and mode. One frame can perform a register read, a register write, or two consecutive register read (fast read mode).

Table 41. UART data access speed with *uart_start_bit_cfg = 0*

UART baud rate [bits/s]	Bits per frame (incl. gap time)	Time per frame [µs]	Frame rate [frames/s]
9600	91	9479.4	105.5
57600	91	1580	633
115200	91	789.9	1265
230400	91	395	2532
1M	93	93	10.75k
2M	93	46.5	21.5k

5.6 UART Single-Wire Programming Interface

Any user programmable parameter can be accessed through the 2-wire programming process, with UART protocol. Performing an end-of-line calibration or in-line programming of a position sensor module containing the RAA2P3500 requires no additional wires. The chip is programmed through the OUT1 and OUT2 outputs at the operative supply voltage range (5 V ±10%, 3.3 V ±10%).

A short programming window is enabled after POR and requires a digital unlock password to enable programming. If no password is sent, the chip resumes its normal operating mode. For more details, see *RAA2P3500 Programming Manual*.

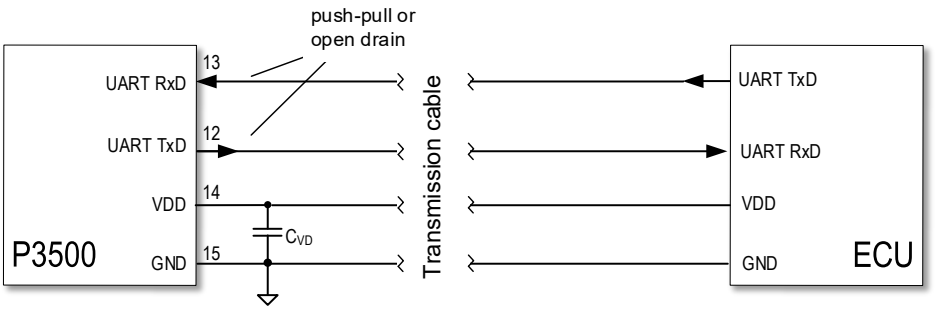


Figure 55. UART NVM programming

5.6.1 Lock Feature

The RAA2P3500 includes a user configurable lock bit option to restrict write and/or read access. When the lock bits are enabled, no further write or read operations to the RAA2P3500 are prohibited.

NOTE
When a RAA2P3500 is locked, it cannot be unlocked.

For more details, see *RAA2P3500 Programming Manual*.

6. Auxiliary Input and Outputs

One analog auxiliary input is available for connecting external devices with analog outputs, which can be read through the SPI or UART interface. Further, a digital output pin is available indicating user programmable features. A summary is shown in Table 42.

Table 42. Auxiliary inputs and digital output options

Interface	Analog input	Digital output
		Register flag (OD)
SafeSPI	Yes (pin 4)	Yes (pin 13)
UART	Yes (pin 10)	n/a
Incremental	n/a	n/a
Incremental + SENT	Yes (pin 10)	n/a

6.1 Analog Input

The analog input is available on pin 4 for SafeSPI and on pin 10 for UART and SENT and can be used to read analog voltages from external sensors via SPI, UART or SENT interfaces. See Table 43 for the key parameters of this input. The analog value must be in relation to VDDD.

Table 43. AIN analog input parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN_AIN}	AIN voltage range		0.2		1.2	V
RES_{AIN}	ADC resolution			12		bits
T_{Smp_AIN}	Sampling rate		4.4			kHz
ACC_{AIN}	Analog Input Accuracy		−1.2		1.2	% VDDD

Both the analog input and the VDDD reference voltages are internally measured and stored in registers. The external load on VDDD cannot exceed 1 mA as specified in Table 4.

6.2 Digital Output

An optional digital output is available and can be configured for various functions, depending on the selected interface, as shown in Table 42.

6.2.1 Register Flag

In this configuration, available in SafeSPI mode, the DOUT output can be used to drive external circuits. It is controlled by writing either of the following options to a register bit to the address 0x029E [0]:

- Register bit 0: FLG output is low
- Register bit 1: FLG output is high

This function can be integrated with a heartbeat feature to provide diagnostic status information alongside the flag value. This status is indicated by a 1.5 kHz pulse, see Figure 56 with a duty cycle of 97% when the flag is high and 3% when the flag is low.

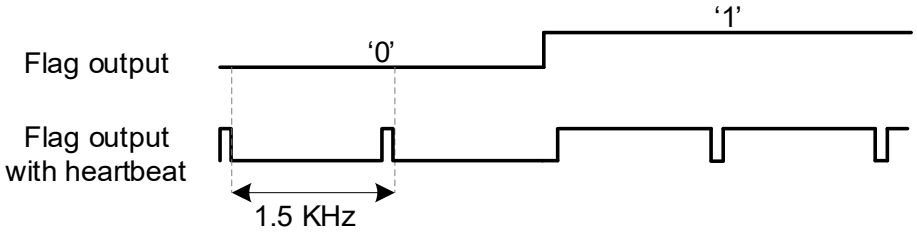


Figure 56. Flag output configurations

7. Functional Safety Mechanisms

The RAA2P3500 includes on-chip diagnostics featuring an extensive number of internal functional safety mechanisms (FSM). These mechanisms can be classified as either temporary or static.

When a fault is detected by a Static FSM, the IC goes to a latched state that can only be terminated by resetting the device. When a fault detected by a Temporary FSM is no longer active, the IC can recover to the Normal Operation mode. For detailed description, see *RAA2P3500 FuSa Manual*.

Table 44. Diagnostic parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{FDTI}	Failure detection time interval (time to detect and internally set a flag describing the error condition)	fdti_cfg = 1			2.3	ms
		fdti_cfg = 0			20	ms

Table 45. Failure detection mechanisms for diagnostics

Category	Failure Safety Mechanism (FSM)	Target failure	Processing Mode	Diagnostic mode
Monitoring of external supply	VDD HK monitor	External supply out of range	Continuous check	Temporary
Monitoring of internal supplies	VDDA out of range	Internal VDDA Analog supply: 1.8 V out of range	Continuous check	Temporary
	VDDA undervoltage	Internal VDDA undervoltage detected	Continuous check	Temporary
	Internal pre-regulators for analog parts and bandgap	Internal pre-regulator for power management (bandgap, analog parts) out of range	Continuous check	Temporary
	VDDD HK monitoring	Internal digital supply VDDD HK out of range	Continuous check	Temporary
	VDDD POR	Internal digital supply VDDD out of range	Continuous check	Temporary
	Pre-reg on power management	Pre-regulator for the power management (output stages) out of range	Continuous check	Temporary
	Short on VDDD digital	VDDD short detected, overcurrent at VDDD pin	Continuous check	Temporary
	VDDint HK monitoring	Supply for the input PADs and for the deep sleep control module: ~VDD - 0.2 V out of range	Continuous check	Temporary
	VDDint POR	Internal VDDint supply out of range detected	Continuous check	Temporary
	High Voltage on Internal VDDA	High voltage on Internal Analog supply - 1.8 V detected	Continuous check	Temporary
	VDD_DRV OUT2 regulator driver	HK for the driver regulator for OUT2 out of range	Continuous check	Temporary
	VDD_LC regulator for LC oscillator	HK for LC oscillator regulator out of range	Continuous check	Temporary
	Bias current fail	Bias current diagnostic out of range	Continuous check	Temporary
Monitoring of RX coils	Primary RX coil SIN short detection	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX SIN	Continuous check	Temporary
	Primary RX coil COS short detection	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX COS	Continuous check	Temporary
	Primary RX coil SIN/COS neighbor inputs short	Short check between SIN/COS coil set detected	Continuous check	Temporary

Category	Failure Safety Mechanism (FSM)	Target failure	Processing Mode	Diagnostic mode
Monitoring of TX coils	TX Common mode voltage	Common mode voltage of TX1/TX2 out of range	Continuous check	Temporary
	TX broken pins	Flag for broken pins of LC oscillator	Continuous check	Static
	LC oscillator stuck	LC oscillator stuck detected	Continuous check	Temporary
	LC frequency monitoring	LC oscillator frequency out of range	Continuous check	Temporary
Monitoring of system clock	System clock frequency	Fault in internal system clock: frequency out of range	Continuous check	Static
	System clock stuck	Fault in internal system clock: stuck detected	Continuous check	Static
Monitoring of the internal communication channel	Internal digital logic fail flag	Internal digital logic fail of the following: ▪ APB Diagnostics ▪ IC internal registers ▪ Permanent/transient failure ▪ FSM failure ▪ CORDIC failure ▪ Xbar monitoring	Continuous check	Static
	Xbar Watchdog	Internal communication halted	Continuous check	Static
Monitoring the internal memory	NVM CRC and shadow register CRC	CRC mismatch over the NVM or internal shadow register, permanent or transient failure	Continuous check	Static
	NVM read error	NVM read timeout fail	Startup	Static
Data path diagnostics	Data path WD/OF/UF/DO	Internal errors, such as overflow, underflow, division by 0, or watchdogs	Continuous check	Temporary
Temperature monitoring	Temperature warning detected	Temperature warning detected	Continuous check	Temporary
	Temperature error (shutdown) detected	Temperature error (shutdown) detected	Continuous check	Static
Magnitude evaluation	Magnitude static error	Magnitude static check error detected for primary coil	Continuous check	Temporary
Monitoring of analog signal path offset	ADC temperature sensor offset fail	Compensation of the internal offset not sufficient	Continuous check	Temporary
Monitoring of the mechanical stress/cracks	Broken chip check	IC die mechanical failures detected	Continuous check	Static
LPF check for signal path	LPF monitoring	Failure in internal LPF	Continuous check	Temporary
AGC monitoring	AGC error monitoring primary coil	Automatic gain control loop not converging	Continuous check	Temporary
	AGC plausibility error "AGC range check" primary coil	Pre-defined acceptable gains for the AGC not sufficient for primary coil	Continuous check	Temporary
Analog input	Analog input out of range HK monitor	Failure on analog input range	Continuous Check	Temporary
	Analog input open HK monitor	Failure on analog input	Continuous Check	Temporary

Category	Failure Safety Mechanism (FSM)	Target failure	Processing Mode	Diagnostic mode
Out2 and IO1 pins monitoring	Out2/IO1 pins monitoring	Overvoltage/undervoltage	Continuous check	Temporary
	Out2/IO1 pins monitoring	Short detection	Continuous check	Temporary

In diagnostic mode, the incremental outputs enter a combination of logic levels that do not occur in normal operation. The diagnostic state depends on the settings of index pulse width and index pulse position as outlined in Table 46. Additionally, the diagnostic status indication varies based on the incremental mode selected.

A summary of the diagnostic state indication is shown in Table 46.

Table 46. Incremental output diagnostic states

Selected ABI Index/Zero position	Diagnostic state indication			
	ABI mode	Step/Direction mode	AB+ PWM mode	UVW mode
Zero/Index: ABI = 001	ABI = 111	SDI = 1x1	PWM = 2.5% duty cycle	UVW = 111
Zero/Index: ABI = 111	ABI = 001	SDI = 0x1	PWM = 97.5% duty cycle	UVW = 000
Zero/Index: ABI = 011	ABI = 101	SDI = 1x1	PWM = 97.5% duty cycle	UVW = 000
Zero/Index: ABI = 101	ABI = 011	SDI = 0x1	PWM = 2.5% duty cycle	UVW = 111

7.1 Shorted and Broken Wire Detection

A fault from a broken or shorted wire refers to the connection between the sensor IC and the control unit (such as MCU or ECU). This includes the soldering of the IC pins, PCB traces, connectors, and cables.

7.1.1 Shorted Wires

Shorts between Ground, Signal and Supply wires can be safely detected, as shown in Table 47.

Table 47. Detection of shorts between wires

Cable connections	Supply	Output	Ground
Supply	Short between two supplies. Only applicable for isolated, redundant sensor IC supplies. Must be monitored and controlled by the external power supply unit supplying the sensors.	Short between Supply and Output. Output switches to tri-state when the output current exceeds the overcurrent threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between Supply and Ground. Overcurrent in the supply line. Must be monitored and controlled by the external power supply unit supplying the sensor.
Output	See description for short between Output and Supply	Short between two different outputs. Outputs switch to tri-state when their output current exceeds the overcurrent threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between Output and Ground. Output switches off when the output current exceeds the overcurrent threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.
Ground	See description for short between ground and supply	See description for short between Output and Ground	Short between Ground and Ground. Separate ground lines are not recommended for EMC reasons

7.1.2 Broken Supply Lines, Incremental Output Modes

As shown in Table 46, the diagnostic state of the incremental outputs depends on the settings for:

- Incremental mode
- Index pulse width
- Index position

If the chip causes a fault from a broken supply line, the outputs will enter a high ohmic state, therefore the diagnostic state must be indicated by means of pull-up and/or pull-down resistors, as shown in Figure 57 and Figure 58.

In ABI and Step/Direction mode, depending on Index pulse programming, the Diagnostic states are either ABI=001 or ABI=111, therefore the external pull-up/pull-down resistors must be connected accordingly, as outlined in Figure 57.

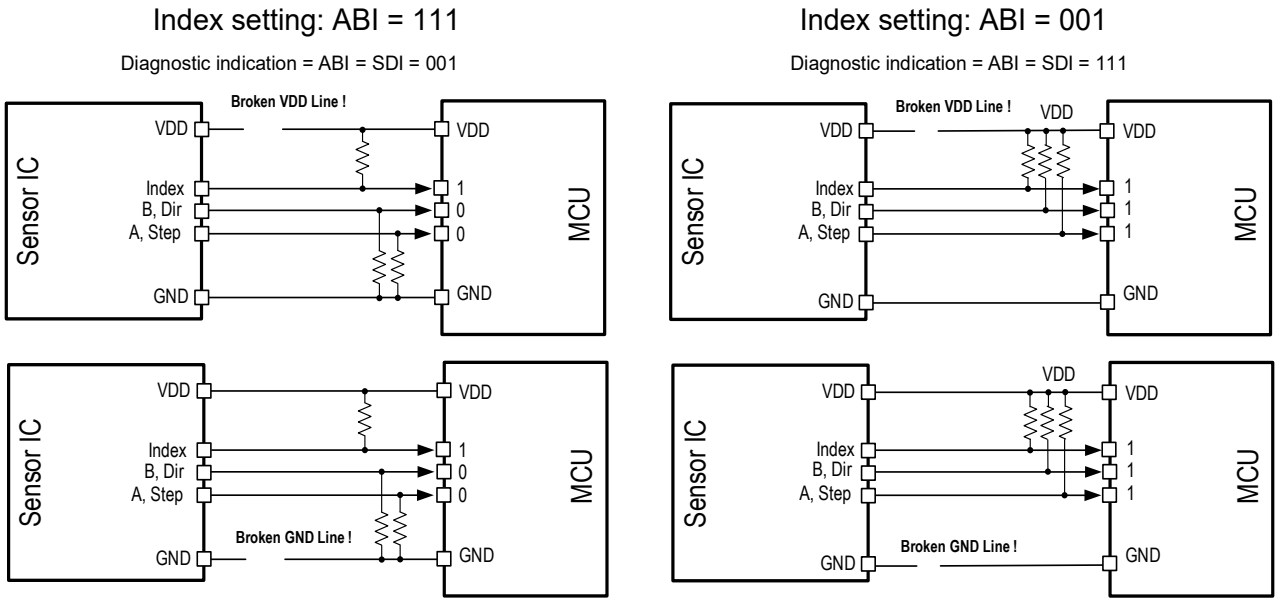


Figure 57. Broken supply diagnostic indication: ABI and Step/Dir modes

In UVW mode, depending on Index pulse programming, the Diagnostic states are either UVW=000 or UVW=111, therefore the external pull-up/pull-down resistors must be connected accordingly, as outlined in Figure 58.

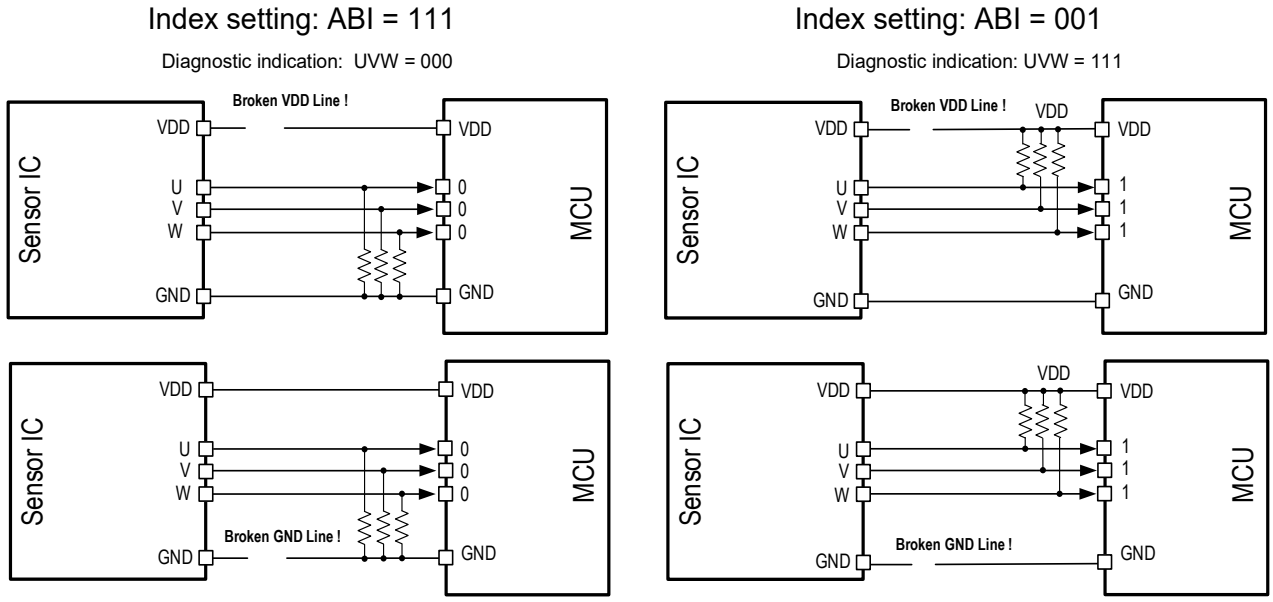


Figure 58. Broken supply diagnostic indication: UVW mode

7.1.3 Broken Supply and Signal Lines, SafeSPI Mode

Both broken supply lines as well as broken signal wires can be easily detected in SafeSPI mode through data transmission errors (wrong CRC, wrong Slave data response). Additional pull-up or pull-down resistors for diagnostic checks are not required in SafeSPI mode.

7.1.4 Broken Signal Wires, Incremental Output Modes

While a fault from a broken supply line can be immediately detected, as outlined in the previous chapter, faults from a broken signal line on an incremental output cause this signal to be permanently stuck at high or low level, depending on the connection of the external pull-up or pull-down resistors. In a rotating system, this will eventually lead to a logical combination of the outputs, resembling a diagnostic state and thus indicating a fault, but it may take up to 1 electrical period of rotation, before this state has been reached.

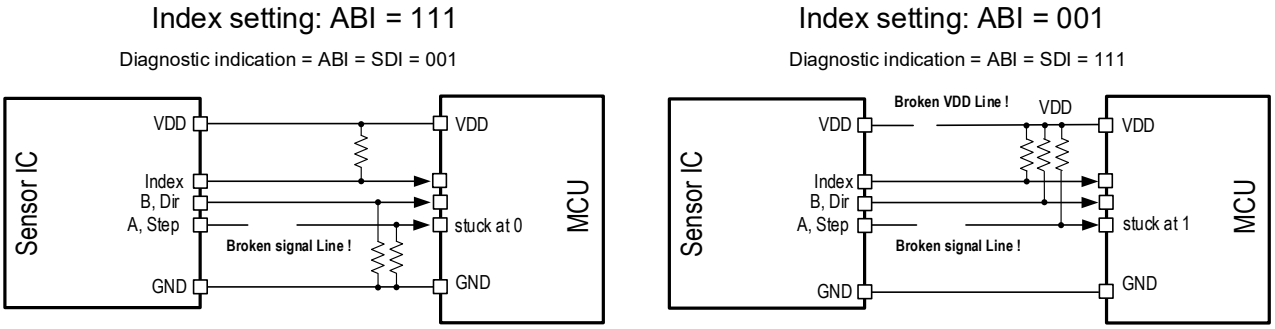


Figure 59. Broken signal wires

8. User Programming Options

Table 48 shows an extract of the main configuration options. A detailed description is provided in the *RAA2P3500 Programming Manual*, available on request from Renesas Electronics.

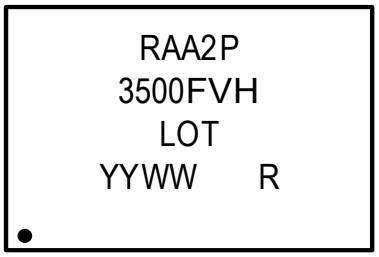
Table 48. Global programming options, RAA2P3500

Programming Option	Description
Power supply mode	3.3 V ±10% or 5.0 V ±10%
Interface options	SPI, UART, ABI, AB+PWM, AB+SENT, Step/Dir interface, Step/dir + PWM, Step/Dir + SENT, UVW interface
Automatic gain control AGC	Enabled/disabled
Number of linearization points	2/4/6/8/16 linearization points, programmable in x and y
Linearization, X and Y positions	Up to 16 linearization points programmable in X (position) and Y (value)
Magnitude upper and lower limit alarm	Static upper and lower magnitude (Sine, Cosine signal strength)
Zero (discontinuity) point	12-bit discontinuity point
Sine and cosine signal offset correction	±127 LSBs
Sine and Cosine amplitude mismatch correction	0% to 199% adjustment range per channel
Digital low pass filter	Depth of digital low pass filter for position output
Turns counter option	Behavior of 12-bit turns counter when overflowing: ▪ stop at max/min, wrap around
Alarm flags	Enable/Disable internal alarm flags for diagnostic indication
Customer ID	48-bit scratchpad register for customer specific data

9. Package Outline Drawing

The package outline drawings are accessible at: https://www.renesas.com/sg/en/document/psc/16-tssop-package-outline-drawing-44mm-body-065mm-pitch-pgg16t1?r=801

10. Marking Diagram



Line 1: First characters of part code RAA2P

Line 2: Next four characters of the part code:
3500F: Single coil high speed

followed by

V = Operation temperature range, Automotive

H = Automotive Qualified

Line 3: “LOT” = Lot number

Line 4: “YYWW” = Manufacturing date:

YY = last two digits of manufacturing year

WW = manufacturing week

R = RoHS compliant statement

11. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
RAA2P3500FVHSP#HA0	16-TSSOP, 4.4 ×5.0 mm	1	13” Reel, 4000 parts/reel	−40° to +160°C
For communication and programming, the RAA2P3500 Application Modules listed below require an RAA2P-COMBOARD, which is available separately.				

12. Revision History

Revision	Date	Description
1.10	Sep 22, 2026	Table 1: Updated pin descriptions Table 5: Added notes Table 8: Updated parameter descriptions Table 10, Table 11, Table 12, Table 13: Updated notes Figure 1, Figure 4, Figure 21: Updated Table 4, Table 19, Table 42, Table 43, Table 48: Updated Section 6.1: Updated description Updated first page
1.00	Dec 10, 2025	Initial release