RAA271084, RAA271084-B

General-Purpose Power Management IC for Automotive Applications

Description

The RAA271084 (ASIL-D) and RAA271084-B (ASIL-B) are general-purpose Power Management Integrated Circuits (PMIC) with high voltage front-end, optimized for providing MCU power in automotive applications.

RAA271084 and RAA271084-B contain a high voltage primary buck/boost controller, a low voltage synchronous buck controller and five low-dropout linear regulators (LDO), two of which can be used as trackers.

RAA271084 supports system safety goals up to ASIL-D, while the RAA271084-B supports ASIL-B. It includes independent references for monitoring of the output voltages, three internal temperature monitors, watchdog timer, MCU error pin monitors, reset generator, a dedicated safety-control state machine and a safety shutdown path. RAA271084 is available in 48-lead SCQFN or 48-lead LQFP-EP, while the RAA271084-B is available in 48-lead SCQFN. Both device are offered as AEC-Q100 Grade 1 operation supporting an ambient temperature range of -40°C to 125°C.

Applications

- Automotive power-train systems
- Automotive gateway systems
- Ideal power supply for Renesas RH850 U2x MCUs

Features

- Input range 2.7V to 42V including cold crank
- Two DC/DC controllers with integrated drivers
  - Buck-Boost DCDC1 5.7V
  - Buck DCDC2 resistor programmable
- Five linear regulators
  - LDO0: 5V (always on)
  - LDO1-4: programmable 3.3V/5V
  - LDO3-4: can be configured as trackers with short-to-battery/short-to-ground and reverse current block
- Low I_Q modes (see Table 1 and Electrical Characteristics Table)
  - Power-off standby mode: 16µA
  - DeepSTOP mode: 160µA
  - EOT (Engine Off Timer) mode: 25µA
- RAA271084 Switching frequency: Selectable 440kHz/2.2MHz with optional pseudo-random spread spectrum clock
- RAA271084-B Switching frequency: 2.2MHz with pseudo random fixed 4 cycle dwell spread spectrum clock
- FET drivers able to source/sink 1.0A/1.5A
- Option for windowed QA watchdog (ASIL-D only) or basic windowed watchdog accessible through SPI
- MCU error input pin (ERRb)
- Programmable MCU reset and Interrupt
- External core voltage monitor (ASIL-D only)
- AEC-Q100 qualified (grade 1)

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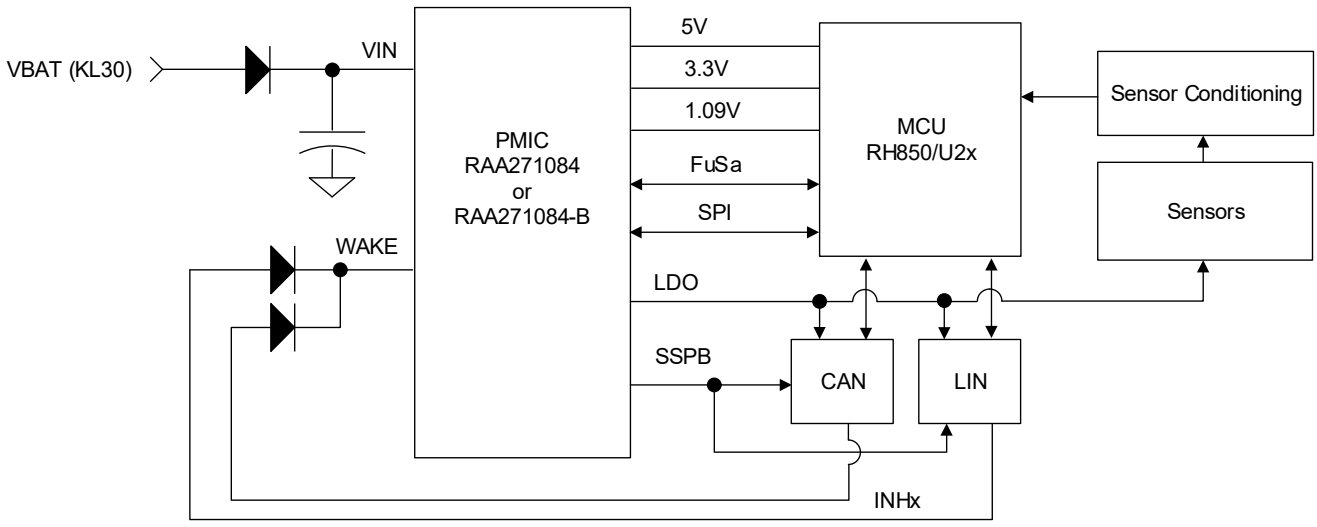


Figure 1. Typical Application Diagram

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1. Overview

1.1 Block Diagram

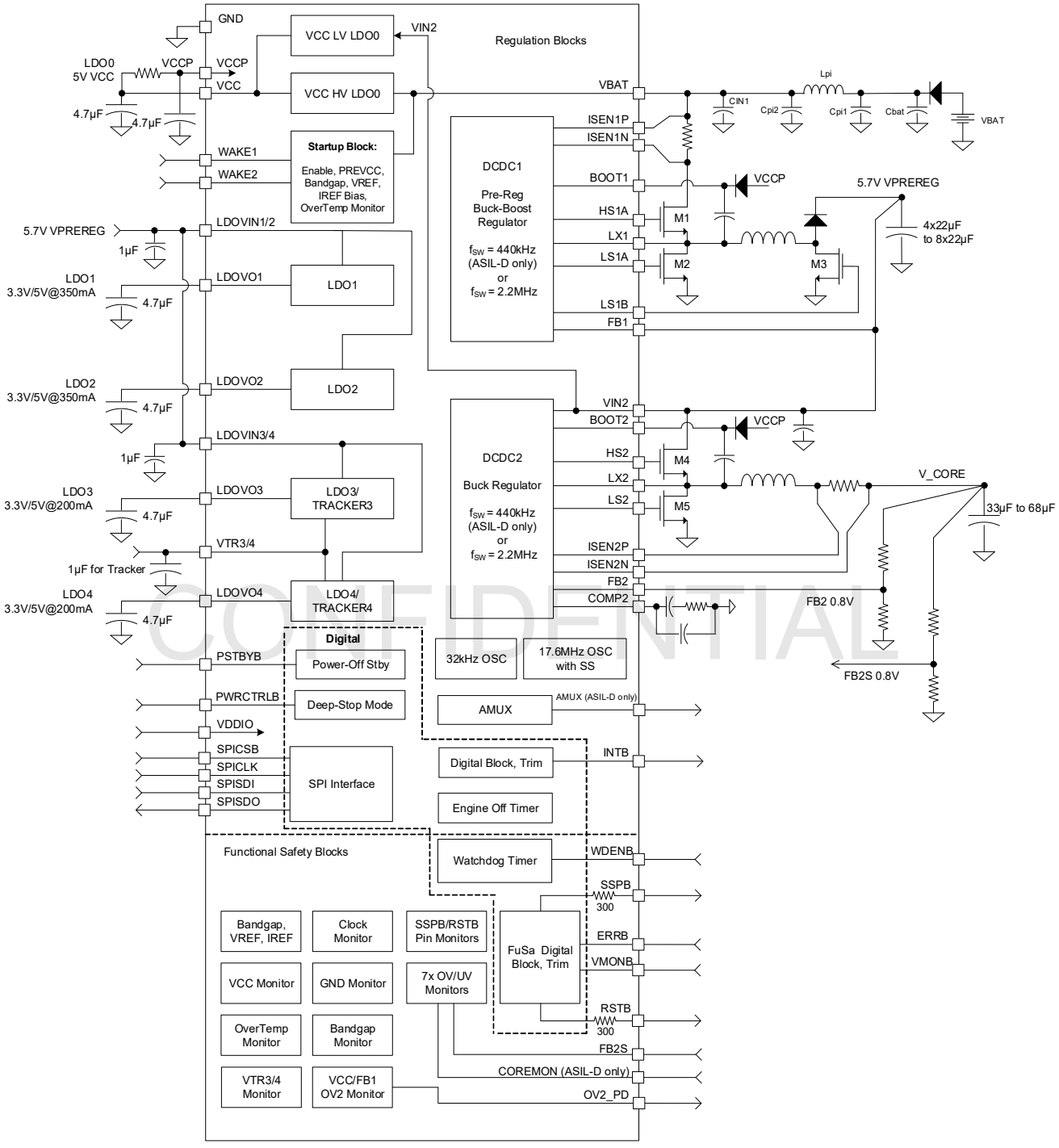


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

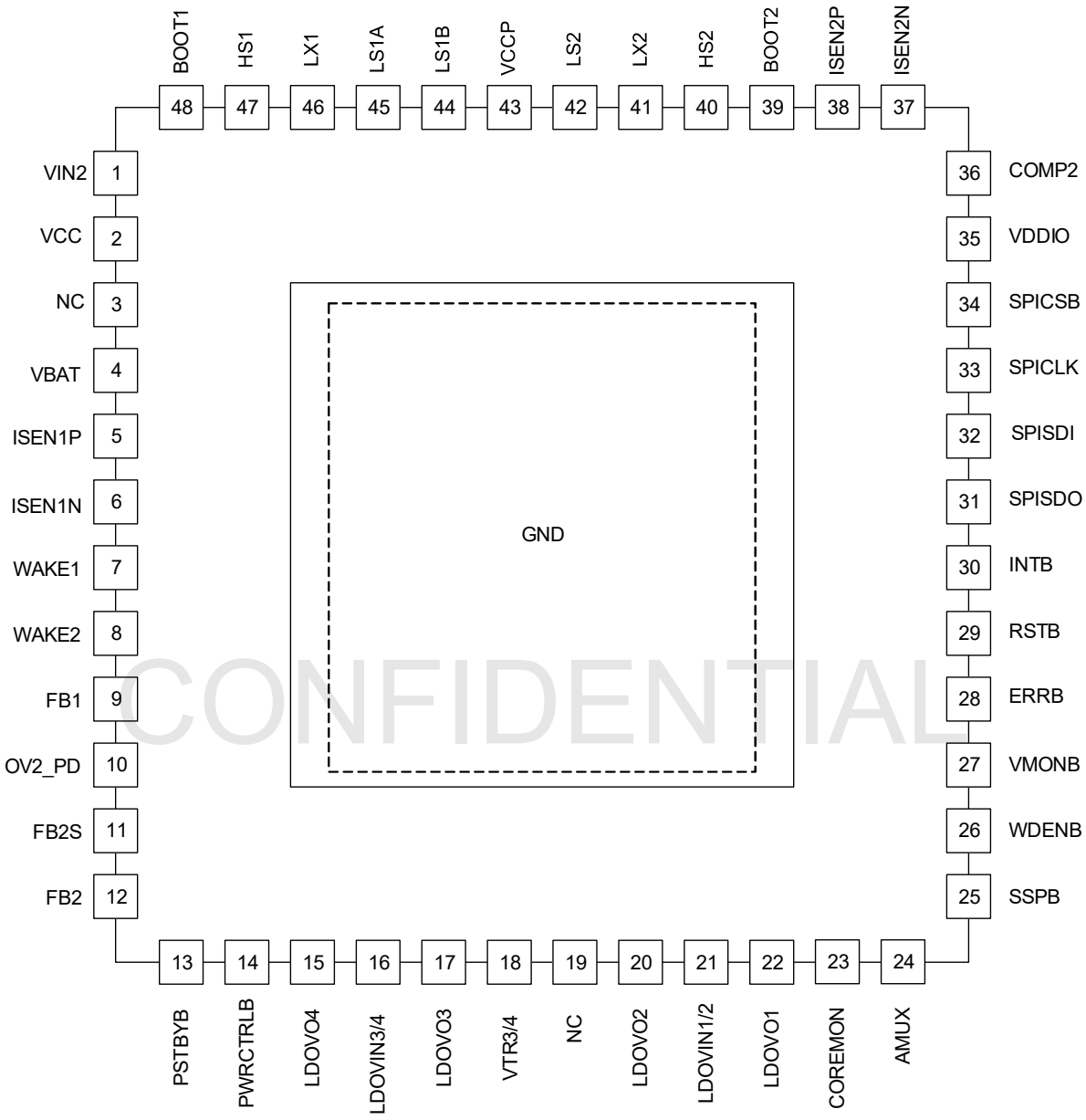
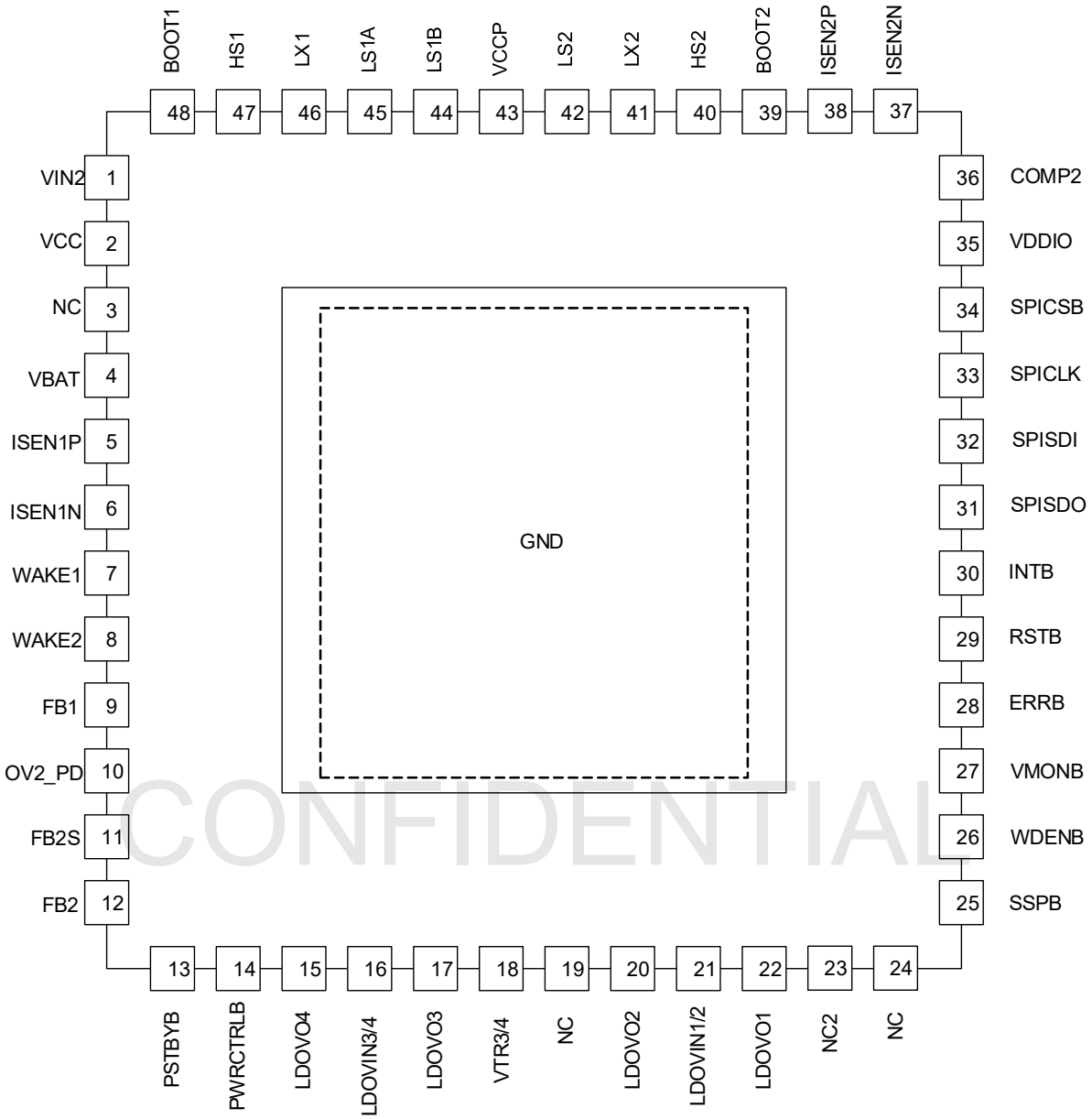


Figure 3. RAA271084 (ASIL-D) Pin Assignments - Top View

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Figure 4. RAA271084-B (ASIL-B) Pin Assignments - Top View

2.2 Pin Descriptions

RAA271084 Pin Number	RAA271084-B Pin Number	Pin Name	Description
1	1	VIN2	Input supply pin for VCC LV LDO0 and Core Buck regulator (DCDC2). Connect a 1µF capacitor to GND close to the pin.
2	2	VCC	LDO0 output and bias supply (5V typical) for internal circuits. A 4.7µF decoupling capacitor should be used between this pin to ground and placed near GND. Using an RC filter connecting to VCCP also provides the power MOSFETs driving power.
3, 19	3, 19, 24	NC	Not Internally connected.
4	4	VBAT	Input supply for the VCC HV LDO0 and DCDC1 regulator. Connect a 1µF capacitor to GND close to the pin.
5	5	ISEN1P	Input current sense pin connected to positive terminal of the current sense resistor, also connected to VBAT.

RAA271084 Pin Number	RAA271084-B Pin Number	Pin Name	Description
6	6	ISEN1N	Input current sense pin connected to the negative terminal of the current sense resistor, also connected to the drain of the high side MOSFET (M1) of DCDC1.
7	7	WAKE1	Wake/Enable control pin 1. Weak pull-down to GND on-chip. A logic high activates the pin.
8	8	WAKE2	Wake/Enable control pin 2. Weak pull-down to GND on-chip. A logic high activates the pin.
9	9	FB1	DCDC1 buck-boost pre-regulator feedback pin. Connect to VOUT1.
10	10	OV2_PD	OV2_PD asserts High if VOUT1 or VCC has excessive overvoltage. Optional to control an external FET switch to discharge VOUT1 excessive overvoltage. OV2_PD output stage has PFET switch pull up with 10Ω $r_{DS(ON)}$ and 10kΩ resistive pull down.
11	11	FB2S	DCDC2 core buck regulator secondary feedback pin for OV and UV monitoring.
12	12	FB2	DCDC2 core buck regulator feedback pin.
13	13	PSTBYB	Input control pin for Power-Off Standby mode. Weak internal pull-up to VDDIO. A logic low activates the pin.
14	14	PWRCTRLB	Input control pin for DeepSTOP mode. Weak internal pull-up to VDDIO. A logic low activates the pin.
15	15	LDOVO4	LDO4 output pin. Connect a 4.7µF capacitor to GND, close to pin.
16	16	LDOVIN3/4	LDO3/4 input pin. Connect a 1µF capacitor to GND, close to pin.
17	17	LDOVO3	LDO3 output pin. Connect a 4.7µF capacitor to GND, close to pin.
18	18	VTR3/4	Tracking reference for LDO3/4 if configured as trackers. Connect a 1µF capacitor to GND close to the pin. If both LDO3 and LDO4 are normal LDO configured, connect this pin to GND.
20	20	LDOVO2	LDO2 output pin. Connect a 4.7µF capacitor to GND close to device pin.
21	21	LDOVIN1/2	LDO1/2 input pin. Connect a 1µF capacitor to GND close to device pin.
22	22	LDOVO1	LDO1 output pin. Connect a 4.7µF capacitor to GND close to device pin.
23	-	COREMON	Monitors an analog voltage of interest in the system. 800mV ±2% reference with two OV and two UV thresholds. If not using the COREMON function, ground this pin.
-	23	NC2	Ground this pin.
24	-	AMUX	MUX output pin that can send out internal analog and digital signals. This pin can be used by the MCU for diagnostic purposes of the PMIC internal circuit status.
25	25	SSPB	Safety defined Secondary safety path output signal. This is an output controlled by the protection digital, capable of indicating to an outside circuit, other than the PMIC or load MCU, that there is an error and to activate a secondary safety path. This pin is push-pull and active low with a 100k internal pull-down to GND. SSPB pin output has 300Ω series resistance to limit the current if SSPB is pulled down externally.
26	26	WDENB	Watchdog enable input and multiple functions pin. It is pulled to GND by a 100k internal pull-down. ▪ Enable/Disable WDT_SST_TIMEOUT timer (see OPT_SST_WDENB_CTRL) ▪ Enable/Disable WDT monitor (see OPT_WDT_WDENB_CTRL) ▪ Used for pin kick when WDT monitor is active (see WDT_PIN_KICK_CTRL and WDT_PIN_KICK_EDGE) ▪ Used as a PGOOD indicator (see WDENB_SEL and OPT_PG_CTRL - 0x20B)
27	27	VMONB	Safety defined digital input designed primarily to work with VMONOUTB signal of RH850 MCU. A logic low asserts the pin and it has a 100k internal pull-down to GND.
28	28	ERRB	Safety defined digital input designed primarily to work with ERROROUT_MB signal of RH850 MCU. A logic low asserts the pin and it has a 100k internal pull-down to GND.
29	29	RSTB	Reset output signal to MCU, push-pull and active low. Assertion of this pin is the main indicator of protection faults and causes the MCU to be held in Reset. This pin has a weak internal pull-down to GND. RSTB pin output has 300Ω series resistance to limit the current if RSTB is pulled down externally.
30	30	INTB	Interrupt output pin to the load MCU, push-pull or open-drain configurable, and active low.

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RAA271084 Pin Number	RAA271084-B Pin Number	Pin Name	Description
31	31	SPISDO	SPI Serial Data Output pin for sending data back to the SPI controller, VDDIO level.
32	32	SPISDI	SPI Serial Data Input pin from the SPI controller. This pin is VDDIO voltage level and has a 100k internal pull-down to GND.
33	33	SPICLK	SPI communication clock pin. This pin is VDDIO voltage level and has a 100k internal pull-down to GND.
34	34	SPICSB	SPI Chip Select select pin. 100k internal pull-up to VDDIO. A logic low activates the pin and begins a SPI transaction.
35	35	VDDIO	IO Power Supply pin used for the SPI interface and other IO pins. Connect a 1µF capacitor to GND close to pin.
36	36	COMP2	Control loop compensation pin for DCDC2. Connect a resistor/capacitor network to ground.
37	37	ISEN2N	Input current sense pin of DCDC2 connected to the negative terminal of the current sense resistor.
38	38	ISEN2P	Input current sense pin of DCDC2 connected to the positive terminal of the current sense resistor.
39	39	BOOT2	Provides connection point for a ceramic boot capacitor providing high-side gate driver supply for DCDC2. The capacitor is charged through an external diode connected to VCCP.
40	40	HS2	Output of DCDC2 high-side MOSFET (M4) gate driver.
41	41	LX2	Connected to the DCDC2 switch node, providing the return path for the high-side MOSFET (M4) gate driver back to BOOT2.
42	42	LS2	Output of DCDC2 low-side MOSFET (M5) gate driver.
43	43	VCCP	Bias supply (5V typical) for MOSFET gate drivers. This pin is connected through an external RC filter to the VCC pin.
44	44	LS1B	Output of DCDC1 low-side MOSFET (M3) gate driver.
45	45	LS1A	Output of DCDC1 low-side MOSFET (M2) gate driver.
46	46	LX1	Connected to the DCDC1 switch node, providing the return path for the high-side MOSFET (M1) gate driver back to BOOT1.
47	47	HS1	Output of DCDC1 high-side MOSFET (M1) gate driver.
48	48	BOOT1	Provides connection point for a ceramic boot capacitor providing high-side gate driver supply for DCDC1. The capacitor is charged through an external diode connected to VCCP.
PAD	PAD	GND	Analog/PGND ground pin.

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3. Specifications

3.1 Absolute Maximum Ratings

***Caution**:* Do not operate above the maximum ratings listed. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VBAT, WAKE1, WAKE2, ISEN1N, ISEN1P, LX1, LDOVO3, LDOVO4	-0.3	45	V
HS1, BOOT1	-0.3	51.5	V
HS2, BOOT2	-0.3	12.5	V
All Other Pins	-0.3	6.5	V
VIN2, FB1, LDOIN1/2 and LDO3/4, pulse width <100µs	-	7.5	V
Maximum Junction Temperature[1]	-	+150	°C
Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per AEC-Q100-002E)	-	2	kV
Charged Device Model (Tested per AEC-Q100-011D) - Corner Pins Only	-	750	V
Charged Device Model (Tested per AEC-Q100-011D) - All Other Pins	-	500	V
Latch-Up (Tested per AEC-Q100-004D; Class 2, Level A)	-	100	mA

1. Operations above the junction temperature of 150°C and up to up to TSD_REG threshold (maximum 180°C) can be sustained by the RAA271084 for a limited duration, but with a degradation of the lifetime. Above TSD_REG threshold (maximum 180°C), the operation of both FuSa and regulation TSDs (TSD_FuSa, TSD_LDO34, and TSD_REG) and full device cannot be guaranteed and can also lead to permanent damage.

3.2 Recommended Operating Conditions

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Parameter	Minimum	Maximum	Unit
Ambient Temperature	-40	+125	°C
Startup Voltage Range, V_{BAT}	4.5	42	V
Battery Voltage Range V_{BAT} after startup	2.7	42	V
FB1, VIN2, LDOVIN1-4	-	5.7	V
Buck DCDC2 Output V_{OUT2}	0.8	5.25	V
LDO0, LDO1, LDO2 Output Capacitor Requirement	2.2	22	µF
LDO3, LDO4 Output Capacitor Requirement (configured as LDO)	2.2	22	µF
LDO3, LDO4 Output Capacitor Requirement and Range (Configured as tracker, includes line capacitance can be supported)	4.7	110	µF

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	48 Ld 7x7 SCQFN Package	θ_{JA}[1]	Junction to ambient	24	°C/W
		θ_{JC}[2]	Junction to case	0.7	
	48 Ld 7x7 LQFP-EP Package	θ_{JA}[1]	Junction to ambient	26	
		θ_{JC}[2]	Junction to case	1.2	

1. θ_{JA} i is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

T_A = -40°C to +125°C and input voltage range (V_{BAT} = 4.5V to 42V) unless specified otherwise.

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Power Supply						
VBAT Startup Voltage	V_{BAT_SU}	VBAT Rising	4.31	4.5	4.67	V
VBAT Shutdown Voltage	V_{BAT_SDN}	VBAT Falling	-	-	2.7	V
VCC POR (Power-On Reset) Voltage	$V_{CC_POR_R}$	VCC Rising	4.07	4.2	4.33	V
VCC Undervoltage Lockout	V_{CC_UVLO}	VCC Falling	3.81	4.0	4.13	V
VCC Undervoltage Lockout Hysteresis	V_{CC_HYST}	-	0.1	0.2	-	V
HV to LV LDO Switchover Threshold	V_{HVLV}	VIN2 Rising	5.36	5.47	5.6	V
HV to LV LDO Switchover Hysteresis	V_{HVLV_HYST}	-	0.055	0.11	-	V
V_{BAT} Supply Current	I_{Q_SD}	PMIC_OFF state. WAKE1 = WAKE2 = 0V	-	4	15	µA
	I_{Q_PSTBY}	Power-Off Standby mode. Current drawn from VBAT includes FET drive current. DCDC1, LDO0 enabled with no load. LDO1-4 and DCDC2 disabled	-	20	-	µA
	I_{Q_DPSTP}	DeepSTOP mode. Current drawn from VBAT includes FET drive current. DCDC1, LDO0, LDO1, LDO2 enabled with no load. DCDC2 and LDO3-4 disabled	-	180	-	µA
	I_{Q_EOT}	EOT only mode, only LDO0 enabled	-	29	60	µA
VCC LDO0 Characteristics						
Input Supply[2]	V_{IN_HVLDO}	V_{IN} = VBAT	5.6	12	42	V
	V_{IN_LVLDO}	V_{IN} = DCDC1	5.415	5.7	5.985	V
LDO0 Output Voltage (VCC)	V_{O_LDO0}	No load	4.75	5	5.25	V
PMIC Operation Current[4]	I_{Q_LDO0}	VBAT = 12V, PMIC operation current drawn from LDO0, in Active mode, exclude FETs driving current	-	10	-	mA
HVLDO Output Current[2]	$I_{O_MAX_HVLD0}$	Current includes gate drive ($Q_g \times f_{SW}$ for all FETs), internal PMIC requirement of 10mA, and any extra load	-	-	130	mA
LVLDO Output Current[2]	$I_{O_MAX_LVLD0}$		-	-	220	mA
LDO0 Warning OV Threshold Accuracy	V_{OV_LDO0}	Nominal Threshold = 4%, 8%, 12%	-2	-	2	%
LDO0 Severe OV Threshold Accuracy	V_{SOV_LDO0}	Nominal Threshold = 10%, 14%	-2	-	2	%
LDO0 Warning UV Threshold Accuracy	V_{UV_LDO0}	Nominal Threshold = -4%, -8%, -12%	-2	-	2	%
LDO0 Severe UV Threshold Accuracy	V_{SUV_LDO0}	Nominal Threshold = -10%, -14%	-2	-	2	%
LDO0 Thermal Shutdown (TSD_REG)[3]	T_{SD0}	Rising Threshold	160	170	180	°C
TSD_REG Hysteresis[3]	T_{SD0HYS}	-	-	15	-	°C

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T_A = -40°C to +125°C and input voltage range (V_{BAT} = 4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
DCDC1 Buck-Boost Controller Characteristics						
Input Supply[2]	V_{IN_DCDC1}	VIN = VBAT	2.7	12	42	V
Output Voltage Range	V_{O_DCDC1}	-	5.60	5.7	5.77	V
Buck-Boost Comparator Threshold	V_{BB}	VBAT rising to enter Buck mode	7.6	7.9	8.26	V
Buck-Boost Comparator Hysteresis	V_{BB_HYS}	VBAT falling to enter Buck-Boost mode	150	300	-	mV
Cycle-by-Cycle Current Limit Voltage Threshold	$V_{OC1_DCDC1_BUCK}$	Voltage across ISENS1 resistor. Buck Mode	45	55	62	mV
	$V_{OC1_DCDC1_BB}$	Voltage across ISENS1 resistor. Buck-boost mode	135	165	202	mV
DCDC1 Soft-Start Time	t_{SS_DCDC1}	OPT_DCDC1_SS_RATE = 10µs/step	-	1.28	-	ms
Dead-Time[3]	T_{DTLH1S}	Low-side low to high-side high	-	25	-	ns
	T_{DTHL1S}	High-side low to low-side high	-	45	-	ns
Max Duty Cycle	T_{DTMAX1}	f_{SW} = 440kHz (ASIL-D only)	98	98.75	-	%
Minimum UG/LG On-Time[3]	T_{MIN_ON1}	-	-	25	-	ns
Minimum UG Off-Time[3]	T_{MIN_OFF1}	-	-	25	-	ns
Warning OV Threshold Accuracy	V_{OV1}	Nominal Threshold = 4%, 6%, 8%	-2	-	2	%
Severe OV Threshold Accuracy	V_{SOV1}	Nominal Threshold = 8%, 10%	-2	-	2	%
Warning UV Threshold Accuracy	V_{UV1}	Nominal Threshold = -4%, -6%, -8%	-2	-	2	%
Severe UV Threshold Accuracy	V_{SUV1}	Nominal Threshold = -8%, -10%	-2	-	2	%
Boot Refresh Threshold	V_{BTRFR1}	Boot voltage falling	3.2	3.4	3.6	V
Boot Refresh Threshold Hysteresis	V_{BTRFR1_HYS}	-	50	-	-	mV
Boot Refresh LG On-Time	T_{BTRFR1_ON}	-	130	180	220	ns
DCDC2 Buck Controller Characteristics						
Input Supply[2]	V_{IN2}	-	5.415	5.7	5.985	V
Reference Voltage	V_{FB2}	-	0.788	0.8	0.812	V
FB2 Pin Leakage Current	I_{FB2}	-	-	-	1.3	µA
Cycle-by-Cycle Current Limit Voltage Threshold	V_{OC1_2}	Voltage across ISENS2 resistor.	25	32	39	mV
Overcurrent Protection Limit Voltage Threshold	V_{OC2_2}	Voltage across ISENS2 resistor. OC2 tracks OC1 and is always higher than OC1.	32	40	48	mV
Cycle-by-Cycle Negative Current Limit Voltage Threshold	V_{NOC_2}	Voltage across ISENS2 resistor	-22.4	-16	-9.6	mV
Dead-Time[3]	T_{DTLH2S}	Low-side low to high-side high	-	25	-	ns
	T_{DTHL2S}	High-side low to low-side high	-	45	-	ns
Max Duty Cycle	T_{DTMAX2}	VIN2 = 5.7V, f_{SW} = 440kHz (ASIL-D only)	98	98.75	-	%

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T_A = -40°C to +125°C and input voltage range (V_{BAT} = 4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Minimum UG/LG On-Time[3]	Tmin_on2	-	-	25	-	ns
Minimum UG Off-Time[3]	Tmin_off2	-	-	25	-	ns
DCDC2 Soft-Start Time	t_{SS}	Internal ramp time from 100mV to 1V	-	1.28	-	ms
Error Amp Transconductance (gm)[3]	GM_{EA}	-	-	1.7	-	mS
Warning OV Threshold Accuracy	V_{OV2}	Nominal Threshold = 4%, 8%, 12%	-2	-	2	%
Severe OV Threshold Accuracy	V_{SOV2}	Nominal Threshold = 10%, 14%	-2	-	2	%
Warning UV Threshold Accuracy	V_{UV2}	Nominal Threshold = -4%, -8%, -12%	-2	-	2	%
Severe UV Threshold Accuracy	V_{SUV2}	Nominal Threshold = -10%, -14%	-2	-	2	%
Boot Refresh Threshold	V_{BTRFR2}	Boot voltage falling	3.2	3.4	3.6	V
Boot Refresh Threshold Hysteresis	V_{BTRFR2_HYS}	-	50	-	-	mV
Boot Refresh LG On-Time	T_{BTRFR2_ON}	-	130	180	220	ns
DCDC[1-2] Output Driver Characteristics						
High-Side Source Current[3]	I_{HS_SRC}	Simulation condition V_{HS} - V_{LX} = 2.5V, V_{BOOT} - V_{LX} = 4.4V	-	0.95	-	A
High-Side Source Resistance[3]	R_{HS_SRC}	100mA source current, V_{BOOT} - V_{LX} = 4.4V	1.68	2.13	4.27	Ω
High-Side Sink Current[3]	I_{HS_SNK}	Simulation condition V_{HS} – V_{LX} = 2.5V, V_{BOOT} – V_{LX} = 4.4V	-	1.35	-	A
High-Side Sink Resistance[3]	R_{HS_SNK}	100mA sink current, V_{BOOT} - V_{LX} = 4.4V	0.67	0.78	1.2	Ω
Low-Side Source Current[3]	I_{LS_SRC}	Simulation condition V_{LS} - V_{GND} = 2.5V, VCCP = 5V	-	0.97	-	A
Low-Side Source Resistance[3]	R_{LS_SRC}	100mA source current, VCCP = 5V	1.4	1.64	2.7	Ω
Low-Side Sink Current[3]	I_{LS_SNK}	Simulation condition V_{LS} - V_{GND} = 2.5V, VCCP = 5V	-	1.73	-	A
Low-Side Sink Resistance[3]	R_{LS_SNK}	100mA sink current, VCCP = 5V	0.67	0.8	1.2	Ω
LDO[1-2] Linear Regulator Characteristics						
Input Supply[2]	V_{IN_LDO12}	Connection to V_{O_DCDC1}	5.415	5.7	5.985	V
Output Voltage	V_{O_LDO12}	5V Setting, I_{LOAD} = 1mA to 350mA LDOIN1/2 = 5.7V	4.925	5	5.075	V
		3.3V Setting, I_{LOAD} = 1mA to 350mA	3.2505	3.3	3.3495	V
LDO[1-2] Quiescent Current	$I_{Q_LDO12_EN}$	LDO enabled, no load	-	100	-	µA
	$I_{Q_LDO12_DIS}$	LDO disabled	-	0	-	µA
Maximum Output Load[2]	$I_{O_MAX_LDO12}$	-	-	-	350	mA
Current Limit	I_{LIM_LDO12}	-	360	-	-	mA

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T_A = -40°C to +125°C and input voltage range (V_{BAT} = 4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Dropout Voltage	V_{DO_LDO12}	I_{LOAD} = $I_{O_MAX_LDO12}$, 3.3V setting	-	-	390	mV
DC Power Supply Rejection Ratio[4]	$PSRR_{LDO12}$	V_{IN_LDO12} = 5.7V ±3%, V_{O_LDO12} = 5V, C_{O_LDO12} = 4.7µF	-	-80	-	dB
		V_{IN_LDO12} = 5.0V ±3%, V_{O_LDO12} = 3.3V, C_{O_LDO12} = 4.7µF	-	-80	-	dB
Load Transient Response[4]	ΔV_{TR_LDO12}	I_{LOAD} = 0 to $I_{O_MAX_LDO12}$, C_{O_LDO12} = 4.7µF, C_{ESR} = 10mΩ	-	-	12	mV
Output Pull-Down Resistance	R_{PD_LDO12}	LDO disabled	-	100	140	Ω
Warning OV Threshold Accuracy	V_{OV_LDO12}	Nominal Threshold = 4%, 8%, 12%	-2	-	2	%
Severe OV Threshold Accuracy	V_{SOV_LDO12}	Nominal Threshold = 10%, 14%	-2	-	2	%
Warning UV Threshold Accuracy	V_{UV_LDO12}	Nominal Threshold = -4%, -8%, -12%	-2	-	2	%
Severe UV Threshold Accuracy	V_{SUV_LDO12}	Nominal Threshold = -10%, -14%	-2	-	2	%
LDO[3-4] Tracker/Linear Regulator Characteristics						
Input Supply[2]	V_{IN_LDO34}	Connection to V_{O_DCDC1}	5.415	5.7	5.985	V
Output Voltage	V_{O_LDO34}	LDO mode, 5V Setting, 1-200mA load LDOIN3/4 = 5.7V	4.925	5	5.075	V
		LDO mode, 3.3V Setting, 1 to 200mA load	3.2505	3.3	3.3495	V
DC Voltage Accuracy	$V_{O_LDO34_ACC}$	LDO Mode (Tracking disabled), at $I_{O_MAX_LDO34}$	-2	-	+2	%
		Tracking enabled, output tracks VTR3/4 pin input, at $I_{O_MAX_LDO34}$	-10	-	+10	mV
Maximum Output Load[2]	$I_{O_MAX_LDO34}$	-	-	-	200	mA
Current Limit	I_{LIM_LDO34}	-	210	-	-	mA
Dropout Voltage	V_{DO_LDO34}	I_{LOAD} = $I_{O_MAX_LDO34}$	-	-	390	mV
DC Power Supply Rejection Ratio[4]	$PSRR_{LDO34}$	V_{IN_LDO34} = 5.7V ±3%, V_{O_LDO34} = 5V, C_{O_LDO34} = 4.7µF	-	-80	-	dB
		V_{IN_LDO34} = 5.0V ±3%, V_{O_LDO34} = 3.3V, C_{O_LDO34} = 4.7µF	-	-80	-	dB
Output Pull-Down Resistance	R_{PD_LDO34}	LDO disabled	60	100	155	Ω
Load Transient Response[4]	ΔV_{TR_LDO34}	Tracker mode, I_{LOAD} = 0 to $I_{O_MAX_LDO34}$, C_{O_LDO34} = 4.7µF, C_{ESR} = 10mΩ	-	-	20	mV
Warning OV Threshold Accuracy	$OVTH_{LDO34}$	Nominal Threshold = 4%, 8%, 12%	-2	-	2	%
Severe OV Threshold Accuracy	$SOVTH_{LDO34}$	Nominal Threshold = 10%, 14%	-2	-	2	%
Warning UV Threshold Accuracy	$UVTH_{LDO34}$	Nominal Threshold = -4%, -8%, -12%	-2	-	2	%

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T_A = -40°C to +125°C and input voltage range (V_{BAT} = 4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Severe UV Threshold Accuracy	$SUVTH_{LDO34}$	Nominal Threshold = -10%, -14%	-2	-	2	%
VTR3/4 Undervoltage Fault[3]	V_{TRUV}	Tracker enabled	-	2.2	-	V
LDO3/4 Thermal Shutdown (TSD_LDO34)[3]	T_{SD34}	Rising Threshold	150	160	170	°C
TSD_LDO34 Hysteresis[3]	$T_{SD34HYS}$	-	-	10	-	°C
Oscillator and Spread Spectrum Characteristics						
Switching Frequency	f_{SWL}	440kHz setting (ASIL-D only)	396	440	484	kHz
	f_{SWH}	2.2MHz setting[3]	1.98	2.2	2.42	MHz
Spread Spectrum Frequency Range[3]	f_{SS}	-	-	4.6	-	%
Engine Off Timer (EOT) Oscillator Characteristics						
EOT Clock Switching Frequency	f_{OSCEOT}	-	-	32768	-	Hz
EOT Time Accuracy	t_{EOT}	-	-5	-	5	%
Input Pin Characteristics						
WAKE1/2 Input Low Voltage Threshold	V_{IL_WAKE}	-	-	-	0.4	V
WAKE1/2 Input High Voltage Threshold	V_{IH_WAKE}	-	1.4	-	-	V
WAKE1/2 Internal Pull-Down Impedance	R_{PD_WK}	-	-	20	-	MΩ
PSTBYB, PWRCTRLB, ERRB, VMONB, WDENB Input Low Voltage Threshold	V_{IL}	-	-	-	0.3×VDDIO	V
PSTBYB, PWRCTRLB, ERRB, VMONB, WDENB Input High Voltage Threshold	V_{IH}	-	0.7×VDDIO	-	-	V
PSTBYB, PWRCTRLB Internal Pull Up Impedance	R_{PU_PWR}	-	-	50	-	MΩ
ERRB, VMONB, WDENB Internal Pull Down Impedance	R_{PD_WD}	-	-	100	-	kΩ
Output Pin Characteristics						
RSTB, SSPB, INTB Low Voltage Output	V_{OL}	1mA load. INTB configured as push/pull	-	0.3	0.6	V
RSTB, SSPB, INTB High Voltage Output	V_{OH}	1mA load. INTB configured as push/pull	VDDIO-0.6	VDDIO-0.3	-	V
INTB Low Voltage Output[3]	V_{OL_OD}	INTB configured as open drain	-	0.3	0.6	V
SSPB Internal Pull-Down Impedance[3]	-	-	-	100	-	kΩ
SSPB, RSTB Series Resistance[3]	-	Internal series resistor between output driver and pad	-	300	-	Ω
OV2_PD Pull-Down Impedance	R_{PD_OV2}	-	-	10	-	kΩ
OV2_PD Output High Voltage	V_{OH_OV2}	-	-	4.25	-	V
SPI Interface						
SPI Frequency Capability[2]	-	-	-	-	8	MHz
SPI Input Low Voltage Threshold	V_{IL}	-	-	-	0.3×VDDIO	V

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T_A = -40°C to +125°C and input voltage range (V_{BAT} = 4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
SPI Input High Voltage Threshold	V_{IH}	-	0.7×VDDIO	-	-	V
SPICSB Internal Pull Up Impedance	R_{PU_SPI}	-	-	100	-	kΩ
SPICLK, SPISDI Internal Pull Down Impedance	R_{PD_SPI}	-	-	100	-	kΩ
SPISDO Low Voltage Output	V_{OL}	-	-	0.3	0.6	V
SPISDO High Voltage Output	V_{OH}	-	VDDIO-0.6	VDDIO-0.3	-	V
Functional Safety Monitors						
FuSa Bandgap Voltage	V_{FBG}	-	1.221	1.233	1.246	V
Bandgap Compare Fault	V_{FBGF}	-	7	10	14	%
Main Clock Over Frequency	f_{OF}	-	35	50	65	%
Main Clock Under Frequency	f_{UF}	-	35	50	65	%
GND Disconnect Fault Threshold	V_{GND_DIS}	-	-	250	-	mV
VCC OV2_PD Overvoltage Fault	V_{VCC_OV2}	VCC Rising	5.96	6.2	6.43	V
FB1 OV2_PD Overvoltage Fault	V_{FB1_OV2}	FB1 (DCDC1 Output) Rising	6.6	7	7.45	V
FuSa Thermal Shutdown (TSD_FuSa)[3]	T_{FS}	Rising Threshold	150	160	170	°C
TSD_FuSa Hysteresis[3]	T_{FSHYS}	-	-	20	-	°C
COREMON OV Threshold Accuracy (ASIL-D only)	V_{COV}	Nominal values: 4%, 8%, 12%	-2	-	2	%
COREMON Severe OV Threshold Accuracy (ASIL-D only)	V_{CSOV}	Nominal values: 10%, 14%	-2	-	2	%
COREMON UV Threshold Accuracy (ASIL-D only)	V_{CUV}	Nominal values: -4%, -8%, -12%	-2	-	2	%
COREMON Severe UV Threshold Accuracy (ASIL-D only)	V_{CSUV}	Nominal values: -10%, -14%	-2	-	2	%

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1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Test condition but not parameter limits.
3. Limits are assured by design or bench test only.
4. Bench tested only.

4. Typical Performance Graphs

V_{BAT} = 12V, T_A = 25°C, V_{O_DCDC1} = V_{IN2} = 5.7V, unless specified otherwise.

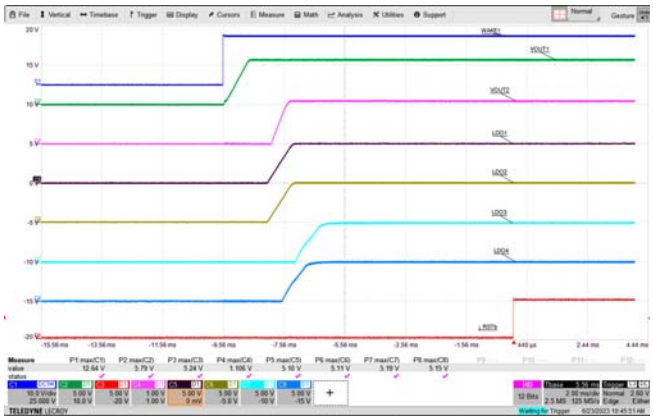


Figure 5. System Startup by Toggling WAKE1 Pin High

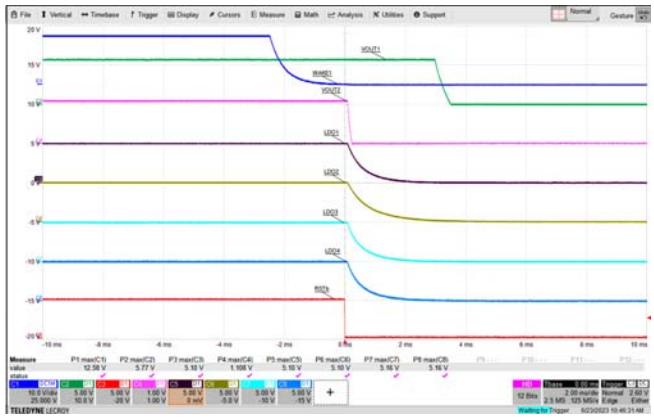


Figure 6. System Shutdown by Toggling WAKE1 Pin Low

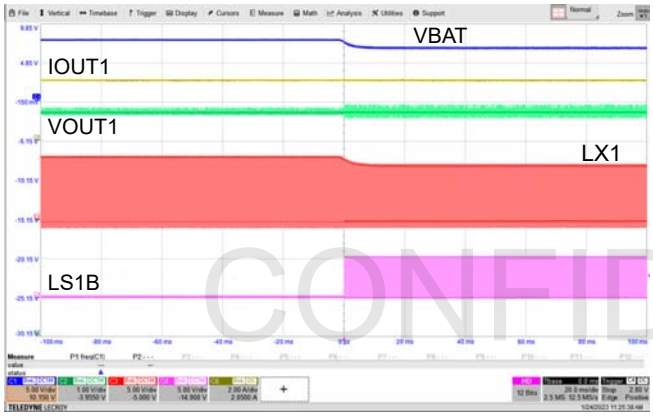


Figure 7. VBAT Ramping Down, DCDC1 Buck to Buck-Boost Mode Transition



Figure 8. VBAT Ramping Up, DCDC1 Buck-Boost to Buck Mode Transition



Figure 9. DCDC1 Load Transient VBAT = 12V, VOUT1 = 5.7V, f_{SW} = 2.2MHz, 0A to 3A



Figure 10. DCDC2 Load Transient VIN2 = 5.7V, VOUT2 = 1.09V, f_{SW} = 2.2MHz, 0.5A to 4A

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V_{BAT} = 12V, T_A = 25°C, V_{O_DCDC1} = V_{IN2} = 5.7V, unless specified otherwise.

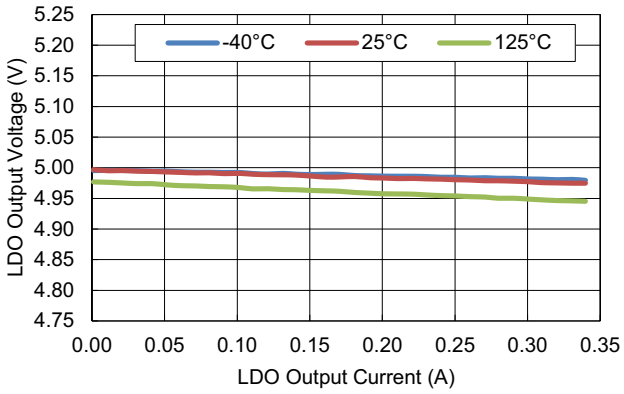


Figure 11. LDO1/LDO2 Load Regulation, 5V Output

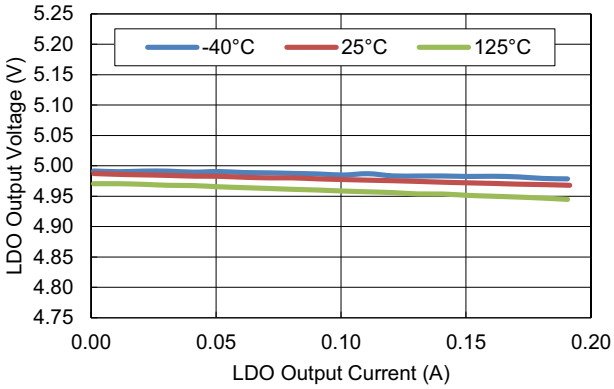


Figure 12. LDO3/LDO4 Load Regulation, 5V Output

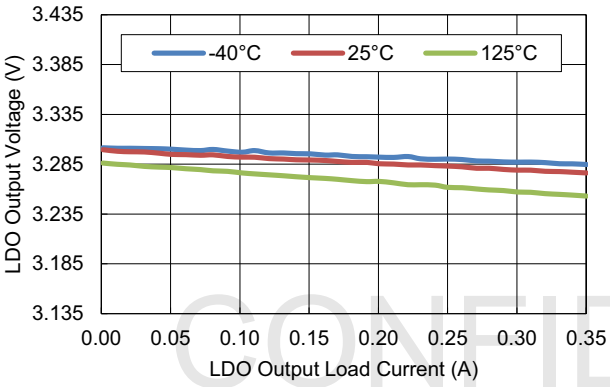


Figure 13. LDO1/LDO2 Load Regulation, 3.3V Output

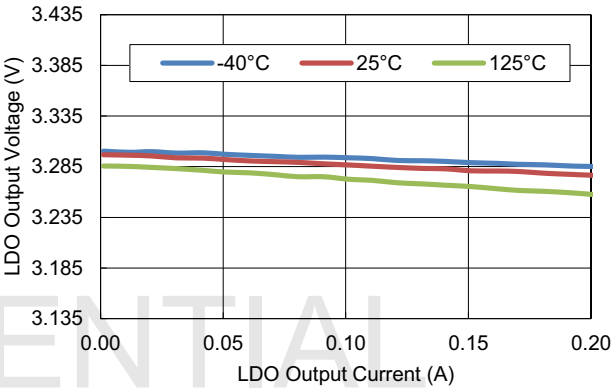


Figure 14. LDO3/LDO4 Load Regulation, 3.3V Output

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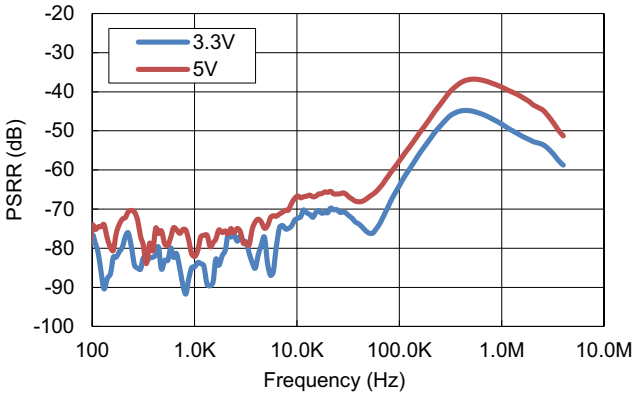


Figure 15. LDO1/LDO2 PSRR vs Frequency, 175mA Load

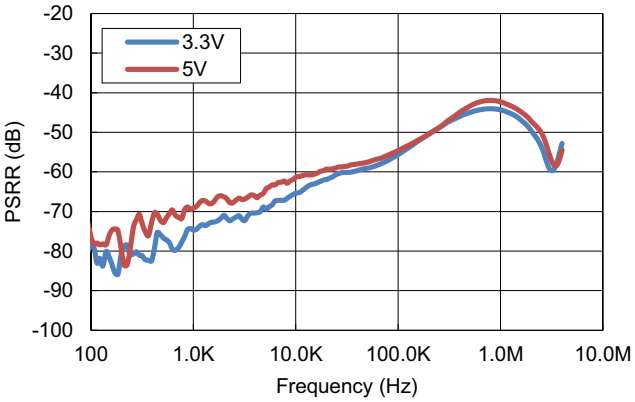


Figure 16. LDO3/LDO4 PSRR vs Frequency, 100mA Load

V_{BAT} = 12V, T_A = 25°C, V_{O_DCDC1} = V_{IN2} = 5.7V, unless specified otherwise.

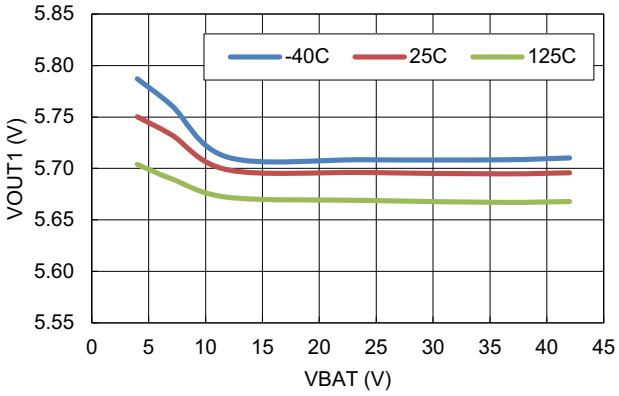


Figure 17. DCDC1 Line Regulation, f_{SW} = 2.2MHz, Load = 3A

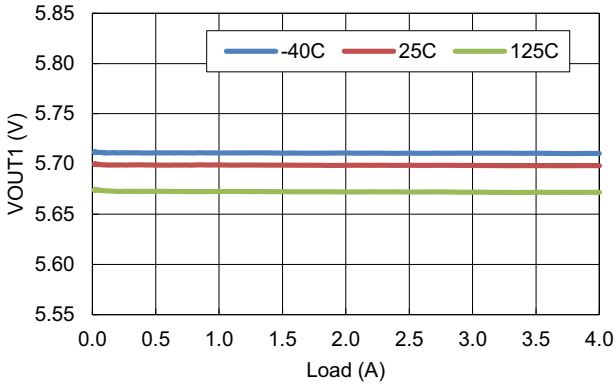


Figure 18. DCDC1 Load Regulation, f_{SW} = 2.2MHz, V_{BAT} = 12V

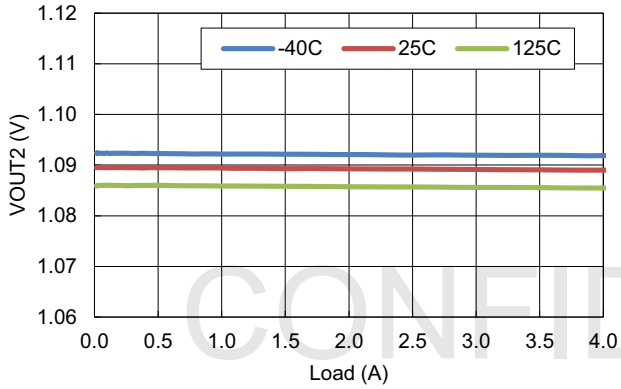


Figure 19. DCDC2 Load Regulation, VOUT2 = 1.09V, f_{SW} = 2.2MHz, V_{IN2} = 5.7V

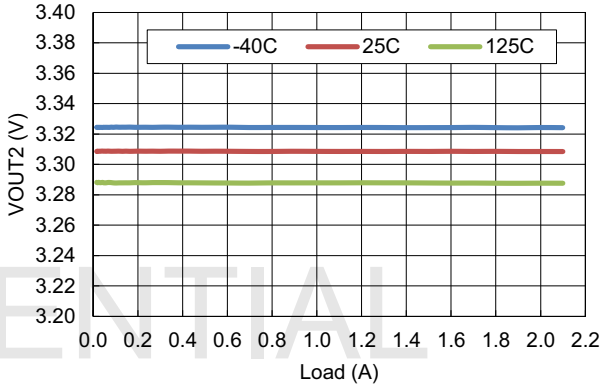


Figure 20. DCDC2 Load Regulation, VOUT2 = 3.3V, f_{SW} = 2.2MHz, V_{IN2} = 5.7V

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5. Functional Description

5.1 Operation of the PMIC

5.1.1 PMIC States

Logic in the PMIC controls operation of DCDC1, DCDC2, and LDOs 1-4 and responds to WAKE, PSTBYB, and PWRCTRLB signals to sequence the PMIC into different operational states. Supplying VBAT > V_{BAT_SU} threshold and either the WAKE pin high begins the PMIC start-up sequence.

Figure 21 shows the overall operational flow of the PMIC. For each state, it shows regulator conditions and output levels of the RSTB and SSPB pins. The following descriptions describe behavior in each of these states.

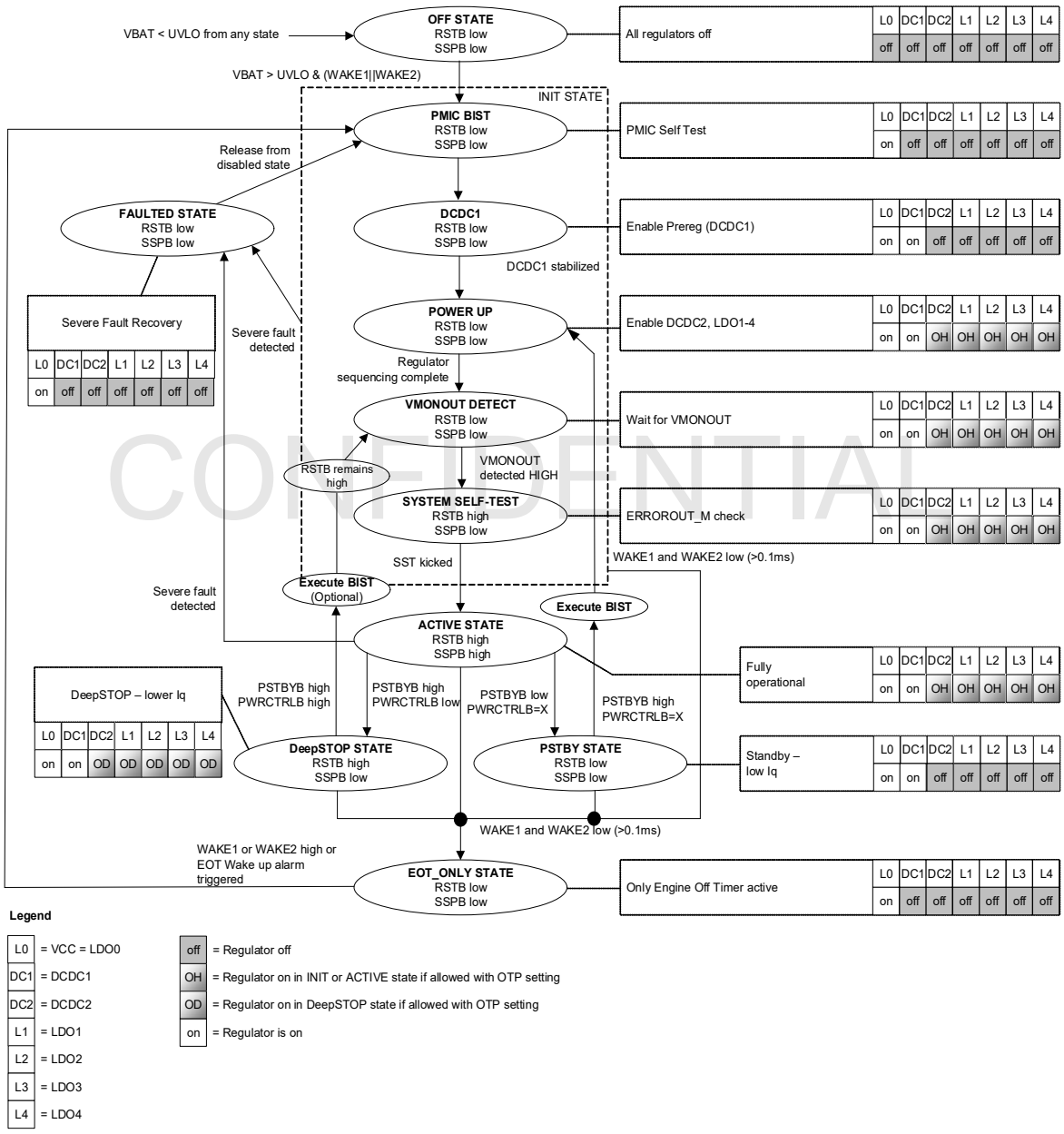


Figure 21. PMIC Operational Diagram

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5.1.2 PMIC Operational Table

Table 1 summarizes the operational states and controls for the PMIC.

Table 1. PMIC Operational Table[1]

VBAT > V_{BAT_SU}	WAKE1 || WAKE2	PSTBYB	PWRCTRLB	EOT	LDO0	DCDC1	DCDC2	LDO1-4	RSTB	SSPB	PMIC State
No	X	X	X	OFF	OFF	OFF	OFF	OFF	Low	Low	OFF
Yes	0→1	X	X	[2]	ON	OFF	OFF	OFF	Low	Low	INIT/PMIC BIST
Yes	1	X	X	[2]	ON	ON	OFF	OFF	Low	Low	INIT/DCDC1
Yes	1	X	X	[2]	ON	ON	OH	OH	Low	Low	INIT/POWER UP
Yes	1	X	X	[2]	ON	ON	OH	OH	Low	Low	INIT/ VMONOUT DETECT
Yes	1	X	X	[2]	ON	ON	OH	OH	High	Low	INIT/SYSTEM SELF-TEST
Yes	1	1	1	[2]	ON	PWM	OH	OH	High	High	ACTIVE
Yes	1	1	0	[2]	ON	AUTO	OD	OD	High	Low	DeepSTOP
Yes	1	0	X	[2]	ON	PFM	OFF	OFF	Low	Low	PSTBY
Yes	1→0	X	X	[2]	ON	OFF	OFF	OFF	Low	Low	EOT_ONLY
Yes	1	X	X	[2]	ON	OFF	OFF	OFF	Low	Low	DISABLED

1. The following helps
   OFF = Regulator off
   ON = Regulator on
   PWM = DCDC1 in forced PWM mode (high power)
   AUTO = DCDC1 automatically selects PWM/PFM mode based on load
   PFM = DCDC1 in forced PFM mode (lowest power)
   OH = Regulator on in INIT and ACTIVE if enabled with OTP programming
   OD = Regulator on in DeepSTOP if enabled with OTP programming
2. EOT must be initially configured and enabled using SPI control from host. When enabled, the EOT continuously runs until VBAT < V_{BAT_SDN}.

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5.1.3 OFF State

VBAT < V_{BAT_SDN} during any state forces an immediate disabling of all PMIC rails. The engine off timer is reset in the OFF state and SPI target communication is disabled.

5.1.4 INIT State

The INIT state is a series of steps which handle start up sequencing between the OFF and ACTIVE STATES when VBAT and WAKE are applied to the PMIC.

- VBAT > V_{BAT_SU} and either WAKE high enables LDO0 power up.
- LDO0 stabilizes, internal oscillators are started, and the PMIC executes self-test [PMIC BIST step].
- DCDC1 is started and stabilizes [DCDC1 step].
- Application regulators are started and stabilized. Regulators used and sequencing order are OTP optional [POWER UP step].
- Wait for the VMONB input high (OTP optional) and assert RSTB high [MCU VMONOUT DETECT step].
- System self-test timer is automatically started using OTP optional timeouts. [SYSTEM SELF-TEST step].
- System self-testing. Can be executed in any order.
  - Wait for high assertion of ERROROUT_M (OTP optional)
  - SPI interface checking (application optional)

- Pin checking (application optional)

- SPI write to the EXIT_SST bit (SST kick) to prevent a system self-test timeout fault (OTP optional).

The application optional steps above for SPI interface checking and Pin checking use PMIC resources to support end-to-end signal integrity checking in an application between the PMIC and host. This is coordinated by the SPI controller to allow software flexibility.

Successful completion of the SYSTEM SELF-TEST step in the INIT State transitions the PMIC into ACTIVE state and SSPB is asserted high. The description above assumes no faults or exceptions in the startup process.

The engine off and watchdog timer features by default are not enabled and must be enabled by a SPI controller to configure the features as required. SPI communication is available during the INIT STATE.

5.1.5 ACTIVE State

When in ACTIVE state, the PMIC can respond to requests for DeepSTOP and Power-off Standby states as indicated by the PWRCTRLB and PSTBYB inputs. ACTIVE STATE is the only PMIC state considered trusted due to all safety mechanisms being fully active and all enabled supplies not responding to a fault. This trusted state is indicated by the SSPB pin output driven to a high level.

5.1.6 DeepSTOP State

Entry into DeepSTOP is only permitted after successful entry into ACTIVE state. Transition occurs when PSTBYB remains high and PWRCTRLB is asserted low. Regulators that remain enabled during DeepSTOP state are OTP selectable. Functional safety monitors are disabled during DeepSTOP state to conserve power. ERRB and VMONB monitors are also disabled.

Setting PWRCTRLB high is a request to return to ACTIVE state. When high, the PMIC sequences application supplies back on, performs VMONOUT checks, and transitions back to the SYSTEM SELF-TEST step. The final transition into ACTIVE is allowed after the SYSTEM SELF-TEST steps are completed.

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Regulators intended to be left on during DeepSTOP mode are DCDC1, LDO1, and LDO2. DCDC1's PFM mode is enabled in DeepSTOP mode. With DCDC1, LDO1, and LDO2 enabled and no load on their outputs, the typical current draw from VBAT is approximately 160uA. LDO3 and LDO4 are not low Iq regulators and are not intended to be used in DeepSTOP mode. LDO3 and LDO4 have short-to-battery and short-to-GND protection which require a charge pump for the gate drive of the pass FET. If either LDO3 or LDO4 are enabled in DeepSTOP, VBAT current increases by 4mA to operate the charge pump.

5.1.7 Power-Off Standby (PSTBY) State

Entry into PSTBY is only permitted after successful entry into ACTIVE state. Transition occurs when pin PSTBYB is asserted low. All application regulators (DCDC2, LDO1 through LDO4) are disabled. DCDC1 remains active in PFM mode and LDO0 remains active in the PSTBY state. Functional safety monitors, ERRB monitor, and VMONB monitor are disabled during PSTBY state to conserve power.

Setting pin PSTBYB high is a request to restart the application supplies. When high, the PMIC transitions back to the POWER UP step to sequence application supplies on.

5.1.8 EOT_ONLY State

During INIT, ACTIVE, DeepSTOP, and PSTBY states, the PMIC immediately transitions into EOT_ONLY if both WAKE inputs are held low for greater than 100µs. The engine off timer remains enabled if previously programmed and all regulators are off except for LDO0. The PMIC_OFF bit of the PWR_MODE_CTRL register (Bit 0) must be set to 0 to enter EOT_ONLY state. Functional safety monitors, ERRB monitor, and VMONB monitor are disabled during EOT_ONLY state to conserve power. Bringing either WAKE pin high or an EOT wakeup alarm trigger transitions the PMIC back to the INIT state for restart.

IMPORTANT: If WAKE1 is hardwired high (such as to a battery), register 0x40[2:1] must be set to 2 before entering EOT_ONLY mode. This sets WAKE1 low internal to the PMIC and ignores the connection at the pin. If WAKE2 is already low at this point, the PMIC enters EOT_ONLY mode immediately on execution of the SPI write.

If WAKE2 is high, bringing WAKE2 low following the SPI write puts the PMIC into EOT_ONLY mode. Bringing WAKE2 high or an EOT wakeup alarm trigger transitions the PMIC back to the INIT state for restart.

5.1.9 PMIC_OFF State

During INIT, ACTIVE, DeepSTOP, and PSTBY states, the PMIC immediately transitions into PMIC_OFF state if both WAKE inputs are held low for greater than 100µs and Bit 0 of the PWR_MODE_CTRL register is written to 1. PMIC_OFF state is a low power mode, which shuts down all regulators including LDO0. This disables all regulators and effectively shuts down the PMIC into a non-powered state. All register settings are cleared.

Setting either WAKE1 or WAKE2 high transitions the PMIC back to the INIT state for restart.

5.1.10 FAULTED State

Faulted state is reserved for serious fault handling because it disables all application regulators and DCDC1. LDO0 remains on. OTP-selectable fault cases are available to program which faults trigger transition into the FAULTED state. The method for exiting FAULTED is OTP programmable to either automatic retry or WAKE pin-controlled options as described in the Register Map.

5.2 Timing Summary

5.2.1 Startup Timing

VBAT, WAKE1, and WAKE2 enable or start the PMIC. With VBAT > V_{BAT_SU} voltage applied, either WAKE1 or WAKE2 high begins the start-up sequence. LDO0 (VCC) is enabled first followed by DCDC1 (5.7V VPREREG). DCDC2, LDO1-4 usage is selected by OTP OPT_HP_X_DIS bits.

Figure 22 shows nominal PMIC start up timing when WAKE rises.

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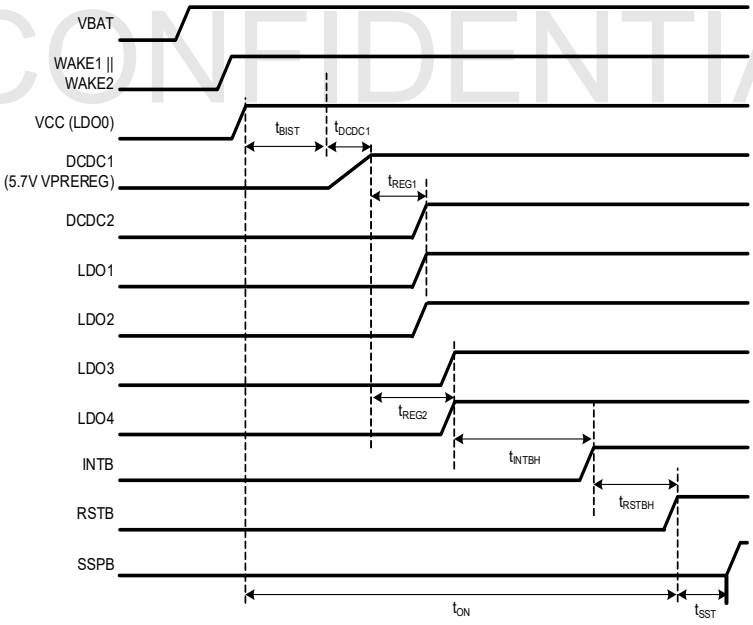


Figure 22. Nominal Startup Timing from Power-Up

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
PMIC Self Test	t_{BIST}	PMIC OTP read, self test of internal logic and safety mechanisms	-	3	-	ms
DCDC1 Start Up	t_{DCDC1}	DCDC1 start up and stabilization	-	1	-	ms
DCDC2, LDO1-4 Start Up	t_{REG1}	DCDC2, LDO1, LDO2 start up with all slot timings set to 0	-	1.5	-	ms
LDO3-4 Start Up	t_{REG2}	LDO3, LDO4 start up 500µs after LDO1, LDO2	-	2	-	ms

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
Regulators ON to INTB High	t_{INTBH}	LDO3, LDO4 configured as LDO	-	3	-	ms
		LDO3, LDO4 configured as tracker	-	5	-	ms
DCDC2, LDO1-4 on to RSTB High	t_{RSTBH}	OPT_RSTB_DLY programmed delay. Time from INTB to RSTB asserted high. 0, 1.5ms, 2ms, and 5ms available settings.	0	-	5	ms
System Self-Test	t_{SST}	Programmable system self-test time	0	-	65	s
Start Up to RSTB High	t_{ON}	Zero slot timing and OPT_RSTB_DLY = 1.5ms. LDO3, LDO4 configured as LDO	-	10	-	ms
		Zero slot timing and OPT_RSTB_DLY = 1.5ms. LDO3, LDO4 configured as tracker	-	12	-	ms

5.2.2 EOT_ONLY State Entry/Exit Timing

Figure 23 shows the entry/exit timing for EOT_ONLY mode when both WAKE pins are low. *Note*: The PMIC follows the disable sequence fully and ignores WAKE signals for a programmed $t_{WAKE_RESTART}$ period after the shutdown request. Also, on exit from EOT_ONLY mode, since VCC is already on the BIST runs in the background as DCDC1 and the other regulators are coming back on, allowing the system to come up as quickly as possible from EOT_ONLY mode.

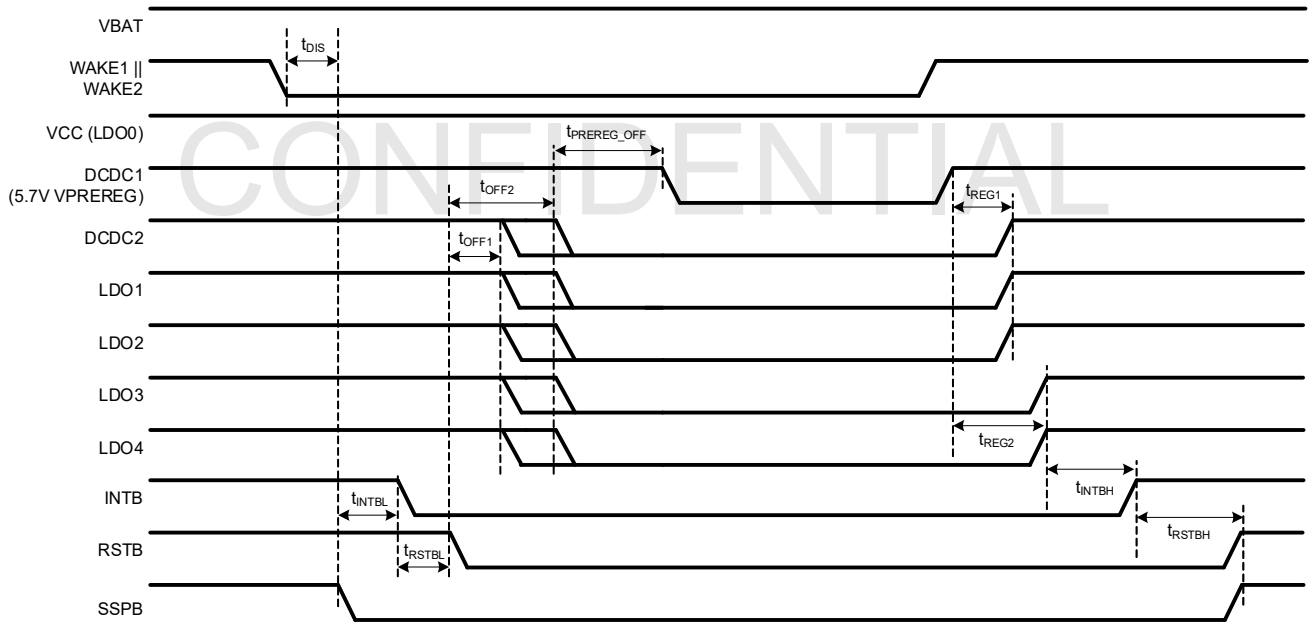


Figure 23. EOT Entry/Exit Timing

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
WAKE low period	t_{DIS}	Minimum period for both WAKE signals low before PMIC disable	-	100	-	µs
INTB low assertion	t_{INTBL}	Disable response to INTB low assertion	-	1	-	ms
RSTB low assertion	t_{RSTBL}	RSTB low assertion after INTB low assertion	-	100	-	µs

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Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
Regulator off delay	t_{OFF1}, t_{OFF2}	RSTB low to regulator disable period. Applies to DCDC1, LDO1-4. Delay selected with OPT_TOFF_DLY_X bits.	0.1	-	1	ms
DCDC2, LDO1-4 to DCDC1 disable time	t_{PREREG_OFF}	DCDC1 switching hangover period after DCDC2, LDO1-4 regulators are disabled.	0	3	-	ms

5.2.3 DeepSTOP Entry/Exit

The PMIC responds to low power state commands using the PWRCTRLB and PSTBYB inputs. PWRCTRLB controls the low power state entry and exit as shown in Figure 24. The PSTBYB input should remain high. DCDC2, LDO1-4 regulator usage in DeepSTOP is selected by OTP bits OPT_DS_X_DIS. These OTP settings are distinct from the OPT_HP_X_DIS bits and are used to allow a subset of regulators to remain active in DeepSTOP state.

When PMIC enters DeepSTOP mode, it disables the regulators that are programmed as disabled in the OPT_DS register. If register 0x20E specified VDDIO pin connection rail is one of these disabled rails, the PMIC recognizes the PWRCTRLB pin as low internally. Therefore, even if PWRCTRLB pin is toggled high externally, the PMIC remains in DeepSTOP mode, unless register 0x20E specified the VDDIO pin connection rail is enabled. In this case, a rising-edge with a pulse-width of at least 60µs at the WAKE2 pin brings the PMIC out of the DeepSTOP mode.

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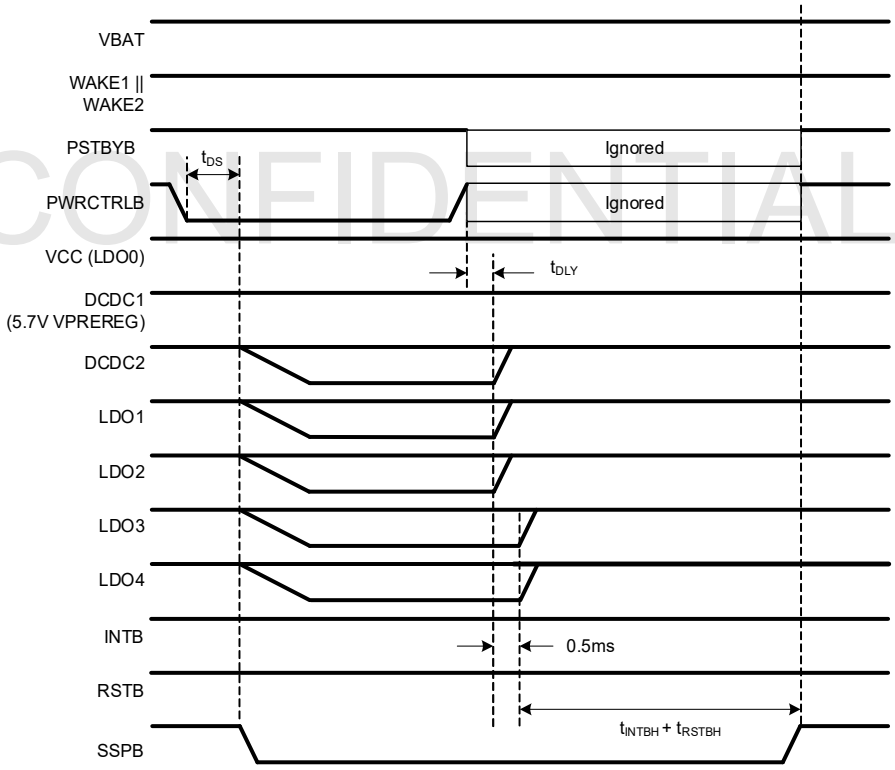


Figure 24. DeepSTOP Entry/Exit

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
PWRCTRL low period	t_{DS}	Minimum PWRCTRL low period to enter DeepSTOP state	-	10	-	µs
Low Iq start-up delay	t_{DLY}	Time from low-Iq mode exit to regulator slot 0 start-up	-	50	-	µs

5.2.4 PSTBY Entry/Exit

The lowest PMIC power state is controlled using the PMIC PSTBYB input set low. PWRCTRLB is ignored in this case. DCDC2, LDO1-4 regulators are disabled and DCDC1 remains enabled in power-off standby (PSTBY) state. The engine off timer continues to run. Figure 25 shows the PSTBY entry and exit.

When PMIC enters PSTBY mode, it disables all the regulators except DCDC1 and LDO0. If register 0x20E specifies that the VDDIO pin connection rail is one of these disabled rails, the PMIC recognizes the PSTBYB pin as low internally. Therefore, even if the PSTBYB pin is toggled high externally, the PMIC remains in PSTBY mode, unless register 0x20E specifies the VDDIO pin connection rail is enabled. In this case, a rising-edge with a pulse-width of at least 60µs at the WAKE2 pin brings the PMIC out of the PSTBY mode.

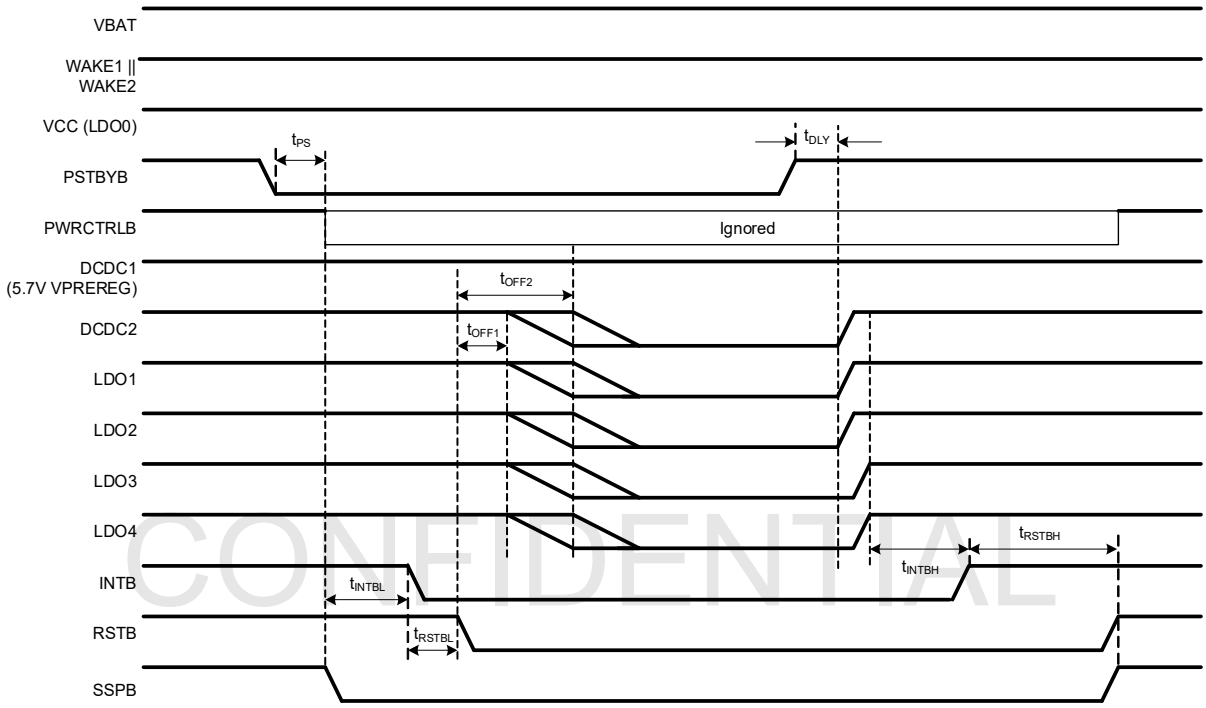


Figure 25. PSTBY Entry/Exit

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
PSTBY low period	t_{PS}	Minimum PSTBY low period to enter PSTBY state	-	10	-	µs

5.2.5 Regulator Output Discharge Wait Time

DCDC1, DCDC2, and LDO1-4 have OTP programmable output discharge wait times controlled by the OPT_*_WAIT_DISCG settings. Depending on application requirements, internal pull-down devices can be enabled to assist with output discharge and the PMIC delays the restart of the regulator output until the timer expires. The OPT_*_WAIT_DISCG selection has priority over pin and SPI-based enables to ensure proper discharge times. Figure 26 shows an example with different discharge wait times for DCDC1, DCDC2, and LDOs.

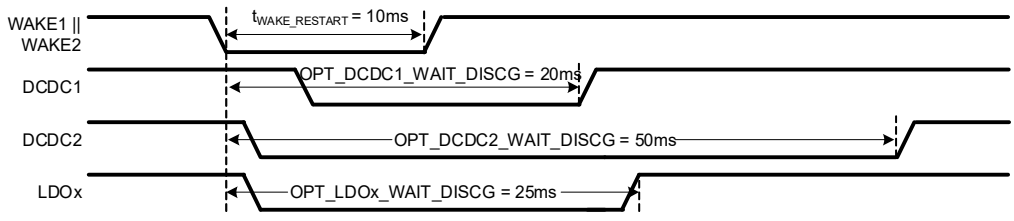


Figure 26. Example of OPT_WAIT_DISCG Settings

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5.2.6 Slot Timing Options

The power-up of DCDC2 and LDO1-4 regulators support slot timing for the WAKE pin start up or PSTBY exit restart timing to create inter-regulator start-up delays. After the t_{DCDC1} period where DCDC1 stabilizes, if OTP-programmed, slot delays 0 through 3 are executed in order.

When exiting DeepSTOP mode, slot timing is disabled and the regulators that were turned off in DeepSTOP restart immediately when PWRCTRLB is released high. If slot timing is required when exiting DeepSTOP, OPT_EN_DS_SLOT must be set to 1, and OPT_WAIT_DISCG settings for all regulators.

OPT_SLOTx_TIME controls the time delays between each of the four slots.

DCDC2, LDO1, LDO2, LDO3, and LDO4 are assigned to one of four slots using OPT_SLOT_X settings.

Regardless of slot settings, INTB rises when the last regulator stabilizes. Example timing is shown in Figure 27 where LDO1 is assigned to slot 1 and LDO2 is assigned to slots 2. LDOs 3 and 4 are assigned to slot 3. Figure 28 shows the available settings for each slot.

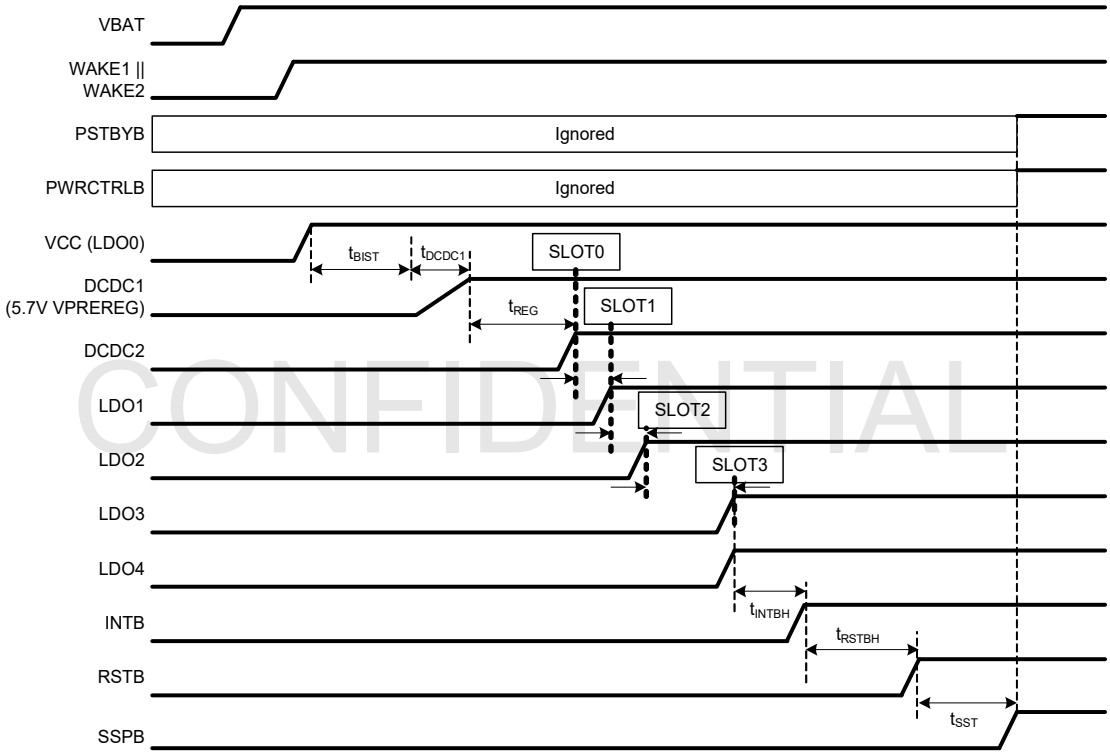


Figure 27. Example Slot Timing

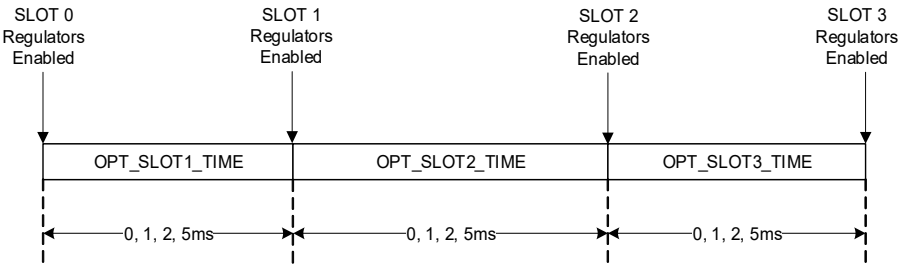


Figure 28. Slot Time Settings

5.2.7 Fault Reaction Timing

The RAA271084 can respond to fault sources as listed in Fault Response Programming. This includes VMONB, ERRB, and internal PMIC faults. Reactions to each fault source are classified in up to four handling cases as programmed with OPT_*_RESP register settings. The four responses cases are named 0, 1, 2, or 3.

- Case 0 – No response (fault ignored).
- Case 1 – Fault only requires RSTB low cycling and automatic restart. All regulators remain enabled. If the faulting source recovers in <10ms, RSTB returns high as shown in Figure 29. If the fault persists, RSTB remains low until the fault is no longer present at which point RSTB is released to the MCU.
- Case 2 – Fault requires forced cycle off of DCDC1, DCDC2, LDO1-LDO4, and RSTB low and automatic restart. The restart time is dependent on the longest OPT_WAIT_DISCHG setting. For example, if one of the regulators being restarted has an OPT_WAIT_DISCHG setting of 50ms, the PMIC does not attempt to restart until after this 50ms time period has expired. Figure 30 shows timing for Case 2 faults.
- Case 3 – Most severe fault reaction requiring PMIC shutdown. PMIC can only be re-enabled using the three options described in the OPT_FAULTED_RELEASE register description. After faulted release, the PMIC restarts. The restart time is dependent on the longest OPT_WAIT_DISCHG setting. For example, if one of the regulators being restarted has an OPT_WAIT_DISCHG setting of 50ms, the PMIC does not attempt to restart until after this 50ms time period has expired. Figure 31 shows the timing for this case.

Regardless of the OPT_*_RESP programming, faults are always recorded in the *_RECORD register and available for INTB assertion.

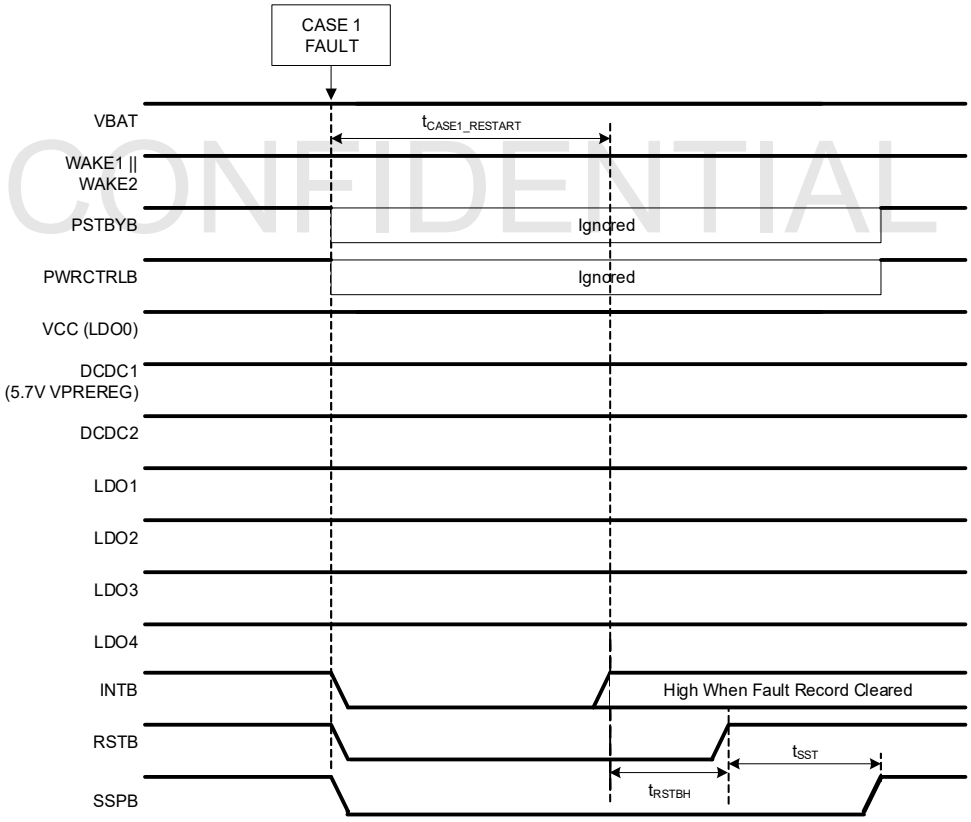


Figure 29. Case 1 Fault Timing

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
Fault to restart	$t_{CASE1_RESTART}$	Fault to PMIC restart time for Case 1	-	10	-	ms

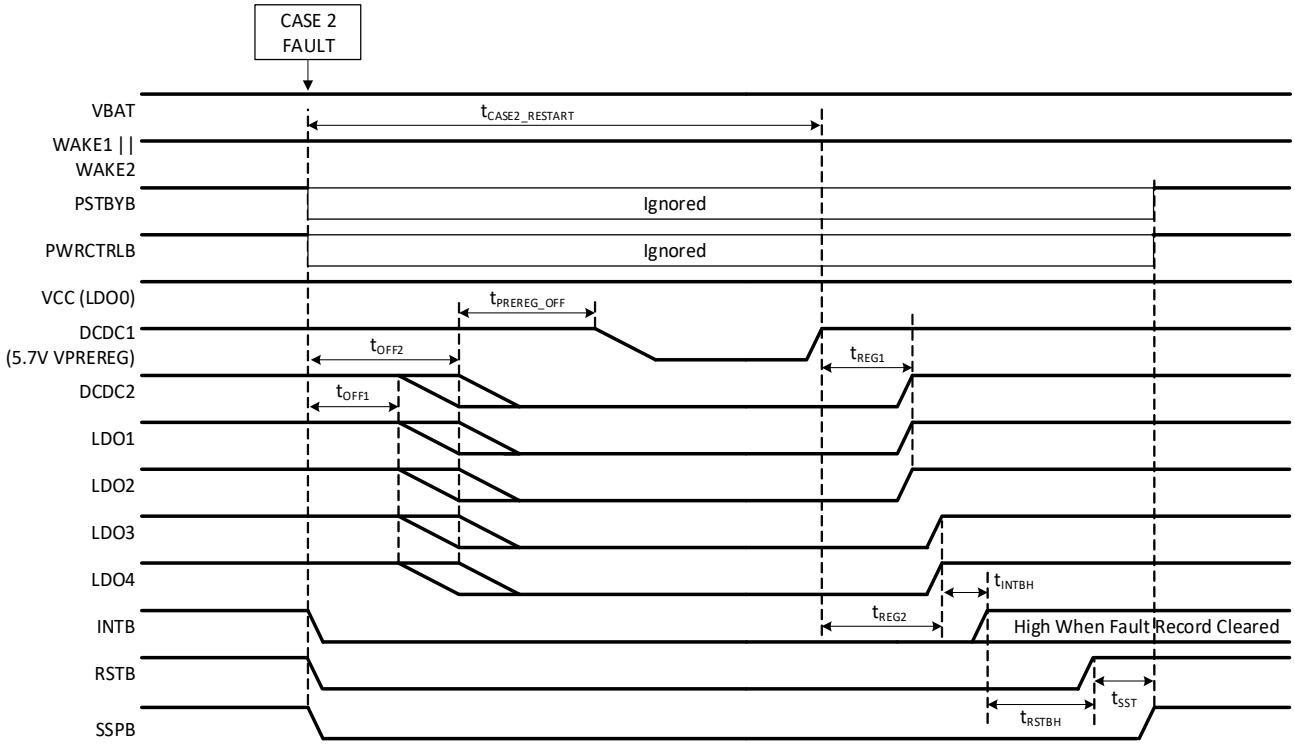
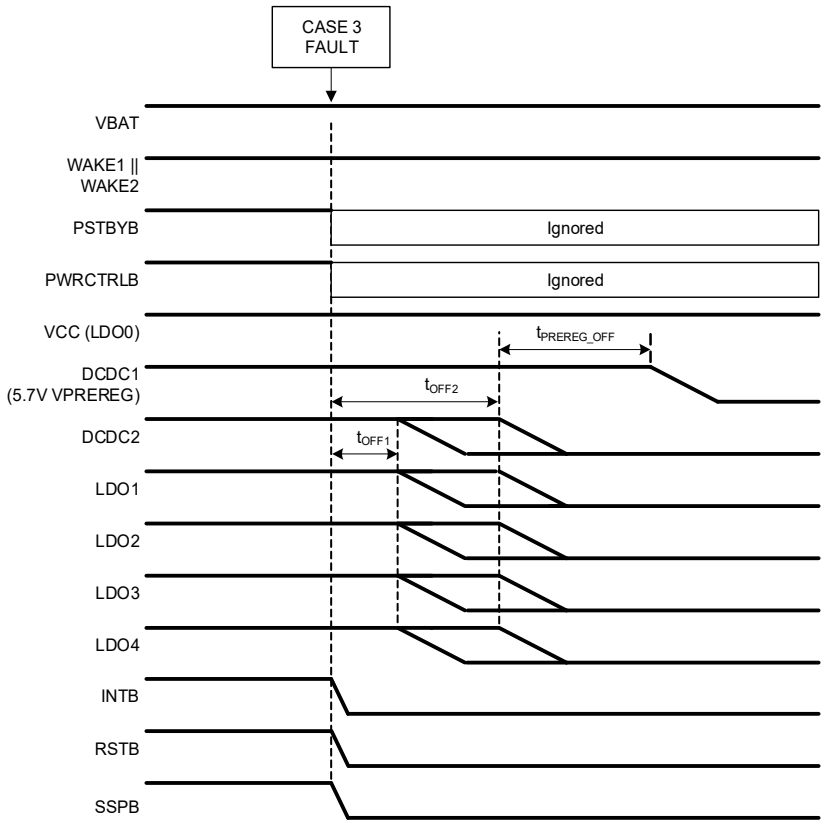


Figure 30. Case 2 Fault Timing

Note: Case 2 faults are typically serious regulator faults such as overcurrent, overvoltage, or undervoltage.

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Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
Fault to restart	$t_{CASE2_RESTART}$	Fault to PMIC restart time for Case 2	-	10	-	ms



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Figure 31. Case 3 Fault Timing

Shutdown timing for Case 3 is identical to Case 2. The method for exiting FAULTED is OTP programmable to either automatic retry or WAKE pin-controlled options as described in the Register Map.

If DCDC1 faults with Case 2 or Case 3 fault response of VBAT below V_{BAT_SDN} (default Case 2 fault response, configured by register 0x120 Bit[7]), OC2 overcurrent (fault response configured by register 0x121 Bits[5:4]), and severe overvoltage (fault response configured by register 0x121 Bits[3:2]), DCDC1 shuts down without delay. In this situation, the hangover time t_{PREREG_OFF} is 0ms.

5.3 Additional Features

5.3.1 SPI Target

A 4-pin SPI target interface is available to support serial access to the PMIC Register Map as listed in the Registers section. Single register address data write and read transfer is supported, and burst read data transfer is also supported with register address auto incrementing during data bursting. An OTP-optional CRC checking feature is available for data integrity checking for reads and writes. SPI transfer formatting and register space are byte organized.

Figure 32 and Figure 33 show basic SPI write and read formatting for transferring a single data byte. When SPICSB is low, the SPI target captures SPISDI data on the rising edge of SPICLK and launches SPISDO data on the falling edge of SPICLK. The MSB of byte 1 indicates write or read and bytes 1 and 2 contain the 10-bit address of the register being addressed. Data is transferred on the third byte and SPICSB returning high terminates the transaction. Most significant bits are transferred first.

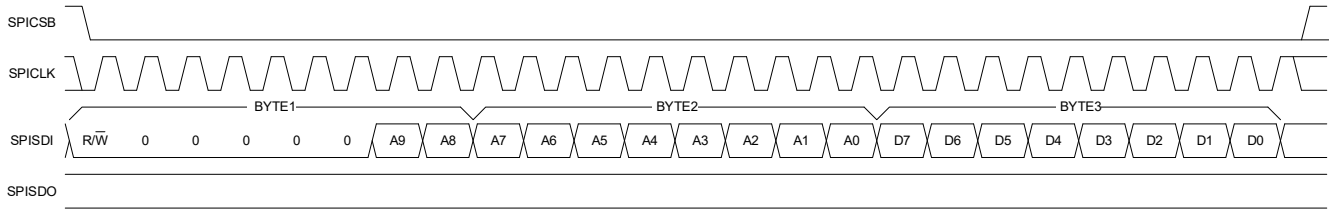


Figure 32. Register Byte Write

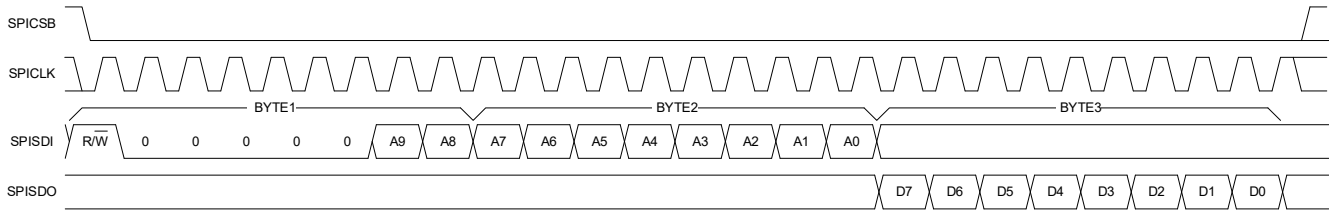


Figure 33. Register Byte Read

An optional CRC feature adds transfer integrity protection using CRC-8 (0x107) with polynomial $x^8+x^2+x^1+1$. For SPI writes, a CRC byte is added after the data byte. If the SPI target receives a correct CRC, the addressed register is written with the supplied data byte. If the CRC mismatches, the register is not written, the SPI_CRC_RECORD bit is set and optionally the INTB pin is asserted to flag the transfer error.

CRC for SPI reads are computed using the SPISDI bytes 1 and 2 and the addressed data byte 3 on SPISDO. The PMIC appends the CRC as byte 4 on SPISDO. The SPI controller should verify this CRC byte matches the computed CRC over bytes 1 to 3.

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For burst reads, each subsequent data byte supplied by the PMIC includes the CRC of the single byte preceding it. Figure 34 shows a SPI read burst with CRC as an example.

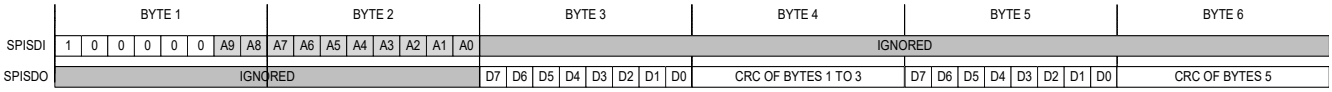


Figure 34. SPI Read Burst Formatting, CRC Enabled

The SPI interface includes a byte write message counter, which increments on a byte write to any register. This read-only register can be read to ensure the number of bytes written to the register map by the SPI controller are as expected.

Many PMIC registers control sensitive operations in the device. A KEY-secured access mechanism gains permission to alter these sensitive registers. A PMIC-provided random KEY value must be read then written back to the SECURE_KEY register to permit one subsequent write of a secured register. A mismatched key or failure to provide a key blocks the write to a secured register. Refer to Registers for secured registers.

By default, the SPISDO pin is always driven. Setting the OPT_SPI_HZ bit in the OPT_DEV_MODE1 register 0x200 configures the SPISDO pin as Hi-Z when SPICSB is high.

SPI Timing is described in Figure 35.

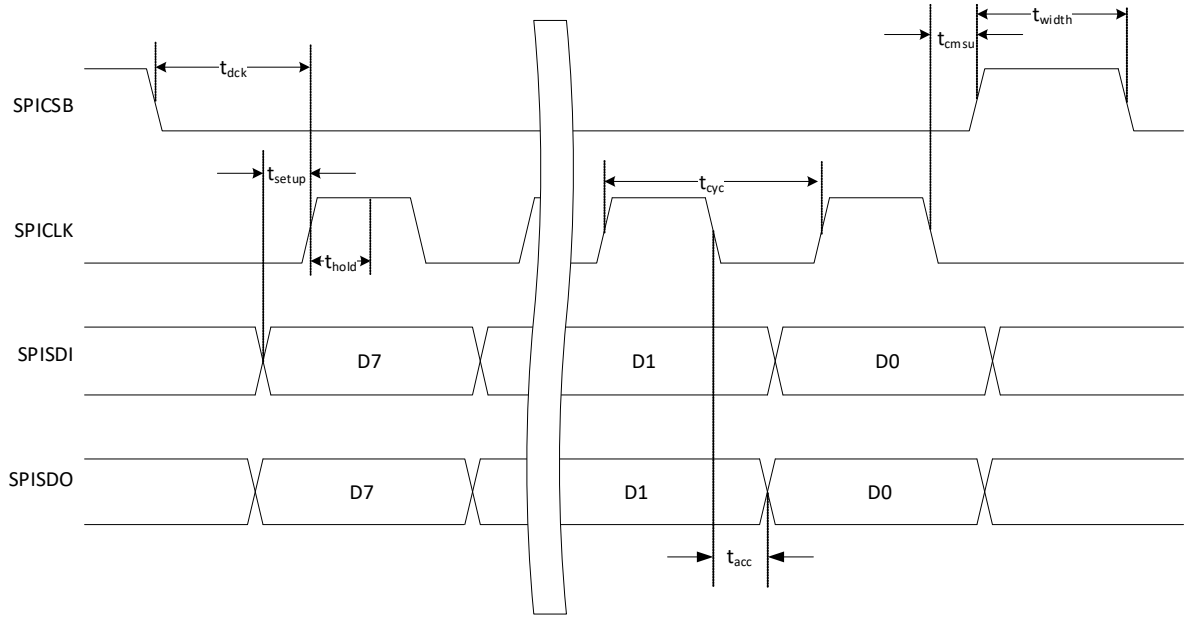


Figure 35. SPI Timing

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
SPICLK delay	t_{dck}	from SPICSB↓ to first SPICLK↑	55	-	-	ns
SPICLK period	t_{cyc}	from SPICLK↑ to SPICLK↑ 30pF load on SPISDO, 28ns setup time	116	-	-	ns
Command setup	t_{cmsu}	from last SPICLK↓ to SPICSB↑	60	-	-	ns
Data setup	t_{setup}	from data change to SPICLK↑	28	-	-	ns
Data hold	t_{hold}	from SPICLK↑ to data change	15	-	-	ns
Data access time	t_{acc}	from SPICLK↓ to data available on SPISDO	-	-	38	ns
H width of SPICSB	t_{width}	from SPI disable to next enable	200	-	-	ns

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5.3.2 Watchdog Timer and SST

The RAA271084 has a multi-function watchdog timer (WDT) to ensure MCU software is still operating normally. The WDT supports basic windowed kicking, 4QA, and 16QA (ASIL-D only) using SPI and pin-based kicking on the WDENB pin. An available error accumulator with threshold settings creates a credit-based system for some tolerance to kicking errors.

The WDT must be configured and enabled by the SPI host for setting operational modes and timeouts appropriate for the application.

As a safety mechanism, an auxiliary System Self-Test (SST) timer based on OTP settings automatically starts in the INIT STATE of the PMIC. This auxiliary timer must be SPI kicked by the host as a final step to affirm all application self-testing has completed successfully, any host required PMIC configuration has completed and the PMIC has permission to enter the ACTIVE state.

This SST timer mechanism is independent from the WDT itself. Failure to kick into the ACTIVE state results in an OTP-programmable reaction by the PMIC as a safety recovery measure.

Figure 36 shows the block diagrams and associated SPI registers for the WDT and SST functions. A detailed description of the WDT feature set follows.

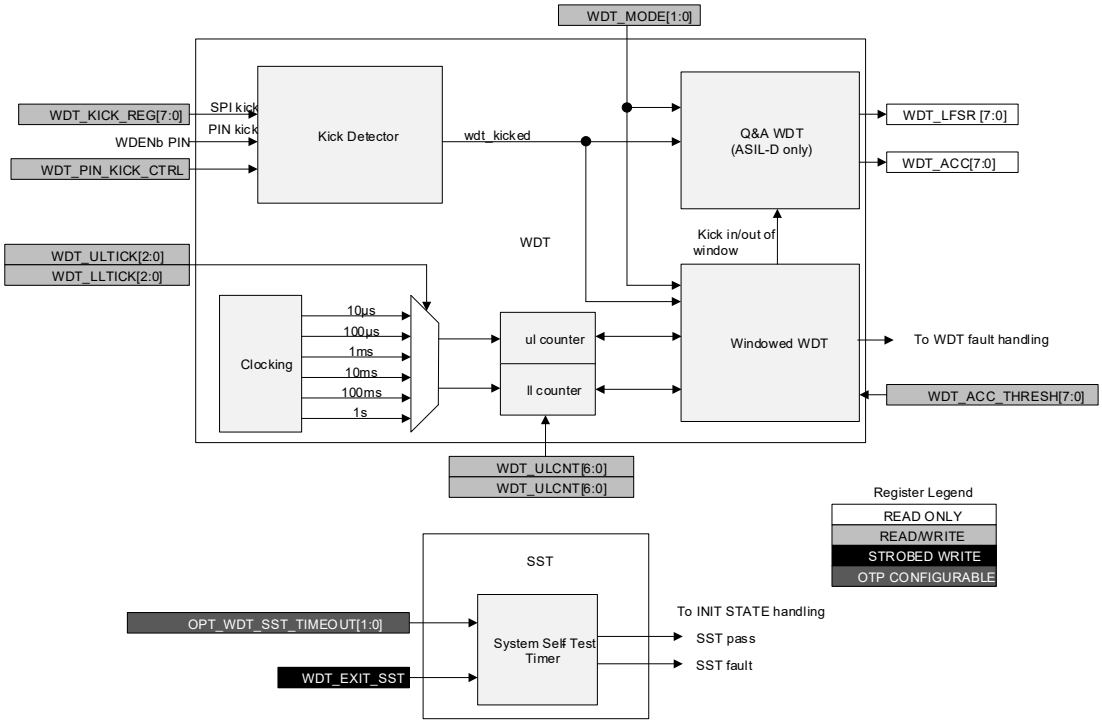


Figure 36. WDT and SST

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5.3.3 Fault Response Programming

Programmable responses are available for each fault monitor. Figure 37 diagrams how LDO1 warning OV fault responses can be configured as an example. The tables that follow provide details on fault response programming for all faults and the associated SPI register names.

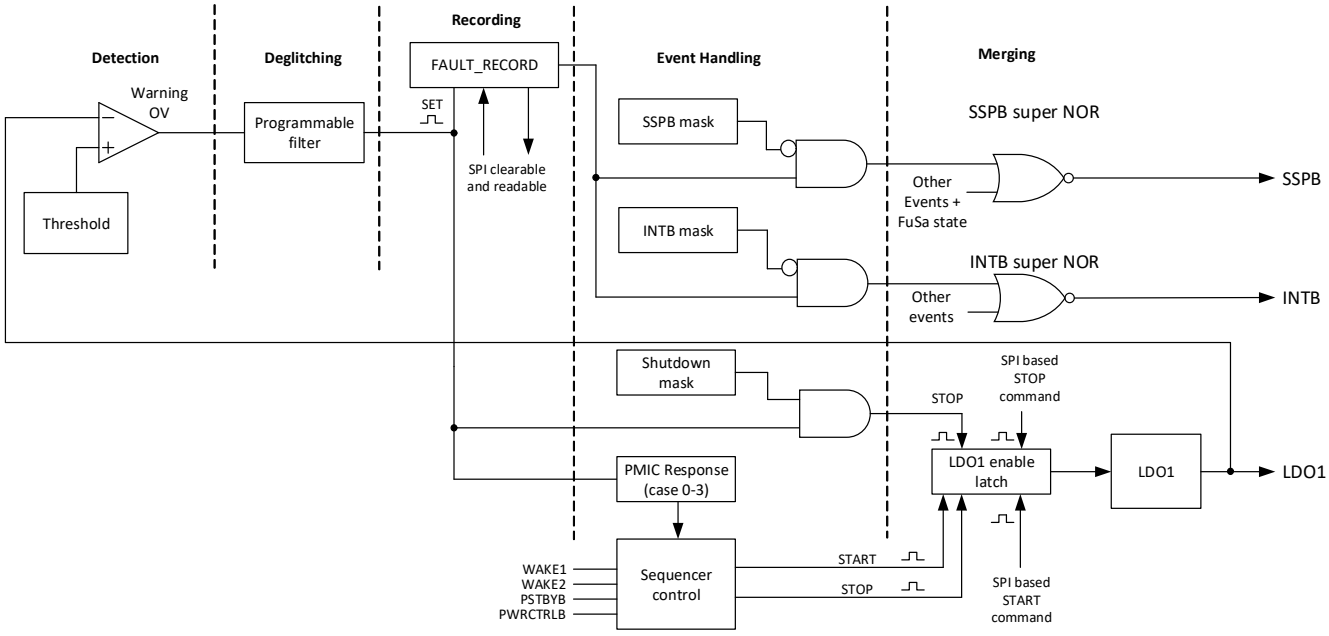


Figure 37. Fault Reaction Programming

- Detection – Correct operation is monitored using a programmable detection threshold.
- Deglitching – Improper operation exceeding a programmable minimum time is considered a fault.
- Recording – The fault event is stored in a SPI-accessible FAULT_RECORD bit. Each fault source has a unique FAULT_RECORD bit. The bit remains set until cleared using SPI. If the fault persists, the record bit remains set. *Note:* The FAULT_RECORD and masking bits control the event handling behavior.
- INTB masking – Assert the INTB pin low to report the event. All FAULT_RECORD bits must either be cleared or masked before INTB returns high. INTB always asserts low when RSTB asserts low during execution of a fault response even if INTB was masked for that fault. When the PMIC exits the faulted state and returns to active, INTB returns high automatically if it was masked for that specific fault. Otherwise, it would require manual clearing using an SPI write. PMIC fault Case 0 fault response does not prevent INTB from asserting low unless INTB is masked for that PMIC fault.
- SSPB masking – Assert the SSPB pin low to report the event. All FAULT_RECORD bits must either be cleared or masked before SSPB returns high. SSPB always asserts low when RSTB asserts low during execution of a fault response even if SSPB was masked for that fault. When the PMIC exits the faulted state and returns to active, SSPB returns high automatically if it was masked for that specific fault. Otherwise, it would require manual clearing using an SPI write. PMIC fault Case 0 fault response does not prevent SSPB from asserting low unless SSPB is masked for that PMIC fault.
- Shutdown masking – Disable the associated regulator output. Other regulators remain on.
- PMIC Case responses – Defines the overall PMIC response to the fault event. Regardless of case programming, the fault event is always stored in the FAULT_RECORD bit.
  - Case 0 – No reaction to fault.
  - Case 1 – RSTB cycled low then high. Regulator outputs remain active.
  - Case 2 – RSTB and all regulator outputs cycled low then high.
  - Case 3 – RSTB and all regulator outputs cycle low and PMIC transitions into FAULTED state. Release from faulted state is programmable using the OPT_FAULTED_RELEASE OTP setting.

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Case 3 fault responses require manipulation of the WAKE pins to release them from the FAULTED state when the fault has been removed. If Case 3 fault responses are selected with a release condition that WAKE1 must be low, then steps are required to ensure the PMIC identifies the WAKE1 level as low even if its hard-wired to a high level (such as a battery). For example, if a Case 3 fault response is selected with OPT_FAULTED_RELEASE = 0, the PMIC can be released from the FAULTED state when the fault is removed by bringing both WAKE pins low and then toggling either one high. If WAKE1 is hard-wired high, register 0x40[2:1] must be set to 2 during the Initialization phase of boot up. This sets WAKE1 low internal to the PMIC and ignores the connection at the pin. Before writing WAKE1 low, the system must hold WAKE2 high, otherwise having both WAKE pins low forces the PMIC to enter EOT_ONLY mode. When the Case 3 fault response is triggered, WAKE1 is already low internal to the PMIC and then the PMIC can be released from the FAULTED state with a low-to-high toggle of WAKE2.

5.3.4 DCDC1/2 and LDO1-4 UV/OV Programmable Responses

Table 2. DCDC1 UV/OV Programmable Responses

Function	DCDC1			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_DCDC1_SEV_OV 8%, 10%	OPT_DCDC1_SEV_UV -8%, -10%	OPT_DCDC1_WARN_OV 4%, 6%, 8%	OPT_DCDC1_WARN_UV -4%, -6%, -8%
Deglitching	OPT_DCDC1_SEV_OVUV_DLY_FILT 1µs, 5µs, 10µs, 25µs		OPT_DCDC1_WARN_OVUV_DLY_FILT 10µs, 25µs, 50µs, 100µs	
Recording	FB1_SEVERE_OV_ FAULT_RECORD	FB1_SEVERE_UV_ FAULT_RECORD	FB1_WARN_OV_FAULT_ RECORD	FB1_WARN_UV_FAULT_ RECORD
PMIC Response	OPT_DCDC1_SEV_UVOV_RESP Cases 0, 1, 2, 3		OPT_DCDC1_WARN_UVOV_RESP Cases 0, 1	
INTB Mask	OPT_INTB_MASK_FB1_UVOV_SEV		OPT_INTB_MASK_FB1_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_FB1_UVOV_SEV		OPT_SSPB_MASK_FB1_UVOV_WARN	

Table 3. DCDC2 UV/OV Programmable Responses

Function	DCDC2			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_DCDC2_SEV_OV 10%, 14%	OPT_DCDC2_SEV_UV -10%, -14%	OPT_DCDC2_WARN_OV 4%, 8%, 12%	OPT_DCDC2_WARN_UV -4%, -8%, -12%
Deglitching	OPT_DCDC2_SEV_OVUV_DLY_FILT 1µs, 5µs, 10µs, 25µs		OPT_DCDC2_WARN_OVUV_DLY_FILT 10µs, 25µs, 50µs, 100µs	
Recording	FB2_SEVERE_OV_FAULT_RECORD	FB2_SEVERE_UV_FAULT_RECORD	FB2_WARN_OV_FAULT_RECORD	FB2_WARN_UV_FAULT_RECORD
PMIC Response	OPT_DCDC2_SEV_UVOV_RESP Cases 0, 1, 2, 3		OPT_DCDC2_WARN_UVOV_RESP Cases 0, 1, 2, 3	
Shutdown Mask	OPT_DCDC2_SEV_UVOV_SHDN Operate, Shutdown		OPT_DCDC2_WARN_UVOV_SHDN Operate, Shutdown	
INTB Mask	OPT_INTB_MASK_FB2_UVOV_SEV		OPT_INTB_MASK_FB2_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_FB2_UVOV_SEV		OPT_SSPB_MASK_FB2_UVOV_WARN	

Table 4. LDO1 UV/OV Programmable Responses

Function	LDO1			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_LDO1_SEV_OV 10%, 14%	OPT_LDO1_SEV_UV -10%, -14%	OPT_LDO1_WARN_OV 4%, 8%, 12%	OPT_LDO1_WARN_UV -4%, -8%, -12%
Deglitching	OPT_LDO1_SEV_OVUV_DLY_FILT 1µs, 5µs, 10µs, 25µs		OPT_LDO1_WARN_OVUV_DLY_FILT 10µs, 25µs, 50µs, 100µs	
Recording	LDO1_SEVERE_OV_FAULT_RECORD	LDO1_SEVERE_UV_FAULT_RECORD	LDO1_WARN_OV_FAULT_RECORD	LDO1_WARN_UV_FAULT_RECORD
PMIC Response	OPT_LDO1_SEV_UVOV_RESP Cases 0, 1, 2, 3		OPT_LDO1_WARN_UVOV_RESP Cases 0, 1	
Shutdown Mask	OPT_LDO1_SEV_UVOV_SHDN Operate, Shutdown		OPT_LDO1_WARN_UVOV_SHDN Operate, Shutdown	
INTB Mask	OPT_INTB_MASK_LDO1_UVOV_SEV		OPT_INTB_MASK_LDO1_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_LDO1_UVOV_SEV		OPT_SSPB_MASK_LDO1_UVOV_WARN	

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Table 5. LDO2 UV/OV Programmable Responses

Function	LDO2			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_LDO2_SEV_OV 10%, 14%	OPT_LDO2_SEV_UV -10%< -14%	OPT_LDO2_WARN_OV 4%, 8%, 12%	OPT_LDO2_WARN_UV -4%, -8%, -12%
Deglitching	OPT_LDO2_SEV_OVUV_DLY_FILT 1µs, 5µs, 10µs, 25µs		OPT_LDO2_WARN_OVUV_DLY_FILT 10µs, 25µs, 50µs, 100µs	
Recording	LDO2_SEVERE_OV_FAULT_RECORD	LDO2_SEVERE_UV_FAULT_RECORD	LDO2_WARN_OV_FAULT_RECORD	LDO2_WARN_UV_FAULT_RECORD
PMIC Response	OPT_LDO2_SEV_UVOV_RESP Cases 0, 1, 2, 3		OPT_LDO2_WARN_UVOV_RESP Cases 0, 1	
Shutdown Mask	OPT_LDO2_SEV_UVOV_SHDN Operate, Shutdown		OPT_LDO2_WARN_UVOV_SHDN Operate, Shutdown	
INTB Mask	OPT_INTB_MASK_LDO2_UVOV_SEV		OPT_INTB_MASK_LDO2_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_LDO2_UVOV_SEV		OPT_SSPB_MASK_LDO2_UVOV_WARN	

Table 6. LDO3 UV/OV Programmable Responses

Function	LDO3			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_LDO3_SEV_OV 10%, 14%	OPT_LDO3_SEV_UV -10%, -14%	OPT_LDO3_WARN_OV 4%, 8%, 12%	OPT_LDO3_WARN_UV -4%, -8%, -12%
Deglitching	OPT_LDO3_SEV_OVUV_DLY_FILT 1µs, 5µs, 10µs, 25µs		OPT_LDO3_WARN_OVUV_DLY_FILT 10µs, 25µs, 50µs, 100µs	
Recording	LDO3_SEVERE_OV_ FAULT_RECORD	LDO3_SEVERE_UV_ FAULT_RECORD	LDO3_WARN_OV_ FAULT_RECORD	LDO3_WARN_UV_FAULT_R ECORD
PMIC Response	OPT_LDO3_SEV_UVOV_RESP Cases 0, 1, 2, 3		OPT_LDO3_WARN_UVOV_RESP Cases 0, 1	
Shutdown Mask	OPT_LDO3_SEV_UVOV_SHDN Operate, Shutdown		OPT_LDO3_WARN_UVOV_SHDN Operate, Shutdown	
INTB Mask	OPT_INTB_MASK_LDO3_UVOV_SEV		OPT_INTB_MASK_LDO3_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_LDO3_UVOV_SEV		OPT_SSPB_MASK_LDO3_UVOV_WARN	

Table 7. LDO4 UV/OV Programmable Responses

Function	LDO4			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_LDO4_SEV_OV 10%, 14%	OPT_LDO4_SEV_UV -10%, -14%	OPT_LDO4_WARN_OV 4%, 8%, 12%	OPT_LDO4_WARN_UV -4%, -8%, -12%
Deglitching	OPT_LDO4_SEV_OVUV_DLY_FILT 1µs, 5µs, 10µs, 25µs		OPT_LDO4_WARN_OVUV_DLY_FILT 10µs, 25µs, 50µs, 100µs	
Recording	LDO4_SEVERE_OV_FAULT _RECORD	LDO4_SEVERE_UV_FAULT _RECORD	LDO4_WARN_OV_FAULT_ RECORD	LDO4_WARN_UV_FAULT _RECORD
PMIC Response	OPT_LDO4_SEV_UVOV_RESP Cases 0, 1, 2, 3		OPT_LDO4_WARN_UVOV_RESP Cases 0, 1	
Shutdown Mask	OPT_LDO4_SEV_UVOV_SHDN Operate, Shutdown		OPT_LDO4_WARN_UVOV_SHDN Operate, Shutdown	
INTB Mask	OPT_INTB_MASK_LDO4_UVOV_SEV		OPT_INTB_MASK_LDO4_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_LDO4_UVOV_SEV		OPT_SSPB_MASK_LDO4_UVOV_WARN	

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5.3.4.1 COREMON and LDO0 UV/OV Programmable Responses

Table 8. COREMON UV/OV Programmable Responses (ASIL-D only)

Function	COREMON			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_COREMON_SEV_OV 10%, 14%	OPT_COREMON_SEV_U V -10%, -14%	OPT_COREMON_WARN_O V 4%, 8%, 12%	OPT_COREMON_ WARN_UV -4%, -8%, -12%
Deglitching	OPT_COREMON_SEV_OV_D LY_FILT 1us, 5µs, 10µs, 25µs	OPT_COREMON_SEV_U V_DLY_FILT 1us, 5µs, 10µs, 25µs	OPT_COREMON_WARN_O V_DLY_FILT 10µs, 25µs, 50µs, 100µs	OPT_COREMON_ WARN_UV_DLY_FILT 10µs, 25µs, 50µs, 10µs
Recording	COREMON_SEVERE_OV _FAULT_RECORD	COREMON_SEVERE_ UV_FAULT_RECORD	COREMON_WARN_OV_ FAULT_RECORD	COREMON_WARN_UV_ FAULT_RECORD
PMIC Response	OPT_COREMON_SEV_OV_R ESP Cases 0, 1, 2, 3	OPT_COREMON_SEV_U V_RESP Cases 0, 1, 2, 3	OPT_COREMON_OV_ RESP Cases 0, 1, 2, 3	OPT_COREMON_UV_RE SP Cases 0, 1, 2, 3
INTB Mask	OPT_INTB_MASK_COREM_UVOV_SEV		OPT_INTB_MASK_COREM_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_COREM_UVOV_SEV		OPT_SSPB_MASK_COREM_UVOV_WARN	

Table 9. LDO0 UV/OV Programmable Responses

Function	VCC (LDO0)			
Fault	Severe overvoltage	Severe undervoltage	Warning overvoltage	Warning undervoltage
Detection Threshold	OPT_LDO0_SEV_OV 10%, 14%	OPT_LDO0_SEV_UV -10%, -14%	OPT_LDO0_WARN_OV 4%, 8%, 12%	OPT_LDO0_WARN_UV -4%, -8%, -12%
Deglitching	OPT_LDO0_SEV_OVUV_DLY_FILT 1µs, 5µs, 10µs, 25µs		OPT_LDO0_WARN_OVUV_DLY_FILT 10µs, 25µs, 50µs, 100µs	
Recording	LDO0_SEVERE_OV_ FAULT_RECORD	LDO0_SEVERE_UV_ FAULT_RECORD	LDO0_WARN_OV_ FAULT_RECORD	LDO0_WARN_UV_ FAULT_RECORD
PMIC Response	OPT_LDO0_SEV_UVOV_RESP Cases 0, 1, 2, 3		OPT_LDO0_WARN_UVOV_RESP Cases 0, 1	
INTB Mask	OPT_INTB_MASK_LDO0_UVOV_SEV		OPT_INTB_MASK_LDO0_UVOV_WARN	
SSPB Mask	OPT_SSPB_MASK_LDO0_UVOV_SEV		OPT_SSPB_MASK_LDO0_UVOV_WARN	

5.3.4.2 DCDC1, DCC2 OC Programmable Responses

Table 10. DCDC1, DCC2 OC Programmable Responses

Block	DCDC1	DCDC2
Fault	Overcurrent	Overcurrent
Recording	DCDC1_OC1_FAULT_RECORD, DCDC1_OC2_FAULT_RECORD	DCDC2_OC2_FAULT_RECORD
PMIC Response	OPT_DCDC1_OC2_RESP Cases 0, 1, 2, 3	OPT_DCDC2_OC2_RESP Case 2, 3
Shutdown Mask	N/A	N/A
INTB Mask	OPT_INTB_MASK_DCDC1_OC1, OPT_INTB_MASK_DCDC1_OC2	OPT_INTB_MASK_DCDC2_OC2
SSPB Mask	OPT_SSPB_MASK_DCDC1_OC2	OPT_SSPB_MASK_DCDC2_OC2

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Block	DCDC1 Buck/Boost Mode Report
Recording	REG1_BUCKBOOST_MODE_RECORD
INTB Mask	OPT_INTB_MASK_REG1_BUCKBOOST_MODE

5.3.4.3 Pin Related Programmable Responses

Table 11. VMONB and ERRB

Function	VMONB	ERRB
Fault	VMONB pin low	ERRB pin low
Deglitching	OPT_VMONB_PER1, VMONB_PER2	OPT_ERRB_PER1, ERRB_PER2
Recording	VMONB_FAULT_RECORD	ERRB_FAULT_RECORD
PMIC Response	OPT_VMONB_RESP Cases 0, 1, 2, 3	OPT_ERRB_RESP Cases 0, 1, 2, 3
INTB Mask	OPT_INTB_VMONB_FAULT	OPT_INTB_ERRB_FAULT
SSPB Mask	OPT_SSPB_VMONB_FAULT	OPT_SSPB_ERRB_FAULT

Table 12. Pin Faults

Block	Pin Faults	
Fault	SSPB pin driven vs sensed mismatch	RSTB pin driven vs sensed mismatch

Table 12. Pin Faults

Deglitching	100µs	
Recording	SSPB_PIN_FAULT_RECORD	RSTB_PIN_FAULT_RECORD
PMIC Response	OPT_SSPB_FLT_RESP Cases 0, 1, 2, 3	OPT_RSTB_FLT_RESP Cases 0, 1, 2, 3
INTB Mask	OPT_INTB_MASK_PIN_FAULT	

5.3.4.4 TSD Programmable Responses

Table 13. TSD Programmable Responses

Block	**TSD**		
Fault	FuSa TSD	LDO3/4 TSD	
Detection Threshold	160C	160C	
Deglitching	OPT_TSD_FUSA_DLY_FILT 50µs, 100µs, 1ms, 2.5ms	N/A	
Recording	TSD_FUSA_FAULT_RECORD	TSD_LDO34_FAULT_RECORD	
PMIC Response	OPT_TSD_FUSA_RESP Case 0, 1, 2, 3	N/A	
Shutdown Mask	N/A	OPT_LDO3_TSD_SHDN	OPT_LDO4_TSD_SHDN
INTB Mask	OPT_INTB_MASK_TSD	OPT_INTB_MASK_TSD34	
SSPB Mask	OPT_SSPB_MASK_TSD	OPT_SSPB_MASK_TSD34	

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5.3.4.5 SPI Interface Fault Responses

Table 14. SPI Interface Fault Responses

Block	**SPI I/F**	
Fault	Transactional write fault	Write data stored SPI register mismatch
Recording	SPI_CRC_FAULT_RECORD	SPI_WRITE_FAULT_RECORD
INTB Mask	OPT_INTB_SPI_FAULT	

5.3.4.6 Architecture Programmable Responses

Table 15. Architecture Programmable Responses

Block	**Architecture Faults**			
Fault	DGND disconnect fault	AGND disconnect fault	VBG_OV_FAULT	VBG_UV_FAULT
Deglitching	OPT_ARCH_MON_DLY_FILT 10µs, 25µs, 50µs, 100µs			
Recording	DGND_FAULT_ RECORD	AGND_FAULT_ RECORD	VBG_OV_FAULT_ RECORD	VBG_UV_FAULT_ RECORD
PMIC Response	OPT_ARCH_MON_FLT_RESP Cases 0, 1, 2, 3			
INTB Mask	OPT_INTB_MASK_ARCHMON_FAULT			
SSPB Mask	OPT_SSPB_MASK_ARCHMON_FAULT			

Table 16. SYSCLK Frequency

Block	**SYSCLK Frequency**	
Fault	clk_over_freq_fault	clk_under_freq_fault

Table 16. SYSCLK Frequency

Deglitching	500µs	
Recording	CLK_OVER_FREQ_FAULT_RECORD	CLK_UNDER_FREQ_FAULT_RECORD
PMIC Response	OPT_SYSCLK_RESP Cases 2, 3	
INTB Mask	OPT_INTB_MASK_SYS_OSC	
SSPB Mask	OPT_SSPB_MASK_SYS_OSC	

Table 17. VBAT Monitor

Block	**VBAT Monitor**
Fault	VBAT < V_{BAT_SDN} detected
Recording	VBAT_UVLO_FAULT_RECORD
PMIC Response	OPT_VBAT_UVLO_FLT_RESP Case 2, 3
INTB Mask	OPT_INTB_MASK_VBAT_UVLO

Table 18. Config Check

Block	**Config Check**
Fault	Config. Recheck mismatch
Recording	CRC_RECHECK_FAULT_RECORD
PMIC Response	OPT_REG_CHK_FLT_RESP Cases 0, 1, 2, 3
INTB Mask	OPT_INTB_MASK_REG_FAULT

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5.3.4.7 Timer Programmable Responses

Table 19. Watchdog Timer

Block	**WDT (Watchdog Timer)**					
Fault	WDT timeout accumulator fault	WDT timeout fault	WDT accumulator fault	WDT answer fault	WDT late fault	WDT early fault
Recording	WDT_TOACC_ FAULT_RECORD	WDT_TO_FAULT_ RECORD	WDT_ACC_FAULT _RECORD	WDT_ANS_ FAULT_ RECORD	WDT_LATE_ FAULT_ RECORD	WDT_EARLY_F AULT_ RECORD
PMIC Response	WDT_TOACC_ FAULT_RESP Cases 0, 1, 2, 3	N/A	WDT_ACC_FAULT _RESP Cases 0, 1, 2, 3	N/A		
INTB Mask	INTB_MASK_ TOACC_FAULT	INTB_MASK_TO_F AULT	INTB_MASK_ACC _FAULT	INTB_MASK_WDT_FAULT		
SSPB Mask	SSPB_MASK_ TOACC_FAULT	SSPB_MASK_TO_ FAULT	SSPB_MASK_ACC _FAULT	SSPB_MASK_WDT_FAULT		

Table 20. System Self Test Timer

Block	SST (System Self Test Timer)
Fault	System self test timeout
Recording	SST_FAULT_RECORD
PMIC Response	OPT_SST_RESP
INTB Mask	OPT_INTB_MASK_SST_FAULT

Table 21. Engine off Timer

Block	EOT (Engine off Timer)			
Fault	EOT count down expired	EOT at counter limit	EOT power-down reached	EOT wakeup reached
Recording	EOT_CD_ALRM_ RECORD	EOT_OVF_ALRM_ RECORD	EOT_PD_ALRM_RECORD	EOT_WU_ALRM_ RECORD
PMIC Response	EOT_CD_CTRL Nothing or exit low power state	N/A	EOT_PD_CTRL Nothing or enter low power state	EOT_WU_CTRL Nothing or exit low power state
INTB Mask	INTB_MASK_CD_ZERO	INTB_MASK_EOT_OVF	INTB_MASK_EOT_PD	INTB_MASK_EOT_WU

5.3.5 PMIC Built in Self Test

The RAA271084 has multiple self-testing features to monitor PMIC health and ensure trusted operation before enabling DCDC1 and application regulators.

Startup self-test features are listed below.

- Logic built-in-self-test (LBIST) is performed on all logic controlling safety monitoring features.
- Analog built-in-self-test (ABIST) is executed on these safety monitors to detect stuck-at faults:
  - DCDC1 UV and OV monitors (warning and severe level)
  - DCDC2 UV and OV monitors (warning and severe level)
  - LDOs 1 through 4, UV and OV (warning and severe level)
  - Coremon UV and OV (warning and severe level) (ASIL-D only)
  - VBG, PGND, and VCC monitors for UV and OV
  - System clock, over and under-frequency, over-temperature
- Stuck-at fault checking for these device pins:
  - RSTB, SSPB

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5.3.6 System Self Test Resources

System self-test is a step where both the PMIC and the host system validate operation before entering trusted operation and assertion of the SSPB safety output pin.

After asserting RSTB high in the INIT state, the PMIC enters the SYSTEM SELF TEST state. All PMIC safety mechanisms are fully operational in this state; however, this does not ensure the host system start up or operation is satisfactory nor is pin connectivity between the host and PMIC is intact. The RAA271084 provides pin controls and a dedicated timer to support these checks.

PMIC to host system pin connectivity checking is available using the SPI interface using the controls shown in Figure 38. This mechanism ensures critical pins such as ERRB, VMONB, WAKE1, WAKE2, PSTBYB, PWRCTRLB, INTB, and WDENB are end-to-end controllable between devices. Input pin controls for transparent hold, set high and set low are available using SPI. Transparent is an input pass through used for normal operation. Hold latches the input value. Set high or low are forced input values.

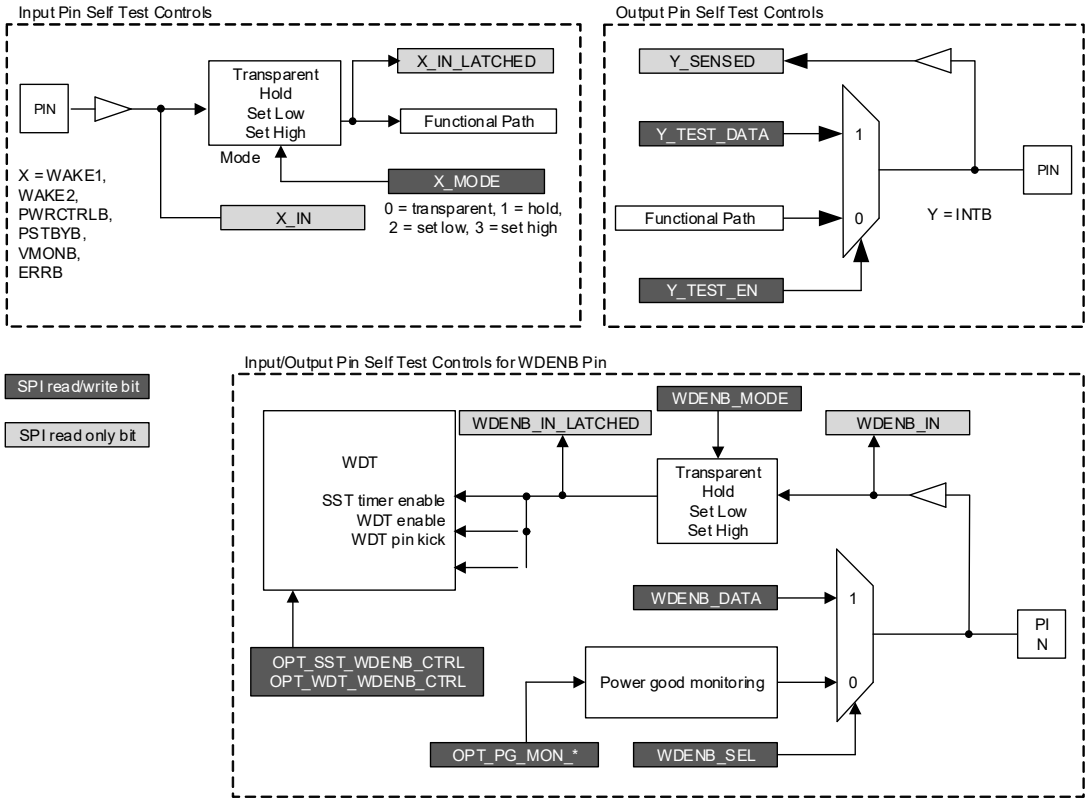


Figure 38. Pin Overrides for Pin Checking

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An SST (system self test) timer is automatically started when RSTB rises as a timeout mechanism during the host system start up period. Timeout values are selected using the OPT_SST_TIMEOUT settings. This creates a window for the system to fully start up and execute application-wide self test procedures. This includes activating, testing, and configuration of PMIC resources by system software. Writing a logic 1 to the EXIT_SST bit disables the timer and transitions the PMIC into ACTIVE state. Failure to complete this step by setting the EXIT_SST bit results in an SST fault. Handling of this fault by the PMIC is OTP programmable. Figure 39 shows the programmable features of the SST.

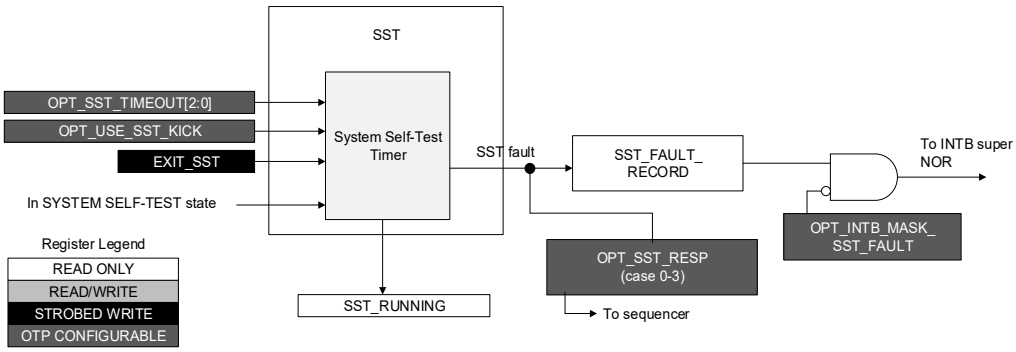


Figure 39. SST Timer

5.3.7 ERRB Fault Monitoring

The ERRB input pin can be programmed to trigger Case 0, 1, 2, or 3 fault reactions in the PMIC. Additionally, ERRB faults can assert the INTB pin and are always reported to the ERRB_FAULT_RECORD status bit. When RSTB is asserted high, PMIC monitoring of the ERRB input starts following configuration of the monitor and remains active unless disabled or RSTB returns low. Monitoring is time-based. If the ERRB input condition persists greater than a programmed minimum period, an ERRB fault is triggered. The ERRB monitoring mode is set using the OPT_ERRB_CTRL1 register and the ERRB monitoring period is set using the OPT_ERRB_CTRL1 and ERRB_CTRL2 registers. The register used depends on the mode of ERRB monitoring being used.

Two modes of ERRB monitoring are supported: Low-level (mode 0) and rising edge + first kick (mode 1). Each of the modes are described in detail in the following sections.

5.3.7.1 Mode 0 – ERRB Low-Level Detect

Low-level is an error condition. If this error persists greater than the programmed period, an ERRB fault is triggered. ERRB high is an OK condition and ERRB timing is disabled. Mode 0 can be set up using OTP programming of the OPT_ERRB_CTRL1 register by writing OPT_ERRB_MODE = 0.

There are two ERRB monitoring period options available for Mode 0. The first option is set with the OPT_ERRB_CTRL1 register. This is an OTP programmable option, which sets up the ERRB monitoring period at boot up and anytime immediately following an MCU reset. This option allows applying a longer monitoring period at startup than what might be required during the application. The period for this option is set with the OPT_ERRB_PER1 field.

The second ERRB monitoring option is controlled by the ERRB_CTRL2 register. This register sets a secondary ERRB period value using the ERRB_PER2 field. Any value written to the ERRB_CTRL2 register configures the ERRB monitor to use the secondary measurement period. To take effect, the ERRB_CTRL2 register must be written while the ERRB input is high. When written, the ERRB_PER2 period is used until either OPT_ERRB_CTRL1 is rewritten, RSTB is asserted low (MCU reset), or the device exits DeepSTOP. After RSTB is asserted low, the ERRB monitor reverts back to OPT_ERRB_PER1. The typical use case is OPT_ERRB_PER1 is used at MCU boot time. Subsequently, the application can update the ERRB_PER2 field to use a more relevant monitor period during application execution.

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When OPT_DS_EXIT_BIST is set to 1, BIST is run when exiting DeepSTOP. Write a 1 to CLEAR_LBIST_STATUS before entering DeepSTOP to clear the LBIST status flag. When exiting DeepSTOP, the system must monitor LBIST_DONE to ensure that LBIST has completed execution before programming the ERRB monitor to restart with the ERRB_PER2 period. If OPT_DS_EXIT_BIST is set to 0, the MCU can reprogram the ERRB monitor period as soon as the core rail is valid, and the SPI communications are functional.

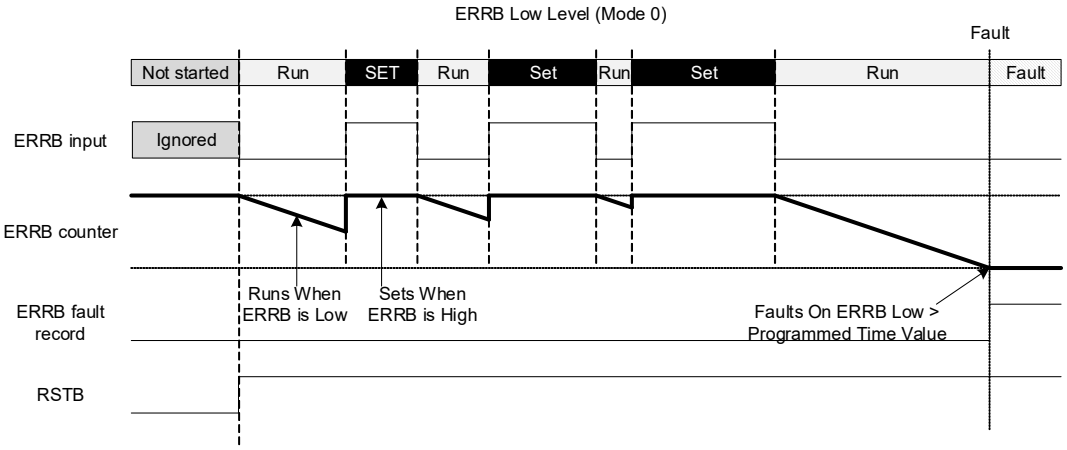


Figure 40. ERRB Low-level Monitoring Option (Mode 0)

5.3.7.2 Mode 1 – Rising Edge Mode + First Kick

Rising edge + first kick allows the first rising edge of the ERRB input to start the ERRB timing process. After RSTB rises, Mode 1 can be configured and initiated. The ERRB level is ignored until the first rising edge is detected. After detection, subsequent rising ERRB edges prevent the ERRB fault timer from expiring. Rising edges occurring greater than a programmed period trigger an ERRB fault response.

Mode 1 is not available as an OTP option. The OTP setting of the OPT_ERRB_CTRL1 register must be 0 and OPT_ERRB_PER1 must not be programmed to a non-zero value. Mode 1 must only use the ERRB_PER2 register for its ERRB monitoring period. Mode 1 is setup by MCU programming during the boot sequence before entry to the Active state. When RSTB is released high to the MCU, three register writes are required to enable the ERRB monitor in Mode 1 in the following sequence:

1. Write OPT_ERRB_CTRL1 = 0x00
2. Write OPT_ERRB_CTRL1 = 0x40
3. Write the required monitoring period into the ERRB_PER2 register.

When this last register write is executed, the PMIC begins Mode 1 ERRB monitoring. This sequence must occur following every MCU reset.

When OPT_DS_EXIT_BIST is set to 1, BIST is run when exiting DeepSTOP. Write a 1 to CLEAR_LBIST_STATUS before entering DeepSTOP to clear the LBIST status flag. When exiting DeepSTOP, the system must monitor LBIST_DONE to ensure that LBIST has completed execution before programming the ERRB monitor to restart in Mode 1 as previously described. If OPT_DS_EXIT_BIST is set to 0, the MCU can reprogram the ERRB monitor as soon as the core rail is valid, and the SPI communications are functional.

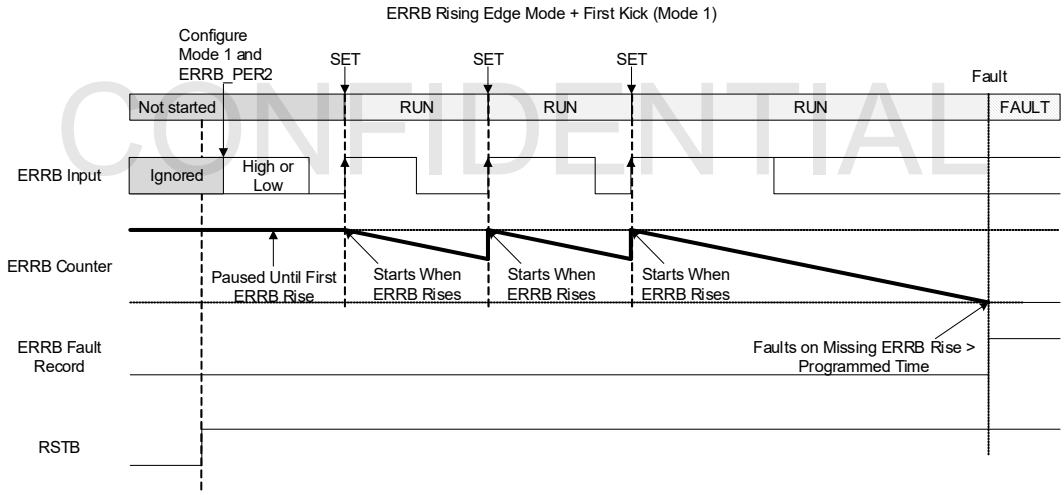


Figure 41. ERRB Edge Mode and First Kick Monitoring (Mode 1)

5.3.8 VMONB Monitoring

The VMONB input pin can be programmed to trigger Case 0, 1, 2, or 3 fault reactions in the PMIC. Additionally, VMONB faults can assert the INTB pin and are always reported to the VMONB_FAULT_RECORD status bit. Power-on default monitoring behavior is controlled using OTP programming of register OPT_VMONB_CTRL1. Monitoring settings during application execution can be adjusted using the VMONB_CTRL2 register.

If enabled, PMIC monitoring of the VMONB input starts when the PMIC detects that all application output power rails have stabilized and have reached power-good. The INTB output is automatically asserted high at this time. Monitoring is time-based. If the VMONB input low condition persists greater than a programmed minimum period, a VMONB fault is triggered.

There are two VMONB monitoring period options available. The first option is set with the OPT_VMONB_CTRL1 register. This is an OTP programmable option that sets up the VMONB monitoring period at boot up and anytime

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immediately following an MCU reset. This option allows applying a longer monitoring period at startup than what might be required during the application. The period for this option is set with the OPT_VMONB_PER1 field.

The second VMONB monitoring option is controlled by the VMONB_CTRL2 register. This register sets a secondary VMONB period value using the VMONB_PER2 field. Any value written to the VMONB_CTRL2 register configures the VMONB monitor to use the secondary measurement period. For the VMONB_PER2 setting to take effect, it must be written while the VMONB input is high. When written, the OPT_VMONB_PER1 value is ignored until either OPT_VMONB_CTRL1 is rewritten, RSTB is asserted low (MCU reset), or the device exits DeepSTOP. After RSTB is asserted low, the VMONB monitor reverts back to OPT_VMONB_PER1. The typical use case is OPT_VMONB_PER1 is used at MCU boot time. Subsequently, the application can update the VMONB_PER2 field to use a more relevant monitor period during application execution.

Since power-good stabilizes before the RSTB high assertion, Renesas recommends that either the OTP default for VMONB is disabled or set to a fault time period greater than the RSTB high assertion timing. This permits the application some time to initialize and configure external application voltage monitors and assert VMONB high before the programmed VMONB monitor timeout, Figure 43. After initialization, the VMONB monitor timeout can be reprogrammed using the VMONB_PER2 register to a reduced time to shorten reaction times if required, see Figure 42.

Low-level on the VMONB input is considered an error condition. If this error persists greater than a programmed period, a VMONB fault is triggered. VMONB high is considered an OK condition.

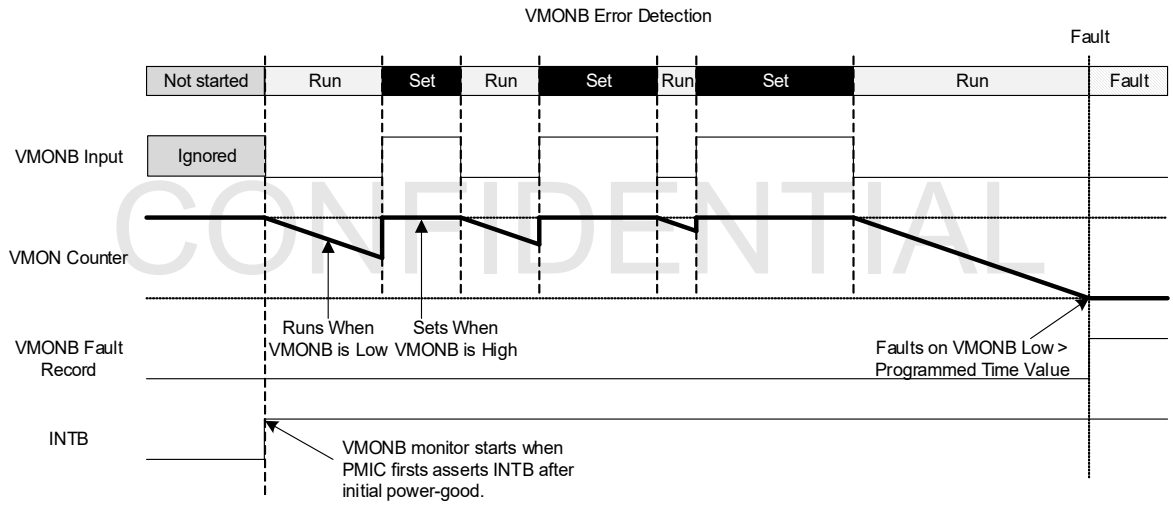


Figure 42. VMONB Error Detection

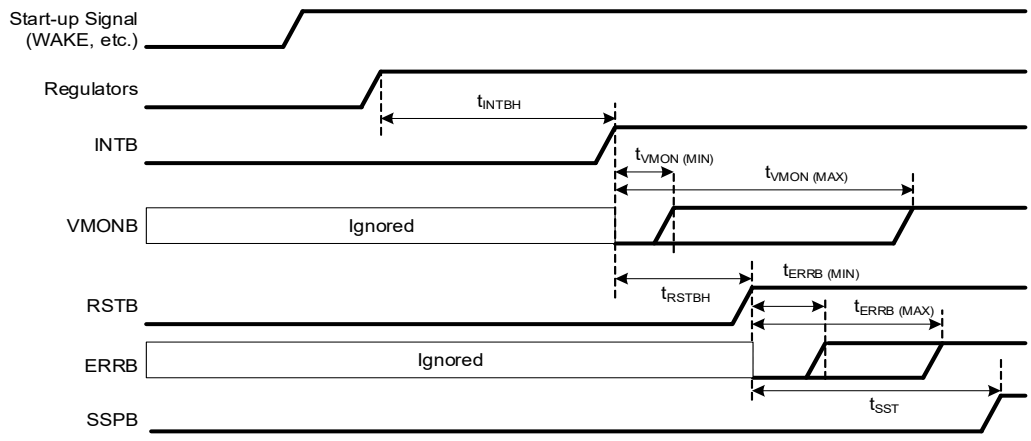


Figure 43. VMONB and ERRB Startup Timing

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
VMONB Fault Detection Timeout	t_{VMON}	Programmable: OPT_VMONB_PER1, VMONB_PER2	227ns	-	477ms	-
ERRB Fault Detection Timeout	t_{ERRB}	Programmable: OPT_ERRB_PER1, ERRB_PER2	227ns	-	477ms	-

Figure 43 shows an example of VMONB and ERRB timing during a start-up sequence. In this timing diagram, OPT_VMONB_RSTB_WAIT is set to 0, so RSTB does not wait for VMONB to go high before it is released. If OPT_VMONB_RSTB_WAIT was set to 1, RSTB would not be released high until VMONB was asserted high.

5.3.9 Watchdog Timer

The RAA271084 has a multi-function watchdog timer (WDT) to support detection of errant MCU software operation. The WDT supports basic windowed kicking, 4QA, and 16QA (ASIL-D only) using SPI and pin-based kicking on the WDENB pin. Available error and timeout accumulators with threshold settings create a credit-based system for some tolerance to kick errors.

The WDT must be configured and enabled by the SPI host for setting operational modes and timeouts appropriate for the application. Enabling is available during the SYSTEM SELF TEST and ACTIVE states of the PMIC by issuing a start command using the WDT_START bit. The WDT automatically disables when transitioning into low power states and must be reconfigured before restart.

Figure 44 shows the block diagrams and associated SPI registers for the WDT function. A detailed description of the WDT feature set follows.

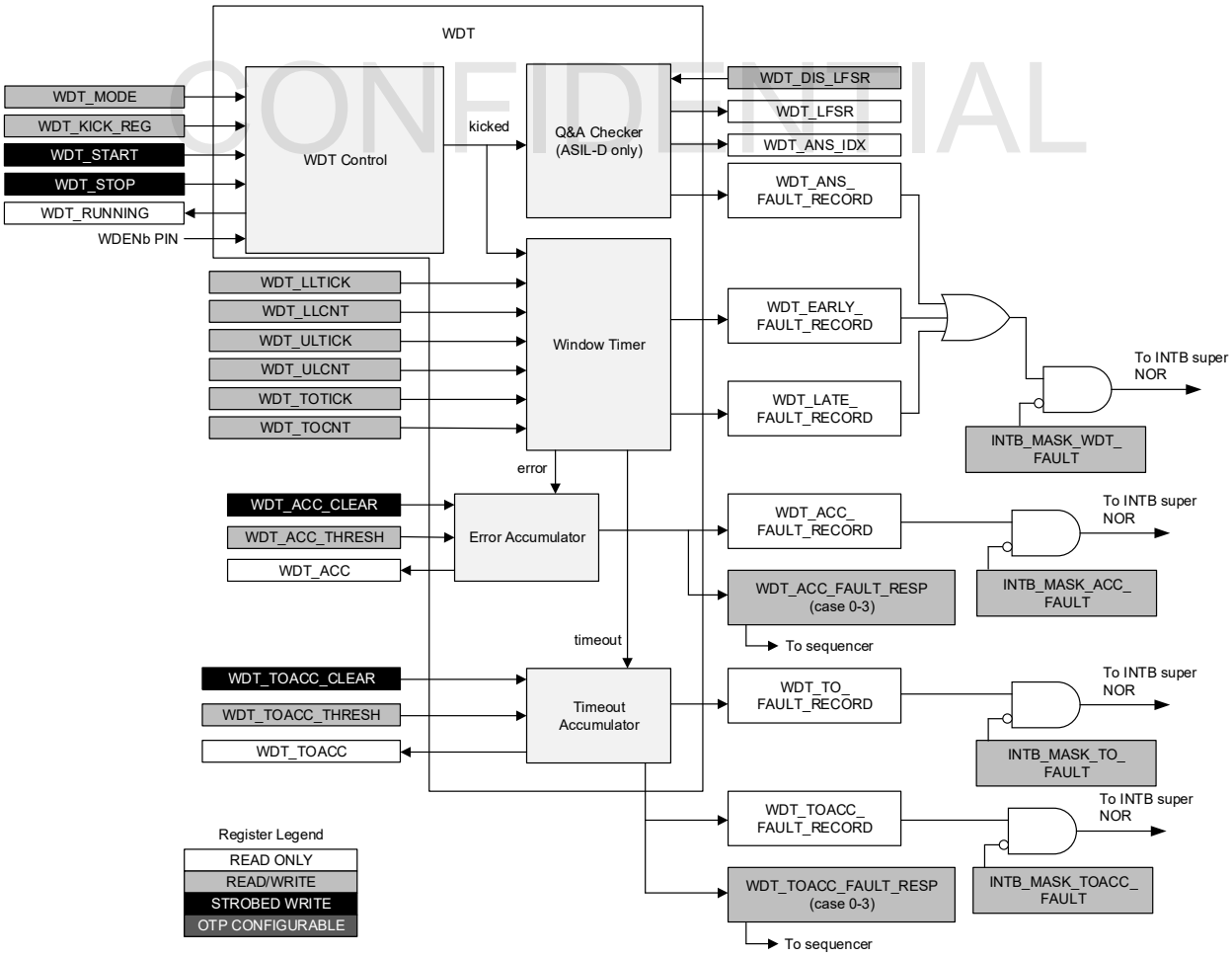


Figure 44. WDT

The PMIC uses SPI writes to the WDT_KICK_REG register or optionally a WDENB pin change to detect periodic activity from a host system to ensure system health. The WDT uses an open window (OW)/closed window (CW) timer concept to measure periods between kicks as shown in Figure 45. Kicking the WDT too frequently or too infrequently can indicate a system software problem potentially requiring a reset for the host or PMIC itself.

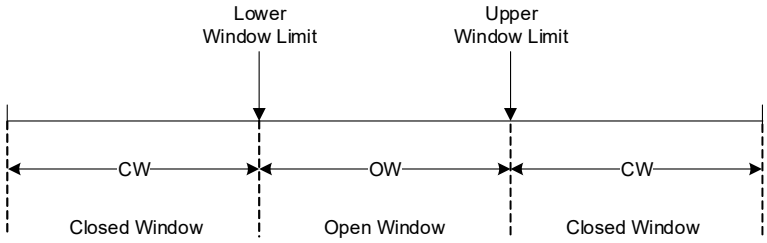


Figure 45. Period Windows and Limits

The WDT_LLTICK and WDT_LLCNT registers set the lower window limit. Kicking more frequently than this period is considered a closed window kick due to being earlier than expected. THE WDT_ULTICK and WDT_ULCNT registers set the upper window limit. Kicking less frequently is also considered a closed window kick due to being later than expected. Between these period settings is an open window kick period considered OK or normal.

The open window/closed window concept has additional programmability for error accumulation, timeouts, and timeout accumulation. Kick data using SPI can also be qualified through a Question and Answer (QA) mechanism (ASIL-D only). Figure 46 shows how these features relate. CW and OW kicks contribute to the WDT_ACC value to create some fault tolerance based on both timing and correct or wrong answers to a PMIC question. Kicks during the OW decrements the error accumulator, while kicks in a CW increments as shown based on answer correctness. A third limit called a timeout is a detection mechanism if the MCU stops providing kicks. Recorded faults can trigger INTB, SSPB, and PMIC reactions as programmed.

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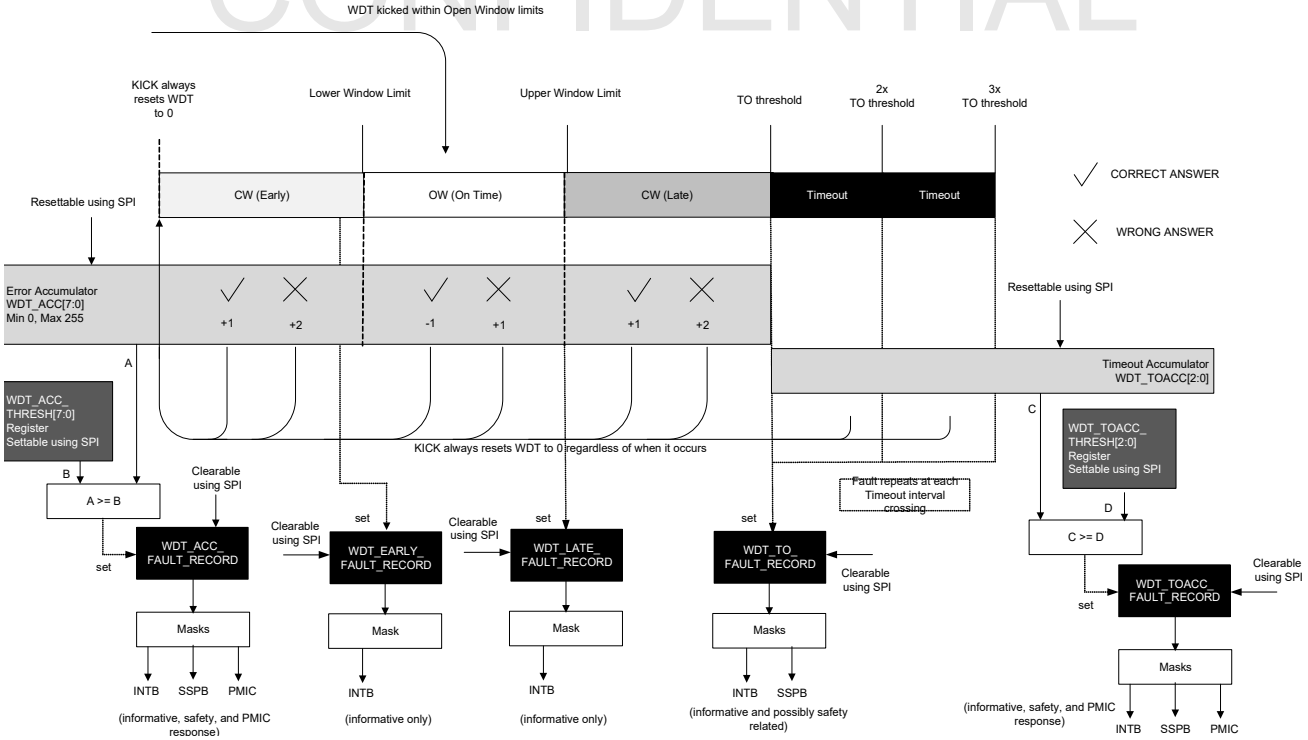


Figure 46. Window, Timeout, and Accumulators

Kick data is supported in three modes; Basic, 4QA, and 16QA (ASIL-D only). The simplest is the Basic mode. A single write of 0x2A to the WDT_KICK_REG or change of the WDENB pin (if enabled) is considered a kick event.

If within the open window, it is considered fault-free. Kicking in a closed window contributes to the WDT fault assertion.

A 4QA mode (ASIL-D only) requires the host to read a single PMIC-provided numerical question and write back an acceptable answer. Writing the answer into the WDT_KICK_REG is considered a kick event. This provides a basic check of host computational integrity. Incorrect answers, even if within the lower and upper limit periods is considered a WDT fault. Bits[7:6] of the WDT_LFSR provide the question token. The answer algorithm for each is shown in Table 22.

Table 22. 4QA WDT Questions/Answers

Token Read from WDT_LFSR		WDT Answer (To be Written Into WDT_KICK_REG[7:0] Register
WDT_LFSR[7]	WDT_LFSR[6]	
0	0	{WDT_LFSR[7:6], WDT_LFSR[5:0]} No changes
0	1	{WDT_LFSR[7:6], (WDT_LFSR[5:0] <<1)} 6 LSBs shift left by 1. Zero filled.
1	0	{WDT_LFSR[7:6], (WDT_LFSR[5:0] >>1)} 6 LSBs shift right by 1. Zero filled.
1	1	{WDT_LFSR[7:6], (WDT_LFSR[5:0])} 6 LSBs logically inverted

A more complex 16QA mode (ASIL-D only) requires a series of 4 unique and sequential answer steps using 16 possible questions. Bits[7:4] of the WDT_LFSR provide the question token for 16QA mode. Writing each answer into the WDT_KICK_REG is considered a single kick event. The first answer (Answer-0) must be provided in the first open window to be considered on-time. The second answer is provided in the next open window and so on. The WDT_ANS_IDX bits (WDT_CONFIG3[3:2]) are provided as an index to inform the system of the location in the 4-answer response sequence. Incorrect answers and too fast or too slow in response times (CW) increment the accumulator. Correct answers with correct timing (OW) decrement the accumulator. If the accumulator meets or exceeds the programmed WDT_ACC_THRESH limit, it is considered a WDT fault.

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Table 23. 16QA Questions/Answers

Question (TOKEN) in WDT_LFSR Register	WD ANSWER (To be written into WDT_KICK_REG Register)			
Token	Answer-0	Answer-1	Answer-2	Answer-3
0x0	0x00	0xF0	0x0F	0xFF
0x1	0x4F	0xBF	0x40	0xB0
0x2	0x16	0xE6	0x19	0xE9
0x3	0x59	0xA9	0x56	0xA6
0x4	0x8A	0x7A	0x85	0x75
0x5	0xC5	0x35	0xCA	0x3A
0x6	0x9C	0x6C	0x93	0x63
0x7	0xD3	0x23	0xDC	0x2C
0x8	0x2D	0xDD	0x22	0xD2
0x9	0x62	0x92	0x6D	0x9D
0xA	0x3B	0xCB	0x34	0xC4
0xB	0x74	0x84	0x7B	0x8B
0xC	0xA7	0x57	0xA8	0x58
0xD	0xE8	0x18	0xE7	0x17
0xE	0xB1	0x41	0xBE	0x4E
0xF	0xFE	0x0E	0xF1	0x01

The SST and WDT timer start up can be controlled using the WDENB pin when WDT_PIN_KICK_CTRL is 0 as follows:

- SST timer is disabled if the OPT_SST_WDENB_CTRL is 0 and the WDENB pin is detected high at SYSTEM_SELF_TEST state entry. Otherwise, the SST timer can run.
- WDT is disabled if OPT_WDT_WDENB_CTRL is 0 and the WDENB pin is detected high at ACTIVE state entry. Otherwise, the WDT timer can run.

When each timer starts operation, setting the WDENB pin cannot stop the timer.

5.3.10 Engine Off Timer

The Engine Off Timer (EOT) function contains a 24-bit count-up timer and an auxiliary 6-bit count down timer operating from a free-running internal 32kHz PMIC oscillator. SPI access for reading and programming the timers is available at any time the RAA271084 is not in the OFF state. Counting rate is 1Hz with a SPI selectable 32768Hz speed up mode to assist with oscillator calibration.

The 24-bit EOT count-up timer is SPI resettable to 0x000000 and increments to a maximum of 0xFFFFFF without rollover. An overflow alarm asserts at maximum value. A SPI programmable wake-up register is available to create wake-up alarms when the EOT reaches or exceeds the programmed WU value. Up counting of the timer can be paused using SPI control. At a 1Hz count rate, the 24-bit timer provides a maximum of 194 days of engine off timing.

The 6-bit count-down timer is SPI settable to 0x3F (63) and decrements to a minimum of 0x00 without underflow. An alarm is available to assert when zero is reached. Down counting of the timer can be paused using SPI control.

When started, the EOT runs even when WAKE1 and WAKE2 are low and until the PMIC is disabled by removing the VBAT supply.

Alarms can drive the INTB pin and optionally trigger PMIC power state changes. Recorded alarms are clearable using SPI. A block diagram of the EOT is shown in Figure 47.

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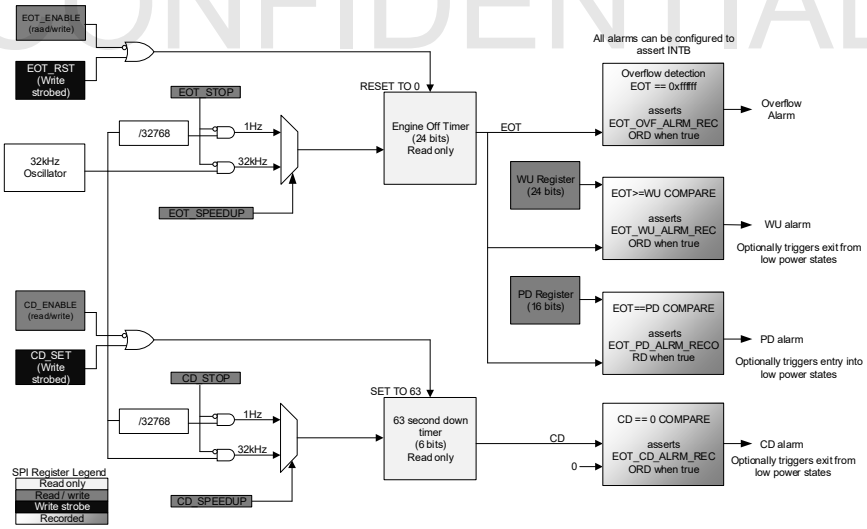


Figure 47. Engine Off Timer

This following describes the sequence used to exit DeepSTOP mode using the EOT wake-up alarm.

Programming setup:

1. Write EOT_WU0, EOT_WU1, and EOT_WU2 to set the wake-up event time
2. Set EOT_WU_CTRL to 1 to wake from DeepSTOP and return to Active mode
3. Set the WU_ALARM_EN bit to 1 to enable the wake-up alarm
4. Set the EOT_ENABLE bit to 1 to enable the EOT. The EOT starts at this point in time.

5. Enter the DeepSTOP mode by either driving the PWRCTRLB pin low or by setting the PWRCTRLB_MODE bit field to b10 (internally sets the state of the PWRCTRLB logic to 0).

PMIC is in DeepSTOP mode at this point until the wake-up alarm is triggered.

When the wake-up alarm is triggered and the PMIC is running again, the following sequence must be followed:

1. Drive the PWRCTRLB pin high if pin control was used to enter DeepSTOP, or write the PWRCTRLB_MODE bit field to b00 (transparent, use pin control for DeepSTOP) or b11 (internally sets the state of the PWRCTRLB logic to 1).
2. Write the EOT_WU_CTRL bit to 0 to restore pin/SPI control of DeepSTOP mode.

Complete the following sequence to turn off and reset EOT timer.

1. Reset WU_ALARM_RECORD to 0.
2. Reset WU_ALARM_EN to 0.
3. Reset EOT_ENABLE to 0.

Use the following sequence to exit EOT mode using the EOT wake-up alarm.

Programming setup:

1. Write EOT_WU0, EOT_WU1, and EOT_WU2 to set the wakeup event time.
2. Set EOT_WU_CTRL to 3 to wake from EOT_ONLY and return to Active mode.
3. Set the WU_ALARM_EN bit to 1 to enable the wakeup alarm.
4. Set the EOT_ENABLE bit to 1 to enable the EOT. The EOT starts at this point in time.
5. Enter the EOT mode by either driving both WAKE1 and WAKE2 pins low or by setting the WAKE1_MODE and WAKE2_MODE bit field to b10 (internally sets the state of the WAKE1 and WAKE2 logic to 0).

PMIC is in EOT_ONLY mode at this point until the wakeup alarm is triggered.

After the wakeup alarm is triggered and the PMIC is running again, the following sequence must be followed.

1. Drive at least one of the WAKE pins high if pin control was used to enter EOT_ONLY, or write the WAKE1_MODE or WAKE2_MODE bit field to b00 (transparent, use pin control for EOT_ONLY) or b11 (internally sets the state of the WAKE1 or WAKE2 logic to 1).
2. Write the EOT_WU_CTRL bit to 0 to restore pin/SPI control of EOT_ONLY mode.

To turn off and reset EOT timer:

1. Reset WU_ALARM_RECORD to 0.
2. Reset WU_ALARM_EN to 0.
3. Reset EOT_ENABLE to 0.

5.3.11 Internal Signal Multiplexer function (AMUX)

RAA271084 (ASIL-D only) contains a multiplexer output pin (AMUX) that can send out either analog or digital signals. Control of the AMUX function is achieved by using the SPI interface. The main function of AMUX is to interface with a load MCU Analog to Digital converter, so that the MCU can check the health of signals inside RAA271084.

Analog MUX outputs are optionally sent through an analog buffer with a small but known offset voltage. The offset voltage of the AMUX analog buffer is measured during ATE test and stored in a signed 6-bit register, OPT_AMUX_BUF_OFFSET, with a weight of 1mV/bit (maximum 31mV, minimum -32mV). A full block diagram of AMUX being used with analog signals is shown in Figure 48. AMUX signal options are shown in register 0x32, AMUX_SEL. If the AMUX multiplexer is enabled in active mode, it is not automatically disabled when RAA271084 enters EOT mode, which increases current consumption in EOT mode. Therefore, the AMUX function should be disabled by setting AMUX_SEL to 0x0 before entering EOT mode to avoid unnecessary power consumption. It is also recommended to set AMUX_SEL to 0x0 whenever the AMUX function is not in use.

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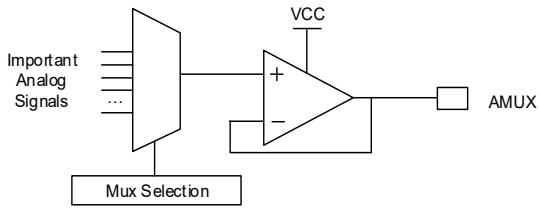


Figure 48. AMUX Analog Signal Block Diagram

Accuracy of the AMUX output varies depending on the divide ratio of the analog signal and the residual offset error of the buffer after applying the calibration factor. The residual offset error is approximately equal to the LSB size of the calibration, 1mV, plus an additional offset error of up to 3mV that is due to uncalibrated temperature shifts. The expected accuracy for each divide ratio, not including residual offset error, is shown in Table 24. This does not include any accuracy errors associated with the voltage being measured, such as ±2% DC accuracy of an LDO output.

Table 24. AMUX Analog Output Accuracy

Divide Ratio	Accuracy
0.025	2.3%
0.2	0.9%
0.25	0.7%

AMUX can also be used with digital signals, where the output is driven by a buffer powered from VDDIO. A block diagram of digital buffer is shown in Figure 49.

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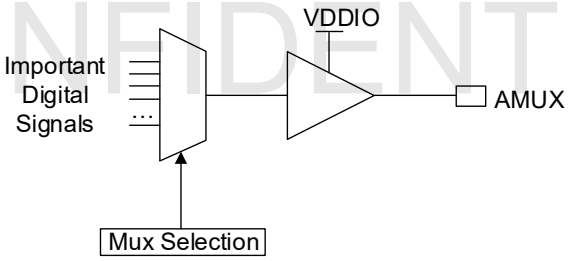


Figure 49. AMUX with Digital Signals Block Diagram

6. Power Management Features

6.1 VCC Regulator, LDO0

The RAA271084 derives its internal supply rail, VCC, from an onboard LDO (LDO0). LDO0 output is generated from either HVLDO or LVLDO. At startup, and before DCDC1 is regulating, HVLDO gets its input from VBAT and supplies VCC to the system. When DCDC1 is regulating and providing 5.7V to the VIN2 pin, LDO0 is automatically switched over to LVLDO to provide VCC more efficiently. This switchover is done to minimize the power dissipation inside the LDO0 pass FET.

LDO0 regulates to 5V only and has low Iq of 10µA at no load. HVLDO can supply up to 130mA and LVLDO can supply up to 220mA. This supply current provides 10mA internal to the PMIC and also all gate drive current to external DCDC1 and DCDC2 FETs (assuming VCCP is connected to VCC external to the PMIC). The current requirement of the external FETs can be calculated for each of the FETs as $Q_G \times f_{SW}$, where Q_G is the gate charge of the FET and f_{SW} is the switching frequency. LDO0 has current limiting circuitry, which protects against a short-to-GND condition, while the OV2_PD circuitry can assert High at a VCC severe overvoltage condition. The output voltage of LDO0 is monitored by UV and OV monitors in the functional safety block.

6.1.1 Start-Up Operation

The start-up procedure requires that VBAT is greater than the startup threshold, V_{BAT_SU}, typically 4.5V. When VBAT > V_{BAT_SU}, the WAKE pin can be asserted to begin the startup process. The WAKE pin assertion starts an internal HV (High Voltage) VCC LDO block that drives the LDO0/VCC pin. When VCC rises above 4.2V, POR (Power-On Reset) is cleared on the digital state machine that controls each regulator enable. After POR, the OTP is loaded, ABIST and LBIST are executed, and the RSTB/SSPB pins are self-tested. After BIST (Built in Self Test) is executed, the DCDC1 regulator is enabled and allowed to soft-start. After the DCDC1 regulator output, which is also connected to VIN2, reaches above the HV to LV switchover threshold voltage, typically 5.5V, the LV VCC LDO block is enabled and HV VCC LDO block is disabled. After this point, VCC_LDO0 is supplied from DCDC1/VIN2 thereby helping with reduced quiescent current demand from VBAT. After a delay, the post regulators DCDC2 and LDO1-LDO4 are enabled in a fuse programmed sequence.

6.2 Buck-boost Regulator DCDC1

DCDC1 is an asynchronous, non-inverting buck-boost regulator that can operate from a wide input voltage range of 2.7V to 42V. During normal operation and with an input voltage greater than 7.9V, the gate drive LS1B is pulled low and the converter works in buck mode, only using switches M1 and M2. During cold-crank conditions, when the V_{BAT} voltage falls below 7.6V, LS1B is switched in phase with HS1A and the converter operates in asynchronous buck-boost mode. There is an automatic hand off between buck and buck-boost modes of operation. In buck CCM, $V_{OUT1} = D \times V_{BAT}$, and in buck-boost CCM, $V_{OUT1} = V_{BAT}(D/1-D)$. Alternatively, in buck mode the duty cycle $D = V_{OUT1}/V_{BAT}$. In buck-boost mode the duty cycle $D = V_{OUT1}/(V_{OUT1}+V_{BAT})$.

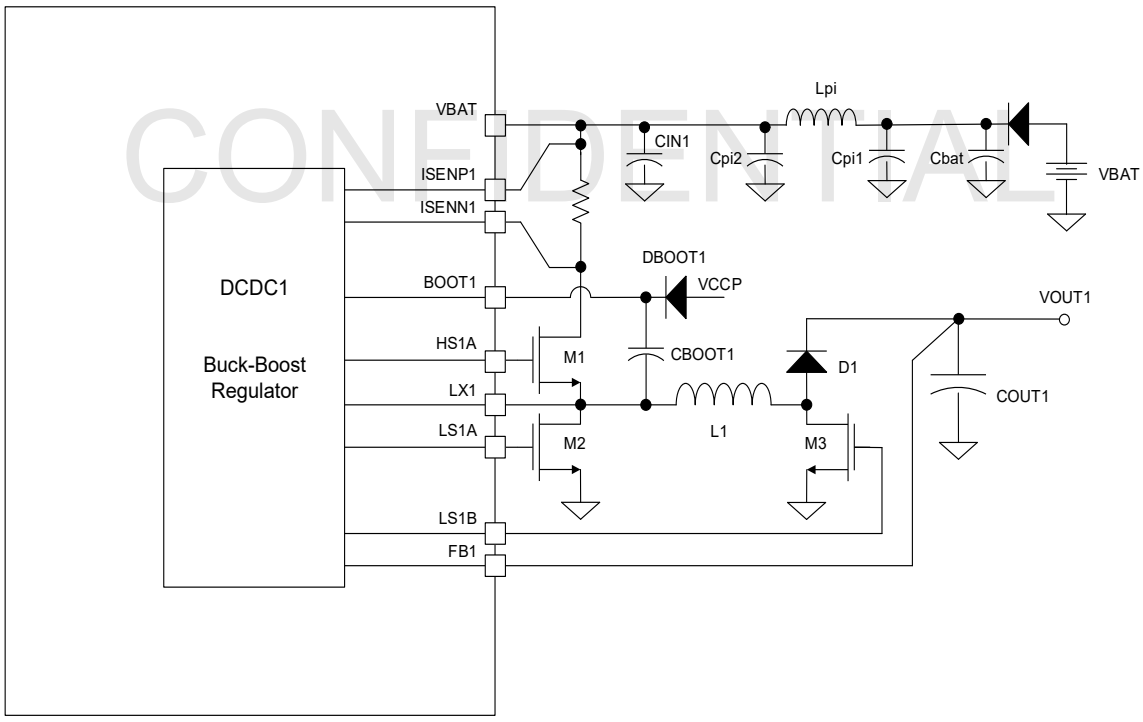


Figure 50. DCDC1 Block Diagram

The DCDC1 also can be configured as a buck only regulator. When DCDC1 is configured as a buck only regulator, the switch M3 can be removed, and the LS1B pin can be left open. When the V_{BAT} voltage falls below 7.6V, the LS1B pin switches but without the switch M3, DCDC1 just works as a buck regulator with the synchronous M1 and M2 switching. When V_{BAT} voltage approaches to VOUT1 output voltage, DCDC1 just enters the dropout operation, that is VOUT1 drops with V_{BAT} until LDO0/VCC reaches its UVLO and RAA271084 shuts down. With buck only mode operation, the output diode D1 also can be removed if the PFM mode is not required, that is if the Power-off Standby and DeepSTOP mode are not required.

6.2.1 DCDC1 Operating Modes

DCDC1 contains internal compensation and has three operating modes: CCM (Continuous Conduction Mode), constant frequency DCM (Discontinuous Conduction Mode), and constant peak PFM (Pulse Frequency Modulation) mode. Under typical load conditions the device operates in CCM mode. As the load drops and the inductor current falls to zero, diode D1 blocks negative current and the regulator operates in DCM mode.

6.2.2 DCDC1 PFM Mode

In Power-off Standby and DeepSTOP modes, DCDC1 uses a PFM (Pulse Frequency Modulation) scheme that issues power pulses at a frequency lower than the programmed switching frequency. The start of a power pulse is initiated by a drop in output voltage below its set reference voltage. First, the high side is turned on until the inductor hits a peak current, then the low side is turned on until the inductor current is zero. If the output is in regulation after the zero cross, then both high and low sides stay off until the output droops again. When in PFM mode, the switching frequency is proportional to the load. As the load increases, the PFM switching frequency also increases until the device eventually exits PFM mode and returns to CCM mode.

6.2.3 DCDC1 Soft-Start

At startup, the converter operates in Soft-Start mode. In this mode, a soft-start reference voltage to the error amplifier is ramped up slowly from zero to V_{REF} through the soft-start DAC circuit. This causes the error amplifier output voltage and the duty cycle of the PWM signal to slowly increase; therefore, avoiding inrush current at the output capacitor during start-up. When the soft-start reference voltage exceeds V_{REF}, the error amplifier output and the PWM duty cycle are dictated by the normal steady state loop behavior and finally settle down to the regulation level.

6.2.4 DCDC1 Overcurrent Limit

DCDC1 has a cycle-by-cycle overcurrent limit protection circuit, where the high-side FET is turned off until the next PWM cycle when the inductor current sensed across the current sense resistor exceeds the OC threshold. It simply truncates the PWM pulse immediately to limit the inductor peak current, and the PWM continues to switch. In buck mode, the OC threshold is 55mV typical and in buck-boost mode the threshold is 165mV typical. In case of an cycle-by-cycle current limit condition, the output voltage of DCDC1 pre-regulator decreases. As long as the overcurrent condition persists, the output voltage continues to decrease until a UV fault is triggered. The OC event flag is stored in an SPI status register and the INTB pin can be configured to assert on an OC event.

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The DCDC1 cycle-by-cycle current limit flags the FAULT_STATUS_7 register 0x106 Bit[4] DCDC1_OC1_FAULT_RECORD, and INTb pin is pulled low if it is not masked for DCDC1 cycle-by-cycle current limit with register OPT_INTB_MASK1 0x140 Bit[2]. While during DCDC1 startup, based on the circuit configuration such as control loop speed, inductor value, startup voltage slew rate, and output capacitance, the startup current charging up the output capacitor could trip the cycle-by-cycle current limit occasionally. This is not a fault condition and cycle-by-cycle current limit flag should be ignored. The fault flag bit can be written 0 to clear, and the INTb signal can be masked as well.

If there is consecutive cycle-by-cycle current limit pulses, for example 16 times by OTP configurable default, it declares a DCDC1 OC2 fault (ASIL-D only).

6.2.5 DCDC1 Undervoltage/Overvoltage Monitors

The output voltage of DCDC1 is monitored by UV/OV monitors in the functional safety block. In case of an undervoltage or an overvoltage condition on the DCDC1 pre-regulator output, DCDC1 is switched off and the device moves into a fail-safe state. The UV/OV flag is stored in SPI status registers.

6.3 Buck Regulator DCDC2

DCDC2 is a synchronous buck converter that converts the pre-regulator DCDC1 5.7V output down to a lower output voltage. The DCDC2 output, V_{OUT2}, is set with a resistor divider from V_{OUT2} to ground with a tap that provides 0.8V to the FB2 pin. A secondary resistor divider from VOUT2 with its tap to the FB2S pin is also provided for functional safety monitoring of the external resistor dividers used by DCDC2. If either resistor string

has a change in the divider tap ratio, the monitor faults because of the error in the ratio. The monitors fault if the regulation loop drives to the wrong voltage or if the monitor loop senses the voltage incorrectly while the regulator is working normally.

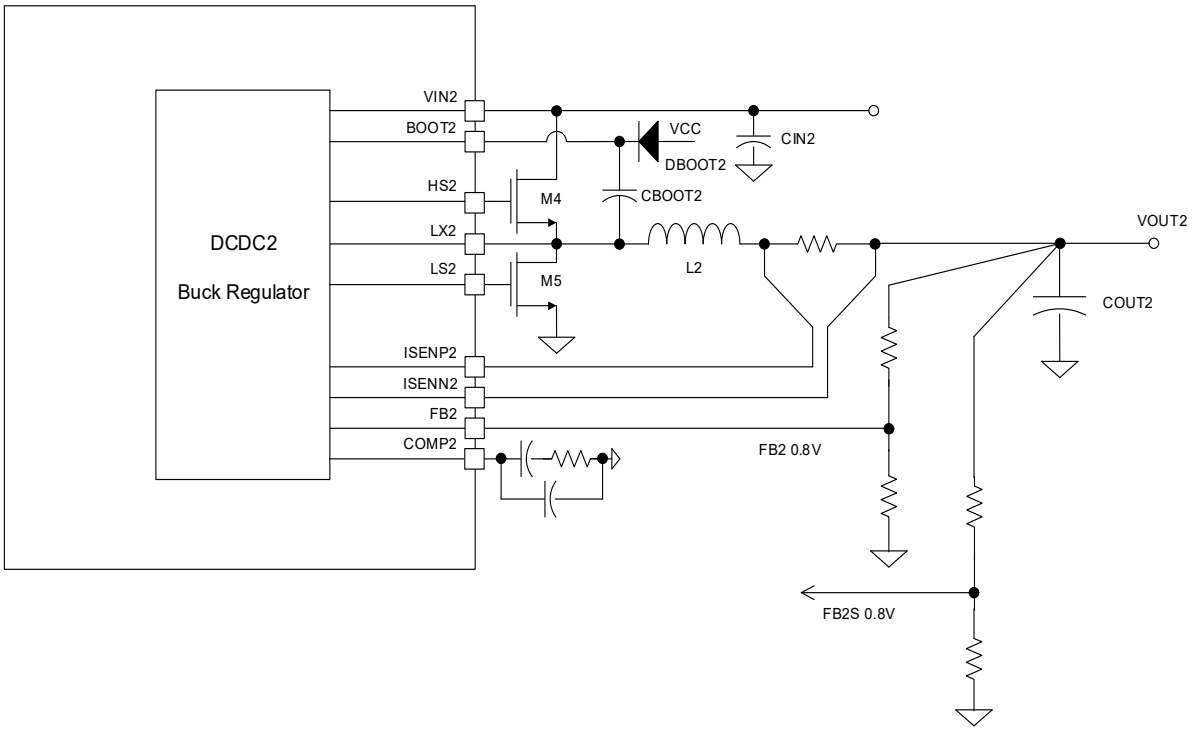


Figure 51. DCDC2 Block Diagram

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6.4 LDO Regulators (LDO1-2)

RAA271084 includes two LDO regulators, each of which has a current capability of 350mA and can be fuse programmed to an output voltage of either 3.3V or 5.0V. LDO1-2 also have current limiting circuitry. This current limit activates when the current across the pass transistor exceeds the OC threshold, limiting the gate drive and hence the current through the pass transistor. If load current is increased beyond the current limit threshold, the output of LDO1-2 begins to decrease quickly.

Table 25. LDO1-2 Recommended Components

Regulator	Input Capacitor	Output Capacitor
LDO1	1.0µF	4.7µF
LDO2	1.0µF	4.7µF

6.5 LDO/Tracker Regulators (LDO3-4)

RAA271084 includes two LDO regulators, each of which has a current capability of 200mA and can be fuse programmed to an output voltage of either 3.3V or 5.0V. LDO3-4 can also be fuse configured to function as tracker supplies, where the output voltage tracks the voltage of an external input pin (VTR3/4) to supply off-board sensors. The Tracker output voltage ranges from 2.2V to the Severe OV threshold, according to the output voltage 3.3V or 5V setting and the Severe OV threshold setting.

Since LDO3-4 can be configured as tracker LDOs to be used with off-module circuit, they have protection for shorts to VBAT, GND and block the reverse current whenever there is output severe OV event. This function is also valid for LDO3-4 configured as normal LDO.

Table 26. LDO3-4 Recommended Components

Regulator	Input Capacitor	Output Capacitor
LDO3	1.0µF	4.7µF
LDO4		4.7µF

6.6 VDDIO Supply Input

The VDDIO pin is the PMIC input supply for the input buffers and output drivers. It is expected that one of the PMIC regulator outputs is connected to the VDDIO pin. Because these regulators are turned on or off depending on the various PMIC fault responses and low power modes, the PMIC requires a register setting to select a specific regulator to associate with the VDDIO input. This selection provides the internal PMIC logic with the information necessary to accommodate instances when VDDIO is powered down and to differentiate a situation where a fault is present such as a broken bond wire. This register is OPT_VDDIO 0x20E. This register must be fused with the correct setting based on the system actual connection of VDDIO.

There is an internal VDDIO_OK comparator used for VDDIO input voltage detection. The VDDIO_OK rising threshold is 2.5V and the falling threshold is 2.0V. If the VDDIO_OK falling threshold is crossed when the VDDIO regulator is enabled, a VDDIO_OK fault is indicated in the VDDIO_OK_FAULT_RECORD bit. OPT_VDDIO_FLT_RESP sets the PMIC fault response when the VDDIO_OK fault is triggered. There is also capability to mask VDDIO_OK faults on INTB (OPT_INTB_MASK_VDDIO_FAULT) and SSPB (OPT_SSPB_MASK_VDDIO_FAULT).

6.7 DCDC1 Severe Overvoltage Protection and OV2_PD Function

The DCDC1 output (VOUT1) might be exposed to momentary or pulsed overvoltage in case of its input voltage up and down glitch causing VOUT1 dropout then recover, or large transient load release event. To avoid severe overvoltage exceeding the RAA271084 and RAA271084-B VOUT1 connected pins voltage rating, Renesas recommends enabling the DCDC1 severe overvoltage Case 2 or Case 3 fault response (configured by register 0x121 Bits[3:2]). This ensures that DCDC1 shuts down during a severe overvoltage event.

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RAA271084 and RAA271084-B also includes a DCDC1 output VOUT1 overvoltage detection function called OV2_PD as redundant protection option. This function detects VOUT1 severe overvoltage through the FB1 pin. The OV2_PD pin asserts high if the overvoltage is higher than 7V typical and becomes low when the overvoltage drops below 6.82V typical. Therefore, the OV2_PD signal can control a FET switch to pull down the VOUT1 overvoltage and limits its amplitude from damaging the VOUT1 connected pins. Series a resistor Rpd with the pull-down FET Qpd to limit the pull-down current while also guarantee quick overvoltage pulling down.

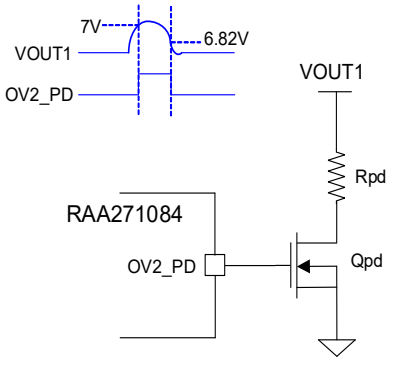


Figure 52. OV2_PD Controlled VOUT1 Overvoltage Pull-Down

7. Registers

This section contains the RAA271084 SPI register map.

Type	Description
R	Readable
W	Writable
F	Default value selectable by fuse. Default column lists value before fuse programming.
W1S	Writing a 1 assertion action. Writing a 0 has no effect.
RW0C	Register is readable. Writing a 0 clears fault status bit. Bit remains cleared if fault was removed. Writing a 1 has no effect.

7.1 DEV_ID_LO_BYTE - 0x00

Name	Bit	Type	Default	Description
ID_LO_BYTE	7:0	R	0x84	Low byte identifier for the RAA271084.

7.2 DEV_ID_HI_BYTE - 0x01

Name	Bit	Type	Default	Description
ID_HI_BYTE	7:0	R	0x10	High byte identifier for the RAA271084.

7.3 DEV_REV_LO_BYTE - 0x02

Name	Bit	Type	Default	Description
REV_LO_BYTE	7:0	R	0x01	Device revision low byte.

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7.4 DEV_REV_HI_BYTE - 0x03

Name	Bit	Type	Default	Description
REV_HI_BYTE	7:0	R	0x0C	Device revision high byte.

7.5 SEQ_STATUS - 0x04

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
LDO4_ENABLED	5	R	0x0	Sequencer status for LDO4 0 = Disabled 1 = Enabled
LDO3_ENABLED	4	R	0x0	Sequencer status for LDO3 0 = Disabled 1 = Enabled
LDO2_ENABLED	3	R	0x0	Sequencer status for LDO2 0 = Disabled 1 = Enabled
LDO1_ENABLED	2	R	0x0	Sequencer status for LDO1 0 = Disabled 1 = Enabled

Name	Bit	Type	Default	Description
DCDC2_ENABLED	1	R	0x0	Sequencer status for DCDC2 0 = Disabled 1 = Enabled
DCDC1_ENABLED	0	R	0x0	Sequencer status for DCDC1 0 = Disabled 1 = Enabled

7.6 PG_STATUS - 0x05

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
LDO0_PG	6	R	0x0	LDO0 power-good status 0 = Not good 1 = Good
LDO4_PG	5	R	0x0	LDO4 power-good status 0 = Not good 1 = Good
LDO3_PG	4	R	0x0	LDO3 power-good status 0 = Not good 1 = Good
LDO2_PG	3	R	0x0	LDO2 power-good status 0 = Not good 1 = Good
LDO1_PG	2	R	0x0	LDO1 power-good status 0 = Not good 1 = Good
DCDC2_PG	1	R	0x0	DCDC2 power-good status 0 = Not good 1 = Good
DCDC1_PG	0	R	0x0	DCDC1 power-good status 0 = Not good 1 = Good

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7.7 DCDC_STATE - 0x08

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
DCDC2_STATE	3:2	R	0x0	DCDC2 Controller State 0 = Idle 1 = Soft start 2 = Normal 3 = Discharge
DCDC1_STATE	1:0	R	0x0	DCDC2 Controller State 0 = Idle 1 = PWM 2 = PFM 3 = Discharge

7.8 LDO_STATE - 0x09

Name	Bit	Type	Default	Description
LDO4_STATE	7:6	R	0x0	LDO4 Controller State 0 = Idle 1 = Soft start 2 = Normal 3 = Discharge
LDO3_STATE	5:4	R	0x0	LDO3 Controller State 0 = Idle 1 = Soft start 2 = Normal 3 = Discharge
LDO2_STATE	3:2	R	0x0	LDO2 controller state 0 = Idle 1 = Soft start 2 = Normal 3 = Discharge
LDO1_STATE	1:0	R	0x0	LDO1 controller state 0 = Idle 1 = Soft start 2 = Normal 3 = Discharge

7.9 CONTROLLER_STATE - 0x0A

Name	Bit	Type	Default	Description
SEQUENCER_STATE	7:4	R	0x0	Regulator sequencer controller state 0 = OFF: POR state. Wait for WAKE high to start regulators 1 = START_DCDC1: VCC is powered, DCDC1 is in startup phase 2 = EOT_ONLY: PMIC is in EOT_ONLY state 3 = POWER_UP: DCDC2, LDO1 through 4 are in startup phase 4 = REGS_UP: All regulators are up and running 5 = POWER_DN: All regulators shut down in sequence 6 = DEEP_STOP: PMIC is in DeepSTOP state 7 = PSTBY_DN: Regulators shut down in sequence, except for DCDC1 8 = PSTBY: PMIC is in PSTBY state 9 = NA 10 = FAULT_REG: Wait 10ms before restart attempt after shutdown due to fault. This is applicable to the Case 2 fault response with automatic restart attempts. 11 = FAULTED: Faulted latch-off state. Applicable to Case 2 fault response. 12 = FAULTED_OFF: Ready to restart from fault 13 = POWER_UP FROM DS_0: Transitional state to load the slot timer configuration for DeepSTOP exit 14 = POWER_UP FROM DS_1: Rails wake up from DeepSTOP in sequence 15 = FAULTED_DN: Rails shutdown in sequence after fault
Reserved	3	R	0x0	-
INIT_STATE	2:0	R	0x0	INIT controller state 0 = INIT_WAIT: After POR wait for WAKE high to proceed 1 = FUSE_RECALL: OTP being loaded to registers 2 = EN_AZ: Regulator and FuSa monitors being calibrated 3 = EN_FUSA: FuSa monitors enabled following ABIST/LBIST 4 = EN_REGS: Regulators enabled

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7.10 FUSA_STATE - 0x0B

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	-
FUSA_EN	4	R	0x0	FuSa Monitor State 0 = Monitors disabled 1 = Monitors enabled
Reserved	3	R	0x0	-
FUSA_STATE	2:0	R	0x0	FuSa FSM State 0 = OFF: FuSa monitors off 1 = STARTUP_MON: FuSa monitors starting up 2 = SYSTEM_SELF_TEST: PMIC in System Self-Test state 3 = VMON_DETECT: PMIC in VMON detect state 4 = NA 5 = NA 6 = ACTIVE: PMIC in ACTIVE state 7 = DEEPSTOP: PMIC in DeepSTOP state

7.11 OPT_SEQ_CTRL - 0x10

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	-
OPT_EN_DS_SLOT	4	FRW	0x0	Controls slot timing usage at the exit of DeepSTOP state 0 = Regulators are enabled as soon as possible when exiting DeepSTOP 1 = Regulators follow slot timing sequence when exiting DeepSTOP
Reserved	3:0	R	0x0	-

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7.12 OPT_SLOT_TIME - 0x11

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_SLOT3_TIME	5:4	FRW	0x0	Sets delay time between slot 2 and slot 3 0 = 0ms 1 = 1ms 2 = 2ms 3 = 5ms
OPT_SLOT2_TIME	3:2	FRW	0x0	Sets delay time between slot 1 and slot 2 0 = 0ms 1 = 1ms 2 = 2ms 3 = 5ms
OPT_SLOT1_TIME	1:0	FRW	0x0	Sets delay time between slot 0 and slot 1 0 = 0ms 1 = 1ms 2 = 2ms 3 = 5ms

7.13 OPT_SLOT_DCDC - 0x12

Name	Bit	Type	Default	Description
Reserved	7:2	R	0x0	-
OPT_SLOT_DCDC2	1:0	FRW	0x0	Startup slot assignment for DCDC2 0 = Slot 0 1 = Slot 1 2 = Slot 2 3 = Slot 3

7.14 OPT_SLOT_LDO - 0x13

Name	Bit	Type	Default	Description
OPT_SLOT_LDO4	7:6	FRW	0x0	Startup slot assignment for LDO4 0 = Slot 0 1 = Slot 1 2 = Slot 2 3 = Slot 3
OPT_SLOT_LDO3	5:4	FRW	0x0	Startup slot assignment for LDO3 0 = Slot 0 1 = Slot 1 2 = Slot 2 3 = Slot 3
OPT_SLOT_LDO2	3:2	FRW	0x0	Startup slot assignment for LDO2 0 = Slot 0 1 = Slot 1 2 = Slot 2 3 = Slot 3
OPT_SLOT_LDO1	1:0	FRW	0x0	Startup slot assignment for LDO1 0 = Slot 0 1 = Slot 1 2 = Slot 2 3 = Slot 3

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7.15 OPT_HP - 0x14

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_HP_LDO4_DIS	5	FRW	0x0	LDO4 control in high power states (initialization and ACTIVE states) 0 = Enabled 1 = Disabled
OPT_HP_LDO3_DIS	4	FRW	0x0	LDO3 control in high power states (initialization and ACTIVE states) 0 = Enabled 1 = Disabled
OPT_HP_LDO2_DIS	3	FRW	0x0	LDO2 control in high power states (initialization and ACTIVE states) 0 = Enabled 1 = Disabled
OPT_HP_LDO1_DIS	2	FRW	0x0	LDO1 control in high power states (initialization and ACTIVE states) 0 = Enabled 1 = Disabled

Name	Bit	Type	Default	Description
OPT_HP_DCDC2_DIS	1	FRW	0x0	DCDC2 control in high power states (initialization and ACTIVE states) 0 = Enabled 1 = Disabled
Reserved	0	R	0x0	-

7.16 OPT_DS - 0x15

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_DS_LDO4_DIS	5	FRW	0x0	LDO4 control in DeepSTOP 0 = Enabled 1 = Disabled
OPT_DS_LDO3_DIS	4	FRW	0x0	LDO3 control in DeepSTOP 0 = Enabled 1 = Disabled
OPT_DS_LDO2_DIS	3	FRW	0x0	LDO2 control in DeepSTOP 0 = Enabled 1 = Disabled
OPT_DS_LDO1_DIS	2	FRW	0x0	LDO1 control in DeepSTOP 0 = Enabled 1 = Disabled
OPT_DS_DCDC2_EN	1	FRW	0x0	DCDC2 control in DeepSTOP 0 = Disabled 1 = Enabled
Reserved	0	R	0x0	-

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7.17 OPT_TOFF_TIME - 0x16

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_TOFF_DLY_LDO4	5	FRW	0x0	LDO4 Disable to off time 0 = 100µs 1 = 1ms
OPT_TOFF_DLY_LDO3	4	FRW	0x0	LDO3 Disable to off time 0 = 100µs 1 = 1ms
OPT_TOFF_DLY_LDO2	3	FRW	0x0	LDO2 Disable to off time 0 = 100µs 1 = 1ms
OPT_TOFF_DLY_LDO1	2	FRW	0x0	LDO1 Disable to off time 0 = 100µs 1 = 1ms
OPT_TOFF_DLY_DCDC2	1	FRW	0x0	DCDC2 Disable to off time 0 = 100µs 1 = 1ms
Reserved	0	R	0x0	-

7.18 DCDC_CTRL - 0x20

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
DCDC2_STOP	3	W1S	0x0	Writing a 1 disables DCDC2 supply. 0 = Ignored 1 = Stop
DCDC2_START	2	W1S	0x0	Writing a 1 enables DCDC2 supply. 0 = Ignored 1 = Start
DCDC1_STOP	1	W1S	0x0	Writing a 1 disables DCDC1 supply. 0 = Ignored 1 = Stop
DCDC1_START	0	W1S	0x0	Writing a 1 enables DCDC1 supply. 0 = Ignored 1 = Start

7.19 LDO_CTRL - 0x21

Name	Bit	Type	Default	Description
LDO4_STOP	7	W1S	0x0	Writing a 1 disables LDO4 supply. 0 = Ignored 1 = Stop
LDO4_START	6	W1S	0x0	Writing a 1 enables LDO4 supply. 0 = Ignored 1 = Start
LDO3_STOP	5	W1S	0x0	Writing a 1 disables LDO3 supply. 0 = Ignored 1 = Stop
LDO3_START	4	W1S	0x0	Writing a 1 enables LDO3 supply. 0 = Ignored 1 = Start
LDO2_STOP	3	W1S	0x0	Writing a 1 disables LDO2 supply. 0 = Ignored 1 = Stop
LDO2_START	2	W1S	0x0	Writing a 1 enables LDO2 supply. 0 = Ignored 1 = Start
LDO1_STOP	1	W1S	0x0	Writing a 1 disables LDO1 supply. 0 = Ignored 1 = Stop
LDO1_START	0	W1S	0x0	Writing a 1 enables LDO1 supply. 0 = Ignored 1 = Start

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7.20 OPT_ERRB_CTRL1 - 0x30

Name	Bit	Type	Default	Description
OPT_ERRB_MODE	7:6	FRW	0x0	Sets level or edge mode for the ERRB timer. 0 = ERRB low runs ERRB timer count down. ERRB high sets and holds timer at ERRB_PER. 1 = ERRB first rising edge starts ERRB timer count down. Additional rising edges reset timer. Timer period set by ERRB_PER 2 = Reserved 3 = Reserved
Reserved	5	FRW	0x0	Set to 0
OPT_ERRB_PER1	4:0	FRW	0x0	Sets ERRB timer value for Mode 0. Set to 0 for Mode 1 (Use ERRB_PER2 for Mode 1). Tolerance is ±25% 0 = ERRB input ignored 1 = 227ns 2 = 455ns 3 = 909ns 4 = 1.818µs 5 = 3.636µs 6 = 7.273µs 7 = 14.454µs 8 = 29.091µs 9 = 58.182µs 10 = 116.364µs 11 = 232.7µs 12 = 465.5µs 13 = 930.9µs 14 = 1.8629ms 15 = 3.724ms 16 = 7.45ms 17 = 14.89ms 18 = 29.79ms 19 = 59.58ms 20 = 119.2ms 21 = 238.3ms 22 = 476.6ms

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7.21 OPT_VMONB_CTRL1 - 0x31

Name	Bit	Type	Default	Description
OPT_VMONB_RSTB_WAIT	7	FRW	0x0	Selects if RSTB must wait for VMONB high 0 = RSTB startup does not wait for VMONB 1 = RSTB must wait for VMONB high at startup
Reserved	6:5	R	0x0	-
OPT_VMONB_PER1	4:0	FRW	0x00	Sets VMONB timer value. Tolerance is ±25% 0 = VMONB input ignored 1 = 227ns 2 = 455ns 3 = 909ns 4 = 1.818µs 5 = 3.636µs 6 = 7.273µs 7 = 14.454µs 8 = 29.091µs 9 = 58.182µs 10 = 116.364µs 11 = 232.7µs 12 = 465.5µs 13 = 930.9µs 14 = 1.8629ms 15 = 3.724ms 16 = 7.45ms 17 = 14.89ms 18 = 29.79ms 19 = 59.58ms 20 = 119.2ms 21 = 238.3ms 22 = 476.6ms Others = Reserved

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7.22 AMUX_SEL - 0x32 (ASIL-D only)

Name	Bit	Type	Default	Description
AMUX_OD_SEL	7	RW	0x0	Drive control when digital signals are output on AMUX pin. Applies only when AMUX_SEL[4:0] is > 16 (decimal). Otherwise ignored. 0 = Use push/pull 1 = Use open drain
Reserved	6:5	R	0x0	-
AMUX_SEL	4:0	RW	0x0	Selection control for AMUX pin 0 = AMUX disabled 1 = VCC 5V Regulation voltage / 4 2 = VCC 5V Safety voltage / 4 3 = Reserved 4 = 1.200V VREF Regulation voltage 5 = 1.200V VREF Safety voltage 6 = GND 7 = VDDIO / 4 voltage 8 = Temp Sensor 9 = VBAT voltage / 40 10 = DCDC1 feedback voltage / 5 11 = DCDC2 feedback voltage 12 = LDO1 VOUT voltage / 4 13 = LDO2 VOUT voltage / 4 14 = LDO3 VOUT voltage / 4 15 = LDO4 VOUT voltage / 4 16 = Tracker input VTR3/4 / 4 17 = EOT Clock (32768Hz) [digital] 18 = System clock (17.6MHz/64) [digital]

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7.23 ERRB_CTRL2 - 0x34

Name	Bit	Type	Default	Description
ERRB_PER_USED	7	R	0x0	Reports the period register currently being used by the ERRB monitor 0 = OPT_ERRB_PER1 value in use 1 = ERRB_PER2 value in use
Reserved	6:5	RW	0x0	Set to 0
ERRB_PER2	4:0	RW	0x0	Sets ERRB timer value. Tolerance is ±25% 0 = ERRB input ignored 1 = 227ns 2 = 455ns 3 = 909ns 4 = 1.818µs 5 = 3.636µs 6 = 7.273µs 7 = 14.454µs 8 = 29.091µs 9 = 58.182µs 10 = 116.364µs 11 = 232.7µs 12 = 465.5µs 13 = 930.9µs 14 = 1.8629ms 15 = 3.724ms 16 = 7.45ms 17 = 14.89ms 18 = 29.79ms 19 = 59.58ms 20 = 119.2ms 21 = 238.3ms 22 = 476.6ms

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7.24 VMONB_CTRL2 - 0x35

Name	Bit	Type	Default	Description
VMONB_PER_USED	7	R	0x0	Reports the period register currently being used by the VMONB monitor 0 = OPT_VMONB_PER1 value in use 1 = VMONB_PER2 value in use
Reserved	6:5	R	0x0	Set to 0
VMONB_PER2	4:0	RW	0x0	Sets secondary VMONB timer value. Tolerance is ±25% 0 = VMONB input ignored 1 = 227ns 2 = 455ns 3 = 909ns 4 = 1.818µs 5 = 3.636µs 6 = 7.273µs 7 = 14.454µs 8 = 29.091µs 9 = 58.182µs 10 = 116.364µs 11 = 232.7µs 12 = 465.5µs 13 = 930.9µs 14 = 1.8629ms 15 = 3.724ms 16 = 7.45ms 17 = 14.89ms 18 = 29.79ms 19 = 59.58ms 20 = 119.2ms 21 = 238.3ms 22 = 476.6ms

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7.25 WAKE_PIN_CTRL - 0x40

Name	Bit	Type	Default	Description
WAKE2_IN_LATCHED	7	R	0x0	WAKE2 input transparent latch value Held WAKE2 input value when WAKE2_MODE = 1
WAKE2_MODE	6:5	RW	0x0	WAKE2 input control 0 = transparent (voltage seen at pin) 1 = Hold 2 = Input set to low 3 = Input set to high
WAKE2_IN	4	R	0x0	WAKE2 pin input value
WAKE1_IN_LATCHED	3	R	0x0	WAKE1 input transparent latch value Held WAKE1 input value when WAKE2_MODE = 1
WAKE1_MODE	2:1	RW	0x0	WAKE1 input control 0 = Transparent (voltage seen at pin) 1 = Hold 2 = Input set to low 3 = Input set to high
WAKE1_IN	0	R	0x0	WAKE1 pin input value

7.26 PWR_PIN_CTRL - 0x41

Name	Bit	Type	Default	Description
PSTBYB_IN_LATCHED	7	R	0x0	PSTBYB input transparent latch value Held PSTBYB input value when PSTBYB_MODE = 1
PSTBYB_MODE	6:5	RW	0x0	PSTBYB input control 0 = transparent (voltage seen at pin) 1 = Hold 2 = Input set to low 3 = Input set to high
PSTBYB_IN	4	R	0x0	PSTBYB pin input value
PWRCTRLB_IN_LATCHED	3	R	0x0	PWRCTRLB input transparent latch value Held PWRCTRLB input value when PWRCTRLB_MODE = 1
PWRCTRLB_MODE	2:1	RW	0x0	PWRCTRLB input control 0 = transparent (voltage seen at pin) 1 = Hold 2 = Input set to low 3 = Input set to high
PWRCTRLB_IN	0	R	0x0	PWRCTRLB pin input value

7.27 INTB_PIN_CTRL - 0x42

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
INTB_TEST_DATA	3	RW	0x0	INTB pin test data Used when INTB_TEST_EN is 1
INTB_TEST_EN	2	RW	0x0	INTB pin test control select 0 = Mission mode 1 = Drive using INTB_TEST_DATA value
Reserved	1	R	0x0	-
INTB_SENSED	0	R	0x0	INTB pin sensed value

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7.28 VMONB_PIN_CTRL - 0x43

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
VMONB_IN_LATCHED	3	R	0x0	VMONB input transparent latch value Held VMONB input value when VMONB_MODE = 1
VMONB_MODE	2:1	RW	0x0	VMONB input control 0 = transparent (voltage seen at pin) 1 = Hold 2 = Input set to low 3 = Input set to high
VMONB_IN	0	R	0x0	VMONB pin input value

7.29 ERRB_PIN_CTRL - 0x44

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
ERRB_IN_LATCHED	3	R	0x0	ERRB input transparent latch value Held ERRB input value when ERRB_MODE = 1

Name	Bit	Type	Default	Description
ERRB_MODE	2:1	RW	0x0	ERRB input control 0 = transparent (voltage seen at pin) 1 = Hold 2 = Input set to low 3 = Input set to high
ERRB_IN	0	R	0x0	ERRB pin input value

7.30 RSTB_PIN_CTRL - 0x45

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
RSTB_TEST_DATA	3	RW	0x0	RSTB pin test data Used when RSTB_TEST_EN = 1
RSTB_TEST_EN	2	RW	0x0	RSTB pin test control select 0 = Mission mode 1 = Drive using RSTB_TEST_DATA value
Reserved	1	R	0x0	-
RSTB_SENSED	0	R	0x0	RSTB pin sensed value

7.31 SSPB_PIN_CTRL - 0x46

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
SSPB_TEST_DATA	3	RW	0x0	SSPB pin test data Used when SSPB_TEST_EN = 1
SSPB_TEST_EN	2	RW	0x0	SSPB pin test control select 0 = Mission mode 1 = Drive using SSPB_TEST_DATA value
Reserved	1	R	0x0	-
SSPB_SENSED	0	R	0x0	SSPB pin sensed value

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7.32 WDENB_PIN_CTRL - 0x47

Name	Bit	Type	Default	Description
WDENB_DATA	7	RW	0x0	WDENB output data Used when WDENB_SEL = 1
Reserved	6	R	0x0	-
WDENB_SEL	5	RW	0x0	WDENB pin output data selection control Selects output data for WDENB pin when OPT_WDENB_OE is set to 1. Otherwise ignored. 0 = Monitor power-goods of regulators as selected by the OPT_PG_CTRL bits 1 = Use WDENB_DATA value for WDENB output
WDENB_OD	4	RW	0x0	WDENB pin drive type selection 0 = Push/pull 1 = Open drain
WDENB_IN_LATCHED	3	R	0x0	WDENB input transparent latch value Held WDENB input value when WDENB_MODE = 1

Name	Bit	Type	Default	Description
WDENB_MODE	2:1	RW	0x0	WDENB input control 0 = transparent (voltage seen at pin) 1 = Hold 2 = Input set to low 3 = Input set to high
WDENB_IN	0	R	0x0	WDENB pin input value

7.33 PWR_MODE_CTRL - 0x48

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x0	-
PMIC_OFF	0	RW	0x0	Allows complete shutdown of PMIC, including LDO0 disabled 0 = Both WAKE pins low powers down DCDC1, DCDC2, LDO1-4 and transitions into EOT_ONLY state. LDO0 remains on. EOT timer is available. 1 = Both WAKE pins low powers down all regulators, including LDO0. EOT timer is also disabled.

7.34 EOT_CTRL1 - 0x60

Name	Bit	Type	Default	Description
CD_SPEEDUP	7	RW	0x0	Count down timer rate 0 = Count down timer decrements at 1Hz rate 1 = Count down timer decrements at 32768Hz rate
CD_STOP	6	RW	0x0	Count down timer stop control Used to pause the count down timer. Note: If CD_ENABLE is 0, the count down timer is held in set (0x3F). 0 = Run count down timer if CD_ENABLE is 1 1 = Pause count down timer if CD_ENABLE is 1
CD_SET	5	W1S	0x0	Count down timer set Not latched. Used to set a decrementing count down timer to 0x3f if enabled. Counting continues after set. 0 = No action 1 = Set count down timer
CD_ENABLE	4	RW	0x0	Count down timer enable When disabled, the 6-bit count down timer is automatically set to 0x3f When enabled and CD_STOP is low, the timer decrements at the rate defined by CD_SPEEDUP. Decrementing halts if the timer reaches a minimum value of 0x00 and triggers an CD_ZERO fault. 0 = Disabled. 1 = Enabled
EOT_SPEEDUP	3	RW	0x0	Engine off timer rate 0 = EOT increments at 1Hz rate 1 = EOT increments at 32768Hz rate
EOT_STOP	2	RW	0x0	Engine off timer stop control Used to pause the EOT. Note if EOT_ENABLE is 0, then engine off timer is held in reset. 0 = Run engine off timer if EOT_ENABLE is 1 1 = Pause engine off timer if EOT_ENABLE is 1

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Name	Bit	Type	Default	Description
EOT_RST	1	W1C	0x0	Engine off timer reset Not latched. Used to reset an incrementing EOT to 0x000000 if enabled. Counting continues after reset. 0 = No action 1 = Reset engine off timer
EOT_ENABLE	0	RW	0x0	Engine off timer enable When disabled, the 24-bit engine off timer is automatically reset to 0x000000 When enabled and EOT_STOP is low, the engine off timer increments at the rate defined by EOT_SPEEDUP. Incrementing halts if the timer reaches a maximum value of 0xFFFFFF and triggers an EOT_OVF fault. 0 = Disabled 1 = Enabled

7.35 EOT_CTRL2 - 0x61

Name	Bit	Type	Default	Description
CD_RUNNING	7	R	0x0	Count down timer status 0 = Not running 1 = Running
Reserved	6:5	R	0x0	-
CD_ALARM_EN	4	RW	0x0	Count down timer alarm enable If enabled and the alarm condition persists, this bit must be cleared to allow clearing of the EOT_CD_ALRM_RECORD bit. 0 = Ignore count down alarm assertion on zero 1 = Allow count down alarm assertion on zero
EOT_RUNNING	3	R	0x0	Engine off timer status 0 = Not running 1 = Running
OVF_ALARM_EN	2	RW	0x0	Engine off timer overflow alarm enable If enabled and the alarm condition persists, this bit must be cleared to allow clearing of the EOT_OVF_ALRM_RECORD bit. 0 = Ignore overflow alarm assertion on match 1 = Allow overflow alarm assertion on match
PD_ALARM_EN	1	RW	0x0	Engine off timer power-down alarm enable If enabled and the alarm condition persists, this bit must be cleared to allow clearing of the EOT_PD_ALRM_RECORD bit. 0 = Ignore power-down alarm assertion on match 1 = Allow power-down alarm assertion on match
WU_ALARM_EN	0	RW	0x0	Engine off timer wakeup alarm enable If enabled and the alarm condition persists, this bit must be cleared to allow clearing of the EOT_WU_ALRM_RECORD bit. 0 = Ignore wakeup alarm assertion on match 1 = Allow wake alarm assertion on match

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7.36 EOT_CTRL3 - 0x62

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
EOT_CD_CTRL	5:4	RW	0x0	Sets EOT 63 second count down alarm action When set to other than 0 and the count down timer triggers, the indicated action is automatically triggered. After the trigger, this register must be set to 0 using SPI to restore pin-based control of the PMIC. The action is taken only if the PMIC is currently in the indicated state. Otherwise ignored. 0 = Do nothing 1 = Exit DeepSTOP and return to ACTIVE 2 = Exit PSTBY state and return to ACTIVE 3 = Exit EOT_ONLY state and restart DCDC1, LDO1-LDO4 as programmed by OTP. LDO0 remains active.
EOT_PD_CTRL	3:2	RW	0x0	Sets EOT PD alarm action When set to other than 0 and the EOT PD triggers, the indicated action is automatically triggered. After the trigger, this register must be set to 0 using SPI to restore pin-based control of the PMIC. The action is taken only if the PMIC is in the active state, otherwise ignored. 0 = Do nothing 1 = Enter DeepSTOP from ACTIVE 2 = Enter PSTBY state from ACTIVE 3 = Enter EOT_ONLY state from ACTIVE
EOT_WU_CTRL	1:0	RW	0x0	Sets EOT WU alarm action When set to other than 0 and the EOT WU triggers, the indicated action is automatically triggered. After the trigger, this register must be set to 0 using SPI to restore pin-based control of the PMIC. The action is taken only if the PMIC is currently in the indicated state. Otherwise ignored. 0 = Do nothing 1 = Exit DeepSTOP and return to ACTIVE 2 = Exit PSTBY state and return to ACTIVE 3 = Exit EOT_ONLY state and restart DCDC1, LDO1-LDO4 as programmed by OTP. LDO0 remains active.

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7.37 EOT_PD0 - 0x63

Name	Bit	Type	Default	Description
EOT_PD0	7:0	RW	0x0	Engine off timer power-down alarm LSByte [7:0]

7.38 EOT_PD1 - 0x64

Name	Bit	Type	Default	Description
EOT_PD1	7:0	RW	0x0	Engine off timer power-down alarm MSByte [15:0] 16-bit power-down alarm [15:0] updated when this byte is written. Sequence of SPI writes to update the EOT power-down alarm must be register 0x63 followed by 0x64.

7.39 EOT_WU0 - 0x65

Name	Bit	Type	Default	Description
EOT_WU0	7:0	RW	0x0	Engine off timer Wake-up alarm LSByte [7:0] This LSByte register does not update after written until the MSByte register is written.

7.40 EOT_WU1 - 0x66

Name	Bit	Type	Default	Description
EOT_WU1	7:0	RW	0x0	Engine off timer Wake-up alarm middle byte [15:8] This middle byte register does not update after written until the MSByte register is written.

7.41 EOT_WU2 - 0x67

Name	Bit	Type	Default	Description
EOT_WU2	7:0	RW	0x0	Engine off timer Wake-up alarm MSByte [23:16] 24-bit Wake-up alarm [23:0] updated when this byte is written. The recommended sequence of SPI writes to update the EOT wakeup alarm is register 0x65 followed by 0x66 then 0x67.

7.42 EOT_TMR0 - 0x68

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Name	Bit	Type	Default	Description
EOT_TMR0	7:0	R	0x0	Engine off timer readback LSByte [7:0] 24-bit engine off timer [23:0] captured when this byte is read

7.43 EOT_TMR1 - 0x69

Name	Bit	Type	Default	Description
EOT_TMR1	7:0	R	0x0	Engine off timer readback middle byte [15:8]

7.44 EOT_TMR2 - 0x6A

Name	Bit	Type	Default	Description
EOT_TMR2	7:0	R	0x0	Engine off timer readback MSbyte [23:16]

7.45 EOT_CD - 0x6B

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
EOT_CD	5:0	R	0x3f	Count down timer readback value

7.46 EOT_PDDB0 - 0x6C

Name	Bit	Type	Default	Description
EOT_PDDB0	7:0	R	0x0	EOT power-down alarm double buffer for EOT_PD0 Returns value of double buffer register

7.47 EOT_WUDB0 - 0x6D

Name	Bit	Type	Default	Description
EOT_WUDB0	7:0	R	0x0	EOT Wake-up alarm double buffer for EOT_WU0 Returns value of double buffer register

7.48 EOT_WUDB1 - 0x6E

Name	Bit	Type	Default	Description
EOT_WUDB1	7:0	R	0x0	EOT Wake-up alarm double buffer for EOT_WU1 Returns value of double buffer register

7.49 WDT_CTRL1 - 0x80

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	-
WDT_RUNNING	4	R	0x0	Watchdog timer running state 0 = WDT stopped 1 = WDT running
Reserved	3:1	R	0x0	-
WDT_START	0	W1S	0x0	Watchdog timer start control Writing a 1 to this bit starts the WDT

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7.50 WDT_CTRL2 - 0x81

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x0	-
WDT_STOP	0	W1S	0x0	Watchdog timer stop control Writing a 1 to this bit stops the WDT

7.51 OPT_WDT_CONFIG1 - 0x82

Name	Bit	Type	Default	Description
OPT_USE_SST_KICK	7	FRW	0x0	Selects if PMIC uses Watchdog SST timer kick to transition into ACTIVE state 0 = WDT SST kick not required to enter ACTIVE STATE 1 = WDT SST kick required to enter ACTIVE state. Otherwise, remain in INIT.
OPT_SST_TIMEOUT	6:4	FRW	0x0	Sets the system self-test timeout. During the INIT state, the PMIC waits this period for ERROUT_M, pin checking and WDT checking and programming to complete. If the EXIT_SST is written before this period, PMIC enters the ACTIVE (safe state). If EXIT_SST is not written, the PMIC responds according to the OPT_SST_RESP[1:0] settings to the SST fault. 0 = 64ms 1 = 128ms 2 = 256ms 3 = 512ms 4 = 1024ms 5 = 4096ms 6 = 32.768s 7= 65.535s
OPT_SST_RESP	3:2	FRW	0x0	Response control when SST kick to ACTIVE is enabled but EXIT_SST is not kicked before OPT_SST_TIMEOUT period expires. 0 = Ignore 1 = Follow Case 1 response 2 = Follow Case 2 response 3 = Follow Case 3 response
OPT_SST_WDENB_CTRL	1	FRW	0x0	Selects if the WDENB pin can disable the SST timer operation at SYSTEM_SELF_TEST entry. This pin-controlled SST feature is only available if OPT_WDENB_OE is 0 (WDENB pin set to input). 0 = WDENB pin high at SYSTEM_SELF_TEST state entry disables SST timer. Otherwise, SST timer can run. 1 = WDENB pin cannot disable the SST timer.
OPT_WDT_WDENB_CTRL	0	FRW	0x0	Selects if the WDENB pin can disable the WDT operation at ACTIVE_STATE entry. This pin-controlled WDT feature is only available if OPT_WDENB_OE is 0 (WDENB pin set to input). 0 = WDENB pin high at ACTIVE state entry disables WDT. Otherwise WDT can run. 1 = WDENB pin cannot disable the WDT.

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7.52 WDT_CONFIG2 - 0x83

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
WDT_PIN_KICK_EDGE	6:5	RW	0x0	WDT edge control for pin-based kicks. Used when WDT_PIN_KICK_CTRL = 1 0 = Either edge 1 = Rising edge 2 = Falling edge 3 = Reserved

Name	Bit	Type	Default	Description
WDT_PIN_KICK_CTRL	4	RW	0x0	Selects if WDENB is used for enabling the WDT or WDT pin kicking. 0 = WDENB is not used for pin kicking. WDENB may be used for WDT enabling as programmed by OPT_SST_WDENB_CTRL and OPT_WDT_WDENB_CTRL bits 1 = WDENB used for pin kicking.
WDT_TOACC_FAULT_RESP	3:2	RW	0x0	Response control when the WDT_TOACC value reaches the WDT_TOACC_THRESH level 0 = Ignore 1 = Follow Case 1 response 2 = Follow Case 2 response 3 = Follow Case 3 response
WDT_ACC_FAULT_RESP	1:0	RW	0x0	Response control when the WDT_ACC value meets or exceeds the WDT_ACC_THRESH level 0 = Ignore 1 = Follow Case 1 response 2 = Follow Case 2 response 3 = Follow Case 3 response

7.53 WDT_CONFIG3 - 0x84 (ASIL-D only)

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	-
WDT_DIS_LFSR	4	RW	0x0	Sets WDT_LFSR question update mode 0 = Random question 1 = Incrementing question
WDT_ANS_IDX	3:2	R	0x0	WDT 16QA answer index. Used in 16QA mode to determine the current answer index in the 4 answer response sequence. 0 = Answer 0 1 = Answer 1 2 = Answer 2 3 = Answer 3
WDT_MODE	1:0	RW	0x0	Sets the expected WDT_KICK_REG SPI data value for WDT kicks. 0 = Basic mode. Kick data is 0x2A. All other values are ignored and handled as a non-kick. 1 = Reserved 2 = 4QA mode. Valid kick data depends on WDT_LFSR value. 3 = 16QA mode. Valid kick data depends on WDT_LFSR value and WDT_ANS_IDX value.

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7.54 WDT_SST - 0x85

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	-
SST_RUNNING	4	R	0x0	System-self-test timer running state If OPT_USE_SST_KICK is programmed to 1 (require kick), the PMIC remains in the system-self-test state and the SST timer runs until a EXIT_SST is issued. If the programmed OPT_SST_TIMEOUT is reached before an EXIT_SST command is written, a SST_FAULT_RECORD fault is triggered. Remaining in the system self-test state periodically issues SST_FAULT_RECORDs at the OPT_SST_TIMEOUT rate. 0 = SST stopped 1 = SST running
Reserved	3:1	R	0x0	-
EXIT_SST	0	W1S	0x0	System Self-Test exit When written as a 1 during SYSTEM_SELF_TEST state and before the SST timer expires, the PMIC enters ACTIVE state and asserts the SSPB safety defined output pin.

7.55 WDT_KICK_REG - 0x86

Name	Bit	Type	Default	Description
WDT_KICK_REG	7:0	RW	0x0	WDT kick register. To kick WDT, write the correct answer in QA mode (ASIL-D only), or write 0x2A in basic mode.

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7.56 WDT_LFSR - 0x87 (ASIL-D only)

Name	Bit	Type	Default	Description
WDT_LFSR	7:0	R	0x0	WDT question register Provides question in QA mode

7.57 WDT_ACC_THRESH - 0x88

Name	Bit	Type	Default	Description
WDT_ACC_THRESH	7:0	RW	0x0	WDT accumulator threshold Sets error threshold. When the error accumulator meets or exceeds this value, a WDT_ACC_FAULT_RECORD is asserted

7.58 WDT_ACC - 0x89

Name	Bit	Type	Default	Description
WDT_ACC	7:0	R	0x0	WDT accumulator value Provides accumulator readback value. Maximum value is 255. Value does not roll over for additional increments.

7.59 WDT_ACC_CLEAR - 0x8A

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x0	-
WDT_ACC_CLEAR	0	W1C	0x0	WDT accumulator clear Writing a 1 to this bit resets the WDT_ACC[7:0] to 0x00

7.60 WDT_TOACC_THRESH - 0x8B

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x0	-
WDT_TOACC_THRESH	2:0	RW	0x0	WDT timeout accumulator threshold Sets error threshold.

7.61 WDT_TOACC - 0x8C

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x0	-
WDT_TOACC	2:0	R	0x0	WDT timeout accumulator value Provides timeout accumulator readback value. Maximum value is 7. Value does not roll over for additional increments.

7.62 WDT_TOACC_CLEAR - 0x8D

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Name	Bit	Type	Default	Description
Reserved	7:1	R	0x0	-
WDT_TOACC_CLEAR	0	W1C	0x0	WDT timeout accumulator clear Writing a 1 to this bit resets the WDT_TOACC[3:0] to 0x00

7.63 WDT_TICK - 0x8E

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
WDT_ULTICK	6:4	RW	0x0	WDT upper period limit tick selection (kick frequency too slow) 0 = 10µs pulse 1 = 100µs pulse 2 = 1ms pulse 3 = 10ms pulse 4 = 100ms pulse 5 = 1s pulse
Reserved	3	R	0x0	-
WDT_LLTICK	2:0	RW	0x0	WDT lower period limit tick selection (kick frequency too fast) 0 = 10µs pulse 1 = 100µs pulse 2 = 1ms pulse 3 = 10ms pulse 4 = 100ms pulse

7.64 WDT_LLCNT - 0x8F

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
WDT_LLCNT	6:0	RW	0x0	WDT lower period limit counter selection (kick frequency too fast) 0-127 decimal

7.65 WDT_ULCNT - 0x90

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
WDT_ULCNT	6:0	RW	0x0	WDT upper period limit counter selection (kick frequency too slow) 0-127 decimal

7.66 WDT_TOTICK - 0x91

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x0	-
WDT_TOTICK	2:0	RW	0x0	WDT error period limit tick selection 0 = 10µs pulse 1 = 100µs pulse 2 = 1ms pulse 3 = 10ms pulse 4 = 100ms pulse 5 = 1s pulse

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7.67 WDT_TOCNT - 0x92

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
WDT_TOCNT	6:0	RW	0x0	WDT error period limit counter selection 0-127 decimal

7.68 FAULT_STATUS_1 - 0x100

Name	Bit	Type	Default	Description
FB2_SEVERE_OV_FAULT_RECORD	7	RW0C	0x0	DCDC2 FB2 severe overvoltage detect 0 = No fault detected 1 = Fault detected
FB2_SEVERE_UV_FAULT_RECORD	6	RW0C	0x0	DCDC2 FB2 severe undervoltage detect 0 = No fault detected 1 = Fault detected
FB2_WARN_OV_FAULT_RECORD	5	RW0C	0x0	DCDC2 FB2 warning overvoltage detect 0 = No fault detected 1 = Fault detected
FB2_WARN_UV_FAULT_RECORD	4	RW0C	0x0	DCDC2 FB2 warning undervoltage detect 0 = No fault detected 1 = Fault detected

Name	Bit	Type	Default	Description
FB1_SEVERE_OV_FAULT_RECORD	3	RW0C	0x0	DCDC1 FB1 severe overvoltage detect 0 = No fault detected 1 = Fault detected
FB1_SEVERE_UV_FAULT_RECORD	2	RW0C	0x0	DCDC1 FB1 severe undervoltage detect 0 = No fault detected 1 = Fault detected
FB1_WARN_OV_FAULT_RECORD	1	RW0C	0x0	DCDC1 FB1 warning overvoltage detect 0 = No fault detected 1 = Fault detected
FB1_WARN_UV_FAULT_RECORD	0	RW0C	0x0	DCDC1 FB1 warning undervoltage detect 0 = No fault detected 1 = Fault detected

7.69 FAULT_STATUS_2 - 0x101

Name	Bit	Type	Default	Description
LDO2_SEVERE_OV_FAULT_RECORD	7	RW0C	0x0	LDO2 severe overvoltage detect 0 = No fault detected 1 = Fault detected
LDO2_SEVERE_UV_FAULT_RECORD	6	RW0C	0x0	LDO2 severe undervoltage detect 0 = No fault detected 1 = Fault detected
LDO2_WARN_OV_FAULT_RECORD	5	RW0C	0x0	LDO2 warning overvoltage detect 0 = No fault detected 1 = Fault detected
LDO2_WARN_UV_FAULT_RECORD	4	RW0C	0x0	LDO2 warning undervoltage detect 0 = No fault detected 1 = Fault detected
LDO1_SEVERE_OV_FAULT_RECORD	3	RW0C	0x0	LDO1 severe overvoltage detect 0 = No fault detected 1 = Fault detected
LDO1_SEVERE_UV_FAULT_RECORD	2	RW0C	0x0	LDO1 severe undervoltage detect 0 = No fault detected 1 = Fault detected
LDO1_WARN_OV_FAULT_RECORD	1	RW0C	0x0	LDO1 warning overvoltage detect 0 = No fault detected 1 = Fault detected
LDO1_WARN_UV_FAULT_RECORD	0	RW0C	0x0	LDO1 warning undervoltage detect 0 = No fault detected 1 = Fault detected

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7.70 FAULT_STATUS_3 - 0x102

Name	Bit	Type	Default	Description
LDO4_SEVERE_OV_FAULT_RECORD	7	RW0C	0x0	LDO4 severe overvoltage detect 0 = No fault detected 1 = Fault detected
LDO4_SEVERE_UV_FAULT_RECORD	6	RW0C	0x0	LDO4 severe undervoltage detect 0 = No fault detected 1 = Fault detected
LDO4_WARN_OV_FAULT_RECORD	5	RW0C	0x0	LDO4 warning overvoltage detect 0 = No fault detected 1 = Fault detected

Name	Bit	Type	Default	Description
LDO4_WARN_UV_FAULT_RECORD	4	RW0C	0x0	LDO4 warning undervoltage detect 0 = No fault detected 1 = Fault detected
LDO3_SEVERE_OV_FAULT_RECORD	3	RW0C	0x0	LDO3 severe overvoltage detect 0 = No fault detected 1 = Fault detected
LDO3_SEVERE_UV_FAULT_RECORD	2	RW0C	0x0	LDO3 severe undervoltage detect 0 = No fault detected 1 = Fault detected
LDO3_WARN_OV_FAULT_RECORD	1	RW0C	0x0	LDO3 warning overvoltage detect 0 = No fault detected 1 = Fault detected
LDO3_WARN_UV_FAULT_RECORD	0	RW0C	0x0	LDO3 warning undervoltage detect 0 = No fault detected 1 = Fault detected

7.71 FAULT_STATUS_4 - 0x103

Name	Bit	Type	Default	Description
CLK_OVER_FREQ_FAULT_RECORD	7	RW0C	0x0	PMIC internal oscillator over frequency detect 0 = No fault detected 1 = Fault detected
CLK_UNDER_FREQ_FAULT_RECORD	6	RW0C	0x0	PMIC internal oscillator under frequency or stopped detect The two methods of recovering from this fault and restarting the PMIC are: ▪ Set both WAKE pins low greater than the maximum programmed discharge times for all regulators. ▪ Issue a PMIC_RESET command using SPI. The PMIC restarts after the maximum programmed discharge times for all regulators. If the under frequency or stopped oscillator fault condition is still present, the PMIC remains disabled. 0 = No fault detected 1 = Fault detected
VMONB_FAULT_RECORD	5	RW0C	0x0	VMONB fault detect. Asserts when VMONB input is low exceeding the programmed period 0 = No fault detected 1 = Fault detected
ERRB_FAULT_RECORD	4	RW0C	0x0	ERRB fault detect. Asserts when the programmed ERRB period is exceeded 0 = No fault detected 1 = Fault detected
COREMON_SEVERE_OV_FAULT_RECORD	3	RW0C	0x0	COREMON severe overvoltage detect (ASIL-D only) 0 = No fault detected 1 = Fault detected
COREMON_SEVERE_UV_FAULT_RECORD	2	RW0C	0x0	COREMON severe undervoltage detect (ASIL-D only) 0 = No fault detected 1 = Fault detected
COREMON_WARN_OV_FAULT_RECORD	1	RW0C	0x0	COREMON warning overvoltage detect (ASIL-D only) 0 = No fault detected 1 = Fault detected
COREMON_WARN_UV_FAULT_RECORD	0	RW0C	0x0	COREMON warning undervoltage detect (ASIL-D only) 0 = No fault detected 1 = Fault detected

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7.72 FAULT_STATUS_5 - 0x104

Name	Bit	Type	Default	Description
LDO0_SEVERE_OV_FAULT_RECORD	7	RW0C	0x0	LDO0 severe overvoltage detect 0 = No fault detected 1 = Fault detected
LDO0_SEVERE_UV_FAULT_RECORD	6	RW0C	0x0	LDO0 severe undervoltage detect 0 = No fault detected 1 = Fault detected
LDO0_WARN_OV_FAULT_RECORD	5	RW0C	0x0	LDO0 warning overvoltage detect 0 = No fault detected 1 = Fault detected
LDO0_WARN_UV_FAULT_RECORD	4	RW0C	0x0	LDO0 warning undervoltage detect 0 = No fault detected 1 = Fault detected
DGND_FAULT_RECORD	3	RW0C	0x0	Safety D-GND monitor bond wire break detect 0 = No fault detected 1 = Fault detected
AGND_FAULT_RECORD	2	RW0C	0x0	Safety A-GND monitor bond wire break detect 0 = No fault detected 1 = Fault detected
VBG_OV_FAULT_RECORD	1	RW0C	0x0	Safety bandgap monitor overvoltage detect 0 = No fault detected 1 = Fault detected
VBG_UV_FAULT_RECORD	0	RW0C	0x0	Safety bandgap monitor undervoltage detect 0 = No fault detected 1 = Fault detected

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7.73 FAULT_STATUS_6 - 0x105

Name	Bit	Type	Default	Description
EOT_CD_ALRM_RECORD	7	RW0C	0x0	Count down zero alarm record Sets when the EOT count down timer reaches zero. The set remains active if the zero persists and the CD_ENABLE bit = 1 0 = No fault detected 1 = Fault detected
EOT_OVF_ALRM_RECORD	6	RW0C	0x0	EOT Overflow alarm detect Sets when the EOT counter reaches the maximum 24-bit value of 0xFFFFFF. The set remains active if the max value persists and the EOT_ENABLE bit = 1 0 = No fault detected 1 = Fault detected
EOT_PD_ALRM_RECORD	5	RW0C	0x0	EOT power-down alarm detect Sets when the EOT counter is equal to the 16-bit EOT power-down alarm value. The set remains active if the = condition persists and the EOT_ENABLE bit = 1 0 = No fault detected 1 = Fault detected

Name	Bit	Type	Default	Description
EOT_WU_ALRM_RECORD	4	RW0C	0x0	EOT Wakeup alarm detect Sets when the EOT counter is greater than or equal to the 24-bit EOT Wakeup alarm value. The set remains active if the ≥ condition persists and the EOT_ENABLE bit = 1 0 = No fault detected 1 = Fault detected
DCDC2_OC2_FAULT_RECORD	3	RW0C	0x0	DCDC2 overcurrent fault (OC2) detect 0 = No fault detected 1 = Fault detected
CRC_RECHECK_FAULT_RECORD	2	RW0C	0x0	Periodic CRC re-checker failed 0 = No fault detected 1 = Fault detected
SPI_CRC_FAULT_RECORD	1	RW0C	0x0	SPI CRC write transaction error detect If OPT_SPI_CRC is 1, this fault record sets if a CRC error is detected on SPI write transactions. If a fault is found, the addressed register is not updated. 0 = No fault detected 1 = Fault detected
SPI_WRITE_FAULT_RECORD	0	RW0C	0x0	SPI Write check error detect SPI register write updates are self-verified using an internal write through mechanism. This is equivalent to a write and read-back check for correctness. If the correctness check fails, this fault record bit is set. 0 = No fault detected 1 = Fault detected

7.74 FAULT_STATUS_7 - 0x106

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Name	Bit	Type	Default	Description
RW_REG_FAULT_RECORD	7	RW0C	0x0	Read/Write register fault detect 0 = No fault detected 1 = Fault detected
REG1_BUCKBOOST_MODE_RECORD	6	RW0C	0x0	REG1 in buck-boost mode detect Reports when DCDC1 enters buck-boost mode 0 = No buck-boost mode detected 1 = Buck-boost mode detected
VBAT_UVLO_FAULT_RECORD	5	RW0C	0x0	VBAT below V_{BAT_SDN} fault detect 0 = No fault detected 1 = Fault detected
DCDC1_OC1_FAULT_RECORD	4	RW0C	0x0	DCDC1 OC fault detect 0 = No fault detected 1 = Fault detected
SSPB_PIN_FAULT_RECORD	3	RW0C	0x0	SSPB drive mismatches sensed 0 = No fault detected 1 = Fault detected
RSTB_PIN_FAULT_RECORD	2	RW0C	0x0	RSTB pin drive mismatches sensed 0 = No fault detected 1 = Fault detected
TSD_FUSA_FAULT_RECORD	1	RW0C	0x0	Safety > 160C over-temperature fault detect 0 = No fault detected 1 = Fault detected
TSD_LDO34_FAULT_RECORD	0	RW0C	0x0	LDO3/4 Tracker > 145C over-temperature fault detect 0 = No fault detected 1 = Fault detected

7.75 FAULT_STATUS_8 - 0x107

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
SST_FAULT_RECORD	6	RW0C	0x0	Sets when the system self-test timer is not kicked before the OPT_SST_TIMEOUT period expires. 0 = No fault detected 1 = Fault detected
WDT_TOACC_FAULT_RECORD	5	RW0C	0x0	Watchdog timer timeout accumulator threshold fault detect Sets when the WDT reaches the timeout accumulator reaches or exceeds the timeout threshold limit 0 = No fault detected 1 = Fault detected
WDT_TO_FAULT_RECORD	4	RW0C	0x0	Watchdog timer timeout fault detect Sets when the WDT reaches the timeout fault detect period as well as multiple of the period 0 = No fault detected 1 = Fault detected
WDT_ACC_FAULT_RECORD	3	RW0C	0x0	Watchdog timer error accumulator threshold fault detect Sets when the WDT error accumulator reaches or exceeds the error threshold limit 0 = No fault detected 1 = Fault detected
WDT_ANS_FAULT_RECORD	2	RW0C	0x0	Watchdog timer answer fault detect Sets when the WDT is kicked with an incorrect answer 0 = No fault detected 1 = Fault detected
WDT_LATE_FAULT_RECORD	1	RW0C	0x0	Watchdog timer late kick fault detect Sets when the WDT is kicked after the upper level set time 0 = No fault detected 1 = Fault detected
WDT_EARLY_FAULT_RECORD	0	RW0C	0x0	Watchdog timer early kick fault detect Sets when the WDT is kicked before the lower level set time 0 = No fault detected 1 = Fault detected

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7.76 FAULT_STATUS_9 - 0x108

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
VDDIO_OK_FAULT_RECORD	3	RW0C	0x0	Sets when VDDIO is not present when the output rail associated with VDDIO as selected by the OPT_VDDIO_SEL value available. 0 = No fault detected 1 = Fault detected
DCDC1_OC2_FAULT_RECORD	2	RW0C	0x0	DCDC1 OC2 fault detect (ASIL-D only) 0 = No fault detected 1 = Fault detected

Name	Bit	Type	Default	Description
MANUAL_FAULT_RECORD	1	RW0C	0x0	Sets when the software-initiated fault response is executed using the MANUAL_FAULT bit. Initiates the fault response as programmed in the MANUAL_FAULT_RESP field. 0 = No fault detected 1 = Fault detected
FUSA_HKOK_FAULT_RECORD	0	RW0C	0x0	Sets when the FuSa Housekeeping OK architecture fault asserts. Indicates if reference sources for safety monitoring are not functioning. 0 = No fault detected 1 = Fault detected

7.77 OPT_FLT_RESP1 - 0x120

Name	Bit	Type	Default	Description
OPT_VBAT_UVLO_FLT_RESP	7	FRW	0x0	VBAT below V_{BAT_SDN} fault response 0 = Follow Case 2 response 1 = Follow Case 3 response
OPT_REG_CHK_FLT_RESP	6:5	FRW	0x0	Register checker fault response 0 = Follow Case 0 response 1 = Follow Case 1 response 2 = Follow Case 2 response 3 = Follow Case 3 response
OPT_SYSCLK_RESP	4	FRW	0x0	System clock fault response control 0 = Follow Case 2 response 1 = Follow Case 3 response
OPT_ERRB_RESP	3:2	FRW	0x0	ERRB fault response control 0 = Case 0. Ignore ERRB. 1 = Follow Case 1 response 2 = Follow Case 2 response 3 = Follow Case 3 response
OPT_VMONB_RESP	1:0	FRW	0x0	VMONB fault response control 0 = Case 0. Ignore VMONB 1 = Follow Case 1 response 2 = Follow Case 2 response 3 = Follow Case 3 response

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7.78 OPT_FLT_RESP2 - 0x121

Name	Bit	Type	Default	Description
OPT_VDDIO_FLT_RESP	7:6	FRW	0x0	VDDIO_OK fault response control 0 = Case 0. No response to VDDIO_OK fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
OPT_DCDC1_OC2_RESP	5:4	FRW	0x0	DCDC1 OC2 overcurrent fault response control (ASIL-D only) 0 = Case 0. No response to DCDC1 OC2 fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
OPT_DCDC1_SEV_UVOV_RESP	3:2	FRW	0x0	DCDC1 Severe under and overvoltage response control 0 = Case 0. No response to DCDC1 severe UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.

Name	Bit	Type	Default	Description
Reserved	1	R	0x0	-
OPT_DCDC1_WARN_UVOV_RESP	0	FRW	0x0	DCDC1 Warning under and overvoltage response control 0 = Case 0. No response to DCDC1 warning UV or OV fault. 1 = Follow Case 1 response.

7.79 OPT_FLT_RESP3 - 0x122

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
OPT_DCDC2_SEV_UVOV_RESP	3:2	FRW	0x0	DCDC2 Severe under and overvoltage response control 0 = Case 0. No response to DCDC2 severe UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
OPT_DCDC2_WARN_UVOV_RESP	1:0	FRW	0x0	DCDC2 Warning under and overvoltage response control 0 = Case 0. No response to DCDC2 warning UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.

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7.80 OPT_FLT_RESP4 - 0x123

Name	Bit	Type	Default	Description
OPT_LDO2_SEV_UVOV_RESP	7:6	FRW	0x0	LDO2 Severe under and overvoltage response control 0 = Case 0. No response to LDO2 severe UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
Reserved	5	R	0x0	-
OPT_LDO2_WARN_UVOV_RESP	4	FRW	0x0	LDO2 Warning under and overvoltage response control 0 = Case 0. No response to LDO2 warning UV or OV fault. 1 = Follow Case 1 response.
OPT_LDO1_SEV_UVOV_RESP	3:2	FRW	0x0	LDO1 Severe under and overvoltage response control 0 = Case 0. No response to LDO1 severe UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
Reserved	1	R	0x0	-
OPT_LDO1_WARN_UVOV_RESP	0	FRW	0x0	LDO1 Warning under and overvoltage response control 0 = Case 0. No response to LDO1 warning UV or OV fault. 1 = Follow Case 1 response.

7.81 OPT_FLT_RESP5 - 0x124

Name	Bit	Type	Default	Description
OPT_LDO4_SEV_UVOV_RESP	7:6	FRW	0x0	LDO4 Severe under and overvoltage response control 0 = Case 0. No response to LDO2 severe UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
Reserved	5	R	0x0	-
OPT_LDO4_WARN_UVOV_RESP	4	FRW	0x0	LDO4 Warning under and overvoltage response control 0 = Case 0. No response to LDO4 warning UV or OV fault. 1 = Follow Case 1 response.
OPT_LDO3_SEV_UVOV_RESP	3:2	FRW	0x0	LDO3 Severe under and overvoltage response control 0 = Case 0. No response to LDO1 severe UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
Reserved	1	R	0x0	-
OPT_LDO3_WARN_UVOV_RESP	0	FRW	0x0	LDO3 Warning under and overvoltage response control 0 = Case 0. No response to LDO1 warning UV or OV fault. 1 = Follow Case 1 response.

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7.82 OPT_FLT_RESP6 - 0x125

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_TSD_FUSA_RESP	5:4	FRW	0x0	Over-temperature fault response control (FuSa TSD) 0 = Case 0. Ignore over-temperature fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.

Name	Bit	Type	Default	Description
OPT_DCDC2_OC2_RESP	3:2	FRW	0x2	DCDC2 overcurrent response control. Must set either Case 2 or Case 3 response 0 = Not supported 1 = Not supported 2 = Follow Case 2 response. 3 = Follow Case 3 response. Default setting is set by OTP configuration. If Bit[3:2] = 0x0 or 0x1, the DCDC2 OC2 fault response is latch off and shuts down immediately.
OPT_ARCH_MON_FLT_RESP	1:0	FRW	0x0	AGND, DGND, BG OV/UV, and FuSA HKOK monitor fault responses 0 = Ignore AGND, DGND, BG OV/UV, and FuSa housekeeping OK faults (not recommended) 1 = Follow Case 1 response. (not recommended) 2 = Follow Case 2 response. 3 = Follow Case 3 response.

7.83 OPT_FLT_RESP7 - 0x126 (ASIL-D only)

Name	Bit	Type	Default	Description
OPT_COREMON_SEV_UV_RESP	7:6	FRW	0x0	Core monitor severe undervoltage response control 0 = Case 0. Ignore COREMON SEVERE UV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
OPT_COREMON_SEV_OV_RESP	5:4	FRW	0x0	Core monitor severe overvoltage response control 0 = Case 0. Ignore COREMON SEVERE OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
OPT_COREMON_WARN_UV_RESP	3:2	FRW	0x0	Core monitor undervoltage response control 0 = Case 0. Ignore COREMON UV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
OPT_COREMON_WARN_OV_RESP	1:0	FRW	0x0	Core monitor overvoltage response control 0 = Case 0. Ignore COREMON OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.

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7.84 OPT_FLT_RESP8 - 0x127

Name	Bit	Type	Default	Description
OPT_LDO0_SEV_UVOV_RESP	7:6	FRW	0x0	LDO0 Severe under and overvoltage response control 0 = Case 0. No response to LDO0 severe UV or OV fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
Reserved	5	R	0x0	-
OPT_LDO0_WARN_UVOV_RESP	4	FRW	0x0	LDO0 Warning under and overvoltage response control 0 = Case 0. No response to LDO0 warning UV or OV fault. 1 = Follow Case 1 response.

Name	Bit	Type	Default	Description
OPT_SSPB_FLT_RESP	3:2	FRW	0x0	SSPB pin fault response control. SSPB pin monitor detects if sensed SSPB pin mismatches expected. 0 = Case 0. Ignore SSPB pin fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.
OPT_RSTB_FLT_RESP	1:0	FRW	0x0	RSTB pin fault response control. RSTB pin monitor detects if sensed RSTB pin mismatches expected. 0 = Case 0. Ignore RSTB pin fault. 1 = Follow Case 1 response. 2 = Follow Case 2 response. 3 = Follow Case 3 response.

7.85 OPT_FLT_SHDN1 - 0x128

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_LDO4_TSD_SHDN	5	FRW	0x0	LDO4 Over-temperature shutdown on fault response control 0 = Ignore fault 1 = Shuts down LDO4 on TSD fault and remain off unless re-enabled using SPI
OPT_LDO3_TSD_SHDN	4	FRW	0x0	LDO3 Over-temperature shutdown on fault response control 0 = Ignore fault 1 = Shuts down LDO3 on TSD fault and remain off unless re-enabled using SPI
Reserved	3:2	R	0x0	-
OPT_DCDC2_SEV_UVOV_SHDN	1	FRW	0x0	DCDC2 Severe UV/OV rail shutdown on fault response control 0 = DCDC2 continues operation on fault. Applies only when OPT_DCDC2_SEV_UVOV_RESP is set to 0 or 1, otherwise shuts down on fault 1 = Shuts down DCDC2 on fault. Can be restarted using SPI. Valid for all OPT_DCDC2_SEV_UVOV_RESP settings
OPT_DCDC2_WARN_UVOV_SHDN	0	FRW	0x0	DCDC2 Warning UV/OV rail shutdown on fault response control 0 = DCDC2 continues operation on fault. Applies only when OPT_DCDC2_WARN_UVOV_RESP is set to 0 or 1, otherwise shuts down on fault 1 = Shuts down DCDC2 on fault. Can be restarted using SPI. Valid for all OPT_DCDC2_WARN_UVOV_RESP settings

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7.86 OPT_FLT_SHDN2 - 0x129

Name	Bit	Type	Default	Description
OPT_LDO4_SEV_UVOV_SHDN	7	FRW	0x0	LDO4/Tracker 4 shutdown response control to severe faults 0 = Ignore fault 1 = Shuts down LDO4 on severe UV or OV fault and remain off unless re-enabled using SPI
OPT_LDO4_WARN_UVOV_SHDN	6	FRW	0x0	LDO4/Tracker 4 shutdown response control to warning faults 0 = Ignore fault 1 = Shuts down LDO4 on warning UV or OV fault and remain off unless re-enabled using SPI
OPT_LDO3_SEV_UVOV_SHDN	5	FRW	0x0	LDO3/Tracker 3 shutdown response control to severe faults 0 = Ignore fault 1 = Shuts down LDO3 on severe UV or OV fault and remain off unless re-enabled using SPI
OPT_LDO3_WARN_UVOV_SHDN	4	FRW	0x0	LDO3/Tracker 3 shutdown response control to warning faults 0 = Ignore fault 1 = Shuts down LDO3 on warning UV or OV fault and remain off unless re-enabled using SPI
OPT_LDO2_SEV_UVOV_SHDN	3	FRW	0x0	LDO2 shutdown response control to severe faults 0 = Ignores fault 1 = Shuts down LDO2 on severe UV or OV fault and remain off unless re-enabled using SPI
OPT_LDO2_WARN_UVOV_SHDN	2	FRW	0x0	LDO2 shutdown response control to warning faults 0 = Ignore fault 1 = Shuts down LDO2 on warning UV or OV fault and remain off unless re-enabled using SPI
OPT_LDO1_SEV_UVOV_SHDN	1	FRW	0x0	LDO1 shutdown response control to severe faults 0 = Ignore fault 1 = Shuts down LDO1 on severe UV or OV fault and remain off unless re-enabled using SPI
OPT_LDO1_WARN_UVOV_SHDN	0	FRW	0x0	LDO1 shutdown response control to warning faults 0 = Ignore fault 1 = Shuts down LDO1 on warning UV or OV fault and remain off unless re-enabled using SPI

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7.87 FAULT_RESP9- 0x12A

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x00	-
MANUAL_FAULT	2	W1S	0x0	Manual fault start control Writing a 1 initiates a SPI triggered fault response case as programmed in the MANUAL_FAULT_RESP value. The MANUAL_FAULT_RECORD bit is also set.
MANUAL_FAULT_RESP	1:0	RW	0x0	Manual fault response control 0 = Case 0. No response 1 = Follow Case 1 response 2 = Follow Case 2 response 3 = Follow Case 3 response

7.88 OPT_INTB_MASK1 - 0x140

Name	Bit	Type	Default	Description
OPT_INTB_MASK_DCDC1_OC2	7	FRW	0x0	DCDC1 OC2 fault to INTB (ASIL-D only) Fault recorded in DCDC1_OC2_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_TSD34	6	FRW	0x0	TSD LDO3/4 monitor fault to INTB pin Fault recorded in TSD_LDO34_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_TSD	5	FRW	0x0	TSD monitor fault to INTB pin Fault recorded in TSD_FUSA_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_SYS_OSC	4	FRW	0x0	System clock monitor (17.6MHz) faults to INTB pin Faults recorded in CLK_OVER_FREQ_FAULT_RECORD and CLK_UNDER_FREQ_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_SPI_FAULT	3	FRW	0x0	SPI CRC and SPI write check faults to INTB pin Faults recorded in SPI_CRC_FAULT_RECORD and SPI_WRITE_THROUGH_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_DCDC1_OC1	2	FRW	0x0	DCDC1 overcurrent fault to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_VBAT_UVLO	1	FRW	0x0	VBAT below V_{BAT_SDN} fault to INTB pin Fault recoded in VBAT_UVLO_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_REG_FAULT	0	FRW	0x0	Register configuration check faults to INTB pin Faults recorded in CRC_RECHECK_FAULT_RECORD and RW_REG_FAULT_RECORD 0 = Not masked 1 = Masked

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7.89 OPT_INTB_MASK2 - 0x141

Name	Bit	Type	Default	Description
OPT_INTB_MASK_VDDIO_FAULT	7	FRW	0x0	VDDIO_OK fault to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_SST_FAULT	6	FRW	0x0	WDT SST fault to INTB pin WDT system self test timer timeout detected 0 = Not masked 1 = Masked
OPT_INTB_MASK_REG1_ BUCKBOOST_MODE	5	FRW	0x0	REG1 buck boost mode to INTB pin Fault recorded in REG1_BUCKBOOST_MODE_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_PIN_FAULT	4	FRW	0x0	Pin fault to INTB pin SSPB or RSTB pin sensed high but driven low. 0 = Not masked 1 = Masked

Name	Bit	Type	Default	Description
OPT_INTB_MASK_FB2_UVOV_SEV	3	FRW	0x0	DCDC2 UV/OV severe faults to INTB pin Faults recorded in FB2_SEVERE_UV_FAULT_RECORD and FB2_SEVERE_OV_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_FB2_UVOV_WARN	2	FRW	0x0	DCDC2 UV/OV warning faults to INTB pin Faults recorded in FB2_WARN_UV_FAULT_RECORD and FB2_OV_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_FB1_UVOV_SEV	1	FRW	0x0	DCDC1 UV/OV severe faults to INTB pin Faults recorded in FB1_SEVERE_UV_FAULT_RECORD and FB1_SEVERE_OV_FAULT_RECORD 0 = Not masked 1 = Masked
OPT_INTB_MASK_FB1_UVOV_WARN	0	FRW	0x0	DCDC1 UV/OV warning faults to INTB pin Faults recorded in FB1_WARN_UV_FAULT_RECORD and FB1_WARN_OV_FAULT_RECORD 0 = Not masked 1 = Masked

7.90 OPT_INTB_MASK3 - 0x142

Name	Bit	Type	Default	Description
OPT_INTB_MASK_LDO4_UVOV_SEV	7	FRW	0x0	LDO4 UV/OV severe faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO4_UVOV_WARN	6	FRW	0x0	LDO4 UV/OV warning faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO3_UVOV_SEV	5	FRW	0x0	LDO3 UV/OV severe faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO3_UVOV_WARN	4	FRW	0x0	LDO3 UV/OV warning faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO2_UVOV_SEV	3	FRW	0x0	LDO2 UV/OV severe faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO2_UVOV_WARN	2	FRW	0x0	LDO2 UV/OV warning faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO1_UVOV_SEV	1	FRW	0x0	LDO1 UV/OV severe faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO1_UVOV_WARN	0	FRW	0x0	LDO1 UV/OV warning faults to INTB pin 0 = Not masked 1 = Masked

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7.91 OPT_INTB_MASK4 - 0x143

Name	Bit	Type	Default	Description
OPT_INTB_MASK_COREM_UVOV_SEV	7	FRW	0x0	Core monitor UV/OV severe faults to INTB pin (ASIL-D only) 0 = Not masked 1 = Masked
OPT_INTB_MASK_COREM_UVOV_WARN	6	FRW	0x0	Core monitor UV/OV warning faults to INTB pin (ASIL-D only) 0 = Not masked 1 = Masked
OPT_INTB_ERRB_FAULT	5	FRW	0x0	ERRB fault to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_VMONB_FAULT	4	FRW	0x0	VMONB fault to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO0_UVOV_SEV	3	FRW	0x0	LDO0 UV/OV severe faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_LDO0_UVOV_WARN	2	FRW	0x0	LDO0 UV/OV warning faults to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_DCDC2_OC2	1	FRW	0x0	DCDC2 overcurrent fault to INTB pin 0 = Not masked 1 = Masked
OPT_INTB_MASK_ARCHMON_FAULT	0	FRW	0x0	Architecture monitors: AGND, DGND, BG UV/OV, FuSa housekeeping faults to INTB pin Faults recorded in AGND_FAULT_RECORD, DGND_FAULT_RECORD, VBG_UV_FAULT_RECORD, VBG_OV_FAULT_RECORD, and FUSA_HKOK_FLT_RECORD 0 = Not masked 1 = Masked

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7.92 INTB_MASK5 - 0x144

Name	Bit	Type	Default	Description
INTB_MASK_CD_ZERO	7	RW	0x1	63 second count-down alarm to INTB pin 0 = Not masked 1 = Masked
INTB_MASK_EOT_OVF	6	RW	0x1	EOT Overflow alarm to INTB pin 0 = Not masked 1 = Masked
INTB_MASK_EOT_PD	5	RW	0x1	EOT power-down alarm to INTB pin 0 = Not masked 1 = Masked
INTB_MASK_EOT_WU	4	RW	0x1	EOT Wake-up alarm to INTB pin 0 = Not masked 1 = Masked
INTB_MASK_TOACC_FAULT	3	RW	0x1	WDT timeout accumulator fault to INTB pin 0 = Not masked 1 = Masked
INTB_MASK_TO_FAULT	2	RW	0x1	WDT timeout fault to INTB pin 0 = Not masked 1 = Masked

Name	Bit	Type	Default	Description
INTB_MASK_ACC_FAULT	1	RW	0x1	WDT accumulator fault to INTB pin 0 = Not masked 1 = Masked
INTB_MASK_WDT_FAULT	0	RW	0x1	WDT early, late, and answer faults to INTB pin 0 = Not masked 1 = Masked

7.93 INTB_MASK6 - 0x145

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x00	-
INTB_MASK_MANUAL_FAULT	0	RW	0x0	SPI-triggered manual fault to INTB pin 0 = Not masked 1 = Masked

7.94 OPT_SSPB_MASK1 - 0x148

Name	Bit	Type	Default	Description
OPT_SSPB_MASK_REG_FAULT	7	FRW	0x0	Register fault to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_TSD34	6	FRW	0x0	TSD34 fault to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_TSD	5	FRW	0x0	TSD fault to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_SYS_OSC	4	FRW	0x0	System Oscillator faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_FB2_UVOV_SEV	3	FRW	0x0	DCDC2 UV/OV severe faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_FB2_UVOV_WARN	2	FRW	0x0	DCDC2 UV/OV warning faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_FB1_UVOV_SEV	1	FRW	0x0	DCDC1 UV/OV severe faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_FB1_UVOV_WARN	0	FRW	0x0	DCDC1 UV/OV warning faults to SSPB pin 0 = Not masked 1 = Masked

7.95 OPT_SSPB_MASK2 - 0x149

Name	Bit	Type	Default	Description
OPT_SSPB_MASK_LDO4_UVOV_SEV	7	FRW	0x0	LDO4 UV/OV severe faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO4_UVOV_WARN	6	FRW	0x0	LDO4 UV/OV warning faults to SSPB pin 0 = Not masked 1 = Masked

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Name	Bit	Type	Default	Description
OPT_SSPB_MASK_LDO3_UVOV_SEV	5	FRW	0x0	LDO3 UV/OV severe faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO3_UVOV_WARN	4	FRW	0x0	LDO3 UV/OV warning faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO2_UVOV_SEV	3	FRW	0x0	LDO2 UV/OV severe faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO2_UVOV_WARN	2	FRW	0x0	LDO2 UV/OV warning faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO1_UVOV_SEV	1	FRW	0x0	LDO1 UV/OV severe faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO1_UVOV_WARN	0	FRW	0x0	LDO1 UV/OV warning faults to SSPB pin 0 = Not masked 1 = Masked

7.96 OPT_SSPB_MASK3 - 0x14A

Name	Bit	Type	Default	Description
OPT_SSPB_MASK_COREM_UVOV_SEV	7	FRW	0x0	Core monitor UV/OV severe faults to SSPB pin (ASIL-D only) 0 = Not masked 1 = Masked
OPT_SSPB_MASK_COREM_UVOV_WARN	6	FRW	0x0	Core monitor UV/OV warning faults to SSPB pin (ASIL-D only) 0 = Not masked 1 = Masked
OPT_SSPB_ERRB_FAULT	5	FRW	0x0	ERRB fault to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_VMONB_FAULT	4	FRW	0x0	VMONB fault to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO0_UVOV_SEV	3	FRW	0x0	LDO0 UV/OV severe faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_LDO0_UVOV_WARN	2	FRW	0x0	LDO0 UV/OV warning faults to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_DCDC2_OC2	1	FRW	0x0	DCDC2 overcurrent fault to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_ARCHMON_FAULT	0	FRW	0x0	Architecture monitors= AGND, DGND, BG UV/OV, and FuSa Housekeeping faults to SSPB pin 0 = Not masked 1 = Masked

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7.97 SSPB_MASK4 - 0x14B

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
SSPB_MASK_TOACC_FAULT	3	RW	0x0	WDT timeout accumulator fault to SSPB pin 0 = Not masked 1 = Masked
SSPB_MASK_TO_FAULT	2	RW	0x0	WDT timeout fault to SSPB pin 0 = Not masked 1 = Masked
SSPB_MASK_ACC_FAULT	1	RW	0x0	WDT accumulator fault to SSPB pin 0 = Not masked 1 = Masked
SSPB_MASK_WDT_FAULT	0	RW	0x0	WDT early, late, and answer faults to SSPB pin 0 = Not masked 1 = Masked

7.98 SSPB_CTRL - 0x14C

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x0	-
FORCE_SSPB_OFF	0	RW	0x0	Force de-assertion of SSPB pin 0 = SSPB pin follows ACTIVE state and any unmasked *_FAULT_RECORD bits. 1 = SSPB is asserted off (safe state). Other controls are ignored.

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7.99 OPT_SSPB_MASK5 - 0x14D

Name	Bit	Type	Default	Description
Reserved	7:2	R	0x0	-
OPT_SSPB_MASK_VDDIO_FAULT	1	FRW	0x0	VDDIO_OK fault to SSPB pin 0 = Not masked 1 = Masked
OPT_SSPB_MASK_DCDC1_OC2	0	FRW	0x0	DCDC1 OC2 fault to SSPB pin (ASIL-D only) 0 = Not masked 1 = Masked

7.100 OPT_VOUT - 0x150

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_LDO4_VOUT	5	FRW	0x0	LDO4 output voltage option 0 = 3.3V 1 = 5V
OPT_LDO3_VOUT	4	FRW	0x0	LDO3 output voltage option 0 = 3.3V 1 = 5V
OPT_LDO2_VOUT	3	FRW	0x0	LDO2 output voltage option 0 = 3.3V 1 = 5V

Name	Bit	Type	Default	Description
OPT_LDO1_VOUT	2	FRW	0x0	LDO1 output voltage option 0 = 3.3V 1 = 5V
Reserved	1:0	FRW	0x0	-

7.101 OPT_FB1_THRESH - 0x151

Name	Bit	Type	Default	Description
OPT_DCDC1_WARN_OV	7:6	FRW	0x0	Sets DCDC1 OV warning fault threshold 0 = 4% 1 = 6% 2 = 8% 3 = 8%
OPT_DCDC1_WARN_UV	5:4	FRW	0x0	Sets DCDC1 UV warning fault threshold 0 = -4% 1 = -6% 2 = -8% 3 = -8%
Reserved	3	R	0x0	-
OPT_DCDC1_SEV_OV	2	FRW	0x0	Sets DCDC1 OV severe fault threshold 0 = 8% 1 = 10%
Reserved	1	R	0x0	-
OPT_DCDC1_SEV_UV	0	FRW	0x0	Sets DCDC1 UV severe fault threshold 0 = -8% 1 = -10%

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7.102 OPT_FB2_THRESH - 0x152

Name	Bit	Type	Default	Description
OPT_DCDC2_WARN_OV	7:6	FRW	0x0	Sets DCDC2 OV warning fault threshold 0 = 4% 1 = 8% 2 = 12% 3 = 12%
OPT_DCDC2_WARN_UV	5:4	FRW	0x0	Sets DCDC2 UV warning fault threshold 0 = -4% 1 = -8% 2 = -12% 3 = -12%
Reserved	3	R	0x0	-
OPT_DCDC2_SEV_OV	2	FRW	0x0	Sets DCDC2 OV severe fault threshold 0 = 10% 1 = 14%
Reserved	1	R	0x0	-
OPT_DCDC2_SEV_UV	0	FRW	0x0	Sets DCDC2 UV severe fault threshold 0 = -10% 1 = -14%

7.103 OPT_LDO1_THRESH - 0x153

Name	Bit	Type	Default	Description
OPT_LDO1_WARN_OV	7:6	FRW	0x0	Sets LDO1 OV warning fault threshold 0 = 4% 1 = 8% 2 = 12% 3 = 12%
OPT_LDO1_WARN_UV	5:4	FRW	0x0	Sets LDO1 UV warning fault threshold 0 = -4% 1 = -8% 2 = -12% 3 = -12%
Reserved	3	R	0x0	-
OPT_LDO1_SEV_OV	2	FRW	0x0	Sets LDO1 OV severe fault threshold 0 = 10% 1 = 14%
Reserved	1	R	0x0	-
OPT_LDO1_SEV_UV	0	FRW	0x0	Sets LDO1 UV severe fault threshold 0 = -10% 1 = -14%

7.104 OPT_LDO2_THRESH - 0x154

Name	Bit	Type	Default	Description
OPT_LDO2_WARN_OV	7:6	FRW	0x0	Sets LDO2 OV warning fault threshold 0 = 4% 1 = 8% 2 = 12% 3 = 12%
OPT_LDO2_WARN_UV	5:4	FRW	0x0	Sets LDO2 UV warning fault threshold 0 = -4% 1 = -8% 2 = -12% 3 = -12%
Reserved	3	R	0x0	-
OPT_LDO2_SEV_OV	2	FRW	0x0	Sets LDO2 OV severe fault threshold 0 = 10% 1 = 14%
Reserved	1	R	0x0	-
OPT_LDO2_SEV_UV	0	FRW	0x0	Sets LDO2 UV severe fault threshold 0 = -10% 1 = -14%

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7.105 OPT_LDO3_THRESH - 0x155

Name	Bit	Type	Default	Description
OPT_LDO3_WARN_OV	7:6	FRW	0x0	Sets LDO3 OV warning fault threshold 0 = 4% 1 = 8% 2 = 12% 3 = 12%
OPT_LDO3_WARN_UV	5:4	FRW	0x0	Sets LDO3 UV warning fault threshold 0 = -4% 1 = -8% 2 = -12% 3 = -12%
Reserved	3	R	0x0	-
OPT_LDO3_SEV_OV	2	FRW	0x0	Sets LDO3 OV severe fault threshold 0 = 10% 1 = 14%
Reserved	1	R	0x0	-
OPT_LDO3_SEV_UV	0	FRW	0x0	Sets LDO3 UV severe fault threshold 0 = -10% 1 = -14%

7.106 OPT_LDO4_THRESH - 0x156

Name	Bit	Type	Default	Description
OPT_LDO4_WARN_OV	7:6	FRW	0x0	Sets LDO4 OV warning fault threshold 0 = 4% 1 = 8% 2 = 12% 3 = 12%
OPT_LDO4_WARN_UV	5:4	FRW	0x0	Sets LDO4 UV warning fault threshold 0 = -4% 1 = -8% 2 = -12% 3 = -12%
Reserved	3	R	0x0	-
OPT_LDO4_SEV_OV	2	FRW	0x0	Sets LDO4 OV severe fault threshold 0 = 10% 1 = 14%
Reserved	1	R	0x0	-
OPT_LDO4_SEV_UV	0	FRW	0x0	Sets LDO4 UV severe fault threshold 0 = -10% 1 = -14%

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7.107 OPT_COREMON_THRESH - 0x157 (ASIL-D only)

Name	Bit	Type	Default	Description
OPT_COREMON_WARN_OV	7:6	FRW	0x0	Sets COREMON OV warning fault threshold 0 = 4% 1 = 8% 2 = 12% 3 = 12%
OPT_COREMON_WARN_UV	5:4	FRW	0x0	Sets COREMON UV warning fault threshold 0 = -4% 1 = -8% 2 = -12% 3 = -12%
Reserved	3	R	0x0	-
OPT_COREMON_SEV_OV	2	FRW	0x0	Sets COREMON OV severe fault threshold 0 = 10% 1 = 14%
Reserved	1	R	0x0	-
OPT_COREMON_SEV_UV	0	FRW	0x0	Sets COREMON UV severe fault threshold 0 = -10% 1 = -14%

7.108 OPT_LDO0_THRESH - 0x158

Name	Bit	Type	Default	Description
OPT_LDO0_WARN_OV	7:6	FRW	0x0	Sets LDO0 OV warning fault threshold 0 = 4% 1 = 8% 2 = 12% 3 = 12%
OPT_LDO0_WARN_UV	5:4	FRW	0x0	Sets LDO0 UV warning fault threshold 0 = -4% 1 = -8% 2 = -12% 3 = -12%
Reserved	3	R	0x0	-
OPT_LDO0_SEV_OV	2	FRW	0x0	Sets LDO0 OV severe fault threshold 0 = 10% 1 = 14%
Reserved	1	R	0x0	-
OPT_LDO0_SEV_UV	0	FRW	0x0	Sets LDO0 UV severe fault threshold 0 = -10% 1 = -14%

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7.109 OPT_FAULT_DLY1 - 0x160

Name	Bit	Type	Default	Description
OPT_DCDC2_SEV_OVUV_DLY_FILT	7:6	FRW	0x0	DCDC2 Severe OVUV filter Fault digital debounce time 0 = 1us 1 = 5µs 2 = 10µs 3 = 25µs
OPT_DCDC2_WARN_OVUV_DLY_FILT	5:4	FRW	0x0	DCDC2 Warning OVUV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs
OPT_DCDC1_SEV_OVUV_DLY_FILT	3:2	FRW	0x0	DCDC1 Severe OVUV filter Fault digital debounce time 0 = 1us 1 = 5µs 2 = 10µs 3 = 25µs
OPT_DCDC1_WARN_OVUV_DLY_FILT	1:0	FRW	0x0	DCDC1 Warning OVUV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs

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7.110 OPT_FAULT_DLY2 - 0x161

Name	Bit	Type	Default	Description
OPT_LDO2_SEV_OVUV_DLY_FILT	7:6	FRW	0x0	LDO2 Severe OVUV filter Fault digital debounce time 0 = 1µs 1 = 5µs 2 = 10µs 3 = 25µs
OPT_LDO2_WARN_OVUV_DLY_FILT	5:4	FRW	0x0	LDO2 Warning OVUV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs
OPT_LDO1_SEV_OVUV_DLY_FILT	3:2	FRW	0x0	LDO1 Severe OVUV filter Fault digital debounce time 0 = 1µs 1 = 5µs 2 = 10µs 3 = 25µs
OPT_LDO1_WARN_OVUV_DLY_FILT	1:0	FRW	0x0	LDO1 Warning OVUV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs

7.111 OPT_FAULT_DLY3 - 0x162

Name	Bit	Type	Default	Description
OPT_LDO4_SEV_OVUV_DLY_FILT	7:6	FRW	0x0	LDO4 Severe OVUV filter Fault digital debounce time 0 = 1µs 1 = 5µs 2 = 10µs 3 = 25µs
OPT_LDO4_WARN_OVUV_DLY_FILT	5:4	FRW	0x0	LDO4 Warning OVUV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs
OPT_LDO3_SEV_OVUV_DLY_FILT	3:2	FRW	0x0	LDO3 Severe OVUV filter Fault digital debounce time 0 = 1µs 1 = 5µs 2 = 10µs 3 = 25µs
OPT_LDO3_WARN_OVUV_DLY_FILT	1:0	FRW	0x0	LDO3 Warning OVUV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs

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7.112 OPT_FAULT_DLY4 - 0x163 (ASIL-D only)

Name	Bit	Type	Default	Description
OPT_COREMON_SEV_UV_DLY_FILT	7:6	FRW	0x0	COREMON Severe UV filter Fault digital debounce time 0 = 1µs 1 = 5µs 2 = 10µs 3 = 25µs
OPT_COREMON_WARN_UV_DLY_FILT	5:4	FRW	0x0	COREMON Warning UV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs
OPT_COREMON_SEV_OV_DLY_FILT	3:2	FRW	0x0	COREMON Severe OV filter Fault digital debounce time 0 = 1µs 1 = 5µs 2 = 10µs 3 = 25µs
OPT_COREMON_WARN_OV_DLY_FILT	1:0	FRW	0x0	COREMON Warning OV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs

7.113 OPT_FAULT_DLY5 - 0x164

Name	Bit	Type	Default	Description
OPT_LDO0_SEV_OVUV_DLY_FILT	7:6	FRW	0x0	LDO0 Severe OVUV filter Fault digital debounce time 0 = 1µs 1 = 5µs 2 = 10µs 3 = 25µs
OPT_LDO0_WARN_OVUV_DLY_FILT	5:4	FRW	0x0	LDO0 Warning OVUV filter Fault digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs
OPT_ARCH_MON_DLY_FILT	3:2	FRW	0x0	VCC OV/UV, AGND, DGND, OV/UV, BG OV/UV Digital debounce time 0 = 10µs 1 = 25µs 2 = 50µs 3 = 100µs
OPT_TSD_FUSA_DLY_FILT	1:0	FRW	0x0	FuSa over temperature filter Fault digital debounce time 0 = 50µs 1 = 100µs 2 = 1ms 3 = 2.5ms

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7.114 OPT_DEV_MODE1 - 0x200

Name	Bit	Type	Default	Description
OPT_PSTBY0_IN_DS	7	FRW	0x0	Controls PSTBYB usage in DeepSTOP state 0 = Ignore PSTBYB low in DeepSTOP state 1 = PSTBYB low in DeepSTOP forces DeepSTOP exit and return to high power state.
OPT_EN_SEC_ACC	6	FRW	0x0	Controls usage of secured register access If set, all SPI registers listed as secure require the write access using a KEY. Refer to the SECURE_KEY register description for details. 0 = Do not use key for secure access 1 = Use key for secure access
OPT_LDO4_MODE	5	FRW	0x0	Selects LDO4 as tracker or LDO. 0 = LDO4 used in tracker mode 1 = LDO4 used in LDO mode
OPT_LDO3_MODE	4	FRW	0x0	Selects LDO3 as tracker or LDO. 0 = LDO3 used in tracker mode 1 = LDO3 used in LDO mode
Reserved	3	R	0x0	-
OPT_SPI_HIZ	2	FRW	0x0	SPISDO Output drive control 0 = Always driven 1 = Hi-Z when SPICSB is high. Driven when SPICSB is low.

Name	Bit	Type	Default	Description
OPT_SSPB_INV	1	FRW	0x0	SSPB pin inversion control 0 = Assert SSPB pin high when in ACTIVE state 1 = Assert SSPB pin low when in ACTIVE state
OPT_SPI_CRC	0	FRW	0x0	SPI CRC format and checking 0 = Not used 1 = Used

7.115 OPT_DEV_MODE2 - 0x201

Name	Bit	Type	Default	Description
OPT_WAIT_VTR	7	FRW	0x0	Use VTR to holdoff tracker startup 0 = LDO tracker waits for VTR UVLO within 3ms of enable, then regardless of VTR UVLO, tracker starts up 1 = LDO tracker waits indefinitely for VTR UVLO to clear for startup
OPT_INTB_OD	6	FRW	0x0	INTB Open drain output selection 0 = Push/pull 1 = Open drain
OPT_RSTB_DLY	5:4	FRW	0x0	At PMIC startup, sets delay between VMONB detected high and RSTB high assertion. Delayed shown are nominal (±20% tolerance) 0 = 0ms 1 = 1.5ms 2 = 2ms 3 = 5ms
OPT_DCDC2_SS_RATE	3:2	FRW	0x0	DCDC2 soft start rate 0 = 10µs/step (128 steps × 10µs/step = 1.28ms total soft start time) 1 = 20µs/step (128 steps × 20µs/step = 2.56ms total soft start time) 2 = 40µs/step (128 steps × 40µs/step = 5.12ms total soft start time) 3 = 100µs/step (128 steps × 100µs/step = 12.8ms total soft start time)
OPT_DCDC1_SS_RATE	1:0	FRW	0x0	DCDC1 soft start rate 0 = 10µs/step (128 steps × 10µs/step = 1.28ms total soft start time) 1 = 20µs/step (128 steps × 20µs/step = 2.56ms total soft start time) 2 = 40µs/step (128 steps × 40µs/step = 5.12ms total soft start time) 3 = 100µs/step (128 steps × 100µs/step = 12.8ms total soft start time)

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7.116 OPT_DEV_MODE3 - 0x202

Name	Bit	Type	Default	Description
OPT_LDO4_SS_RATE	7:6	FRW	0x0	LDO4 soft start rate 0 = 10µs/step (128 steps × 10µs/step = 1.28ms total soft start time) 1 = 20µs/step (128 steps × 20µs/step = 2.56ms total soft start time) 2 = 40µs/step (128 steps × 40µs/step = 5.12ms total soft start time) 3 = 100µs/step (128 steps × 100µs/step = 12.8ms total soft start time)
OPT_LDO3_SS_RATE	5:4	FRW	0x0	LDO3 soft start rate 0 = 10µs/step (128 steps × 10µs/step = 1.28ms total soft start time) 1 = 20µs/step (128 steps × 20µs/step = 2.56ms total soft start time) 2 = 40µs/step (128 steps × 40µs/step = 5.12ms total soft start time) 3 = 100µs/step (128 steps × 100µs/step = 12.8ms total soft start time)
Reserved	3	R	0x0	-
OPT_LDO2_SS_RATE	2	FRW	0x0	LDO2 soft start rate 0 = 10µs/step (128 steps × 10µs/step = 1.28ms total soft start time) 1 = 20µs/step (128 steps × 20µs/step = 2.56ms total soft start time)
Reserved	1	R	0x0	-
OPT_LDO1_SS_RATE	0	FRW	0x0	LDO1 soft start rate 0 = 10µs/step (128 steps × 10µs/step = 1.28ms total soft start time) 1 = 20µs/step (128 steps × 20µs/step = 2.56ms total soft start time)

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7.117 SEL_DEV_MODE1 - 0x203

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	-
SEL_FREQ_REG2	4	FRW	0x0	Selects the DCDC2 center switching frequency 0 = 440kHz (ASIL-D only) 1 = 2.2MHz
Reserved	3:1	R	0x0	-
SEL_FREQ_REG1	0	FRW	0x0	Selects the DCDC1 center switching frequency 0 = 440kHz (ASIL-D only) 1 = 2.2MHz

7.118 OPT_WAIT_DISCHG1 - 0x204

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
OPT_DCDC2_WAIT_DISCG[1]	3:2	FRW	0x0	DCDC2 Discharge before restart control 0 = Regulator must wait for 50ms to discharge before allowed to restart 1 = Regulator must wait for 20ms to discharge before allowed to restart 2 = Regulator must wait for 10ms to discharge before allowed to restart 3 = Regulator can restart any time
OPT_DCDC1_WAIT_DISCG	1:0	FRW	0x0	DCDC1 Discharge before restart control 0 = Regulator must wait for 50ms to discharge before allowed to restart 1 = Regulator must wait for 20ms to discharge before allowed to restart 2 = Regulator must wait for 10ms to discharge before allowed to restart 3 = Regulator can restart any time

1. If DCDC1 is restarting, the settings in this register must be ≥ the setting of the OPT_DCDC1_WAIT_DISCG setting

7.119 OPT_WAIT_DISCHG2 - 0x205

Name	Bit	Type	Default	Description
OPT_LDO4_WAIT_DISCG[1]	7:6	FRW	0x0	LDO4 Discharge before restart control 0 = Regulator must wait for 50ms (Tracker mode) or 25ms (LDO mode) to discharge before allowed to restart 1 = Regulator must wait for 20ms (Tracker mode) or 10ms (LDO mode) to discharge before allowed to restart 2 = Regulator must wait for 10ms (Tracker mode) or 5ms (LDO mode) to discharge before allowed to restart 3 = Regulator can restart any time
OPT_LDO3_WAIT_DISCG[1]	5:4	FRW	0x0	LDO3 Discharge before restart control 0 = Regulator must wait for 50ms (Tracker mode) or 25ms (LDO mode) to discharge before allowed to restart 1 = Regulator must wait for 20ms (Tracker mode) or 10ms (LDO mode) to discharge before allowed to restart 2 = Regulator must wait for 10ms (Tracker mode) or 5ms (LDO mode) to discharge before allowed to restart 3 = Regulator can restart any time
OPT_LDO2_WAIT_DISCG[1]	3:2	FRW	0x0	LDO2 Discharge before restart control 0 = Regulator must wait for 25ms to discharge before allowed to restart 1 = Regulator must wait for 10ms to discharge before allowed to restart 2 = Regulator must wait for 5ms to discharge before allowed to restart 3 = Regulator can restart any time
OPT_LDO1_WAIT_DISCG[1]	1:0	FRW	0x0	LDO1 Discharge before restart control 0 = Regulator must wait for 25ms to discharge before allowed to restart 1 = Regulator must wait for 10ms to discharge before allowed to restart 2 = Regulator must wait for 5ms to discharge before allowed to restart 3 = Regulator can restart any time

1. If DCDC1 is restarting, the settings in this register must be ≥ the setting of the OPT_DCDC1_WAIT_DISCG setting

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7.120 OPT_PD_CTRL - 0x206

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_DIS_PD_LDO4	5	FRW	0x0	Controls LDO4 pull down 0 = Pull-down enabled when regulator is off 1 = Pull-down not used
OPT_DIS_PD_LDO3	4	FRW	0x0	Controls LDO3 pull down 0 = Pull-down enabled when regulator is off 1 = Pull-down not used
OPT_DIS_PD_LDO2	3	FRW	0x0	Controls LDO2 pull down 0 = Pull-down enabled when regulator is off 1 = Pull-down not used
OPT_DIS_PD_LDO1	2	FRW	0x0	Controls LDO1 pull down 0 = Pull-down enabled when regulator is off 1 = Pull-down not used
OPT_DIS_PD_DCDC2	1	FRW	0x0	Controls DCDC2 pull down 0 = Pull-down enabled when regulator is off 1 = Pull-down not used
OPT_DIS_PD_DCDC1	0	FRW	0x0	Controls DCDC1 pull down 0 = Pull-down enabled when regulator is off 1 = Pull-down not used

7.121 OPT_STATE_CTRL - 0x207

Name	Bit	Type	Default	Description
OPT_FLT_HIC_CNT	7:6	FRW	0x0	Controls repeated fault count for Case 3 faults when OPT_FAULTED_RELEASE = 0. If limit is reached, latch off. 0 = 8 times 1 = 16 times 2 = 32 times 3 = 64 times
Reserved	5	FRW	0x1	Set to 1 Note: Bit[5] set to 1 by OTP configuration as default. Bit[5] value 1 enables the Case 2 and Case 3 fault response hiccup operation, so this bit requires to be set as 1 together with Case 2 or Case 3 fault response configuration.
OPT_DS_EXIT_BIST	4	FRW	0x0	BIST execution at DEEP_STOP exit control 0 = Do not run BIST on DEEP_STOP exit 1 = Run BIST on DEEP_STOP exit

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Name	Bit	Type	Default	Description
OPT_FAULTED_RELEASE	3:2	FRW	0x0	Sets behavior for exiting FAULTED state. FAULTED state is entered upon detection of Case 3 faults. If fault is removed perform the release sequence according to the following settings. 0 = Disable and restart up to a total of OPT_FLT_HIC_CNT attempts. If fault has not cleared, remain off. To release from FAULTED state when fault is removed, both WAKEs must be brought low and toggle either pin high to restart. Low period for WAKE pin restart is 1ms (minimum). 1 = WAKE1 low. PMIC remains in FAULTED state until WAKE1 is toggled low then high. Low period for WAKE1 restart is 1ms (minimum). 2 = WAKE2 low. PMIC remains in FAULTED state until WAKE2 is toggled low then high. Low period for WAKE2 restart is 1ms (minimum) 3 = Both WAKEs low. Set both WAKES low 1ms (minimum) then toggle either WAKE pin high to restart.
Reserved	1	FRW	0x0	-
Reserved	0	FRW	0x0	-

7.122 OPT_SS - 0x208 (ASIL-D only)

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x0	-
OPT_SPREAD_SPECTRUM	2:0	FRW	0x0	Selects spread spectrum algorithm 0 = spread spectrum disabled 1 = two slope modulation, 9.13kHz 2 = Pseudorandom w/random dwell 1-8 cycles 3 = Pseudorandom w/random dwell 4-32 cycles 4 = triangular modulation, 8.85kHz 5 = Pseudorandom w/fixed 4 cycle dwell 6 = Pseudorandom w/fixed 8 cycle dwell 7 = Pseudorandom w/fixed 24 cycle dwell

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7.123 OPT_WDENB_CTRL - 0x209

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x00	-
OPT_WDENB_OE	0	FRW	0x0	Selects direction of the WDENB pin 0 = Set to input 1 = Set to output

7.124 COREMON_CTRL - 0x20A (ASIL-D only)

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	-
COREMON_SEV_OV_EN	3	RW	0x0	COREMON Severe OV monitor enable 0 = Disable 1 = Enable
COREMON_SEV_UV_EN	2	RW	0x0	COREMON Severe UV monitor enable 0 = Disable 1 = Enable

Name	Bit	Type	Default	Description
COREMON_WARN_OV_EN	1	RW	0x0	COREMON Warning OV monitor enable 0 = Disable 1 = Enable
COREMON_WARN_UV_EN	0	RW	0x0	COREMON Warning UV monitor enable 0 = Disable 1 = Enable

7.125 OPT_PG_CTRL - 0x20B

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
OPT_PG_MON_LDO4	6	FRW	0x0	Enables LDO4 power-good monitoring on WDENB pin. 0 = Power-good status of regulator ignored 1 = Power-good status of regulator is monitored
OPT_PG_MON_LDO3	5	FRW	0x0	Enables LDO3 power-good monitoring on WDENB pin. 0 = Power-good status of regulator ignored 1 = Power-good status of regulator is monitored
OPT_PG_MON_LDO2	4	FRW	0x0	Enables LDO2 power-good monitoring on WDENB pin. 0 = Power-good status of regulator ignored 1 = Power-good status of regulator is monitored
OPT_PG_MON_LDO1	3	FRW	0x0	Enables LDO1 power-good monitoring on WDENB pin. 0 = Power-good status of regulator ignored 1 = Power-good status of regulator is monitored
OPT_PG_MON_DCDC2	2	FRW	0x0	Enables DCDC2 power-good monitoring on WDENB pin. 0 = Power-good status of regulator ignored 1 = Power-good status of regulator is monitored
OPT_PG_MON_DCDC1	1	FRW	0x0	Enables DCDC1 power-good monitoring on WDENB pin. 0 = Power-good status of regulator ignored 1 = Power-good status of regulator is monitored
OPT_PG_MON_LDO0	0	FRW	0x0	Enables LDO0 power-good monitoring on WDENB pin. 0 = Power-good status of regulator ignored 1 = Power-good status of regulator is monitored

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7.126 OPT_AMUX_BUF_OFFSET - 0x20C (ASIL-D only)

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_AMUX_BUF_OFFSET	5:0	R	0x0	Stored AMUX buffer offset correction value 1mv/bit, signed

7.127 OPT_CALIB_OSC32K - 0x20D

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x0	-
OPT_CALIB_OSC32K	2:0	FRW	0x0	32768Hz oscillator center frequency calibration

7.128 OPT_VDDIO - 0x20E

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
OPT_VDDIO_SEL	5:0	FRW	0x00	Used to indicate which PMIC output is externally connected to VDDIO 0 = VDDIO is connected to supply that is always powered (e.g. VCC)" 1 = LDO1 externally tied to VDDIO 2 = LDO2 externally tied to VDDIO 3 = LDO3 externally tied to VDDIO 4 = LDO4 externally tied to VDDIO 5 = DCDC2 externally tied to VDDIO

7.129 DATA_STORE - 0x20F

Name	Bit	Type	Default	Description
DATA_BYTE	7:0	RW	0x00	Available for application data storage. Not used by PMIC. Retains value unless PMIC transitions to OFF state (LDO0 OFF).

7.130 HOST_MSGCNT - 0x210

Name	Bit	Type	Default	Description
MSG_CNT	7:0	RW	0x0	Host Message Counter Increments on a byte write to any register. Ensures number of bytes written to the register map are as expected. The 8-bit value overflows from 255 to 0 SPI reads do not increment the host message counter.

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7.131 SECURE_KEY - 0x211

Name	Bit	Type	Default	Description
KEY	7:0	RW	0x00	Random key used to permit 1 write to a secured SPI register. When OPT_EN_SEC_ACC is set to 1, all SPI writes must read this random KEY value and write the same value back to the KEY register. This permits one subsequent write to any register in the 0x000 to 0x2FF range. A new randomized KEY value is created each time the KEY used. If the wrong key is provided, writes to the SPI register are blocked. Key is not required for reading secured registers.

7.132 BIST_DIAG_1 - 0x220

Name	Bit	Type	Default	Description
BIST_STAT_FB2_SEV_UV	7	R	0x0	BIST results for DCDC2 Severe UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_FB2_SEV_OV	6	R	0x0	BIST results for DCDC2 Severe OV monitor 0 = Failed or not run 1 = Passed

Name	Bit	Type	Default	Description
BIST_STAT_FB2_WARN_UV	5	R	0x0	BIST results for DCDC2 Warning UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_FB2_WARN_OV	4	R	0x0	BIST results for DCDC2 Warning OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_FB1_SEV_UV	3	R	0x0	BIST results for DCDC1 Severe UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_FB1_SEV_OV	2	R	0x0	BIST results for DCDC1 Severe OV monitor
BIST_STAT_FB1_WARN_UV	1	R	0x0	BIST results for DCDC1 Warning UV monitor
BIST_STAT_FB1_WARN_OV	0	R	0x0	BIST results for DCDC1 Warning OV monitor

7.133 BIST_DIAG_2 - 0x221

Name	Bit	Type	Default	Description
BIST_STAT_LDO2_SEV_UV	7	R	0x0	BIST results for LDO2 Severe UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO2_SEV_OV	6	R	0x0	BIST results for LDO2 Severe OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO2_WARN_UV	5	R	0x0	BIST results for LDO2 Warning UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO2_WARN_OV	4	R	0x0	BIST results for LDO2 Warning OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO1_SEV_UV	3	R	0x0	BIST results for LDO1 Severe UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO1_SEV_OV	2	R	0x0	BIST results for LDO1 Severe OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO1_WARN_UV	1	R	0x0	BIST results for LDO1 Warning UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO1_WARN_OV	0	R	0x0	BIST results for LDO1 Warning OV monitor 0 = Failed or not run 1 = Passed

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7.134 BIST_DIAG_3 - 0x222

Name	Bit	Type	Default	Description
BIST_STAT_LDO4_SEV_UV	7	R	0x0	BIST results for LDO4 Severe UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO4_SEV_OV	6	R	0x0	BIST results for LDO4 Severe OV monitor 0 = Failed or not run 1 = Passed

Name	Bit	Type	Default	Description
BIST_STAT_LDO4_WARN_UV	5	R	0x0	BIST results for LDO4 Warning UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO4_WARN_OV	4	R	0x0	BIST results for LDO4 Warning OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO3_SEV_UV	3	R	0x0	BIST results for LDO3 Severe UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO3_SEV_OV	2	R	0x0	BIST results for LDO3 Severe OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO3_WARN_UV	1	R	0x0	BIST results for LDO3 Warning UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO3_WARN_OV	0	R	0x0	BIST results for LDO3 Warning OV monitor 0 = Failed or not run 1 = Passed

7.135 BIST_DIAG_4 - 0x223

Name	Bit	Type	Default	Description
BIST_STAT_LDO0_SEV_UV	7	R	0x0	BIST results for LDO0 Severe UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO0_SEV_OV	6	R	0x0	BIST results for LDO0 Severe OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO0_WARN_UV	5	R	0x0	BIST results for LDO0 Warning UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_LDO0_WARN_OV	4	R	0x0	BIST results for LDO0 Warning OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_COREMON_SEV_UV	3	R	0x0	BIST results for COREMON Severe UV monitor (ASIL-D only) 0 = Failed or not run 1 = Passed
BIST_STAT_COREMON_SEV_OV	2	R	0x0	BIST results for COREMON Severe OV monitor (ASIL-D only) 0 = Failed or not run 1 = Passed
BIST_STAT_COREMON_WARN_UV	1	R	0x0	BIST results for COREMON Warning UV monitor (ASIL-D only) 0 = Failed or not run 1 = Passed
BIST_STAT_COREMON_WARN_OV	0	R	0x0	BIST results for COREMON Warning OV monitor (ASIL-D only) 0 = Failed or not run 1 = Passed

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7.136 BIST_DIAG_5 - 0x224

Name	Bit	Type	Default	Description
BIST_STAT_TSD_FUSA	7	R	0x0	BIST results for FuSa temperature sense monitor 0 = Failed or not run 1 = Passed
BIST_STAT_TSD_REG	6	R	0x0	BIST results for regulation temperature sense monitor 0 = Failed or not run 1 = Passed
BIST_STAT_SYS_CLK_UNF	5	R	0x0	BIST results for system clock under frequency monitor 0 = Failed or not run 1 = Passed
BIST_STAT_SYS_CLK_OVF	4	R	0x0	BIST results for system clock over frequency monitor 0 = Failed or not run 1 = Passed
BIST_STAT_VBG_UV	3	R	0x0	BIST results for VBG UV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_VBG_OV	2	R	0x0	BIST results for VBG OV monitor 0 = Failed or not run 1 = Passed
BIST_STAT_DGND	1	R	0x0	BIST results for DGND monitor 0 = Failed or not run 1 = Passed
BIST_STAT_AGND	0	R	0x0	BIST results for AGND monitor 0 = Failed or not run 1 = Passed

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7.137 BIST_DIAG_6 - 0x225

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	-
BIST_STAT_AZ	5	R	0x0	BIST results for FuSa auto-zero. 0 = Failed or not run 1 = Passed
BIST_STAT_FUSA_HKOK	4	R	0x0	BIST results for FuSa housekeeping OK monitor. 0 = Failed or not run 1 = Passed
BIST_STAT_FUSE_INIT	3	R	0x0	BIST results for fuse shadow initialization. Reports proper initialization of OPT_* registers after VBAT startup. *Note*: If an OPT_* register is altered using SPI, this bit returns to 0. In this case, 0 does not indicate a fail. 0 = OPT_* registers do not match fuse array 1 = Initial OPT_* register load matches fuse array (pass)
BIST_STAT_SSPB	2	R	0x0	BIST results for SSPB pin monitor 0 = Failed or not run 1 = Passed
BIST_STAT_RSTB	1	R	0x0	BIST results for RSTB pin monitor 0 = Failed or not run 1 = Passed
BIST_STAT_TSD_LDO34	0	R	0x0	BIST results for LDO3/4 temperature sensor monitor 0 = Failed or not run 1 = Passed

7.138 BIST_DIAG_7 - 0x226

Name	Bit	Type	Default	Description
LBIST_PASSED	7	R	0x0	LBIST passed. Valid after LBIST completes 0 = LBIST fail (if LBIST_DONE = 1) 1 = LBIST passed
LBIST_DONE	6	R	0x0	LBIST complete 0 = LBIST has not completed 1 = LBIST completed
Reserved	5	R	0x0	-
CLEAR_LBIST_STATUS	4	W1S	0x0	Writing this bit to a 1 clears the LBIST_DONE and LBIST_PASSED status bits. These bits are also automatically updated after LBIST is executed. 0 = No action 1 = Clear LBIST_DONE and LBIST_PASSED status bits
ABIST_PASSED	3	R	0x0	ABIST passed. Valid after ABIST completes 0 = ABIST fail (if ABIST_DONE = 1) 1 = ABIST passed
ABIST_DONE	2	R	0x0	ABIST complete 0 = ABIST has not completed 1 = ABIST completed
Reserved	1	R	0x0	-
CLEAR_ABIST_STATUS	0	W1S	0x0	Writing this bit to a 1 clears the ABIST_DONE and ABIST_PASSED status bits. These bits are also automatically updated after ABIST is executed. 0 = No action 1 = Clear ABIST_DONE and ABIST_PASSED status bits

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7.139 SLOT_MON_DCDC - 0x230

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
MON_DCDC2_SLOT	6:4	R	0x0	MON_DCDC2 slot monitor *Note*: Rails started in the same slot time have the same order i. 0 = DCDC2 rail is powered-down 1, 2, 3, 4, 5: DCDC2 rail is powered-up with order I in the rail power-up sequence.
Reserved	3	R	0x0	-
MON_DCDC1_SLOT	2:0	R	0x0	MON_DCDC1 slot monitor *Note*: Rails started in the same slot time have the same order i. DCDC1 should have i = 1 when it is in power-up since it is started first. 0 = DCDC1 rail is powered-down 1, 2, 3, 4, 5: DCDC1 rail is powered-up with order I in the rail power-up sequence.

7.140 SLOT_MON_LDO12 - 0x231

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
MON_LDO2_SLOT	6:4	R	0x0	MON_LDO2 slot monitor *Note*: Rails started in the same slot time have the same order i. 0 = LDO2 rail is powered-down 1, 2, 3, 4, 5: LDO2 rail is powered-up with order I in the rail power-up sequence.
Reserved	3	R	0x0	-
MON_LDO1_SLOT	2:0	R	0x0	MON_LDO1 slot monitor *Note*: Rails started in the same slot time have the same order i. 0 = LDO1 rail is powered-down 1, 2, 3, 4, 5: LDO1 rail is powered-up with order I in the rail power-up sequence

7.141 SLOT_MON_LDO34 - 0x232

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	-
MON_LDO4_SLOT	6:4	R	0x0	MON_LDO4 slot monitor *Note*: Rails started in the same slot time have the same order i. 0 = LDO4 rail is powered-down 1, 2, 3, 4, 5: LDO4 rail is powered-up with order I in the rail power-up sequence.
Reserved	3	R	0x0	-
MON_LDO3_SLOT	2:0	R	0x0	MON_LDO3 slot monitor *Note*: Rails started in the same slot time have the same order i. 0 = LDO3 rail is powered-down 1, 2, 3, 4, 5: LDO3 rail is powered-up with order I in the rail power-up sequence

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7.142 MON_SLOT1_TIME - 0x233

Name	Bit	Type	Default	Description
MON_SLOT1_TIME	7:0	R	0x0	Measurement of the OPT_SLOT1_TIME (which is 0,1,2,5ms) done by a monitor independent from the power sequencer. MON_SLOT1_TIME[7:0] provides a value based on a 100µs period. Therefore the measured time in µs is: MON_SLOT1_TIME[7:0] ×100µs. The 100µs period has a variability of ±25% due to the 17.6MHz oscillator. This register is meaningful only if read when all the enable signals of the enabled rails are 1 (DCDC1_ENABLED, DCDC2_ENABLED, LDO1_ENABLED, LDO2_ENABLED, LDO3_ENABLED, LDO4_ENABLED).

7.143 MON_SLOT2_TIME - 0x234

Name	Bit	Type	Default	Description
MON_SLOT2_TIME	7:0	R	0x0	Measurement of the OPT_SLOT2_TIME (which is 0,1,2,5ms) done by a monitor independent from the power sequencer. MON_SLOT2_TIME[7:0] provides a value based on a 100µs period. Therefore the measured time in µs is: MON_SLOT2_TIME[7:0] ×100µs. The 100µs period has a variability of ±25% due to the 17.6MHz oscillator. This register is meaningful only if read when all the enable signals of the enabled rails are 1 (DCDC1_ENABLED, DCDC2_ENABLED, LDO1_ENABLED, LDO2_ENABLED, LDO3_ENABLED, LDO4_ENABLED).

7.144 MON_SLOT3_TIME - 0x235

Name	Bit	Type	Default	Description
MON_SLOT3_TIME	7:0	R	0x0	Measurement of the OPT_SLOT3_TIME (which is 0,1,2,5ms) done by a monitor independent from the power sequencer. MON_SLOT3_TIME[7:0] provides a value based on a 100µs period. Therefore the measured time in µs is: MON_SLOT3_TIME[7:0] ×100µs. The 100µs period has a variability of ±25% due to the 17.6MHz oscillator. This register is meaningful only if read when all the enable signals of the enabled rails are 1 (DCDC1_ENABLED, DCDC2_ENABLED, LDO1_ENABLED, LDO2_ENABLED, LDO3_ENABLED, LDO4_ENABLED).

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7.145 MON_TEST - 0x240

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x0	-
PARITY_REGS_FORCE_FAIL	0	RW	0x0	Used to force a fail of the R/W register parity check mechanism 0 = Do not create fail 1 = Create fail

7.146 SOFT_RESET - 0x280

Name	Bit	Type	Default	Description
SOFT_RESET	7:0	RW	0x0	SOFT reset Toggles RSTB low when the inverted value of the secure KEY value is written to this register. Other values are ignored. Timing follows the Case 1 fault handling. Read SECURE_KEY register 0x211. Take SECURE_KEY[7:0] = 1011 0001 as example, the inverted value (invert each bit from 1 to 0 and from 0 to 1) is Bit[7:0] = 0100 1110 to be written to SOFT_RESET register.

7.147 HARD_RESET - 0x281

Name	Bit	Type	Default	Description
HARD_RESET	7:0	RW	0x0	Hard reset Sequences rails and RSTB low when the nibble swapped value of the secure KEY value is written to this register. Other values are ignored. Timing follows the Case 2 fault handling. Read SECURE_KEY register 0x211. Take SECURE_KEY[7:0] = 1011 0001 as example, the nibble swapped value (swap Bit[7:4] with Bit[3:0]) is Bit[7:0] = 0001 1011 to be written to HARD_RESET register.

7.148 PMIC_RESET - 0x282

Name	Bit	Type	Default	Description
PMIC_RESET	7:0	RW	0x0	PMIC reset Issues a controlled shutdown, reset, and restart sequence when the bit reversed value of the secure KEY value is written to this register. Other values are ignored. Timing follows the EOT_ONLY shutdown sequence and all regulator outputs are disabled except LDO0. LDO0 remains enabled. Regulators execute their programmed output discharge times before restart. Registers are returned to their power-on reset value. OTP values are reloaded. BIST is re-executed. Regulator restart follows the WAKE-controlled PMIC enable timing. Read SECURE_KEY register 0x211. Take SECURE_KEY[7:0] = 1011 0001 as example, the bit reversed value (reverse the bit order from LSB to MSB) is Bit[7:0] = 1000 1101 to be written to PMIC_RESET register.

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7.149 RSTB_CNT - 0x283

Name	Bit	Type	Default	Description
RSTB_CNT_CLR	7	W1C	0x0	Clears the RSTB_CNT counter. The RSTB_CNT register can only be cleared one time per power cycle. If the RSTB_CNT register requires to be cleared more than one time, either a full power cycle or software execution of PMIC_RESET is required. 0 = Ignored 1 = Clear RSTB_CNT counter
RSTB_CNT	6:0	R	0x0	Increments on PMIC RSTB rising edge at startup. Reads back as 0x1 after first startup. Increments on each following RSTB startup. Does not roll over.

7.150 FUSE_STATUS - 0x339

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	-
FUSE_CRC_FAIL	4	R	0x0	Fuse CRC check status 0 = Pass 1 = Fail

Name	Bit	Type	Default	Description
Reserved	3:1	R	0x0	-
FUSE_CTRL_BUSY	0	R	0x0	Fuse controller state 0 = Fuse controller idle 1 = Fuse controller is reading or writing fuse array. SPI fuse shadow register write access disabled during this time.

7.151 FUSE_ID1 - 0x3C1

Name	Bit	Type	Default	Description
FUSE_ID	7:0	R	0x0	OTP Revision ID, MSByte Refer to datasheet addendum for the OTP reversion ID. Contact with Renesas for this register access.

7.152 FUSE_ID2 - 0x3D0

Name	Bit	Type	Default	Description
FUSE_ID	7:0	R	0x0	OTP Revision ID, LSByte Refer to datasheet addendum for the OTP reversion ID. Contact with Renesas for this register access.

8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

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9. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg #	MSL Rating	Carrier Type	Temp. Range
RAA2710844R6JHFP#HA0	RAA271084 4R6JHFP	48-LQFP-EP, 7 × 7 mm	Q48.7x7D	3	Reel, 1k	-40 to +125°C
RAA2710844R6JHNP#HA0	RAA271084 4R6JHNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844R62HNP#HA0	RAA271084 4R62HNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844211HNP#HAD	RAA271084 4211HNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844R6HHFP#HA0	RAA271084 4R6HHFP	48-LQFP-EP, 7 × 7 mm	Q48.7x7D	3	Reel, 1k	-40 to +125°C
RAA2710844R6HHNP#HA0	RAA271084 4R6HHNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844241HFP#HAD	RAA271084 4241HFP	48-LQFP-EP, 7 × 7 mm	Q48.7x7D	3	Reel, 1k	-40 to +125°C
RAA2710844R61HNP#HA0	RAA271084 4R61HNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA27108440F1HNP#HAD	RAA271084 40F1HNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844R6YHNP#HA0	RAA271084 4R6YHNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844R6YHFP#HA0	RAA271084 4R6YHFP	48-LQFP-EP, 7 × 7 mm	Q48.7x7D	3	Reel, 1k	-40 to +125°C
RAA2710844R65HNP#HA0	RAA271084 4R65HNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844R5KHNP#HA0	RAA271084 4R5KHNP	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844801HNP#HAB[4]	RAA271084 4801HNPB	48-SCQFN, 7 × 7 mm	L48.7x7N	3	Reel, 4k	-40 to +125°C
RAA2710844281HFP#HAD	RAA271084 4281HFP	48-LQFP-EP, 7 × 7 mm	Q48.7x7D	3	Reel, 1k	-40 to +125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For more information about Moisture Sensitivity Level (MSL), see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. The part number RAA2710844801HNP#HAB refers to RAA271084-B (ASIL-B).

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Table 27. Key Differences Between Parts

Part Number	System Safety Goal	Switching Frequency	Spread Spectrum	Watchdog	DCDC1 Overcurrent Protection	COREMON	AMUX	Package
RAA271084	ASIL-D	440kHz or 2.2MHz	Optional pseudo-random spread spectrum clock	Windowed QA or basic windowed watchdog	OC1 and OC2	Available	Available	LQFP or SCQFN
RAA271084-B	ASIL-B	2.2MHz	Pseudo-random with fixed 4 cycle dwell spread spectrum clock	Basic windowed watchdog	OC1	Not available	Not available	SCQFN

Table 28. RAA271084 Orderable Part Number's OTP Configuration

Part Number	OTP#[1]	DCDC1 f_{SW}	DCDC2 f_{SW}	LDO1 V_{OUT}	LDO2 V_{OUT}	LDO3 V_{OUT}	LDO3 Tk / Reg	LDO4 V_{OUT}	LDO4 Tk / Reg	VDDIO	Additional Settings
RAA2710844R6JHNP#HA0	0D.11	440kHz	440kHz	5.0V	5.0V	5.0V	Tracker	5.0V	Tracker	LDO1	SDO pin High-Z
RAA2710844R6JHFP#HA0	0D.11	440kHz	440kHz	5.0V	5.0V	5.0V	Tracker	5.0V	Tracker	LDO1	SDO pin High-Z
RAA2710844R62HNP#HA0	1C.10	440kHz	440kHz	3.3V	3.3V	5.0V	Tracker	5.0V	Tracker	LDO1	-
RAA2710844211HNP#HAD	21.10	440kHz	440kHz	3.3V	3.3V	5.0V	Tracker	5.0V	Regulator	LDO1	SDO pin High-Z
RAA2710844R6HHFP#HA0	0C.10	2.2MHz	2.2MHz	5.0V	5.0V	5.0V	Tracker	5.0V	Tracker	LDO1	-
RAA2710844R6HHNP#HA0	0C.10	2.2MHz	2.2MHz	5.0V	5.0V	5.0V	Tracker	5.0V	Tracker	LDO1	-
RAA2710844241HFP#HAD	24.10	2.2MHz	2.2MHz	5.0V	5.0V	5.0V	Tracker	5.0V	Tracker	LDO1	Enable SST
RAA2710844R61HNP#HA0	06.12	2.2MHz	2.2MHz	5.0V	5.0V	5.0V	Regulator	5.0V	Regulator	DCDC2	RSTb delay 5ms
RAA27108440F1HNP#HAD	0F.10	2.2MHz	2.2MHz	5.0V	5.0V	3.3V	Regulator	3.3V	Regulator	LDO1	-
RAA2710844R6YHNP#HA0	0E.10	2.2MHz	2.2MHz	5.0V	3.3V	5.0V	Regulator	5.0V	Tracker	LDO1	SLOT1/2/3 = 2ms; LDO1 = SLOT2; LDO2 = SLOT1; LDO3 = SLOT2; LDO4 = SLOT3;
RAA2710844R65HNP#HA0	19.10	2.2MHz	2.2MHz	5.0V	3.3V	3.3V	Regulator	3.3V	Regulator	LDO0	DCDC1 soft start rate 40us/step
RAA2710844R5KHNP#HA0	18.11	2.2MHz	2.2MHz	3.3V	3.3V	3.3V	Regulator	3.3V	Regulator	LDO1	-
RAA2710844281HFP#HAD	28.1	440KHz	2.2MHz	5.0V	5.0V	5.0V	Tracker	5.0V	Tracker	LDO1	Enable SPI CRC

1. For more information on OTP configuration options, please contact Renesas marketing or sales team.

Table 29. RAA271084-B Orderable Part Number's OTP Configuration

Part Number	OTP#[1]	DCDC1 f_{SW}	DCDC2 f_{SW}	LDO1 V_{OUT}	LDO2 V_{OUT}	LDO3 V_{OUT}	LDO3 Tk / Reg	LDO4 V_{OUT}	LDO4 Tk / Reg	VDDIO	Additional Settings
RAA2710844801HNP#HAB	80.10	2.2MHz	2.2MHz	5.0V	5.0V	5.0V	Tracker	5.0V	Tracker	LDO1	-

1. For more information on OTP configuration options, please contact Renesas marketing or sales team.

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10. Revision History

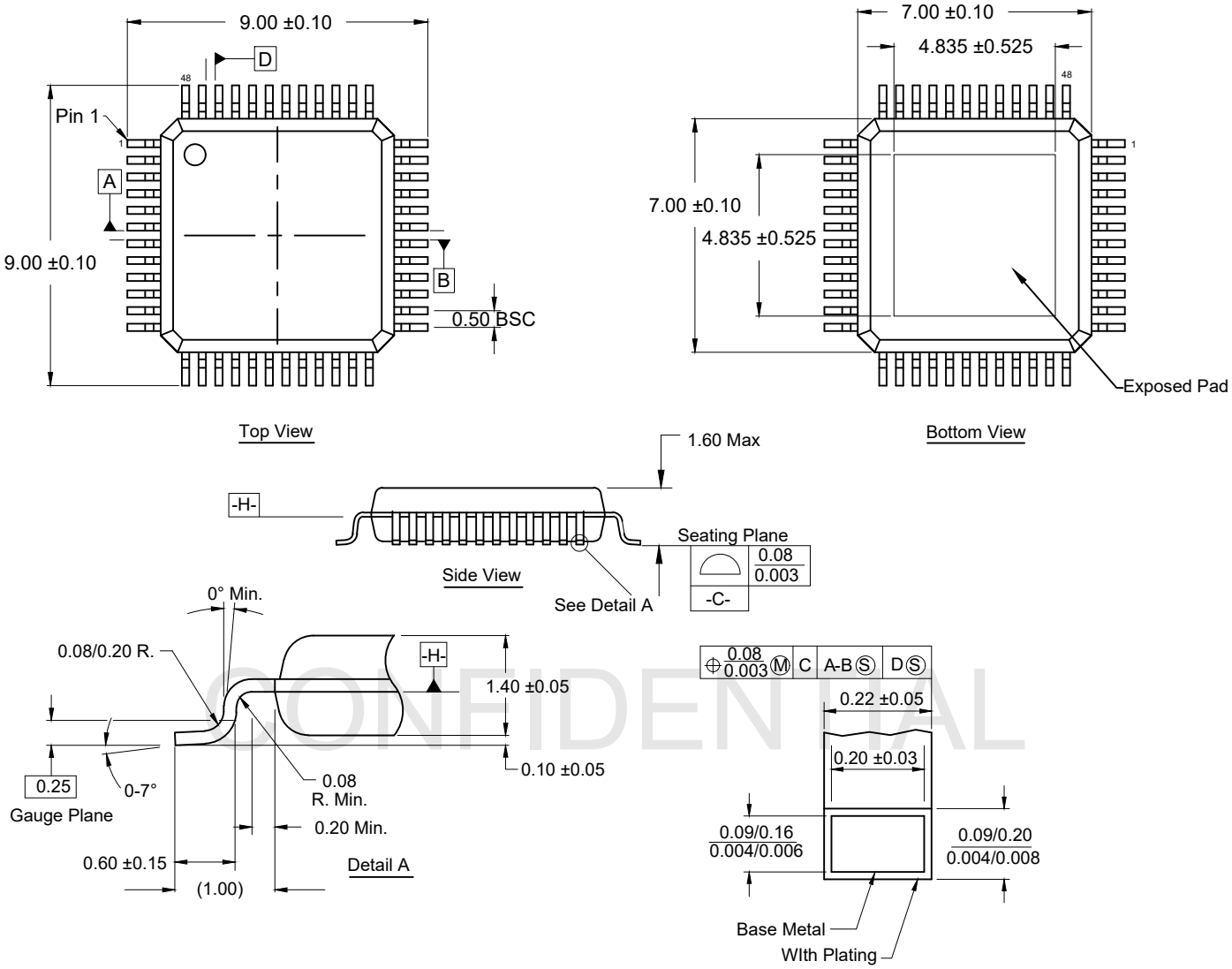
Revision	Date	Description
1.08	Oct 26, 2026	▪ Added recommendation for AMUX function usage in Section 5.3.11 Internal Signal Multiplexer function (AMUX). ▪ Updated register value description of DCDC_STATE - 0x08 Bits[1:0] • 1 = PWM, 2 = PFM. ▪ Updated register type of LDO_STATE - 0x09 Bits[1:0] LDO1_STATE to be R.
1.07	Mar 5, 2026	▪ Removed annotation [1] on page 1. ▪ Added DCDC1 fault response description related to shutdown delay t_{PREREG_OFF} at the end of Section 5.2.7. ▪ Updated Section 6.7 description about DCDC1 severe overvoltage protection and OV2_PD function. ▪ Updated POD Q48.7x7D to the latest version; changes are as follows: • Placed into the latest template. ▪ Updated POD L48.7x7N to the latest version; changes are as follows: • Added a width dimension of 0.25 mm on the Recommended Land Pattern.
1.06	Dec 12, 2025	▪ Added RAA2710844281HFP#HAD to ordering Information and Table 28. ▪ Updated POD.
1.05	Jun 6, 2025	▪ Updated RAA271084-B pin 23 to be NC2. ▪ Updated Table10 to include DCDC1 OC2 fault record, fault response cases, and INTB mask. ▪ Updated Register 0x03 to show 0x0C as default for rev.C ▪ Updated Register 0x30 Bits[4:0] to have type FRW as it is an OTP option. ▪ Updated Ordering Information table. ▪ Added New OTP configuration Tables 28 and 29 for 1084 and 1084-B.

Revision	Date	Description
1.04	Apr 22, 2025	▪ Added RAA271084-B information throughout. ▪ Updated DCDC1 OC2 options to be ASIL-D only. ▪ Updated Figure 1. Typical Application Diagram. ▪ Updated OPT_INTB_MASK_DCDC1_OC to OPT_INTB_MASK_DCDC1_OC1. ▪ Updated DCDC1_OC_FAULT_RECORD to DCDC1_OC1_FAULT_RECORD. ▪ Updated Table 10 to include OPT_SSPB_MASK_DCDC1_OC2 in DCDC1 SSPB Mask. ▪ Register 0x8F, 0x90, and 0x91 updated counter selection to 127 decimal. ▪ Removed ASIL-D only from register 0x207. ▪ Updated Register 0x143's Core monitor masks to ASIL-D only. ▪ Updated the key difference table to include the OC2 difference in DCDC1 overcurrent protection.
1.03	Jan 21, 2025	▪ Updated Features section. ▪ Removed OV2PD_BIST 0x228 and OV2PD_STATUS 0x229 registers. ▪ Added description of OV2_PD application.
1.02	Dec 19, 2024	▪ Updated Pin 10 description. ▪ Updated Table 18.
1.01	Dec 9, 2024	▪ Removed SPI burst write related descriptions. ▪ Changed register 0x207 Bit[1:0] to be Reserved as 0x0. ▪ Updated register bit value 0x00 as 0x0 for consistency. ▪ Added register 0x08, 0x09, and 0x339 tables. ▪ Added notes for register 0x3C1 and 0x3D0. ▪ Added pin LDOVO3 and LDOVO4 to abs max ▪ Added VIN2, FB1, LDOIN1/2 and LDO3/4 pins pulse voltage spec as 7.5V <100us to abs max. ▪ Added additional notes for SSPB, RSTB, INTB, and OV2_PD pins in the Pin Descriptions table. ▪ Added additional explanation for existing DeepSTOP and PSTBY modes with WAKE2 pin edge trigger. ▪ Added Min/Max values for the LDO0 Thermal Shutdown (TSD_REG) spec. ▪ Added TSD_REG Hysteresis spec. ▪ Added min/max values and updated typical value from 1.68 to 2.13 for the High-Side Source Resistance spec. ▪ Added min/max values for the High-Side Sink Resistance and Low-Side Source Resistance specs. ▪ Added min/max values and updated the typical value from 0.6 to 0.8 for the Low-Side Sink Resistance spec. ▪ Updated DCDC1 Output Voltage min/max values from 5.415 to 5.60 and 5.985 to 5.77. ▪ Updated the LDO[1-2] and LDO[3-4] Output Voltage min/max values as follows: • Changed 4.9 to 4.925 and 5.1 to 5.075. • Changed 3.23 to 3.2505 and 3.37 to 3.3495. ▪ Added min value for the Output Pull-Down Resistance spec. ▪ Added min/max values for the LDO3/4 Thermal Shutdown (TSD_LDO34) spec. ▪ Added the TSD_LDO34 Hysteresis spec. ▪ Updated min/max values from 151 to 150 and 169 to 170 for the FuSa Thermal Shutdown (TSD_FuSa). ▪ Added the TSD_FuSa Hysteresis spec.
1.00	Oct 4, 2024	Initial release

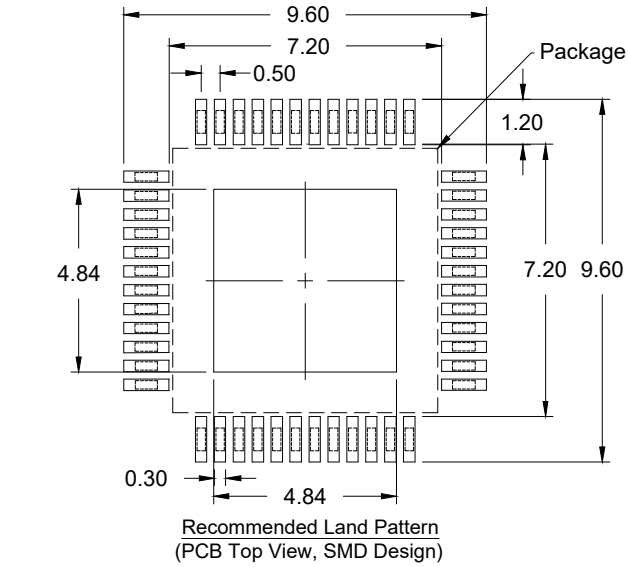
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Package Outline Drawing

Q48.7x7D
PL0048AA
48 LQFP 7.0 x 7.0 x 1.6 mm Body, 0.5 mm Pitch
Rev 01, Feb 20, 2026



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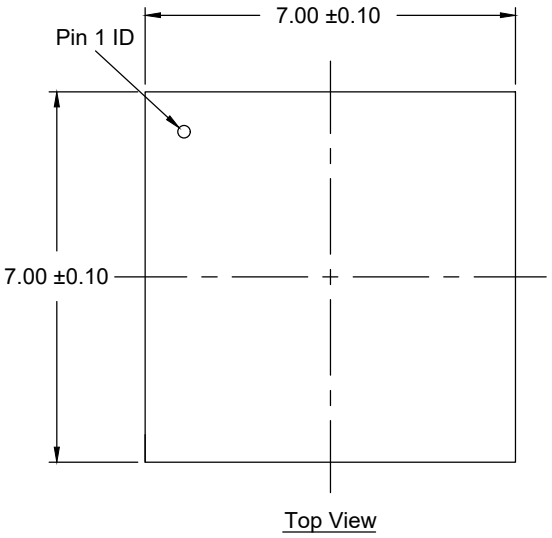
Notes:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982
3. Lead to lead width and length to be determined at seating plane. -C-
4. Body width and length to be determined at datum plane. -H-
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.025mm (0.10 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion not cause the lead width to exceed the maximum b dimension by more that 0.08mm (0.003 inch)
7. Package outline compliant to JEDEC MS-026BBC.

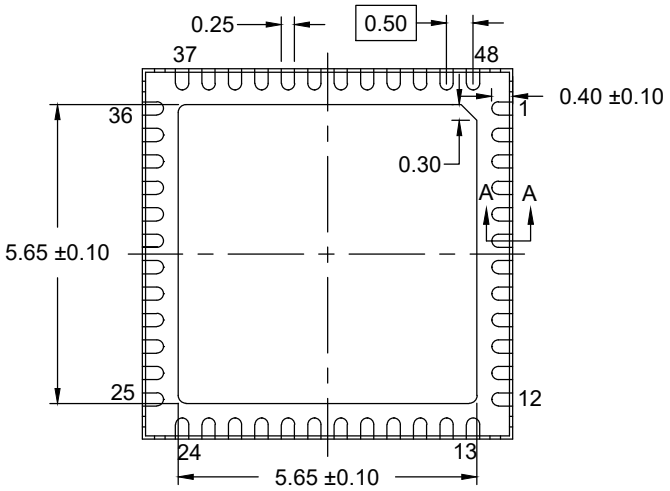
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Package Outline Drawing

QV0048AG
L48.7x7N
48-SCQFN 7.0 x 7.0 x 0.9 mm Body, 0.5 mm Pitch (ePad:5.65 x5.65 mm)
Rev04, Jan 5, 2026

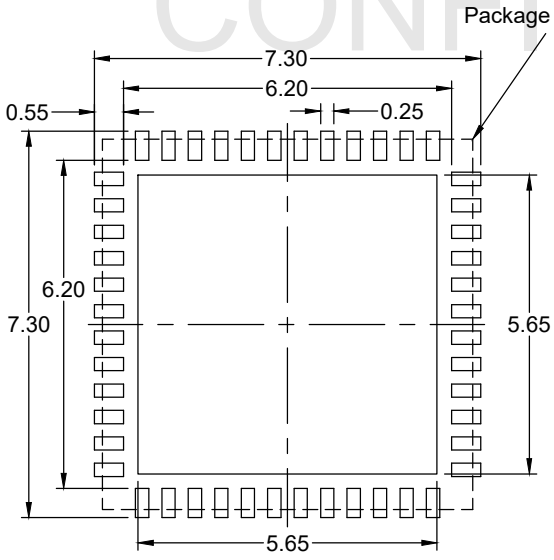


Top View

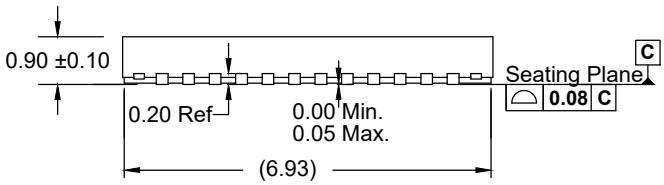


Bottom View

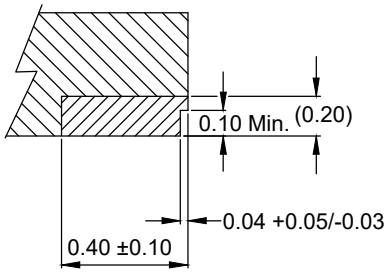
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Typical Recommended Land Pattern



Side View



Section : A-A
Scale : NTS

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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