RAA271005/RAA271005L

General Purpose IC for Power Management Applications

The RAA271005 is a general-purpose Power Management IC (PMIC) suitable for R-Car SoC series.

The RAA271005/RAA271005L contains five DC/DC switching regulators and six low-drop out linear regulators (LDO). Buck1 of RAA271005 provides 12A output current and RAA271005L provides up to 6A. DCDC5 (Buck5) switching regulator can be configured to work in buck mode or can be configured as a boost. The RAA271005/RAA271005L PMIC supports low power operation where three of the switching regulators (Buck3 to Buck5) have been optimized to consume low quiescent current.

RAA271005/RAA271005L supports up to ASIL D functional safety and includes an independent reference for monitoring of the output voltages, dual internal temperature monitors, challenge response watchdog timer, SoC and MCU error pin monitors, reset generator, a dedicated safety-control state machine, and safety shutdown path. An integrated 12-bit ADC monitors all input rails, output rails, internal temperature, and includes additional inputs to monitor external analog sources.

RAA271005/RAA271005L is available in a 6×11 BGA package, with 0.65mm pitch. The device is offered as AEC-Q100 Grade 1 operation, supporting an ambient temperature range of -40°C to 125°C.

Applications

- Automotive Gateway Systems
- Automotive Vision Systems
- Automotive LIDAR Systems
- Ideal power supply for Renesas R-Car S4 and other SoCs

Features

- Input range: 2.7V to 5.5V
- Five high-efficiency switching regulators with adjustable output voltages
  - RAA271005 Buck1: I_{OUT} = 12A; V_{OUT} from 0.3V to 3.3V
  - RAA271005L Buck1: I_{OUT} = 6A; V_{OUT} from 0.3V to 3.3V
  - 2.5A (Buck2); V_{OUT} from 0.3V to 3.3V
  - 2.5A (Buck3 to Buck5); V_{OUT} from 0.5V to 3.3V
    - Merged-mode (Buck3 and Buck4); 2 × 2.5A = 5A output
    - Buck5 can operate as asynchronous boost up to 5.0V V_{OUT}
  - 6 Linear Drop Out (LDO) Regulators
    - 4 x 75mA; V_{OUT} = 1.8V or 3.3V
    - 2 x 500mA; V_{OUT} = 0.6V to 3.3V
- 12-bit Analog-to-Digital converter for monitoring with programmable OV/UV thresholds.
- Programmable power sequence. Fully supports S4 and other SoC sequence requirements.
- Low-Iq Deep Stop / Always On (AWO) Mode
- Suspend-to-RAM / DDR-backup Mode
- Supports R-Car SoC Activation
- Q&A Watchdog Timer
- Configurable through I^2C or SPI interface
- SoC and MCU error pin monitor
- AEC-Q100 qualified (grade 1)

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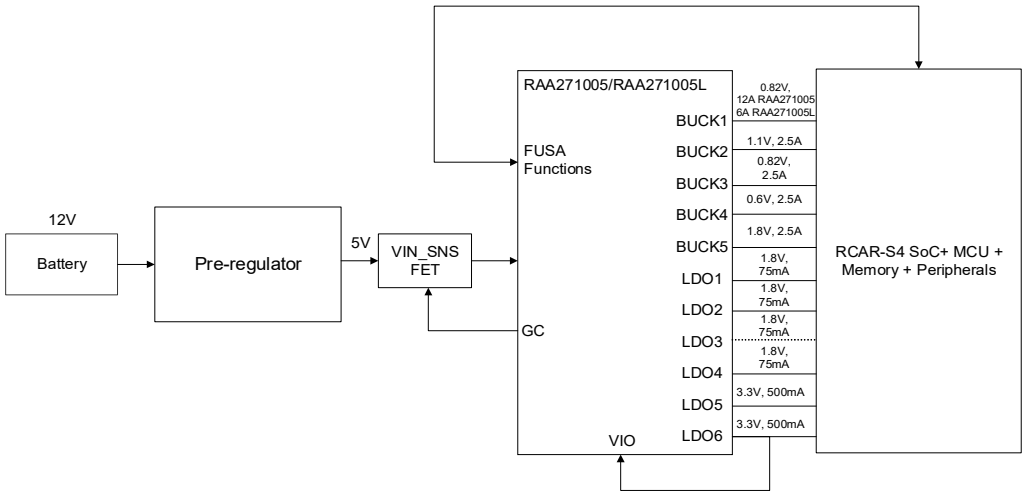


Figure 1. Typical Application Block Diagram

Contents

1. Overview . . . 14

1.1 Typical Application Diagrams . . . 14

1.2 Block Diagram . . . 16

2. Pin Information . . . 17

2.1 Pin Assignments . . . 17

2.2 Pin Descriptions . . . 17

2.2.1 I/O Pin Configurations . . . 20

2.2.2 I/O Pin Descriptions . . . 20

3. Specifications . . . 21

3.1 Absolute Maximum Ratings . . . 21

3.2 Recommended Operating Conditions . . . 22

3.3 Thermal Information . . . 22

3.4 Electrical Specifications . . . 22

4. Applications Section . . . 33

4.1 Power Sequencing . . . 33

4.2 Functional Safety . . . 34

4.3 Digital Interfaces . . . 34

4.4 SPI Serial Interface . . . 34

4.4.1 SPI Data Protocol . . . 34

4.4.2 SPI Configuration . . . 36

4.4.3 SPI Timing . . . 37

4.5 I^2C Interface . . . 38

4.5.1 I^2C Bus Operation . . . 38

4.5.2 I^2C Timing . . . 39

4.6 Theory of Operation Overview . . . 41

4.6.1 Buck2 DCM Operation Overview . . . 41

4.6.2 Buck[3-5] PFM Operation Overview . . . 42

4.7 Recommended External Components and Considerations . . . 43

4.8 Layout Guidelines . . . 44

4.8.1 Laying out Buck[1-5] . . . 44

4.8.2 All Other Components Placement and PCB Routing . . . 47

4.8.3 PCB Thermal Considerations . . . 47

5. Power Management Features . . . 48

5.1 Buck Regulators, Buck[1-5] . . . 48

5.1.1 Buck Output Voltage Selection . . . 48

5.1.2 Buck Regulator Startup Ramp Rate . . . 49

5.1.3 Buck Dynamic Voltage Scaling . . . 49

5.1.4 Buck Regulator Protection Features . . . 50

5.1.5 DCDC5/Buck5 Configured as Boost . . . 52

5.1.6 Buck3 and Buck4 Merged Mode for 5A Buck . . . 52

5.2 LDO Regulators, LDO[1-6] . . . 52

5.2.1 LDO Output Voltage, LDO[1-4] . . . 52

5.2.2 LDO Output Voltage, LDO[5-6] . . . 52

5.2.3 LDO Startup Ramp Rate . . . 53

5.2.4 LDO Protection Features . . . 53

5.3 Discharge and Discharge Detect Feature . . . 54

5.4 Fault Reactions . . . 56
5.5 Regulation Interrupts . . . 56
5.6 Power Grouping and Power State Transitions . . . 59
5.6.1 Power Grouping . . . 59
5.6.2 Power Flow Diagrams . . . 60
5.6.3 Power State Transitions (R-Car S4 SoC Example) . . . 61
5.7 Overvoltage Protection Gate Control . . . 67
5.8 RAA271005/RAA271005L GPIO . . . 69
5.8.1 General Purpose IOs . . . 69
5.8.2 Power-Good Indicator (IO6, IO13) . . . 69
5.8.3 Interrupt of Regulation . . . 70
5.8.4 DVS pin . . . 70
5.8.5 Following EN . . . 70
5.9 Regulation Hiccup Feature . . . 70
5.10 Lock Release/OTP Retry ADC3 Pin Option. . . . 71
5.11 Invalid Deep Stop . . . 71

6. Protection Features . . . 72

6.1 Monitoring ADC . . . 72
6.1.1 Monitoring ADC Inputs . . . 73
6.1.2 External Differential Measurement . . . 74
6.1.3 Monitoring ADC Input Range . . . 74
6.1.4 Monitoring System IIR Filter . . . 75
6.1.5 Sampling Rate . . . 76
6.1.6 ADC Data Format . . . 76
6.2 Overvoltage (OV) and Undervoltage (UV) Monitoring . . . 76
6.3 Over-Temperature Warning and Shutdown . . . 76
6.4 Watchdog Timer (WDT) . . . 77
6.4.1 16-Question Watchdog Timer (QA16WDT) . . . 78
6.4.2 4-Question Watchdog Timer (QA4WDT) . . . 78
6.4.3 Windowed Watchdog Timer (WWDT) . . . 79
6.5 Fault Reactions During Cold-Start and Deep Stop . . . 79
6.6 Protection Interrupt Pin (IRQ#) . . . 79

7. Register Map . . . 80

7.1 OTP Programmability . . . 80
7.2 Regulation Register Descriptions - Defaults . . . 80
7.2.1 0x000 - IO_PAGE_REGU . . . 80
7.2.2 0x001 - IO_CHIPNAME_REGU . . . 80
7.2.3 0x002 - IO_CHIPVERSION_REGU . . . 80
7.2.4 0x003 - IO_DIEID3_REGU . . . 80
7.2.5 0x004 - IO_DIEID2_REGU . . . 80
7.2.6 0x005 - IO_DIEID1_REGU . . . 81
7.2.7 0x006 - IO_DIEID0_REGU . . . 81
7.2.8 0x00A - OTP_VERSION_REGU . . . 81
7.2.9 0x022 - IO_MODECTRL_REGU (OTP) . . . 81
7.2.10 0x023 - IO_MODECTRL2_REGU (OTP) . . . 82
7.2.11 0x02D - CHIPTSTATE_BUCK_PGOOD . . . 82
7.2.12 0x02E - CHIPTSTATE_LDO_PGOOD . . . 82
7.2.13 0x030 - FLT_MASK_OTP (OTP) . . . 83

7.2.14 0x031 - FLT_MASK_TEMP (OTP) . . . 83
7.2.15 0x032 - FLT_MASK_BUCK1 (OTP) . . . 84
7.2.16 0x033 - FLT_MASK_BUCK2 (OTP) . . . 84
7.2.17 0x034 - FLT_MASK_BUCK3 (OTP) . . . 85
7.2.18 0x035 - FLT_MASK_BUCK4 (OTP) . . . 85
7.2.19 0x036 - FLT_MASK_BUCK5 (OTP) . . . 86
7.2.20 0x037 - FLT_MASK_LDO (OTP) . . . 86
7.2.21 0x038 - FLT_MASK_IF (OTP) . . . 87
7.2.22 0x040 - FLT_RECORD_OTP . . . 87
7.2.23 0x041 - FLT_RECORD_TEMP . . . 88
7.2.24 0x042 - FLT_RECORD_BUCK1 . . . 88
7.2.25 0x043 - FLT_RECORD_BUCK2 . . . 89
7.2.26 0x044 - FLT_RECORD_BUCK3 . . . 89
7.2.27 0x045 - FLT_RECORD_BUCK4 . . . 90
7.2.28 0x046 - FLT_RECORD_BUCK5 . . . 91
7.2.29 0x047 - FLT_RECORD_LDO . . . 91
7.2.30 0x048 - FLT_RECORD_IF . . . 92
7.2.31 0x049 - FLT_RECORD_LDO_DISC_DET . . . 92
7.2.32 0x04C – IO_GP3CFGMSB . . . 93
7.2.33 0x04D – IO_GP3CFGLSB . . . 93
7.2.34 0x056 - IO_GPIO_DATAIN . . . 93
7.2.35 0x057 - IO_GPIO_DATAOUT . . . 94
7.2.36 0x05C - IO_GPIO_0_DATAOUT_UP_DLY . . . 94
7.2.37 0x05D - IO_GPIO_0_DATAOUT_DN_DLY . . . 94
7.2.38 0x05E - IO_GPIO_1_DATAOUT_UP_DLY . . . 94
7.2.39 0x05F - IO_GPIO_1_DATAOUT_DN_DLY . . . 94
7.2.40 0x060 - IO_GPIO_2_DATAOUT_UP_DLY . . . 94
7.2.41 0x061 - IO_GPIO_2_DATAOUT_DN_DLY . . . 94
7.2.42 0x062 - IO_GPIO_3_DATAOUT_UP_DLY . . . 94
7.2.43 0x63 - IO_GPIO_3_DATAOUT_DN_DLY . . . 95
7.2.44 0x06F - LOCK_OUT_CFG . . . 95
7.2.45 0x070 - BUCK1_DVS0CFG1 (OTP) . . . 95
7.2.46 0x071 - BUCK1_DVS0CFG0 (OTP) . . . 95
7.2.47 0x072 - BUCK1_DVS1CFG1 (OTP) . . . 95
7.2.48 0x073 - BUCK1_DVS1CFG0 (OTP) . . . 96
7.2.49 0x075 - BUCK1_DVSSEL (OTP) . . . 96
7.2.50 0x076 - BUCK1_EN_DLY (OTP) . . . 96
7.2.51 0x077 - BUCK1_SHUTDN_DLY (OTP) . . . 96
7.2.52 0x080 - BUCK2_DVS0CFG1 (OTP) . . . 96
7.2.53 0x081 - BUCK2_DVS0CFG0 (OTP) . . . 97
7.2.54 0x086 - BUCK2_EN_DLY (OTP) . . . 97
7.2.55 0x087 - BUCK2_SHUTDN_DLY (OTP) . . . 97
7.2.56 0x090 - BUCK3_DVS0CFG1 (OTP) . . . 97
7.2.57 0x091 - BUCK3_DVS0CFG0 (OTP) . . . 97
7.2.58 0x096 - BUCK3_EN_DLY (OTP) . . . 98
7.2.59 0x097 - BUCK3_SHUTDN_DLY (OTP) . . . 98
7.2.60 0x0A0 - BUCK4_DVS0CFG1 (OTP) . . . 98
7.2.61 0x0A1 - BUCK4_DVS0CFG0 (OTP) . . . 98
7.2.62 0x0A6 - BUCK4_EN_DLY (OTP) . . . 98

7.2.63 0x0A7 - BUCK4_SHUTDN_DLY (OTP) . . . 98
7.2.64 0x0B0 - BUCK5_DVS0CFG1 (OTP) . . . 99
7.2.65 0x0B1 - BUCK5_DVS0CFG0 (OTP) . . . 99
7.2.66 0x0B6 - BUCK5_EN_DLY (OTP) . . . 99
7.2.67 0x0B7 - BUCK5_SHUTDN_DLY (OTP) . . . 99
7.2.68 0x0C3 - LDO1_EN_DLY (OTP) . . . 99
7.2.69 0x0C4 - LDO1_SHUTDN_DLY (OTP) . . . 99
7.2.70 0x0C5 - LDO2_EN_DLY (OTP) . . . 100
7.2.71 0x0C6 - LDO2_SHUTDN_DLY (OTP) . . . 100
7.2.72 0x0C7 - LDO3_EN_DLY (OTP) . . . 100
7.2.73 0x0C8 - LDO3_SHUTDN_DLY (OTP) . . . 100
7.2.74 0x0C9 - LDO4_EN_DLY (OTP) . . . 100
7.2.75 0x0CA - LDO4_SHUTDN_DLY (OTP) . . . 100
7.2.76 0x0CB - LDO5_EN_DLY (OTP) . . . 100
7.2.77 0x0CC - LDO5_SHUTDN_DLY (OTP) . . . 100
7.2.78 0x0CD - LDO6_EN_DLY (OTP) . . . 101
7.2.79 0x0CE - LDO6_SHUTDN_DLY (OTP) . . . 101
7.2.80 0x0CF - HICCUP_RESTRT_DLY (OTP) . . . 101
7.2.81 0x0D0 - HICCUP_CNT_LIM (OTP) . . . 101
7.2.82 0x0D1 - DISC_DET_CFG (OTP) . . . 101
7.2.83 0x0D2 - BUCK_DISC_VTH0 (OTP) . . . 102
7.2.84 0x0D3 - BUCK_DISC_VTH1 (OTP) . . . 102
7.2.85 0x0D4 - LDO_DISC_VTH0 (OTP) . . . 103
7.2.86 0x0D5 - LDO_DISC_VTH1 (OTP) . . . 103
7.2.87 0x0D6 – MISC_CTRL_REGU (OTP) . . . 103
7.2.88 0x125 – IO_PD (OTP) . . . 104
7.2.89 0x176 - BACKUP_CFG (OTP) . . . 104
7.2.90 0x223 - I_IO_INTERNALVERSION_REGU (OTP) . . . 104
7.3 Protection Register Descriptions - Defaults . . . 104
7.3.1 0x000 - IO_PAGE . . . 104
7.3.2 0x001 - IO_CHIPNAME . . . 104
7.3.3 0x002 - IO_CHIPVERSION . . . 105
7.3.4 0x003 - IO_DIEID3 . . . 105
7.3.5 0x004 - IO_DIEID2 . . . 105
7.3.6 0x005 - IO_DIEID1 . . . 105
7.3.7 0x006 - IO_DIEID0 . . . 105
7.3.8 0x007 - IO_CHIPSTATE . . . 106
7.3.9 0x008 - FUSA_CTRL_1_A . . . 106
7.3.10 0x009 - FUSA_CTRL_2 . . . 106
7.3.11 0x00A - FUSA_CTRL_3 . . . 106
7.3.12 0x00B - FUSA_CTRL_4 . . . 107
7.3.13 0x00C - FUSA_CTRL_5 . . . 107
7.3.14 0x00D - FUSA_CHK_CVM1 . . . 108
7.3.15 0x00E - FUSA_STATUS_CVM1 . . . 108
7.3.16 0x00F - FUSA_STATUS_CVM2 . . . 109
7.3.17 0x010 - FUSA_STATUS_1 . . . 109
7.3.18 0x011 - FUSA_STATUS_2 . . . 110
7.3.19 0x012 - FUSA_STATUS_2A . . . 110
7.3.20 0x013 - FUSA_STATUS_3 . . . 110

7.3.21 0x014 - FUSA_STATUS_4 . . . 110
7.3.22 0x015 - FUSA_SOC_CHK_1 . . . 111
7.3.23 0x016 - IO_HOST_MSGCNT . . . 111
7.3.24 0x017 - CLK_CNT_1 . . . 111
7.3.25 0x018 - CLK_CNT_2 . . . 111
7.3.26 0x019 - FLT_RECORD_A . . . 112
7.3.27 0x01A - FLT_RECORD_B . . . 113
7.3.28 0x01B - FLT_RECORD_GND_AVIN . . . 113
7.3.29 0x01C - FLT_RECORD_BG_Temp . . . 114
7.3.30 0x01D - FLT_RECORD_IntLDOs . . . 115
7.3.31 0x01E - FLT_RECORD_ExtLDOs . . . 116
7.3.32 0x01F - FLT_RECORD_BUCKS_B . . . 116
7.3.33 0x020 - FLT_RECORD_BUCKS_A . . . 117
7.3.34 0x021 - FLT_RECORD_ExtINPs_7_0 . . . 118
7.3.35 0x028 - OTP_RWADDR . . . 118
7.3.36 0x02A - OTP_FLT_RECORD . . . 119
7.3.37 0x02D - ADCMON_COPY_SAMPLE . . . 120
7.3.38 0x02E - ADCMON_COPY_DATA_MSB . . . 122
7.3.39 0x02F - ADCMON_COPY_DATA_LSB . . . 122
7.3.40 0x030 - ADCMON_DATAMSB_Offset . . . 122
7.3.41 0x031 - ADCMON_DATALSB_Offset . . . 122
7.3.42 0x032 - ADCMON_DATAMSB_Temp2 . . . 122
7.3.43 0x033 - ADCMON_DATALSB_Temp2 . . . 122
7.3.44 0x034 - ADCMON_DATAMSB_Temp3 . . . 122
7.3.45 0x035 - ADCMON_DATALSB_Temp3 . . . 122
7.3.46 0x036 - ADCMON_DATAMSB_BGRegu . . . 123
7.3.47 0x037 - ADCMON_DATALSB_BGRegu . . . 123
7.3.48 0x038 - ADCMON_DATAMSB_PGNDRegu . . . 123
7.3.49 0x039 - ADCMON_DATALSB_PGNDRegu . . . 123
7.3.50 0x03A - IntLDORegu_0_ADCMON_DATAMSB_IntLDORegu . . . 123
7.3.51 0x03B - IntLDORegu_0_ADCMON_DATALSB_IntLDORegu . . . 123
7.3.52 0x03C - IntLDORegu_1_ADCMON_DATAMSB_IntLDORegu . . . 123
7.3.53 0x03D - IntLDORegu_1_ADCMON_DATALSB_IntLDORegu . . . 123
7.3.54 0x03E - IntLDORegu_2_ADCMON_DATAMSB_IntLDORegu . . . 124
7.3.55 0x03F - IntLDORegu_2_ADCMON_DATALSB_IntLDORegu . . . 124
7.3.56 0x040 - IntLDORegu_3_ADCMON_DATAMSB_IntLDORegu . . . 124
7.3.57 0x041 - IntLDORegu_3_ADCMON_DATALSB_IntLDORegu . . . 124
7.3.58 0x042 - IntLDORegu_4_ADCMON_DATAMSB_IntLDORegu . . . 124
7.3.59 0x043 - IntLDORegu_4_ADCMON_DATALSB_IntLDORegu . . . 124
7.3.60 0x044 - IntLDORegu_5_ADCMON_DATAMSB_IntLDORegu . . . 124
7.3.61 0x045 - IntLDORegu_5_ADCMON_DATALSB_IntLDORegu . . . 124
7.3.62 0x046 - IntLDOProt_0_ADCMON_DATAMSB_IntLDOProt . . . 125
7.3.63 0x047 - IntLDOProt_0_ADCMON_DATALSB_IntLDOProt . . . 125
7.3.64 0x048 - IntLDOProt_1_ADCMON_DATAMSB_IntLDOProt . . . 125
7.3.65 0x049 - IntLDOProt_1_ADCMON_DATALSB_IntLDOProt . . . 125
7.3.66 0x04A - ADCMON_DATAMSB_AVIN1 . . . 125
7.3.67 0x04B - ADCMON_DATALSB_AVIN1 . . . 125
7.3.68 0x04C - ADCMON_DATAMSB_AVIN2 . . . 125
7.3.69 0x04D - ADCMON_DATALSB_AVIN2 . . . 126

7.3.70 0x04E - extLDO_0_ADCMON_DATAMSB_ExtLDO . . . 126
7.3.71 0x04F - extLDO_0_ADCMON_DATALSB_ExtLDO . . . 126
7.3.72 0x050 - extLDO_1_ADCMON_DATAMSB_ExtLDO . . . 126
7.3.73 0x051 - extLDO_1_ADCMON_DATALSB_ExtLDO . . . 126
7.3.74 0x052 - extLDO_2_ADCMON_DATAMSB_ExtLDO . . . 126
7.3.75 0x053 - extLDO_2_ADCMON_DATALSB_ExtLDO . . . 126
7.3.76 0x054 - extLDO_3_ADCMON_DATAMSB_ExtLDO . . . 126
7.3.77 0x055 - extLDO_3_ADCMON_DATALSB_ExtLDO . . . 127
7.3.78 0x056 - extLDO_4_ADCMON_DATAMSB_ExtLDO . . . 127
7.3.79 0x057 - extLDO_4_ADCMON_DATALSB_ExtLDO . . . 127
7.3.80 0x058 - extLDO_5_ADCMON_DATAMSB_ExtLDO . . . 127
7.3.81 0x059 - extLDO_5_ADCMON_DATALSB_ExtLDO . . . 127
7.3.82 0x05A - PVIN_0_ADCMON_DATAMSB_PVIN . . . 127
7.3.83 0x05B - PVIN_0_ADCMON_DATALSB_PVIN . . . 127
7.3.84 0x05C - PVIN_1_ADCMON_DATAMSB_PVIN . . . 127
7.3.85 0x05D - PVIN_1_ADCMON_DATALSB_PVIN . . . 128
7.3.86 0x05E - PVIN_2_ADCMON_DATAMSB_PVIN . . . 128
7.3.87 0x05F - PVIN_2_ADCMON_DATALSB_PVIN . . . 128
7.3.88 0x060 - PVIN_3_ADCMON_DATAMSB_PVIN . . . 128
7.3.89 0x061 - PVIN_3_ADCMON_DATALSB_PVIN . . . 128
7.3.90 0x062 - PVIN_4_ADCMON_DATAMSB_PVIN . . . 128
7.3.91 0x063 - PVIN_4_ADCMON_DATALSB_PVIN . . . 128
7.3.92 0x064 - VOUT_0_ADCMON_DATAMSB_VOUT . . . 128
7.3.93 0x065 - VOUT_0_ADCMON_DATALSB_VOUT . . . 129
7.3.94 0x066 - VOUT_1_ADCMON_DATAMSB_VOUT . . . 129
7.3.95 0x067 - VOUT_1_ADCMON_DATALSB_VOUT . . . 129
7.3.96 0x068 - VOUT_2_ADCMON_DATAMSB_VOUT . . . 129
7.3.97 0x069 - VOUT_2_ADCMON_DATALSB_VOUT . . . 129
7.3.98 0x06A - VOUT_3_ADCMON_DATAMSB_VOUT . . . 129
7.3.99 0x06B - VOUT_3_ADCMON_DATALSB_VOUT . . . 129
7.3.100 0x06C - VOUT_4_ADCMON_DATAMSB_VOUT . . . 129
7.3.101 0x06D - VOUT_4_ADCMON_DATALSB_VOUT . . . 130
7.3.102 0x06E - ADCMON_DATAMSB_SPARE_0 . . . 130
7.3.103 0x06F - ADCMON_DATALSB_SPARE_0 . . . 130
7.3.104 0x070 - ADCMON_DATAMSB_Temp4 . . . 130
7.3.105 0x071 - ADCMON_DATALSB_Temp4 . . . 130
7.3.106 0x072 - ADCMON_DATAMSB_SPARE_1 . . . 130
7.3.107 0x073 - ADCMON_DATALSB_SPARE_1 . . . 130
7.3.108 0x074 - EXT_0_ADCMON_DATAMSB_EXT . . . 130
7.3.109 0x075 - EXT_0_ADCMON_DATALSB_EXT . . . 131
7.3.110 0x076 - EXT_1_ADCMON_DATAMSB_EXT . . . 131
7.3.111 0x077 - EXT_1_ADCMON_DATALSB_EXT . . . 131
7.3.112 0x078 - EXT_2_ADCMON_DATAMSB_EXT . . . 131
7.3.113 0x079 - EXT_2_ADCMON_DATALSB_EXT . . . 131
7.3.114 0x07A - EXT_3_ADCMON_DATAMSB_EXT . . . 131
7.3.115 0x07B - EXT_3_ADCMON_DATALSB_EXT . . . 131
7.3.116 0x07C - EXT_4_ADCMON_DATAMSB_EXT . . . 131
7.3.117 0x07D - EXT_4_ADCMON_DATALSB_EXT . . . 132
7.3.118 0x07E - EXT_5_ADCMON_DATAMSB_EXT . . . 132

7.3.119 0x07F - EXT_5_ADCMON_DATALSB_EXT . . . 132
7.3.120 0x080 - EXT_6_ADCMON_DATAMSB_EXT . . . 132
7.3.121 0x081 - EXT_6_ADCMON_DATALSB_EXT . . . 132
7.3.122 0x082 - EXT_7_ADCMON_DATAMSB_EXT . . . 132
7.3.123 0x083 - EXT_7_ADCMON_DATALSB_EXT . . . 132
7.3.124 0x084 - EXT_8_ADCMON_DATAMSB_EXT . . . 132
7.3.125 0x085 - EXT_8_ADCMON_DATALSB_EXT . . . 133
7.3.126 0x086 - EXT_9_ADCMON_DATAMSB_EXT . . . 133
7.3.127 0x087 - EXT_9_ADCMON_DATALSB_EXT . . . 133
7.3.128 0x088 - EXT_10_ADCMON_DATAMSB_EXT . . . 133
7.3.129 0x089 - EXT_10_ADCMON_DATALSB_EXT . . . 133
7.3.130 0x08A - EXT_11_ADCMON_DATAMSB_EXT . . . 133
7.3.131 0x08B - EXT_11_ADCMON_DATALSB_EXT . . . 133
7.3.132 0x08C - EXT_12_ADCMON_DATAMSB_EXT . . . 133
7.3.133 0x08D - EXT_12_ADCMON_DATALSB_EXT . . . 134
7.3.134 0x08E - EXT_13_ADCMON_DATAMSB_EXT . . . 134
7.3.135 0x08F - EXT_13_ADCMON_DATALSB_EXT . . . 134
7.3.136 0x090 - EXT_14_ADCMON_DATAMSB_EXT . . . 134
7.3.137 0x091 - EXT_14_ADCMON_DATALSB_EXT . . . 134
7.3.138 0x092 - EXT_15_ADCMON_DATAMSB_EXT . . . 134
7.3.139 0x093 - EXT_15_ADCMON_DATALSB_EXT . . . 134
7.3.140 0x094 - MTE_CFG_CTRL_A . . . 135
7.3.141 0x095 - WDT_KICK_REG . . . 135
7.3.142 0x096 - WDT_LFSR . . . 135
7.3.143 0x09B - I_LOCK_OUT_CFG (OTP) . . . 135
7.3.144 0x102 - IO_MODECTRL (OTP) . . . 136
7.3.145 0x103 - IO_I2CADDR (OTP) . . . 136
7.3.146 0x104 - IO_I2C_SPICFG (OTP) . . . 136
7.3.147 0x105 - IO_FUNC_CFG (OTP) . . . 137
7.3.148 0x107 - WDT_CFG0 (OTP) . . . 137
7.3.149 0x108 - WDT_CFG1 (OTP) . . . 137
7.3.150 0x109 - WDT_CFG2 (OTP) . . . 138
7.3.151 0x10A - WDT_CFG3 . . . 138
7.3.152 0x10B - WDT_CFG4 (OTP) . . . 138
7.3.153 0x10C - FUSA_CTRL_1 (OTP) . . . 138
7.3.154 0x10D - FUSA_CHK_CVM2H (OTP) . . . 139
7.3.155 0x10E - FUSA_CHK_CVM2L (OTP) . . . 142
7.3.156 0x10F - FUSA_CHK_CVM3H (OTP) . . . 145
7.3.157 0x110 - FUSA_CHK_CVM3L (OTP) . . . 148
7.3.158 0x111 - FUSA_CHK_CVM4H (OTP) . . . 151
7.3.159 0x112 - FUSA_CHK_CVM4L (OTP) . . . 154
7.3.160 0x113 - FUSA_CHK_CVM5H (OTP) . . . 157
7.3.161 0x114 - FUSA_CHK_CVM5L (OTP) . . . 160
7.3.162 0x115 - FUSA_CTRL_MTE (OTP) . . . 163
7.3.163 0x116 - FUSA_TIMER_1 (OTP) . . . 163
7.3.164 0x117 - FUSA_TIMER_2 (OTP) . . . 164
7.3.165 0x118 - FUSA_TIMER_3 (OTP) . . . 165
7.3.166 0x119 - FUSA_TIMER_4 (OTP) . . . 166
7.3.167 0x11A - FUSA_CTRL_A (OTP) . . . 167

7.3.168 0x11B - FUSA_CTRL_B (OTP) . . . 167
7.3.169 0x11C - FUSA_CTRL_C (OTP) . . . 168
7.3.170 0x11D - FUSA_CTRL_D (OTP) . . . 168
7.3.171 0x11E - FUSA_CTRL_E (OTP) . . . 169
7.3.172 0x11F - SOC_PIN_DATA_1 (OTP) . . . 169
7.3.173 0x120 - SOC_PIN_DATA_2 (OTP) . . . 170
7.3.174 0x121 - SOC_PIN_DATA_3 (OTP) . . . 170
7.3.175 0x122 - SOC_PIN_DATA_4 (OTP) . . . 171
7.3.176 0x125 - FUSA_CTRL_CVM1 (OTP) . . . 172
7.3.177 0x126 - FUSA_CTRL_CVM2 (OTP) . . . 173
7.3.178 0x127 - FUSA_CTRL_CVM3 (OTP) . . . 174
7.3.179 0x128 - FUSA_CTRL_CVM4 (OTP) . . . 175
7.3.180 0x129 - FUSA_CTRL_CVM5 (OTP) . . . 176
7.3.181 0x12A - FUSA_CTRL_CVM6 (OTP) . . . 177
7.3.182 0x12C - FLT_MASK_B (OTP) . . . 178
7.3.183 0x12D - ADCMON_MASK_GND_AVIN (OTP) . . . 178
7.3.184 0x12E - ADCMON_MASK_BG_TEMP (OTP) . . . 179
7.3.185 0x12F - ADCMON_MASK_IntLDOs (OTP) . . . 180
7.3.186 0x130 - ADCMON_MASK_ExtLDOs (OTP) . . . 181
7.3.187 0x131 - ADCMON_MASK_BUCKs_B (OTP) . . . 181
7.3.188 0x132 - ADCMON_MASK_BUCKs_A (OTP) . . . 182
7.3.189 0x133 - ADCMON_MASK_ExtINPs_7_0 (OTP) . . . 183
7.3.190 0x134 - ADCMON_CFG (OTP) . . . 183
7.3.191 0x135 - ADCMON_EXT_CFG (OTP) . . . 184
7.3.192 0x136 - ADCMON_Gain_IIRCoeff_Offset (OTP) . . . 184
7.3.193 0x13B - ADCMON_Gain_IIRCoeff_Temp (OTP) . . . 184
7.3.194 0x13C - ADCMON_ShutDNLimitMSB_Temp (OTP) . . . 184
7.3.195 0x13D - ADCMON_ShutDNLimitLSB_Temp (OTP) . . . 184
7.3.196 0x13E - ADCMON_WarnLimitMSB_Temp (OTP) . . . 185
7.3.197 0x13F - ADCMON_WarnLimitLSB_Temp (OTP) . . . 185
7.3.198 0x140 - ADCMON_ShutDNLimitMSB_Temp4 (OTP) . . . 185
7.3.199 0x141 - ADCMON_ShutDNLimitLSB_Temp4 (OTP) . . . 185
7.3.200 0x142 - ADCMON_Gain_IIRCoeff_BGRegu (OTP) . . . 185
7.3.201 0x147 - ADCMON_Gain_IIRCoeff_PGNDRegu (OTP) . . . 186
7.3.202 0x148 - ADCMON_LimHighMSB_PGNDRegu (OTP) . . . 186
7.3.203 0x149 - ADCMON_LimHighLSB_PGNDRegu (OTP) . . . 186
7.3.204 0x14A - ADCMON_LimLowMSB_PGNDRegu (OTP) . . . 187
7.3.205 0x14B - ADCMON_LimLowLSB_PGNDRegu (OTP) . . . 187
7.3.206 0x14C - ADCMON_Gain_IIRCoeff_IntLDO (OTP) . . . 187
7.3.207 0x151 - ADCMON_Gain_IIRCoeff_AVIN1 (OTP) . . . 187
7.3.208 0x152 - ADCMON_LimHighMSB_AVIN1 (OTP) . . . 188
7.3.209 0x153 - ADCMON_LimHighLSB_AVIN1 (OTP) . . . 188
7.3.210 0x154 - ADCMON_LimLowMSB_AVIN1 (OTP) . . . 188
7.3.211 0x155 - ADCMON_LimLowLSB_AVIN1 (OTP) . . . 189
7.3.212 0x156 - ADCMON_Gain_IIRCoeff_SPARE_0 (OTP) . . . 189
7.3.213 0x157 - ADCMON_LimHighMSB_SPARE_0 (OTP) . . . 189
7.3.214 0x158 - ADCMON_LimHighLSB_SPARE_0 (OTP) . . . 190
7.3.215 0x159 - ADCMON_LimLowMSB_SPARE_0 (OTP) . . . 190
7.3.216 0x15A - ADCMON_LimLowLSB_SPARE_0 (OTP) . . . 190

7.3.217 0x15B - extLDO_0_ADCMON_Gain_IIRCoeff_ExtLDO (OTP) 190
7.3.218 0x15C - extLDO_0_ADCMON_LimHighMSB_ExtLDO (OTP) 191
7.3.219 0x15D - extLDO_0_ADCMON_LimHighLSB_ExtLDO (OTP) 191
7.3.220 0x15E - extLDO_0_ADCMON_LimLowMSB_ExtLDO (OTP) 191
7.3.221 0x15F - extLDO_0_ADCMON_LimLowLSB_ExtLDO (OTP) 191
7.3.222 0x160 - extLDO_1_ADCMON_Gain_IIRCoeff_ExtLDO (OTP) 192
7.3.223 0x161 - extLDO_1_ADCMON_LimHighMSB_ExtLDO (OTP) 192
7.3.224 0x162 - extLDO_1_ADCMON_LimHighLSB_ExtLDO (OTP) 192
7.3.225 0x163 - extLDO_1_ADCMON_LimLowMSB_ExtLDO (OTP) 193
7.3.226 0x164 - extLDO_1_ADCMON_LimLowLSB_ExtLDO (OTP) 193
7.3.227 0x165 - extLDO_2_ADCMON_Gain_IIRCoeff_ExtLDO (OTP) 193
7.3.228 0x166 - extLDO_2_ADCMON_LimHighMSB_ExtLDO (OTP) 194
7.3.229 0x167 - extLDO_2_ADCMON_LimHighLSB_ExtLDO (OTP) 194
7.3.230 0x168 - extLDO_2_ADCMON_LimLowMSB_ExtLDO (OTP) 194
7.3.231 0x169 - extLDO_2_ADCMON_LimLowLSB_ExtLDO (OTP) 194
7.3.232 0x16A - extLDO_3_ADCMON_Gain_IIRCoeff_ExtLDO (OTP) 195
7.3.233 0x16B - extLDO_3_ADCMON_LimHighMSB_ExtLDO (OTP) 195
7.3.234 0x16C - extLDO_3_ADCMON_LimHighLSB_ExtLDO (OTP) 195
7.3.235 0x16D - extLDO_3_ADCMON_LimLowMSB_ExtLDO (OTP) 196
7.3.236 0x16E - extLDO_3_ADCMON_LimLowLSB_ExtLDO (OTP) 196
7.3.237 0x16F - extLDO_4_ADCMON_Gain_IIRCoeff_ExtLDO (OTP) 196
7.3.238 0x170 - extLDO_4_ADCMON_LimHighMSB_ExtLDO (OTP) 197
7.3.239 0x171 - extLDO_4_ADCMON_LimHighLSB_ExtLDO (OTP) 197
7.3.240 0x172 - extLDO_4_ADCMON_LimLowMSB_ExtLDO (OTP) 197
7.3.241 0x173 - extLDO_4_ADCMON_LimLowLSB_ExtLDO (OTP) 197
7.3.242 0x174 - extLDO_5_ADCMON_Gain_IIRCoeff_ExtLDO (OTP) 198
7.3.243 0x175 - extLDO_5_ADCMON_LimHighMSB_ExtLDO (OTP) 198
7.3.244 0x176 - extLDO_5_ADCMON_LimHighLSB_ExtLDO (OTP) 198
7.3.245 0x177 - extLDO_5_ADCMON_LimLowMSB_ExtLDO (OTP) 199
7.3.246 0x178 - extLDO_5_ADCMON_LimLowLSB_ExtLDO (OTP) 199
7.3.247 0x179 - PVIN_0_ADCMON_Gain_IIRCoeff_PVIN (OTP) 199
7.3.248 0x17A - PVIN_0_ADCMON_LimHighMSB_PVIN (OTP) 200
7.3.249 0x17B - PVIN_0_ADCMON_LimHighLSB_PVIN (OTP) 200
7.3.250 0x17C - PVIN_0_ADCMON_LimLowMSB_PVIN (OTP) 200
7.3.251 0x17D - PVIN_0_ADCMON_LimLowLSB_PVIN (OTP) 200
7.3.252 0x17E - PVIN_1_ADCMON_Gain_IIRCoeff_PVIN (OTP) 201
7.3.253 0x17F - PVIN_1_ADCMON_LimHighMSB_PVIN (OTP) 201
7.3.254 0x180 - PVIN_1_ADCMON_LimHighLSB_PVIN (OTP) 201
7.3.255 0x181 - PVIN_1_ADCMON_LimLowMSB_PVIN (OTP) 202
7.3.256 0x182 - PVIN_1_ADCMON_LimLowLSB_PVIN (OTP) 202
7.3.257 0x183 - PVIN_2_ADCMON_Gain_IIRCoeff_PVIN (OTP) 202
7.3.258 0x184 - PVIN_2_ADCMON_LimHighMSB_PVIN (OTP) 203
7.3.259 0x185 - PVIN_2_ADCMON_LimHighLSB_PVIN (OTP) 203
7.3.260 0x186 - PVIN_2_ADCMON_LimLowMSB_PVIN (OTP) 203
7.3.261 0x187 - PVIN_2_ADCMON_LimLowLSB_PVIN (OTP) 203
7.3.262 0x188 - PVIN_3_ADCMON_Gain_IIRCoeff_PVIN (OTP) 204
7.3.263 0x189 - PVIN_3_ADCMON_LimHighMSB_PVIN (OTP) 204
7.3.264 0x18A - PVIN_3_ADCMON_LimHighLSB_PVIN (OTP) 204
7.3.265 0x18B - PVIN_3_ADCMON_LimLowMSB_PVIN (OTP) 205

7.3.266 0x18C - PVIN_3_ADCMON_LimLowLSB_PVIN (OTP) 205
7.3.267 0x18D - PVIN_4_ADCMON_Gain_IIRCoeff_PVIN (OTP) 205
7.3.268 0x18E - PVIN_4_ADCMON_LimHighMSB_PVIN (OTP) 206
7.3.269 0x18F - PVIN_4_ADCMON_LimHighLSB_PVIN (OTP) 206
7.3.270 0x190 - PVIN_4_ADCMON_LimLowMSB_PVIN (OTP) 206
7.3.271 0x191 - PVIN_4_ADCMON_LimLowLSB_PVIN (OTP) 206
7.3.272 0x192 - VOUT_0_ADCMON_Gain_IIRCoeff_VOUT (OTP) 207
7.3.273 0x193 - VOUT_0_ADCMON_LimHighMSB_VOUT (OTP) 207
7.3.274 0x194 - VOUT_0_ADCMON_LimHighLSB_VOUT (OTP) 207
7.3.275 0x195 - VOUT_0_ADCMON_LimLowMSB_VOUT (OTP) 208
7.3.276 0x196 - VOUT_0_ADCMON_LimLowLSB_VOUT (OTP) 208
7.3.277 0x197 - VOUT_1_ADCMON_Gain_IIRCoeff_VOUT (OTP) 208
7.3.278 0x198 - VOUT_1_ADCMON_LimHighMSB_VOUT (OTP) 209
7.3.279 0x199 - VOUT_1_ADCMON_LimHighLSB_VOUT (OTP) 209
7.3.280 0x19A - VOUT_1_ADCMON_LimLowMSB_VOUT (OTP) 209
7.3.281 0x19B - VOUT_1_ADCMON_LimLowLSB_VOUT (OTP) 209
7.3.282 0x19C - VOUT_2_ADCMON_Gain_IIRCoeff_VOUT (OTP) 210
7.3.283 0x19D - VOUT_2_ADCMON_LimHighMSB_VOUT (OTP) 210
7.3.284 0x19E - VOUT_2_ADCMON_LimHighLSB_VOUT (OTP) 210
7.3.285 0x19F - VOUT_2_ADCMON_LimLowMSB_VOUT (OTP) 211
7.3.286 0x1A0 - VOUT_2_ADCMON_LimLowLSB_VOUT (OTP) 211
7.3.287 0x1A1 - VOUT_3_ADCMON_Gain_IIRCoeff_VOUT (OTP) 211
7.3.288 0x1A2 - VOUT_3_ADCMON_LimHighMSB_VOUT (OTP) 212
7.3.289 0x1A3 - VOUT_3_ADCMON_LimHighLSB_VOUT (OTP) 212
7.3.290 0x1A4 - VOUT_3_ADCMON_LimLowMSB_VOUT (OTP) 212
7.3.291 0x1A5 - VOUT_3_ADCMON_LimLowLSB_VOUT (OTP) 212
7.3.292 0x1A6 - VOUT_4_ADCMON_Gain_IIRCoeff_VOUT (OTP) 213
7.3.293 0x1A7 - VOUT_4_ADCMON_LimHighMSB_VOUT (OTP) 213
7.3.294 0x1A8 - VOUT_4_ADCMON_LimHighLSB_VOUT (OTP) 213
7.3.295 0x1A9 - VOUT_4_ADCMON_LimLowMSB_VOUT (OTP) 214
7.3.296 0x1AA - VOUT_4_ADCMON_LimLowLSB_VOUT (OTP) 214
7.3.297 0x1AB - EXT_0_ADCMON_Gain_IIRCoeff_EXT (OTP) 214
7.3.298 0x1AC - EXT_0_ADCMON_LimHighMSB_EXT (OTP) 215
7.3.299 0x1AD - EXT_0_ADCMON_LimHighLSB_EXT (OTP) 215
7.3.300 0x1AE - EXT_0_ADCMON_LimLowMSB_EXT (OTP) 215
7.3.301 0x1AF - EXT_0_ADCMON_LimLowLSB_EXT (OTP) 215
7.3.302 0x1B0 - EXT_1_ADCMON_Gain_IIRCoeff_EXT (OTP) 216
7.3.303 0x1B1 - EXT_1_ADCMON_LimHighMSB_EXT (OTP) 216
7.3.304 0x1B2 - EXT_1_ADCMON_LimHighLSB_EXT (OTP) 216
7.3.305 0x1B3 - EXT_1_ADCMON_LimLowMSB_EXT (OTP) 217
7.3.306 0x1B4 - EXT_1_ADCMON_LimLowLSB_EXT (OTP) 217
7.3.307 0x1B5 - EXT_2_ADCMON_Gain_IIRCoeff_EXT (OTP) 217
7.3.308 0x1B6 - EXT_2_ADCMON_LimHighMSB_EXT (OTP) 218
7.3.309 0x1B7 - EXT_2_ADCMON_LimHighLSB_EXT (OTP) 218
7.3.310 0x1B8 - EXT_2_ADCMON_LimLowMSB_EXT (OTP) 218
7.3.311 0x1B9 - EXT_2_ADCMON_LimLowLSB_EXT (OTP) 218
7.3.312 0x1BA - EXT_3_ADCMON_Gain_IIRCoeff_EXT (OTP) 219
7.3.313 0x1BB - EXT_3_ADCMON_LimHighMSB_EXT (OTP) 219
7.3.314 0x1BC - EXT_3_ADCMON_LimHighLSB_EXT (OTP) 219

7.3.315 0x1BD - EXT_3_ADCMON_LimLowMSB_EXT (OTP) 220
7.3.316 0x1BE - EXT_3_ADCMON_LimLowLSB_EXT (OTP) 220
7.3.317 0x1BF - EXT_4_ADCMON_Gain_IIRCoeff_EXT (OTP) 220
7.3.318 0x1C0 - EXT_4_ADCMON_LimHighMSB_EXT (OTP) 221
7.3.319 0x1C1 - EXT_4_ADCMON_LimHighLSB_EXT (OTP) 221
7.3.320 0x1C2 - EXT_4_ADCMON_LimLowMSB_EXT (OTP) 221
7.3.321 0x1C3 - EXT_4_ADCMON_LimLowLSB_EXT (OTP) 221
7.3.322 0x1C4 - EXT_5_ADCMON_Gain_IIRCoeff_EXT (OTP) 222
7.3.323 0x1C5 - EXT_5_ADCMON_LimHighMSB_EXT (OTP) 222
7.3.324 0x1C6 - EXT_5_ADCMON_LimHighLSB_EXT (OTP) 222
7.3.325 0x1C7- EXT_5_ADCMON_LimLowMSB_EXT (OTP) 223
7.3.326 0x1C8 - EXT_5_ADCMON_LimLowLSB_EXT (OTP) 223
7.3.327 0x1C9 - EXT_6_ADCMON_Gain_IIRCoeff_EXT (OTP) 223
7.3.328 0x1CA - EXT_6_ADCMON_LimHighMSB_EXT (OTP) 224
7.3.329 0x1CB - EXT_6_ADCMON_LimHighLSB_EXT (OTP) 224
7.3.330 0x1CC - EXT_6_ADCMON_LimLowMSB_EXT (OTP) 224
7.3.331 0x1CD - EXT_6_ADCMON_LimLowLSB_EXT (OTP) 224
7.3.332 0x1CE - EXT_7_ADCMON_Gain_IIRCoeff_EXT (OTP) 225
7.3.333 0x1CF - EXT_7_ADCMON_LimHighMSB_EXT (OTP) 225
7.3.334 0x1D0 - EXT_7_ADCMON_LimHighLSB_EXT (OTP) 225
7.3.335 0x1D1 - EXT_7_ADCMON_LimLowMSB_EXT (OTP) 226
7.3.336 0x1D2 - EXT_7_ADCMON_LimLowLSB_EXT (OTP) 226
7.3.337 0x1D3 - EXT_8_ADCMON_Gain_IIRCoeff_EXT (OTP) 226
7.3.338 0x1D4 - EXT_9_ADCMON_Gain_IIRCoeff_EXT (OTP) 227
7.3.339 0x1D5 - EXT_10_ADCMON_Gain_IIRCoeff_EXT (OTP) 227
7.3.340 0x1D6 - EXT_11_ADCMON_Gain_IIRCoeff_EXT (OTP) 228
7.3.341 0x1D7 - EXT_12_ADCMON_Gain_IIRCoeff_EXT (OTP) 228
7.3.342 0x1D8 - EXT_13_ADCMON_Gain_IIRCoeff_EXT (OTP) 229
7.3.343 0x1D9 - EXT_14_ADCMON_Gain_IIRCoeff_EXT (OTP) 229
7.3.344 0x1DA - EXT_15_ADCMON_Gain_IIRCoeff_EXT (OTP) 230
7.3.345 0x264 - I_FUSA_CTRL_DBG (OTP) 230
7.3.346 0x301 - ADCMON_Gain_IIRCoeff_SPARE_1 (OTP) 231
7.3.347 0x302 - ADCMON_LimHighMSB_SPARE_1 (OTP) 231
7.3.348 0x303 - ADCMON_LimHighLSB_SPARE_1 (OTP) 231
7.3.349 0x304 - ADCMON_LimLowMSB_SPARE_1 (OTP) 232
7.3.350 0x305 - ADCMON_LimLowLSB_SPARE_1 (OTP) 232
7.3.351 0x306 - ADCMON_ShutDNLimitMSB_Temp_2B (OTP) 232
7.3.352 0x307 - ADCMON_ShutDNLimitLSB_Temp_2B (OTP) 232
7.3.353 0x309 – FUSA_TIMER_5 (OTP) 232

8. Package Outline Drawing 233

9. Ordering Information 233

10. Revision History 234

1. Overview

1.1 Typical Application Diagrams

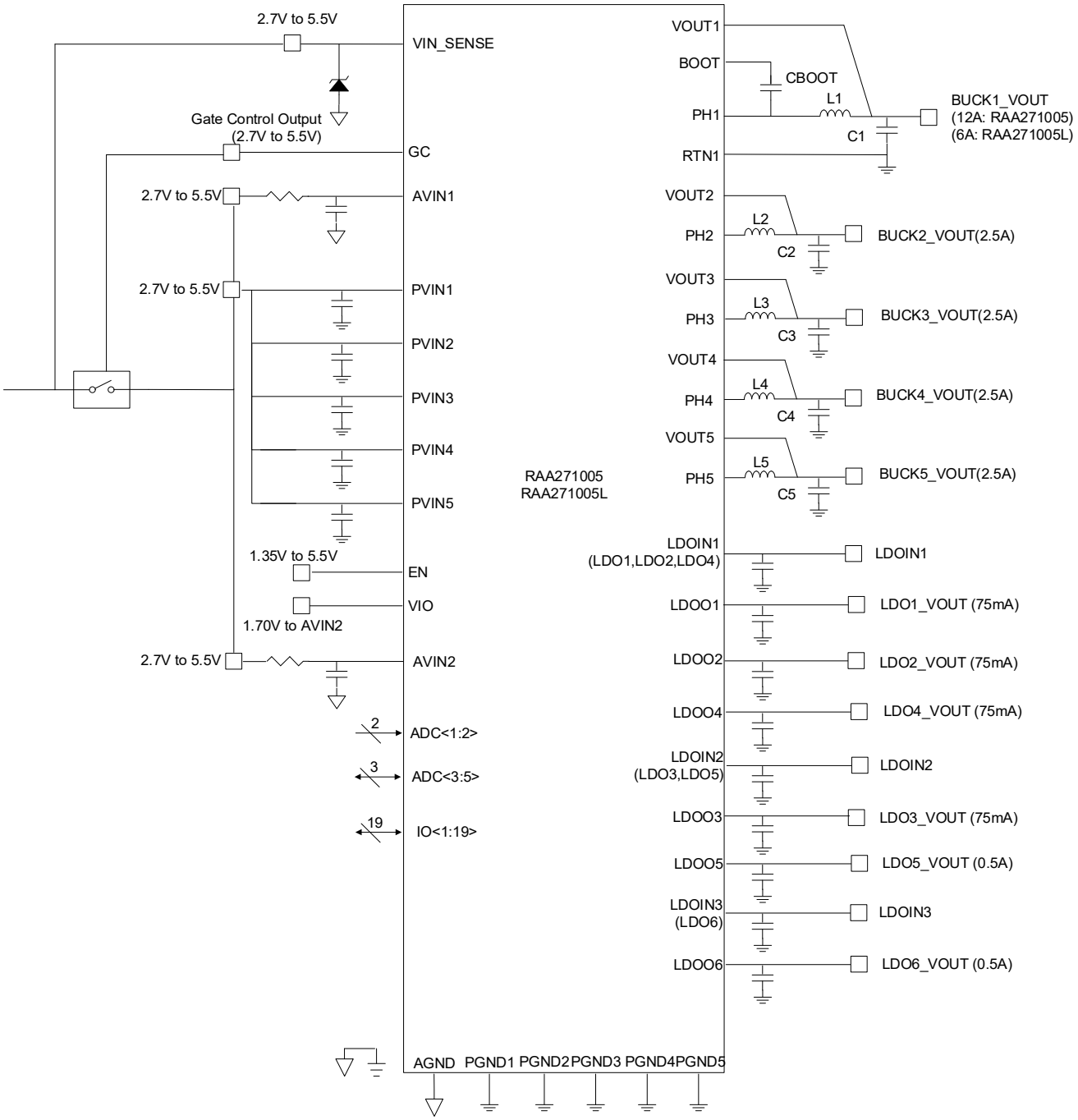


Figure 2. Typical Application Diagram with Five Bucks

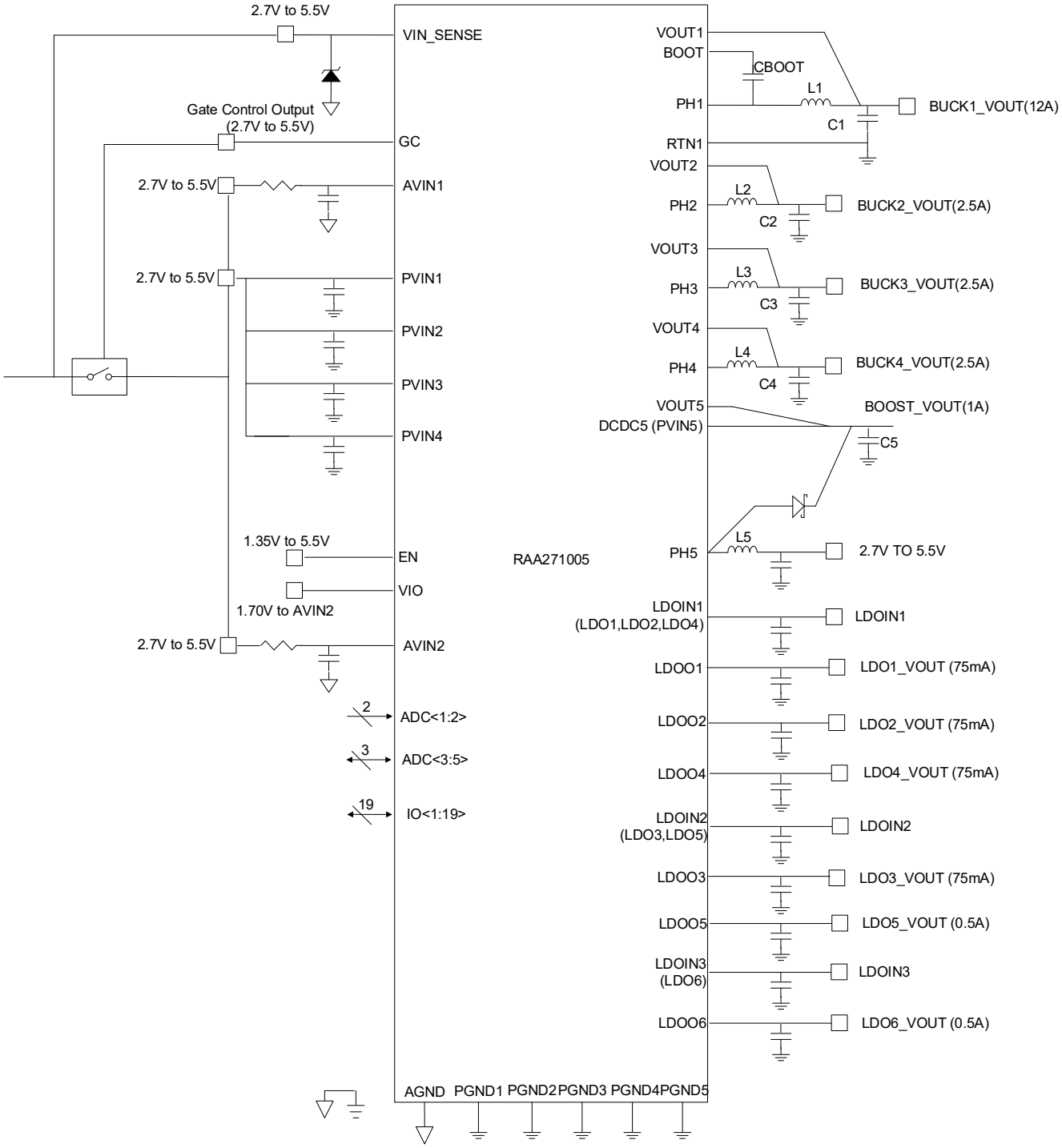


Figure 3. Typical Application Diagram with Four Bucks + One Boost

1.2 Block Diagram

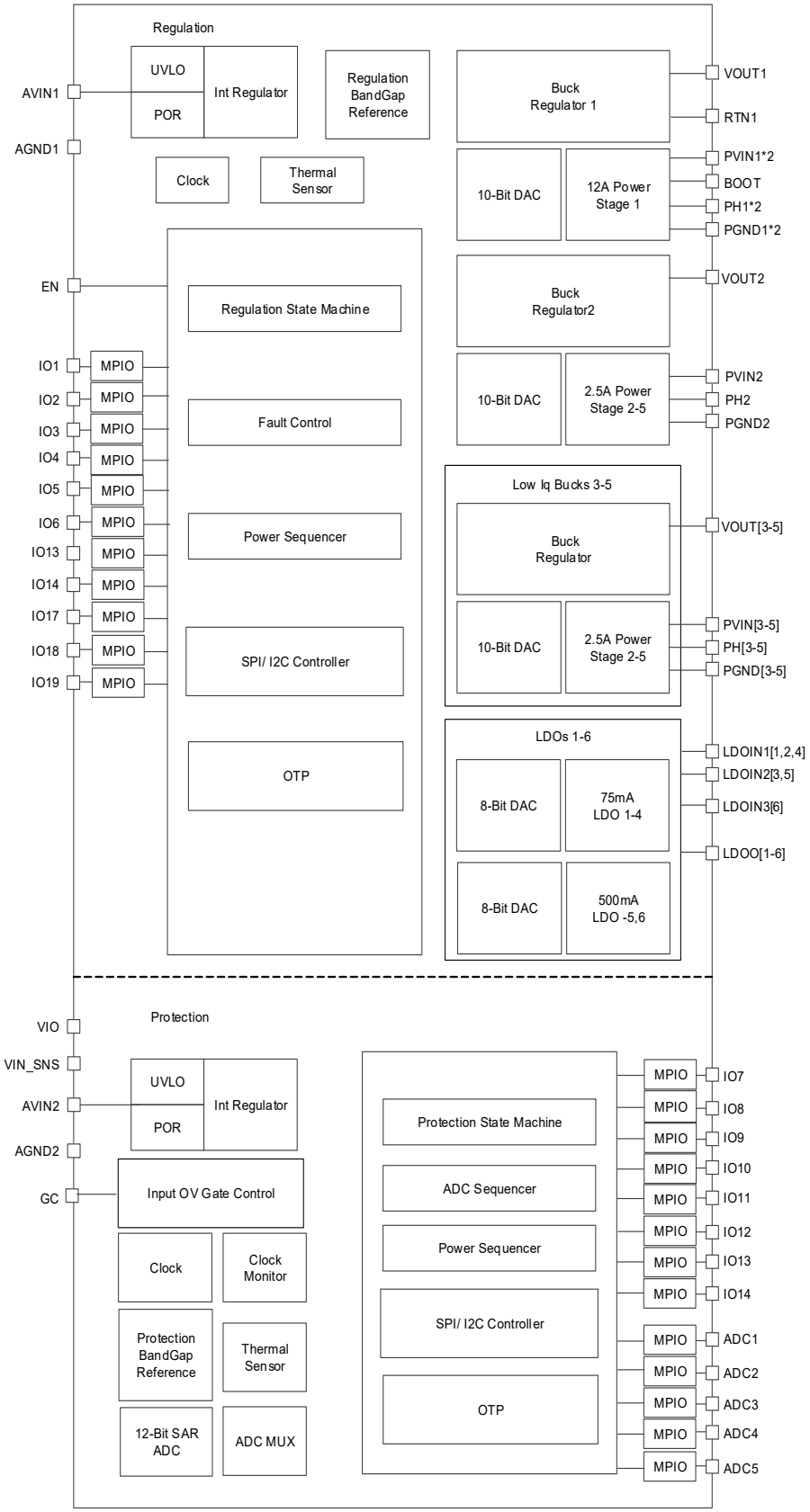


Figure 4. Simplified Block Diagram

2. Pin Information

2.1 Pin Assignments

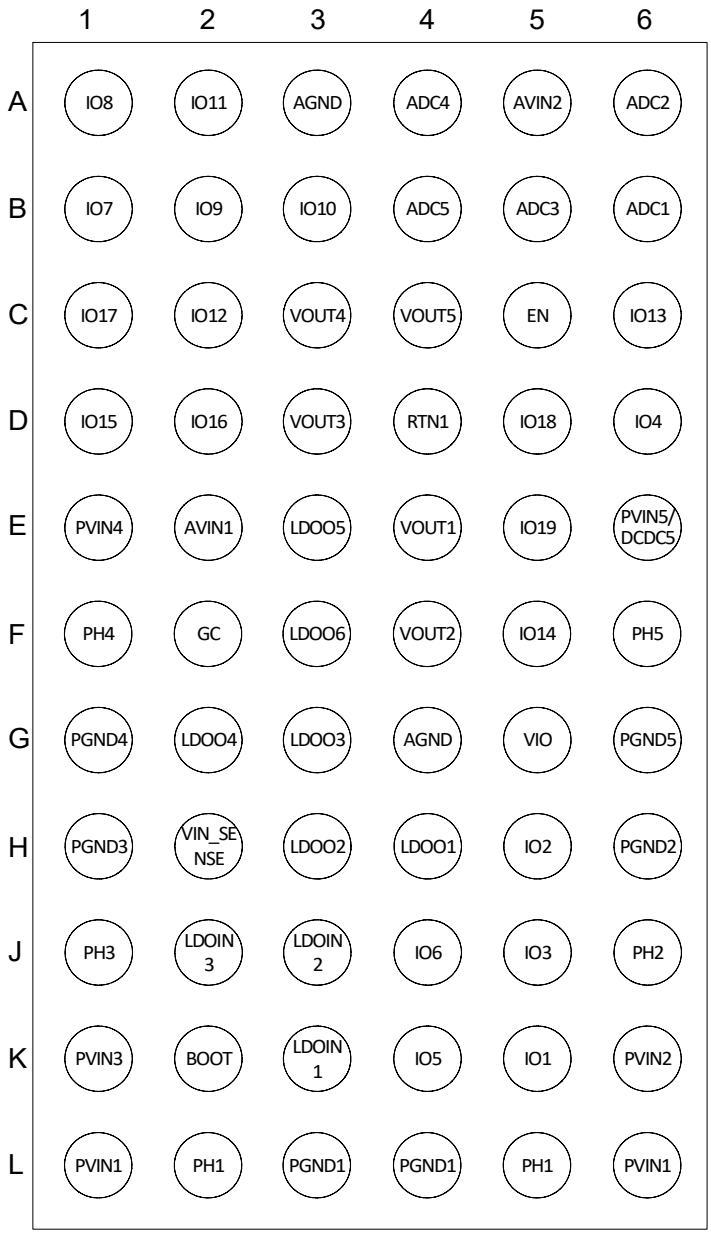


Figure 5. Pin Assignments – Balls Facing Down

2.2 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
A1	IO8	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
A2	IO11	Input/Output	
A3	AGND	GND	Analog ground
A4	ADC4	Input/Output	External ADC input or ADC decoder output
A5	AVIN2	Input	Analog supply voltage 2, 2.7V to 5.5V. This should be connected to AVIN1 on PCB.

Pin Number	Pin Name	Pin Type	Description
A6	ADC2	Input	External ADC input
B1	IO7	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
B2	IO9	Input/Output	
B3	IO10	Input/Output	
B4	ADC5	Input/Output	External ADC input or ADC decoder output
B5	ADC3	Input/Output	External ADC input or ADC decoder output. Can be configured to use as Lock Release signal.
B6	ADC1	Input	External ADC input
C1	IO17	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
C2	IO12	Input/Output	
C3	VOUT4	Input	Remote sense of the output voltage of Buck4
C4	VOUT5	Input	Remote sense of the output voltage of Buck5.
C5	EN	Input	Chip enable
C6	IO13	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
D1	IO15	Input/Output	
D2	IO16	Input/Output	
D3	VOUT3	Input	Remote sense of the output voltage of Buck3
D4	RTN1	Input	Remote ground sense at the load for Buck1
D5	IO18	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
D6	IO4	Input/Output	
E1	PVIN4	Input	Power supply for Buck4 power stage.
E2	AVIN1	Input	Analog supply voltage 1
E3	LDOO5	Output	LDO 5 power output
E4	VOUT1	Input	Remote sense of the output voltage of Buck1
E5	IO19	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
E6	PVIN5/ DCDC5	Input	Power supply for Buck5 power stage.
F1	PH4	Output	Switching node for Buck4 power stage.
F2	GC	Output	Gate control
F3	LDOO6	Output	LDO 6 power output
F4	VOUT2	Input	Remote sense of the output voltage of Buck2
F5	IO14	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
F6	PH5	Output	Switching node for Buck5 power stage.
G1	PGND4	GND	Ground connection for Buck4 power stage.
G2	LDOO4	Output	LDO 4 power output
G3	LDOO3	Output	LDO 3 power output
G4	AGND	GND	Analog ground (connect to analog ground with single connection to power ground)
G5	VIO	Input	I/O Supply Voltage
G6	PGND5	GND	Ground connection for Buck5 power stage.

Pin Number	Pin Name	Pin Type	Description
H1	PGND3	GND	Ground connection for Buck3 power stage.
H2	VIN_SENSE	Input	Input voltage monitoring pin for input overvoltage protection gate control (connect to V_{IN} if not used).
H3	LDOO2	Output	LDO 2 power output.
H4	LDOO1	Output	LDO 1 power output.
H5	IO2	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
H6	PGND2	GND	Ground connection for Buck2 power stage.
J1	PH3	Output	Switching node for Buck3 power stage.
J2	LDOIN3	Input	LDO 6 power input.
J3	LDOIN2	Input	LDO 3 and 5 power input.
J4	IO6	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
J5	IO3	Input/Output	
J6	PH2	Output	Switching node for Buck2 power stage.
K1	PVIN3	Input	Power supply for Buck3 power stage.
K2	BOOT	Input	Supply for boosted gate drive for Buck1.
K3	LDOIN1	Input	LDO 1, 2, and 4 power input.
K4	IO5	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
K5	IO1	Input/Output	
K6	PVIN2	Input	Power supply for Buck2 power stage.
L1, L6	PVIN1	Input	Power supply for Buck1 power stage.
L2, L5	PH1	Output	Switching node for Buck1 power stage.
L3, L4	PGND1	GND	Ground connection for Buck1 power stage.

2.2.1 I/O Pin Configurations

RAA271005/RAA271005L supports a number of different pin configurations to address different application requirements. The pin mode value is factory programmed.

Table 1. IO Pin Default Configuration Table[1]

Pin Mode	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8	IO9	IO10	IO11	IO12	IO13	IO14	IO15	IO16	IO17	IO18	IO19
0x0	SCK	SS_B2	SS_B	MOSI	MISO	GPIO/DVS	SDI1	PRESET#	SDO1	SDO2	PRESETOUT	SDI2	GPIO	IRQ#	SDI3	SDI4	PWR_CTRL1	PWR_CTRL2	BKUP
0x1	SCL	SDA	GPIO1	GPIO2	GPIO3	GPIO/DVS	SDI1	PRESET#	SDO1	SDO2	PRESETOUT	SDI2	GPIO	IRQ#	SDI3	SDI4	PWR_CTRL1	PWR_CTRL2	BKUP

1. IO3, IO4, IO5, IO6, IO13, IO19 can be configured through OTP for other settings.

2.2.2 I/O Pin Descriptions

Table 2. I/O Descriptions

IO Name	Type	Description
IO6(GPIO / DVS)	Output	General Purpose IO or Buck1 Dynamic Voltage Scaling Pin
IO7(SDI1 / ERROROUT)	Input	R-Car SoC Error Notification Signal
IO8(PRESET#)	Output	Reset Signal sent to R-Car SoC
SDO1 / STB_N	Output	Standby Control Signal for CAN transceiver
SDO2 / SSP	Output	Secondary Safety Path Signal
IO14(IRQ#)	Output	Interrupt signal to R-Car SoC
IO17/IO18(PWR_CTRL1,2)	Input	Power Control inputs from the R-Car SoC to sequence certain rails
IO11(PRESETOUT)	Input	Reset notification signal from R-Car SoC
SDI2 / VMONOUT0	Input	Digital CVM Error signal notification from R-Car SoC
SDI3 / VMONOUT1	Input	
SDI4	Input	Safety Defined Input. Generic Error notification input signal.
IO19(BKUP)	Output	Signal indicating the turn-off of non-memory and non-AWO rails in Suspend-to-RAM mode
SS_B, SS_B2	Input	SPI Auxiliary select signals
SCK	Input	SPI clock signal
MOSI	Input	SPI Main Output Auxiliary Input Signal
MISO	Output	SPI Main Input Auxiliary Output Signal
SCL	Input	I^2C Clock Signal
SDA	Input/ Output	I^2C Data Signal
GPIOx	Input/ Output	General Purpose IO

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum[1]	Unit
PVIN[1-5], AVIN[1-2], LDOIN[1-3] pins to AGND, PGND[1-5]	-0.3	6	V
VOUT[3-5]	-0.3	(V_{OUT_PROG} + 0.3V)	V
VOUT[1], VOUT[2]	-0.3	(V_{OUT_PROG} + 0.3V) with max AVIN1, AVIN2	V
LDOO[1,2,4]	-0.3	(LDOIN1 + 0.3V) with max 6V	V
LDOO[3,5]	-0.3	(LDOIN2 + 0.3V) with max 6V	V
LDOO[6]	-0.3	(LDOIN3 + 0.3V) with max 6V	V
EN to AGND	-0.3	(VIN-SENSE + 0.3V) with max 6V	V
VIO to AGND	-0.3	AVIN + 0.3	V
PH[1-5] to PGND[1-5]	-0.3	PVIN + 0.3	V
PH[1] to PGND[1] transients for 1ns	-3.0	10.8	V
PH[2-5] to PGND[2-5] transients for 3ns	-2.5	10.0	V
ADC[1-5] to AGND	-0.3	AVIN2 + 0.3	V
GPIO[1-19] pins to AGND	-0.3	VIO + 0.3	V
RTN1, AGND[1-2] to PGND[1-5]	-0.3	0.3	V
VIN_SENSE to AGND	-0.3	12.5	V
GC to AGND	-0.3	(VIN-SENSE + 0.3V) with max 6V	V
BOOT to PH1	-0.3	6	V
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per AEC-Q100-002E)	-	2	kV
Charged Device Model (Tested per AEC-Q100-011)	-	500	V
Charged Device Model Corner Pins (Tested per AEC-Q100-011D)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. V_{OUT_PRG} is the programmed output voltage of the regulator: $V_{OUT[1-5]}$.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage (AVIN1, AVIN2 to GND)	2.7	5.5	V
Supply Voltage (PVINx to GND)	2.7	5.5	V
Supply Voltage (LDOIN1 to GND)	2.7	5.5	V
Supply Voltage (LDOIN2 to GND)	1.8 (LDO3 OFF) 2.7 (LDO3 ON)	5.5	V
Supply Voltage (LDOIN3 to GND)	1.8	5.5	V
Supply Voltage (VIN_SENSE to GND)	2.7	5.5	V
Ambient Temperature	-40	+125	°C
VIO Voltage (VIO to GND)	1.7	AVIN2	V
Buck1 Operating Current	0	12	A
Buck [2-5] Operating Current	0	2.5	A
LDO1-4 Operating Current	0	75	mA
LDO5-6 Operating Current	0	500	mA

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	66 Ball BGA Package	θ_{JA}[1]	Junction to ambient	18.5	°C/W
		θ_{JC}[2]	Junction to case	8.8	°C/W

1. θ_{JA} is measured in free air with the component mounted on a 48mil FR-4 8-layer 1oz Cu board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is taken at the package top center.

3.4 Electrical Specifications

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Input Supply						
Supply Voltage	AVIN	-	**2.7**	-	**5.5**	V
	PVIN	-	**2.7**	-	**5.5**	V
I/O Supply Voltage	VIO	-	**1.7**	-	**AVIN**	V
Operating Current at VIN_SENSE	Iq_S	EN = 0V, VIN_SENSE = 5V	-	2.2	**5**	µA
		EN = High, VIN_SENSE = 5V	-	8.5	**25**	µA

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Operating Current at AVIN	Iq	EN = 0V, AVINx = 5V	-	1	**3**	µA
		I_{OUT} = 0A, AVINx = 5V, PFM Mode, Buck3 enabled, Low Iq Mode (Deep Stop), T_J = 25°C, ADCx Pins = GND, SDOx Pins = GND	-	100	160	µA
		I_{OUT} = 0A, AVINx = 5V, PFM Mode, Buck3 enabled, Low Iq Mode (Deep Stop), T_J = 150°C	-	-	**1000**	µA
		I_{OUT} = 0A, AVIN1 = 5V, switching, all rails enabled	-	-	**5**	mA
		I_{OUT} = 0A, AVIN2 = 5V, switching, all rails enabled	-	-	**13.9**	mA
UVLO Rising Threshold	V_{UVLOR}	AVIN1, AVIN2, and VIN_SENSE	**2.7**	-	**2.9**	V
UVLO Falling Threshold	V_{UVLOF}	AVIN1, AVIN2, and VIN_SENSE	**2.5**	-	**2.7**	V
UVLO Hysteresis	$V_{UVLOhys}$	-	**154**	200	**225**	mV
PVIN4 UV Rising	-	PVIN4 UV rising threshold	**2.7**	-	**2.9**	V
PVIN4 UV Falling	-	PVIN4 UV falling threshold	**2.5**	-	**2.7**	V
AVIN1 OVP Rising Threshold	V_{OVPR}	-	**5.7**	5.85	**6**	V
AVIN1 OVP Hysteresis	V_{OVPhys}	-	**197**	210	**221**	mV
AVIN1 OVP Detection Time	-	±50mV step	-	7	-	µs
VIN_SENSE OVP Rising Threshold	V_{OVPR_S}	-	**5.45**	5.61	**5.8**	V
VIN_SENSE OVP Falling Threshold	V_{OVPF_S}	-	**3.93**	4.08	**4.25**	V
VIO UV Rising Threshold	V_{VIO_UVR}	-	**1.5**	-	**1.6**	V
VIO UV Falling Threshold	V_{VIO_UVF}	-	**1.44**	-	**1.55**	V
Buck Regulators: Regulation						
DC Output Voltage Accuracy	-	V_{OUT} > 0.8V, guaranteed to maximum load currents specified in Thermal Information (recommended operating conditions), CCM/PWM mode	**-1.5**	-	**1.5**	%
		V_{OUT} ≤ 0.8V, guaranteed to maximum load currents specified in Thermal Information (recommended operating conditions), CCM/PWM mode	**-13**	-	**13**	mV

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Buck Output UVP Threshold Accuracy	V_{UVP}	BUCKx_VOUTFBDIV[1:0] = 0b00; Threshold: -60mV, -100mV, -150mV, -200mV	**-30**	-	**30**	mV
		BUCKx_VOUTFBDIV[1:0] = 0b01; Threshold: -100mV, -150mV, -200mV, -250mV	**-40**	-	**40**	mV
		BUCKx_VOUTFBDIV[1:0] = 0b10; Threshold: -100mV, -150mV, -200mV, -250mV	**-46**	-	**46**	mV
		BUCKx_VOUTFBDIV[1:0] = 0b11; Threshold: -100mV, -150mV, -200mV, -250mV	**-120**	-	**120**	mV
Buck Output OVP Threshold Accuracy	V_{OVP}	BUCKx_VOUTFBDIV[1:0] = 0b00; Threshold: 60mV, 100mV, 150mV, 200mV	**-30**	-	**30**	mV
		BUCKx_VOUTFBDIV[1:0] = 0b01; Threshold: 100mV, 150mV, 200mV, 250mV	**-40**	-	**40**	mV
		BUCKx_VOUTFBDIV[1:0] = 0b10; Threshold: 100mV, 150mV, 200mV, 250mV	**-46**	-	**46**	mV
		BUCKx_VOUTFBDIV[1:0] = 0b11; Threshold: 100mV, 150mV, 200mV, 250mV	**-120**	-	**120**	mV
Buck Output UVP Detection Time	-	BUCKx_VOUTFBDIV[1:0] = 0b00, V_{OUT} = 0.8V, 1mV/µs slew-rate	-	6.5	-	µs
		BUCKx_VOUTFBDIV[1:0] = 0b11, V_{OUT} = 3.3V, 1mV/µs slew-rate	-	20.7	-	µs
Buck Output OVP Detection Time	-	BUCKx_VOUTFBDIV[1:0] = 0b00, V_{OUT} = 0.8V, 1mV/µs slew-rate	-	5.5	-	µs
		BUCKx_VOUTFBDIV[1:0] = 0b11, V_{OUT} = 3.3V, 1mV/µs slew-rate	-	15.8	-	µs
Buck1 Positive Overcurrent Limit	I_{LIMIT}	RAA271005 POC threshold accuracy	**12**	15	**18**	A
		RAA271005L POC threshold accuracy	**6**	9	**12**	A
Buck1 Negative Overcurrent Limit	I_{NLIMIT}	RAA271005 NOC threshold accuracy	**12**	15	**18**	A
		RAA271005L NOC threshold accuracy	**6**	9	**12**	A
Buck2 Positive Overcurrent Limit	I_{LIMIT}	POC threshold accuracy	**3**	4	**5**	A
Buck2 Negative Overcurrent Limit	I_{NLIMIT}	NOC threshold accuracy	**-20**	-	**20**	%
Buck3-5 Positive Overcurrent Limit	I_{LIMIT}	POC threshold accuracy	**-20**	-	**20**	%

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Buck3-5 Negative Overcurrent Limit	I_{NLIMIT}	NOC threshold accuracy	**-20**	-	**20**	%
Buck Min On-Time	Tmin-on	Buck1	-	-	**25**	ns
		Buck2	-	-	**20**	ns
		Buck3-5	-	-	**40**	ns
Buck Min Off-Time	Tmin-off	Buck1	-	-	**45**	ns
		Buck2	-	-	**20**	ns
		Buck3-5	-	-	**35**	ns
Discharge Resistance of Buck Output when Disabled	Buck 1 Rds_B1	4.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 0.83V	**4.5**	6.8	**16**	Ω
		4.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 0.4V	**4.5**	6.2	**15**	Ω
		4.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 0.1V	**4.2**	6.0	**14.5**	Ω
		2.7V ≤ V_{IN} < 4.5V, V_{OUT} = 0.83V	**4.5**	-	**29**	Ω
		2.7V ≤ V_{IN} < 4.5V, V_{OUT} = 0.4V	**4.5**	-	**24**	Ω
		2.7V ≤ V_{IN} < 4.5V, V_{OUT} = 0.1V	**4.5**	-	**21**	Ω
	Buck 2-5 Rds_B25	4.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 1.83V	**25**	46	**80**	Ω
		4.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 0.83V	**13**	29	**55**	Ω
		4.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 0.4V	**11**	25	**48**	Ω
		4.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 0.1V	**10**	23	**43**	Ω
		2.7V ≤ V_{IN} < 4.5V, V_{OUT} = 1.83V	**33**	-	**220**	Ω
		2.7V ≤ V_{IN} < 4.5V, V_{OUT} = 0.83V	**17**	-	**130**	Ω
		2.7V ≤ V_{IN} < 4.5V, V_{OUT} = 0.4V	**12.5**	-	**100**	Ω
		2.7V ≤ V_{IN} < 4.5V, V_{OUT} = 0.1V	**11**	-	**85**	Ω
Buck Regulators: Startup Response						
Buck Power-Up Slew Rate	V_{BCK_SLEW}	2.7V ≤ V_{IN} ≤ 5.5V, VOUTFBDIV = 1.0 (0.5 for Buck5)	**-10**	-	**10**	%
Buck Regulators: Switching Frequency						
R5 CCM Switching Frequency	f_{SW}	Buck1	-	2.33	-	MHz
		Buck2	-	2.33	-	MHz
R5 CCM Frequency Tolerance	f_{SW_TOL}	Buck[1-2] steady state operation (refer to section Buck Regulators, Buck[1-5] for CCM conditions)	**-15**	-	**15**	%
Fixed Frequency Tolerance	f_{SW_TOL}	Buck[1-2]; CCM, spread spectrum disabled.	-10	-	10	%
PCM CCM Switching Frequency	f_{SW}	Buck[3-5]; CCM, spread spectrum disabled.	-	2.2	-	MHz
PCM CCM Frequency Tolerance	f_{SW_TOL}	Buck[3-5]; CCM, spread spectrum disabled.	**-10**	-	**10**	%

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Buck Regulators: PFM Entry/Exit Transition Currents						
PWM to PFM Current Threshold	$I_{PWM-PFM}$	Buck2, DCM Ratio = 1.2 (V_{IN} = 5V, V_{OUT} = 1.1V, L = 240nH, C = 2×22µF)	-	800	-	mA
		Buck3-5 (V_{IN} = 5V, V_{OUT} = 0.83V, L = 240nH, C = 3×22µF)	-	200	-	mA
PFM to PWM Current Threshold	$I_{PFM-PWM}$	Buck2, DCM Ratio = 1.2 (V_{IN} = 5V, V_{OUT} = 1.1V, L = 240nH, C = 2×22µF)	-	960	-	mA
		Buck3-5 (V_{IN} = 5V, V_{OUT} = 0.83V, L =240nH, C = 3×22µF)	-	400	-	mA
Boost Regulator Option (Buck5)						
Input Voltage Range for Boost	V_{IN_BOOST}	-	**2.5**	3.3	**5.5**	V
DC Output Voltage Accuracy	-	V_{OUT} = 5V	**-2**	-	**2**	%
Pull-Down Resistance of Output	-	-	-	-	-	-
Switching Frequency CCM	f_{SW}	Spread spectrum disabled. Two options available		2.2		MHz
Fixed CCM Frequency Tolerance	f_{SW_TOL}	-	**-15**	-	**15**	%
Merged Mode Buck Regulator (Buck3 and Buck4)						
Buck3-4 Merged Positive Overcurrent Limit	I_{LIMIT}	POC threshold accuracy, I_{LIMIT} = 11.0A	**-20**	-	**20**	%
Buck3-4 Merged Negative Overcurrent Limit	I_{NLIMIT}	NOC threshold accuracy, I_{NLIMIT} = 10.6A	**-20**	-	**20**	%
DC Output Voltage Accuracy	-	V_{OUT} > 0.8V, guaranteed to max load currents specified in Thermal Information (recommended operating conditions), CCM/PWM mode	**-1.5**	-	**1.5**	%
	-	V_{OUT} ≤ 0.8V, guaranteed to max load currents specified in Thermal Information (recommended operating conditions), CCM/PWM mode	**-13**	-	**13**	mV
Switching Frequency CCM	f_{SW}	Spread spectrum disabled. Two options available.	-	2.2	-	MHz
Fixed CCM Frequency Tolerance	f_{SW_TOL}	-	**-15**	-	**15**	%

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Linear Regulators: LDO 1-4						
Input Voltage Range for LDO	V_{IN_LDO}	-	**2.7**	-	**5.5**	V
Operating Bias Current at LDO_IN1 (Only LDO1 Active)	Iq_ldo1	V_{LDOOUT} = 1.8V, 3.3V; I_{OUT} = 0	-	3.5	**6.5**	µA
		V_{LDOOUT} = 1.8V, 3.3V; I_{OUT} = 0.5mA	-	7.1	**16.5**	µA
		V_{LDOOUT} = 1.8V, 3.3V; I_{OUT} = 60mA	-	123	**140**	µA
		V_{LDOOUT} = 1.8V, 3.3V; I_{OUT} = 75mA	-	150	**170**	µA
DC Output Voltage Accuracy	-	V_{LDOOUT} = 1.8V, 3.3V; $V_{LDOOUT} < V_{LDOIN} - V_{DO}$, I_{OUT} = 0mA	**-1.5**	-	**1.5**	%
Rated Output Current	I_{OUTMAX}	V_{LDOIN} > 2.5V	**75**	-	-	mA
LDO UVP Threshold Accuracy	V_{UVP}	V_{LDOOUT} = 1.8V	**-30**	-	**30**	mV
		V_{LDOOUT} = 3.3V	**-60**	-	**60**	mV
LDO UVP Detection Time	-	1.8V Output, 6% setting, 5mV/µs	-	5.5	-	µs
Output Current Limit	I_{OUT_LIM}	-	**76**	95	**140**	mA
Dropout Voltage	V_{DO}	$V_{DO} = V_{LDOIN} – V_{LDOOUT}$, I_{OUT} = 75mA	-	-	**875**	mV
DC Load Regulation	ΔV_{LDOOUT} over I_{OUT}	0mA < I_{OUT} ≤ 75mA, V_{LDOOUT} = 1.8V	**-30**	-	-	mV
		0mA < I_{OUT} ≤ 75mA, V_{LDOOUT} = 3.3V	**-56.3**	-	-	mV
DC Line Regulation	-	$V_{LDOIN} = V_{INMIN}$ to V_{INMAX}, I_{OUT} = 0, V_{LDOOUT} = 1.8V	-	-	**4**	mV/V
		$V_{LDOIN} = V_{INMIN}$ to V_{INMAX}, I_{OUT} = 0, V_{LDOOUT} = 3.3V	-	-	**8**	mV/V
Power Supply Ripple Rejection	PSRR	f ≤ 1MHz, I_{OUT} = 0	-	35	-	dB
LDO Power-Up Slew Rate	V_{LDO_SLEW}	15mV/µs setting	**-10**	-	**10**	%
Pull-Down Resistance LDO Output when Disabled	Rds_LDO	-	**65**	90	**200**	Ω
Linear Regulators: LDO 5-6						
Input Voltage Range for LDO	V_{IN_LDO}	-	**1.8**	3.6	**5.5**	V
Operating Bias Current at LDO_IN5 (Only LDO5 Active)	Iq_ldo5	V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 0	-	225	**275**	µA
		V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 0.5mA	-	230	**280**	µA
		V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 100mA	-	1.475	**1.8**	mA
		V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 500mA	-	6.475	**7.89**	mA

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Operating Bias Current at LDO_IN6 (Only LDO6 Active)	Iq_ldo6	V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 0	-	233	**272**	µA
		V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 0.5mA	-	235	**287**	µA
		V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 100mA	-	1.475	**1.8**	mA
		V_{LDOOUT} = 0.6V, 1.8V, 3.3V; I_{OUT} = 500mA	-	6.475	**7.89**	mA
DC Output Voltage Accuracy	-	V_{LDOOUT} = 2.6V to 3.6V; V_{LDOOUT} < V_{LDOIN} - V_{DO}, I_{OUT} = 0mA	**-1.5**	-	**1.5**	%
		V_{LDOOUT} = 1.8V to 2.5V; V_{LDOOUT} < V_{LDOIN} - V_{DO}, I_{OUT} = 0mA	**-2.0**	-	**2.0**	%
		V_{LDOOUT} = 0.6V to 1.8V; V_{LDOOUT} < V_{LDOIN} - V_{DO}, I_{OUT} = 0mA	**-36**		**36**	mV
Rated Output Current	I_{OUTMAX}	V_{LDOIN} > 2.5V	**500**	-	-	mA
LDO UVP Threshold Accuracy	V_{UVP}	V_{LDOOUT} = 3.3V	**-60**	-	**60**	mV
LDO UVP Detection Time	-	3.3V Output, 6% setting, 5mV/µs	-	8.3	-	µs
Output Current Limit	I_{OUT_LIM}	-	**500**	-	**1000**	mA
Dropout Voltage	V_{DO}	V_{DO} = V_{LDOIN} - V_{LDOOUT}, I_{OUT} = 500mA, V_{LDOOUT} = 1.8V	-	-	**700**	mV
		V_{DO} = V_{LDOIN} - V_{LDOOUT}, I_{OUT} = 500mA, V_{LDOOUT} = 3.3V	-	-	**500**	mV
DC Load Regulation	ΔV_{LDOOUT} over I_{OUT}	0mA < I_{OUT} ≤ 500mA, V_{LDOOUT} = 0.6V	**-36**	-	-	mV
		0mA < I_{OUT} ≤ 500mA, V_{LDOOUT} = 1.8V	**-36**	-	-	mV
		0mA < I_{OUT} ≤ 500mA, V_{LDOOUT} = 3.3V	**-36**	-	-	mV
DC Line Regulation	-	V_{LDOIN} = 4.5V to 5.5V, I_{OUT} = 200mA, V_{LDOOUT} = 3.3V	-	0.2	**5**	mV/V
Power Supply Ripple Rejection	PSRR	f = 10kHz, I_{OUT} = ½ I_{OUTMAX}	-	40	-	dB
		f = 2.2MHz, I_{OUT} = ½ I_{OUTMAX}		10	-	
LDO Power-Up Slew Rate	V_{LDO_SLEW}	15mV/µs setting	**-10**	-	**10**	%
Pull-Down Resistance LDO Output when Disabled	Rds_LDO	-	**65**	85	**190**	Ω
GPIO: Chip Enable Logic Input						
EN Pin Falling Threshold	V_{THF}	AVIN1, AVIN2	-	-	**0.5**	V
EN Pin Rising Threshold	V_{THR}	AVIN1, AVIN2	**1.35**	-	-	V
EN Pin Minimum On-Time	-	Enable sampling period	**50**	-	-	µs

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
GPIO: Logic Threshold Levels						
Low-Level Input Voltage	V_{IL}	-	-	-	**0.25×VIO**	V
High-Level Input Voltage	V_{IH}	-	**0.72×VIO**	-	-	V
Input Hysteresis	V_{HYS}	-	**0.1×VIO**	-	-	V
Low-Level Output Voltage	V_{OL}	0.5mA/1mA sink at ≥(20%/50%) drive strength	-	-	**0.4**	V
High-Level Output Voltage	V_{OH}	0.5mA/1mA source at ≥(20%/50%) drive strength	**VIO-0.4**	-	-	V
GPIO Pull-Down Resistance	Rds_gpio	-	**117**	180	**243**	kΩ
Serial Interfaces						
I^2C Frequency Capability	f_{I2C}	-	**0.4**	-	**3.4**	MHz
SPI Frequency Capability	f_{SPI}	-	-	-	**26**	MHz
Over-Temperature Threshold						
Over-Temperature Rising Threshold Accuracy	OTR	Over-temperature threshold program from 135ºC to 170ºC in 5ºC increments. This is thermal trip comparator, triggered on rising temperature.	**-9**	-	**9**	ºC
Over-Temperature Falling Threshold Accuracy	OTF	Over-temperature threshold program from 90ºC to 125ºC in 5ºC increments. This is thermal trip comparator, untriggered when falling temperature	**-9**	-	**9**	ºC
Analog to Digital Converter						
Resolution	-	-	-	12	-	Bits
Reference Voltage	-	-	-	1.23	-	V
Sample Period	-	Internal Measurements	-	45	-	µs
		External Measurements without external MUX	-	110	-	µs
		External Measurements with external MUX	-	360	-	µs
ADC3 GPIO IN Signal as Lock Release Option						
ADC3 Pin Low-Level Input Voltage	$ADC3V_{IL}$	-	-	-	**¼×AVIN2**	V
ADC3 Pin High-Level Input Voltage	$ADC3V_{IH}$	-	**¾×AVIN2**	-	-	V
ADC Monitoring Accuracy						
Temperature Accuracy	-	IIR = 1/16	**-4**	-	**4**	ºC
Accuracy 0.6V	-	PGA Gain = 1.4, IIR = 1/16	**-1.5**	-	**1.5**	%
Accuracy 0.82V	-	PGA Gain = 0.8, IIR = 1/16	**-1.5**	-	**1.5**	%
Accuracy 1.1V	-	PGA Gain = 0.5, IIR = 1/16	**-1.5**	-	**1.5**	%
Accuracy 1.2V	-	PGA Gain = 0.5, IIR = 1/16	**-1.5**	-	**1.5**	%

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Accuracy 1.8V	-	PGA Gain = 0.333, IIR = 1/16	**-1.5**	-	**1.5**	%
Accuracy 2.5V	-	PGA Gain = 0.333, IIR = 1/16	**-1.5**	-	**1.5**	%
Accuracy 3.3V	-	PGA Gain = 0.125, IIR = 1/16	**-1.5**	-	**1.5**	%
Accuracy 4.0V	-	PGA Gain = 0.125, IIR = 1/16	**-1.5**	-	**1.5**	%
Accuracy 5.0V	-	PGA Gain = 0.125, IIR =1/16	**-1.5**	-	**1.5**	%
BUCK, LDO, AVIN, and PVIN ADC Monitoring Accuracy						
Accuracy 0.6V	-	PGA Gain = 1.4, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 0.82V	-	PGA Gain = 0.8, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 1.1V	-	PGA Gain = 0.5, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 1.2V	-	PGA Gain = 0.5, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 1.8V	-	PGA Gain = 0.333, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 2.5V	-	PGA Gain = 0.333, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 3.3V	-	PGA Gain = 0.125, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 4.0V	-	PGA Gain = 0.125, IIR =1/16	**-1.5**	-	**1.5**	%
Accuracy 5.0V	-	PGA Gain = 0.125, IIR =1/16	**-1.5**	-	**1.5**	%
Buck, LDO, AVIN, and PVIN ADC UV/OV Monitoring Accuracy						
OV Monitoring Accuracy	-	0.1V ≤ V_{OUT} < 0.3V Apply corresponding PGA gain (Table 26) with maximum input closest to OV and UV Thresholds. Default IIR = 1/16	**-20**	-	**20**	mV
	-	0.3V ≤ V_{OUT} < 0.56V Apply corresponding PGA gain (Table 26) with maximum input closest to OV and UV Thresholds. Default IIR = 1/16	**-4**	-	**4**	%
	-	0.56V ≤ V_{OUT} ≤ 5.5V Apply corresponding PGA gain (Table 26) with maximum input closest to OV and UV Thresholds. Default IIR = 1/16	**-1.5**	-	**1.5**	%

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
UV Monitoring Accuracy	-	0.1V ≤ V_{OUT} < 0.3V Apply corresponding PGA gain (Table 26) with maximum input closest to OV and UV Thresholds. Default IIR = 1/16	**-20**	-	**20**	mV
	-	0.3V ≤ V_{OUT} < 0.56V Apply corresponding PGA gain (Table 26) with maximum input closest to OV and UV Thresholds. Default IIR = 1/16	**-4**	-	**4**	%
	-	0.56V ≤ V_{OUT} ≤ 5.5V Apply corresponding PGA gain (Table 26) with maximum input closest to OV and UV Thresholds. Default IIR = 1/16	**-1.5**	-	**1.5**	%
Gate Control						
GC Response Time	-	VIN_SENSE ramp rate = 200mV/µs	-	-	**1**	µs
Startup/Shutdown Sequence Fixed Delays						
Buck Regulator Fixed Delay from EN	$T_{SU_BK_DELAY}$	See section Power State Transitions (R-Car S4 SoC Example)	**1.24**	1.58	**1.91**	ms
LDO Fixed Delay from EN	$T_{SU_LDO_DELAY}$	See section Power State Transitions (R-Car S4 SoC Example)	**0.99**	1.27	**1.55**	ms
Buck Regulator Fixed Delay from PWRCTLx	$T_{SU_BK_DELAY_PW}$	See section Power State Transitions (R-Car S4 SoC Example)	**0.81**	0.9	**0.99**	ms
LDO Fixed Delay from PWRCTLx	$T_{SU_LDO_DELAY_PW}$	See section Power State Transitions (R-Car S4 SoC Example)	**0.43**	0.48	**0.53**	ms
Protection BIST Delay	T_{BIST}	-	**4.17**	5.63	**7.09**	ms
Programmable Delays						
Delay Tolerance	-	All programmable delays; due to internal clock tolerance	**-10**	-	**10**	%
Discharge Detect						
DISC_TOUT Tolerance	-	-	**-10**	-	**10**	%
BUCK1_DISC_VTH Tolerance	-	VOUTFBDIV=1.0 Threshold: -150mV, -200mV, -250mV, -300mV	**-20**	-	**25**	mV

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C up to T_J = 150°C and PVIN, AVIN = 2.7V ~ 5.5V. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
BUCK2-5_DISC_VTH Tolerance	-	VOUTFBDIV=1.0 Threshold: -150mV, -200mV, -250mV, -300mV	**-20**	-	**20**	mV
		VOUTFBDIV=0.75 Threshold: -150mV, -200mV, -250mV, -300mV	**-25**	-	**25**	mV
		VOUTFBDIV=0.5 Threshold: -150mV, -200mV, -250mV, -300mV	**-30**	-	**35**	mV
		VOUTFBDIV=0.2, Threshold: -150mV, -200mV, -250mV, -300mV	**-100**	-	**100**	mV
LDOx_DISC_VTH Tolerance	-	LDO1-4, 1.8V Threshold: -150mV, -200mV, -250mV, -300mV	**-30**	-	**25**	mV
LDOx_DISC_VTH Tolerance	-	LDO 5,6, 3.3V Threshold: -150mV, -200mV, -250mV, -300mV	**-55**	-	**45**	mV

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits are established by characterization and are not production tested. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Applications Section

4.1 Power Sequencing

Both the startup and shutdown sequencing of RAA271005/RAA271005L are user programmable. Figure 6 shows a generic example for seven outputs versus Enable.

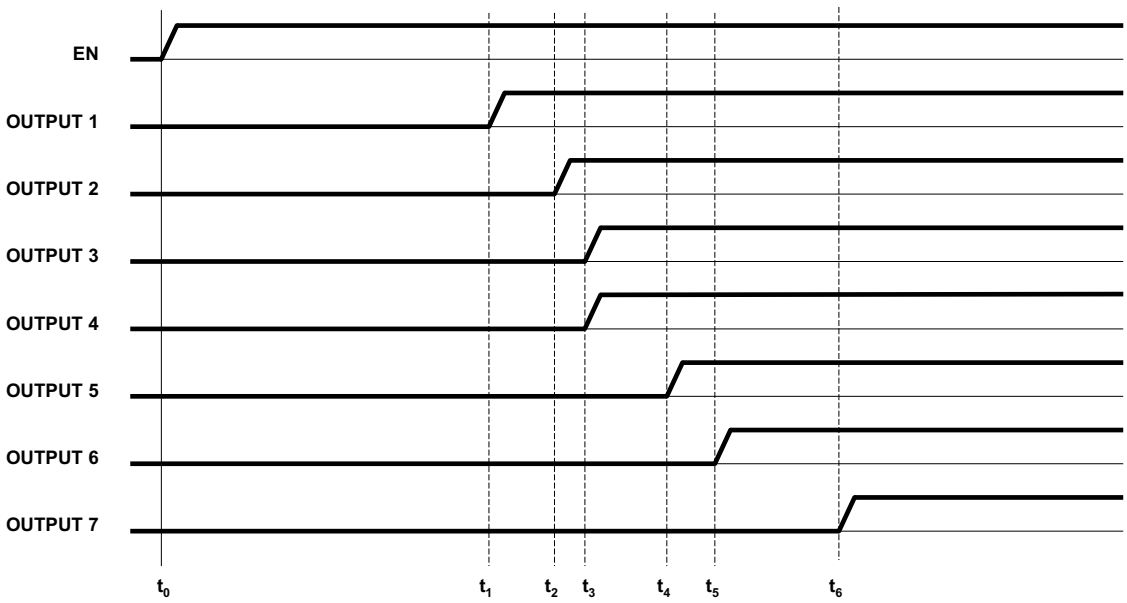


Figure 6. Startup Sequencing Example

For each output of RAA271005/RAA271005L (Buck[1-5] and LDO[1-6]), the startup delay can be programmed from a value of 0ms to 63ms in 0.25ms steps. This sequence can be set in registers *_EN_DLY where * is one of Buck1, Buck2, Buck3, Buck4, Buck5, LDO1, LDO2, LDO3, LDO4, LDO5, or LDO6. In the example startup sequence shown in Figure 6, OUTPUT1 has a 0ms delay from EN and the other outputs have an integer delay between 0.25ms and 63ms with ±10% tolerance.

Note: In this example, OUTPUT3 and OUTPUT4 have the same delay value. Even for a value of 0 for *_EN_DLY, there is a fixed wait time while the chip starts up and completes LBIST. This additional delay time is 1ms (typ). While the EN_DLY value specifies when an output begins to startup, each output also starts up with a factory programmed ramp rate, which is specified in Buck Regulator Startup Ramp Rate and LDO Startup Ramp Rate. An example of shutdown sequencing is shown in Figure 7.

Note: This example shows all rails configured as Always On (AWO) power group rails. S4 application uses power grouping into three categories known as AWO rails, PWRCTL1 rails, and PWRCTL2 rails. When power grouping is used the startup sequence has additional delays than shown in Figure 6. At EN high, the PMIC begins the power-up sequence by turning on the AWO rails and outputs an EXTPOC# signal, which is used by the MCU to enable the PWRCTL1 rails and SoC to enable the PWRCTL2 rails. When all the rails are enabled by the PMIC, PGOOD output signal is generated to indicate that the startup sequence is complet. The Power Grouping and Power State Transitions section shows more detail about the S4 power-up sequence as an example when the power control grouping is used by the application.

Note: Ensure the startup delays are set such that PGOOD >5ms after EN. This is the minimum time required by the sequencing control.

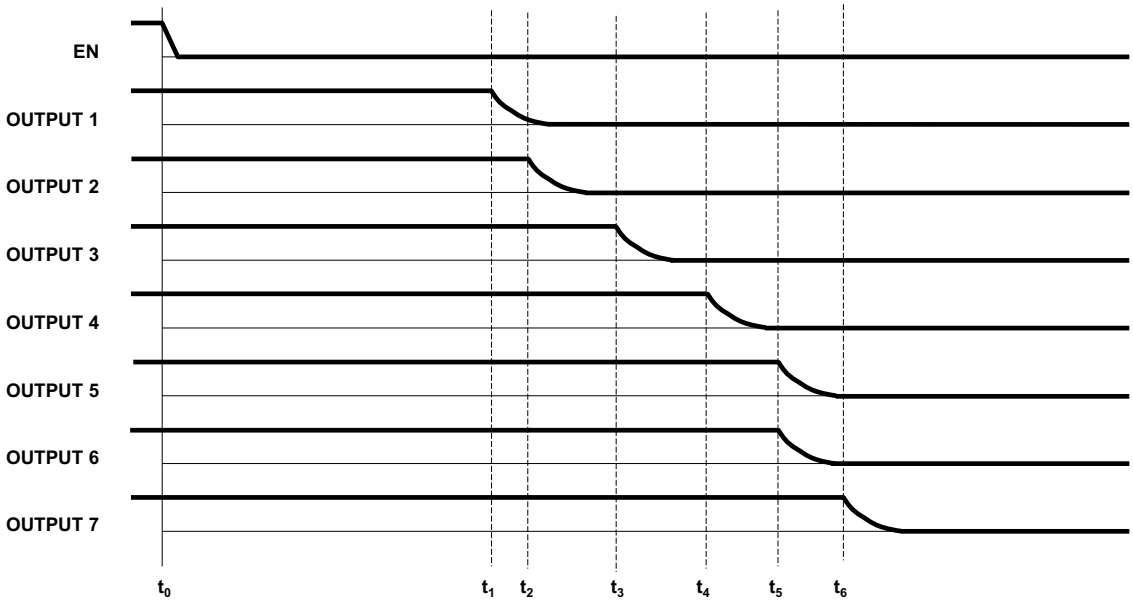


Figure 7. Shutdown Sequencing Example

Similar to the startup sequencing setting, each output can delay shutdown by between 0 to 63ms, which is specified in register *_SHUTDN_DLY. In Figure 7, the value of t_1 - t_0 can be 0ms. During shutdown, the sequencer gives the command to shut down a specific channel, which causes that output to go high impedance (both switches Hi-Z for buck regulators and the LDO output PMOS Hi-Z for LDO regulators) and pull down through a resistance, Rds_Bx or Rds_LDO.

Note: This example does not account for the additional delays due to power grouping. When the grouping of AWO, PWRCTL1, and PWRCTL2 is used, the rails follow the Deep Stop, S2R modes depending on the PWRCTL1/2 inputs. The Power Grouping and Power State Transitions section shows more detail about the S4 power-down sequence as an example when the power control grouping is used by the application.

4.2 Functional Safety

Functional safety for RAA271005/RAA271005L is described fully in the *Safety Application Note*.

4.3 Digital Interfaces

Depending on the pin mode option, RAA271005/RAA271005L can be controlled by an I^2C interface or by an SPI interface. Either interface can be used to read or write registers using the addressing mechanism of the specific interface. Each interface is described in the two following sections.

Note: To read/write an address after 0x100, it is necessary to write a value to IO_PAGE and access the Auxiliary address after changing the page. This is described in an application note with the filename, *RAA271005_I2C_PAGING_App-Note.pdf* (contact local sales office for copy).

4.4 SPI Serial Interface

The SPI interface is a general specification 4-wire auxiliary interface capable of operating at a clock speed of up to 26MHz. It is based on byte transfers. *Note*: There are two different auxiliary select pins in RAA271005/RAA271005L, (1) the regulation digital that is controlled by selection pin SS_B and (2) the protection digital that is controlled by SS_B2.

4.4.1 SPI Data Protocol

Both Read and Write SPI transactions begin when SS_B goes low and end when SS_B goes high.

4.4.1.1 Write Operation

To write to the RAA271005/RAA271005L, the Main must drive SS_B low, send the Control Byte, the register address, and the packet length (if IO_SPIMODE = 1), and finally as the data bytes are written, SS_B high is driven high to terminate the transaction (see Figure 8). The MSB of the Control byte is the R/W bit that must be set to write operation. Bit [6] AI indicates if it is going to be a single-byte write operation or a multi-byte write. Bit [1] and bit [0] of the Control byte indicate the page number of the register location that must be written (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address must be followed by an 8-bit packet length, which indicates the number of bytes to be written. Following the packet length field, the Main must send the data bytes. When all eight bits of data are received, they are written to the specified register address, and the RAA271005/RAA271005L increments the register address.

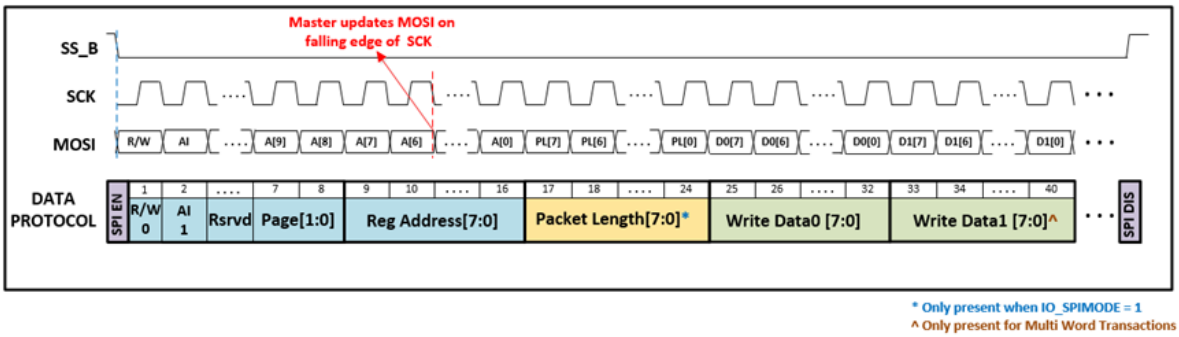


Figure 8. SPI Write Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

In single-byte transactions (AI = 0 or Packet length = 1), the RAA271005/RAA271005L goes into a wait state and waits for SS_B to go high.

In multi-byte transactions with IO_SPIMODE = 1, the RAA271005/RAA271005L writes the subsequently received data bytes to sequentially incremented addresses until the number of bytes are received as specified by the packet length;
next, the RAA271005/RAA271005L goes into a wait state to wait for SS_B to go high. For multi-byte transactions with IO_SPIMODE = 0 and AI = 1, the RAA271005/RAA271005L continues to write the subsequently received data bytes to sequentially incremented addresses until SS_B goes high. If SS_B goes high in the middle of a transaction, the transaction is terminated. The data byte is written if all eight bits are received.

4.4.1.2 Read Operation

To read from the RAA271005/RAA271005L, the Main must drive SS_B low and then send the Control Byte, followed by register address, packet length (if IO_SPIMODE = 1). Next, the RAA271005/RAA271005L sends the data bytes from the requested registers and finally the Main drives SS_B high to terminate the transaction. The MSB of the Control byte is the R/W bit that needs to be set to the read operation (see Table 3). Bit [6], AI indicates if it is going to be a single-byte read operation or a multi-byte read. Bits [1] and [0] of the Control byte indicate the page number of the register location be read (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address must be followed by an 8-bit packet length, which indicates the number of bytes to be written. Following the packet length field, the RAA271005/RAA271005L sends the data from the requested register. When all eight bits of data from the requested register address are sent, the RAA271005/RAA271005L increments the register address.

In a single-byte transaction, (AI = 0 or Packet length = 1), the RAA271005/RAA271005L goes into a wait state and waits for SS_B to go high.

In a multi-byte transaction with IO_SPIMODE = 1, the RAA271005/RAA271005L sends the data bytes from sequentially incremented addresses until a number of bytes are sent as specified by the packet length; next, RAA271005/RAA271005L goes into a wait state and waits for SS_B to go high. For multi-byte transactions with IO_SPIMODE = 0 and AI = 1, the RAA271005/RAA271005L keeps sending data bytes from sequentially incremented addresses until SS_B goes high.

Note: The MISO pin is pulled low while SS_B is high. The MISO pin is also low in FULL RUN but high during Deep Stop.

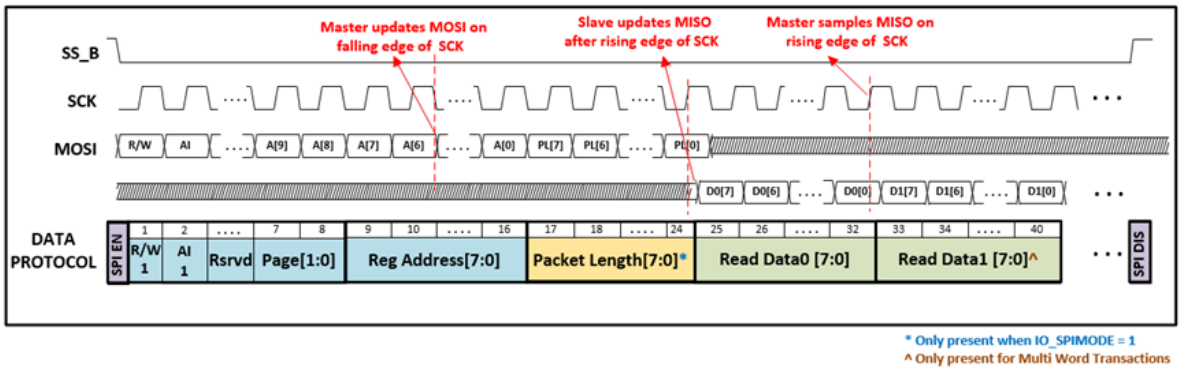


Figure 9. SPI Read Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

Table 3. Read/Write Bit Indicating Read or Write Operation

R/W	Read/Write Bit Indicating Read or Write Operation
AI	Auto Increment. 1 indicates multi-byte transfer, 0 indicates single-byte transfer.
Page	2-bit page address of the register to be written/read
Address	8-bit register address of the register to be written/read
Packet Length	8-bit packet length indicating number of data bytes to be transferred. Overrides AI when IO_SPIMODE = 1
Read Data	Data in the register at address, Address [7:0] + n
Write Data	Data to be written to the register at address, Address [7:0] + n

4.4.2 SPI Configuration

The following register bits configure the SPI operation:

- IO_SPICPOL – SPI clock polarity, RAA271005/RAA271005L is configured as active high, IO_SPICPOL = 0.
- IO_SPICPHA – SPI clock phase, RAA271005/RAA271005L samples data on rising edge of SPI clock, IO_SPICPHA = 0.

The four possible modes of clocking are shown in Figure 10.

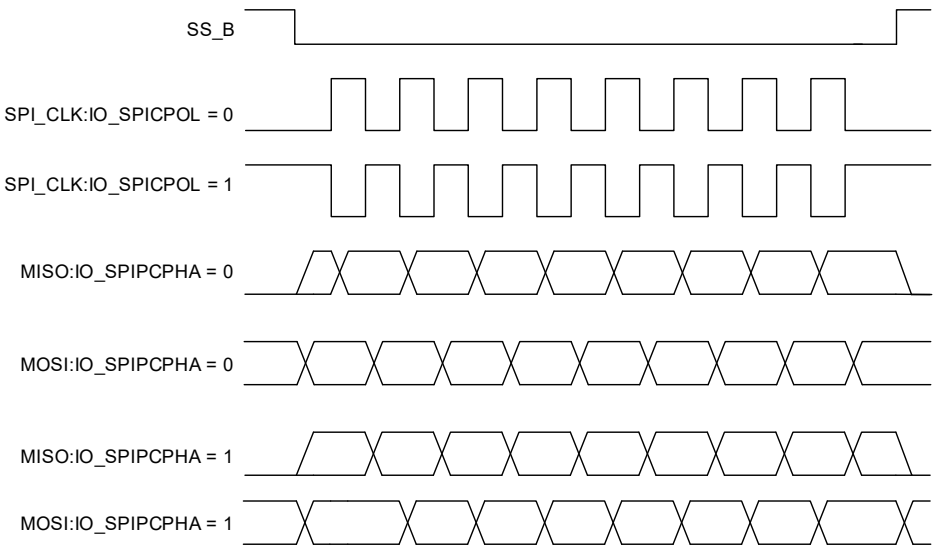


Figure 10. Four Possible Clocking Modes

- IO_SPIRWPOL – R/W bit polarity, RAA271005/RAA271005L SPI_RWPOL is set to 0, 1: Read, 0: Write.

Table 4. SPI_RWPOL R/W Bit Settings

SPI_RWPOL	R/W	Operation
0	0	Write
0	1	Read

- IO_SPIMODE – Packet length enable. The RAA271005/RAA271005L uses packet length mode by default, which means, the third data byte from Main is the packet length and indicates the total number of data words to be sent/received in a transaction.

4.4.3 SPI Timing

Figure 11 shows SPI timing for IO_SPICPOL = 0; IO_SPICPHA = 0. The timing values in Table 5 hold true for other values of IO_SPICPOL, and IO_SPICHPA.

Table 5. Timing Values

Parameter	Condition	Symbol	Min	Max	Units
Clock Period	-	t_1	38.4	-	ns
Enable Lead Time	-	t_2	12	-	ns
Enable Lag Time	-	t_3	12	-	ns
Clock High or Low Time	-	t_4	15	-	ns
Data Setup Time (Input)	-	t_5	12	-	ns
Data Hold Time (Input)	-	t_6	10	-	ns
Delay Time After Clock Edge (Output)	1.8V ≤ VIO ≤ 5.5V	t_7	5	35	ns
	3.3V ≤ VIO ≤ 5.5V		5	28	ns
Load Capacitance	-	C_L	-	10	pF

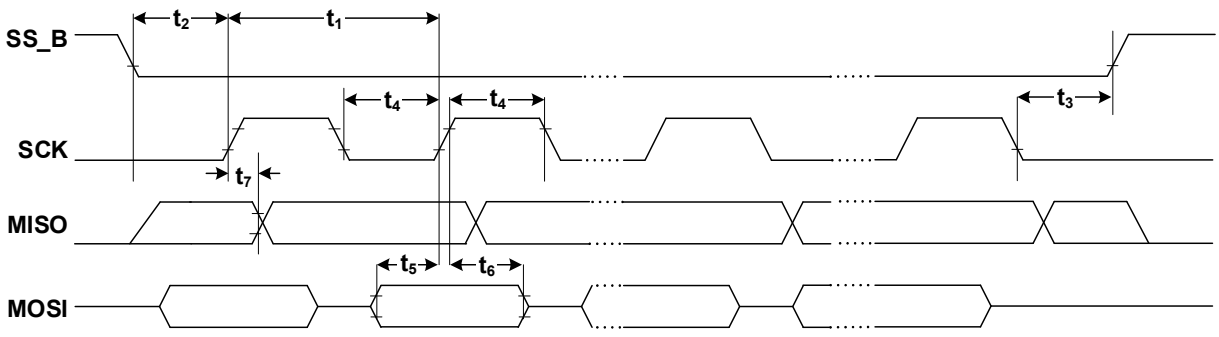


Figure 11. SPI Timing for IO_SPICPHA = 0, IO_SPICPOL = 0

4.5 I²C Interface

The I²C interface is a simple, bidirectional 2-wire bus protocol, consisting of the Serial Clock Control (SCL/I2C_CLK) and the Serial Data Signal (SDA/I2C_SDA). The RAA271005/RAA271005L hosts an Auxiliary I²C interface that supports data speeds up to 3.4Mbps. I2C_CLK is an input to the RAA271005/RAA271005L and is supplied by the controller, whereas SDA is bidirectional. The RAA271005/RAA271005L has an open-drain output to transmit data on SDA. *Note:* An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The RAA271005/RAA271005L uses a 7-bit hardware address scheme. Both regulation and protection digital have separate auxiliary addresses and each can be uniquely set by a onetime programmable fuse.

4.5.1 I²C Bus Operation

The chip supports 7-bit addressing. The RAA271005/RAA271005L I²C device address is reconfigurable through the OTP.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first. Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 14).

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The RAA271005/RAA271005L continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met.

Note: All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

An Acknowledge (or ACK), is a software convention that indicates a successful data transfer. The transmitting device, either Main or Auxiliary, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (Figure 14). The RAA271005/RAA271005L also responds with an ACK after recognition of a START condition, followed by a valid Identification (also known as I²C Address) Byte. The RAA271005/RAA271005L also responds with an ACK after receiving a Data Byte of a write operation. The Main must respond with an ACK after receiving a Data Byte of a read operation.

4.5.1.1 Write Operation

A Write operation requires a START condition, followed by an RAA271005/RAA271005L I²C Address byte with the R/W bit set to 0, a Register Address Byte, Data Bytes, and a STOP condition. After each byte, the RAA271005/RAA271005L responds with an ACK. After every data byte, the RAA271005/RAA271005L auto increments the register address so that subsequent data bytes are written to sequentially incremental register locations.

Note: A STOP condition that terminates the write operation must be sent by the Main after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, the write is not performed.

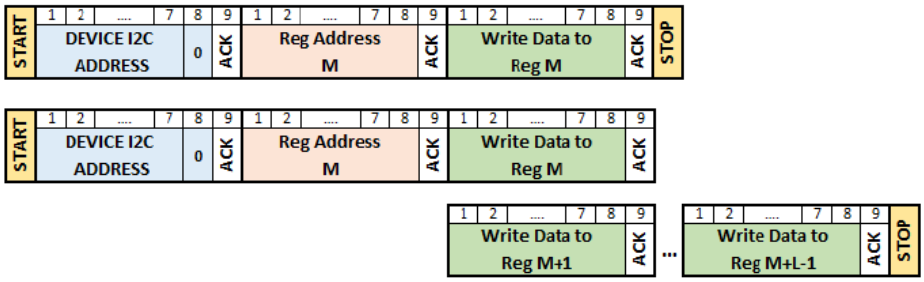


Figure 12. I²C Write Operation

4.5.1.2 Read Operation

A Read operation consists of a 3-byte dummy write instruction to send the register address to begin reading from, followed by a Current Address Read operation. The Main initiates the operation, issuing the following sequence: a START condition, followed by an RAA271005/RAA271005L I²C Address byte with the R/W bit set to 0, a Register Address Byte, a second START, and a second RAA271005/RAA271005L I²C Address byte with the R/W bit set to 1. After each of the three bytes, the RAA271005/RAA271005L responds with an ACK. Next, the RAA271005/RAA271005L transmits the data bytes. The Main terminates the Read operation from the RAA271005/RAA271005L by issuing a STOP condition following the last bit of the last data byte. After every data byte, the RAA271005/RAA271005L auto increments the register address so that subsequent data bytes are sent from sequentially incremented register locations.

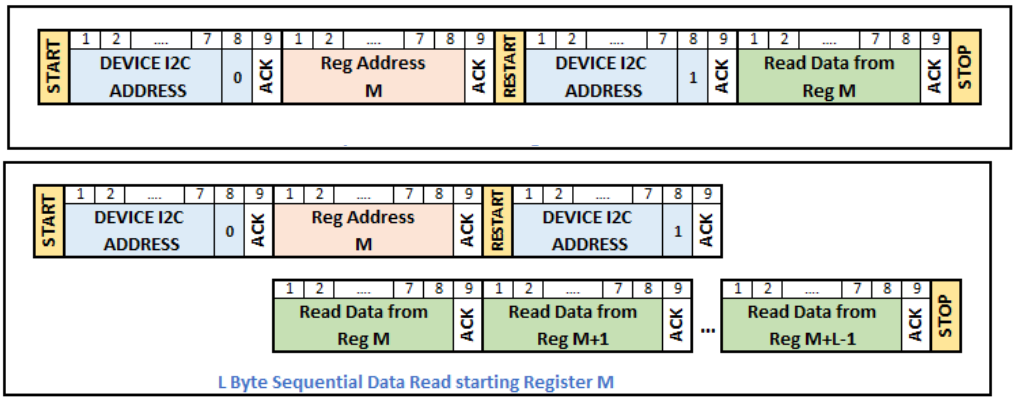


Figure 13. I²C Read Operation

4.5.2 I²C Timing

The timing specifications of the I²C I/O from the I²C spec are shown in Figure 14 and Table 6. The I²C controller provides an Auxiliary I²C transceiver capable of interpreting I²C protocol in Standard, Fast, Fast+, and High Speed modes.

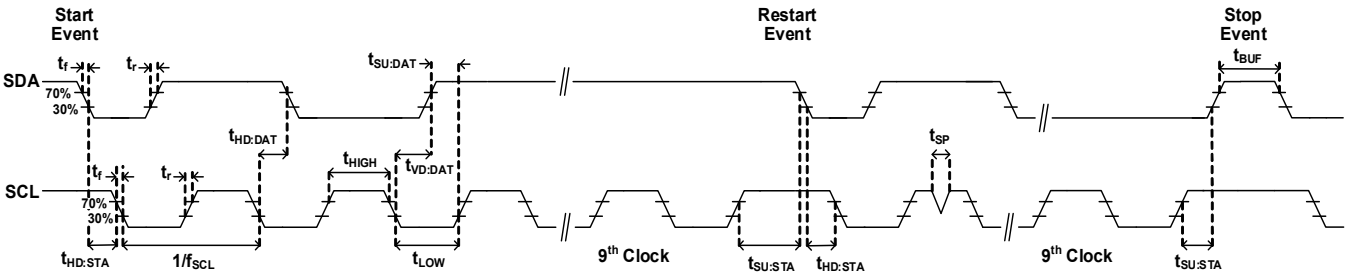


Figure 14. I²C Timing

Table 6. I²C Specification

Parameter	Symbol	Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	
Clock Frequency	f_{SCL}	0	400	0	1000	0	3400	kHz
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	t_{HD};STA	600	-	260	-	160	-	ns
LOW Period of the SCL Clock	t_{LOW}	1300	-	500	-	160	-	ns
HIGH Period of the SCL Clock	t_{HIGH}	600	-	260	-	60	-	ns
Setup Time for a Repeated START Condition	$t_{SU;STA}$	600	-	260	-	160	-	ns
Data Hold Time	$t_{HD;DAT}$	15	-	15	-	15	70	ns
Data Setup Time	$t_{SU;DAT}$	100	-	50	-	10	-	ns
Rise Time of SCL	t_{rCL}	-	300	-	120	-	40	ns
Fall Time of SCL	t_{fCL}	-	300	-	120	-	40	ns
Rise Time of SDA	t_{rDA}	20	300	-	120	10	80	ns
Fall Time of SDA	t_{fDA}	20 × (V_{DD}/5.5V)	300	20 × (V_{DD}/5.5V)	120	10	80	ns
Setup Time for STOP Condition	$t_{SU;STO}$	600	-	260	-	160	-	ns
Bus Free Time between a STOP and START Condition	t_{BUF}	1300	-	500	-	-	-	ns
Capacitive Load for each Bus Line	C_b	-	400	-	400		100	pF
Output Fall Time from VIHmin to VILmax	t_{of}	20 × (V_{DD} /5.5V)	250	20 × (V_{DD}/5.5V)	120	10	80	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	0	50	0	50	0	10	ns

4.6 Theory of Operation Overview

The RAA271005/RAA271005L uses multiple architectures for the DCDC converters each optimized for its operating conditions. An in-depth theory of operation can be found by looking at the Renesas website and other generic explanations available online and in books. Table 7 is an overview of each architecture used.

Table 7. DCDC Converter Default Architectures

DCDC Output	Architecture	Features
Buck1, Buck2	R5 Modulator Rapid Robust Ripple Regulator	▪ Best in class transient for large load steps ▪ Stable operating frequency steady-state ▪ Variable frequency during transients
Buck3, Buck4, and Buck5	Fixed Frequency Peak Current Mode	▪ Simplified over-current protection ▪ Better stability by reducing output to single pole ▪ Low Iq bias current and PFM light load efficiency

Buck1 and Buck2 are intended for large dynamic loads; therefore, the R5 modulator is implemented to give the best transient response with the least amount of output decoupling. Bucks 3 through 5 are for lower power and use peak-current mode as the modulator simplifying the integrated control circuit and allowing lower bias current for always-on rails.

Buck3 through Buck5 operate in PFM, Pulse Frequency Modulation (discontinuous mode or diode-mode), while Buck1 is always PWM/CCM, Pulse Width Modulation/Continuous Conduction Modulation mode. Buck2 uses frequency division lowering the switching frequency when in light load. See Buck Regulators, Buck[1-5] for additional programmable modes of operation for the buck regulators.

4.6.1 Buck2 DCM Operation Overview

Buck2 on RAA271005/RAA271005L provides the ability to automatically transition from Continuous conduction mode (CCM) into a discontinuous conduction mode (DCM) to increase light-load efficiency. This means that the low-side MOSFET channel conducts when the current is from the source to drain direction but does not allow current in the reverse direction. This emulates a non-synchronous buck with a free-wheeling diode. By preventing reverse current across the inductor, power loss can be reduced. In addition, BUCK2 does not rely on a fixed clock to set or reset PWM pulses. As a result, it can naturally skip pulses when necessary. When the load current is light, the switching frequency of the loop is lowered reducing the switching losses dramatically. With DCM mode enabled, when the inductor current reaches 0, BUCK2 makes the transition into DCM and the conduction time in this mode is governed by the DCM/CCM ratio setting.

A visual representation of the signals of interest in DCM is shown here in Figure 15:

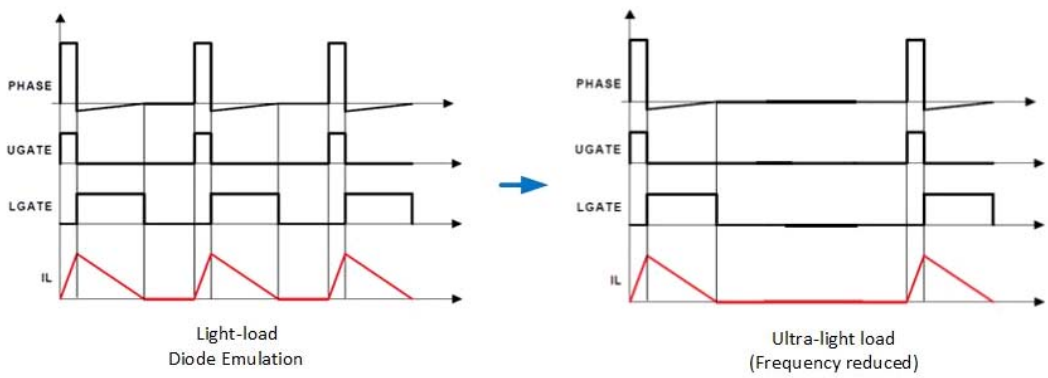


Figure 15. Buck2 DCM Waveform Example

4.6.2 Buck[3-5] PFM Operation Overview

In normal operation, the buck operates in Pulse Width Modulation (PWM) mode at a fixed frequency. If Force Continuous Conduction Mode (FCCM) is not enforced, when the load decreases to a preset level the buck enters Pulse Frequency Modulation (PFM) mode. When in PFM mode, the buck operates in a frequency which depends on load level. For each pulse, the HS FET turns on until the peak inductor current reaches a fixed level; next, the LS turns on until the inductor current reaches 0A. At this point, the power stage enters Tri-state until the next pulse happens. For each pulse with fixed peak inductor current, the output ripple voltage mainly depends on the inductor and capacitor values, which determines the amount of charge that needs to be delivered to the output capacitor.

When the load decreases, the output capacitor is discharged more slowly, and the buck stays in tri-state for a longer time before issuing another pulse. In other words, the switching frequency of the buck drops to save power. Alternately, when the load increases to a preset level where the maximum PFM frequency is reached, the buck enters PWM mode so that the buck is operating at higher but constant frequency. The peak inductor current is now controlled to be dependent on the load level.

Note: In PFM mode, there is no POC/NOC protection because the current sense block is disabled for power savings.

Note: The output voltage accuracy for Buck[3-5] in PFM mode is slightly different from PWM mode. Figure 16 and the following information show the factors involved:

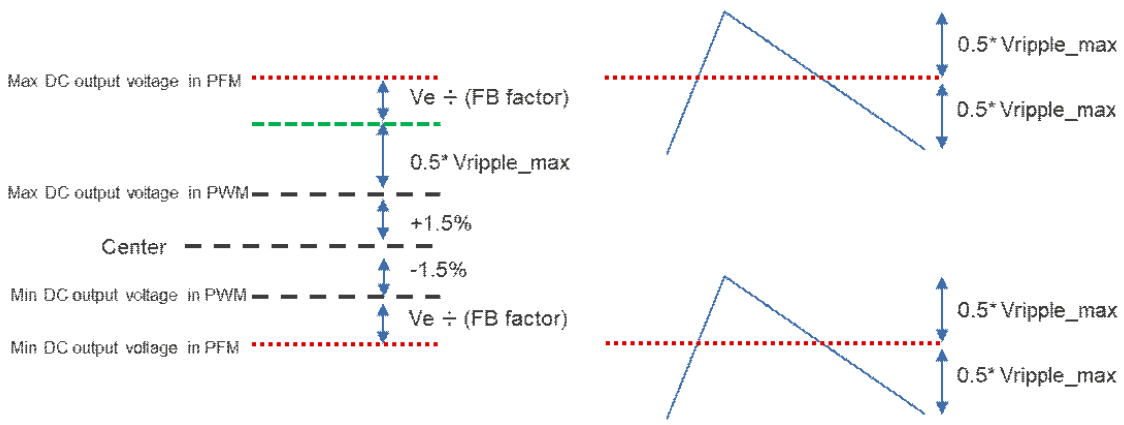


Figure 16. Buck[3-5] Output Voltage during PFM Mode

V_{OUT} DC Accuracy in PFM Mode:

Max = Max DC Output Voltage Accuracy in PWM + (Vripple_max)/2 + Ve/(VOUTFBDIV)

Min = Min DC Output Voltage Accuracy in PWM - Ve/(VOUTFBDIV)

- Max/Min DC Output Voltage Accuracy in PWM mode are specified in the Electrical Specifications table.
- Ve: 2mV Max which accounts for variations of internal blocks associated with PFM.
- VOUTFBDIV: 1.0, 0.75, 0.5, and 0.2 depending on OTP setting (see Buck Output Voltage Selection).
- Vripple (Ripple voltage) variation depends on BOM configuration, and peak inductor current variation.

Note: The output current at which the Buck[2-5] switches from PWM to PFM mode and back (PFM to PWM) depends on the given output voltage and BOM. The PWM to PFM threshold can vary with the input voltage, but for the given BOM and conditions in the Electrical Specifications table for Buck2 (V_{IN} = 5V, V_{OUT} = 1.1V, L = 240nH, C = 2×22µF), Buck[3-5] (V_{IN} = 5V, V_{OUT} = 0.83V, L = 220nH, C = 3×22µF), and the typical threshold (800mA for Buck2, 200mA for Buck[3-5]), the minimum threshold is 100mA for Buck2 and 50mA for Buck[3-5].

4.7 Recommended External Components and Considerations

Based on the operating option, the buck regulators can be used with a different minimum amount of output capacitance to maintain their load transient specifications. Table 8 shows the recommended BOM to achieve the best transient performance on each rail.

Table 8. Recommended BOM

Output	Cin	L	Minimum C_{OUT}[1]
BUCK1	4 × 10µF + 4 × 2.2µF + 4 × 0.1µF	100 ~ 330nH	4x47µF + HF Bypass
BUCK2	10µF + 0.1µF	220 ~ 470nH	1x22µF + HF Bypass
BUCK3	10µF + 0.1µF		
BUCK4	10µF + 0.1µF		
BUCK5	10µF + 0.1µF		
LDO1,2,3,4	-	-	2.2µF
LDO5,6	-	-	1µF
LDOIN1, LDOIN2, LDOIN3	1µF + 0.1µF	-	-

1. Maximum C_{OUT} (LDO) = 10µF

Other recommended values for miscellaneous RCs are shown on the reference schematic in Figure 17.

Note: ADC3-5 pins are changed to become outputs and these outputs are low during CVM test in SoC activation. If any external device output is connected directly to ADC3-5 and not through an external mux, the output of the external device has a low impedance path to ground during this time. If the output of the device cannot withstand this, it is suggested to put 10k resistor before the ADC3-5 input pin.

Note: For proper usage of the SDO pins, external pull-ups or pull-downs are required to avoid floating conditions on these signals. Refer to section 10.1 in the *Safety Application Note*.

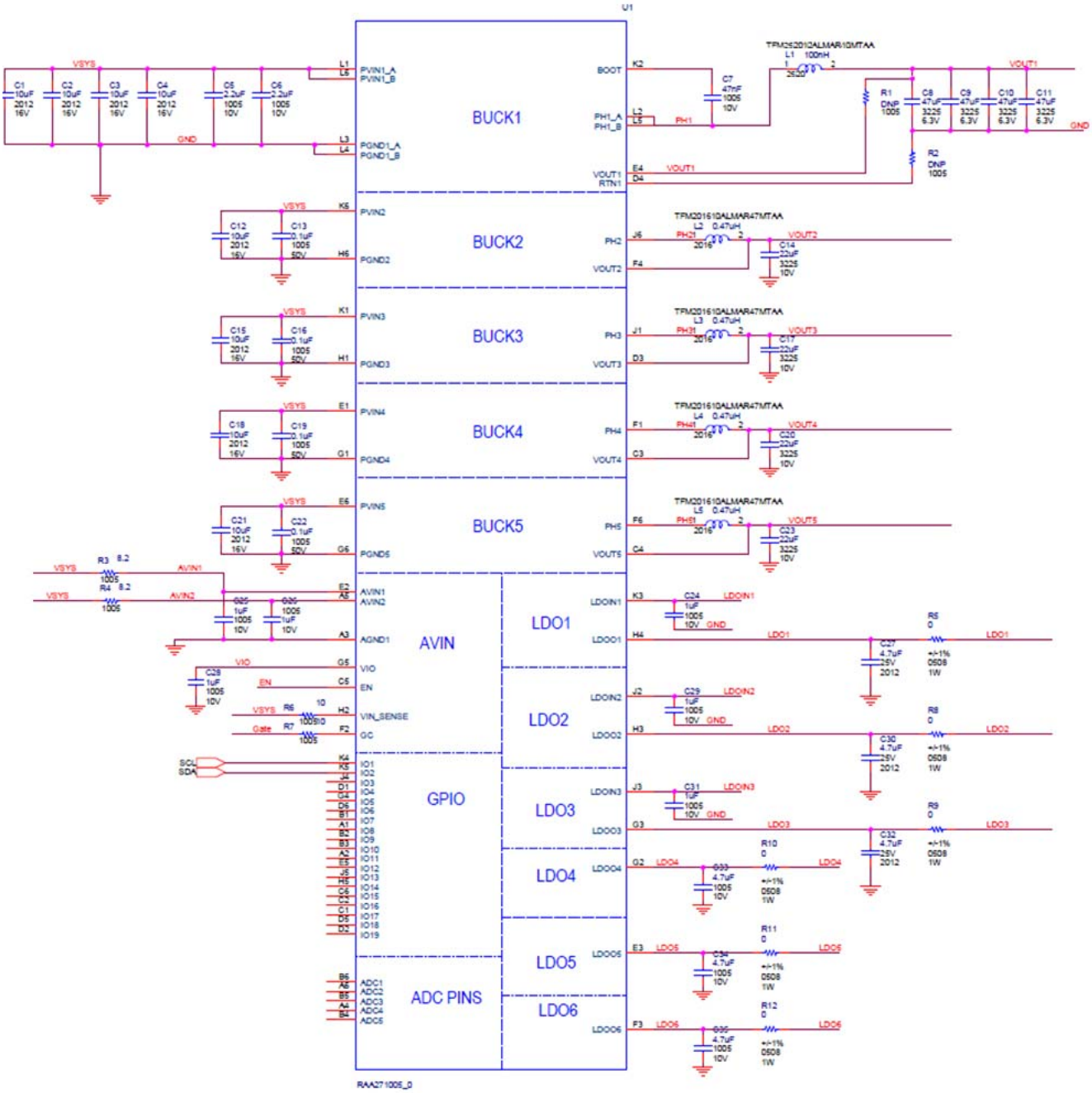


Figure 17. Reference Schematic

4.8 Layout Guidelines

4.8.1 Laying out Buck[1-5]

1. Place the input capacitors as close as possible to the Buck's PVIN and PGND pins with the least impedance routing
2. Connect all PGND pins together through GND copper plane and use multiple vias connecting the inner and other GND layers.

3. Connect the Buck-1 PH1 pins together through a PH1 copper plane on the PMIC component layer.
4. Place inductors as close as possible to the PMIC.
5. Place the output bulk capacitor COUT1 close to the inductor L1 output terminal.
   a. Minimize the GND distance of the input capacitor CIN1 and the output capacitor COUT1. If CIN1 GND plane and CIN2 GND plane cannot be connected directly with copper, use enough vias connecting them to the inner or other GND plane respectively so that the two GND planes can be connected through the other GND layers with minimized resistance.
   b. Solid ground plane is helpful for a good EMI performance, current conduction, and thermal dissipation.
6. If possible, use two or multiple layer or wide enough PCB copper trace for the output voltage VOUT1 to minimize the conduction loss, because Buck-1 output carries high current.

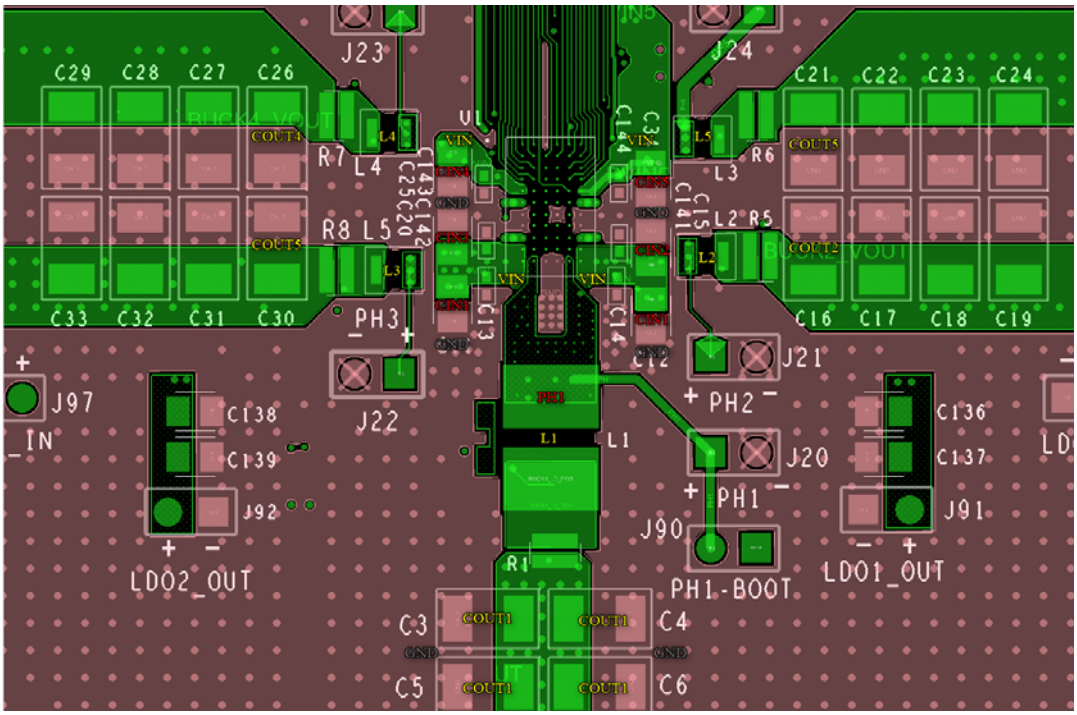


Figure 18. Top Layer

7. For the Buck-1 bootstrap cap CBOOT (recommended 47nF), place it on the PCB bottom component layer.
   a. Use a via connecting BOOT pin to the bottom layer and use a via connecting PH1 net to the bottom layer.
   b. Minimize the loop and the PCB trace of Boot pin → Boot trace → Cboot → PH1 trace.
   c. Use at least a 10 mil width trace for the Boot trace and PH1 trace to conduct the Buck-1 high-side FET driver current.
   d. Keep all other smaller signals away from BOOT and PH1 via/trace/copper.

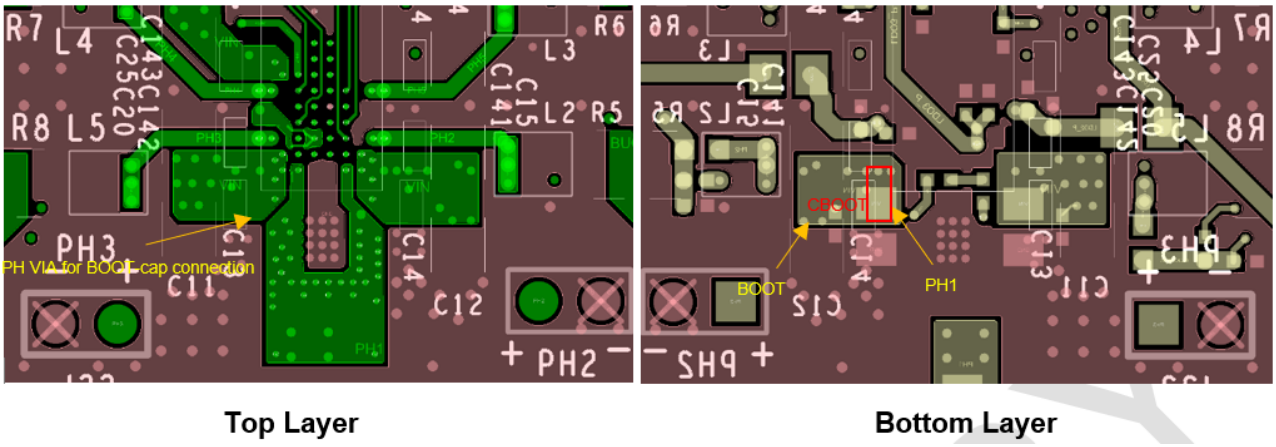


Figure 19. Top and Bottom Layer

8. Run the VOUT1 and RTN1 output voltage feedback differential trace in parallel, staying away from the PH1, PH2, PH3, PH4, PH5, and BOOT nets noisy signal via/trace/copper, and away from any high-speed digital signals. Shield the VOUT1 and RTN1 differential parallel traces with GND copper.

Important: Limit the impedance for the VOUT1 and RTN1 traces to less than 100mΩ. This is because the discharge resistor and discharge detect circuit inside the PMIC staying within the electrical specifications for these functions.

9. Connect the VOUT1 and RTN1 differential sensing point to the VOUT1 output high-frequency ceramic cap bank to minimize the feedback ripple and noise.

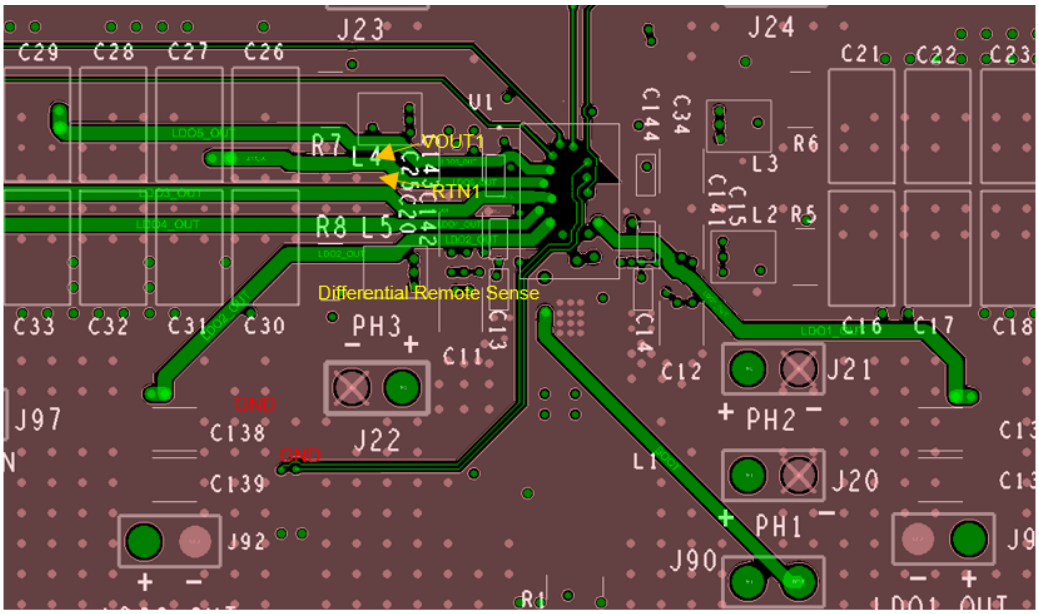


Figure 20. Differential Remote Sense

10. Use the inner layer or bottom layer to run the PH traces, connect to the PH pin and inductor pad through multiple vias.
    a. The PH trace should be wide enough to carry the output current.
    b. Avoid any sensitive signal close to the PH trace and via.

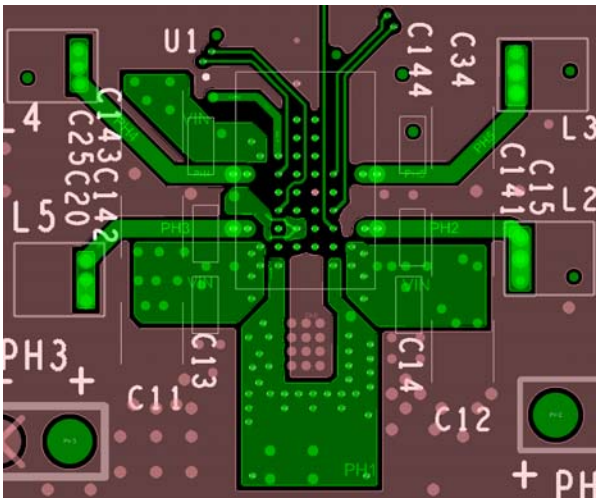


Figure 21. PH Trace

4.8.2 All Other Components Placement and PCB Routing

1. Place the LDOIN1, LDOIN2, LDOIN3 input capacitors as close as possible to the pins
2. Place the LDO1-6 output capacitors as close as possible to the LDO1-6 output pins, respectively.
3. Place the AVIN1 pin and AVIN2 pin R-C filter capacitor as close as possible to the AVIN1 and AVIN2 pins, respectively. Always reference the decoupling capacitor GND pad to a quiet GND plane.
4. Run the ADCs and GPIOs digital traces away from the PH1/2/3/4/5 and BOOT noisy signal via/trace/copper

4.8.3 PCB Thermal Considerations

The indicated thermal impedances θ_{JA} and θ_{JC} are determined using JEDEC standard testing as noted in the Recommended Operating Conditions, but additional improvements can be made using either or both of the listed recommendations. *Note:* These recommendations should be considered if the RAA271005/RAA271005L is being used to supply a large amount of power from its combined outputs and the junction temperature of the device is too high:

- Providing more PCB copper (larger shapes and/or adding layers) to dissipate more heat from the bottom of the device.
- Provide airflow over the top of the device and/or add a heatsink attached to the top of the package. The thermal resistance of the package molding material is sufficient enough to allow a heatsink to be used this manner.

5. Power Management Features

5.1 Buck Regulators, Buck[1-5]

RAA271005/RAA271005L includes five DC/DC buck step-down regulators. Each regulator has an output voltage adjustable by using a 10-bit DAC and a feedback divider.

For Buck1 and Buck2, the frequency of each buck can be set to hysteretic (varying frequency), fixed frequency, or pseudo-random spread spectrum frequency. Of these three options, hysteretic mode offers the best transient performance, and it is the default mode set in OTP.

Buck3, Buck4, and Buck5 are peak current mode control regulators, which the peak of the inductor current is controlled cycle by cycle, allowing for current limiting against overcurrent conditions without an additional control loop. Buck1 operates in forced PWM mode whereas Buck[2-5] have capability to operate in PFM mode at light loads when set through OTP. Buck[3-5] are the low Iq bucks that offer the lowest quiescent current when operating in PFM mode at light load.

Note: With the RAA271005/RAA271005L R5 hysteretic modulator mode, a stable switching frequency is achieved in steady state while allowing variable frequency and duty cycle in response to transients. For designs that have low-noise layout (careful to keep sense lines away from large signals and make use on an analog ground that is connected to PGND away from the power stage), the IC limits are ±15%. However, this is not always possible when high-frequency noise enters the feedback loop and one can see up to ±25% or ±30% frequency variations. This is not an issue for the R5 modulator because it is stable over this range of switching frequencies and the frequency changes seen during transients.

5.1.1 Buck Output Voltage Selection

The output voltage for each buck regulator is set by a feedback divider and a 10-bit DAC. While the feedback divider ratio is factory programmed, the DAC value can be changed by adjusting the values of BUCKx_DVS0VOUT92 and BUCKx_DVS0VOUT10. These values are the top eight bits and lower two bits of the 10-bit DAC, respectively. For the output voltage to change, the value of BUCKx_DVS0VOUT10 must be written.

For Buck1 only, there is a value for the second DVS code in BUCK1_DVS1VOUT. More details on Buck1 DVS are described in the Buck Dynamic Voltage Scaling section.

The output voltage for each buck based on the FB divider setting used is shown in Equation 1. *Note:* To ensure proper regulation, the buck output voltage must be set to a value between 0.3V and 3.3V.

(EQ. 1) $$V_{BUCK} = \frac{1.223 \times DAC[9:0]}{(1023) \times VOUTFBDIV}$$

Where DAC is the 10-bit Buck DAC code and FBDIV is the feedback divider value. *Note:* FBDIV can be factory programmed to a value of 1, 0.75, 0.5, or 0.25.

Note: There is a minimum limit to the output voltage that can be regulated to. This is because of the minimum on-time of the buck, the switching frequency of the regulator, and the input voltage. This limit is the worst at no-load because the duty has to increase to compensate for losses, so the following equation explains the V_{OUT} limit at no-load:

(EQ. 2) $$V_{OUT\text{-}MIN} = T_{MIN\text{-}ON} \times F_{SW\text{-}MAX} \times V_{IN\text{-}MAX}$$

It is best to check what this limit is and if it is not low enough then look at changing the f_{SW} or V_{IN} maximum limits.

5.1.1.1 Buck DAC Step Size

The step size for each DAC code in () can also be rewritten as mV/bit as shown in Table 9.

Table 9. Buck DAC Step Size

VOUTFBDIV Value	DAC Step Size (mV/bit)
1.0	1.195
0.75	1.594
0.5	2.391
0.25	5.977

5.1.2 Buck Regulator Startup Ramp Rate

The rate at which the buck regulators ramp up during startup can be factory programmed to different options. This ramp rate depends on the voltage range used for the buck regulator and therefore, the value of VOUTFBDIV. Table 10 shows the factory programmable startup ramp rate options.

Table 10. Buck Regulator Ramp Rate Options

VOUTFBDIV Value	Option Number	Buck Ramp Rate (mV/µs)
1	0	1.2
1	1	3
1	2	7.1
1	3	14.2
1	4	6
1	5	12
0.75	0	1.6
0.75	1	3.2
0.75	2	6.3
0.75	3	12.6
0.5	0	1.2
0.5	1	2.4
0.5	2	6
0.5	3	12
0.2	0	1.5
0.2	1	3
0.2	2	7.4
0.2	3	14.8

5.1.3 Buck Dynamic Voltage Scaling

While all buck regulators can change output voltage by changing the DAC value, Buck1 has several options to achieve DVS. There are two independently programmable voltage settings for the Buck1 controller, which can set the output voltage. These settings are DVS0 and DVS1. By changing the DVS number selected, the corresponding output voltage is selected. There are two methods to select the DVS output voltage.

- Method 1 – Use internal registers to select DVS by writing to the BUCK1_DVSSELECT bit in the BUCK1_DVSSEL register using SPI or I^2C. To use this method, the BUCK1_DVSCTRL bit has to be set to 0b0

for the corresponding buck. The BUCK1DVSSELECT bit allows you to switch between the two different DVS settings, each corresponding to a set of DVS registers holding the DVS information.

For example, DVS0 corresponds to BUCK1_DVS0VOUT92[7:0] and BUCK1_DVS0VOUT10[1:0]. The two register values combined represent the complete 10-bit DAC code for DVS0.

- Method 2 – Using the GPIO6 pin to achieve DVS, there are two variations depending on the IO_PINMODE register setting. See Table 1.

Note: To use DVS using the GPIO/MPIO pins requires IO_PINMODE to be OTP programmed before a start-up boot sequence is initiated.

Note: On-the-fly programming is not recommended for the following configurations. (i) IO_PINMODE = 1 or 3: DVFS pin available.

5.1.4 Buck Regulator Protection Features

5.1.4.1 Positive Overcurrent Protection (POC)

Buck[1-5] have positive overcurrent feature. For Buck[1-2], the HS FET has filtered sampled current limits. Buck[3-5] HS FET use a cycle-by-cycle current limit. The reaction to these faults is programmable and the fault reactions can be masked through the mask registers. When the fault reactions are not masked and the rail trips an POC fault, the outputs are tri-stated immediately, and the fault is reported to the digital to which the protection block responds by going to the error state after which all rails are disabled.

Note: Buck1 is rated for a higher output current of 12A(RAA271005), 6A(RAA271005L). The POC response time is up to 2.5µs for a 1-5A/µs load slew-rate so one needs to set the POC level such that the output current never exceeds 20A by the time the POC responds.

Note: Buck2 is rated for an output current of 2.5A. The POC response time is up to 2.5µs for a 1-5A/µs load slew-rate so it is required to set the POC level so that the output current never exceeds 8A peak by the time the POC responds. Buck[3-5] has cycle-by-cycle overcurrent detection, and HS FET turns off when the inductor current reaches the OC trip point. The POC response time depends on PVIN, V_{OUT}, inductor value (L). For example, when PVIN = 5V, V_{OUT} = 0.8V, L = 240nH, OC comparator delay is up to 25ns. The POC level should be set so that the output current never exceeds 8A peak by the time the POC responds.

5.1.4.2 Negative Overcurrent Protection (NOC)

Buck[1-5] have negative overcurrent feature. The LS current sense detects the NOC threshold. The fault reaction to the NOC is programmable through OTP/mask registers. When the fault reactions are not masked and the rail trips an NOC fault, the outputs are tri-stated immediately, and the fault is reported to the digital to which the protection block responds by going to the error state after which all rails are disabled.

5.1.4.3 Output OV/UV

Buck[1-5] have OV/UV comparator with programmable thresholds. The OV/UV comparator tracks the output voltage of the buck and when the VOUT crosses above the programmed OV threshold, trips an OV fault. When VOUT dips below the UV threshold, it trips an UV fault. When the fault reactions are not masked and the rail trips an OV/UV fault, the outputs are tri-stated immediately, and the fault is reported to the digital to which the protection block responds by going to the error state after which all rails are disabled.

Note: Typical detection reaction times for various conditions are provided in the Electrical Specifications section but expected maximum times for these same conditions are indicated here for reference:

Buck UVP detection time maximum values:

BUCKx_VOUTFBDIV[1:0] = 0b00, V_{OUT} = 0.8V, 1mV/µs; 11.9µs

BUCKx_VOUTFBDIV[1:0] = 0b11, V_{OUT} = 3.3V, 1mV/µs; 23.6µs

Buck OVP detection time maximum values:

BUCKx_VOUTFBDIV[1:0] = 0b00, V_{OUT} = 0.8V, 1mV/µs; 7.7µs

BUCKx_VOUTFBDIV[1:0] = 0b11, V_{OUT} = 3.3V, 1mV/µs; 18.8µs

5.1.4.4 Regulation Over-Temperature Fault and Warning

Regulation block contains an over-temperature protection with a programmable rising (OTR) and falling (OTF) threshold. When the fault reactions are not masked and the rail trips an OT fault, the outputs are tri-stated immediately, and the fault is reported to the digital to which the protection block responds by going to the error state after which all rails are disabled. The temperature must fall again below the falling threshold, to be able to re-enable the PMIC. In a real system, set the protection thermal sensors to detect the over-temperature fault first.

5.1.4.5 Buck Regulators Spread Spectrum Operation

Buck regulators support quasi-random spread spectrum operation in fixed frequency mode to reduce emissions. This mode is implemented using a divided version of the internal oscillator while modulating control bits to rapidly adjust the oscillator center frequency.

Note: The center frequency used in spread spectrum mode is factory programmable (same as fixed f_{sw} setting).

The frequency deviation in fixed frequency mode can be factory programmed between ±3.5% to ±1%. There is also a dwell (or pause) time that keeps the oscillation to a fixed frequency for a certain period. The dwell time can be fixed or random in time.

The full list of factory programmable options in spread spectrum mode are listed here in Table 11, Table 12, and Table 13. If spread spectrum is selected, Buck3, 4, and 5 regulators are applied spread spectrum operation. Buck1 and 2 can be chosen either spread spectrum or hysteretic mode.

Table 11. Spread Spectrum Amplitude Options

Maximum Frequency Deviation (%)	Option Number
1	0
2	1
3	2
3.5	3

Table 12. Spread Spectrum Direction Options

Direction	Option Number
Spread spectrum disabled	0
Downwards only (-)	1
Centered (+ and -)	2
Upwards only (+)	3

Table 13. Spread Spectrum Frequency Dwell Settings

Dwell Setting	Option Number
Random dwell for 0 to 1.75µs	0
Random dwell for 0 to 3.75µs	1
Random dwell for 0.75 to 7.75µs	2
Random dwell for 0 to 15.75µs	3
Fixed dwell for 1.75µs	4
Fixed dwell for 3.25µs	5
Fixed dwell for 7.75µs	6
Fixed dwell for 14.25µs	7

5.1.5 DCDC5/Buck5 Configured as Boost

DCDC5 regulator can be configured as an asynchronous mode. The HS FET is disabled, and an external diode is used for the asynchronous operation. In Boost mode, VOUT5 becomes the input of the boost and PVIN5 is the output of the boost. Boost feature can be enabled using OTP.

5.1.6 Buck3 and Buck4 Merged Mode for 5A Buck

These two bucks can be set to be merged to make a single 5A Buck Regulator. When done, the power stage FETs are connected in parallel with only one control loop active. The output pins for each are then connected together (PVIN, PH, PGND) and behave as a single buck regulator. The output specifications are double that of each Buck3 and Buck4.

5.2 LDO Regulators, LDO[1-6]

RAA271005/RAA271005L includes 6 LDOs (4×75mA, and 2×500mA). The output of each LDO[1-4] can be set to 1.8V or 3.3V while LDO[5-6] is programmed by an 8-bit DAC and each output is independent. LDO[1-6] have 3 separate power inputs at pins LDOIN1, LDOIN2, and LDOIN3. The output of each LDO[1-4] should be connected to a 1µF filtering capacitor, and LDO[5-6] should be connected to a 4.7µF filtering capacitor.

Renesas does not recommend operating the LDO[1-4] with a large dropout voltage (LDOIN - LDOOUT) and a high current. The power dissipated by each LDO must be less than 600mW. This power can be calculated using Equation 3:

(EQ. 3) $$P_{DISS} = (V_{LDOIN} - V_{LDOO}) \times I_{OUT}$$

5.2.1 LDO Output Voltage, LDO[1-4]

LDO[1-4] can be set to an output voltage of 1.8V or 3.3V.

5.2.2 LDO Output Voltage, LDO[5-6]

Both LDOs can be set to an output voltage of 0.6V to 3.6V in 15.35mV steps. The output voltage is set by the 8-bit DAC value in registers LDO5_VOUT_CORE and LDO6_VOUT_CORE for LDO5 and LDO6 respectively and each output is independent. The LDO output voltage for LDO5 or LDO6 follows Equation 4.

(EQ. 4) $$VLDO = \frac{3.2 \times 1.223 \times DAC[7:0]}{(255)}$$

Note: The output voltage of the LDO must be set above 0.6V to ensure proper operation.

5.2.3 LDO Startup Ramp Rate

Like the buck regulators, LDO[1-6] starts up with a factory-programmed ramp rate based on Table 14 and Table 15.

Table 14. LDO[1-4] Ramp Rate Options

Option Number	1.8V Ramp Rate (mV/µs)	3.3V Ramp Rate (mV/µs)
0	8.56	15.68
1	4.28	7.84
2	2.14	3.92
3	1.07	1.96
4	0.53	0.98
5	0.27	0.49
6	0.13	0.25

Table 15. LDO[5-6] Ramp Rate Options

Option Number	Ramp Rate (mV/µs)
0	15.4
1	7.7
2	3.9
3	2
4	1
5	0.5
6	0.2

5.2.4 LDO Protection Features

5.2.4.1 LDO UV Fault

Each LDO[1-6] implements an output UV comparator. When the LDO output dips below the programmed UV threshold, the comparator trips on a LDO UV fault. When the LDO UV fault reaction is not masked and the rail trips an LDO UV fault, the output is tri-stated immediately, the fault is reported to the digital, the protection block responds by going to the error state, and finally, all the rails are disabled.

Note: Typical detection reaction times for various conditions are provided in the Electrical Specifications section but expected maximum times for these same conditions are indicated here for reference:

- LDO UVP detection time maximum values:
  - 1.8V Output, 6% setting, 5mV/µs; 14.3µs
  - 3.3V Output, 6% setting, 5mV/µs; 11.5µs

5.2.4.2 LDO OC fault

Each LDO[1-6] implements an OC detection. Although the OC does not trip a fault but limits the current, the LDO can sustain, and therefore, eventually causes a UV fault to protect the system.

5.3 Discharge and Discharge Detect Feature

When the rails in RAA271005/RAA271005L are disabled either due to a fault or loss of EN, the internal pull downs are enabled and the outputs discharge.

In addition, the RAA271005/RAA271005L implements a discharge detect feature. When enabled, this feature ensures that output voltage of any disabled regulator reaches OTP programmable voltage level before it can start-up again. A disable request can either come from a normal system event such as entering into Deep Stop mode or from a fault event (OV, OC, and others).

Note: When DCDC5 is configured as a boost regulator, the discharge detect feature is not available for the output on this regulator since the output can not be discharged below the input supply voltage.

During the shutdown process, a UV detection block of the corresponding regulator is used with a user-chosen reference, and it stays enabled for programmable DISC_TOUT duration. If the required discharge level is reached before DISC_TOUT expires, the system allows the regulator to be powered-up again (Figure 22).

If one or more regulators do not reach the discharge level and DISC_TOUT expires, associated fault reporting register bits are set and the PMIC either allows regulator(s) to restart or latch-off based on the FLT_CTRL_DISC_DET setting (Figure 23).

If the disable event is triggered by the EN pin and the EN pin level is low at the completion of DISC_TOUT, all regulators are disabled regardless of the FLT_CTRL_DISC_DET option selected. The PMIC also goes to a power-off state and the register content is lost.

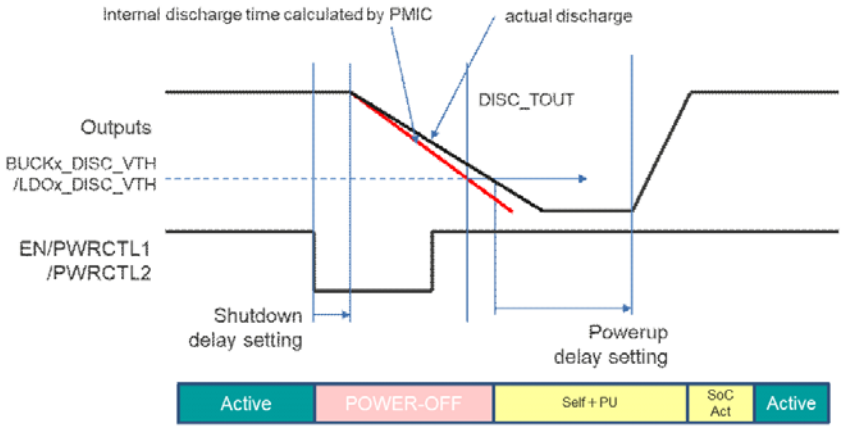


Figure 22. Discharge Detect (No Fault)

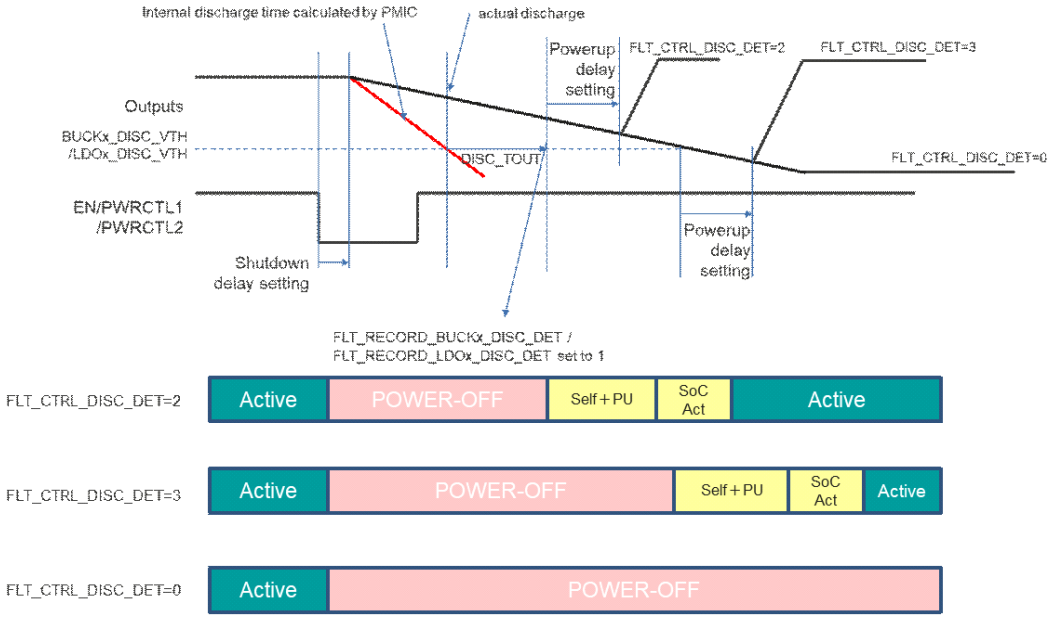


Figure 23. Discharge Detect (Fault)

Table 16. Discharge Detect Programmable Options

Option	Description
EN_DISC_DET	1: Discharge detect feature is enabled for all regulators 0: Discharge detect feature is disabled
BUCKx_DISC_VTH/LDOx_DISC_VTH	Discharge level selection 150mV, 200mV, 250mV, 300mV
DISC_TOUT	Timer selection for how long UV detection stays on. LDO: 1ms, 5ms, 10ms, 20ms, 40ms, 60ms, 100ms, 150ms BUCK: 1ms, 5ms, 10ms, 20ms, 32ms, 112ms, 112ms, 112ms
FLT_CTRL_DISC_DET	2: Restart 1: Reserved 0: Latch-off all
FLT_RECORD_BUCKx_DISC_DET / FLT_RECORD_LDOx_DISC_DET	1: Discharge detect fault is detected for the rail 0: No discharge detect fault

FLT_CTRL_DISC_DET Options:

- 0: If a DISC_DETECT failure occurs, all regulators are shut down and kept disabled including the rails that were not part of the initial shutdown request. For example, discharge failure in PWRCTL1/2 rails when going into Deep Stop also causes the Always On rails to shutdown.
- 1: Reserved
- 2: Regulators restart when discharge detect timer expires even if the discharge fault is detected (assuming all other enable conditions are met).
- 3: Equivalent to infinite DISC_TOUT timer. Regulators restart only if and when threshold crossing is achieved. Slight increase in Iq should be expected when this option is selected as discharge detect related circuitry stays enabled.

5.4 Fault Reactions

The Buck and LDO regulators have several faults that they can report and react.

Table 17. Fault Reactions

Fault Name	Regulator Type	Reaction	Description
Overvoltage	Buck only	Does nothing.	Ignore the fault.
		Shuts down this buck.	Force the buck to disable.
		Shuts down all regulators.	Force all regulators to disable.
Undervoltage	Buck and LDO	Does nothing.	Ignore the fault.
		Shuts down this regulator.	Force the regulator to disable.
		Shuts down all regulators.	Force all regulators to disable.
High-Side Positive Overcurrent Limit	Buck only	Does nothing.	Ignore the fault.
		Shuts down this regulator.	Force the buck to disable.
		Shuts down all regulators.	Force all regulators to disable.
Low-Side Negative Overcurrent Limit	Buck only	Does nothing.	Ignore the fault.
		Shuts down this regulator.	Force the buck to disable.
		Shuts down all regulators.	Force all regulators to disable.
Regulation Over-Temperature Protection	Buck and LDO	Does nothing.	Ignore the fault.
		Shuts down this regulator.	Force the buck to disable.
		Shuts down all regulators.	Force all regulators to disable.

5.5 Regulation Interrupts

Regulation faults causing Interrupts can be individually masked by changing the bits in the FLT_MASK* registers and faults can be read through the FLT_RECORD* registers.

Note: Both registers exist in the regulation register map, Table 18 shows a list of the individual faults that can trigger the IRQ# pin.

Table 18. Regulation Fault Signals

Description	Register Map Name	Maskable?	Notes
OTP Program Warning	OTPPROGWARN	Y	Not used by user
OTP Programming Address Fault	OTPPROGADDR	Y	Not used by user
OTP Programming Fault	OTPPTOG	Y	Not used by user
OTP Initial Failure	OTPINIT	Y	OTP download engine failed to complete
OTP CRC Failure 2	OTPCRCPAGE2	Y	CRC failure bit [2]
OTP CRC Failure 1	OTPCRCPAGE01	Y	CRC failure bit [1]
OTP Read Duration Fault	OTPTIMEOUT	Y	OTP Read duration > ~8msec
OTP Not Programmed Fault	OTPNOTPGMD	Y	-
Boot Occurred	FLT_BOOT	Y	Indicates that boot process has occurred
Over-Temperature Rising	TEMPSDR	Y	Indicates that the over-temperature block in the regulation area is over its threshold value (rising threshold)

Table 18. Regulation Fault Signals (Cont.)

Description	Register Map Name	Maskable?	Notes
Over-Temperature Falling	TEMPSDF	Y	Indicates that the over-temperature block in the regulation area has fallen below the threshold (falling threshold, Shutdown - Hysteresis)
Buck1 Low-Side Negative Overcurrent (NOC)	BUCK1_UC	Y	-
Buck1 High-Side Positive Overcurrent (POC)	BUCK1_OC	Y	-
Buck1 Overvoltage	BUCK1_OV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is +60mV, +100mV, +150mV, or +250mV Factory programmable threshold for all other Vout range settings is +100mV, +150mV, +200mV, or +250mV
Buck1 Undervoltage	BUCK1_UV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is -60mV, -100mV, -150mV, or -250mV Factory programmable threshold for all other Vout range settings is -100mV, -150mV, -200mV, or -250mV
Buck2 Low-Side Negative Overcurrent (NOC)	BUCK2_LSWUC	Y	-
Buck2 High-Side Positive Overcurrent (POC)	BUCK2_HSWOC	Y	-
Buck2 Overvoltage	BUCK2_OV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is +60mV, +100mV, +150mV, or +250mV Factory programmable threshold for all other Vout range settings is +100mV, +150mV, +200mV, or +250mV
Buck2 Undervoltage	BUCK2_UV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is -60mV, -100mV, -150mV, or -250mV Factory programmable threshold for all other Vout range settings is -100mV, -150mV, -200mV, or -250mV
Buck3 Low-Side Negative Overcurrent (NOC)	BUCK3_LSWUC	Y	-
Buck3 High-Side Positive Overcurrent (POC)	BUCK3_HSWOC	Y	-
Buck3 Overvoltage	BUCK3_OV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is +60mV, +100mV, +150mV, or +250mV Factory programmable threshold for all other Vout range settings is +100mV, +150mV, +200mV, or +250mV
Buck3 Undervoltage	BUCK3_UV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is -60mV, -100mV, -150mV, or -250mV Factory programmable threshold for all other Vout range settings is -100mV, -150mV, -200mV, or -250mV
Buck4 PVIN OK	BUCK4_PVIN_OK	Y	Indicates whether there is a fault on PVIN4
Buck4 Low-Side Negative Overcurrent (NOC)	BUCK4_LSWUC	Y	-
Buck4 High-Side Positive Overcurrent (POC)	BUCK4_HSWOC	Y	-

Table 18. Regulation Fault Signals (Cont.)

Description	Register Map Name	Maskable?	Notes
Buck4 Overvoltage	BUCK4_OV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is +60mV, +100mV, +150mV, or +250mV Factory programmable threshold for all other Vout range settings is +100mV, +150mV, +200mV, or +250mV
Buck4 Undervoltage	BUCK4_UV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is -60mV, -100mV, -150mV, or -250mV Factory programmable threshold for all other Vout range settings is -100mV, -150mV, -200mV, or -250mV
Buck5 Low-Side Negative Overcurrent (NOC)	BUCK5_LSWUC	Y	-
Buck5 High-Side Positive Overcurrent (POC)	BUCK5_HSWOC	Y	-
Buck5 Overvoltage	BUCK5_OV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is +60mV, +100mV, +150mV, or +250mV Factory programmable threshold for all other Vout range settings is +100mV, +150mV, +200mV, or +250mV
Buck5 Undervoltage	BUCK5_UV	Y	Factory programmable threshold for Vout range setting of 0.3V~1.2V is -60mV, -100mV, -150mV, or -250mV Factory programmable threshold for all other Vout range settings is -100mV, -150mV, -200mV, or -250mV
LDO1-4 Undervoltage	LDO1_UV/ LDO2_UV/ LDO3_UV/ LDO4_UV	Y	Undervoltage detection for LDO1-4. Factory programmable threshold of -6%. -10%
LDO5/6 Undervoltage	LDO5_UV/LDO6_UV	Y	Undervoltage detection for LDO5-6. Factory programmable threshold of -6%. -10%, -20%
VBAT Overvoltage	VBAT_OV	Y	Overvoltage fault on AVIN1
SPI CRC Error	FLT_SPI	Y	Indicates a fault during a SPI transaction while CRC for SPI communication is enabled
I^2C CRC Error	FLT_I2C	Y	Indicates a fault during an I^2C transaction while CRC for I^2C communication is enabled

5.6 Power Grouping and Power State Transitions

5.6.1 Power Grouping

The RAA271005/RAA271005L allows the flexibility for all regulators (5 Bucks + 6 LDOs) to be defined to be a part of five groups:

- Always On GROUP – This group of regulators turns ON/OFF automatically following EN pin.
- PWRCTL1 GROUP – This group of regulators turns ON/OFF automatically following PWRCTL1 pin.
- PWRCTL2 GROUP – This group of regulators turns ON/OFF automatically following PWRCTL2 pin.
- S2R GROUP – This is a subgroup of the PWRCTL1 and PWRCTL2 groups. When a regulator is put into this group, pin control can be inhibited dynamically with a register write.
- SW SHDN GROUP – This is a subgroup of Always On GROUP. Regulators in this group turn ON automatically with EN. They can be turned OFF either following EN or also can be turned off by a register write. Regulators that are supposed to be disabled during S2R should be put into this group.

Note: BUCK3, BUCK4, and Buck5 have a lower quiescent current than BUCK2. Renesas recommends considering these three bucks first to be used for Suspend-to-RAM.

Note: If no regulators are assigned to either the PWRCTL1 or PWRCTL2 Group, where the PWRCTL1 or PWRCTL2 pins are not used, ensure to tie these pins low with a 10kΩ.*Note:* There must be at least one regulator assigned to the PWRCTRL1 S2R / PWRCTRL2 S2R power group for IO19-BKUP signal/pin to function. The BKUP signal is indicator for S2R rails. If none are assigned in the S2R GROUP, there is no Suspend-to-RAM power sequence state at the system level.

Table 19. Power Grouping Control

Controls					Always On GROUP		PWRCTL1 GROUP		PWRCTL2 GROUP	
EN Pin	PWRCTL1 Pin	PWRCTL2 Pin	S2R Register	SW SHDN Register	MAIN Group	SW SHDN Subgroup	MAIN Group	S2R Subgroup	MAIN Group	S2R Subgroup
ON	ON/OFF	ON/OFF	Disabled	Disabled	ON	ON	PWRCTL1	PWRCTL1	PWRCTL2	PWRCTL2
ON	ON/OFF	ON/OFF	Enabled	Disabled	ON	ON	PWRCTL1	S2R	PWRCTL2	S2R
ON	ON/OFF	ON/OFF	Disabled	Enabled	ON	SW SHDN	PWRCTL1	PWRCTL1	PWRCTL2	PWRCTL2
OFF	X	X	X	Disabled	OFF	OFF	OFF	OFF	OFF	OFF
OFF	X	X	X	Enabled	OFF	OFF	OFF	OFF	OFF	OFF

5.6.2 Power Flow Diagrams

Blocks shown as double line border are programmable. These are for understanding basic operation of the RAA271005/RAA271005L but are not meant to cover every possible situation.

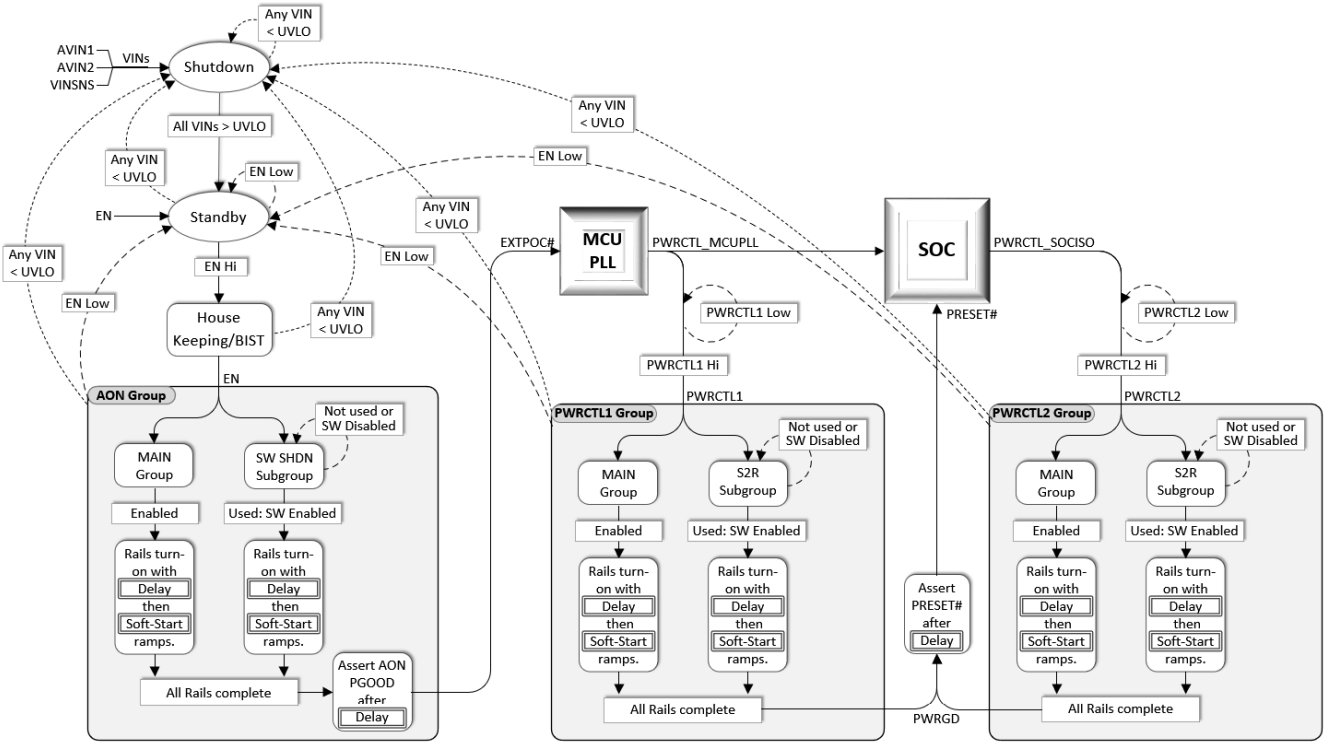


Figure 24. Power-up and Power-down Flow Diagram

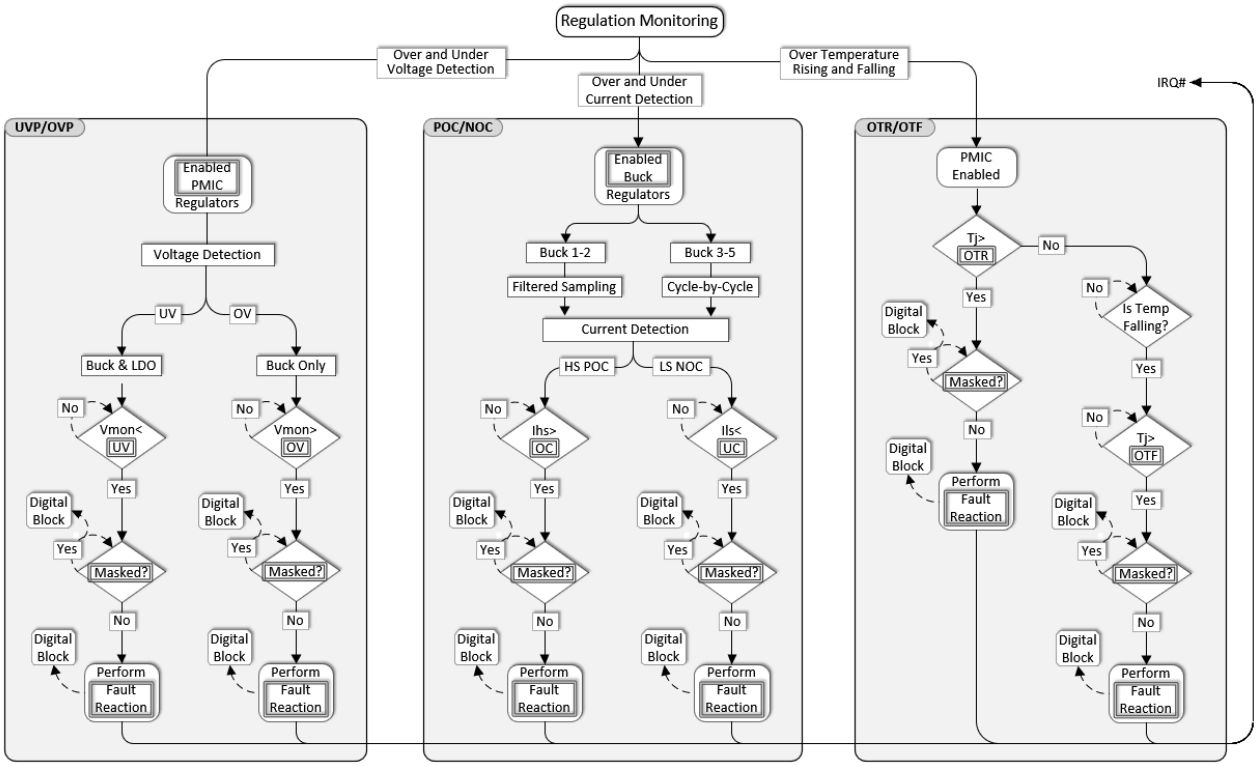


Figure 25. Power-up and Power-down Flow Diagram

5.6.3 Power State Transitions (R-Car S4 SoC Example)

5.6.3.1 Cold Start (Power Off to Full Run)

Cold start is the power mode transition where the PMIC is enabled from the powered off state. The Always On group of rails powers up immediately when EN is brought high. When all the Always On rails are powered up, EXTPOC# toggles high to output Always On PGOOD. The MCUPLL reads the EXTPOC# and generates a PWRCTL1 high input to the PMIC that enables PWRCTL1 group rails. PWRCTL1 signal is monitored by the S4 SoC to generate a PWRCTL2 high input to the PMIC that enables the PWRCTL2 group rails. When all the rails are Always On, PWRCTL1 and PWRCTL2 are enabled, and the PGOOD signal toggles high to indicate all the rails are up. After the programed timer, the PRESET# signal is brought high and the PMIC is in Full Run mode.

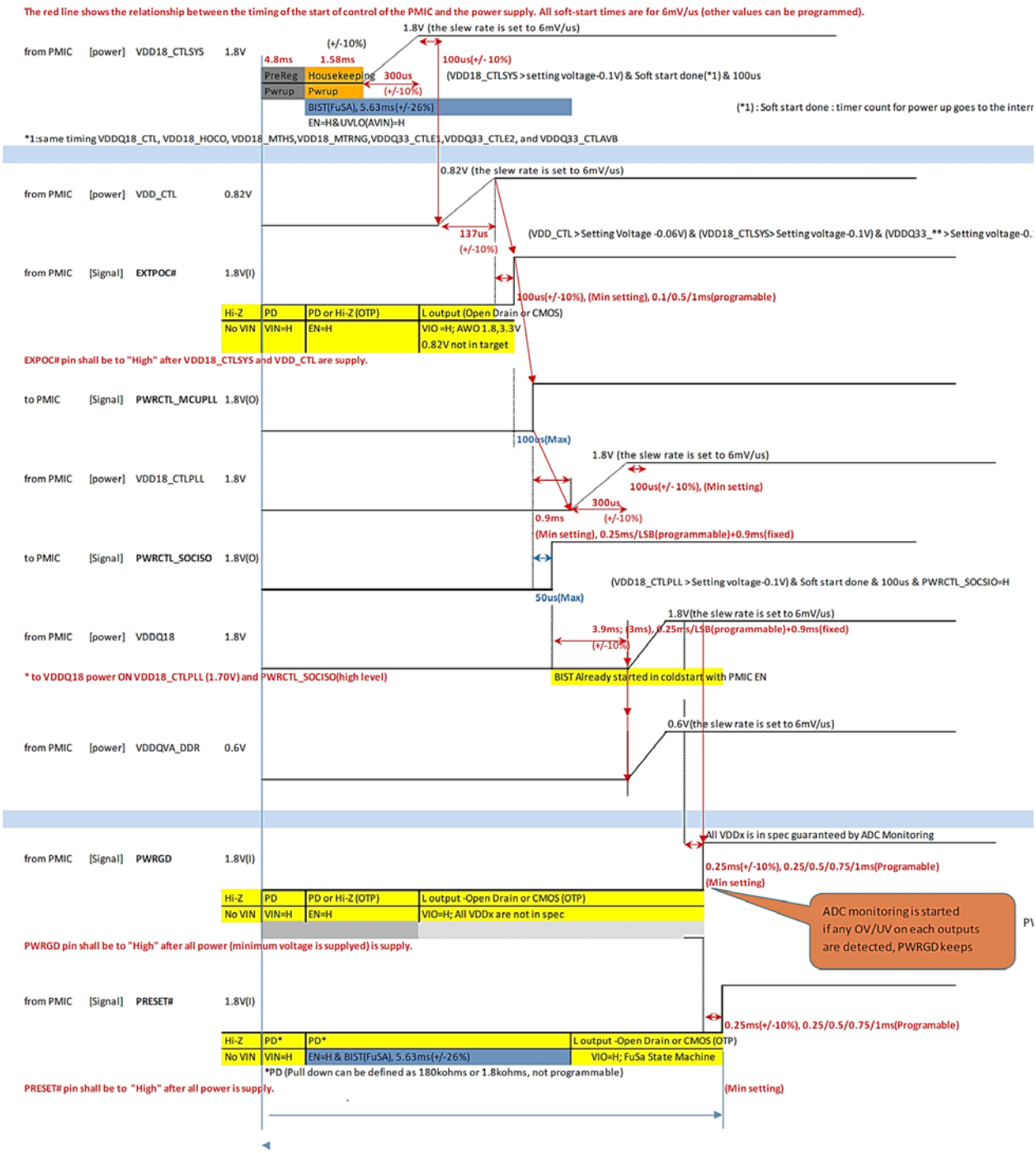


Figure 26. Cold Start (Power Off → Full Run) Timing

5.6.3.2 Full Run to Deep Stop

The Cold Start (Power Off to Full Run) section explains the Full Run mode entry. In Deep Stop mode, the rails in PWRCTL2 group are disabled. Please note that rails designated to PWRCTL1, SW_SHDN, or Always On will remain on. For generic SOCs or MCUs the Low IQ mode bit needs to be requested, for S4 SOC this is automatically configured in the OTP. If PWRCTL1 GROUP rails need to be turned off during Deep Stop mode, PWRCTL1 can be set low either after PWRCTL2 is low or before PWRCTL2. However, if PWRCTL1 is set low before PWRCTL2, the time difference between them must be between 18.93µs and 23.15µs, as shown in Figure 27.

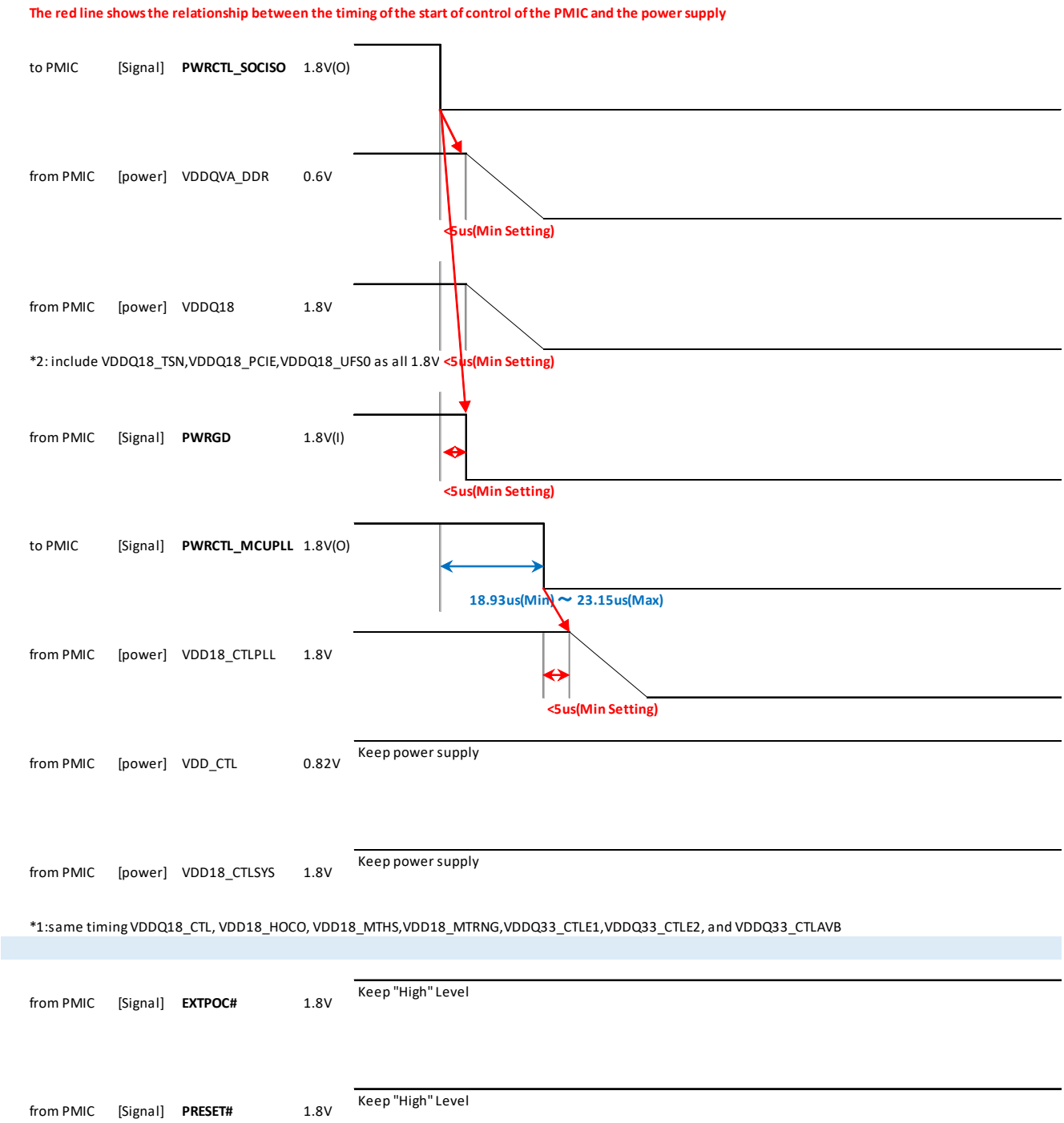


Figure 27. Full Run → Deep Stop Timing

5.6.3.3 Warm Start (Deep Stop to Full Run)

The Full Run to Deep Stop section explains the Deep Stop mode entry. To exit the Deep Stop mode, the system pulls the PWRCTL1 and PWRCTL2 pins high. All the rails including Bucks and LDOs turn on, and the protection digital wakes up on PWRCTL2 high as set by the OTP.

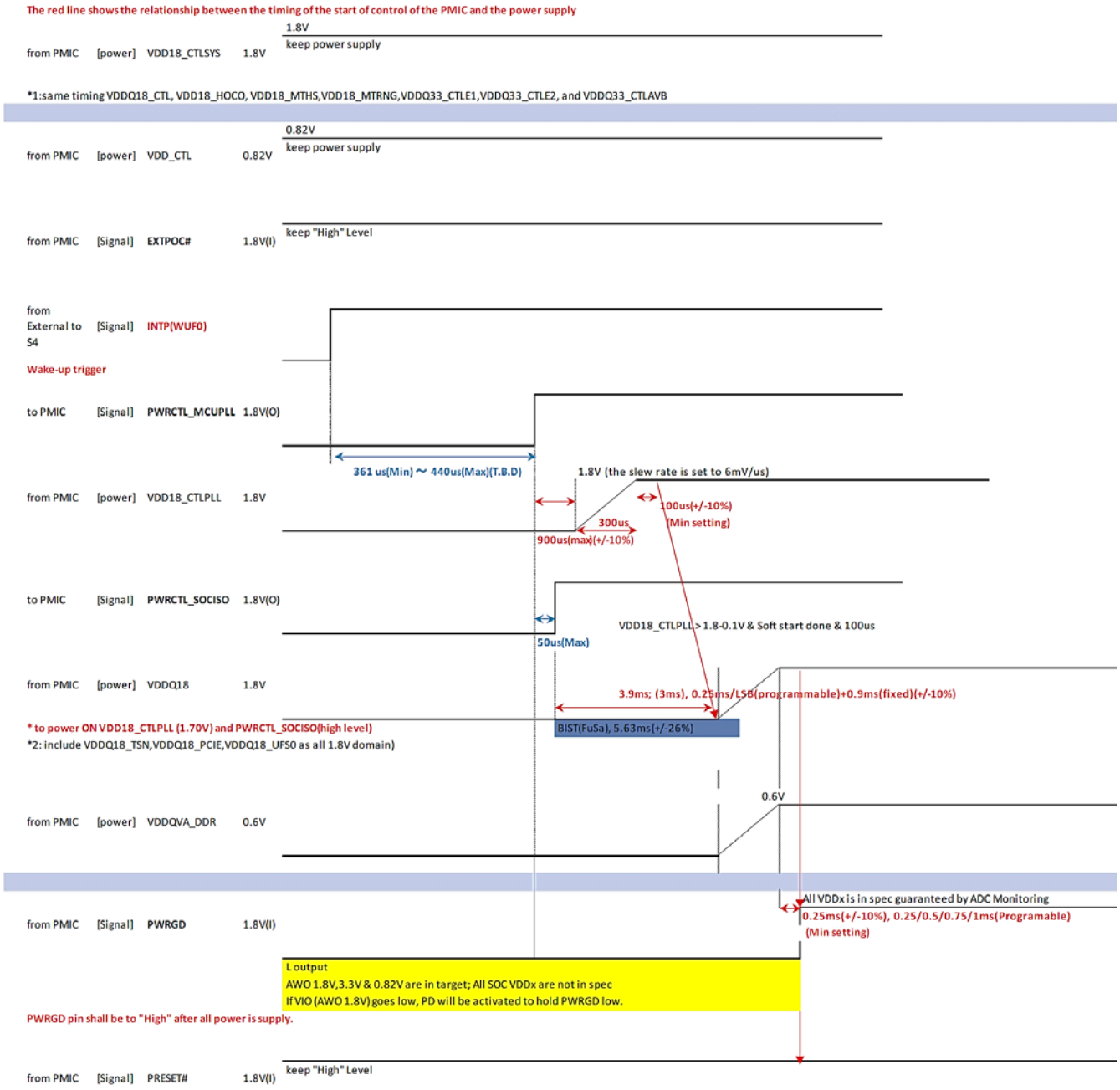


Figure 28. Warm Start (Deep Stop → Full Run) Timing

5.6.3.4 Full Run to Suspend-to-RAM

The PMIC implements a Suspend-to-RAM mode that is used for the DDR Back up sequence. The S4 system requires specific rails to remain on during the S2R mode. The PMIC enters this mode when the REG_DDR_BKUP register is written to 1, and this is indicated on the BKUP (GPIO19 configurable) pin. When the PWRCTL2 signal is brought low and BKUP is set high, the regulators that have been designated to remain on during this low power mode (S2R rails) remain on, but the regulators that have been selected to turn off are disabled. The S4 begins the DDR backup procedure with the critical rails on.

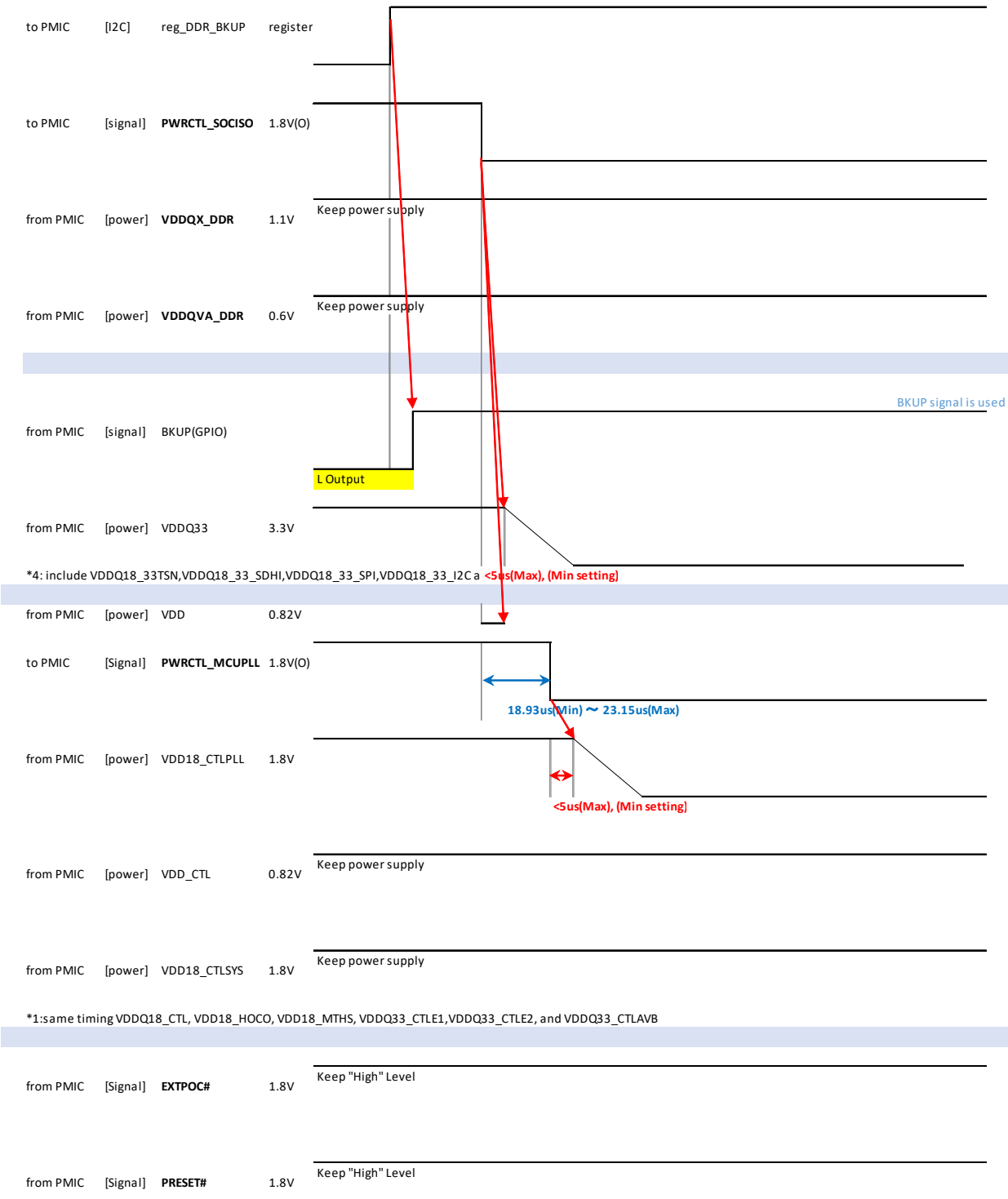


Figure 29. Full Run → S2R Timing

5.6.3.5 Suspend-to-RAM to Full Run

The PMIC goes from Suspend-to-RAM to Full Run when the PWRCTL2 pin is asserted back to high level. The regulators, which disabled during this mode, restart, and the PGOOD asserts high when all regulators have completed their soft-start sequences. The BKUP (GPIO19 configurable) pin asserts back to low as the REG_DDR_BKUP register is written to 0 to end the S2R mode, and the system returns to the Full Run mode.

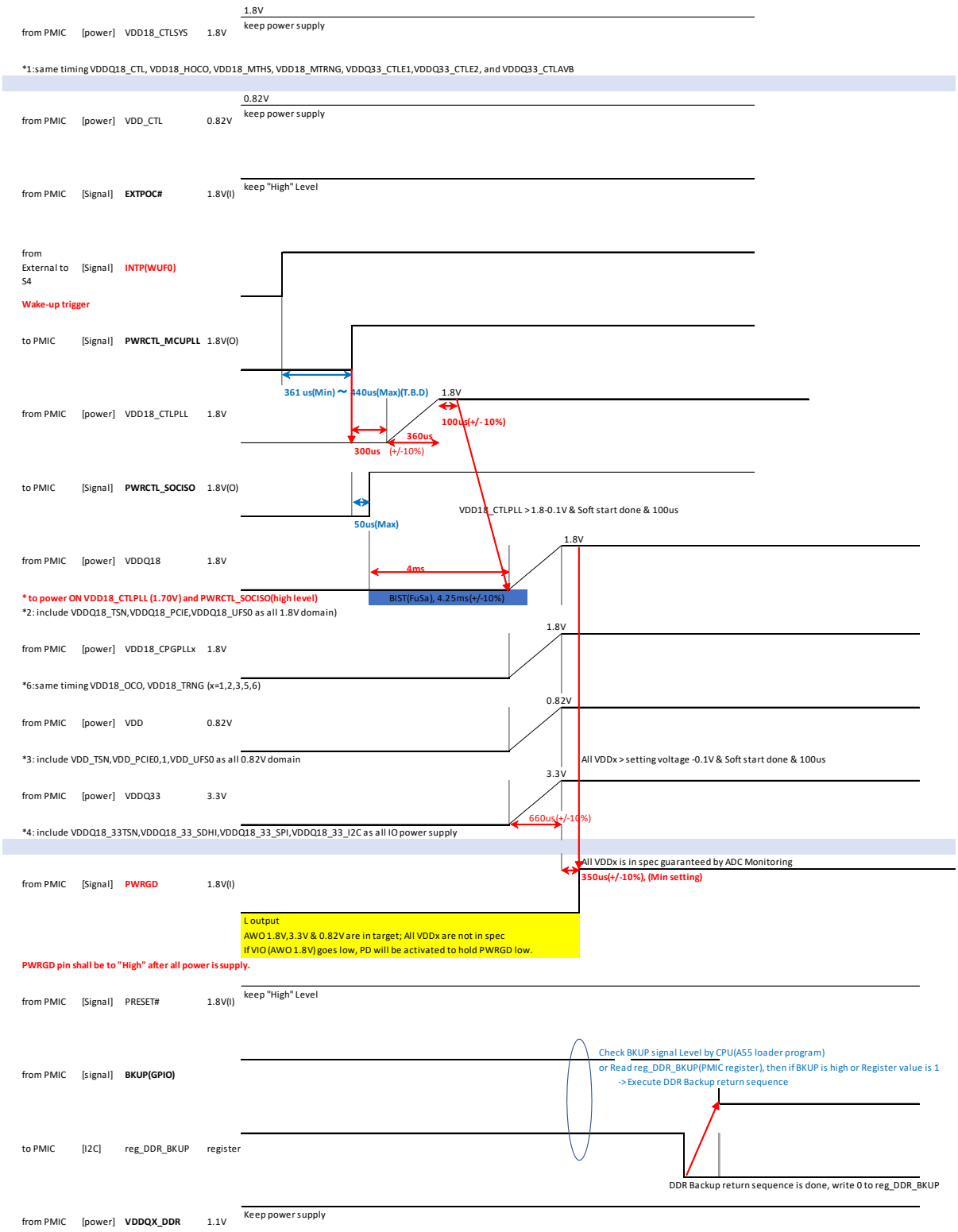


Figure 30. S2R → Full Run Timing

5.6.3.6 Comparison Between Deep Stop and Suspend-to-RAM

Table 20 compares Deep Stop mode and Suspend-to-RAM mode by highlighting their key differences and requirements. Both modes use PWRCTL2 for entry and share similar timing constraints, but they differ in power rail control, register requirements, and IO control.

Table 20. Comparison of Deep Stop and Suspend-to-RAM Mode

Feature	Deep Stop	Suspend-to-RAM
Use PWRCTRL2 to enter mode	Yes	Yes
Buck3 in PFM	Yes	Yes
Time difference between PWRCTL1 low and then PWRCTL2 low	18.93us to 23.15us	18.93us to 23.15us
ALWAYS ON Group remains ON	Yes	Yes
PWRCTL1 Group remains ON	No	Depends on whether rails are part of S2R rails
PWRCTL2 Group remains ON	No	Depends on whether rails are part of S2R rails
Use IO19	No	Yes
Register write required	No	Yes
PRESET Level	OTP setting: PRESETb_DEEPSTOP	OTP setting: PRESETb_DEEPSTOP
SoC Activation Upon Exit	Yes	Yes
BIST Test Upon Exit	Yes	Yes

5.6.3.7 Suspend-to-RAM Power Rails

In normal S2R mode, rails that need to remain on during S2R mode must have their Power State set to ALWAYS ON or PWRCTL1/2 GROUP and Used with Suspend to RAM set to TRUE, while rails that should turn off during S2R mode must be assigned to PWRCTL1/2 GROUP with Used with Suspend to RAM set to FALSE.

Table 21. Rails Status in S2R

<table>
<tr><th colspan="2">SW_BKUP = FALSE</th><th colspan="8">Rails Status</th></tr>
<tr><th colspan="2">Normal S2R mode</th><th colspan="2">PWRCTL1 GROUP</th><th colspan="2">PWRCTL2 GROUP</th><th colspan="2">ALWAYS ON GROUP</th><th colspan="2">SW_SHDN GROUP</th></tr>
<tr><td colspan="2">PWRCTLs State</td><td colspan="2">Used with S2R?</td><td colspan="2">Used with S2R?</td><td colspan="2">Used with S2R?</td><td colspan="2">Used with S2R?</td></tr>
<tr><td>PWRCTL1</td><td>PWRCTL2</td><td>FALSE</td><td>TRUE</td><td>FALSE</td><td>TRUE</td><td>FALSE</td><td>TRUE</td><td>FALSE</td><td>TRUE</td></tr>
<tr><td>L</td><td>L</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>ON</td><td rowspan="4">Not Applicable</td><td colspan="2" rowspan="4">N/A[1]
(Only available in SW BKUP)</td></tr>
<tr><td>H</td><td>L</td><td>ON</td><td>ON</td><td>OFF</td><td>ON</td><td>ON</td></tr>
<tr><td>L[2]</td><td>H[2]</td><td colspan="2">Error State</td><td colspan="2">Error State</td><td>Error State</td></tr>
<tr><td>H[3]</td><td>H[3]</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td></tr>
</table>

1. The SW_SDHN GROUP is only available when using the SW_BKUP option. If a rail that during S2R mode for normal S2R option, set it to PWRCTL1/2 when used with Suspend to RAM? option set to FALSE.
2. This condition is invalid because PWRCTL2 is required to enter S2R mode along with the REG_DDR_BKUP (0x176) register write. If PWRCTL1 is set Low while PWRCTL2 remains High, the PMIC goes into Error State as it never went into S2R mode.
3. If PWRCTL2 is not set low, the system does not enter S2R mode. Therefore, keeping both PWRCTL1 and PWRCTL2 High prevents entry into S2R mode.

5.6.3.8 SW BKUP Power Rails

In SW_BKUP mode, rails that need to remain on during S2R mode must have their Power State set to ALWAYS ON GROUP. Rails that should turn off during S2R mode must be assigned to the SW_SHDN Group. One rail that remains on during S2R mode must be configured with its Power State set to PWRCTL1 with “Used with Suspend to RAM” set to TRUE.

PWRCTL1 and PWRCTL2 is inverted internally if SW_BKUP option is chosen. When 0x3 is written to REG_DDR_BKUP (0x176) register, it will internally pull PWRCTL2 low to get into S2R mode, followed by pulling PWRCTL1 low.

When using SW_BKUP mode:

- A rail that remains on during S2R mode must have its Power State set to PWRCTL1 with Used with Suspend to RAM enabled.
- Other rails must be assigned to either the SW_SHDN Group or the ALWAYS ON GROUP.

Table 22. Rails Status in SW_BKUP

SW_BKUP = TRUE		Rails Status							
Software S2R mode (SW_BKUP)		PWRCTL1 GROUP		PWRCTL2 GROUP[1]		ALWAYS ON GROUP		SW_SHDN GROUP	
PWRCTLs State		Used with S2R?		Used with S2R?		Used with S2R?		Used with S2R?	
PWRCTL 1	PWRCTL2	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE	FALSE	TRUE
L	L	N/A[2]	ON	Not Applicable		ON	N/A	OFF	N/A[3]
H	L	N/A[4]	N/A[4]			ON		OFF	
L	H	N/A[5]	N/A[5]			ON		OFF	
H	H	N/A[4]	N/A[4]			ON		OFF	

1. No rails are allowed to be set to PWRCTL2 in S2R mode.
2. Power State set to PWRCTL1 and Used with Suspend to RAM set to FALSE option is not allowed.
3. Rails that are in SW_SHDN Group are automatically turn off in S2R mode when the REG_DDR_BKUP (0x176) register write happen. It is not configurable to remain on during S2R mode.
4. PWRCTL1 is pulled low internally when REG_DDR_BKUP (0x17)6 register write happen so it will never be High during SW_BKUP.
5. PWRCTL2 is pulled low internally when REG_DDR_BKUP (0x176) register write happen so it will never be High during S2R mode. In the case where PWRCTL2 is High, PMIC does not go into S2R mode.

5.7 Overvoltage Protection Gate Control

The RAA271005/RAA271005L has continuous input voltage monitoring through the VIN_SENSE pin. This continuous monitoring allows the RAA271005/RAA271005L to detect if the input voltage exceeds a pre-programmed OV threshold (VOVPR_S) that asserts the GC pin High, which turns off Q9 essentially cutting of the input voltage to the PMIC. The circuit (Figure 31) allows for the proper start up of the PMIC, with R154 ensuring that Q9 is on when the VIN_SENSE voltage is ramping up presumably from the primary regulator. The GC feature has a recovery falling threshold fixed at VOVPF_S. If the VIN_SENSE falls below this after tripping an OV condition, RAA271005/RAA271005L recovers the OV condition, GC is again pulled low, and Q9 is on again (Figure 32). The GC pin has a built-in self test that is enabled in the OTP. The GC feature also implements a hangover timer. The hangover timer keeps Q9 enabled only if all the downstream rails are not turned off. This ensures that the power-down timing sequence is followed by a power-off, regardless if EN is lost.

Note: The GC block inside the RAA271005/RAA271005L is enabled when EN goes high; if EN remains low once VIN is present, the GC block remains disabled, and the GC pin does not respond (remain high).

Note: In applications that do not use the GC function, the GC pin can be left floating and the FET removed. However, VIN_SENSE needs to be tied to VIN. Also, the GC self-test (GC_SELFT_FAULT) must be masked in the OTP setting.

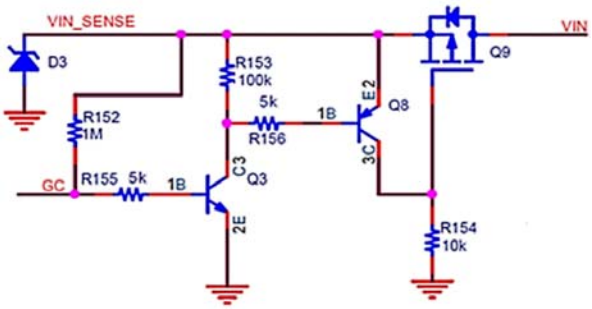


Figure 31. GC Circuit

EN	VIN_SENSE	GC
High	$>V_{UVLOR}$ and $<V_{OVPR_S}$	Low
High	$<V_{UVLOR}$ or $>V_{OVPR_S}$	High
Low	X	High

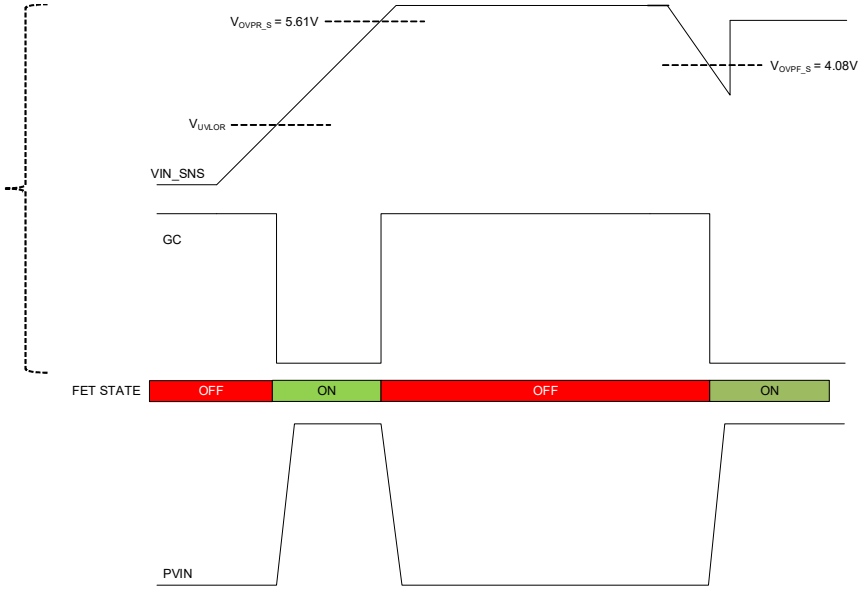


Figure 32. GC Operation at OV and OV Recovery

5.8 RAA271005/RAA271005L GPIO

The RAA271005/RAA271005L has five GPIO pins (IO3, IO4, IO5, IO6, IO13), which can be programmed by OTP for multiple functions. The following are the functions available for the GPIO pins.

- Generic IO where it can read a valid logic level when configured as an input or drive a programmed logic level (IO3, IO4, IO5) when configured as an output.
- Power-good indicator
- Interrupt of Regulation block
- DVS control (IO6)
- Following EN

Function	IO3	IO4	IO5	IO6	IO13
General IO	✓	✓	✓	-	-
PGOOD	✓	✓	✓	✓	✓
Interrupt of Regulation	✓	✓	✓	✓	✓
DVS Control	-	-	-	✓	-
Following EN	✓	✓	✓	✓	✓

5.8.1 General Purpose IOs

IO3, IO4, and IO5 can each be configured as a general-purpose input/output. RAA271005/RAA271005L allows these to be configured as open-drain or push pull with internal programmable pull-ups (60kΩ or 1.8MΩ) or pull-downs (180kΩ). The polarity of the signal can be set as active low or active high. The assert and de-assert delays are programmable through the OTP settings.

When the IOs are configured as an input, the IO levels are brought into the IO_GPIO_DATAIN registers. When configured as an output, writing to the register IO_GPIO_DATAOUT brings the corresponding outputs to the programmed H/L state.

Table 23. IO Register Configurations

IO	Register for IO Configured Input	Register for IO Configured Output
IO3	IO_GPIO_DATAIN[0]	IO_GPIO_DATAOUT[0]
IO4	IO_GPIO_DATAIN[1]	IO_GPIO_DATAOUT[1]
IO5	IO_GPIO_DATAIN[2]	IO_GPIO_DATAOUT[2]

5.8.2 Power-Good Indicator (IO6, IO13)

GPIOs can each be configured as a power-good indicator. The PGOOD signal toggles high to indicate the corresponding group rails are up. For the power grouping detail, see Power Grouping.

Power Good	H Condition
PGOOD_GLB(PGOOD)	All regulators are in range
PGOOD_ALWON(EXTPOC)	All regulators of always on group are in range.
PGOOD_CTL1	All regulators of PWRCTL1 group are in range.
PGOOD_CTL2	All regulators of PWRCTL2 group are in range.
PGOOD_S2R	All regulators of S2R group are in range.
PGOOD_SW	All regulators of SW SHDN group are in range.

5.8.3 Interrupt of Regulation

GPIOs can each be configured as an interrupt of the Regulation block. This interrupt is asserted when the regulation fault in Table 18 is detected.

5.8.4 DVS pin

There are two independently programmable voltage settings for the Buck1 controller, which can set the output voltage. These voltage settings are selected by changing the DVS using the GPIO/MPIO pins. For details, see Buck Dynamic Voltage Scaling.

5.8.5 Following EN

When configured as a Follow EN, the device has the capability to be assigned in the power sequencer.

At power-up (EN:H), the follow EN asserts after the OTP download is complete. At power-down (EN:L), the signal de-asserts low just after EN inputs L.

5.9 Regulation Hiccup Feature

Regulation block implements a hiccup feature which automatically retries to power-up the rails when there is an OC/UV/OV/OT/AVIN_OV fault in regulation block during Deep Stop mode when protection block is not available. If the condition causing fault is not cleared and PGOOD does not happen, the PMIC keeps retrying from cold start. On every retry, the retry counter is incremented by 1. If on one of the retries, PMIC gets PGOOD the counter resets. This behavior is shown in Figure 33.

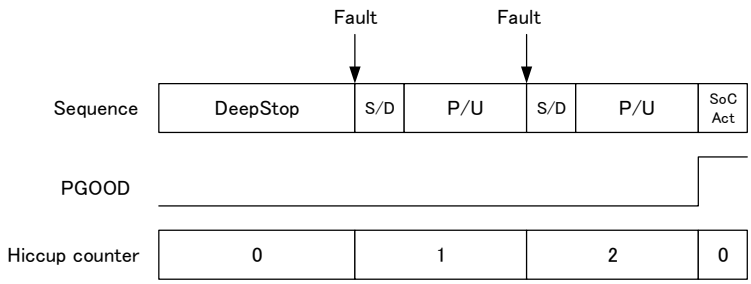


Figure 33. Hiccup Counter Behavior

If the PMIC never comes out of restarts and the counter rolls over the OTP setting, the PMIC latches off. An EN toggle/UVLO condition is required for a fresh power-up. This behavior is shown in Figure 34.

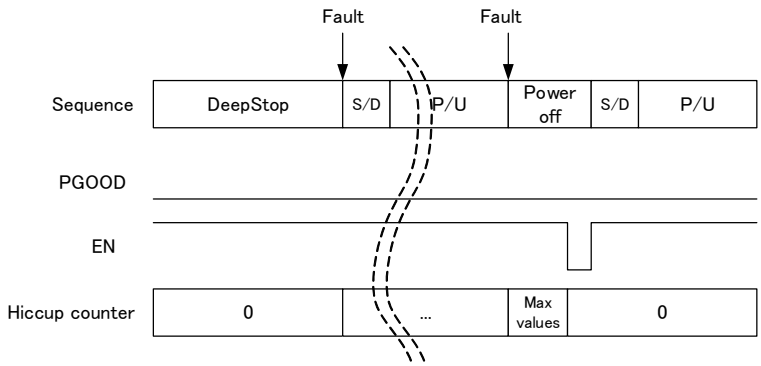


Figure 34. Hiccup Counter Reset (EN toggle)

The hiccup retry count can be set through OTP using one of the following settings:

Table 24. Hiccup Feature

Hiccup Counter Setting	Number of Retries
0x0	Infinite
0x1	4 times
0x2	8 times
0x3	15 times

The hiccup interval is set to retry every 1ms.

5.10 Lock Release/OTP Retry ADC3 Pin Option.

Under certain conditions, the regulator can enter a lock state which disables its outputs. Enable can be toggled to restart the regulators, but there is another option where the ADC3 pin can be configured as a Lock Release signal (see regulation register bits LOCK_RELEASE_Pinsel and protection register bits I_LOCK_RELEASE_PinSel).

The following list describes the conditions that cause a lock. *Note:* An OTP download retry happens using the ADC3 pin in this scenario.

- Hiccup counter maxing out in Deep Stop
- Discharge Detect fault (when latch-off option is selected)
- OTP Download failure

5.11 Invalid Deep Stop

Invalid Deep Stop is defined as a PWRCTL2 signal toggling from high to low when PGOOD is not high. Invalid Deep Stop can happen in Cold Start or during Warm Start.

During Invalid Deep Stop, PRESETb is low and all regulators shut down. Protection goes to an Error state because of REGU_FLT, and the rest of the operation is controlled by the Protection FuSa block.

6. Protection Features

While the Regulation side of the chip handles the power management functions and delivers stable power to all outputs, the Protection side of the chip monitors all output and internal signals for faults.

6.1 Monitoring ADC

The RAA271005/RAA271005L uses a sophisticated multi-channel 12-bit SAR ADC to continuously monitor all output rails, critical internal signals, and the chip temperature. The ADC samples are processed by a digital averaging filter to reduce noise and increase accuracy.

The monitoring system can also measure up to 16 external signals by using five dedicated ADC pins. These ADC pins can be configured either as all analog inputs (ADC1 to ADC5), or they can be configured to use external multiplexers. If external multiplexers are used, pins ADC1 and ADC2 are analog inputs and pins ADC3 to ADC5 are digital outputs to control the digital multiplexers with fixed timing (the VOL and VOH characteristics are the same as the GPIOs, but using AVIN2 as the supply instead of VIO). A block diagram of the monitoring system is shown in Figure 35 (an option for a suitable device for the mux is the NX3L4051PW-Q100J).

Protection register 0x135 - ADCMON_EXT_CFG can be used to configure the external mux options. Refer to the *Safety Application Note* for the register description.

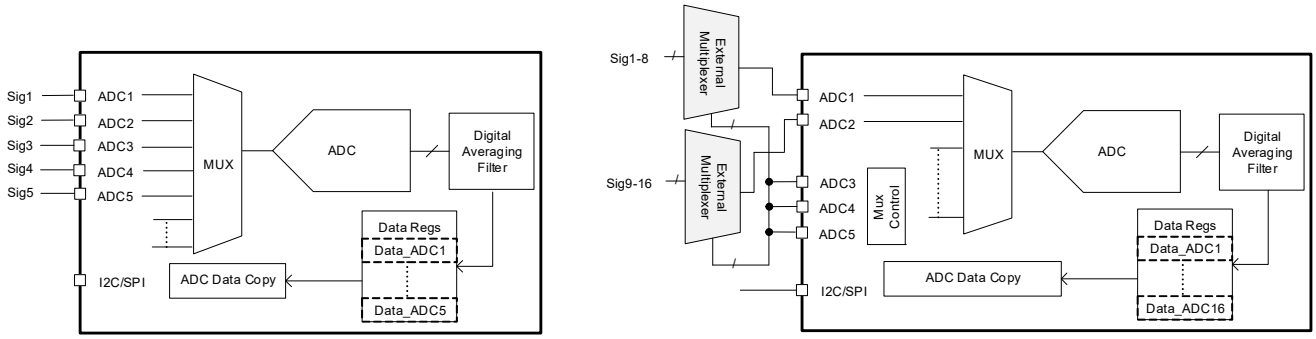


Figure 35. Monitoring ADC

The ADC High/Low thresholds, averaging filter coefficient (IIR), and full-scale range (PGA gain) are all independently programmable for external measurements 1 to 8. The ADC conversion result can be setup and read back using the ADC copy registers. Figure 36 shows the EN timing for ADC monitoring when the system starts up from a cold start. The ADC monitoring for all rails starts after the system enters full run.

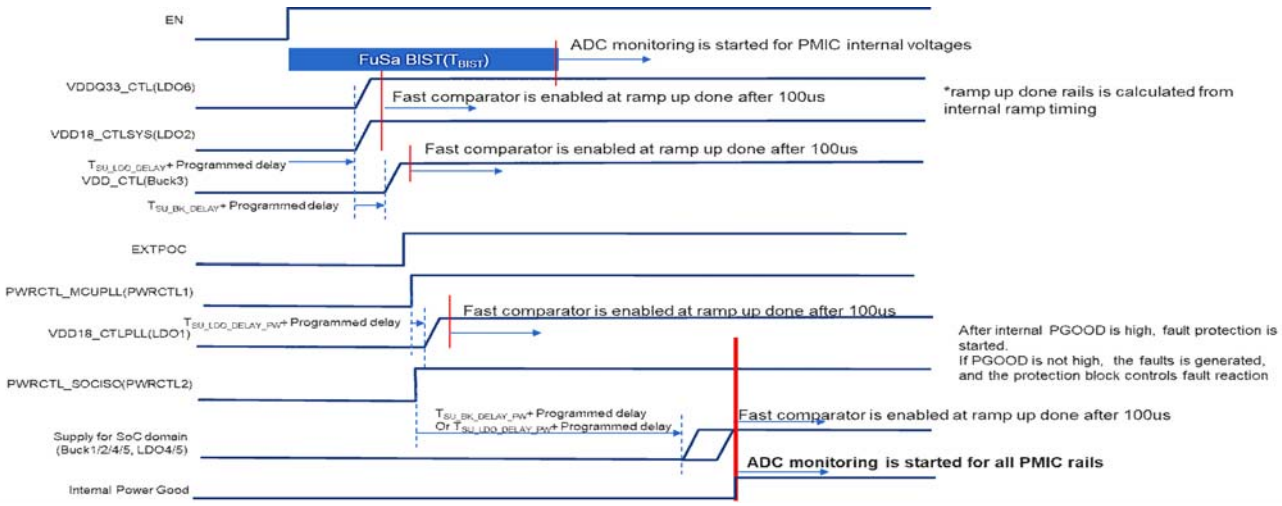


Figure 36. EN Timing for ADC Monitoring

6.1.1 Monitoring ADC Inputs

The monitoring system monitors the outputs of each of the ADC inputs shown in Table 25. Monitoring is performed by comparing the current ADC Data with a High Limit and Low Limit value that is set in the same format as the ADC readings.

Table 25. All Monitoring ADC Inputs

ADC Input Description	Register Map Name	Scaling Factor	Unit
ADC Internal Offset	ADCMON_Offset	1	Codes
Temperature	ADCMON_Temp	4	°C
Temperature (redundant copy)	ADCMON_Temp_Delta	4	°C
Regulation Bandgap	ADCMON_BGRegu	4000	V
Regulation PGND	ADCMON_PGNDRegu	4000	V
Regulation Internal LDO #1	IntLDORegu_0_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #2	IntLDORegu_1_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #3	IntLDORegu_2_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #4	IntLDORegu_3_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #5	IntLDORegu_4_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #6	IntLDORegu_5_ADCMON_IntLDORegu	3000	V
Protection Internal LDO #1	IntLDOProt_0_ADCMON_IntLDOProt	3000	V
Protection Internal LDO #2	IntLDOProt_1_ADCMON_IntLDOProt	3000	V
AVIN1 Voltage	ADCMON_AVIN1	4000	V
AVIN2 Voltage	ADCMON_AVIN2	4000	V
LDO1 Voltage	extLDO_0_ADCMON_ExtLDO	4000	V
LDO2 Voltage	extLDO_1_ADCMON_ExtLDO	4000	V
LDO3 Voltage	extLDO_2_ADCMON_ExtLDO	4000	V
LDO4 Voltage	extLDO_3_ADCMON_ExtLDO	4000	V
LDO5 Voltage	extLDO_4_ADCMON_ExtLDO	4000	V
LDO6 Voltage	extLDO_5_ADCMON_ExtLDO	4000	V
PVIN1 Voltage	PVIN_0_ADCMON_PVIN	533	V
PVIN2 Voltage	PVIN_1_ADCMON_PVIN	533	V
PVIN3 Voltage	PVIN_2_ADCMON_PVIN	533	V
PVIN4 Voltage	PVIN_3_ADCMON_PVIN	533	V
PVIN5 Voltage	PVIN_4_ADCMON_PVIN	533	V
Buck1 (VOUT1) Voltage	VOUT_0_ADCMON_VOUT	4000	V
Buck2 (VOUT2) Voltage	VOUT_1_ADCMON_VOUT	4000	V
Buck3 (VOUT3) Voltage	VOUT_2_ADCMON_VOUT	4000	V
Buck4 (VOUT4) Voltage	VOUT_3_ADCMON_VOUT	4000	V
Buck5 (VOUT5) Voltage	VOUT_4_ADCMON_VOUT	4000	V
ADC1 / External ADC Mux Channel 0	EXT_0_ADCMON_EXT	4000	V
ADC2 / External ADC Mux Channel 1	EXT_1_ADCMON_EXT	4000	V

Table 25. All Monitoring ADC Inputs

ADC Input Description	Register Map Name	Scaling Factor	Unit
ADC3 / External ADC Mux Channel 2	EXT_2_ADCMON_EXT	4000	V
ADC4 / External ADC Mux Channel 3	EXT_3_ADCMON_EXT	4000	V
ADC5 / External ADC Mux Channel 4	EXT_4_ADCMON_EXT	4000	V
External ADC Mux Channel 5	EXT_5_ADCMON_EXT	4000	V
External ADC Mux Channel 6	EXT_6_ADCMON_EXT	4000	V
External ADC Mux Channel 7	EXT_7_ADCMON_EXT	4000	V
External ADC Mux Channel 8	EXT_8_ADCMON_EXT	4000	V
External ADC Mux Channel 9	EXT_9_ADCMON_EXT	4000	V
External ADC Mux Channel 10	EXT_10_ADCMON_EXT	4000	V
External ADC Mux Channel 11	EXT_11_ADCMON_EXT	4000	V
External ADC Mux Channel 12	EXT_12_ADCMON_EXT	4000	V
External ADC Mux Channel 13	EXT_13_ADCMON_EXT	4000	V
External ADC Mux Channel 14	EXT_14_ADCMON_EXT	4000	V
External ADC Mux Channel 15	EXT_15_ADCMON_EXT	4000	V

6.1.2 External Differential Measurement

The RAA271005/RAA271005L can make an external differential voltage measurement with a full set of monitoring and measurement register controls. This measurement channel is a computed control and represented as SPARE0 (or SPARE_0) where it is equal to ADC5 - ADC4 (ADC readings). This can measure a high-power external voltage regulator and provides protection monitoring for it.

To implement this, connect ADC5 to the positive sense, and ADC4 to the negative sense; next, use the SPARE0 channel for any external measurement.

Note: Because of the sampling time between ADC4 and ADC5 (45µsec), for this computed result to be accurate, the external differential signal should be low-pass filtered with a cutoff of 700Hz or less (0.225msec time-constant).

6.1.3 Monitoring ADC Input Range

The monitoring ADC includes a Programmable Gain Amplifier (PGA) to precondition analog inputs. The output of the PGA is connected to the ADC. The ADC itself has an input voltage range of ±980mV.

RAA271005/RAA271005L has 8 PGA gain settings that set the effective input voltage range of the input to the ADC. The PGA gain for each ADC channel can be set independently. All PGA gain input effective ranges are shown in Table 26.

Note: Refer to the *Safety Application Note*, section *ADC BIST*, for maximum OV threshold limits for each PGA Gain Option.

Note: See Figure 37 for a block diagram that shows the operation of the PGA Gain and ADC.

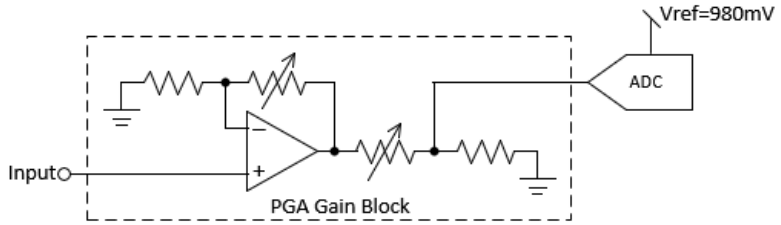


Figure 37. PGA Gain and ADC Block Diagram

Table 26. PGA Gain Settings

Option Number	PGA Gain	Input Voltage Range	Input Voltage Range (to meet specified accuracy)
0	0.125	-0.3V to +7.408V	+2.741V to +7.408V
1	0.5	-0.3V to +1.851V	+1.044V to +1.851V
2	2	-0.3V to +0.462V	+0.115V to +0.462V
3	8	-0.1V to +0.115V	+0.100 V to +0.115V
4	0.333	-0.3V to +2.780V	+1.674V to +2.780V
5	0.8	-0.3V to +1.158V	+0.561V to +1.158V
6	For PVIN Monitoring Only		+2.741V to +5.500V
7	1.4	-0.3V to +0.659V	+0.462V to +0.659V

6.1.4 Monitoring System IIR Filter

The monitoring ADC includes an Infinite Impulse Response (IIR) filter to reduce noise and improve accuracy. The IIR filter has the following transfer function:

(EQ. 5) $$\text{AVERAGE} = \frac{\text{NewSample} - z^{-1} \times \text{Average}}{2^{-m}} + z^{-1} \times \text{Average}$$

The value of m can be independently set from 0 to 7 for each monitored rail, so the IIR can have the following values listed in Table 27.

Table 27. IIR Coefficient Options

Option	IIR Averaging Value
0	1
1	1/2
2	1/4
3	1/8
4	1/16
5	1/32
6	1/64
7	1/128

6.1.5 Sampling Rate

The sampling rates for different ADC channels are shown in Table 28.

Table 28. ADC Sampling Rate of Different Inputs

PMIC Outputs (Buck[1-5], LDO[1-6])	PMIC Internal	ADC1 to ADC5 Pins without MUX	ADC1 to ADC5 Pins with MUX
45µs	45µs	110µs	360µs

6.1.6 ADC Data Format

The data in all ADC registers are represented by 16-bit signed number with an LSB of 0.25mV (or 0.25°C for temperature readings). Some of the ADC inputs have an attenuation before the PGA, so the scaling factor in Table 25 is not the same for all channels.

To convert an ADC value to a real number, perform the following calculation:

1. Convert the digital value to a signed number.
2. Divide by the scaling factor specified in Table 25.

Examples:

- Channel VOUT_1_ADCMON_VOUT = 0x13E8 (decimal 5096)
  Value / Scaling_factor = 5096 / 4000 = 1.274V
- Channel ADCMON_Temp = 0xFFAD (decimal -83)
  Value / Scaling_factor = -83/4 = -20.75°C

6.2 Overvoltage (OV) and Undervoltage (UV) Monitoring

Using the SAR ADC, all the internal and external voltages of RAA271005/RAA271005L are continuously monitored and compared against a digital Overvoltage (OV) and Undervoltage (UV) value. If any of these signals is outside of the OV and UV levels, a protection fault is triggered.

The OV and UV levels for all internal and external regulators are factory programmed in one-time programmable memory, but they can be specified by the customer for each application. The full list of regulators that are monitored for OV and UV conditions are shown in Table 25.

Note: For OVP detection of AVIN1, a typical response time is given in the Electrical Specifications. There is also an expected maximum detection time for AVIN1 OVP of 11µsec (for a ±50mV step).

6.3 Over-Temperature Warning and Shutdown

Like OV and UV protection for voltages, the protection-side temperature sensor is monitored by the ADC and temperature thresholds can be set, namely, a Warning threshold and a Shutdown threshold. Both thresholds can be specified by the customer, are factory programmed in one-time programmable memory, and can be any temperature value with a resolution of 0.25°C.

6.4 Watchdog Timer (WDT)

RAA271005/RAA271005L contains a watchdog timer that can be used in several ways to ensure that the PMIC is still alive and able to respond to serial commands. The following are the three watchdog options available in RAA271005/RAA271005L:

- 16-question watchdog
- 4-question watchdog
- Windowed watchdog function

Note: Refer to *Safety Application Note* for proper configuration of the WDT in the OTP.

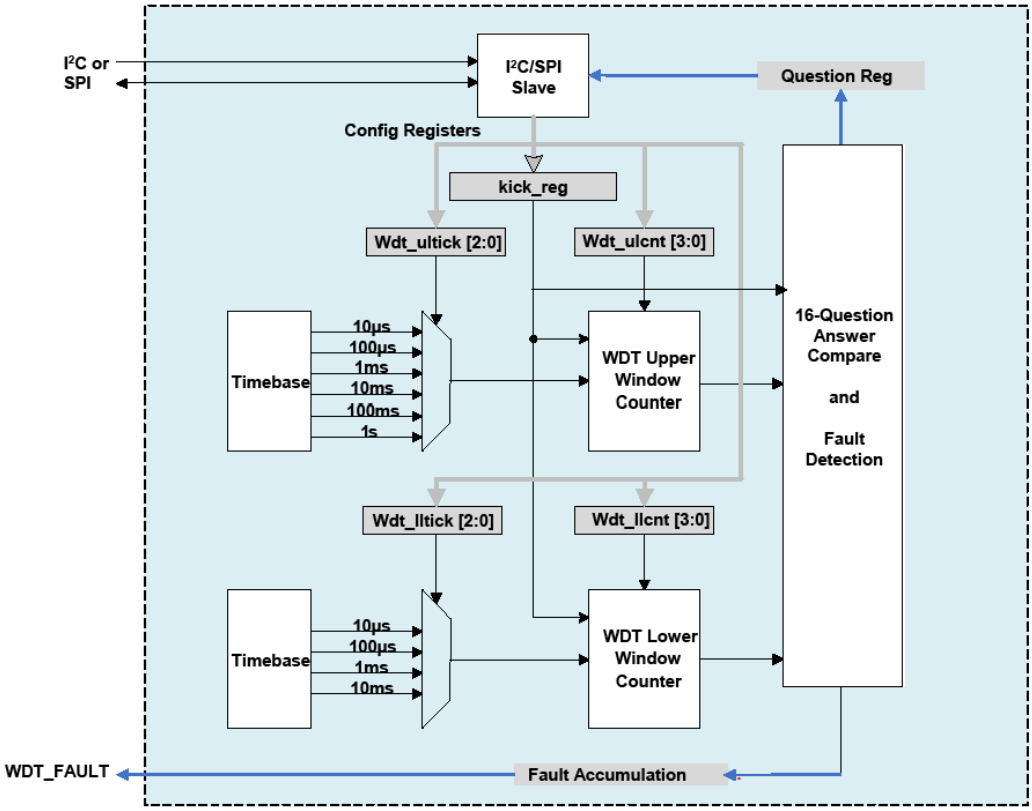


Figure 38. Watchdog Timer (WDT)

6.4.1 16-Question Watchdog Timer (QA16WDT)

In the 16-Question/Answer watchdog mode, the RAA271005/RAA271005L provides a token value by reading the top four bits of register 0x96 - WDT_LFSR. After sending the token, the RAA271005/RAA271005L expects the four answer bytes to be written to register 0x95 - WDT_KICK_REG in the order Answer-0, Answer-1, Answer-2, and Answer-3 with the values shown in Table 29.

Table 29. QA16WDT Questions and Answers

Token	Watchdog Answer			
	Answer-3	Answer-2	Answer-1	Answer-0
0x0	0xFF	0x0F	0xF0	0x00
0x1	0xB0	0x40	0xBF	0x4F
0x2	0xE9	0x19	0xE6	0x16
0x3	0xA6	0x56	0xA9	0x59
0x4	0x75	0x85	0x7A	0x8A
0x5	0x3A	0xCA	0x35	0xC5
0x6	0x63	0x93	0x6C	0x9C
0x7	0x2C	0xDC	0x23	0xD3
0x8	0xD2	0x22	0xDD	0x2D
0x9	0x9D	0x6D	0x92	0x62
0xA	0xC4	0x34	0xCB	0x3B
0xB	0x8B	0x7B	0x84	0x74
0xC	0x58	0xA8	0x57	0xA7
0xD	0x17	0xE7	0x18	0xE8
0xE	0x4E	0xBE	0x41	0xB1
0xF	0x01	0xF1	0x0E	0xFE

Note: It is possible to simplify the table slightly by noticing that some of the answers have just the MSB, LSB, or full value of Answer-0 flipped. Using C syntax:

- Answer-1 = Answer-0 ^ 0xF0
- Answer-2 = Answer-0 ^ 0x0F
- Answer-3 = Answer-0 ^ 0xFF

6.4.2 4-Question Watchdog Timer (QA4WDT)

The 4-Question/Answer watchdog mode is similar to the 16-Question/Answer watchdog mode, but the number of questions is reduced to four and there is only one answer. In QA4WDT mode, Bits [7:6] of register 0x096 - WDT_LFSR read the Token and Bits [5:0] compute the WD answer. As with the QA16WDT, the answer is written back to register 0x095 - WDT_KICK_REG.

Table 30. QA4WDT Questions and Answers

Token Read From WDT_LFSR		WD Answer To be written to WDT_KICK_REG
WDT_LFSR [7]	WDT_LFSR [6]	
0	0	WDT_LFSR [5:0]
0	1	WDT_LFSR [5:0] shifted 1 bit to the left

Table 30. QA4WDT Questions and Answers

1	0	WDT_LFSR [5:0] shifted 1 bit to the right
1	1	Inverse of WDT_LFSR <5:0>

6.4.3 Windowed Watchdog Timer (WWDT)

The watchdog function can also be used in a basic Windowed Kick mode. When configured in this way, the PMIC expects the value 0x2A to be continuously written to register 0x095 - WDT_KICK_REG within the configured time window.

6.5 Fault Reactions During Cold-Start and Deep Stop

- Faults during COLD_START – Protection block takes over; Regu hiccup counter does not increment. Re-start handled by FuSa SM. (Protection active; Low Iq control not asserted by Regulation block).
- Faults during DEEP_STOP and S2R – Handled by Regulation block, hiccup counter increments every fault. Happens until PWRCTL2 is received. After, if fault happens, hiccup counter not incremented (not in DEEP_STOP anymore).

6.6 Protection Interrupt Pin (IRQ#)

RAA271005/RAA271005L contains an interrupt pin (IRQ#) that reacts to faults in the protection digital. This pin is configured as push-pull output by default that is powered by the VIO supply and asserts LO when a fault is recorded. The interrupt pin can be configured in OTP as CMOS/OD output according to the application requirements.

IRQ# reacts to the following:

- Protection digital internal logic faults (such as self-test, clock monitor)
- Watchdog faults
- CRC communication faults
- AVIN/GND OV/UV faults
- Internal reference OV/UV faults
- Internal LDO OV/UV faults
- Buck regulator OV/UV faults
- LDO regulator OV/UV faults
- External ADC channel OV/UV faults
- Faults related to OTP (one-time programmable memory)

Note: A full list of faults and their reactions is located in the *RAA271005 Safety Application Note*.

7. Register Map

7.1 OTP Programmability

Please request OTP creator.

Note: An OTP download failure loads all registers back to defaults.

Note: NOC is referred to as LSWUC in the register maps; POC is referred to as HSWOC in the register maps.

7.2 Regulation Register Descriptions - Defaults

7.2.1 0x000 - IO_PAGE_REGU

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3:0	IO_PAGE	RW	Page selection for register table 0x0: Customer Page 0x1: Reserved 0x2: Reserved 0x3: Reserved	0x0

7.2.2 0x001 - IO_CHIPNAME_REGU

Bit	Name	R/W	Description	Default
7:0	IO_CHIPNAME	RO	Chip Name, Set by Renesas in metal 0x03: RAA271005/RAA271005L	0x03

7.2.3 0x002 - IO_CHIPVERSION_REGU

Bit	Name	R/W	Description	Default
7:0	IO_CHIPVERSION	RO	Chip Version, Set by Renesas in metal 0xA1: RAA271005A0 0xB1: RAA271005B0 0xC1: RAA271005C01 0xC2: RAA271005C02/ RAA271005LC02	0xC2

7.2.4 0x003 - IO_DIEID3_REGU

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	0xFE

7.2.5 0x004 - IO_DIEID2_REGU

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	0xDC

7.2.6 0x005 - IO_DIEID1_REGU

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	0xBA

7.2.7 0x006 - IO_DIEID0_REGU

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Byte 0 of Die ID set by Renesas (not checked by CRC in OTP)	0x98

7.2.8 0x00A - OTP_VERSION_REGU

Bit	Name	R/W	Description	Default
7:0	OTP_VERSION	RO	OTP version for registers in page 0x2	0x01

7.2.9 0x022 - IO_MODECTRL_REGU (OTP)

Bit	Name	R/W	Description	Default
7	IO_BUCK1_EN	RW	Enable for BUCK1 0x0: Buck1 Disabled 0x1: Buck1 Enabled	0x1
6	IO_BUCK2_EN	RW	Enable for BUCK2 0x0: Buck2 Disabled 0x1: Buck2 Enabled	0x1
5	IO_BUCK3_EN	RW	Enable for BUCK3 0x0: Buck3 Disabled 0x1: Buck3 Enabled	0x1
4	IO_BUCK4_EN	RW	Enable for BUCK4 0x0: Buck4 Disabled 0x1: Buck4 Enabled	0x1
3	IO_BUCK5_EN	RW	Enable for BUCK5 0x0: Buck5 Disabled 0x1: Buck5 Enabled	0x1
2	Reserved	RW	Reserved	0x0
1	Reserved	RW	Reserved	0x0
0	IO_REGVALID	RO	0x0: OTP not programmed 0x1: OTP Programmed	0x0

7.2.10 0x023 - IO_MODECTRL2_REGU (OTP)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0x0
5	IO_LDO6_EN	RW	Enable for LDO6 0x0: LDO6 Disabled 0x1: LDO6 Enabled	0x1
4	IO_LDO5_EN	RW	Enable for LDO5 0x0: LDO5 Disabled 0x1: LDO5 Enabled	0x1
3	IO_LDO4_EN	RW	Enable for LDO4 0x0: LDO4 Disabled 0x1: LDO4 Enabled	0x1
2	IO_LDO3_EN	RW	Enable for LDO3 0x0: LDO3 Disabled 0x1: LDO3 Enabled	0x1
1	IO_LDO2_EN	RW	Enable for LDO2 0x0: LDO2 Disabled 0x1: LDO2 Enabled	0x1
0	IO_LDO1_EN	RW	Enable for LDO1 0x0: LDO1 Disabled 0x1: LDO1 Enabled	0x1

7.2.11 0x02D - CHIPTSTATE_BUCK_PGOOD

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0x0
4	BUCK5_PGOODSTATE	RO	PGOOD for BUCK5	0x0
3	BUCK4_PGOODSTATE	RO	PGOOD for BUCK4	0x0
2	BUCK3_PGOODSTATE	RO	PGOOD for BUCK3	0x0
1	BUCK2_PGOODSTATE	RO	PGOOD for BUCK2	0x0
0	BUCK1_PGOODSTATE	RO	PGOOD for BUCK1	0x0

7.2.12 0x02E - CHIPTSTATE_LDO_PGOOD

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0x0
5	LDO6_PGOODSTATE	RO	PGOOD for LDO6	0x0
4	LDO5_PGOODSTATE	RO	PGOOD for LDO5	0x0
3	LDO4_PGOODSTATE	RO	PGOOD for LDO4	0x0
2	LDO3_PGOODSTATE	RO	PGOOD for LDO3	0x0
1	LDO2_PGOODSTATE	RO	PGOOD for LDO2	0x0
0	LDO1_PGOODSTATE	RO	PGOOD for LDO1	0x0

7.2.13 0x030 - FLT_MASK_OTP (OTP)

Bit	Name	R/W	Description	Default
7	FLT_MASKOTPPROGWARN	RW	Mask INT for OTP PROG WARN (1 out of 4 bit failed) 0x0: Passed to output pin 0x1: Masked from output pin	0x0
6	FLT_MASKOTPPROGADDR	RW	Mask INT for OTP PROG ADDR failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
5	FLT_MASKOTPPROG	RW	Mask INT for OTP PROG failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
4	FLT_MASKOTPINIT	RW	Mask INT for OTP INIT failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASKOTPCRCPAGE2	RW	Mask INT for OTP CRC Page 2 failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
2	FLT_MASKOTPCRCPAGE01	RW	Mask INT for OTP CRC Page 0 and Page 1 failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASKOTPTIMEOUT	RW	Mask INT for FLT_OTPTIMEOUT[0] Fault 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASKOTPNOTPGMD	RW	Mask INT for FLT_OTPNOTPGMD[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.14 0x031 - FLT_MASK_TEMP (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	FLT_MASK_INVALID_ DEEPSTOP	RW	Mask INT for INVALID_DEEPSTOP 0x0: Passed to output pin 0x1: Masked from output pin	0x0
5:0	Reserved	RO	Reserved	0x0

7.2.15 0x032 - FLT_MASK_BUCK1 (OTP)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0x0
4	FLT_MASK_BUCK1_LSWUC	RW	Mask INT for FLT_BUCK1_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_MASK_BUCK1_HSWOC	RW	Mask INT for FLT_BUCK1_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK1_OV	RW	Mask INT for FLT_BUCK1_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK1_UV	RW	Mask INT for FLT_BUCK1_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.16 0x033 - FLT_MASK_BUCK2 (OTP)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0x0
4	FLT_MASK_BUCK2_LSWUC	RW	Mask INT for FLT_BUCK2_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_MASK_BUCK2_HSWOC	RW	Mask INT for FLT_BUCK2_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK2_OV	RW	Mask INT for FLT_BUCK2_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK2_UV	RW	Mask INT for FLT_BUCK2_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.17 0x034 - FLT_MASK_BUCK3 (OTP)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0x0
4	FLT_MASK_BUCK3_LSWUC	RW	Mask INT for FLT_BUCK3_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_MASK_BUCK3_HSWOC	RW	Mask INT for FLT_BUCK3_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK3_OV	RW	Mask INT for FLT_BUCK3_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK3_UV	RW	Mask INT for FLT_BUCK3_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.18 0x035 - FLT_MASK_BUCK4 (OTP)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0x0
5	FLT_MASK_BUCK4_PVIN_OK	RW	Mask INT for FLT_BUCK4_PVIN_OK[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
4	FLT_MASK_BUCK4_LSWUC	RW	Mask INT for FLT_BUCK4_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_MASK_BUCK4_HSWOC	RW	Mask INT for FLT_BUCK4_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK4_OV	RW	Mask INT for FLT_BUCK4_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK4_UV	RW	Mask INT for FLT_BUCK4_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.19 0x036 - FLT_MASK_BUCK5 (OTP)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0x0
4	FLT_MASK_BUCK5_LSWUC	RW	Mask INT for FLT_BUCK5_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_MASK_BUCK5_HSWOC	RW	Mask INT for FLT_BUCK5_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK5_OV	RW	Mask INT for FLT_BUCK5_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK5_UV	RW	Mask INT for FLT_BUCK5_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.20 0x037 - FLT_MASK_LDO (OTP)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0x0
5	FLT_MASK_LDO6_UV	RW	Mask INT for FLT_LDO6_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
4	FLT_MASK_LDO5_UV	RW	Mask INT for FLT_LDO5_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASK_LDO4_UV	RW	Mask INT for FLT_LDO4_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
2	FLT_MASK_LDO3_UV	RW	Mask INT for FLT_LDO3_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_LDO2_UV	RW	Mask INT for FLT_LDO2_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_LDO1_UV	RW	Mask INT for FLT_LDO1_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.21 0x038 - FLT_MASK_IF (OTP)

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	0x00
2	FLT_MASK_VBAT_OV	RW	Mask INT for FLT_VBAT_OV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_SPI	RW	Mask INT for FLT_SPI 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_I2C	RW	Mask INT for FLT_I2C 0x0: Passed to output pin 0x1: Masked from output pin	0x0

7.2.22 0x040 - FLT_RECORD_OTP

Bit	Name	R/W	Description	Default
7	FLT_OTPPROGWARN	RW	OTP Program Warning that one of the 4 bits in diff/redundant prog mode failed. Read returns status. Write 0 to clear. 0x0: All 4 bits programmed correctly 0x1: 1 out of 4 bits programmed incorrectly but overall bit is correct	0x0
6	FLT_OTPPROGADDR	RW	OTP PROG ADDR failure. Read returns status. Write 0 to clear. 0x0: Programming address is in the correct range 0x1: Programming address is out of acceptable range	0x0
5	FLT_OTPPROG	RW	OTP PROG failure. Read returns status. Write 0 to clear. 0x0: Programming passed 0x1: Programming failed	0x0
4	FLT_OTPINIT	RW	OTP INIT failure. Read returns status. Write 0 to clear. 0x0: Read Initialization passed 0x1: Read Initialization failed	0x0
3	FLT_OTPCRCPAGE2	RW	OTP CRC Failure on Page 2. Read returns status. Write 0 to clear. 0x0: No OTP Failure 0x1: OTP CRC Failure	0x0
2	FLT_OTPCRCPAGE01	RW	OTP CRC Failure on Page 0 or Page 1. Read returns status. Write 0 to clear. 0x0: No OTP Failure 0x1: OTP CRC Failure	0x0
1	FLT_OTPTIMEOUT	RW	OTP Read Duration Fault. Read returns status. Write 0 to clear. 0x0: No OTP Read Duration Fault 0x1: OTP Read Duration ≥ 256*Low Freq Clock Periods (~8ms)	0x0
0	FLT_OTPNOTPGMD	RW	Read of OTP to see if OTP has been programmed. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0

7.2.23 0x041 - FLT_RECORD_TEMP

Bit	Name	R/W	Description	Default
7	FLT_BOOT	RW	BOOT occurred. Read returns status. Write 0 to clear. Informative only. Does not assert interrupt. 0x0: No boot process has occurred since the last time this register was read. 0x1: Boot process has occurred (set high after OTP Read is finished)	0x0
6	FLT_INVALID_DEEPSTOP	RW	Invalid DeepSTOP detected. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
5:2	Reserved	RO	Reserved	0x0
1	FLT_TEMPSDR	RW	Over-Temperature (OT) Shutdown (rising threshold). Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
0	FLT_TEMPSDF	RW	Over-Temperature (OT) Shutdown (falling edge) (Shutdown – Hysteresis). Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0

7.2.24 0x042 - FLT_RECORD_BUCK1

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	FLT_BUCK1_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
5	Reserved	RO	Reserved	0x0
4	FLT_BUCK1_LSWUC	RW	LS Way Under Current (WOC) for BUCK1. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_BUCK1_HSWOC	RW	HS Way Overcurrent (WOC) for BUCK1. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
1	FLT_BUCK1_OV	RW	Overvoltage (OV) for BUCK1. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
0	FLT_BUCK1_UV	RW	Undervoltage (UV) for BUCK1. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0

7.2.25 0x043 - FLT_RECORD_BUCK2

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	FLT_BUCK2_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
5	Reserved	RO	Reserved	0x0
4	FLT_BUCK2_LSWUC	RW	LS Way Under Current (WOC) for BUCK2. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_BUCK2_HSWOC	RW	HS Way Overcurrent (WOC) for BUCK2. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
1	FLT_BUCK2_OV	RW	Overvoltage (OV) for BUCK2. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
0	FLT_BUCK2_UV	RW	Undervoltage (UV) for BUCK2. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0

7.2.26 0x044 - FLT_RECORD_BUCK3

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	FLT_BUCK3_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
5	Reserved	RO	Reserved	0x0
4	FLT_BUCK3_LSWUC	RW	LS Way Under Current (WOC) for BUCK3. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_BUCK3_HSWOC	RW	HS Way Overcurrent (WOC) for BUCK3. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
1	FLT_BUCK3_OV	RW	Overvoltage (OV) for BUCK3. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
0	FLT_BUCK3_UV	RW	Undervoltage (UV) for BUCK3. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0

7.2.27 0x045 - FLT_RECORD_BUCK4

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	FLT_BUCK4_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
5	Reserved	RO	Reserved	0x0
5	FLT_BUCK4_PVIN4_OK	RW	PVIN4_OK for BUCK4. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0
4	FLT_BUCK4_LSWUC	RW	LS Way Under Current (WOC) for BUCK4. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_BUCK4_HSWOC	RW	Way Overcurrent (WOC) for BUCK4. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
1	FLT_BUCK4_OV	RW	Overvoltage (OV) for BUCK4. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
0	FLT_BUCK4_UV	RW	Undervoltage (UV) for BUCK4. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0

7.2.28 0x046 - FLT_RECORD_BUCK5

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	FLT_BUCK5_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
5	Reserved	RO	Reserved	0x0
4	FLT_BUCK5_LSWUC	RW	LS Way Under Current (WOC) for BUCK5. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
3	Reserved	RO	Reserved	0x0
2	FLT_BUCK5_HSWOC	RW	Way Overcurrent (WOC) for BUCK5. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
1	FLT_BUCK5_OV	RW	Overvoltage (OV) for BUCK5. Read returns status. Write 0 to clear. 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold	0x0
0	FLT_BUCK5_UV	RW	Undervoltage (UV) for BUCK5. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0

7.2.29 0x047 - FLT_RECORD_LDO

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0x0
5	FLT_LDO6_UV	RW	Undervoltage (UV) for LDO6. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0
4	FLT_LDO5_UV	RW	Undervoltage (UV) for LDO5. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0
3	FLT_LDO4_UV	RW	Undervoltage (UV) for LDO4. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0
2	FLT_LDO3_UV	RW	Undervoltage (UV) for LDO3. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0
1	FLT_LDO2_UV	RW	Undervoltage (UV) for LDO2. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0
0	FLT_LDO1_UV	RW	Undervoltage (UV) for LDO1. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0

7.2.30 0x048 - FLT_RECORD_IF

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	0x00
2	FLT_VBAT_OV	RW	VBAT Over voltage. Read returns status. Write 0 to clear. 0x0: No fault, greater than threshold 0x1: Fault, less than threshold	0x0
1	FLT_SPI	RW	SPI CRC error. Read returns status. Write 0 to clear. 0x0: No fault detected 0x1: Fault detected	0x0
0	FLT_I2C	RW	I^2C CRC error. Read returns status. Write 0 to clear. 0x0: No fault detected 0x1: Fault detected	0x0

7.2.31 0x049 - FLT_RECORD_LDO_DISC_DET

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0x0
5	FLT_LDO6_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
4	FLT_LDO5_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
3	FLT_LDO4_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
2	FLT_LDO3_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
1	FLT_LDO2_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0
0	FLT_LDO1_DISC_DET	RW	Discharge Detect error. Read returns status. Write 0 to clear. 0x0: No fault 0x1: Fault	0x0

7.2.32 0x04C – IO_GP3CFGMSB

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3:2	IO_GP3PULLUPDOWN	RW	Selects pull-up on IO14/IRQ# pin. 0x0: No pull-up or pull-down 0x1: Pull-down of 10uA/180kohms 0x2: Pull-up of 22.5uA/80kohms 0x3: Pull-up of 1uA/1.8Mohms	0x0
1:0	IO_GP3DRIVE	RW	Selects output drive strength of IO14/IRQ# pin. 0x0: Min (20% of Max) 0x1: 50% of Max 0x2: 80% of Max 0x3: Max	0x0

7.2.33 0x04D – IO_GP3CFGLSB

Bit	Name	R/W	Description	Default
7	IO_GP3DIGDIRECTION	RW	Digital Data Direction of IO14/IRQ# 0x0: Output IO acts like an output 0x1: IO devices as turned off and functions as input	0x0
6	IO_GP3OPENDRAIN	RW	Modifies digital output mode of IO14/IRQ# pin. 0x0: Configure as a CMOS output buffer 0x1: Configure as an open drain with pull-up/pull-down set by IO_GP3PULLUPDOWN	0x0
5	IO_GP3INVERT	RW	Polarity control for IO14/IRQ# pin. 0x0 Noninverting buffers used 0x1: Inverting buffers used	0x0
4	IO_GP3I2CGLTCHFLTR	RW	Enable I^2C Glitch (receive) filter. 0x0: I^2C glitch filter not enabled 0x1: I^2C glitch filter enabled	0x0
3	IO_GP3I2CSLEWFLTR	RW	Enable I^2C Slew (transmit) filter. 0x0: I^2C slew filter not enabled 0x1: I^2C slew filter enabled	0x0
2:0	Reserved	RO	Reserved	0x0

7.2.34 0x056 - IO_GPIO_DATAIN

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	
2:0	IO_GPIO_DATAIN	RO	Bit2: IO5; Bit1: IO4; Bit0:IO3	0x0

7.2.35 0x057 - IO_GPIO_DATAOUT

Bit	Name	R/W	Description	Default
7:7	Reserved	RO	Reserved	
6:0	IO_GPIO_DATAOUT	RW	Bit6: IO19; Bit5: IO14; Bit4: IO13; Bit3: IO6; Bit2: IO5; Bit1: IO4; Bit0:IO3	0x0

7.2.36 0x05C - IO_GPIO_0_DATAOUT_UP_DLY

Bit	Name	R/W	Description	Default
7:0	GP_0_DOUT_UP_DLY	RW	Up delay for IO4	0x0

7.2.37 0x05D - IO_GPIO_0_DATAOUT_DN_DLY

Bit	Name	R/W	Description	Default
7:0	GP_0_DOUT_DN_DLY	RW	Down delay for IO4	0x0

7.2.38 0x05E - IO_GPIO_1_DATAOUT_UP_DLY

Bit	Name	R/W	Description	Default
7:0	GP_1_DOUT_UP_DLY	RW	Up delay for IO5	0x0

7.2.39 0x05F - IO_GPIO_1_DATAOUT_DN_DLY

Bit	Name	R/W	Description	Default
7:0	GP_1_DOUT_DN_DLY	RW	Down delay for IO5	0x0

7.2.40 0x060 - IO_GPIO_2_DATAOUT_UP_DLY

Bit	Name	R/W	Description	Default
7:0	GP_2_DOUT_UP_DLY	RW	Up delay for IO6	0x0

7.2.41 0x061 - IO_GPIO_2_DATAOUT_DN_DLY

Bit	Name	R/W	Description	Default
7:0	GP_2_DOUT_DN_DLY	RW	Down delay for IO6	0x0

7.2.42 0x062 - IO_GPIO_3_DATAOUT_UP_DLY

Bit	Name	R/W	Description	Default
7:0	GP_3_DOUT_UP_DLY	RW	Up delay for IO13	0x0

7.2.43 0x63 - IO_GPIO_3_DATAOUT_DN_DLY

Bit	Name	R/W	Description	Default
7:0	GP_3_DOUT_DN_DLY	RW	Down delay for IO13	0x0

7.2.44 0x06F - LOCK_OUT_CFG

Bit	Name	R/W	Description	OTP	Default
7:0	LOCK_OUT_CFG	RW	Bitwise mask to block write controls to Regulation block register map.	0x0	0x00

7.2.45 0x070 - BUCK1_DVS0CFG1 (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK1_DVS0VOUT92	RW	Upper 8 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0	0xD7

7.2.46 0x071 - BUCK1_DVS0CFG0 (OTP)

Bit	Name	R/W	Description	Default
7:6	BUCK1_DVS0VOUT10	RW	Lower 2 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0 *Note:* When DVS configuration 0 is selected (via pins or registers) any write to BUCK_DVS0CFG0 causes a DVS ramping to occur	0x3
5	BUCK1_DVS0DECAY	RW	Buck DECAY for DVS Config 0. *Note:* Set BUCK_DECAYCOMP[0] = 0x1 to enable comparator 0x0: Active pull down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO	Reserved	0x0
0	BUCK1_DVS0BPS4	RW	Buck Power State Mode for DVS Config 0 0x0: BPS0 Multiphase DCM/CCM 0x1: BPS1 DAC 0V, Tristate Output (higher IQ, Faster recovery)	0x0

7.2.47 0x072 - BUCK1_DVS1CFG1 (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK1_DVS1VOUT92	RW	Upper 8 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0	0xAD

7.2.48 0x073 - BUCK1_DVS1CFG0 (OTP)

Bit	Name	R/W	Description	Default
7:6	BUCK1_DVS1VOUT10	RW	Lower 2 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0 *Note:* When DVS configuration 0 is selected (via pins or registers) any write to BUCK_DVS0CFG0 causes a DVS ramping to occur	0x3
5	BUCK1_DVS1DECAY	RW	Buck DECAY for DVS Config 0. *Note:* Set BUCK_DECAYCOMP[0] = 0x1 to enable comparator 0x0: Active pull down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO	Reserved	0x0
0	BUCK1_DVS1BPS4	RW	Buck Power State Mode for DVS Config 0 0x0: BPS0 Multiphase DCM/CCM 0x1: BPS1 DAC 0V, Tristate Output (higher IQ, Faster recovery)	0x0

7.2.49 0x075 - BUCK1_DVSSEL (OTP)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0x00
1	BUCK1_DVSCTRL	RW	BUCK DVS Control. DVS_1 DVS_0 Active DVS Configuration registers. 0x0: Use BUCK_DVSSELECT[0] to select active DVS configuration 0x1: Use DVS Pin to control DVS selection	0x0
0	BUCK1_DVSSELECT	RW	BUCK DVS Selection. *Note:* When BUCK_DVSCTRL[0] = 0x0 any write to the register BUCK_DVSSEL causes a DVS ramping event to occur 0x0: Use DVS Config 0 in BUCK_DVS0CFG and BUCK_DVS0VOUT 0x1: Use DVS Config 1 in BUCK_DVS1CFG and BUCK_DVS1VOUT	0x0

7.2.50 0x076 - BUCK1_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK1_EN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.51 0x077 - BUCK1_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK1_SHUTDN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.52 0x080 - BUCK2_DVS0CFG1 (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK2_DVS0VOUT92	RW	Upper 8 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0	0xFF

7.2.53 0x081 - BUCK2_DVS0CFG0 (OTP)

Bit	Name	R/W	Description	Default
7:6	BUCK2_DVS0VOUT10	RW	Lower 2 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0 *Note:* When DVS configuration 0 is selected (via pins or registers) any write to BUCK_DVS0CFG0 causes a DVS ramping to occur	0x3
5	BUCK2_DVS0DECAY	RW	Buck DECAY for DVS Config 0 0x0: Active pull down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate) *Note:* Set BUCK_DECAYCOMP[0] = 0x1 to enable comparator	0x0
4:1	Reserved	RO	Reserved	0x0
0	BUCK2_DVS0BPS4	RW	Buck Power State Mode for DVS Config 0 0x0: BPS0 Multiphase DCM/CCM 0x1: BPS1 DAC 0V, Tristate Output (higher IQ, Faster recovery)	0x0

7.2.54 0x086 - BUCK2_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK2_EN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.55 0x087 - BUCK2_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK2_SHUTDN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.56 0x090 - BUCK3_DVS0CFG1 (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK3_DVS0VOUT92	RW	Upper 8 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0	0xFF

7.2.57 0x091 - BUCK3_DVS0CFG0 (OTP)

Bit	Name	R/W	Description	Default
7:6	BUCK3_DVS0VOUT10	RW	Lower 2 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0 *Note:* When DVS configuration 0 is selected (via pins or registers) any write to BUCK_DVS0CFG0 causes a DVS ramping to occur	0x3
5	BUCK3_DVS0DECAY	RW	Buck DECAY for DVS Config 0 0x0 Active pull down, decay determined by selected slew rate 0x1 Decay Mode (load determines slew rate) *Note:* Set BUCK_DECAYCOMP[0] = 0x1 to enable comparator	0x0
4:1	Reserved	RO	Reserved	0x0
0	BUCK3_DVS0BPS4	RW	Buck Power State Mode for DVS Config 0 0x0 BPS0 Multiphase DCM/CCM 0x1 BPS1 DAC 0V, Tristate Output (higher IQ, Faster recovery)	0x0

7.2.58 0x096 - BUCK3_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK3_EN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.59 0x097 - BUCK3_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK3_SHUTDN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.60 0x0A0 - BUCK4_DVS0CFG1 (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK4_DVS0VOUT92	RW	Upper 8 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0	0xFF

7.2.61 0x0A1 - BUCK4_DVS0CFG0 (OTP)

Bit	Name	R/W	Description	Default
7:6	BUCK4_DVS0VOUT10	RW	Lower 2 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0 *Note:* When DVS configuration 0 is selected (via pins or registers) any write to BUCK_DVS0CFG0 causes a DVS ramping to occur	0x3
5	BUCK4_DVS0DECAY	RW	Buck DECAY for DVS Config 0 0x0 Active pull down, decay determined by selected slew rate 0x1 Decay Mode (load determines slew rate) *Note:* Set BUCK_DECAYCOMP[0] = 0x1 to enable comparator	0x0
4:1	Reserved	RO	Reserved	0x0
0	BUCK4_DVS0BPS4	RW	Buck Power State Mode for DVS Config 0 0x0 BPS0 Multiphase DCM/CCM 0x1 BPS1 DAC 0V, Tristate Output (higher IQ, Faster recovery)	0x0

7.2.62 0x0A6 - BUCK4_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK4_EN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.63 0x0A7 - BUCK4_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK4_SHUTDN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.64 0x0B0 - BUCK5_DVS0CFG1 (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK5_DVS0VOUT92	RW	Upper 8 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0	0xFF

7.2.65 0x0B1 - BUCK5_DVS0CFG0 (OTP)

Bit	Name	R/W	Description	Default
7:6	BUCK5_DVS0VOUT10	RW	Lower 2 bits of 10 bit DAC[9:0] value to generate VOUT for DVS Config 0 *Note:* When DVS configuration 0 is selected (via pins or registers) any write to BUCK_DVS0CFG0 causes a DVS ramping to occur	0x3
5	BUCK5_DVS0DECAY	RW	Buck DECAY for DVS Config 0 0x0 Active pull down, decay determined by selected slew rate 0x1 Decay Mode (load determines slew rate) *Note:* Set BUCK_DECAYCOMP[0] = 0x1 to enable comparator	0x0
4:1	Reserved	RO	Reserved	0x0
0	BUCK5_DVS0BPS4	RW	Buck Power State Mode for DVS Config 0 0x0 BPS0 Multiphase DCM/CCM 0x1 BPS1 DAC 0V, Tristate Output (higher IQ, Faster recovery)	0x0

7.2.66 0x0B6 - BUCK5_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK5_EN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.67 0x0B7 - BUCK5_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	BUCK5_SHUTDN_DLY	RW	Delay time from BUCK_EN pin to BUCK_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.68 0x0C3 - LDO1_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO1_EN_DLY	RW	Delay time from LDO_EN pin to LDO_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.69 0x0C4 - LDO1_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO1_SHUTDN_DLY	RW	Delay time from LDO_EN pin to LDO_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.70 0x0C5 - LDO2_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO2_EN_DLY	RW	Delay time from LDO_EN pin to LDO_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.71 0x0C6 - LDO2_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO2_SHUTDN_DLY	RW	Delay time from LDO_EN pin to LDO_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.72 0x0C7 - LDO3_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO3_EN_DLY	RW	Delay time from LDO_EN pin to LDO_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.73 0x0C8 - LDO3_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO3_SHUTDN_DLY	RW	Delay time from LDO_EN pin to LDO_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.74 0x0C9 - LDO4_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO4_EN_DLY	RW	Delay time from LDO_EN pin to LDO_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.75 0x0CA - LDO4_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO4_SHUTDN_DLY	RW	Delay time from LDO_EN pin to LDO_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.76 0x0CB - LDO5_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO5_EN_DLY	RW	Delay time from LDO_EN pin to LDO_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.77 0x0CC - LDO5_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO5_SHUTDN_DLY	RW	Delay time from LDO_EN pin to LDO_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.78 0x0CD - LDO6_EN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO6_EN_DLY	RW	Delay time from LDO_EN pin to LDO_en control asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.79 0x0CE - LDO6_SHUTDN_DLY (OTP)

Bit	Name	R/W	Description	Default
7:0	LDO6_SHUTDN_DLY	RW	Delay time from LDO_EN pin to LDO_en control de-asserted. Delay = (integer value of register) ms [0.25ms/LSB]	0x00

7.2.80 0x0CF - HICCUP_RESTRT_DLY (OTP)

Bit	Name	R/W	Description	Default
7	FAULT_DNDLY	RW	Fault Down Delay: all regulator faults delayed 0x0: Do not delay 0x1: Delay faults	0x0
6	Reserved	RO	Reserved	0x0
5:0	HICCUP_RESTRT_DLY	RW	Restart delay time for LDO after faulting when hiccup is enabled. Delay = (integer value of register) ms (0.25ms/LSB) Value is used for LDO1 and LDO2	0x01

7.2.81 0x0D0 - HICCUP_CNT_LIM (OTP)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0x00
1:0	HICCUP_CNT_LIM	RW	Limit of hiccup events 0: infinite 1: 4 times 2: 8 times 3: 15 times	0x0

7.2.82 0x0D1 - DISC_DET_CFG (OTP)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x00
3:1	DISC_TOUT	RW	Discharge Detect Timeout 0x0: 1ms (LDO, BUCK) 0x1: 5ms (LDO, BUCK) 0x2: 10ms (LDO, BUCK) 0x3: 20ms (LDO, BUCK) 0x4: 40ms (LDO), 32ms (BUCK) 0x5: 60ms (LDO), 112ms (BUCK) 0x6: 100ms (LDO), 112ms (BUCK) 0x7: 150ms (LDO), 112ms (BUCK)	0x0
0	EN_DISC_DET	RW	Control of Discharge Detect for all regulators 0x0: Disabled 0x1: Enabled	0x0

7.2.83 0x0D2 - BUCK_DISC_VTH0 (OTP)

Bit	Name	R/W	Description	Default
7:6	BUCK4_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0
5:4	BUCK3_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0
3:2	BUCK2_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0
1:0	BUCK1_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0

7.2.84 0x0D3 - BUCK_DISC_VTH1 (OTP)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0x00
1:0	BUCK5_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0

7.2.85 0x0D4 - LDO_DISC_VTH0 (OTP)

Bit	Name	R/W	Description	Default
7:6	LDO4_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0
5:4	LDO3_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0
3:2	LDO2_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0
1:0	LDO1_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0

7.2.86 0x0D5 - LDO_DISC_VTH1 (OTP)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3:2	LDO6_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0
1:0	LDO5_DISC_VTH	RW	Discharge level selection 0x0: 150mV 0x1: 200mV 0x2: 250mV 0x3: 300mV	0x0

7.2.87 0x0D6 – MISC_CTRL_REGU (OTP)

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	0x00
2	FLT_CTRL_INVALID_DEEPSTOP	RW	Invalid DeepSTOP fault reaction mask 0: React 1: No reaction	0x0
1:0	LOCK_RELEASE_Pinsel	RW	Control how ADC3 pin is used to release from lock states caused by faults 0x0: Rising edge 0x1: Falling edge 0x2: High 0x3: Disable	0x1

7.2.88 0x125 – IO_PD (OTP)

Bit	Name	R/W	Description	Default
7:6	REQ_LOWIQB_CFG	RW	0x0: Always tied high 0x1: Following PWRCTL2 0x2: With BACKUP_CTRL[1] register write (When software based entry to S2R is used) 0x3: PWRCTL2 & register write (Secure option for pin controlled protection reset)	0x0
5:0	Reserved	RO	Reserved	0x1F

7.2.89 0x176 - BACKUP_CFG (OTP)

Bit	Name	R/W	Description	Default
7	REQ_LOWIQB_PIN_SEC	RW	Secure option for pin controlled Deep Stop entry. Both PWRCTRL2 activation & writing this bit = 0x1, must be done. Register IO_PD[7:6]: REQ_LOWIQB_CFG must be set to 0x3 to allow this secure setup.	0x0
6:1	Reserved	RO	Reserved	0x0
0	BACKUP_CTRL	RW	0x0 = BKUP signal is asserted low 0x1 = BKUP signal is asserted high	0x0

7.2.90 0x223 - I_IO_INTERNALVERSION_REGU (OTP)

Bit	Name	R/W	Description	Default
7:0	I_IO_INTERNALVERSION	RW	Internal chip version set by Renesas	0x01

7.3 Protection Register Descriptions - Defaults

7.3.1 0x000 - IO_PAGE

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3:0	IO_PAGE	RW	Page selection for register table 0x0: Customer Page 0x1: Reserved (Renesas only page. Can write to page 1 registers only if IO_KEY[3:0][7:0] is same I_IOSTOREDKEY[3:0][7:0] (stored key). 0x2: Reserved 0x3: Reserved	0x0

7.3.2 0x001 - IO_CHIPNAME

Bit	Name	R/W	Description	Default
7:0	IO_CHIPNAME	RO	Chip Name 0x3: RAA271005/RAA271005L	0x01

7.3.3 0x002 - IO_CHIPVERSION

Bit	Name	R/W	Description	Default
7:0	IO_CHIPVERSION	RO	Chip Version, Set by Renesas in metal 0xA1: RAA271005A0 0xB1: RAA271005B0 0xC1: RAA271005C01 0xC2: RAA271005C02/ RAA271005LC02	0xC2

7.3.4 0x003 - IO_DIEID3

Bit	Name	R/W	Description	Default
7:0	IO_DIEID3	RO	Die ID3. The die ID is a 32-bit value compose of (IO_DIEID3 + IO_DIEID2 + IO_DIEID1 + IO_DIEID0). This register is the MSB value of the die ID. *Note:* this register is not CRC checked during OTP operation.	0xFE

7.3.5 0x004 - IO_DIEID2

Bit	Name	R/W	Description	Default
7:0	IO_DIEID2	RO	Die ID2. The die ID is a 32-bit value compose of (IO_DIEID3 + IO_DIEID2 + IO_DIEID1 + IO_DIEID0). This register is the 2nd MSB value of the die ID. *Note:* this register is not CRC checked during OTP operation.	0xDC

7.3.6 0x005 - IO_DIEID1

Bit	Name	R/W	Description	Default
7:0	IO_DIEID1	RO	Die ID1. The die ID is a 32-bit value compose of (IO_DIEID3 + IO_DIEID2 + IO_DIEID1 + IO_DIEID0). This register is the 2nd LSB value of the die ID. *Note:* this register is not CRC checked during OTP operation.	0xBA

7.3.7 0x006 - IO_DIEID0

Bit	Name	R/W	Description	Default
7:0	IO_DIEID0	RO	Die ID0. The die ID is a 32-bit value compose of (IO_DIEID3 + IO_DIEID2 + IO_DIEID1 + IO_DIEID0). This register is the LSB value of the die ID. *Note:* this register is not CRC checked during OTP operation.	0x98

7.3.8 0x007 - IO_CHIPSTATE

Bit	Name	R/W	Description	Default
7	BG_BANDGAPOK	RO	Bandgap Status 0x0: NOT OK 0x1: OK	0x0
6	INTLDO_VDDOK	RO	Internal LDOs status 0x0: NOT OK 0x1: Ok	0x0
5	INTERRUPT	RO	INTERRUPT bit asserts when any type of Fault happens. It includes all faults of internal and external LDOs and all BUCKs from ADC monitoring system, plus all faults of WDT, CRC, ClkMon, FaultDetectBist and LBIST.	0x0

7.3.9 0x008 - FUSA_CTRL_1_A

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3:2	SDO_1_ASSERT	RW	Assert SDO2 to selected logic level 0x0: No assert 0x1: Assert high 0x2: Assert low 0x3: Tri-stated	0x0
1:0	SDO_0_ASSERT	RW	Assert SDO1 to selected logic level 0x0: No assert 0x1: Assert high 0x2: Assert low 0x3: Tri-stated	0x0

7.3.10 0x009 - FUSA_CTRL_2

Bit	Name	R/W	Description	Default
7:0	SINT_CHK_START	RW	Writing Non-Zero value to this register starts the Serial Interface Test (SINT). (*Note:* Refer to the *Safety Application Note* for SINT details)	0x00

7.3.11 0x00A - FUSA_CTRL_3

Bit	Name	R/W	Description	Default
7:0	SINT_CHK_RW	RW	SoC writes data read from FUSA_SOC_CHK_1 register here for SINT. (*Note:* Refer to the *Safety Application Note* for SINT details)	0x00

7.3.12 0x00B - FUSA_CTRL_4

Bit	Name	R/W	Description	Default
7:6	EXT_PIN_CHK_TIME	RW	Delay time for PMIC to verify expected pin states after FUSA_CTRL_4 register write. 0x0: 4µs 0x1: 8µs 0x2: 16µs 0x3: 32µs	0x0
5:0	EXT_PIN_CHK	RW	[5]: Global enable for external pin check2 0x0: Check disabled 0x1: Check enabled [4]: Expected state for signal SDI_1 0x0: Expected state low 0x1: Expected state high [3]: Expected state for signal PRESETOUT 0x0: Expected state low 0x1: Expected state high [2]: Expected state for signal SDI_2 0x0: Expected state low 0x1: Expected state high [1]: Expected state for signal SDI_3 0x0: Expected state low 0x1: Expected state high [0]: Expected state for signal SDI_4 0x0: Expected state low 0x1: Expected state high	0x00

7.3.13 0x00C - FUSA_CTRL_5

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	0x00
2	FORCE_ST_OPT	RW	0x0: User must write 0x0 to this register for getting out of FORCED (RESET/ ERROR) state after writing Non-Zero value. 0x1: User does not need to reset this register to get out of FORCED state. FuSa state m/c transition to next state. (*Note:* Refer to the *Safety Application Note* for Force Error/Reset functionality)	0x0
1:0	FORCE_ST_ERROR_RESET	RW	Writing non zero value forces FuSa state m/c transition to requested state:RESET, ERROR or ACTIVE state. 0x0: Do nothing. 0x1: To RESET state 0x2: To ERROR state 0x3:To ACTIVE state (*Note:* Forcing to ACTIVE state must also have I_DEBUG1_CFG_I_dbg_func[3] set to b'1'.)	0x0

7.3.14 0x00D - FUSA_CHK_CVM1

Bit	Name	R/W	Description	Default
7	CVM_TEST_DONE	RO	0x0: CVM Test is not done 0x1: CVM Test is done	0x0
6:5	CVM_TEST_FAIL	RO	Fault status of current CVM test slot 0x0: No fault. 0x1: Fault in measurements done through ADC1 channel 0x2: Fault in measurements done through ADC2 channel 0x3: Fault in both channels. (*Note:* Valid during CVM tests only)	0x0
4:1	Reserved	RO	Reserved	0x0
0	CVM_TEST_START	RW	0x0: Do nothing 0x1: Starts the CVM test (*Note:* Refer to the *Safety Application Note* for CVM test details)	0x0

7.3.15 0x00E - FUSA_STATUS_CVM1

Bit	Name	R/W	Description	Default
7:6	CVM_TEST_FAIL_3	RO	CVM Test Slot3 status register. 0x0: ADC2 pass, ADC1 pass 0x1: ADC2 pass, ADC1 fail 0x2: ADC2 fail, ADC1 pass 0x3: ADC2 fail, ADC1 fail	0x0
5:4	CVM_TEST_FAIL_2	RO	CVM Test Slot2 status register. 0x0: ADC2 pass, ADC1 pass 0x1: ADC2 pass, ADC1 fail 0x2: ADC2 fail, ADC1 pass 0x3: ADC2 fail, ADC1 fail	0x0
3:2	CVM_TEST_FAIL_1	RO	CVM Test Slot1 status register. 0x0: ADC2 pass, ADC1 pass 0x1: ADC2 pass, ADC1 fail 0x2: ADC2 fail, ADC1 pass 0x3: ADC2 fail, ADC1 fail	0x0
1:0	Reserved	RO	Reserved	0x0

7.3.16 0x00F - FUSA_STATUS_CVM2

Bit	Name	R/W	Description	Default
7:6	CVM_TEST_FAIL_7	RO	(*** Not Used ***)	0x0
5:4	CVM_TEST_FAIL_6	RO	CVM Test Slot6 status register. 0x0: ADC2 pass, ADC1 pass 0x1: ADC2 pass, ADC1 fail 0x2: ADC2 fail, ADC1 pass 0x3: ADC2 fail, ADC1 fail	0x0
3:2	CVM_TEST_FAIL_5	RO	CVM Test Slot5 status register. 0x0: ADC2 pass, ADC1 pass 0x1: ADC2 pass, ADC1 fail 0x2: ADC2 fail, ADC1 pass 0x3: ADC2 fail, ADC1 fail	0x0
1:0	CVM_TEST_FAIL_4	RO	CVM Test Slot4 status register. 0x0: ADC2 pass, ADC1 pass 0x1: ADC2 pass, ADC1 fail 0x2: ADC2 fail, ADC1 pass 0x3: ADC2 fail, ADC1 fail	0x0

7.3.17 0x010 - FUSA_STATUS_1

Bit	Name	R/W	Description	Default
7:5	SAFETY_CRTL_STATE	RO	Status register showing current FuSa state (Safety Control State) 0x0: POWER OFF 0x1: SELF DIAGNOSIS 0x2: POWERUP SEQ 0x3: SOC ACTIVATION 0x4: ACTIVE 0x5: RESET 0x6: ERROR 0x7: LOCK	0x0
4	SOC_ACTIVATED	RO	0x0: SoC Activation tests are being performed or failed. 0x1: Sock Activation tests passed.	0x0
3	WDT_FirstMSG_done	RO	0x0: First WDT message not received in SOC ACT. state. 0x1: First WDT message received in SOC ACT. state.	0x0
2:0	SocActiva_STATE	RO	Status register value represents current state of SOC testing state m/c with in SoC Activation FuSa State 0x0: IDLE 0x4: EXT PIN CHK 1 0x5: SINT CHK 0x6: EXT PIN CHK 2 0x7: START_WDT	0x0

7.3.18 0x011 - FUSA_STATUS_2

Bit	Name	R/W	Description	Default
7:0	CLK_MON_STAT	RO	Clock monitoring result using Protection 32MHz clock as reference. 0x80: Freq(Prot32KHz) < 32KHz - %High limit setting 0x40: Freq(Prot32KHz) > 32KHz + % High limit setting 0x20: Freq(Prot32KHz) < 32KHz - %Low limit setting 0x10: Freq(Prot32KHz) > 32KHz + %Low limit setting 0x08: Freq(Regu32KHz) < 32KHz - %High limit setting 0x04: Freq(Regu32KHz) > 32KHz + % High limit setting 0x02: Freq(Regu32KHz) < 32KHz - %Low limit setting 0x01: Freq(Regu32KHz) > 32KHz + %Low limit setting (*Note:* High/Low limit setting configured in CLK_MON_CTRL[7] = 0: High = 25% Low = 12.5%; =1: High = 50% Low = 25%)	0x00

7.3.19 0x012 - FUSA_STATUS_2A

Bit	Name	R/W	Description	Default
7:0	CLK_MON_STAT_A	RO	Clock monitoring results using Regulation 32MHz clock as reference 0x80: Freq(Prot32KHz) < 32KHz - %High limit setting 0x40: Freq(Prot32KHz) > 32KHz + % High limit setting 0x20: Freq(Prot32KHz) < 32KHz - %Low limit setting 0x10: Freq(Prot32KHz) > 32KHz + %Low limit setting 0x08: Freq(Regu32KHz) < 32KHz - %High limit setting 0x04: Freq(Regu32KHz) > 32KHz + % High limit setting 0x02: Freq(Regu32KHz) < 32KHz - %Low limit setting 0x01: Freq(Regu32KHz) > 32KHz + %Low limit setting (*Note:* High/Low limit setting configured in CLK_MON_CTRL[7] = 0: High = 25% Low = 12.5%; =1: High = 50% Low = 25%)	0x00

7.3.20 0x013 - FUSA_STATUS_3

Bit	Name	R/W	Description	Default
7:2	CLKMON_STAT2	RO	[5]: Protection digital HF clock is switched to Regulation 32MHz clock [4]: Protection digital LF clock is switched to Regulation 32KHz clock [3]: Prot clk32M stuck [2]: -- [1]: Regu clk32M stuck [0]: --	0x00
1	PMIC_POST_PASSED	RO	0x0: At least one Self Diagnosis test has failed. 0x1: All Self Diagnosis tests have passed	0x0
0	MTE_MODE_STATUS	RO	0x1: PMIC is in DEBUG mode (MTE mode). 0x0: PMIC is in normal mode.	0x0

7.3.21 0x014 - FUSA_STATUS_4

Bit	Name	R/W	Description	Default
7:0	SafetyCtrl_ErrCnt	RO	Safe state (RESET or ERROR FuSa states) visit counter [7:4]: RESET state visit counter (Also knows as SoC Error Counter) [3:0]: ERROR state visit counter (Also known as PMIC Error Counter)	0x00

7.3.22 0x015 - FUSA_SOC_CHK_1

Bit	Name	R/W	Description	Default
7:0	SINT_CHK_COPY	RO	PMIC copies the data written to FUSA_CTRL_2 register here. SoC is expected to read this register value and write it back to FUSA_CTRL_3 register to complete SINT. (*Note:* Refer to the *Safety Application Note* for SINT details)	0x00

7.3.23 0x016 - IO_HOST_MSGCNT

Bit	Name	R/W	Description	Default
7:0	HOST_MSGCNT	RO	Count value for the valid write operation from HOST.	0x00

7.3.24 0x017 - CLK_CNT_1

Bit	Name	R/W	Description	Default
7:0	FREERUN_CNT_UPPER	RO	Upper byte of free running 16bit counter (Reference clock is Protection 32MHz clock)	0x00

7.3.25 0x018 - CLK_CNT_2

Bit	Name	R/W	Description	Default
7:0	FREERUN_CNT_LOWER	RO	Lower byte of free running 16-bit counter (Reference clock is Protection 32MHz clock), (*Note:* It resets to 0 when this register is tried to be written with any value.)	0x00

7.3.26 0x019 - FLT_RECORD_A

Bit	Name	R/W	Description	Default
7	FLT_Presetout	RO	PRESETOUT fault record. 0x0: passed or not started 0x1: test failed (Is set in SOC Activation if ext pin check 1 fails or PRESET# - PRESETOUT loop back check fails in RESET state)	0x0
6	FLT_SintCheck	RO	Serial Interface Test (SINT) fault record 0x0: passed or not started 0x1: test failed	0x0
5	FLT_ExtPinCheck2	RO	External pin check 2 (SDI1, SDI2, SDI3, SDI4, PRESETOUT pin used) test fault record 0x0: passed or not started 0x1: test failed	0x0
4	FLT_GC_SelfT_fault	RO	GC Self Test Fault Record 0x0: No fault detected 0x1: Fault detected	0x0
3	FLT_SDI_3	RO	SDI_4 pin fault (Active FuSa state) record 0x0: No fault detected 0x1: fault detected	0x0
2	FLT_SDI_2	RO	SDI_3 pin fault (Active FuSa state) record 0x0: No fault detected 0x1: fault detected	0x0
1	FLT_SDI_1	RO	SDI_2 pin fault (Active FuSa state) record 0x0: No fault detected 0x1: fault detected	0x0
0	FLT_SDI_0	RO	SDI_1 pin fault (Active FuSa state) record 0x0: No fault detected 0x1: fault detected	0x0

7.3.27 0x01A - FLT_RECORD_B

Bit	Name	R/W	Description	Default
7	FLT_PmicErrExceed	RO	Maximum PMIC error counter fault record 0x0: No fault detected. PMIC error counter does not reach maximum value 0x1: fault detected due to PMIC error counter reached maximum value	0x0
6	FLT_SocErrExceed	RO	Maximum SOC error counter fault record 0x0: No fault detected. SOC error counter does not reach maximum value 0x1: fault detected due to SOC error counter reached maximum value	0x0
5	FLT_WDT	RO	WDT fault record 0x0: No fault detected for the WDT operation 0x1: fault detected for WDT operation	0x0
4	FLT_RegCRC	RO	Fault record for communication interface (I^2C or SPI for protection and regulation) CRC fault 0x0: No CRC error detected 0x1: CRC error detected	0x0
3	FLT_ClkMon	RO	Clock monitoring fault record (drift and stuck at faults) 0x0: No fault detected for the clock monitoring 0x1: Clock monitoring fault detected	0x0
2	FLT_ReguOT	RO	Fault record for Regulation faults (such as OV, UV, HSWOC, LSWUC …, OT, VABAT OV) 0x0: No fault 0x1: At least one of the Regulation faults detected.	0x0
1	FLT_FaultDetectBist	RO	Monitoring system's Fault module BIST (Fault Detect BIST) test result record 0x0: BIST passed 0x1: BIST failed	0x0
0	FLT_LBIST	RO	LBIST test result record. 0x0: LBIST passed 0x1: LBIST failed	0x0

7.3.28 0x01B - FLT_RECORD_GND_AVIN

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3	FaultStatus_AVIN2_Prot	RO	AVIN2(Protection power supply) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
2	FaultStatus_AVIN1_Regu	RO	AVIN1(Regulation power supply) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
1	FaultStatus_PGND_Regu	RO	PGND (Regulation) channel fault record 0x0: ADC monitoring within range 0x1: ADC monitoring out of range	0x0
0	FaultStatus_Offset	RO	Offset channel fault record 0x0: ADC monitoring within range 0x1: ADC monitoring out of range	0x0

7.3.29 0x01C - FLT_RECORD_BG_Temp

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	FaultStatus_SPARE_1	RO	SPARE_1 channel fault record 0x0: ADC monitoring within range 0x1: ADC monitoring out of range	0x0
5	FaultStatus_Temp_ExtreemLow	RO	Temp2 (Protection Temperature sensor) channel extreme Low temperature fault record 0x0: Temperature is above limit 0x1: Temperature is below limit	0x0
4	FaultStatus_TEMP2_SENSOR	RO	Protection OT BIST channel fault record 0x0: Val(Ref. TEMP Sensor) = Val(Temp Sensor) 0x1: Val(Ref. TEMP Sensor) ≠ Val(Temp Sensor)	0x0
3	FaultStatus_TempShdn	RO	Temp2 (Protection Temperature sensor) severity status 0x0: Temperature is below critical shutdown temperature limit 0x1: Temperature is above critical shutdown temperature limit	0x0
2	FaultStatus_TempWarn	RO	Temp2 (Protection Temperature sensor) warning status 0x0: Temperature is below warning temperature limit 0x1: Temperature is above warning temperature limit	0x0
1	FaultStatus_Temp4_Shdn_Regu	RO	Temp4 (Regulation Temperature sensor) severity status 0x0: Temperature is below critical shutdown temperature limit 0x1: Temperature is above critical shutdown temperature limit	0x0
0	FaultStatus_BG_REGU	RO	Bandgap (Regulation) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0

7.3.30 0x01D - FLT_RECORD_IntLDOs

Bit	Name	R/W	Description	Default
7	FaultStatus_IntLDOProt_1	RO	Internal LDO1 Prot (Protection Internal LDO) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
6	FaultStatus_IntLDOProt_0	RO	Internal LDO0 Prot (Protection Internal LDO) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
5	FaultStatus_IntLDORegu_5	RO	Internal LDO5 Regu (Regulation Internal LDO) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
4	FaultStatus_IntLDORegu_4	RO	Internal LDO4 Regu (Regulation Internal LDO) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
3	FaultStatus_IntLDORegu_3	RO	Internal LDO3 Regu (Regulation Internal LDO) channel fault record 0x0: ADC monitoring within range 0x1: ADC monitoring out of range	0x0
2	FaultStatus_IntLDORegu_2	RO	Internal LDO2 Regu (Regulation Internal LDO) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
1	FaultStatus_IntLDORegu_1	RO	Internal LDO1 Regu (Regulation Internal LDO) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
0	FaultStatus_IntLDORegu_0	RO	Internal LDO0 Regu (Regulation Internal LDO) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0

7.3.31 0x01E - FLT_RECORD_ExtLDOs

Bit	Name	R/W	Description	Default
7	FaultStatus_SPARE0	RO	SPARE0 (ADC5 - ADC4) Channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
6	Reserved	RO	Reserved	0x0
5	FaultStatus_ExtLDORegu_5	RO	External LDO6 channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
4	FaultStatus_ExtLDORegu_4	RO	External LDO5 channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
3	FaultStatus_ExtLDORegu_3	RO	External LDO4 channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
2	FaultStatus_ExtLDORegu_2	RO	External LDO3 channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
1	FaultStatus_ExtLDORegu_1	RO	External LDO2 channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
0	FaultStatus_ExtLDORegu_0	RO	External LDO1 channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0

7.3.32 0x01F - FLT_RECORD_BUCKS_B

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0x00
1	FaultStatus_Buck_1_VOUT	RO	VOUT1 (Remote voltage sense pin of Buck1) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
0	FaultStatus_Buck_1_PVIN	RO	PVIN1 (power stage supply pin of 15A Buck1) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0

7.3.33 0x020 - FLT_RECORD_BUCKS_A

Bit	Name	R/W	Description	Default
7	FaultStatus_Buck_5_VOUT	RO	VOUT5 (Remote voltage sense pin of 1A Buck5) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
6	FaultStatus_Buck_5_PVIN	RO	PVIN5 (power stage supply pin of 1A Buck5) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
5	FaultStatus_Buck_4_VOUT	RO	VOUT4 (Remote voltage sense pin of 1A Buck4) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
4	FaultStatus_Buck_4_PVIN	RO	PVIN4 (power stage supply pin of 1A Buck4) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
3	FaultStatus_Buck_3_VOUT	RO	VOUT3 (Remote voltage sense pin of 1A Buck3) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
2	FaultStatus_Buck_3_PVIN	RO	PVIN3 (power stage supply pin of 1A Buck3) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
1	FaultStatus_Buck_2_VOUT	RO	VOUT2 (Remote voltage sense pin of 1A Buck2) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
0	FaultStatus_Buck_2_PVIN	RO	PVIN2 (power stage supply pin of 1A Buck2) channel fault record 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0

7.3.34 0x021 - FLT_RECORD_ExtINPs_7_0

Bit	Name	R/W	Description	Default
7	FaultStatus_EXT_7_Prot	RO	EXT7 channel fault record (* valid when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
6	FaultStatus_EXT_6_Prot	RO	EXT6 channel fault record (* valid when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
5	FaultStatus_EXT_5_Prot	RO	EXT5 channel fault record (* valid when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
4	FaultStatus_EXT_4_Prot	RO	EXT4 channel fault record (* corresponds to ADC5 pin when ADCMON_EXT_CFG[0] = 0) (* corresponds to EXT4 input when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
3	FaultStatus_EXT_3_Prot	RO	EXT3 channel fault record (* corresponds to ADC4 pin when ADCMON_EXT_CFG[0] = 0) (* corresponds to EXT3 input when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
2	FaultStatus_EXT_2_Prot	RO	EXT2 channel fault record (* corresponds to ADC3 pin when ADCMON_EXT_CFG[0] = 0) (* corresponds to EXT2 input when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
1	FaultStatus_EXT_1_Prot	RO	EXT1 channel fault record (* corresponds to ADC2 pin when ADCMON_EXT_CFG[0] = 0) (* corresponds to EXT1 input when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0
0	FaultStatus_EXT_0_Prot	RO	EXT0 channel fault record (* corresponds to ADC1 pin when ADCMON_EXT_CFG[0] = 0) (* corresponds to EXT0 input when ADCMON_EXT_CFG[0] = 1) 0x0: ADC monitoring data within range 0x1: ADC monitoring data out of range	0x0

7.3.35 0x028 - OTP_RWADDR

Bit	Name	R/W	Description	Default
7	OTP_CRC_FAULT	RO	OTP download CRC fail 0x1: CRC fail on OTP download 0x0: CRC pass on OTP download	0x0
6:0	Reserved	RO	Reserved	0x0

7.3.36 0x02A - OTP_FLT_RECORD

Bit	Name	R/W	Description	Default
7	OTP_FLT_DLOAD_Timeout	RO	Fault record for "OTP down load time out" Fault. This bit is cleared on read. 0x0: No fault 0x1: Fault recorded	0x0
6	OTP_FLT_INIT_Fail	RO	Fault record for "OTP initial check" failure. This bit is cleared on read. 0x0: No fault 0x1: Fault recorded	0x0
5	OTP_FLT_CRC_FailPage0	RO	Fault record for "OTP CRC Page 0" failure. This bit is cleared on read. 0x0: No fault 0x1: Fault recorded *Note:* * When "Register Double Check during down load" Fault occurs then both bits- "OTP_FLT_CRC_FailPage0" and "OTP_FLT_CRC_FailPage2" are set.	0x0
4	OTP_FLT_CRC_FailPage2	RO	Fault record for "OTP CRC Page 2" failure. This bit is cleared on read. 0x0: No fault 0x1: Fault recorded *Note:* * When "Register Double Check during down load" Fault occurs then both bits – OTP_FLT_CRC_FailPage0 and OTP_FLT_CRC_FailPage2 are set.	0x0
3	OTP_FLT_PGM_NotPGMD	RO	Fault record for "OTP not programmed" fault. This bit is cleared on read. 0x0: No fault 0x1: Fault recorded	0x0
2	OTP_FLT_PGM_Warn	RO	Fault record for "OTP Program warning" (1 out of 4 bit failed). This bit is cleared on read. (*This is only valid while OTP is being programmed) 0x0: No fault 0x1: Fault recorded	0x0
1	OTP_FLT_PGM_WrongAddr	RO	Fault record for "OTP wrong program ADDR" failure. This bit is cleared on read. (*This is only valid while OTP is being programmed) 0x0: No fault 0x1: Fault recorded	0x0
0	OTP_FLT_PGM_Error	RO	Fault record for "OTP program failed". This bit is cleared on read. (*This is only valid while OTP is being programmed) 0x0: No fault 0x1: Fault recorded	0x0

7.3.37 0x02D - ADCMON_COPY_SAMPLE

Bit	Name	R/W	Description	Default
7	ADCMON_COPY_SAMPLE_ RDY	RO	ADC_DATA_READY goes low when ADC_DATACOPY is written and becomes high when ADC monitoring data is copied to ADC_DATA_[MSB,LSB] 0x0: Copied Sample Not Ready 0x1: Copied Sample Ready	0x0
6	ADCMON_COPY_EXTADC	RW	Copy sample request of ADC input source 0x0: Copy request for ADC monitoring channels (exclude EXT0 through EXT15) 0x1: Copy request for External channels of ADC monitoring (EXT 0 through EXT15)	0x0

Bit	Name	R/W	Description	Default
5:0	ADCMON_COPY_SAMPLE	RW	ADC_COPY_SAMPLE[4:0] Index when ADCMON_COPY_EXTADC[6] = 0 0x00: Offset channel 0x01: Temp2 channel 0x02: Protection OT BIST channel 0x03: BG Regu channel 0x04: PGND channel 0x05: Ext.LDO1 channel 0x06: Ext.LDO2 channel 0x07: Ext.LDO3 channel 0x08: Ext LDO4 channel 0x09: Ext LDO5 channel 0x0a: Ext LDO6 channel 0x0b: Int. LDO1 Prot channel 0x0c: Int. LDO0 Prot channel 0x0d: SPARE0 channel 0x0e: AVIN2 channel 0x10: AVIN1 channel 0x11: Int.LDO0 Regu channel 0x12: Int. LDO1 Regu channel 0x13: Int. LDO2 Regu channel 0x14: Int. LDO3 Regu channel 0x15: PVIN1 channel 0x16: VOUT1 channel 0x17: PVIN2 channel 0x18: VOUT2 channel 0x19: PVIN3 channel 0x1a: VOUT3 channel 0x1b: PVIN4 channel 0x1c: VOUT4 channel 0x1d: PVIN5 channel 0x1e: VOUT5 channel 0x20: Int. LDO4 Regu channel 0x21: Int. LDO5 Regu channel 0x22: Temp4 (Regulation temp sensor) channel 0x23: SPARE_1 channel ADC_COPY_SAMPLE[4:0] Index when ADCMON_COPY_EXTADC[6] = 1 0x00: EXT0 channel 0x01: EXT1 channel 0x02: EXT2 channel 0x03: EXT3 channel 0x04: EXT4 channel 0x05: EXT5 channel 0x06: EXT6 channel 0x07: EXT7 channel 0x08: EXT8 channel 0x09: EXT9 channel 0x0a: EXT10 channel 0x0b: EXT11 channel 0x0c: EXT12 channel 0x0d: EXT13 channel 0x0e: EXT14 channel 0x0f: EXT15 channel *Note:* When ADC_DATACOPY is written, the sample data from the channel that was selected by ADC_COPY_SAMPLE is copied to ADC_DATA	0x00

7.3.38 0x02E - ADCMON_COPY_DATA_MSB

Bit	Name	R/W	Description	Default
7:0	ADCMON_COPY_DATA_MSB	RO	Upper Byte of ADC_DATA	0x00

7.3.39 0x02F - ADCMON_COPY_DATA_LSB

Bit	Name	R/W	Description	Default
7:0	ADCMON_COPY_DATA_LSB	RO	Lower Byte of ADC_DATA	0x00

7.3.40 0x030 - ADCMON_DATAMSB_Offset

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_Offset	RO	Upper byte of 16 bits ADC result for offset measurement	0x00

7.3.41 0x031 - ADCMON_DATALSB_Offset

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_Offset	RO	Lower byte of 16 bits ADC result for offset measurement	0x00

7.3.42 0x032 - ADCMON_DATAMSB_Temp2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_Temp2	RO	Upper byte of 16 bits ADC result for temperature sensor TEMP2 (protection) measurement	0x00

7.3.43 0x033 - ADCMON_DATALSB_Temp2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_Temp2	RO	Lower byte of 16 bits ADC result for temperature sensor TEMP2 (protection) measurement	0x00

7.3.44 0x034 - ADCMON_DATAMSB_Temp3

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_Temp3	RO	Upper byte of 16 bits ADC result for Protection OT BIST measurement	0x00

7.3.45 0x035 - ADCMON_DATALSB_Temp3

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_Temp3	RO	Lower byte of 16 bits ADC result for Protection OT BIST measurement	0x00

7.3.46 0x036 - ADCMON_DATAMSB_BGRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_BGRegu	RO	Upper byte of 16 bits ADC result for Bandgap (Regulation) measurement	0x00

7.3.47 0x037 - ADCMON_DATALSB_BGRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_BGRegu	RO	Lower byte of 16 bits ADC result for Bandgap (Regulation) measurement	0x00

7.3.48 0x038 - ADCMON_DATAMSB_PGNDRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ PGNDRegu	RO	Upper byte of 16 bits ADC result for PGND (Regulation) measurement	0x00

7.3.49 0x039 - ADCMON_DATALSB_PGNDRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ PGNDRegu	RO	Lower byte of 16 bits ADC result for PGND (Regulation) measurement	0x00

7.3.50 0x03A - IntLDORegu_0_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDORegu	RO	Upper byte of 16 bits ADC result for Internal LDO0(Regulation) measurement.	0x00

7.3.51 0x03B - IntLDORegu_0_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDORegu	RO	Lower byte of 16 bits ADC result for Internal LDO0 (Regulation) measurement.	0x00

7.3.52 0x03C - IntLDORegu_1_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDORegu	RO	Upper byte of 16 bits ADC result for Internal LDO1(Regulation) measurement.	0x00

7.3.53 0x03D - IntLDORegu_1_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDORegu	RO	Lower byte of 16 bits ADC result for Internal LDO1 (Regulation) measurement.	0x00

7.3.54 0x03E - IntLDORegu_2_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDORegu	RO	Upper byte of 16 bits ADC result for Internal LDO2 (Regulation) measurement.	0x00

7.3.55 0x03F - IntLDORegu_2_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDORegu	RO	Lower byte of 16 bits ADC result for Internal LDO2 (Regulation) measurement.	0x00

7.3.56 0x040 - IntLDORegu_3_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDORegu	RO	Upper byte of 16 bits ADC result for Internal LDO3(Regulation) measurement.	0x00

7.3.57 0x041 - IntLDORegu_3_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDORegu	RO	Lower byte of 16 bits ADC result for Internal LDO3 (Regulation) measurement.	0x00

7.3.58 0x042 - IntLDORegu_4_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDORegu	RO	Upper byte of 16 bits ADC result for Internal LDO4 (Regulation) measurement.	0x00

7.3.59 0x043 - IntLDORegu_4_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDORegu	RO	Lower byte of 16 bits ADC result for Internal LDO4 (Regulation) measurement.	0x00

7.3.60 0x044 - IntLDORegu_5_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDORegu	RO	Upper byte of 16 bits ADC result for Internal LDO5 (Regulation) measurement.	0x00

7.3.61 0x045 - IntLDORegu_5_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDORegu	RO	Lower byte of 16 bits ADC result for Internal LDO5 (Regulation) measurement.	0x00

7.3.62 0x046 - IntLDOProt_0_ADCMON_DATAMSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDOProt	RO	Upper byte of 16 bits ADC result for Internal LDO0 (Protection) measurement.	0x00

7.3.63 0x047 - IntLDOProt_0_ADCMON_DATALSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDOProt	RO	Lower byte of 16 bits ADC result for Internal LDO0 (Protection) measurement.	0x00

7.3.64 0x048 - IntLDOProt_1_ADCMON_DATAMSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ IntLDOProt	RO	Upper byte of 16 bits ADC result for Internal LDO1 (Protection) measurement.	0x00

7.3.65 0x049 - IntLDOProt_1_ADCMON_DATALSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ IntLDOProt	RO	Lower byte of 16 bits ADC result for Internal LDO1 (Protection) measurement.	0x00

7.3.66 0x04A - ADCMON_DATAMSB_AVIN1

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_AVIN1	RO	Upper byte of 16 bits ADC result for AVIN1 power supply (Regulation) measurement.	0x00

7.3.67 0x04B - ADCMON_DATALSB_AVIN1

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_AVIN1	RO	Lower byte of 16 bits ADC result for AVIN1 power supply (Regulation) measurement.	0x00

7.3.68 0x04C - ADCMON_DATAMSB_AVIN2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_AVIN2	RO	Upper byte of 16 bits ADC result for AVIN2 power supply (Protection) measurement.	0x00

7.3.69 0x04D - ADCMON_DATALSB_AVIN2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_AVIN2	RO	Lower byte of 16 bits ADC result for AVIN2 power supply (Protection) measurement.	0x00

7.3.70 0x04E - extLDO_0_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16 bits ADC result for Ext. LDO1 (Regulation) measurement.	0x00

7.3.71 0x04F - extLDO_0_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16 bits ADC result for Ext. LDO1 (Regulation) measurement.	0x00

7.3.72 0x050 - extLDO_1_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16 bits ADC result for Ext. LDO2 (Regulation) measurement.	0x00

7.3.73 0x051 - extLDO_1_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16 bits ADC result for Ext. LDO2 (Regulation) measurement.	0x00

7.3.74 0x052 - extLDO_2_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16 bits ADC result for Ext. LDO3 (Regulation) measurement.	0x00

7.3.75 0x053 - extLDO_2_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16 bits ADC result for Ext. LDO3 (Regulation) measurement.	0x00

7.3.76 0x054 - extLDO_3_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16 bits ADC result for Ext. LDO4 (Regulation) measurement.	0x00

7.3.77 0x055 - extLDO_3_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16 bits ADC result for Ext. LDO4 (Regulation) measurement.	0x00

7.3.78 0x056 - extLDO_4_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16 bits ADC result for Ext. LDO5 (Regulation) measurement.	0x00

7.3.79 0x057 - extLDO_4_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16 bits ADC result for Ext. LDO5 (Regulation) measurement.	0x00

7.3.80 0x058 - extLDO_5_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16 bits ADC result for Ext. LDO6 (Regulation) measurement.	0x00

7.3.81 0x059 - extLDO_5_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16 bits ADC result for Ext. LDO6 (Regulation) measurement.	0x00

7.3.82 0x05A - PVIN_0_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16 bits ADC result for PVIN1 (Regulation) measurement.	0x00

7.3.83 0x05B - PVIN_0_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16 bits ADC result for PVIN1 (Regulation) measurement.	0x00

7.3.84 0x05C - PVIN_1_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16 bits ADC result for PVIN2 (Regulation) measurement.	0x00

7.3.85 0x05D - PVIN_1_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16 bits ADC result for PVIN2 (Regulation) measurement.	0x00

7.3.86 0x05E - PVIN_2_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16 bits ADC result for PVIN3 (Regulation) measurement.	0x00

7.3.87 0x05F - PVIN_2_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16 bits ADC result for PVIN3 (Regulation) measurement.	0x00

7.3.88 0x060 - PVIN_3_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16 bits ADC result for PVIN4 (Regulation) measurement.	0x00

7.3.89 0x061 - PVIN_3_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16 bits ADC result for PVIN4 (Regulation) measurement.	0x00

7.3.90 0x062 - PVIN_4_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16 bits ADC result for PVIN5 (Regulation) measurement.	0x00

7.3.91 0x063 - PVIN_4_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16 bits ADC result for PVIN5 (Regulation) measurement.	0x00

7.3.92 0x064 - VOUT_0_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16 bits ADC result for VOUT1 (Regulation) measurement.	0x00

7.3.93 0x065 - VOUT_0_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16 bits ADC result for VOUT1 (Regulation) measurement.	0x00

7.3.94 0x066 - VOUT_1_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16 bits ADC result for VOUT2 (Regulation) measurement.	0x00

7.3.95 0x067 - VOUT_1_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16 bits ADC result for VOUT2 (Regulation) measurement.	0x00

7.3.96 0x068 - VOUT_2_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16 bits ADC result for VOUT3 (Regulation) measurement.	0x00

7.3.97 0x069 - VOUT_2_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16 bits ADC result for VOUT3 (Regulation) measurement.	0x00

7.3.98 0x06A - VOUT_3_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16 bits ADC result for VOUT4 (Regulation) measurement.	0x00

7.3.99 0x06B - VOUT_3_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16 bits ADC result for VOUT4 (Regulation) measurement.	0x00

7.3.100 0x06C - VOUT_4_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16 bits ADC result for VOUT5 (Regulation) measurement.	0x00

7.3.101 0x06D - VOUT_4_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16 bits ADC result for VOUT5 (Regulation) measurement.	0x00

7.3.102 0x06E - ADCMON_DATAMSB_SPARE_0

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ SPARE_0	RO	Upper byte of 16 bits ADC result for Spare_0 (Regulation) measurement.	0x00

7.3.103 0x06F - ADCMON_DATALSB_SPARE_0

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ SPARE_0	RO	Lower byte of 16 bits ADC result for Spare_0 (Regulation) measurement.	0x00

7.3.104 0x070 - ADCMON_DATAMSB_Temp4

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_Temp4	RO	Upper byte of 16 bits ADC result for temperature sensor TEMP4 (Regulation) measurement	0x00

7.3.105 0x071 - ADCMON_DATALSB_Temp4

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_Temp4	RO	Lower byte of 16 bits ADC result for temperature sensor TEMP4 (Regulation) measurement	0x00

7.3.106 0x072 - ADCMON_DATAMSB_SPARE_1

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ SPARE_1	RO	Upper byte of 16 bits ADC result for GND () measurement	0x00

7.3.107 0x073 - ADCMON_DATALSB_SPARE_1

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ SPARE_1	RO	Lower byte of 16 bits ADC result for GND () measurement	0x00

7.3.108 0x074 - EXT_0_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for EXT0 channel measurement. (* ADC1 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.109 0x075 - EXT_0_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for EXT0 channel measurement. (* ADC1 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.110 0x076 - EXT_1_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for EXT1 channel measurement. (* ADC2 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.111 0x077 - EXT_1_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for EXT1 channel measurement. (* ADC2 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.112 0x078 - EXT_2_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for EXT2 channel measurement. (* ADC3 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.113 0x079 - EXT_2_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for EXT2 channel measurement. (* ADC3 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.114 0x07A - EXT_3_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for EXT3 channel measurement. (* ADC4 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.115 0x07B - EXT_3_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for EXT3 channel measurement. (* ADC4 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.116 0x07C - EXT_4_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for EXT4 channel measurement. (* ADC5 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.117 0x07D - EXT_4_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for EXT4 channel measurement. (* ADC5 pin when ADCMON_EXT_CFG[0] = 0)	0x00

7.3.118 0x07E - EXT_5_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT5 channel measurement.	0x00

7.3.119 0x07F - EXT_5_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT5 channel measurement.	0x00

7.3.120 0x080 - EXT_6_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT6 channel measurement.	0x00

7.3.121 0x081 - EXT_6_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT6 channel measurement.	0x00

7.3.122 0x082 - EXT_7_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT7 channel measurement.	0x00

7.3.123 0x083 - EXT_7_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT7 channel measurement.	0x00

7.3.124 0x084 - EXT_8_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT8 channel measurement.	0x00

7.3.125 0x085 - EXT_8_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT8 channel measurement.	0x00

7.3.126 0x086 - EXT_9_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT9 channel measurement.	0x00

7.3.127 0x087 - EXT_9_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT9 channel measurement.	0x00

7.3.128 0x088 - EXT_10_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT10 channel measurement.	0x00

7.3.129 0x089 - EXT_10_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT10 channel measurement.	0x00

7.3.130 0x08A - EXT_11_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT11 channel measurement.	0x00

7.3.131 0x08B - EXT_11_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT11 channel measurement.	0x00

7.3.132 0x08C - EXT_12_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT12 channel measurement.	0x00

7.3.133 0x08D - EXT_12_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT12 channel measurement.	0x00

7.3.134 0x08E - EXT_13_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT13 channel measurement.	0x00

7.3.135 0x08F - EXT_13_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT13 channel measurement.	0x00

7.3.136 0x090 - EXT_14_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT14 channel measurement.	0x00

7.3.137 0x091 - EXT_14_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT14 channel measurement.	0x00

7.3.138 0x092 - EXT_15_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16 bits ADC result for External EXT15 channel measurement.	0x00

7.3.139 0x093 - EXT_15_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16 bits ADC result for External EXT15 channel measurement.	0x00

7.3.140 0x094 - MTE_CFG_CTRL_A

Bit	Name	R/W	Description	Default
7:1	Reserved	-	Reserved	0x00
0	MTE_BURN	RW	Burn debug(MTE) fuse 0x0: -- 0x1: One time command for burning the fuse (*Note:* Refer to the *Safety Application Note* for details of fuse burning operation)	0x0

7.3.141 0x095 - WDT_KICK_REG

Bit	Name	R/W	Description	Default
7:0	WDT_KICK_REG	RW	WDT Kick data register (* to be written by user with correct answer)	0x00

7.3.142 0x096 - WDT_LFSR

Bit	Name	R/W	Description	Default
7:0	WDT_LFSR	RO	Question register for Advance mode WDT Read back this register to get question sent by part.	0x00

7.3.143 0x09B - I_LOCK_OUT_CFG (OTP)

Bit	Name	R/W	Description	Default
7:0	I_LOCK_OUT	RW	Bit when set would lock registers of category mentioned [0]: Password access [1]: FUSA general setup [2]: Soft reset control [3]: Vmon thresholds, threshold delays, ADC setup [4]: Watchdog Settings [5]: I/O setup [6]: FLT masking for Vmon [7]: SoC Activation	0x00

7.3.144 0x102 - IO_MODECTRL (OTP)

Bit	Name	R/W	Description	Default
7	MTE_TM	RW	0x0: MTE Test mode disable 0x1: MTE Test mode enable	0x0
6	MTE_DIS	RW	0x0: Debug(MTE) mode. FuSa fault reactions are disabled while faults are recorded. 0x1: Normal mode	0x0
5:4	Reserved	RO	Reserved	0x2
3	INTERRUPT_MASKING_OPT	RW	Interrupt Pin Masking Option 0x0: All faults (both masked and unmasked) propagate to IRQ# pin 0x1: Only unmasked faults propagate to IRQ# pin.	0x0
2:1	Reserved	RO	Reserved	0x2
0	IO_REGVALID	RO	Status of OTP download to shadow register and CRC check 0x0: OTP not programmed or OTP download failed CRC check. All Registers set to POR values. 0x1: OTP download is successful and passed CRC check Registers set to OTP values.	0x0

7.3.145 0x103 - IO_I2CADDR (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:0	IO_I2CADDR	RW	I^2C Auxiliary ID Address[6:0]	0x1D

7.3.146 0x104 - IO_I2C_SPICFG (OTP)

Bit	Name	R/W	Description	Default
7	IO_I2C_SPEED	RW	I^2C speed control 0x0: Low speed glitch and slew filters by default 0x1: Glitch and slew filters set for high speed 3.4MHz mode	0x0
6	IO_SDA_SLEWFLTR	RW	Transmit slew rate control for I^2C SDA 0x0: Disable slew filtering 0x1: Enable slew filtering	0x0
5	IO_SPIPWPOL	RW	R/W polarity 0x0: 1 - Read, 0 - Write 0x1: 1 - Write, 0 - Read	0x0
4	IO_IRQ_CMOS	RW	(* … Not Used …)	0x1
3	IO_IRQ_INVERT	RW	(* … Not Used …)	0x1
2	IO_SPICPOL	RW	SPI clock polarity 0x0: Active high 0x1: Active low	0x0
1	IO_SPICPHA	RW	SPI clock phase 0x0: Sample on leading (first) clock edge 0x1: Sample on trailing (second) clock edge	0x0
0	IO_SPIMODE	RW	SPI mode selection 0x0: Byte mode 0x1: Byte mode with packet length field	0x1

7.3.147 0x105 - IO_FUNC_CFG (OTP)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3	SINT_NOSTART_BYPASS	RW	0x0: Fault reaction and fault reporting happens when SINT test is NOT started 0x1: No fault reaction and fault reporting when SINT test is NOT started. (*Note:* Setting 1 does not prevent fault reaction and fault reporting in case FUSA_CTRL_2 (SINT start register) register is written and fault occurs)	0x0
2:1	Reserved	RO	Reserved	0x0
0	REGCRC_EN	RW	I^2C/SPI Communication CRC Mode selection 0x0: Communication DOES NOT include CRC check. 0x1: Communication includes CRC check	0x0

7.3.148 0x107 - WDT_CFG0 (OTP)

Bit	Name	R/W	Description	Default
7	WDT_DIS_LFSR	RW	0x0: Question value is generated by Pseudo random 0x1:Question value generated by Sequentail order	0x0
6:5	WDT_RSVD_CFG	RW	Reserved field	0x0
4:3	WDT_KICK_SEL	RW	WDT kick input selection 0x0: Communication Interface (I^2C or SPI) 0x1: Not used 0x2: Not used 0x3: Not used	0x0
2	WDT_WWDT_ADV_MODE	RW	WDT mode selection 0x0: Basic WDT 0x1: Advancd mode (Q & A) WDT	0x1
1	WDT_WWDT_ADV_16Q	RW	Advance mode Q&A scheme 0x0: 4 Q&A scheme mode 0x1: 16 Q&A scheme mode	0x1
0	WDT_WWDT_EN	RW	WDT Enable 0x0: Disable WDT 0x1: Enable WDT	0x1

7.3.149 0x108 - WDT_CFG1 (OTP)

Bit	Name	R/W	Description	Default
7:4	WDT_ULCNT	RW	Upper limit counter value: Value*WDT_ULTICK	0x0
3:0	WDT_LLCNT	RW	Lower limit counter value: Value*WDT_LLTICK	0x0

7.3.150 0x109 - WDT_CFG2 (OTP)

Bit	Name	R/W	Description	Default
7:6	WDT_WWDT_ACC_TH	RW	Advance mode accumulated Fault threshold 0x0: 1 0x1: 15 0x2: 31 0x3: 63	0x3
5:3	WDT_ULTICK	RW	Upper limit tick unit: 0x0: 0s (invalid) 0x1: 10µs 0x2: 100µs 0x3: 1ms 0x4: 10ms 0x5: 100ms 0x6: 1s 0x7: 0s (invalid)	0x0
2:0	WDT_LLTICK	RW	Lower limit tick unit: 0x0: 0s (invalid) 0x1: 10µs 0x2: 100µs 0x3: 1ms 0x4: 10ms 0x5: 100ms 0x6: 1s 0x7: 0s (invalid)	0x0

7.3.151 0x10A - WDT_CFG3

Bit	Name	R/W	Description	Default
7:0	WDT_WWDT_ACC	RO	Current value of wrong answer score accumulation: 0 ~ 255	0x00

7.3.152 0x10B - WDT_CFG4 (OTP)

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	-

7.3.153 0x10C - FUSA_CTRL_1 (OTP)

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	0x08
2	STIL_MODE_EN	RW	Enable STIL mode within SOC Activation (SOC ACT.) State 0x0: NO STIL state allowed within SOC ACT.state 0x1: STIL state allowed within SOC ACT. state (*Note:* Refer to the *Safety Application Note* for STIL MODE)	0x0
1:0	Reserved	RO	Reserved	0x0

7.3.154 0x10D - FUSA_CHK_CVM2H (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH1 (continued)	RW	High threshold voltage setting of ADC1 and ADC 2 inputs, when voltage level configured as 2'b00 in their slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -1392 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH1 (continued)	RW	0x2A: 672 0xAA: -1376 0x2B: 688 0xAB: -1360 0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH1	RW	0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x08

7.3.155 0x10E - FUSA_CHK_CVM2L (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL1 (continued)	RW	Low threshold voltage setting of ADC1 and ADC 2 inputs, when voltage level configured as 2'b00 in their slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -1392 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL1 (continued)	RW	0x2A: 672 0xAA: -1376 0x2B: 688 0xAB: -1360 0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL1	RW	0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x01

7.3.156 0x10F - FUSA_CHK_CVM3H (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH2 (continued)	RW	High threshold voltage setting of ADC1 and ADC 2 inputs, when voltage level configured as 2'b01 in their slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -1392 0x2A: 672 0xAA: -1376 0x2B: 688 0xAB: -1360 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH2 (continued)	RW	0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH2	RW	0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x08

7.3.157 0x110 - FUSA_CHK_CVM3L (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL2 (continued)	RW	Low threshold voltage setting of ADC1 and ADC 2 inputs, when voltage level configured as 2'b01 in their slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -1392 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL2 (continued)	RW	0x2A: 672 0xAA: -1376 0x2B: 688 0xAB: -1360 0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL2	RW	0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x01

7.3.158 0x111 - FUSA_CHK_CVM4H (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH3 (continued)	RW	High threshold voltage setting of ADC1 input, when voltage level configured as 2'b10 in its slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -1392 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH3 (continued)	RW	0x2A: 672 0xAA: -1376 0x2B: 688 0xAB: -1360 0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH3	RW	0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x08

7.3.159 0x112 - FUSA_CHK_CVM4L (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL3 (continued)	RW	Low threshold voltage setting of ADC1 input, when voltage level configured as 2'b10 in its slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -139 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL3 (continued)	RW	0x2A: 672 0xAA: -1376 0x2B: 688 0xAB: -1360 0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL3	RW	0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x01

7.3.160 0x113 - FUSA_CHK_CVM5H (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH4 (continued)	RW	High threshold voltage setting of ADC2 input, when voltage level configured as 2'b10 in its slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -1392 0x2A: 672 0xAA: -1376 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH4 (continued)	RW	0x2B: 688 0xAB: -1360 0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 (continued)	0x08

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THH4	RW	0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x08

7.3.161 0x114 - FUSA_CHK_CVM5L (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL4 (continued)	RW	Low threshold voltage setting of ADC2 input, when voltage level configured as 2'b10 in its slot configuration register. (*1LSB = 16mV, format: 2's compliment) 0x0: 0 0x80: -2048 0x1: 16 0x81: -2032 0x2: 32 0x82: -2016 0x3: 48 0x83: -2000 0x4: 64 0x84: -1984 0x5: 80 0x85: -1968 0x6: 96 0x86: -1952 0x7: 112 0x87: -1936 0x8: 128 0x88: -1920 0x9: 144 0x89: -1904 0xA: 160 0x8A: -1888 0xB: 176 0x8B: -1872 0xC: 192 0x8C: -1856 0xD: 208 0x8D: -1840 0xE: 224 0x8E: -1824 0xF: 240 0x8F: -1808 0x10: 256 0x90: -1792 0x11: 272 0x91: -1776 0x12: 288 0x92: -1760 0x13: 304 0x93: -1744 0x14: 320 0x94: -1728 0x15: 336 0x95: -1712 0x16: 352 0x96: -1696 0x17: 368 0x97: -1680 0x18: 384 0x98: -1664 0x19: 400 0x99: -1648 0x1A: 416 0x9A: -1632 0x1B: 432 0x9B: -1616 0x1C: 448 0x9C: -1600 0x1D: 464 0x9D: -1584 0x1E: 480 0x9E: -1568 0x1F: 496 0x9F: -1552 0x20: 512 0xA0: -1536 0x21: 528 0xA1: -1520 0x22: 544 0xA2: -1504 0x23: 560 0xA3: -1488 0x24: 576 0xA4: -1472 0x25: 592 0xA5: -1456 0x26: 608 0xA6: -1440 0x27: 624 0xA7: -1424 0x28: 640 0xA8: -1408 0x29: 656 0xA9: -1392 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL4 (continued)	RW	0x2A: 672 0xAA: -1376 0x2B: 688 0xAB: -1360 0x2C: 704 0xAC: -1344 0x2D: 720 0xAD: -1328 0x2E: 736 0xAE: -1312 0x2F: 752 0xAF: -1296 0x30: 768 0xB0: -1280 0x31: 784 0xB1: -1264 0x32: 800 0xB2: -1248 0x33: 816 0xB3: -1232 0x34: 832 0xB4: -1216 0x35: 848 0xB5: -1200 0x36: 864 0xB6: -1184 0x37; 880 0xB7: -1168 0x38: 896 0xB8: -1152 0x39: 912 0xB9: -1136 0x3A: 928 0xBA: -1120 0x3B: 944 0xBB: -1104 0x3C: 960 0xBC: -1088 0x3D: 976 0xBD: -1072 0x3E: 992 0xBE: -1056 0x3F: 1008 0xBF: -1040 0x40: 1024 0xC0: -1024 0x41: 1040 0xC1: -1008 0x42: 1056 0xC2: -992 0x43; 1072 0xC3: -976 0x44: 1088 0xC4: -960 0x45: 1104 0xC5: -944 0x46: 1120 0xC6: -928 0x47: 1136 0xC7: -912 0x48: 1152 0xC8: -896 0x49: 1168 0xC9: -880 0x4A: 1184 0xCA: -864 0x4B: 1200 0xCB: -848 0x4C: 1216 0xCC: -832 0x4D: 1232 0xCD: -816 0x4E: 1248 0xCE: -800 0x4F: 1264 0xCF: -784 0x50: 1280 0xD0: -768 0x51: 1296 0xD1: -752 0x52: 1312 0xD2: -736 0x53: 1328 0xD3: -720 0x54: 1344 0xD4: -704 0x55: 1360 0xD5: -688 0x56: 1376 0xD6: -672 0x57: 1392 0xD7: -656 0x58: 1408 0xD8: -640 0x59: 1424 0xD9: -624 (continued)	0x01

Bit	Name	R/W	Description	Default
7:0	CVM_TEST_THL4	RW	0x5A: 1440 0xDA: -608 0x5B: 1456 0xDB: -592 0x5C: 1472 0xDC: -576 0x5D: 1488 0xDD: -560 0x5E: 1504 0xDE: -544 0x5F: 1520 0xDF: -528 0x60: 1536 0xE0: -512 0x61: 1552 0xE1: -496 0x62: 1568 0xE2: -480 0x63: 1584 0xE3: -464 0x64: 1600 0xE4: -448 0x65: 1616 0xE5: -432 0x66: 1632 0xE6: -416 0x67: 1648 0xE7: -400 0x68: 1664 0xE8: -384 0x69: 1680 0xE9: -368 0x6A: 1696 0xEA: -352 0x6B: 1712 0xEB: -336 0x6C: 1728 0xEC: -320 0x6D: 1744 0xED: -304 0x6E: 1760 0xEE: -288 0x6F: 1776 0xEF: -272 0x70: 1792 0xF0: -256 0x71: 1808 0xF1: -240 0x72: 1824 0xF2: -224 0x73: 1840 0xF3: -208 0x74: 1856 0xF4: -192 0x75: 1872 0xF5: -176 0x76: 1888 0xF6: -160 0x77: 1904 0xF7: -144 0x78: 1920 0xF8: -128 0x79: 1936 0xF9: -112 0x7A: 1952 0xFA: -96 0x7B: 1968 0xFB: -80 0x7C: 1984 0xFC: -64 0x7D: 2000 0xFD: -48 0x7E: 2016 0xFE: -32 0x7F: 2032 0xFF: -16	0x01

7.3.162 0x115 - FUSA_CTRL_MTE (OTP)

Bit	Name	R/W	Description	Default
7:6	Reserved	-	Reserved	0x0
5:4	SDO_0_PIN_VAL_MTE	RW	SDO1 pin value for debug(MTE) mode 0x0: Logic level 0 0x1: Logic level 1 0x2: Logic level Hi-Z 0x3: Logic level Hi-Z	0x0
3:2	SDO_1_PIN_VAL_MTE	RW	SDO2 pin value for debug(MTE) mode 0x0: Logic level 0 0x1: Logic level 1 0x2: Logic level Hi-Z 0x3: Logic level Hi-Z	0x1
1:0	Reserved	RO	Reserved	0x1

7.3.163 0x116 - FUSA_TIMER_1 (OTP)

Bit	Name	R/W	Description	Default
7:6	TIMEOUT_SELFD_ST	RW	FuSa state Self Diagnosis time out setting 0x0: 1ms 0x1: 2ms 0x2: 4ms 0x3: 8ms	0x1
5:2	TIMEOUT_MIN_ERROR_ST	RW	FuSa state Error time out setting (*Error state time out must be chosen greater than maximum shutdown delays of all regulators including discharge detect time out if applicable. When FAULT_DNDLY= 0, error state time out must be chosen greater than discharge detect time out if applicable) 0x0: 10ms 0x1: 20ms 0x2: 40ms 0x3: 60ms 0x4: 80ms 0x5: 130ms 0x6: 260ms 0x7: 1.04s 0x8: 2.00s 0x9: 4.00s 0xA-0xF: 10ms	0x5
1:0	TIMEOUT_PRESETOUT	RW	PRESET# low to PRESETOUT becoming low time out setting (*applied in FuSa state RESET) 0x0: 128µs 0x1: 256µs 0x2: 384µs 0x3: 480µs	0x0

7.3.164 0x117 - FUSA_TIMER_2 (OTP)

Bit	Name	R/W	Description	Default
7:5	TIMEOUT_SOCACTIVA_ST	RW	FuSa state SOC Activation time out setting 0x0: 15.62ms 0x1: 31.25ms 0x2: 46.87ms 0x3: 62.50ms 0x4: 78.12ms 0x5: 93.75ms 0x6: 125ms 0x7: 250ms	0x0
4:3	TIMEOUT_STIL_MODE	RW	FuSa state STIL Mode time out setting (*This mode is valid with in SOC ACT. state) 0x0: 5ms 0x1: 10ms 0x2: 15ms 0x3: 20ms	0x0
2:0	SINT_TOUT	RW	Allowed duration for Serial Interface Test (SINT) to finish. Timer starts with SINT_CHK_START register write. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: 1056µs 0x4: 2ms 0x5: 4ms 0x6: 8ms 0x7: 16ms	0x0

7.3.165 0x118 - FUSA_TIMER_3 (OTP)

Bit	Name	R/W	Description	Default
7:6	TIMEOUT_PRESET_CHK_TOUT	RW	Pin check 1 time out setting (*Valid in FuSa state SocActivation) 0x0: 8ms 0x1: 16ms 0x2: 24ms 0x3: 32ms	0x0
5:3	TIMEOUT_STIL_DLY_TIME	RW	Delay time from start of SOC ACTIVATION state to STIL mode entry. 0x0: 8ms 0x1: 16ms 0x2: 24ms 0x3: 32ms 0x4: 40ms 0x5: 48ms 0x6: 56ms 0x7: 64ms	0x0
2:0	TIMEOUT_PRESETOUT_DLY_TIME	RW	Delay before FuSa state machine moves from RESET to SOC ACTIVATION state following successful PRESET#/PRESETOUT check 0x0: 0ms 0x1: 8ms 0x2: 16ms 0x3: 24ms 0x4: 32ms 0x5: 40ms 0x6: 48ms 0x7: 56ms	0x0

7.3.166 0x119 - FUSA_TIMER_4 (OTP)

Bit	Name	R/W	Description	Default
7:4	TIMEOUT_PUSEQ_ST	RW	FuSa state "Power-Up" time out setting (*Power-Up state time out must be chosen greater than maximum start up delays of all regulators) 0x0: 4ms 0x1: 8ms 0x2: 12ms 0x3: 16ms 0x4: 20ms 0x5: 24ms 0x6: 28ms 0x7: 32ms 0x8: 36ms 0x9: 40ms 0xA: 44ms 0xB: 48ms 0xC: 52ms 0xD: 56ms 0xE: 60ms 0xF: 64ms	0x0
3:2	PGOOD_DLY	RW	Delay between internal PGOOD signal and start of regulator voltage monitoring by protection block. (*valid only if FUSA_CTRL_D:PgoodDlyTimerDone_DIS = 0) 0x0: 250µs 0x1: 500µs 0x2: 750 µs 0x3: 1000µs	0x0
1:0	PRESETb_DLY	RW	Delay between start of regulator voltage monitoring to PRESET# pin release. 0x0: 250µs 0x1: 500µs 0x2: 750µs 0x3: 1000µs	0x0

7.3.167 0x11A - FUSA_CTRL_A (OTP)

Bit	Name	R/W	Description	Default
7:5	CLK_MON_CTRL	RW	[2]: clk mon threshold 0x0: clock monitoring threshold narrow: freq diff: 12.5% < (warning region) < 25%, beyond 25% is fail. 0x1: clock monitoring threshold wide: freq diff: 25.0% < (warning region) < 50%, beyond 50% is fail. [1]: enable for clock frequency skew monitoring based on Prot 32MHz clock 0x0: disable 0x1: enable [0]: enable for clock frequency skew monitoring based on Regu 32MHz clock 0x0: disable 0x1: enable	0x7
4:3	Reserved	-	Reserved	0x0
2	OT_PROT_BIST_BYPASS	RW	Mask Fault reaction to (Temp2-Temp3) check failure in PowerUp state and Soc Activation state. 0x0: not masked 0x1: masked (*Note:* FLT_MASK** bit can be used to mask same fault reaction in other FuSa states)	0x0
1	ADC_BIST_BYPASS	RW	Mask fault reaction to ADC BIST failure in Self-Diagnosis state. (*ADC BIST - evaluation of ADC offset, BG channel, Int.LDOs channel, AVIN1/2 channels,PGND channel in Self Diagnosis state) 0x0: not masked 0x1: masked	0x0
0	Reserved	RO	Reserved	-

7.3.168 0x11B - FUSA_CTRL_B (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:5	SOC_ERR_CNT_MAX	RW	0x0: SoC Error Count check Disable 0x1: max cnt = 4 0x2: max cnt = 8 0x3: max cnt = 15	0x3
4:3	PMIC_ERR_CNT_MAX	RW	0x0: PMIC Error Count check Disable 0x1: max cnt = 4 0x2: max cnt = 8 0x3: max cnt = 15	0x3
2	ErrorToLock_TR_OPT_A	RW	AVIN(1,2) channel monitoring OV fault reaction 0x0: Error state 0x1: Lock state (*Note:* Error state is still be visited when going to Lock state)	0x0
1:0	Reserved	RO	Reserved	-

7.3.169 0x11C - FUSA_CTRL_C (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6	GC_SelfT_FltRecord_DIS	RW	Self Test Record for GC	0x0
5	PRESETb_DEEPSTOP	RW	PRESETb out data during Deep Stop only when no fault situation.	0x1
4:0	Reserved	RO	Reserved	-

7.3.170 0x11D - FUSA_CTRL_D (OTP)

Bit	Name	R/W	Description	Default
7	PgoodDlyTimerDone_DIS	RW	Control of exit from FuSa state power-up. 0x0: Exit power-up FuSa state upon receiving PGOOD GLB high from regulation **. 0x1: Exit Power-up FuSa state when its timer expires. **Limitation: PGOOD GLB must become high before power-up state timer expires. PGOOD GLB signal becomes high when all regulators have ramped up.	0x0
6	PRESET_CHECK_DIS	RW	PRESET#- PRESETOUT check in Soc Activation (External pin check1) 0x0: Enabled 0x1: Disabled	0x0
5	Reserved	RO	Reserved	0x0
4:0	EXTPINCHK2_EN	RW	Enable External pin check2 [4]: for PIN SDI_1 0x0: Not checked 0x1: Checked [3]: for PIN PRESETOUT 0x0: Not checked 0x1: Checked [2]: for PIN SDI_2 0x0: Not checked 0x1: Checked [1]: for PIN SDI_3 0x0: Not checked 0x1: Checked [0]: for PIN SDI_4 0x0: Not checked 0x1: Checked	0x00

7.3.171 0x11E - FUSA_CTRL_E (OTP)

Bit	Name	R/W	Description	Default
7:4	SDI_FltReAct	RW	SDI pins FuSa reaction configuration (* Applied when in Active FuSa state) [3]: SDI_4 pin 0x0: transition to RESET FuSa state 0x1: transition to Error FuSa state [2]: SDI_3 pin 0x0: transition to RESET FuSa state 0x1: transition to Error FuSa state [1]: SDI_2 pin 0x0: transition to RESET FuSa state 0x1: transition to Error FuSa state [0]: SDI_1 pin 0x0: transition to RESET FuSa state 0x1: transition to Error FuSa state	0x0
3:0	SDI_FltMask	RW	FuSa reaction Mask for SDI pins (*occuring in "ACTIVE" FuSa state) [3]: Apply to SDI_4 pin 0x0: Not masked 0x1: Masked [2]: Apply to SDI_3 pin 0x0: Not masked 0x1: Masked [1]: Apply to SDI_2 pin 0x0: Not masked 0x1: Masked [0]: Apply to SDI_1 pin. 0x0: Not masked 0x1: Masked	0x0

7.3.172 0x11F - SOC_PIN_DATA_1 (OTP)

Bit	Name	R/W	Description	Default
7:6	SDO_0_PIN_VAL_SACTIVASTIL	RW	SDO1 pin configuration in Stil State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x1
5:4	SDO_0_PIN_VAL_SOCACTIVA	RW	SDO1 pin configuration in SocActivation FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0
3:2	SDO_0_PIN_VAL_PupSeq	RW	SDO1 pin configuration in Power-Up FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x1
1:0	SDO_0_PIN_VAL_SELFD	RW	SDO1 pin configuratin in Self Diagnosis FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x2

7.3.173 0x120 - SOC_PIN_DATA_2 (OTP)

Bit	Name	R/W	Description	Default
7:6	SDO_0_PIN_VAL_LOCK	RW	SDO1 pin configuratin in Lock FuSa state 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x1
5:4	SDO_0_PIN_VAL_ERROR	RW	SDO1 pin configuration in Error FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x1
3:2	SDO_0_PIN_VAL_RESET	RW	SDO1 pin configuration in RESET FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0
1:0	SDO_0_PIN_VAL_ACTIVE	RW	SDO1 pin configuratin in Active FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0

7.3.174 0x121 - SOC_PIN_DATA_3 (OTP)

Bit	Name	R/W	Description	Default
7:6	SDO_1_PIN_VAL_ SACTIVASTIL	RW	SDO2 pin configuration in Stil State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x1
5:4	SDO_1_PIN_VAL_ SOCACTIVA	RW	SDO2 pin configuration in SocActivation FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0
3:2	SDO_1_PIN_VAL_PupSeq	RW	SDO2 pin configuration in Power-Up FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0
1:0	SDO_1_PIN_VAL_SELFD	RW	SDO2 pin configuratin in Self Diagnosis FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x2

7.3.175 0x122 - SOC_PIN_DATA_4 (OTP)

Bit	Name	R/W	Description	Default
7:6	SDO_1_PIN_VAL_LOCK	RW	SDO2 pin configuratin in Lock FuSa state 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0
5:4	SDO_1_PIN_VAL_ERROR	RW	SDO2 pin configuration in Error FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0
3:2	SDO_1_PIN_VAL_RESET	RW	SDO2 pin configuration in RESET FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x0
1:0	SDO_1_PIN_VAL_ACTIVE	RW	SDO2 pin configuratin in Active FuSa State 0x0: output mode, digital data 0 0x1: output mode, digital data 1 0x2: input mode, digital data Hi-Z 0x3: input mode, digital data Hi-Z	0x2

7.3.176 0x125 - FUSA_CTRL_CVM1 (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_SLOT1	RW	CVM SLOT 1 configuration [7]: Slot Enable 0x0: disabled 0x1: enabled [6:4]: Slot Delay (Samples received after reaching 75% of programmed delay are considered valid. Last valid sample is used for fault evaluation) 0x0: 256µs 0x1: 384µs 0x2: 512µs 0x3: 640µs 0x4: 1024µs 0x5: 1280µs 0x6: 1920µs 0x7: 2816µs [3:2]: Limit high and limit low threshold value register selection for ADC1 pin (SOC name -VTHREF0) 0x0: [Limit high register used -FUSA_CHK_CVM2H , Limit low register used -FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] 0x3: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] [1:0]: Limit high and limit low threshold value register selection for ADC2 pin (SOC name -VTHSENSE0) 0x0: [Limit high register used -FUSA_CHK_CVM2H, Limit high register used - FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L] 0x3: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L]	0x00

7.3.177 0x126 - FUSA_CTRL_CVM2 (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_SLOT2	RW	CVM SLOT 2 configuration [7]: Slot Enable 0x0: disabled 0x1: enabled [6:4]: Slot Delay (Samples received after reaching 75% of programmed delay are considered valid. Last valid sample is used for fault evaluation) 0x0: 256µs 0x1: 384µs 0x2: 512µs 0x3: 640µs 0x4: 1024µs 0x5: 1280µs 0x6: 1920µs 0x7: 2816µs [3:2]: Limit high and limit low threshold value register selection for ADC1 pin (SOC name -VTHREF0) 0x0: [Limit high register used -FUSA_CHK_CVM2H , Limit low register used -FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] 0x3: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] [1:0]: Limit high and limit low threshold value register selection for ADC2 pin (SOC name -VTHSENSE0) 0x0: [Limit high register used -FUSA_CHK_CVM2H, Limit high register used - FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L] 0x3: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L]	0x2D

7.3.178 0x127 - FUSA_CTRL_CVM3 (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_SLOT3	RW	CVM SLOT 3 configuration [7]: Slot Enable 0x0: disabled 0x1: enabled [6:4]: Slot Delay (Samples received after reaching 75% of programmed delay are considered valid. Last valid sample is used for fault evaluation) 0x0: 256µs 0x1: 384µs 0x2: 512µs 0x3: 640µs 0x4: 1024µs 0x5: 1280µs 0x6: 1920µs 0x7: 2816µs [3:2]: Limit high and limit low threshold value register selection for ADC1 pin (SOC name -VTHREF0) 0x0: [Limit high register used -FUSA_CHK_CVM2H , Limit low register used -FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] 0x3: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] [1:0]: Limit high and limit low threshold value register selection for ADC2 pin (SOC name -VTHSENSE0) 0x0: [Limit high register used -FUSA_CHK_CVM2H, Limit high register used - FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L] 0x3: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L]	0x7A

7.3.179 0x128 - FUSA_CTRL_CVM4 (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_SLOT4	RW	CVM SLOT 4 configuration [7]: Slot Enable 0x0: disabled 0x1: enabled [6:4]: Slot Delay (Samples received after reaching 75% of programmed delay are considered valid. Last valid sample is used for fault evaluation) 0x0: 256µs 0x1: 384µs 0x2: 512µs 0x3: 640µs 0x4: 1024µs 0x5: 1280µs 0x6: 1920µs 0x7: 2816µs [3:2]: Limit high and limit low threshold value register selection for ADC1 pin (SOC name -VTHREF0) 0x0: [Limit high register used -FUSA_CHK_CVM2H , Limit low register used -FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] 0x3: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] [1:0]: Limit high and limit low threshold value register selection for ADC2 pin (SOC name -VTHSENSE0) 0x0: [Limit high register used -FUSA_CHK_CVM2H, Limit high register used - FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L] 0x3: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L]	0x0A

7.3.180 0x129 - FUSA_CTRL_CVM5 (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_SLOT5	RW	CVM SLOT 5 configuration [7]: Slot Enable 0x0: disabled 0x1: enabled [6:4]: Slot Delay (Samples received after reaching 75% of programmed delay are considered valid. Last valid sample is used for fault evaluation) 0x0: 256µs 0x1: 384µs 0x2: 512µs 0x3: 640µs 0x4: 1024µs 0x5: 1280µs 0x6: 1920µs 0x7: 2816µs [3:2]: Limit high and limit low threshold value register selection for ADC1 pin (SOC name -VTHREF0) 0x0: [Limit high register used -FUSA_CHK_CVM2H , Limit low register used -FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] 0x3: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] [1:0]: Limit high and limit low threshold value register selection for ADC2 pin (SOC name -VTHSENSE0) 0x0: [Limit high register used -FUSA_CHK_CVM2H, Limit high register used - FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L] 0x3: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L]	0x2C

7.3.181 0x12A - FUSA_CTRL_CVM6 (OTP)

Bit	Name	R/W	Description	Default
7:0	CVM_SLOT6	RW	CVM SLOT 6 configuration [7]: Slot Enable 0x0: disabled 0x1: enabled [6:4]: Slot Delay (Samples received after reaching 75% of programmed delay are considered valid. Last valid sample is used for fault evaluation) 0x0: 256µs 0x1: 384µs 0x2: 512µs 0x3: 640µs 0x4: 1024µs 0x5: 1280µs 0x6: 1920µs 0x7: 2816µs [3:2]: Limit high and limit low threshold value register selection for ADC1 pin (SOC name -VTHREF0) 0x0: [Limit high register used -FUSA_CHK_CVM2H , Limit low register used -FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] 0x3: [Limit high register used -FUSA_CHK_CVM4H, Limit high register used -FUSA_CHK_CVM4L] [1:0]: Limit high and limit low threshold value register selection for ADC2 pin (SOC name -VTHSENSE0) 0x0: [Limit high register used -FUSA_CHK_CVM2H, Limit high register used - FUSA_CHK_CVM2L] 0x1: [Limit high register used -FUSA_CHK_CVM3H, Limit high register used -FUSA_CHK_CVM3L] 0x2: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L] 0x3: [Limit high register used -FUSA_CHK_CVM5H, Limit high register used -FUSA_CHK_CVM5L]	0x75

7.3.182 0x12C - FLT_MASK_B (OTP)

Bit	Name	R/W	Description	Default
7	FLT_MaskPmicErrExceed	RW	Fault reaction Mask for PMIC Error Exceed fault 0x0: Not masked 0x1: Masked	0x0
6	FLT_MaskSocErrExceed	RW	Fault reaction Mask for SOC Error Exceed fault 0x0: not masked 0x1: masked	0x0
5	FLT_MaskReguOT	RW	Fault reaction Mask for Regulation faults such as OV, UV, HSWOC, LSWUC etc. 0x0: Not masked 0x1: Masked	0x0
4	FLT_MaskWDT	RW	Fault reaction Mask for WDT fault 0x0: Not masked 0x1: Masked	0x0
3	FLT_MaskRegCRC	RW	Fault reaction Mask for communciation CRC fault 0x0: Not masked 0x1: Masked (*Note:* Masks regulation and protection CRC fault)	0x0
2	FLT_MaskClkMon	RW	Fault reaction Mask for the Clock monitoring faults (*excluding stuck at faults) 0x0: Not masked 0x1: Masked	0x0
1	FLT_MaskFaultDetectBist	RW	Fault reaction Mask for Fault Detect BIST failure (*BIST evaluated in FuSa state Self Diagnosis) 0x0: Masked 0x1: Not masked	0x0
0	FLT_MaskLBIST	RW	Fault reaction Mask for LBIST failure (*BIST evaluated in FuSa state Self Diagnosis) 0x0: Not masked 0x1: Masked	0x0

7.3.183 0x12D - ADCMON_MASK_GND_AVIN (OTP)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0x0
3	FaultMask_AVIN2_Prot	RW	Fault reaction Mask for ADC monitoring channel AVIN2 (Protection supply) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
2	FaultMask_AVIN1_Regu	RW	Fault reaction Mask for ADC monitoring channel AVIN1 (Regulation supply) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
1	FaultMask_PGND_Regu	RW	Fault reaction Mask for ADC monitoring channel PGND (Buck3 PGND) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
0	Reserved	RO	Reserved	-

7.3.184 0x12E - ADCMON_MASK_BG_TEMP (OTP)

Bit	Name	R/W	Description	Default
7:6	Reserved	RO	Reserved	0x1
5	FaultMask_Temp2_ ExtrLowTemp_Prot	RW	Fault reaction mask for TEMP2 channel (Protection Temperature sensor) extreem low tempearture limit violation 0x0: Not masked. 0x1: maksed.	0x0
4	FaultMask_Temp3_Prot	RW	Fault reaction Mask for Protection OT BIST 0x0: Not masked 0x1: Masked	0x0
3	FaultMask_Temp2_ShutDown_ Prot	RW	Fault reaction Mask for TEMP2 channel (Protection Temperature sensor) Shutdown limit violation 0x0: Not masked 0x1: Masked	0x0
2	FaultMask_Temp2_Warn_Prot	RW	Fault reaction Mask for TEMP2 channel (Protection Temperature sensor) Warning limit violation (*warning limit violation is evaluated at the time of exit from Error FuSa state) 0x0: Not masked - remain in Error state until Warning limit violation is removed 0x1: Masked - transition to Power-Up state after Error state timer expires.	0x0
1	FaultMask_Temp4_ShutDown_ Regu	RW	Fault reaction mask for TEMP4 channel (Regulation Temerature sensor) shutdown limit violation 0x0: Not masked. 0x1: maksed.	0x0
0	FaultMask_BG_Regu	RW	Fault reaction Mask for ADC monitoring channel BGRegu (Regulation bandgap) threshold limit violation 0x0: Not masked 0x1: Masked	0x0

7.3.185 0x12F - ADCMON_MASK_IntLDOs (OTP)

Bit	Name	R/W	Description	Default
7	FaultMask_IntLDO_5_Regu	RW	Fault reaction Mask for ADC monitoring channel Int. LDO5 Regu (Regulation Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
6	FaultMask_IntLDO_4_Regu	RW	Fault reaction Mask for ADC monitoring channel Int. LDO 4 Regu (Regulation Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
5	FaultMask_IntLDO_3_Regu	RW	Fault reaction Mask for ADC monitoring channel Int. LDO3 Regu (Regulation Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
4	FaultMask_IntLDO_2_Regu	RW	Fault reaction Mask for ADC monitoring channel Int. LDO2 Regu (Regulation Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
3	FaultMask_IntLDO_1_Regu	RW	Fault reaction Mask for ADC monitoring channel Int. LDO1 Regu (Regulation Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
2	FaultMask_IntLDO_0_Regu	RW	Fault reaction Mask for ADC monitoring channel Int. LDO0 Regu (Regulation Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
1	FaultMask_IntLDO_1_Prot	RW	Fault reaction Mask for ADC monitoring channel Int. LDO1 Prot (Protection Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
0	FaultMask_IntLDO_0_Prot	RW	Fault reaction Mask for ADC monitoring channel Int. LDO0 Prot (Protection Internal LDO) threshold limit violation 0x0: Not masked 0x1: Masked	0x0

7.3.186 0x130 - ADCMON_MASK_ExtLDOs (OTP)

Bit	Name	R/W	Description	Default
7	FaultMask_SPARE0_Prot	RW	Fault reaction mask for ADC monitoring channel SPARE0 (ADC5 - ADC4) threshold limit violation 0x0: Not masked 0x1: Masked	0x1
6	Reserved	RO	Reserved	0x0
5	FaultMask_ExtLDO_5	RW	Fault reaction Mask for ADC monitoring channel Ext.LDO5 (connected to regulator LDO 6) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
4	FaultMask_ExtLDO_4	RW	Fault reaction Mask for ADC monitoring channel Ext.LDO4 (connected to regulator LDO 5) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
3	FaultMask_ExtLDO_3	RW	Fault reaction Mask for ADC monitoring channel Ext.LDO3 (connected to regulator LDO 4) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
2	FaultMask_ExtLDO_2	RW	Fault reaction Mask for ADC monitoring channel Ext.LDO2 (connected to regulator LDO 3) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
1	FaultMask_ExtLDO_1	RW	Fault reaction Mask for ADC monitoring channel Ext.LDO1 (connected to regulator LDO 2) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
0	FaultMask_ExtLDO_0	RW	Fault reaction Mask for ADC monitoring channel Ext.LDO0 (connected to regulator LDO 1) threshold limit violation 0x0: Not masked 0x1: Masked	0x0

7.3.187 0x131 - ADCMON_MASK_BUCKs_B (OTP)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0x00
1	FaultMask_Buck1_VOUT_ Regu	RW	Fault reaction Mask for ADC monitoring channel VOUT1 (connected to sense terminal of Buck1) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
0	FaultMask_Buck1_PVIN_Regu	RW	Fault reaction Mask for ADC monitoring channel PVIN1 threshold limit violation 0x0: Not masked 0x1: Masked	0x0

7.3.188 0x132 - ADCMON_MASK_BUCKs_A (OTP)

Bit	Name	R/W	Description	Default
7	FaultMask_Buck5_VOUT_ Regu	RW	Fault reaction Mask for ADC monitoring channel VOUT5 (connected to sense terminal of Buck5) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
6	FaultMask_Buck5_PVIN_Regu	RW	Fault reaction Mask for ADC monitoring channel PVIN5 threshold limit violation 0x0: Not masked 0x1: Masked	0x0
5	FaultMask_Buck4_VOUT_ Regu	RW	Fault reaction Mask for ADC monitoring channel VOUT4 (connected to sense terminal of Buck4) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
4	FaultMask_Buck4_PVIN_Regu	RW	Fault reaction Mask for ADC monitoring channelPVIN4 (PVIN4) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
3	FaultMask_Buck3_VOUT_ Regu	RW	Fault reaction Mask for ADC monitoring channel VOUT3 (connected to sense terminal of Buck3) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
2	FaultMask_Buck3_PVIN_Regu	RW	Fault reaction Mask for ADC monitoring channel PVIN3 threshold limit violation 0x0: Not masked 0x1: Masked	0x0
1	FaultMask_Buck2_VOUT_ Regu	RW	Fault reaction Mask for ADC monitoring channel VOUT2 (connected to sense terminal of Buck2) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
0	FaultMask_Buck2_PVIN_Regu	RW	Fault reaction Mask for ADC monitoring channel PVIN2 (PVIN2) threshold limit violation 0x0: Not masked 0x1: Masked	0x0

7.3.189 0x133 - ADCMON_MASK_ExtINPs_7_0 (OTP)

Bit	Name	R/W	Description	Default
7	FaultMask_EXT_7_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 7 (available when external Mux mode selected) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
6	FaultMask_EXT_6_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 6 (available when external Mux mode selected) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
5	FaultMask_EXT_5_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 5 (available when external Mux mode selected) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
4	FaultMask_EXT_4_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 4 (ADC5, when this pin is analog input) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
3	FaultMask_EXT_3_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 3 (ADC4, when this pin is analog input) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
2	FaultMask_EXT_2_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 2 (ADC3, when this pin is analog input) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
1	FaultMask_EXT_1_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 1 (ADC2, when this pin is analog input) threshold limit violation 0x0: Not masked 0x1: Masked	0x0
0	FaultMask_EXT_0_Prot	RW	Fault reaction Mask for ADC monitoring channel EXT 0 (ADC1, when this pin is analog input) threshold limit violation 0x0: Not masked 0x1: Masked	0x0

7.3.190 0x134 - ADCMON_CFG (OTP)

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	-

7.3.191 0x135 - ADCMON_EXT_CFG (OTP)

Bit	Name	R/W	Description	Default
7:6	ExtAdcIO_Aux345Fix	RW	ADC3, ADC4, and ADC5 output behavior when supporting 16 external channels 0x0: [ADC5, ADC4, ADC3] pin output digital data auto increments every 45µs (control signal to external MUX to support 16 external channels) 0x1: [ADC5, ADC4, ADC3] pin output digital data is fixed. Data value = ADCMON_EXT_CFG[3:1]	0x0
5:4	Reserved	RO	Reserved	0x0
3:1	ExtAdcIO_Aux345Sel	RW	User entered digital output value This value becomes output on ADC5 through ADC3 pins if auto generation of MUX control is disabled . (ADCMON_EXT_CFG[7:6] = 0x1).	0x0
0	ExtAdcIO_AuxMODE	RW	Configuration selection of ADC1, ADC2, ADC3, ADC4, ADC5 pins 0x0: ADC1, ADC2, ADC3, ADC4, ADC5 pins are analog inputs. 0x1: ADC1 & ADC2 pins are analog inputs. ADC3, ADC4, ADC5 pins are digital output control signals for two 8x1 Muxes that support monitoring of 16 channels (EXT0 to EXT15)	0x0

7.3.192 0x136 - ADCMON_Gain_IIRCoeff_Offset (OTP)

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	-

7.3.193 0x13B - ADCMON_Gain_IIRCoeff_Temp (OTP)

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	-

7.3.194 0x13C - ADCMON_ShutDNLimitMSB_Temp (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_ShutDNLimitMSB_Temp	RW	Upper byte of 16 bit wide Temperature Shutdown threshold for Temp2 channel Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_Temp} → range -273 to 255°C 1 LSB = 0.25°C Example: in hex(258) = in dec(600) = in degC(150)	0x02

7.3.195 0x13D - ADCMON_ShutDNLimitLSB_Temp (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_ShutDNLimitLSB_Temp	RW	Lower byte of 16 bit wide Temperature Shutdown threshold for Temp2 channels Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_Temp} → range 0 to 255°C 1LSB = 0.25°C	0x58

7.3.196 0x13E - ADCMON_WarnLimitMSB_Temp (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_WarnLimitMSB_Temp	RW	Upper byte of 16 bit wide Temperature Warning threshold for Temp2 channel Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_Temp} → range 0 to 255°C 1LSB = 0.25°C Example: in hex(168) =in dec(360) = in degC(90)	0x01

7.3.197 0x13F - ADCMON_WarnLimitLSB_Temp (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_WarnLimitLSB_Temp	RW	Lower byte of 16 bit wide Temperature Warning threshold for Temp2 channel Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_Temp} → range 0 to 255°C 1LSB = 0.25°C	0x68

7.3.198 0x140 - ADCMON_ShutDNLimitMSB_Temp4 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_ShutDNLimitMSB_Temp4	RW	Upper byte of 16 bit wide Temperature Shutdown threshold for Temp4 channel Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_Temp} → range -273 to 255°C 1 LSB = 0.25^0 C Example: in hex(258) = in dec(600) = in degC(150)	0x02

7.3.199 0x141 - ADCMON_ShutDNLimitLSB_Temp4 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_ShutDNLimitLSB_Temp4	RW	Lower byte of 16 bit wide Temperature Shutdown threshold for Temp4 channel Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_Temp} → range -273 to 255°C 1LSB = 0.25°C	0x58

7.3.200 0x142 - ADCMON_Gain_IIRCoeff_BGRegu (OTP)

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	-

7.3.201 0x147 - ADCMON_Gain_IIRCoeff_PGNDRegu (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_PGNDRegu	RW	PGA GAIN settings for PGND (Regulation) channel (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x2
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_PGNDRegu	RW	IIR coefficient settings for PGND (Regulation) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.202 0x148 - ADCMON_LimHighMSB_PGNDRegu (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_PGNDRegu	RW	Upper byte of 16 bit wide Limit High threshold for PGND (Regulation) channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV Example: in hex(4C2) = in dec(1218) = in mV(1218 x 0.25mV = 304)	0x04

7.3.203 0x149 - ADCMON_LimHighLSB_PGNDRegu (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_PGNDRegu	RW	Lower byte of 16 bit wide Limit High threshold for PGND (Regulation) channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV	0xC2

7.3.204 0x14A - ADCMON_LimLowMSB_PGNDRegu (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_PGND Regu	RW	Upper byte of 16 bit wide Limit Low threshold for PGND (Regulation) channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV Default value = -295.5mV (0xFB62) Example: in hex(FB62) = in dec(-1182) = in mV(-1182 x 0.25mV = -295.5)	0xFB

7.3.205 0x14B - ADCMON_LimLowLSB_PGNDRegu (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_PGND Regu	RW	Lower byte of 16 bit wide Limit Low threshold for PGND (Regulation) channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV	0x62

7.3.206 0x14C - ADCMON_Gain_IIRCoeff_IntLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	-

7.3.207 0x151 - ADCMON_Gain_IIRCoeff_AVIN1 (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_AVIN1	RW	PGA GAIN settings for AVIN1 and AVIN2 (power supplies) channels (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0

Bit	Name	R/W	Description	Default
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_AVIN1	RW	IIR coefficient settings for AVIN1 and AVIN2 (power supplies) channels 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.208 0x152 - ADCMON_LimHighMSB_AVIN1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ AVIN1	RW	Upper byte of 16 bit wide Limit High threshold for AVIN1 (Regulation power supply) channel Limit = {ADCMON_LimHighMSB_AVIN1, ADCMON_LimHighLSB_AVIN1} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.209 0x153 - ADCMON_LimHighLSB_AVIN1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_AVIN1	RW	Lower byte of 16 bit wide Limit High threshold for AVIN1 (Regulation power supply) channel Limit = {ADCMON_LimHighMSB_AVIN1, ADCMON_LimHighLSB_AVIN1} 1LSB = 0.25mV	0xF8

7.3.210 0x154 - ADCMON_LimLowMSB_AVIN1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_AVIN1	RW	Upper byte of 12 bit wide Limit Low threshold for AVIN1 (Regulation power supply) channel Limit = {ADCMON_LimHighMSB_AVIN1, ADCMON_LimHighLSB_AVIN1} 1LSB = 0.25mV Default value =2.6047V (0x28B2) Example: in hex(28B2) = in dec(10418) = in mV(10418 x 0.25mV = 2604)	0x28

7.3.211 0x155 - ADCMON_LimLowLSB_AVIN1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_AVIN1	RW	Lower byte of 16 bit wide Limit Low threshold for AVIN1 (Regulation power supply) channel Limit = {ADCMON_LimHighMSB_AVIN1, ADCMON_LimHighLSB_AVIN1} 1LSB = 0.25mV	0xB2

7.3.212 0x156 - ADCMON_Gain_IIRCoeff_SPARE_0 (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_SPARE_0	RW	PGA GAIN settings for SPARE_0 channel (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x2
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_SPARE_0	RW	IIR coefficient settings for SPARE_0 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.213 0x157 - ADCMON_LimHighMSB_SPARE_0 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ SPARE_0	RW	Upper byte of 16 bit wide Limit High threshold for SPARE_0 channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV Default value = +304.5mV (0x04C2) Example: in hex(4C2) = in dec(1218) = in mV(1218 x 0.25mV = 304.5)	0x04

7.3.214 0x158 - ADCMON_LimHighLSB_SPARE_0 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ SPARE_0	RW	Lower byte of 16 bit wide Limit High threshold for SPARE_0 channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV	0xC2

7.3.215 0x159 - ADCMON_LimLowMSB_SPARE_0 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ SPARE_0	RW	Upper byte of 16 bit wide Limit Low threshold for SPARE_0 channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV Example: in hex(FB62) = in dec(-1182) = in mV(-1182 x 0.25mV = -295.5)	0xFB

7.3.216 0x15A - ADCMON_LimLowLSB_SPARE_0 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ SPARE_0	RW	Lower byte of 16 bit wide Limit Low threshold for SPARE_0 channel Limit = {ADCMON_LimHighMSB_PGNDRegu, ADCMON_LimHighLSB_PGNDRegu} 1LSB = 0.25mV	0x62

7.3.217 0x15B - extLDO_0_ADCMON_Gain_IIRCoeff_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_ExtLDO	RW	PGA GAIN settings for Ext.LDO 1 channel (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x4
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_ExtLDO	RW	IIR coefficient settings for Ext.LDO1 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.218 0x15C - extLDO_0_ADCMON_LimHighMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit High threshold for Ext.LDO1 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(1D1E) = in dec(7454) = in mV(7454 x 0.25mV = 1863)	0x1D

7.3.219 0x15D - extLDO_0_ADCMON_LimHighLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit High threshodl for Ext.LDO1 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x1E

7.3.220 0x15E - extLDO_0_ADCMON_LimLowMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ ExtLDO	RW	Upper byte of 16 bit Limit Low threshold for Ext.LDO1 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(1B21) = in dec(6945) = in mV(6945 x 0.25mV = 1736)	0x1B

7.3.221 0x15F - extLDO_0_ADCMON_LimLowLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit Low threshold for Ext.LDO1 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x21

7.3.222 0x160 - extLDO_1_ADCMON_Gain_IIRCoeff_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_ExtLDO	RW	PGA GAIN settings for Ext.LDO2 channel (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_ExtLDO	RW	IIR coefficient settings for Ext.LDO2 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.223 0x161 - extLDO_1_ADCMON_LimHighMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit High threshold for Ext.LDO2 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(2D4B) = in dec(11595) = in mV(11595 x 0.25mV = 2898)	0x2D

7.3.224 0x162 - extLDO_1_ADCMON_LimHighLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit High threshold for Ext.LDO2 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x4B

7.3.225 0x163 - extLDO_1_ADCMON_LimLowMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit Low threshold for Ext.LDO2 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(2A34) = in dec(10804) = in mV(10804 x 0.25mV = 2701)	0x2A

7.3.226 0x164 - extLDO_1_ADCMON_LimLowLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit Low threshold for Ext.LDO2 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x34

7.3.227 0x165 - extLDO_2_ADCMON_Gain_IIRCoeff_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_ExtLDO	RW	PGA GAIN settings for Ext.LDO3 channel (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x4
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_ExtLDO	RW	IIR coefficient settings for Ext.LDO3 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.228 0x166 - extLDO_2_ADCMON_LimHighMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit High threshold for Ext.LDO3 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Default value = 1. 8635V (0x1D1E) Example: in hex(1D1E) = in dec(7454) = in mV(7454 x 0.25mV = 1863.5)	0x1D

7.3.229 0x167 - extLDO_2_ADCMON_LimHighLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit High threshold for Ext.LDO3 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x1E

7.3.230 0x168 - extLDO_2_ADCMON_LimLowMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit Low threshold for Ext.LDO3 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Default value = 1. 7365V (0x1B21) Example: in hex(1B21) = in dec(6945) = in mV(6945 x 0.25mV = 1736.5)	0x1B

7.3.231 0x169 - extLDO_2_ADCMON_LimLowLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit Low threshold for Ext.LDO3 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x21

7.3.232 0x16A - extLDO_3_ADCMON_Gain_IIRCoeff_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_ExtLDO	RW	PGA GAIN settings for Ext.LDO4 channel (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_ExtLDO	RW	IIR coefficient settings for Ext.LDO4 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.233 0x16B - extLDO_3_ADCMON_LimHighMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit High threshold for Ext.LDO4 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(2D4B) = in dec(11595) = in mV(11595 x 0.25mV = 2898.5)	0x2D

7.3.234 0x16C - extLDO_3_ADCMON_LimHighLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit High threshold for Ext.LDO4 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x4B

7.3.235 0x16D - extLDO_3_ADCMON_LimLowMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit Low threshold for Ext.LDO4 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(2A34) = in dec(10804) = in mV(10804 x 0.25mV = 2701)	0x2A

7.3.236 0x16E - extLDO_3_ADCMON_LimLowLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit Low threshold for Ext.LDO4 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x34

7.3.237 0x16F - extLDO_4_ADCMON_Gain_IIRCoeff_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_ExtLDO	RW	PGA GAIN settings for Ext.LDO5 channel (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x4
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_ExtLDO	RW	IIR coefficient settings for Ext.LDO5 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.238 0x170 - extLDO_4_ADCMON_LimHighMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit High threshold for Ext.LDO5 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Default value = 1. 8635V (0x1D1E) Example: in hex(1D1E) = in dec(7454) = in mV(7454 x 0.25mV = 1863.5)	0x1D

7.3.239 0x171 - extLDO_4_ADCMON_LimHighLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit High threshold for Ext.LDO5 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x1E

7.3.240 0x172 - extLDO_4_ADCMON_LimLowMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit Low threshold for Ext.LDO5 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(1B21) = in dec(6945) = in mV(6945 x 0.25mV = 1736.5)	0x1B

7.3.241 0x173 - extLDO_4_ADCMON_LimLowLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit Low threshold for Ext.LDO5 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x21

7.3.242 0x174 - extLDO_5_ADCMON_Gain_IIRCoeff_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_ExtLDO	RW	PGA GAIN settings for Ext.LDO6 channel (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_ExtLDO	RW	IIR coefficient settings for Ext.LDO6 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.243 0x175 - extLDO_5_ADCMON_LimHighMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit High threshold for Ext.LDO6 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(2D4B) = in dec(11595) = in mV(11595 x 0.25mV = 2898.5)	0x2D

7.3.244 0x176 - extLDO_5_ADCMON_LimHighLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit High threshold for Ext.LDO6 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x4B

7.3.245 0x177 - extLDO_5_ADCMON_LimLowMSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ ExtLDO	RW	Upper byte of 16 bit wide Limit Low threshold for Ext.LDO6 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(2A34) = in dec(10804) = in mV(10804 x 0.25mV = 2701)	0x2A

7.3.246 0x178 - extLDO_5_ADCMON_LimLowLSB_ExtLDO (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ ExtLDO	RW	Lower byte of 16 bit wide Limit Low threshold for Ext.LDO6 channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV	0x34

7.3.247 0x179 - PVIN_0_ADCMON_Gain_IIRCoeff_PVIN (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_PVIN	RW	PGA GAIN settings for PVIN1(power stage supply of Buck1) channel (*Input voltage = 1/7.5 * PVIN1) (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x6
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_PVIN	RW	IIR coefficient settings for PVIN1 (power stage supply of Buck1) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.248 0x17A - PVIN_0_ADCMON_LimHighMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_PVIN	RW	Upper byte of 16 bit wide Limit High threshold for PVIN1 (power stage supply of Buck1) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV Example: in hex(B90) = in dec(2960) = in mV(2960 x 0.25mV = 740)	0x0B

7.3.249 0x17B - PVIN_0_ADCMON_LimHighLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_PVIN	RW	Lower byte of 16 bit wide Limit High threshold for PVIN1(power stage supply of Buck1) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x90

7.3.250 0x17C - PVIN_0_ADCMON_LimLowMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_PVIN	RW	Upper byte of 16 bit wide Limit Low threshold for PVIN1 (power stage supply of Buck1) channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Default value = 330mV (0x535) Example: in hex(535) = in dec(1333) = in mV(1333 x 0.25mV = 330)	0x05

7.3.251 0x17D - PVIN_0_ADCMON_LimLowLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_PVIN	RW	Lower byte of 16 bit wide Limit Low threshold for PVIN1 (power stage supply of Buck1) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x35

7.3.252 0x17E - PVIN_1_ADCMON_Gain_IIRCoeff_PVIN (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_PVIN	RW	PGA GAIN settings for PVIN2 (power stage supply of Buck2) channel (*Input voltage = 1/7.5 x PVIN2) (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x6
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_PVIN	RW	IIR coefficient settings for PVIN2 (power stage supply of Buck2) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.253 0x17F - PVIN_1_ADCMON_LimHighMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_PVIN	RW	Upper byte of 16 bit wide Limit High threshold for PVIN2 (power stage supply of Buck2) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV Example: in hex(B90) = in dec(2960) = in mV(2960 x 0.25mV = 740)	0x0B

7.3.254 0x180 - PVIN_1_ADCMON_LimHighLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_PVIN	RW	Lower byte of 16 bit wide Limit High threshold for PVIN2(power stage supply of Buck2) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x90

7.3.255 0x181 - PVIN_1_ADCMON_LimLowMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_PVIN	RW	Upper byte of 16 bit wide Limit Low threshold for PVIN2 (power stage supply of Buck2) channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(535) = in dec(1333) = in mV(1333 x 0.25mV = 330)	0x05

7.3.256 0x182 - PVIN_1_ADCMON_LimLowLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_PVIN	RW	Lower byte of 16 bit wide Limit Low threshold for PVIN2 (power stage supply of Buck2) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x35

7.3.257 0x183 - PVIN_2_ADCMON_Gain_IIRCoeff_PVIN (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_PVIN	RW	PGA GAIN settings for PVIN3 (power stage supply of Buck3) channel (*Input voltage = 1/7.5 x PVIN3) (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x6
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_PVIN	RW	IIR coefficient settings for PVIN3 (power stage supply of Buck1) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.258 0x184 - PVIN_2_ADCMON_LimHighMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_PVIN	RW	Upper byte of 16 bit wide Limit High threshold for PVIN3 (power stage supply of Buck3) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV Example: in hex(B90) = in dec(2960) = in mV(2960 x 0.25mV = 740)	0x0B

7.3.259 0x185 - PVIN_2_ADCMON_LimHighLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_PVIN	RW	Lower byte of 16 bit wide Limit High threshold for PVIN3(power stage supply of Buck3) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x90

7.3.260 0x186 - PVIN_2_ADCMON_LimLowMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_PVIN	RW	Upper byte of 16 bit wide Limit Low threshold for PVIN3 (power stage supply of Buck3) channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(535) = in dec(1333) = in mV(1333 x 0.25mV = 330)	0x05

7.3.261 0x187 - PVIN_2_ADCMON_LimLowLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_PVIN	RW	Lower byte of 16 bit wide Limit Low threshold for PVIN3 (power stage supply of Buck3) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x35

7.3.262 0x188 - PVIN_3_ADCMON_Gain_IIRCoeff_PVIN (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_PVIN	RW	PGA GAIN settings for PVIN4 (power stage supply of Buck4) channel (*Input voltage = 1/7.5 x PVIN4) (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x6
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_PVIN	RW	IIR coefficient settings for PVIN4 (power stage supply of Buck4) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.263 0x189 - PVIN_3_ADCMON_LimHighMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_PVIN	RW	Upper byte of 16 bit wide Limit High threshold for PVIN4 (power stage supply of Buck4) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV Example: in hex(B90) = in dec(2960) = in mV(2960 x 0.25mV = 740)	0x0B

7.3.264 0x18A - PVIN_3_ADCMON_LimHighLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_PVIN	RW	Lower byte of 16 bit wide Limit High threshold for PVIN4(power stage supply of Buck4) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x90

7.3.265 0x18B - PVIN_3_ADCMON_LimLowMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_PVIN	RW	Upper byte of 16 bit wide Limit Low threshold for PVIN4 (power stage supply of Buck1) channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(535) = in dec(1333) = in mV(1333 x 0.25mV = 330)	0x05

7.3.266 0x18C - PVIN_3_ADCMON_LimLowLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_PVIN	RW	Lower byte of 16 bit wide Limit Low threshold for PVIN4 (power stage supply of Buck4) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x35

7.3.267 0x18D - PVIN_4_ADCMON_Gain_IIRCoeff_PVIN (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_PVIN	RW	PGA GAIN settings for PVIN5 (power stage supply of Buck5) channel (*Input voltage = 1/7.5 x PVIN5) (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x6
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_PVIN	RW	IIR coefficient settings for PVIN5 (power stage supply of Buck5) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.268 0x18E - PVIN_4_ADCMON_LimHighMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_PVIN	RW	Upper byte of 16 bit wide Limit High threshold for PVIN5 (power stage supply of Buck5) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV Example: in hex(B90) = in dec(2960) = in mV(2960 x 0.25mV = 740)	0x0B

7.3.269 0x18F - PVIN_4_ADCMON_LimHighLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_PVIN	RW	Lower byte of 16 bit wide Limit High threshold for PVIN5(power stage supply of Buck5) channel Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x90

7.3.270 0x190 - PVIN_4_ADCMON_LimLowMSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_PVIN	RW	Upper byte of 16 bit wide Limit Low threshold for PVIN5 (power stage supply of Buck5) channel Limit = {ADCMON_LimHighMSB_ExtLDO, ADCMON_LimHighLSB_ExtLDO} 1LSB = 0.25mV Example: in hex(535) = in dec(1333) = in mV(1333 x 0.25mV = 330)	0x05

7.3.271 0x191 - PVIN_4_ADCMON_LimLowLSB_PVIN (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_PVIN	RW	Lower byte of 16 bit wide Limit Low threshold for PVIN5 (power stage supply of Buck5) channel (Regulation) threshold (lower) Limit = {ADCMON_LimHighMSB_PVIN, ADCMON_LimHighLSB_PVIN} 1LSB = 0.25mV	0x35

7.3.272 0x192 - VOUT_0_ADCMON_Gain_IIRCoeff_VOUT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_VOUT	RW	PGA GAIN setting for VOUT1 (remote voltage sense of Buck1) channel (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x5
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_VOUT	RW	IIR coefficient settings for VOUT1 (remote voltage sense of Buck1) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.273 0x193 - VOUT_0_ADCMON_LimHighMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ VOUT	RW	Upper byte of 16 bit wide Limit High threshold for VOUT1 (remote voltage sense of Buck1) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Default value = 828.3V (0x0CF0) Example: in hex(CF0) = in dec(3312) = in mV(3312 x 0.25mV = 828.25)	0x0C

7.3.274 0x194 - VOUT_0_ADCMON_LimHighLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_VOUT	RW	Lower byte of 16 bit wide Limit High threshold for VOUT1 (remote voltage sense of Buck1) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0xF0

7.3.275 0x195 - VOUT_0_ADCMON_LimLowMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_VOUT	RW	Upper byte of 16 bit wide Limit Low threshold for VOUT1 (remote voltage sense of Buck1) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} Example: in hex(C0F) = in dec(2960) = in mV(2960 x 0.25mV = 771.75)	0x0C

7.3.276 0x196 - VOUT_0_ADCMON_LimLowLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_VOUT	RW	Lower byte of 16 bit wide Limit Low threshold for VOUT1 (remote voltage sense of Buck1) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0x0F

7.3.277 0x197 - VOUT_1_ADCMON_Gain_IIRCoeff_VOUT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_VOUT	RW	PGA GAIN settings for VOUT2 (remote voltage sense of Buck2) channel (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x1
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_VOUT	RW	IIR coefficient settings for VOUT2 (remote voltage sense of Buck2) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.278 0x198 - VOUT_1_ADCMON_LimHighMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_VOUT	RW	Upper byte of 16 bit wide Limit High threshold for VOUT2 (remote voltage sense of Buck2) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Example: in hex(11CB0) = in dec(4555) = in mV(4555 x 0.25mV = 1138.75)	0x11

7.3.279 0x199 - VOUT_1_ADCMON_LimHighLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_VOUT	RW	Lower byte of 16 bit wide Limit High threshold for VOUT2 (remote voltage sense of Buck2) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0xCB

7.3.280 0x19A - VOUT_1_ADCMON_LimLowMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_VOUT	RW	Upper byte of 16 bit wide Limit Low threshold for VOUT2 (remote voltage sense of Buck2) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Example: in hex(1094) = in dec(4244) = in mV(4244 x 0.25mV = 1061)	0x10

7.3.281 0x19B - VOUT_1_ADCMON_LimLowLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_VOUT	RW	Lower byte of 16 bit wide Limit Low threshold for VOUT2 (remote voltage sense of Buck2) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0x94

7.3.282 0x19C - VOUT_2_ADCMON_Gain_IIRCoeff_VOUT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_VOUT	RW	PGA GAIN settings for VOUT3 (remote voltage sense of Buck3) channel (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x4
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_VOUT	RW	IIR coefficient settings for VOUT3 (remote voltage sense of Buck3) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.283 0x19D - VOUT_2_ADCMON_LimHighMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_VOUT	RW	Upper byte of 16 bit wide Limit High threshold for VOUT3 (remote voltage sense of Buck3) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Example: in hex(1D1E) = in dec(7454) = in mV(7454 x 0.25mV = 1863)	0x1D

7.3.284 0x19E - VOUT_2_ADCMON_LimHighLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_VOUT	RW	Lower byte of 16 bit wide Limit High threshold for VOUT3 (remote voltage sense of Buck3) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0x1E

7.3.285 0x19F - VOUT_2_ADCMON_LimLowMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_VOUT	RW	Upper byte of 16 bits wide Limit High threshold for VOUT3 (remote voltage sense of Buck3) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} → range 0 to 2.4V 1LSB = 0.25mV Example: in hex(47B) = in dec(1147) = in mV(1147 x 0.25mV = 286)	0x04

7.3.286 0x1A0 - VOUT_2_ADCMON_LimLowLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_VOUT	RW	Lower byte of 16 bits for VOUT3 remote voltage sense (Regulation) threshold (lower) Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0x7B

7.3.287 0x1A1 - VOUT_3_ADCMON_Gain_IIRCoeff_VOUT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_VOUT	RW	PGA GAIN settings for VOUT4 (remote voltage sense of Buck4) channel (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_VOUT	RW	IIR coefficient settings for VOUT4 (remote voltage sense of Buck4) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.288 0x1A2 - VOUT_3_ADCMON_LimHighMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_VOUT	RW	Upper byte of 16 bit wide Limit High threshold for VOUT4 (remote voltage sense of Buck4) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Example: in hex(3561) = in dec(13665) = in mV(13665 x 0.25mV = 3416)	0x35

7.3.289 0x1A3 - VOUT_3_ADCMON_LimHighLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_VOUT	RW	Lower byte of 16 bit wide Limit High threshold for VOUT4 (remote voltage sense of Buck4) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0x61

7.3.290 0x1A4 - VOUT_3_ADCMON_LimLowMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_VOUT	RW	Upper byte of 16 bit wide Limit Low threshold for VOUT4 (remote voltage sense of Buck4) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Example: in hex(31BE) = in dec(12734) = in mV(12734 x 0.25mV = 3183)	0x31

7.3.291 0x1A5 - VOUT_3_ADCMON_LimLowLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_VOUT	RW	Lower byte of 16 bit wide Limit Low threshold for VOUT4 (remote voltage sense of Buck4) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0xBE

7.3.292 0x1A6 - VOUT_4_ADCMON_Gain_IIRCoeff_VOUT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_VOUT	RW	PGA GAIN settings for VOUT5 (remote voltage sense of Buck5) channel (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x1
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_VOUT	RW	IIR coefficient settings for VOUT5 (remote voltage sense of Buck5) channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.293 0x1A7 - VOUT_4_ADCMON_LimHighMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_VOUT	RW	Upper byte of 16 bit wide Limit High threshold for VOUT5 (remote voltage sense of Buck5) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Example: in hex(1369) = in dec(4969) = in mV(4969 x 0.25mV = 1242)	0x13

7.3.294 0x1A8 - VOUT_4_ADCMON_LimHighLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_VOUT	RW	Lower byte of 16 bit wide Limit High threshold for VOUT5 (remote voltage sense of Buck5) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0x69

7.3.295 0x1A9 - VOUT_4_ADCMON_LimLowMSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_VOUT	RW	Upper byte of 16 bit wide Limit Low threshold for VOUT5 (remote voltage sense of Buck5) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV Default value = 1. 157V (0x1216) Example: in hex(1216) = in dec(4630) = in mV(4630 x 0.25mV = 1157)	0x12

7.3.296 0x1AA - VOUT_4_ADCMON_LimLowLSB_VOUT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_VOUT	RW	Lower byte of 16 bit wide Limit Low threshold for VOUT5 (remote voltage sense of Buck5) channel Limit = {ADCMON_LimHighMSB_VOUT, ADCMON_LimHighLSB_VOUT} 1LSB = 0.25mV	0x16

7.3.297 0x1AB - EXT_0_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT0 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT0 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.298 0x1AC - EXT_0_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT0 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.299 0x1AD - EXT_0_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT0 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.300 0x1AE - EXT_0_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT0 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0xFC

7.3.301 0x1AF - EXT_0_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT0 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x18

7.3.302 0x1B0 - EXT_1_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT1 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT1 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.303 0x1B1 - EXT_1_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT1 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.304 0x1B2 - EXT_1_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT1 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.305 0x1B3 - EXT_1_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT1 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0xFC

7.3.306 0x1B4 - EXT_1_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT1 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x18

7.3.307 0x1B5 - EXT_2_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT2 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT2 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.308 0x1B6 - EXT_2_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT2 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.309 0x1B7 - EXT_2_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT2 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.310 0x1B8 - EXT_2_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT2 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0x00

7.3.311 0x1B9 - EXT_2_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT2 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x00

7.3.312 0x1BA - EXT_3_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT3 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT3 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.313 0x1BB - EXT_3_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT3 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.314 0x1BC - EXT_3_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT3 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.315 0x1BD - EXT_3_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT3 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0x00

7.3.316 0x1BE - EXT_3_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT3 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x00

7.3.317 0x1BF - EXT_4_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT4 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT4 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.318 0x1C0 - EXT_4_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT4 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.319 0x1C1 - EXT_4_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT4 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.320 0x1C2 - EXT_4_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT4 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0x00

7.3.321 0x1C3 - EXT_4_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT4 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x00

7.3.322 0x1C4 - EXT_5_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT5 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT5 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.323 0x1C5 - EXT_5_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT5 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.324 0x1C6 - EXT_5_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT5 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.325 0x1C7- EXT_5_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT5 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0x00

7.3.326 0x1C8 - EXT_5_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT5 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x00

7.3.327 0x1C9 - EXT_6_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT6 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT6 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.328 0x1CA - EXT_6_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT6 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.329 0x1CB - EXT_6_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT6 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.330 0x1CC - EXT_6_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT6 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0x00

7.3.331 0x1CD - EXT_6_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT6 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x00

7.3.332 0x1CE - EXT_7_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT7 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT7 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.333 0x1CF - EXT_7_ADCMON_LimHighMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_EXT	RW	Upper byte of 16 bit wide Limit High threshold for EXT7 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(58F8) = in dec(22776) = in mV(22776 x 0.25mV = 5694)	0x58

7.3.334 0x1D0 - EXT_7_ADCMON_LimHighLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_EXT	RW	Lower byte of 16 bit wide Limit High threshold for EXT7 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0xF8

7.3.335 0x1D1 - EXT_7_ADCMON_LimLowMSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_EXT	RW	Upper byte of 16 bit wide Limit Low threshold for EXT7 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV Example: in hex(FC18) = in dec(-1000) = in mV(-1000 x 0.25mV = -250)	0x00

7.3.336 0x1D2 - EXT_7_ADCMON_LimLowLSB_EXT (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_EXT	RW	Lower byte of 16 bit wide Limit Low threshold for EXT7 channel Limit = {ADCMON_LimHighMSB_EXT, ADCMON_LimHighLSB_EXT} 1LSB = 0.25mV	0x00

7.3.337 0x1D3 - EXT_8_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT8 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT8 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.338 0x1D4 - EXT_9_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN setting for EXT9 channel. 0x0: 0.125 (default) 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT9 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 (default) 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.339 0x1D5 - EXT_10_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT10 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT10 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.340 0x1D6 - EXT_11_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN setting for EXT11 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT11 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.341 0x1D7 - EXT_12_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT12 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT12 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.342 0x1D8 - EXT_13_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN setting for EXT13 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT13 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.343 0x1D9 - EXT_14_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN setting for EXT14 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT14 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.344 0x1DA - EXT_15_ADCMON_Gain_IIRCoeff_EXT (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_EXT	RW	PGA GAIN settings for EXT15 channel. (*Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x0
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_EXT	RW	IIR coefficient settings for EXT15 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.345 0x264 - I_FUSA_CTRL_DBG (OTP)

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	0x0
2	I_LOCK_RELEASE	RW	Writing to this register takes system from LOCK state to SELF_DIAGNOSIS state. It is cleared in SELF DIAGNOSIS state.	0x0
1:0	I_LOCK_RELEASE_PinSel	RW	Setting this register to accept the LOCK release function by the PIN(ADC3). 0x0: Use LockReleasePin Rising Edge 0x1: Use LockReleasePin Falling Edge 0x2: Use LockReleasePin level high(active high) 0x3: LOCK release function is not be performed by the PIN	0x1

7.3.346 0x301 - ADCMON_Gain_IIRCoeff_SPARE_1 (OTP)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0x0
6:4	ADC_PGA_Gain_SPARE_1	RW	PGA GAIN settings for SPARE_1 channel. (* Input voltage x PGA Gain < V(BG)/1.25, V(BG) = ~ 1.231V must be satisfied) 0x0: 0.125 0x1: 0.5 0x2: 2 0x3: 8 0x4: 0.333 0x5: 0.8 0x6: 1.25 0x7: 1.4 (*Note:* Refer to data sheet for ADC Full Scale values of each PGA gain setting)	0x2
3	Reserved	RO	Reserved	0x0
2:0	ADC_IIR_Coeff_SPARE_1	RW	IIR coefficient settings for SPARE_1 channel 0x0: 1(no averaging) 0x1: 1/2 0x2: 1/4 0x3: 1/8 0x4: 1/16 0x5: 1/32 0x6: 1/64 0x7: 1/128	0x4

7.3.347 0x302 - ADCMON_LimHighMSB_SPARE_1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighMSB_ SPARE_1	RW	Upper byte of 16 bit wide Limit High threshold for SPARE_1 channel Limit = {ADCMON_LimHighMSB_SPARE_1, ADCMON_LimHighLSB_SPARE_1} 1LSB = 0.25mV Example: in hex(20B) = in dec(523) = in mV(523x0.25mV = 130)	0x02

7.3.348 0x303 - ADCMON_LimHighLSB_SPARE_1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimHighLSB_ SPARE_1	RW	Lower byte of 16 bit wide Limit High threshold for SPARE_1 channel Limit = {ADCMON_LimHighMSB_SPARE_1, ADCMON_LimHighLSB_SPARE_1} 1LSB = 0.25mV	0x0B

7.3.349 0x304 - ADCMON_LimLowMSB_SPARE_1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowMSB_ SPARE_1	RW	Upper byte of 16 bit wide Limit Low threshold for SPARE_1 channel Limit = {ADCMON_LimHighMSB_SPARE_1, ADCMON_LimHighLSB_SPARE_1} 1LSB = 0.25mV Example: in hex(FB62) = in dec(-1182) = in mV(-1182 x 0.25mV = -295)	0xFB

7.3.350 0x305 - ADCMON_LimLowLSB_SPARE_1 (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_LimLowLSB_ SPARE_1	RW	Lower byte of 16 bit wide Limit Low threshold for SPARE_1 channel Limit = {ADCMON_LimHighMSB_SPARE_1, ADCMON_LimHighLSB_SPARE_1} 1LSB = 0.25mV	0x62

7.3.351 0x306 - ADCMON_ShutDNLimitMSB_Temp_2B (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_ShutDNLimitMSB_ Temp_2B	RW	Upper byte of 16 bit wide Temperature Shutdown threshold for Temp2 channel: This value is applied only in SOC Activation state. Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_Temp} → range 0 to 255°C 1 LSB = 0.25°C Example: in hex(258) = in dec(600) = in degC(150)	0x02

7.3.352 0x307 - ADCMON_ShutDNLimitLSB_Temp_2B (OTP)

Bit	Name	R/W	Description	Default
7:0	ADCMON_ShutDNLimitLSB_ Temp_2B	RW	Lower byte of 16 bit wide Temperature Shutdown threshold for Temp2 and Temp3 channels: This value is applied only in SOC Activation state. Limit = {ADCMON_ShutDNLimitMSB_Temp, ADCMON_ShutDNLimitLSB_ Temp} → range 0 to 255°C 1LSB = 0.25°C	0x58

7.3.353 0x309 – FUSA_TIMER_5 (OTP)

Bit	Name	R/W	Description	Default
7:0	Reserved	RO	Reserved	0x0
1:0	DeepStop_PRESETb_EXT_ TIMER	RO	Timer for extending PRESETb pin high at the entrance of DeepStop 0x0: 0ms 0x1: 1ms 0x2: 2ms 0x3: 8ms	0x2

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

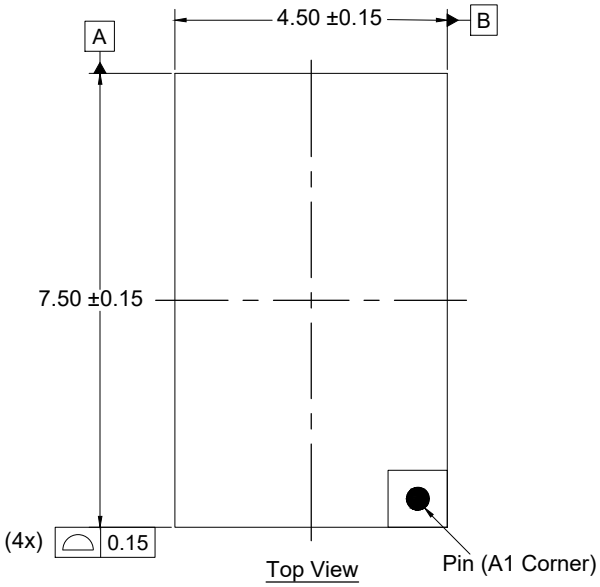
9. Ordering Information

Part Number[1][2]	Part Marking	Buck1 I_{OUT}	OTP Configuration[3]	Package Description[4] (RoHS Compliant)	Pkg. Dwg #	Carrier Type[5]	Temp. Range
RAA271005A4HBG#AC0	271005 A4HBG	12A	No customized OTP	66 Ball BGA, 7.5mm×4.5mm	V66.4.50x7.50	Tray	-40 to +125°C
RAA2710054R64HBG#HC0	271005 R64 HBG	12A	OTP-17.61	66 Ball BGA, 7.5mm×4.5mm	V66.4.50x7.50	Reel, 3k	-40 to +125°C
RAA2710054R4KHBG#HC0	271005 R4K HBG	12A	OTP-11.61	66 Ball BGA, 7.5mm×4.5mm	V66.4.50x7.50	Reel, 3k	-40 to +125°C
RAA2710054266HBG#HC0	271005 266HBG	12A	OTP-26.69	66 Ball BGA, 7.5mm×4.5mm	V66.4.50x7.50	Reel, 3k	-40 to +125°C
RAA2710054L00HBG#HC0	-	6A	No customized OTP	66 Ball BGA, 7.5mm×4.5mm	V66.4.50x7.50	Reel, 3k	-40 to +125°C
RTKA271005DE0000BU	Comprehensive Evaluation Board						

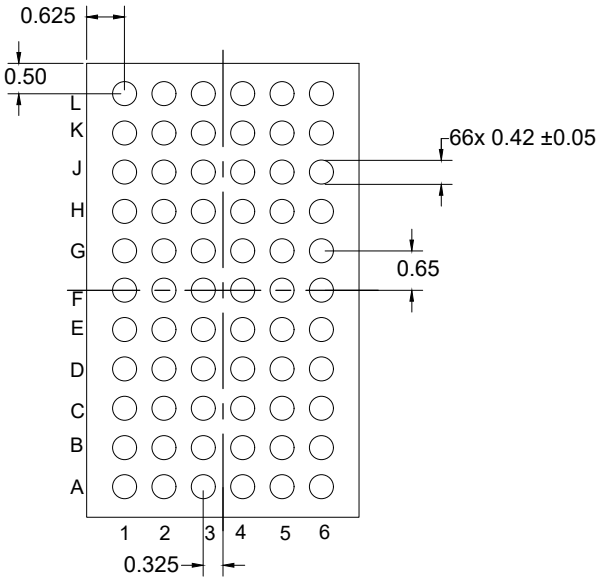
1. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu-e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL) rating, see the RAA271005 product page. For more information about MSL, see TB363.
3. For OTP configuration details, contact Renesas.
4. For the Pb-Free Reflow Profile, see TB493.
5. See TB347 for details about reel specifications.

10. Revision History

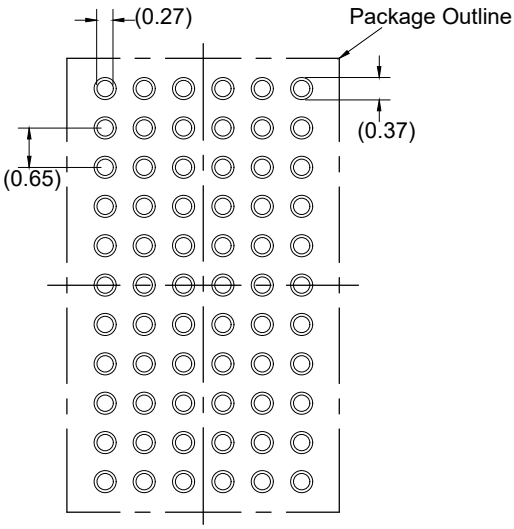
Revision	Date	Description
1.03	Jul 31, 2026	▪ Added RAA271005L part information throughout the document. ▪ Updated Ordering Information table. ▪ Updated Table 8.
1.02	Nov 20, 2025	▪ Added V_{LDOOUT} = 0.6V test condition for Operating Bias Current at LDO_IN5 and LDO_IN6. ▪ Added V_{LDOOUT} = 0.6V to 1.8V row to DC Output Voltage Accuracy spec for LDO5-6. ▪ Added V_{LDOOUT} = 0.6V row to DC Load Regulation spec for LDO5-6. ▪ Updated Register 0x056 - IO_GPIO_DATAOUT. ▪ Updated/Added content under RAA271005 GPIO section. ▪ Updated Buck Regulators Spread Spectrum Operation section. ▪ Updated Table 20. ▪ Updated Register 0x11C - FUSA_CTRL_C (OTP). ▪ Updated Fault Reactions During Cold-Start and Deep Stop section. ▪ Updated Register 0x102 - IO_MODECTRL (OTP). ▪ Removed Registers 0x123 and 0x124. ▪ Updated Ordering Information table.
1.01	May 9, 2025	▪ Updated Features. ▪ Updated Figure 3. ▪ Updated 2.2.1 I/O Pin Configurations. ▪ Updated Table 2. ▪ Electrical Specifications: • Updated Operating Current at AVIN. • Updated R5 CCM Switching Frequency. • Added Fixed Frequency Tolerance. • Updated PCM CCM Switching Frequency. ▪ Updated Figure 11 to match the values of Table 5. ▪ Updated Table 10. ▪ Updated 5.1.3, Buck Dynamic Voltage Scaling. ▪ Updated Table 18. ▪ Updated 5.6.1 Power Grouping. ▪ Updated Table 19. ▪ Updated 5.6.3.2 Full Run to Deep Stop. ▪ Added 5.6.3.6 Comparison Between Deep Stop and Suspend-to-RAMt ▪ Added 5.6.3.7 Suspend-to-RAM Power Rails ▪ Added 5.6.3.8 SW BKUP Power Rails. ▪ Updated 5.9 Regulation Hiccup Feature.
1.00	Jul 26, 2024	Initial release



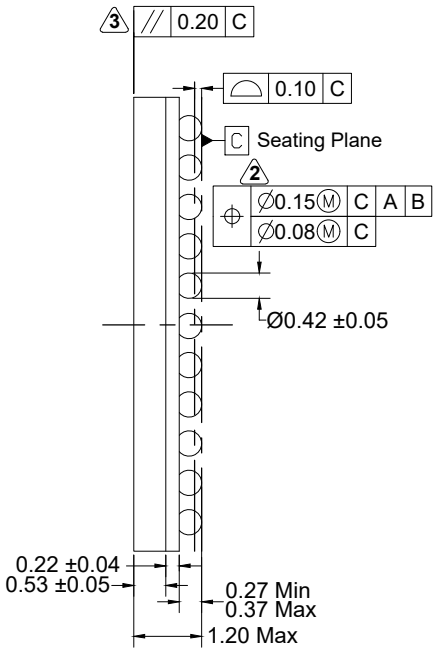
Top View



Bottom View



Typical Recommended Land Pattern



Side View

Notes:

1. All dimensions and tolerances conform to ASME Y14.5 - 2009.
2. Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.
4. Unless otherwise specified, dimensions are in millimeters.

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