RAA223181

900V Off-Line Flyback Regulator

The RAA223181 is an off-line Flyback regulator with a 900V integrated MOSFET, designed for high input voltage and high reliability application of smart meter power supplies and other general isolated power supplies.

The RAA223181 operates in DCM with constant switching frequency at full load. The system is inherently stable with an easy feedback loop design, while switching at constant frequency without interfering the communication of the smart meter. At light load, RAA223181 enters burst mode operation to reduce the IC power consumption, while keeping the burst frequency less than 3kHz to avoid interference to the PLC frequency band.

RAA223181 features a unique short-time heavy load operation mode, which delivers up to 12W output power for a programmed time period. This allows the smart meter power supply to be designed at regular power level without being over-designed for 2x power in the transmission mode, which greatly reduces system cost.

RAA223181 also has a cost-saving feature for the input voltage higher than $265V_{AC}$, where usually two stacked 400v electrolytic capacitors are required after the bridge rectifier. RAA223181 uses only one 400V capacitor. The IC detects the over-voltage and disconnect the input capacitor from the DC bus with a MOSFET and stop switching. This saves the cost on expensive high voltage electrolytic capacitors.

In addition, the RAA223181 adopts valley switching technique to reduce the switching losses to improve thermal performance at high temperature operation. Besides it also features input brown-out protection, output overload, short circuit, VccUV, VccOV, VinUV, peak current limit, primary short, and over-temperature protections.

All these features are integrated in a SO16-13 package.

Features

- Flyback regulator with 900V 10Ω MOSFET
- Single 400V input capacitor for input up to $450V_{AC}$
- Frequency doubling for heavy load operation (up to 12W), with programmable duration <100ms
- Valley switching to reduce switching losses
- Programmable constant frequency DCM operation (recommended range 50kHz ~100kHz)
- Burst mode operation at light load
- Protection features: Short-Circuit Protection (SCP), Overload Protection (OLP), Input Undervoltage Lockout (VinUV), Input OVP, VCC Overvoltage Protection (VccOV), VCC Undervoltage Lockout (VccUV) and Over-Temperature Protection (OTP).

Applications

- Smart Meter
- Large appliances
- Industry control

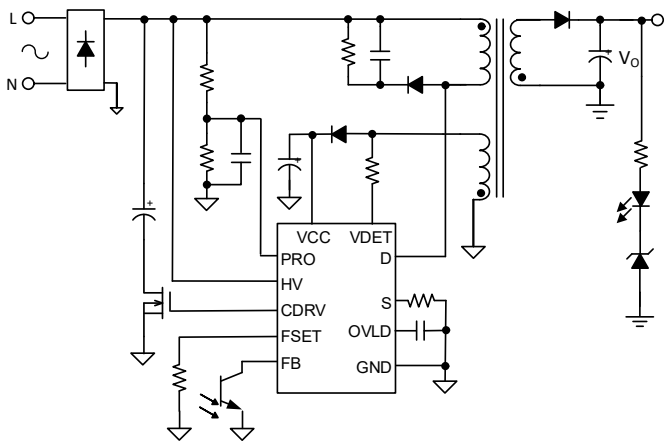

Figure 1. Typical RAA223181 Flyback Circuit

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1. Overview

1.1 Block Diagram

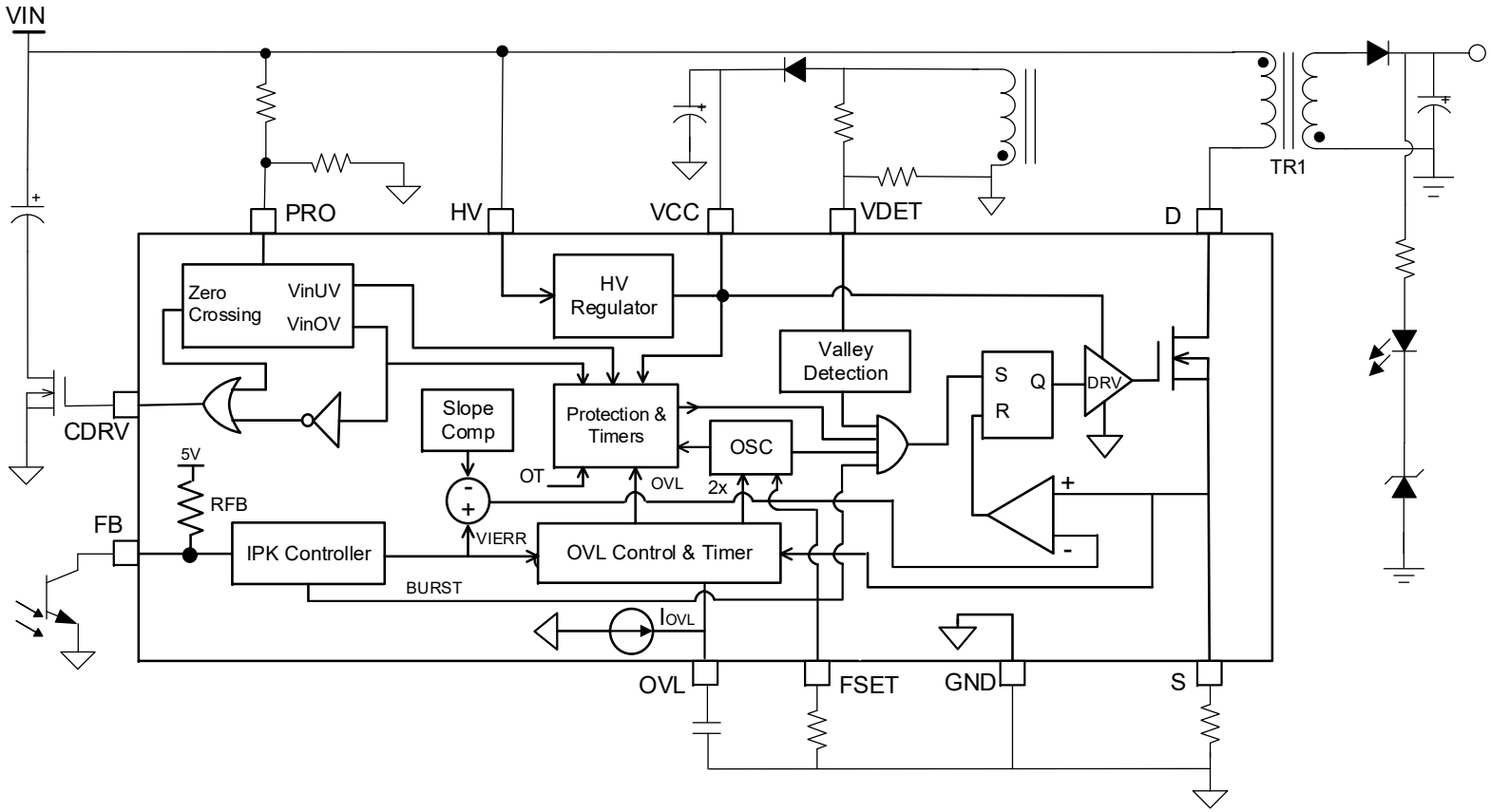
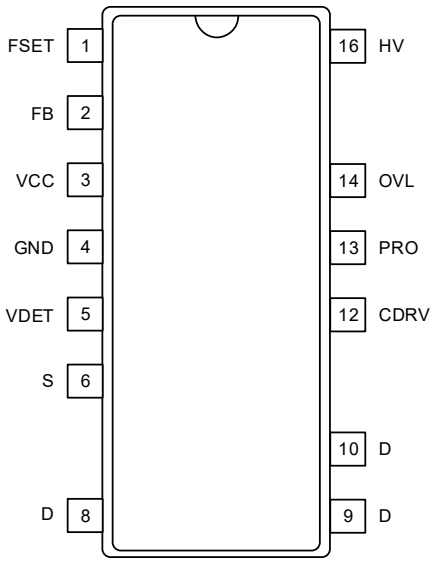


Figure 2. Block Diagram of RAA223181

2. Pin Information

2.1 Pin Configuration



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	FSET	Oscillator frequency set
2	FB	Feedback
3	VCC	IC supply voltage
4	GND	Signal ground
5	VDET	Valley detection
6	S	Source of power FET
8, 9, 10	D	Drain of power FET
12	CDRV	Gate of input capacitor disconnection MOSFET
13	PRO	Bus over-voltage sense
14	OVL	Short-time heavy load programming
16	HV	High voltage startup

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC	-0.3	+30	V
VFB	-0.3	+5	V
VDET	-0.3	+5	
CDRV	-0.3	+30	
PRO	-0.3	+5	
HV	-0.3	+700	V
D (to S)	- 0.3	+900V	V
Continuous Power Dissipation (T_A = +25°C)		1	W
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	1.2		kV
Charged Device Model (Tested per JS-002-2018)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
13 Ld SOIC	27.4	31

1. θ_{JA} is measured on a FR4 2oz PCB with copper size of 165mm^2 on pin 8,9 and 10 at 26C ambient.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-60	+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V_{CC}	10	18	V
Ambient Temperature	-40	+125	°C

3.4 Electrical Specifications

Typical operating conditions at 25°C, V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Startup and Power FET						
Internal V_{CC} Startup Current	I_{VCC_START}	V_{CC} = 8V, V_{DRAIN} = 100V		3.5	8	mA
Drain Leakage Current	I_{D_LEAK}	V_{CC} = 12V, V_D = 375V, V_{FB} = 0V		1	3.5	µA
HV Bias	I_{HV_BIAS}	V_{CC} = 13V, V_{DRAIN} = 375V			5	µA
Power FET Breakdown Voltage	$V_{(BR)DSS}$		900			V
Power FET On-Resistance	$r_{DS(ON)}$	T_J = 25°C, V_{CC} = 12V, I_{DS} = 300mA		10	13	Ω
		T_J = 125°C		22	26	Ω
Power FET Output Capacitance	C_{oss}	V_{DS} = 25V, V_{GS} = 0V		47		pF
V_{CC} Supply						
V_{CC} Start (Rising)/HV Regulator Off	V_{CC_START}	V_{HV} = 100V	11	12	13	V
V_{CC} (Falling) /HV Regulator On	V_{CC_HVON}	V_{HV} = 100V	8	9	10	V
HV regulator On/Off Hysteresis	V_{VCC_HYS}		2	3	4	V
V_{CC} Undervoltage Threshold (Falling)	V_{CC_UVLO}	IC stop switching	5	5.5	6	V
V_{CC} OVP Threshold	V_{CC_OVP}		18	20.6	23.5	V
V_{CC} OV Latch-Off Threshold	V_{CC_OVL}		23.5	26	28.5	V
V_{CC} Quiescent Current	I_{VCC_Q}	V_{FB} = 0.4V, no switching		465	685	µA
V_{CC} Current During Switching	I_{VCC}	V_{FB} > 0.7V, switching frequency = 50kHz, D = 0.48		660	810	µA
Current Sense						
Max Current Sensing Threshold	V_{CS_MAX}	V_{FB} = 4V,	425	500	570	mV
SCP Threshold	V_{CS_SC}			1000		mV
Minimum Current Sensing Threshold	V_{CS_MIN}			75		mV
Leading Edge Blank Time	t_{LEB}		300	350	570	ns
Feedback						
Transconductance	GM	V_{FB} to V_{CS}		0.225		V/V
FB Pin Pull-Up Resistor	R_{FB}		24	35		kΩ
FB Threshold Entering Burst Mode	V_{BURL}		400	500	600	mV
FB Threshold Exiting Burst Mode	V_{BURH}		650	750	850	mV
FB Threshold Into 2x Frequency	V_{FB_2XF}		2.6	3.2	4	V
FB Threshold Out of 2x Frequency	V_{FB_1XF}		2	2.6	3.2	V
FB Threshold for Overload Protection	V_{FB_OLP}		3.6	4	4.8	V
FB Internal Pull-Up Voltage	V_{FB_MAX}		4.4	4.9		V
Programmable Heavy Load						
OVL Pin Source Current	I_{OVL}			10.5	11.8	µA
OVL Pin Discharge Current	I_{OVL_D}		1.8	2		µA

Typical operating conditions at 25°C, V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise specified. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
OVL Pin Threshold	V_{OVL}		3.6	4	4.6	V
Input Undervoltage and Overvoltage Protection						
PRO Pin UV Rising Threshold	V_{BUSUV_R}		0.4	0.5	0.6	V
PRO Pin UV Falling Threshold	V_{BUSUV_F}		0.33	0.4	0.48	V
PRO Pin OV Threshold (Rising)	V_{BUSOV_R}		3.9	4.5	5.2	V
PRO Pin OV Falling Hysteresis	V_{BUSOV_HYS}		0.4	0.5	0.6	V
OV Falling Delay	T_{BUSOV_DL}		1.4	1.6		ms
CDRV Driver Low-Side On-Resistance	R_{DS_L}			17	32	Ω
CDRV Driver Source Current	I_{DRVS}			25		mA
Frequency						
FSET Pin Reference Voltage	V_{FSET}		2.3	2.5	2.7	V
Oscillator Frequency	f_{SW}	R_{FSET} = 187k	42.5	49	55	kHz
Dithering		Percent frequency	-4		4	%
Double Frequency	f_{SW_2x}		86	93	98.5	kHz
Valley Detection						
Ringing frequency		Assured by design	550		1000	kHz
Timing						
Maximum Duty Cycle	D_{MAX}	f_{SW} = 50kHz	42	48	54	%
OVL Blanking	T_{OVL_BLK}	2 Cycles, 50kHz		40		µs
Startup Timer	T_{ST}	4096 cycles, 50kHz		82		ms
Hiccup Restart Delay	T_{HICC}	16384 cycles, 50kHz		328		ms
OLP/OCP Delay Timer	T_{OLP}	2048 cycles, f_{SW} = 100kHz, V_{FB}>4.5V		20.5		ms
VinUV Delay Timer	T_{VINUV}	2048 cycles, f_{SW} = 100kHz		20.5		ms
Thermal						
Over-Temperature Threshold	OTP_{TH}			150		C
Over-Temperature Hysteresis	OTP_{HYS}			30		C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Performance Graphs

4.1 Characterization Curves

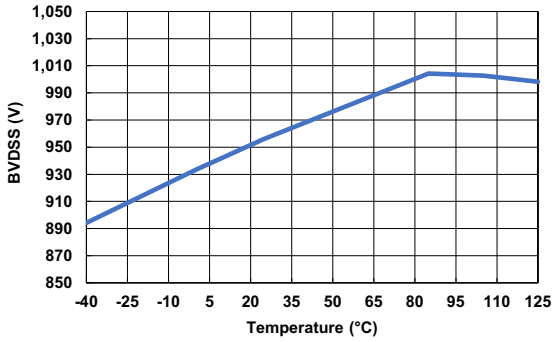


Figure 3. Breakdown Voltage vs Temperature

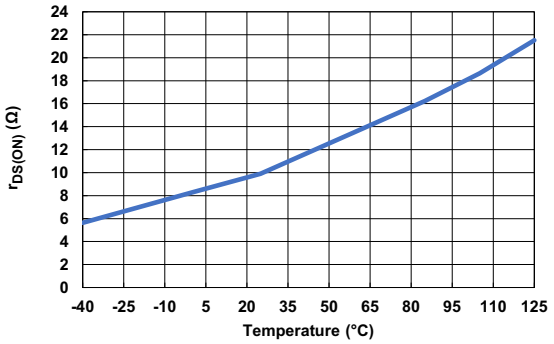


Figure 4. $r_{DS(ON)}$ vs Temperature

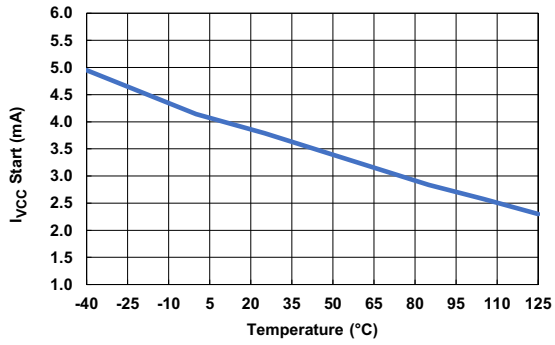


Figure 5. V_{CC} Start Current vs Temperature

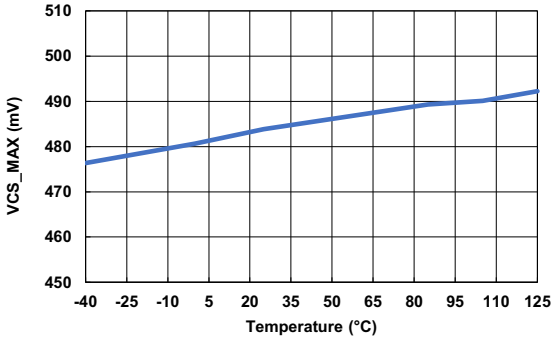


Figure 6. Maximum Current Sensing Threshold vs Temperature

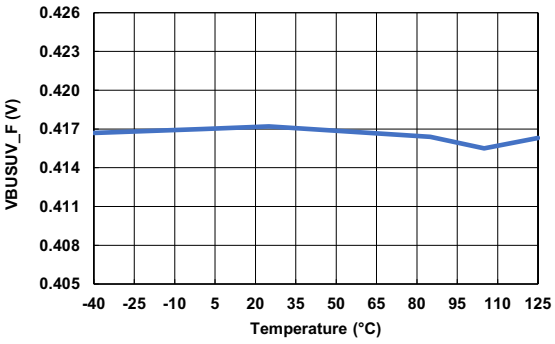


Figure 7. PRO Undervoltage Falling vs Temperature

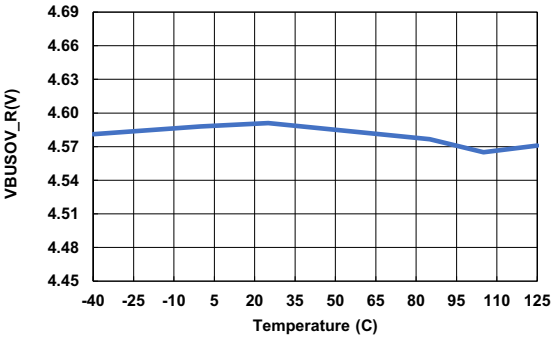


Figure 8. BUS Overvoltage Rising vs Temperature

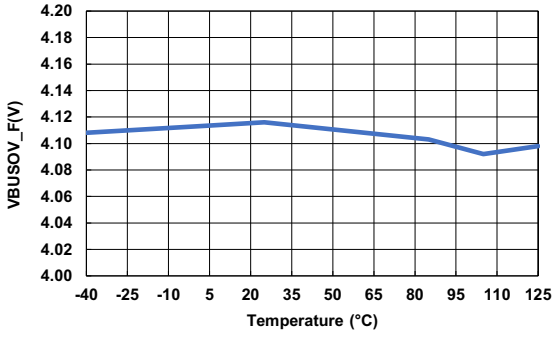


Figure 9. BUS Overvoltage Falling vs Temperature

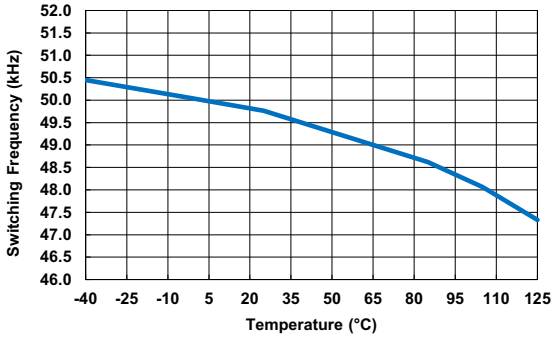


Figure 10. Switching Frequency vs Temperature (R_{FSET} = 187k)

4.2 Typical Waveforms

V_{IN} = 230V_{AC}, V_O = 13V, I_O = 450mA, L_{PRI} = 1.3mH, C_O = 1000uF, T_A = 25C

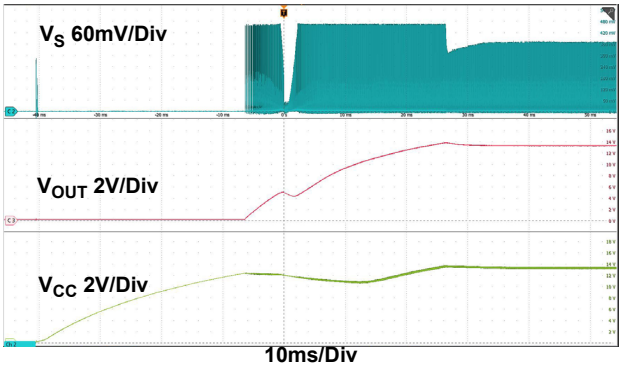


Figure 11. Startup

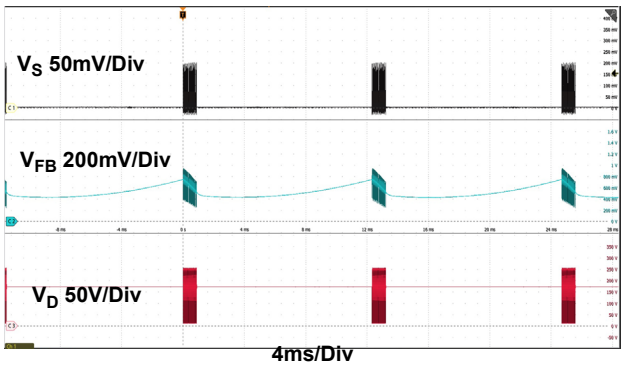


Figure 12. Light Load Operation

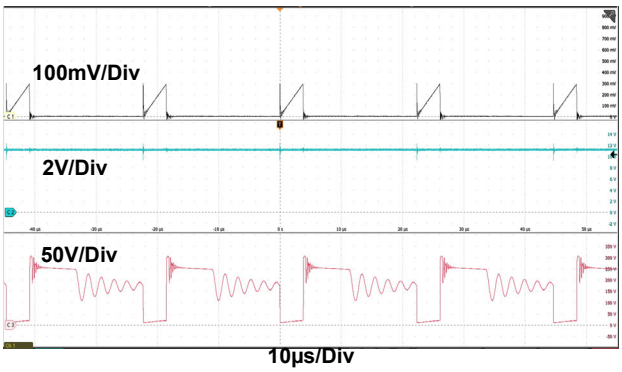


Figure 13. Full Load Operation

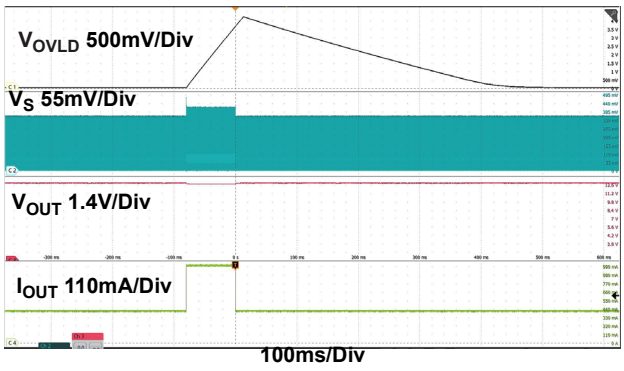


Figure 14. Short-Time Heavy Load Operation

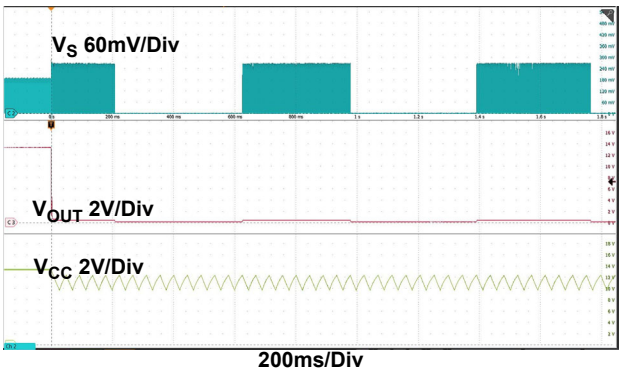


Figure 15. Short-Circuit/Overload Protection

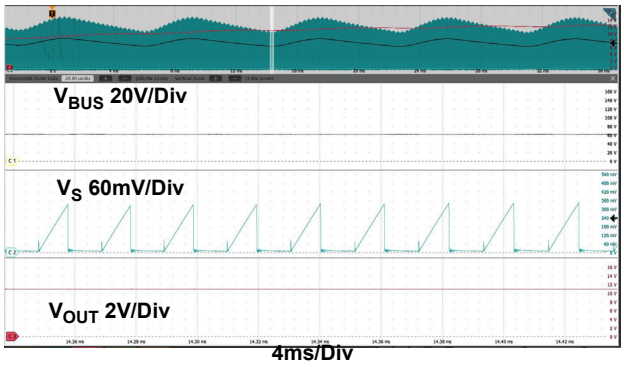


Figure 16. Input Brownout Protection (V_{IN} = 80V_{AC})

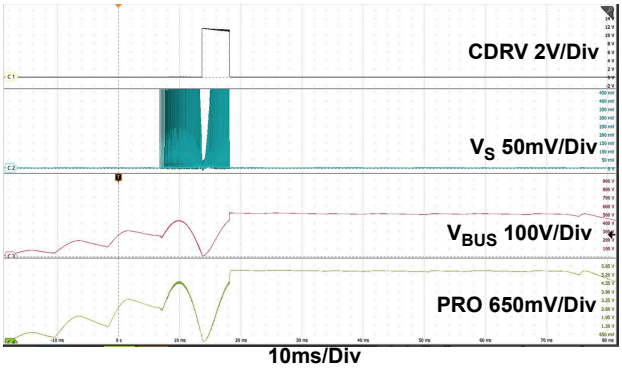


Figure 17. BUS Overvoltage Protection

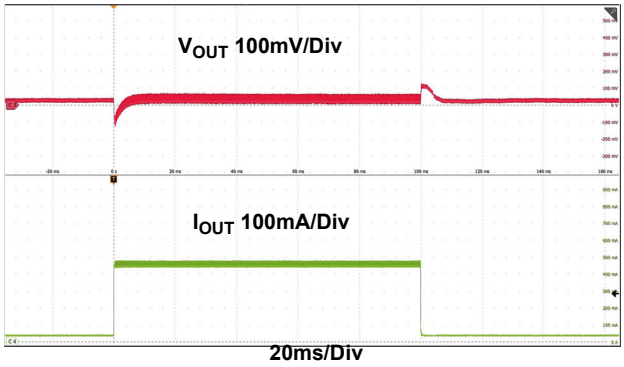


Figure 18. Load Transient (45mA-450mA)

V_{IN} = 230V_{AC}, V_O = 13V, I_O = 450mA, L_{PRI} = 1.3mH, C_O = 1000uF, T_A = 25C

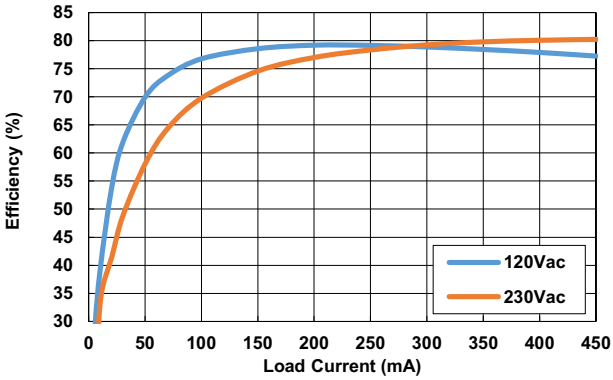


Figure 19. Efficiency

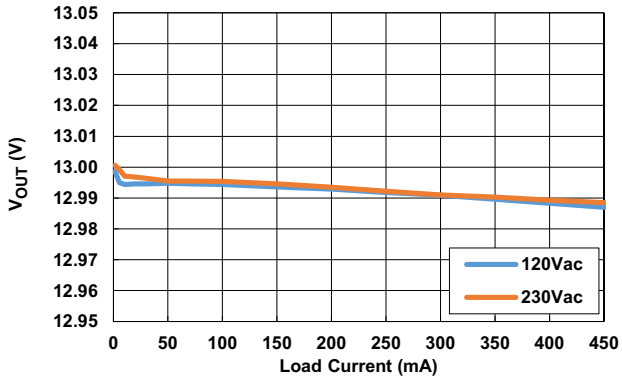


Figure 20. Load Regulation

5. Detailed Description

The RAA223181 adopts constant frequency switching with secondary side regulation as Figure 21 shows. When power is less than 7W, it operates in DCM at the chosen switching frequency. When the power is bigger than 7W, it operates in CCM at the doubled frequency for a programmed time (<100ms). However, the power needs to be less than 12W to avoid over load protection. It uses the valley detection to ensure the DCM and reduce the switching losses.

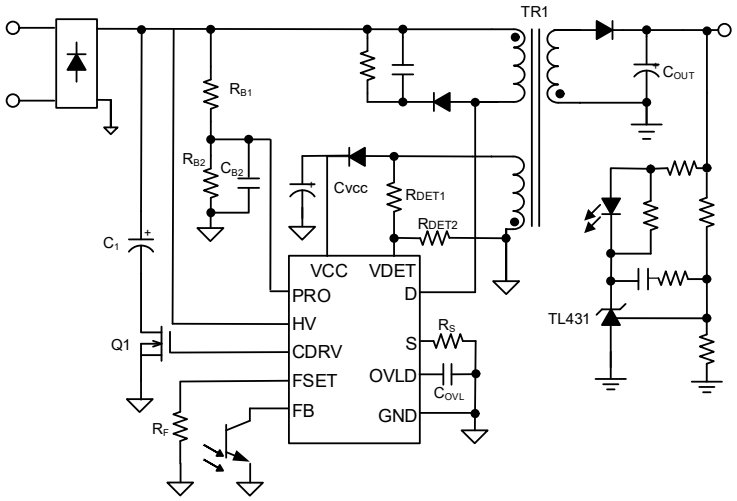


Figure 21. RAA223181 Flyback Application Circuit

Constant frequency PWM mode: In full load, the IC regulates the output voltage with an error amplifier (TL431) through the opto-coupler and peak current control. The feedback pin is the error output opto-coupled from the secondary side. Its voltage level controls peak current in every switching cycle. The turn-on point is set by the internal fixed frequency oscillator and valley detection circuit, which senses the voltage on the auxiliary winding. If the valley is not detected, it waits for the nearest valley to turn on the FET. The valley detection is illustrated in Figure 22. Because the ringing frequency usually ranges from 500kHz to 1MHz, the possible half ringing cycle delay only causes ~5% frequency variation.

Burst Mode: At the light load, the regulator transitions into burst mode operation to save power consumption while keeping switching frequency constant without interfering the communication. The burst frequency is designed to be less than 3kHz, to avoid the minimum frequency of the narrowband PLC communication. During light load, the FB voltage is reduced and when it drops below V_{BURL}, the part enters burst mode operation. The IC stops switching. When FB voltage rises back to V_{BURH}, the IC resumes switching until FB voltage falls back to

V_{BURL}. In Burst mode, the peak current is less than 150mA, effectively avoiding the audible noises. The above operation is illustrated in Figure 23.

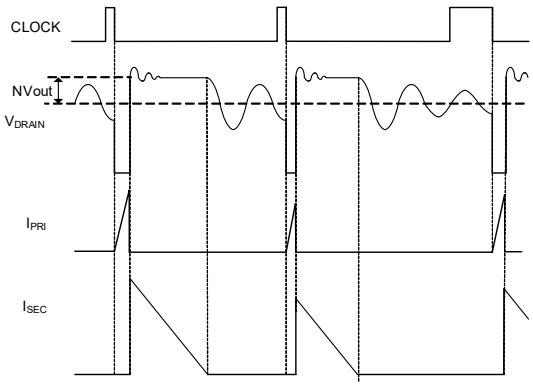


Figure 22. Valley Switching

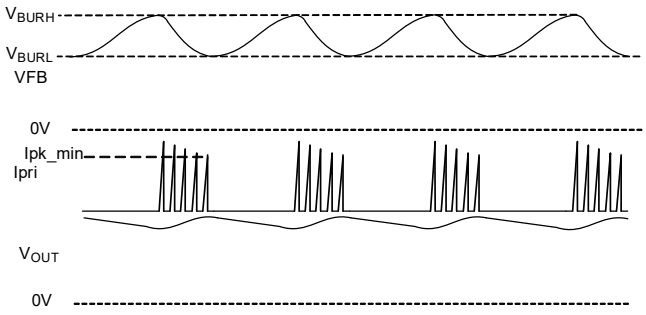


Figure 23. Burst Mode Operation at Light Load

Short-time heavy load operation (OVL): The IC allows a short-time heavy load operation over a programmable time not exceeding 100ms. When $V_{FB} > V_{FB_2XF}$, oscillator frequency is doubled, valley detection is disabled, and the part operates in CCM. At the same time, a programmable timer starts - an internal 10µA current charges the external capacitor on pin OVL. When the OVL pin reaches V_{OVL}, the heavy load operation stops, and the IC waits for 5 times the programmed heavy load operation time before the heavy load operation is allowed again. When $V_{FB} < V_{FB_1XF}$, the part exits heavy load operation even before the heavy load timer expires. If the load is too heavy, FB continues rising to V_{FB_OLP}, the heavy load operation stops, and the overload protection is triggered. The operation is shown in Figure 24.

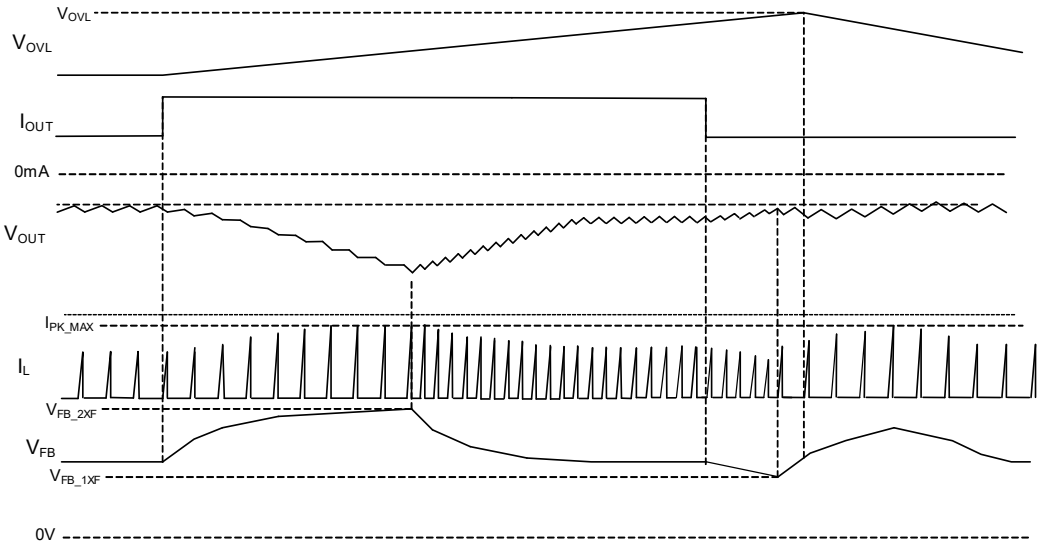


Figure 24. Short-Time Heavy Load Operation

Single capacitor operation for input overvoltage: The IC features a capacitor saving feature by employing an optional external MOSFET driven by the CDRV pin. The FET is connected in series with a 400V input buffer capacitor, as shown in Figure 29. The FET is on in normal operation. When the input has a voltage over the maximum operating voltage, sensed by the PRO pin through a resistor divider, the FET is turned off and disconnected the buffer capacitor from the BUS, protecting the capacitor from by overvoltage damage. When the bus voltage drops low enough, the IC resumes switching. The FET is initially off at the startup, controlled by a low

CDRV, until the bus voltage is pulled down low enough by the switching current, it is turned on with minimum voltage and current stresses. Also, the inrush current is reduced. The operation is illustrated in Figure 25.

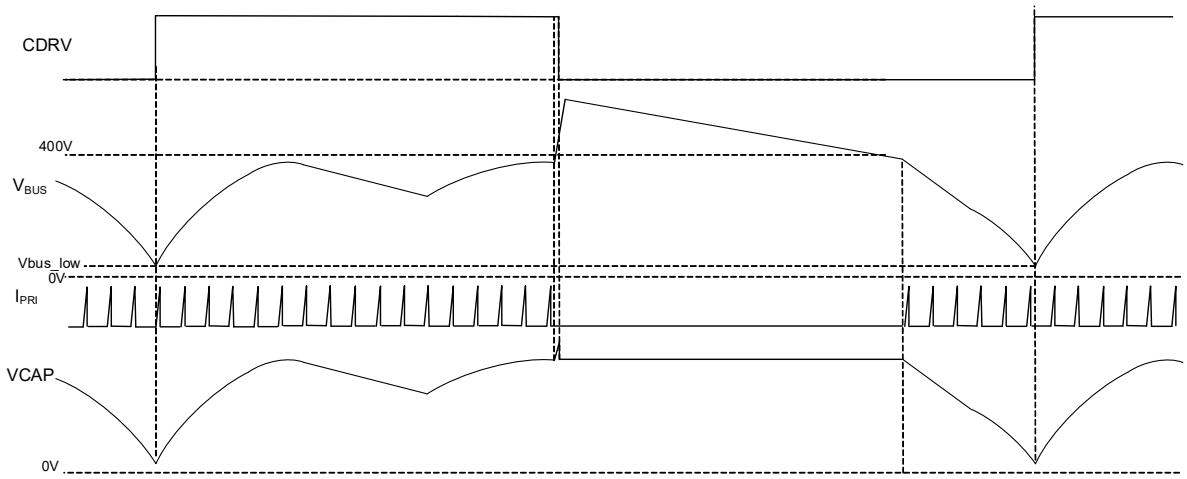


Figure 25. Input Overvoltage Protection and Zero-Voltage Turn-On/Off Buffer Capacitor MOSFET

This feature allows the customer to use only one 400V buffer capacitor and a 650V MOSFET to sustain an input bus overvoltage event up to 650V, which can be caused by a wrong $265V_{AC}$ input phase-to-phase connection, without using two stacked 400V buffer capacitors of twice the capacitance. This saves an expensive 400V capacitor with a cheaper power MOSFET.

5.1 Soft Start-Up

When the input voltage (rectified bus) is higher than 50V or so, the IC starts up with the V_{CC} capacitor being charged by an internal HV current source. When V_{CC} reaches up to V_{CC_START}, the IC begins switching, and a startup timer begins (~82ms). At the same time, the internal HV regulator turns off until V_{CC} drops below 9V then it turns on again. Before the timer expires, the DCM operation with constant max peak current is enforced to ensure a soft start-up. The SCP is disabled during the start-up blanking time. When V_{OUT} is fully established, V_{CC} is supplied by the auxiliary winding, and the internal HV current source is off most of the time in steady-state operation to save power consumption. The startup process is illustrated in Figure 26.

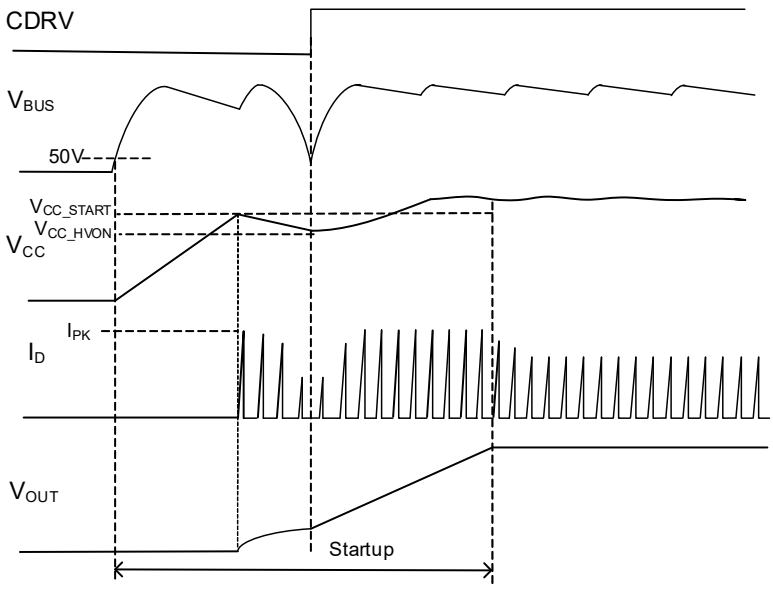


Figure 26. Start-Up Diagram

5.2 Overload and Short-Circuit Protection

If an overload or a short-circuit occurs, V_{FB} rises high. When V_{FB} reaches to V_{FB_2XF}, the heavy load operation is enabled with twice the switching frequency. If V_{FB} continues to rise and reach to another threshold V_{FB_OLP}, and current sense detected above V_{CS_MAX} after a blanking time, a fault delay timer starts. If these thresholds are still reached after the timer expires (~20.5ms), the heavy load operation is disabled, and the IC stops switching for a hiccup time (~328ms). The IC resumes switching after the timer expires. The logic sequence is shown in Figure 27.

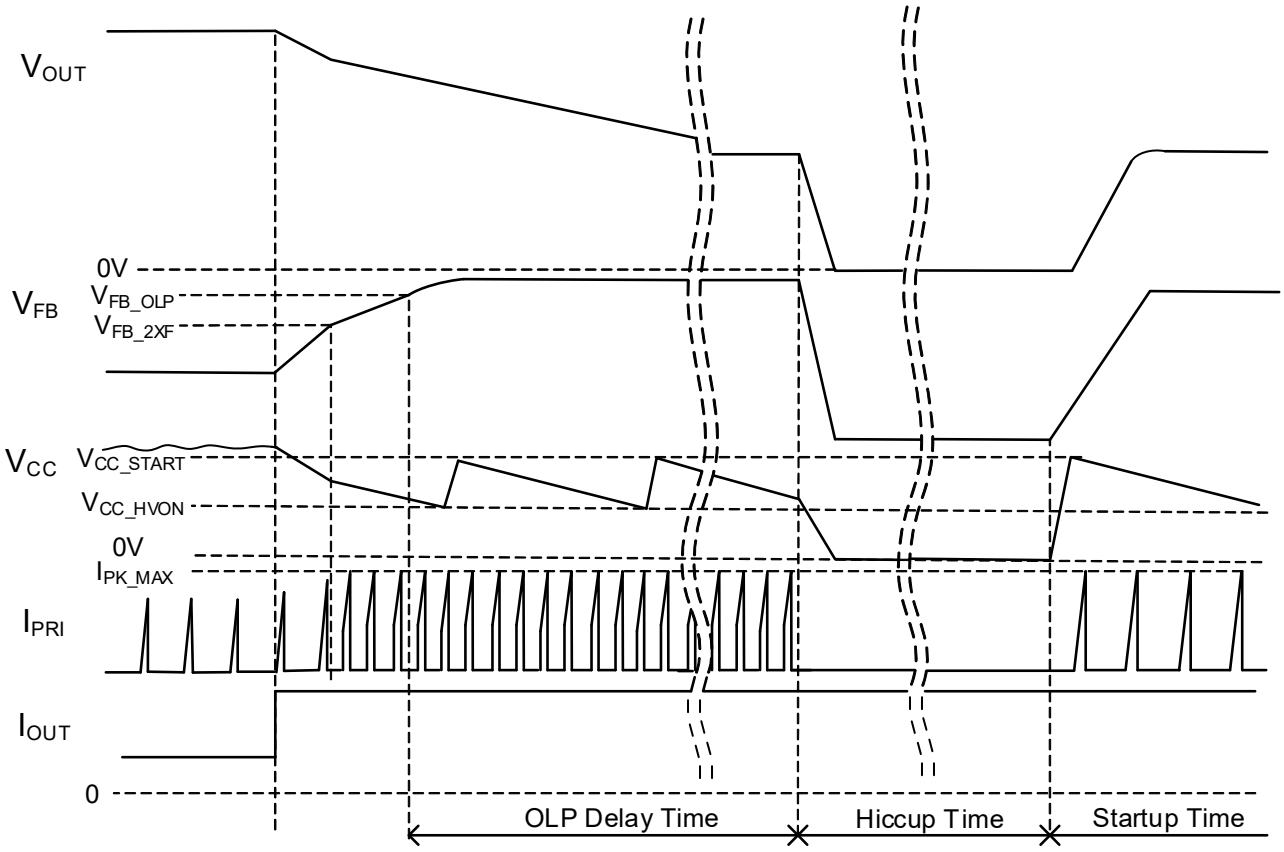


Figure 27. Overload Protection Diagram

6. Application Topologies

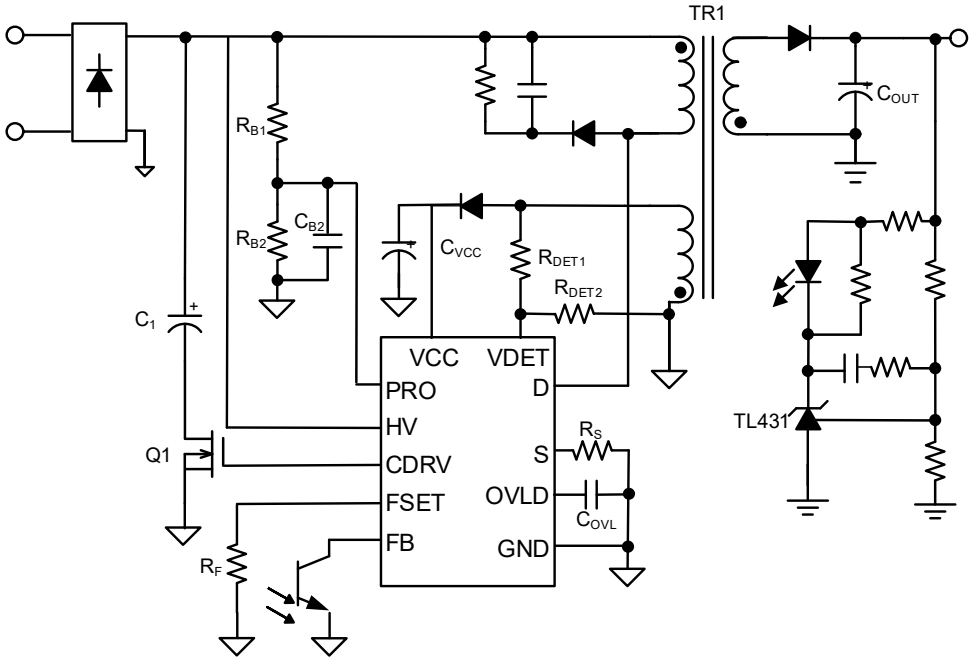


Figure 28. RAA223181 Flyback with BUS Overvoltage Protection

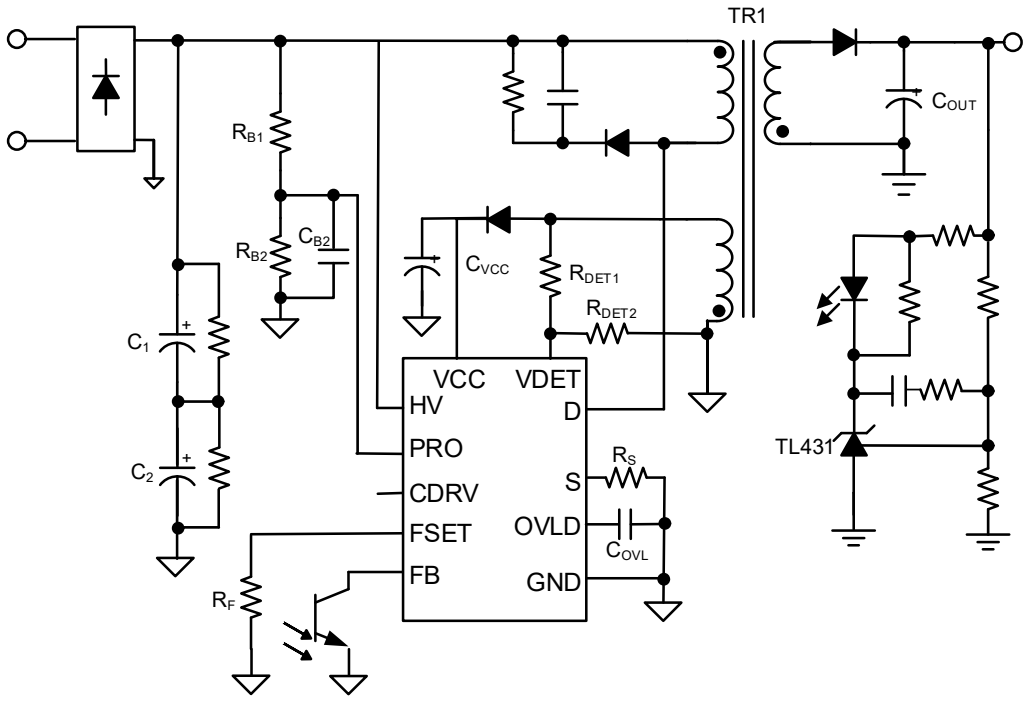


Figure 29. RAA223181 Flyback without the capacitor MOSFET

7. Design Guidance

7.1 Input Buffer Capacitor

The input buffer capacitor provides a DC voltage with less voltage ripple for a given power. For example, how low the bus voltage can drop to determines the power Flyback can deliver. Equation 1 calculates the required minimum bus valley voltage for the target output power, where I_{PKFL} is the peak current required for your full load operation. η is the assumed full load efficiency at $85V_{AC}$.

(EQ. 1) $$V_{valley} = \frac{2P_{OUT}}{\eta I_{PKFL} D_{MAX}}$$

To keep the bus valley above this value, the buffer capacitance needs to be large enough to not only support normal output power but also a short-time heavy load up to 2x normal output power. The required capacitance is then calculated using Equation 2, .

(EQ. 2) $$C_{in} = \frac{2P_{OUT}\left(0.25 + \frac{1}{2\pi}\operatorname{asin}\frac{\sqrt{2}V_{acmin} - V_{valley}}{\sqrt{2}V_{acmin}}\right)}{\eta V_{acmin}(\sqrt{2}V_{acmin} - 40)f_{LINE}}$$

7.2 Transformer Primary Inductance and Turns Ratio

Since the regulator operates in DCM operation, the primary inductance has to be small enough so that the inductor current always resets within a switching cycle while still large enough to deliver enough power at minimum AC input. Accordingly, the required primary inductance is calculated using Equation 3, while Equation 4 specifies its maximum value. To avoid subharmonics in 2x frequency operation at the minimum input voltage, L_P must be smaller than 1.6mH according to the slope compensation.

(EQ. 3) $$L_P \geq \frac{D_{MAX} V_{valley}}{f_{SW} I_{PKFL}}$$

(EQ. 4) $$L_P \leq \frac{D_{MAX} V_{valley}}{f_{SW}(2I_{PKFL} - I_{PKMAX})}$$

Since the bus voltage can be as low as 40V when operating in CCM for short-time heavy load at low input line, the transformer turns ratio needs to be set properly so duty cycle is not too big to maintain the require output voltage. Therefore, the maximum turns ratio is calculated using Equation 5. If D_{max} is chosen as 0.67, and V_{HVMIN} = 40V, N_{max} = 6.25.

(EQ. 5) $$N \leq \frac{V_{HVMIN}}{V_o} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

In the meantime, the turns ratio needs to large enough so that the maximum peak current can fully reset when D_{max} is reached at the valley of the minimum AC input. The minimum turns ratio needs to satisfy Equation 6.

(EQ. 6) $$N \geq \frac{L_P I_{PKFL} f_{SW}}{(1 - D_{MAX})V_O}$$

7.3 Current Sensing Resistor

The peak current is sensed through R_{SENSE} on the S pin and compared with the internal current command. When the sensed voltage reaches the command, the MOSFET is turned off. With the chosen R_{SENSE}, the maximum peak current is limited by an internal current sense voltage limit, V_{CS_MAX}. To have a good regulation without hitting peak current limit, V_{SENSE} should be set around $0.9V_{CS_MAX}$. R_{SENSE} is calculated using Equation 7.

Note: R_{SENSE} must be evaluated for proper power capability.

(EQ. 7) $$R_{SENSE} = \frac{0.9V_{CSMAX}}{I_{PKFL}}$$

7.4 FSET Pin Resistor

The FSET pin resistor sets the switching frequency. The resistor value is calculated using Equation 8.

(EQ. 8) $$R_{FSET} = \frac{3.72V_{FSET}}{f_{SW}} \times 10^{6} (k\Omega)$$

7.5 VDET Pin Resistors

The valley switching is detected at VDET pin by resistor dividers, R_{DET1} and R_{DET2}. R_{DET1} is calculated using Equation 9 and R_{DET2} is calculated using Equation 10. N_{PA} is the turns ratio of primary winding to auxiliary winding, and V_{ACMAX} is the maximum AC input voltage. N_{SA} is the turns ratio of the output winding to the auxiliary winding. V_{DF} is forward voltage of the output diode.

(EQ. 9) $$R_{DET1} \geq \frac{\sqrt{2}V_{ACMAX}}{N_{PA}} (k\Omega)$$

(EQ. 10) $$R_{DET2} < \frac{R_{DET1} \times 5}{\frac{V_{DF} + V_{OUT}}{N_{SA}} - 5}$$

7.6 PRO Pin Resistors

The PRO pin sets the V_{IN} OV threshold and V_{IN} UV threshold. The resistor divider needs to ensure the V_{IN} OV protection at right bus voltage.

(EQ. 11) $$R_{B1} = \frac{V_{BUSOV} - V_{BUSOV_R}}{V_{BUSOV_R}} \bullet R_{B2}$$

V_{BUSOV} is the maximum bus voltage allowed and is usually chosen slightly above the voltage rating of the input capacitor, C1, but below 110% of the rated capacitor voltage if the input capacitor has to be protected by the CDRV feature. To minimize the power dissipation, R_{B2} is usually chosen between 5k-25kΩ. When R_{B1}, R_{B2} are chosen, the V_{IN} UV threshold is set around 50V and 40V for V_{IN} rising and falling, respectively.

7.7 PRO Pin Capacitor

The capacitor at the PRO pin, CB2, helps filter out the noise to ensure normal operation of the IC. It also delays the voltage rise on the PRO pin when an input surge occurs, so it does not trigger OV protection and keeps the bulky capacitor connected to the BUS using the external FET. The capacitance of C_{B2} is calculated using Equation 12, where $V_{PROMAX} = V_{acmax}*\sqrt{2}*R_{B1}/(R_{B1}+R_{B2})$.

(EQ. 12) $$C_{B2} > \frac{30}{\left(\frac{R_{B1} \times R_{B2}}{R_{B1} + R_{B2}}\right) \times \ln\left(1 - \frac{V_{BUSOVR} - V_{PROMAX}}{625 \times R_{B2}/(R_{B1} + R_{B2}) - V_{PROMAX}}\right)^{-1}} (\mu F)$$

7.8 MOSFET in Series with C_1

The MOSFET in series with C_1 is turned off during the input OV; therefore, it needs to have the voltage rating of 650V, so it can sustain a voltage as high as the rectified voltage of $450V_{AC}$ input. Also, it needs to survive lightning events when a surge current passes through. Together with input surge energy absorbing components, the FET needs to have at least 200V at 10A pulse conduction rating, specified by its SOA curve. For details about the input stage design recommendation for surge energy control, see the evaluation board manual.

7.9 OLV Pin Capacitor

The capacitor on the OLV programs the time duration when the short-time over load is allowed, which is recommended not more than 100ms. The capacitor value, C_{OVL}, is calculated using Equation 13. If a much longer time duration is programmed by using a cap bigger than what Equation 13 specifies, or shorting the pin to ground, the heavy load the IC can support may be limited by its thermal capability on a given PCB, especially at low AC input and high ambient temperature. If heavy load support is not required, the OVL pin can be floated. Therefore, the IC always operates with the constant frequency set by R_{FSET}.

(EQ. 13) $$C_{OLV} \leq \frac{I_{OVL}}{10V_{OVL}}$$

7.10 Output Capacitance

The minimum output capacitance is chosen by consideration of switching ripple, step load response, and in some applications, the required output hold-time when input is cut off.

7.11 PCB Layout Guidance

Proper layout is important to ensure a stable operation, good thermal behavior, EMI performance, and reliable operation for various operating environments. Pay attention to the following layout recommendations.

- Leave proper spacing (recommend minimum 2mm) between high voltage (maximum 900V) traces and low voltage traces
- Keep a small loop from the input filter capacitor to IC, transformer primary winding, and to the ground of input capacitor, and a small loop consisted of transformer secondary winding, output capacitor, and output diode.
- Keep enough copper area on the IC drain pin (not less than $165mm^2$ for 6W output power) for better thermal performance.
- Place the V_{CC} decoupling capacitor close to the VCC pin.

The PCB layout example is shown in Figure 30 and Figure 31.

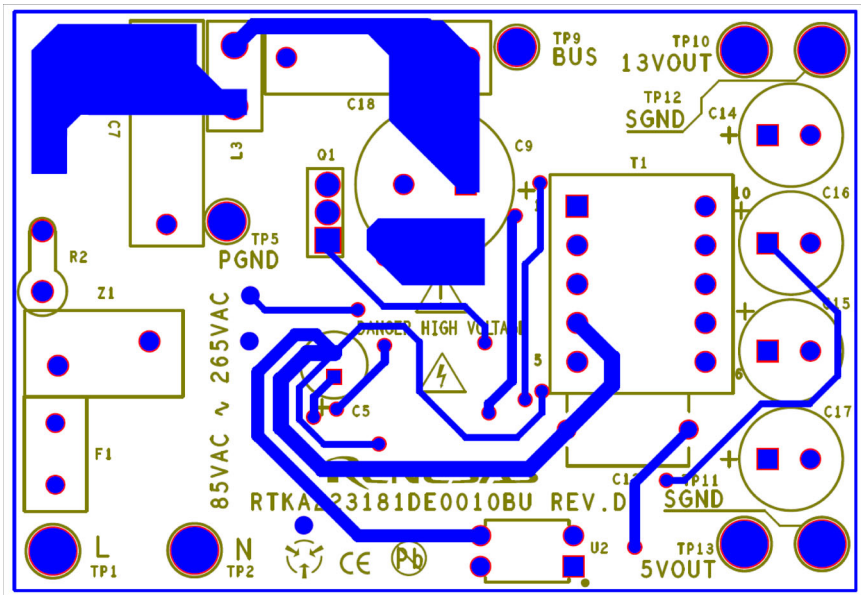


Figure 30. PCB Top Layer

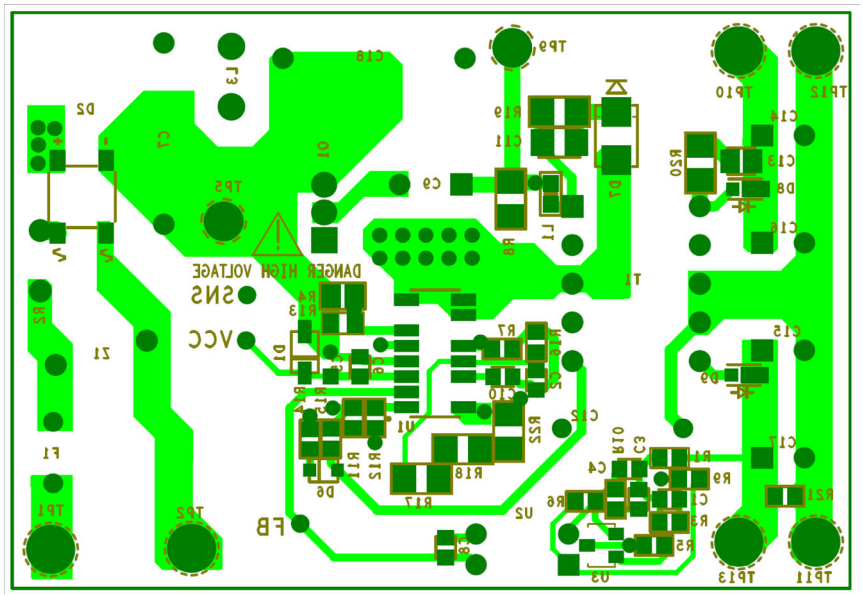


Figure 31. PCB Bottom Layer

8. EMI Performance

Conducted EMI pre-compliance for EN55022/CISPR22 (V_{OUT} = 13V, I_{OUT} = 450mA)

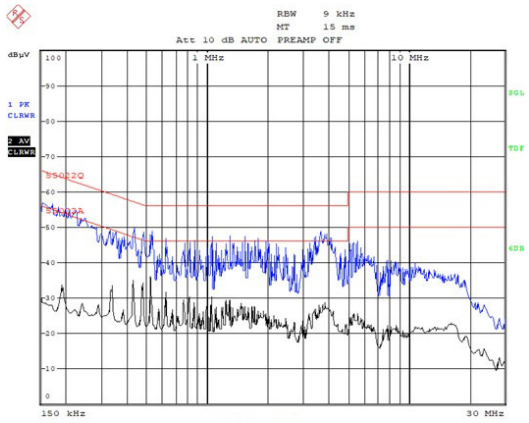


Figure 32. Line, 120V_{AC}

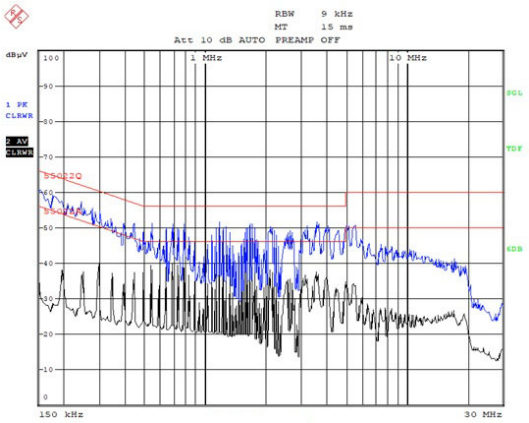


Figure 33. Line, 230V_{AC}

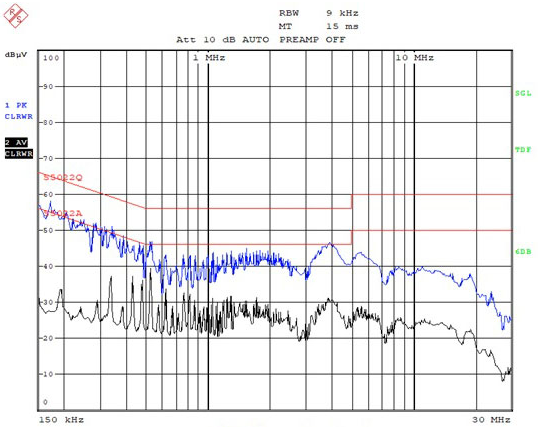


Figure 34. Neutral, 120V_{AC}

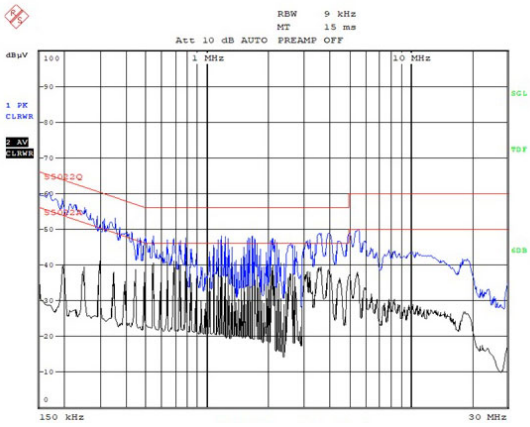
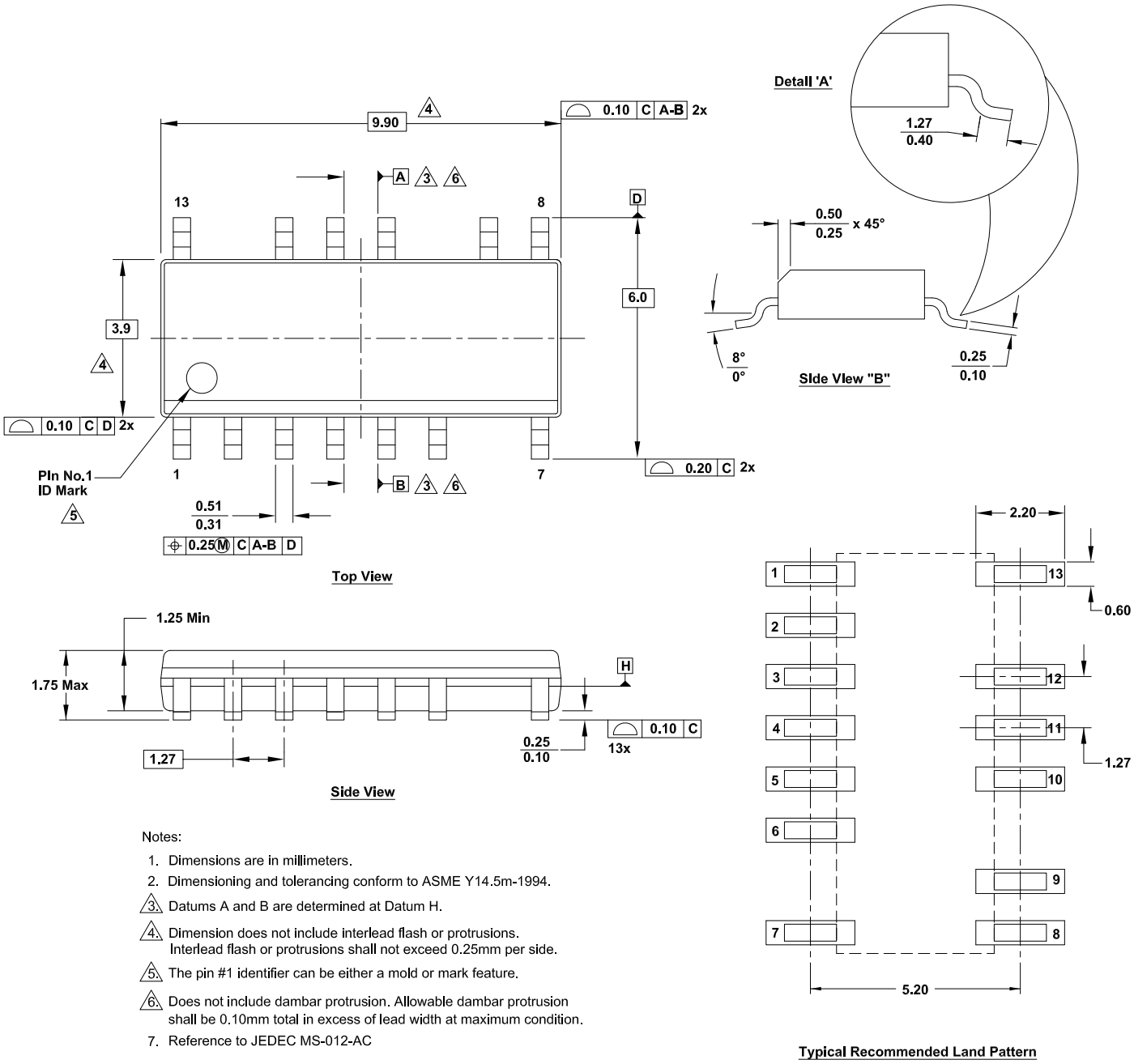


Figure 35. Neutral, 230V_{AC}

9. Package Outline Drawing

For the most recent package outline drawing, see M13.15.

M13.15
13 Lead Narrow Body Small Outline Plastic Package
Rev 0, 6/20



Notes:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA2231814GSP#HA0	223181	13 Ld SOIC	M13.15	Reel, 2.5k	-40 to +150°C
RAA2231814GSP#MA0				Reel, 250	
RTKA223181DE0010BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL), see the RAA223181 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

11. Revision History

Rev.	Date	Description
1.00	Oct 13, 2021	Initial release

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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