RAA214290

1A 20V Wide Input Voltage Range LDO Linear Regulator

The RAA214290 is a linear voltage regulator that operates from 2.5V to 20V and provides up to 1A of output current with a typical dropout of 540mV. The output voltage is adjustable with external feedback resistors anywhere from 1.224V to 18V.

The ground current is typically 80µA at no load and drops to 3µA when in shutdown, making it great for battery-powered and USB devices.

The device features excellent line and load regulation, input UVLO with hysteresis, enable control, short-circuit current limit with foldback, and over-temperature shutdown protection with hysteresis.

The device is stable with a minimum 2.2µF output capacitor and is available in an 8-Ld 3mm×3mm DFN or 8-Ld SOIC package.

Features

- Wide Input Voltage Range: 2.5V to 20V
- Max Output Current: 1A
- Dropout Voltage: 540mV typical at 1A
- Low Ground Current
- Output Voltage Adjustable: 1.224V to 18V
- Excellent Line and Load Regulation
- Stable with an output capacitor as low as 2.2µF
- Short-Circuit Current Limit with fold-back
- Over-Temperature Shutdown Protection
- 8-Ld DFN (3mm×3mm) and SOIC package

Applications

- Battery-Powered Equipment
- MCU Power Supply
- Electric Meters
- USB Devices
- Laptop Computers and Tablets
- Portable Modules and Appliances

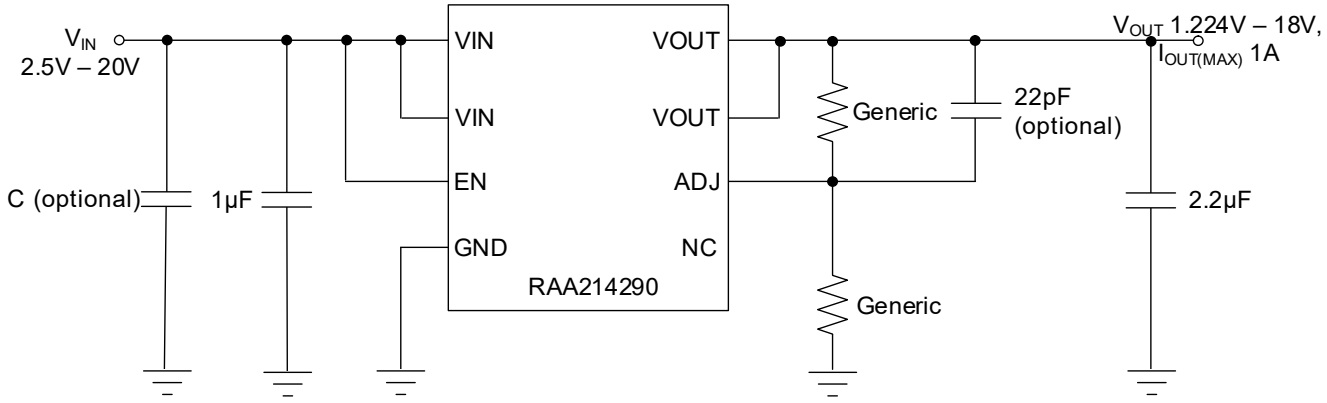


Figure 1. Typical Application Circuit

Contents

1. Overview

1.1 Block Diagram

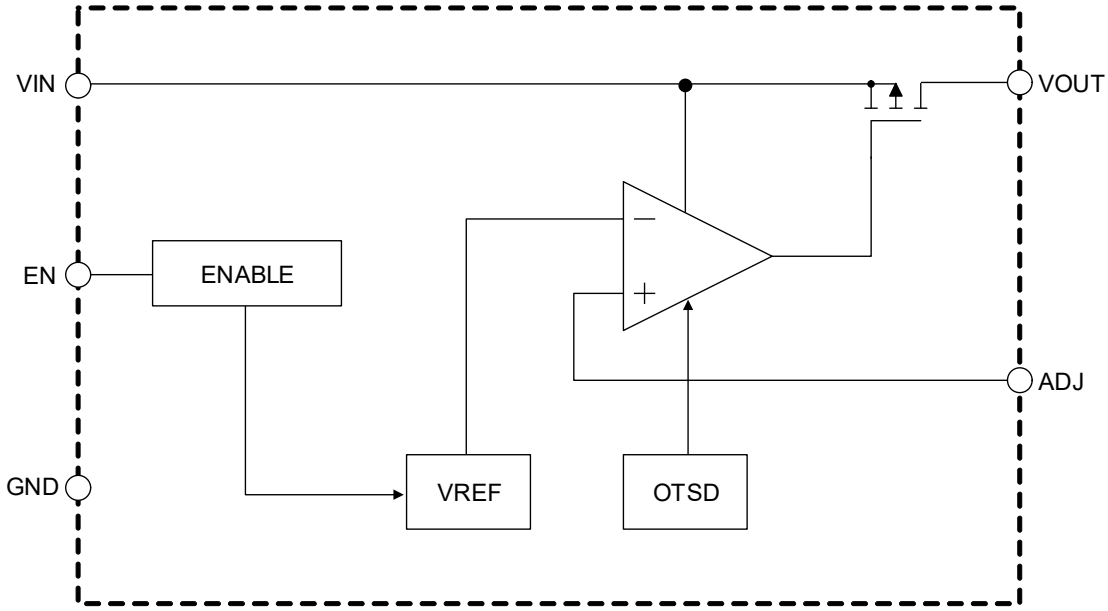
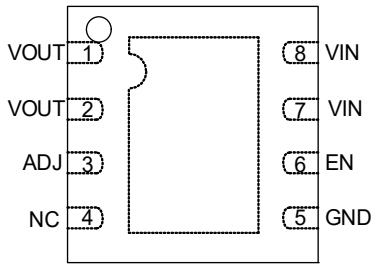


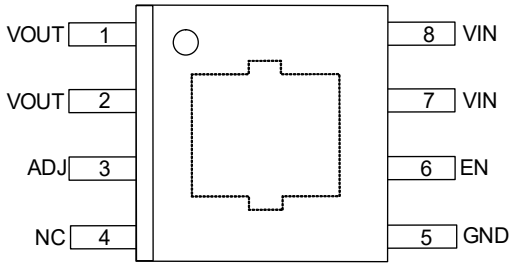
Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



3mm×3mm DFN - Top View



SOIC - Top View

2.2 Pin Descriptions

Pin Name	Pin Number	Description
VOUT	1,2	VOUT are the regulated output voltage pins that supply power to the load. For stable operation across the full temperature range, input range, output range, and load extremes, a minimum 2.2µF X5R/X7R output capacitor is required between this pin and GND.
ADJ	3	ADJ is the adjustable pin. The ADJ pin is internally set to 1.224V using the band-gap circuitry. The external voltage divider formed around this pin sets the LDO output voltage. When the pin is shorted to VOUT, the output voltage is set to a minimum of 1.224V. See Adjusting the Output Voltage for more information on setting the output voltage.
GND	5	GND is the ground pin. This pin must be tied to GND.
EN	6	EN is the ENABLE input. Setting this pin LOW turns OFF the LDO, and setting it HIGH turns ON the LDO. ***IMPORTANT:*** This pin should not be left floating. Instead, tie it to the VIN pins for automatic enabling.
VIN	7,8	VIN are the input voltage pins that supply power to the LDO. Renesas recommends a 10µF and 1µF input capacitor from this pin to GND. Place the 1uF as close as possible to the VIN pins.
EPAD		EPAD is the exposed pad on the bottom of the package. To ensure proper electrical and thermal performance, solder the exposed pad to the PCB ground plane and tie it directly to the ground Pin 5. See Layout Guidelines for more layout guidelines for this pin.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, VIN	-0.3	+22	V
Enable Input Voltage, EN	-0.3	+22	V
Output Voltage, VOUT	-0.3	+22	V
Adjustable Pin Voltage, ADJ	-0.3	+6	V
Output Current, IOUT	-	1	A
Maximum Junction Temperature	-40	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. All voltages referenced to VSS unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, V_{IN}	+2.5	+20	V
Enable Input Voltage, EN	0	+20	V
Output Voltage, V_{OUT}	0	+18	V
Adjustable Pin Voltage, ADJ	0	+5	V
Output Current, I_{OUT}	0	1	A
Output Capacitor, C_{OUT}	2.2	68	µF
Junction Temperature	-40	+125	°C

1. All voltages referenced to VSS unless otherwise specified.

3.3 Thermal Specifications

Parameter[1]	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld SOICEP	θ_{JA}[2]	Junction to ambient	54	°C/W
		θ_{JC}[3]	Junction to case	13	
	8 Ld DFN3×3	θ_{JA}[2]	Junction to ambient	56	
		θ_{JC}[3]	Junction to case	14	

1. Specified at published junction to ambient thermal resistance for a junction temperature of +150°C. See [3] for test condition to establish junction to ambient thermal resistance.
2. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

I_{OUT} = 1mA, C_{OUT} = 2.2µF, C_{IN} = 10µF, V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, V_{EN} = 5V unless otherwise specified. Typical values are at T_A = 25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C**.

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage	V_{OUT}	-	**1.2**	-	**18**	V
Input Voltage	V_{IN}	-	**2.5**	-	**20**	V
Reference Voltage Accuracy	V_{REF}	V_{IN} = 2.5V to 20V, T = 25°C	-1.7	-	+1.7	%
		T = -40°C to 125°C	**-2.0**	-	**+2.0**	
Reference Voltage	V_{REF}	-	-	1.224	-	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{OUT}+1V to 20V, I_{OUT} = 1mA	-	0.02	**0.05**	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 5V, I_{OUT} = 100µA to 1A	-	0.0033	-	%/mA
Dropout Voltage [2]	V_{DO}	I_{OUT} = 10mA, V_{OUT} = 3.3V	-	4.5	-	mV
		I_{OUT} = 50mA, V_{OUT} = 3.3V	-	22	-	
		I_{OUT} = 1A, V_{OUT} = 3.3V	-	540	**1150**	
Shutdown Current	I_{SHDN}	V_{EN} = 0, V_{IN} = 2.5V	-	3	-	µA
		V_{EN} = 0, V_{IN} = 20V	-	7	**13**	
Ground Current	I_{GND}	I_{OUT} = 0mA, V_{IN} = 2.5V, V_{EN} = 5V	-	80	-	µA
		I_{OUT} = 10mA, V_{IN} = 2.5V, V_{EN} = 5V	-	112	-	
		I_{OUT} = 500mA, V_{IN} = 2.5V, V_{EN} = 5V	-	170	-	
		I_{OUT} = 1000mA, V_{IN} = 2.5V, V_{EN} = 5V	-	212	-	
Power Supply Rejection Ratio	PSRR	FREQ = 100Hz, I_{OUT} = 50mA, V_{IN} = 6V, V_{OUT} = 5V	-	95	-	dB
		FREQ = 10kHz, I_{OUT} = 50mA, V_{IN} = 6V, V_{OUT} = 5V	-	70	-	
Output Voltage Noise	-	BW = 10Hz to 100kHz I_{OUT} = 10mA, C_{OUT} = 10µF	-	173	-	μV_{RMS}
EN Rising Threshold	-	-	**1.35**	1.5	**1.65**	V
EN Hysteresis	-	-	**125**	190	**245**	mV

I_{OUT} = 1mA, C_{OUT} = 2.2µF, C_{IN} = 10µF, V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, V_{EN} = 5V unless otherwise specified. Typical values are at T_A = 25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C**. (Cont.)

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
EN Leakage Current	-	V_{EN} = 20V	-	1	-	uA
VIN UVLO Rising Threshold	-	-	-	2.1	-	V
VIN UVLO Hysteresis	-	-	-	200	-	mV
Short-Circuit Current Limit	-	No Foldback	-	1250	-	mA
		With Foldback, V_{IN}-V_{OUT} = 18V	-	430	-	
Short-Circuit Current Foldback Threshold	-	V_{IN}-V_{OUT}	-	8	-	V
Thermal Shutdown	-	-	-	150	-	°C
Hysteresis	-	-	-	20	-	°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Dropout voltage is the input-to-output voltage difference at which the ouptut voltage is 100mV below its normal value.

4. Typical Performance Graphs

4.1 Load Transient

C_{IN} = 10µF, unless otherwise stated.

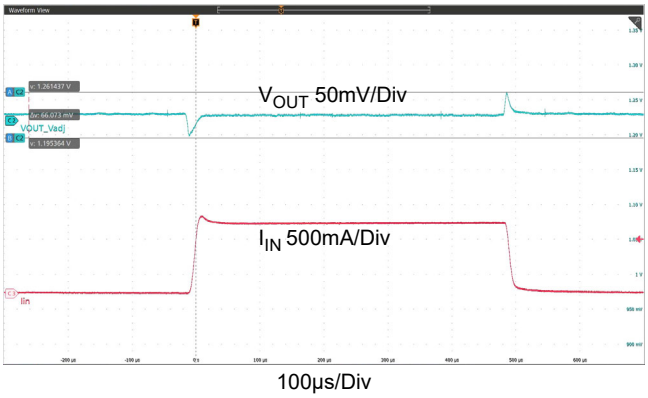


Figure 3. Load Transient Response for 25°C (V_{IN} = 2.5V, V_{OUT} = Adj., C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1mA to 1A to 1mA at 100mA/µs

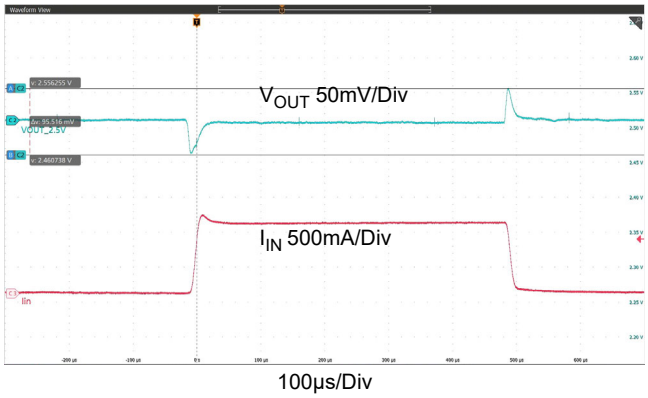


Figure 4. Load Transient Response for 25°C (V_{IN} = 3.5V, V_{OUT} = 2.5V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1mA to 1A to 1mA at 100mA/µs

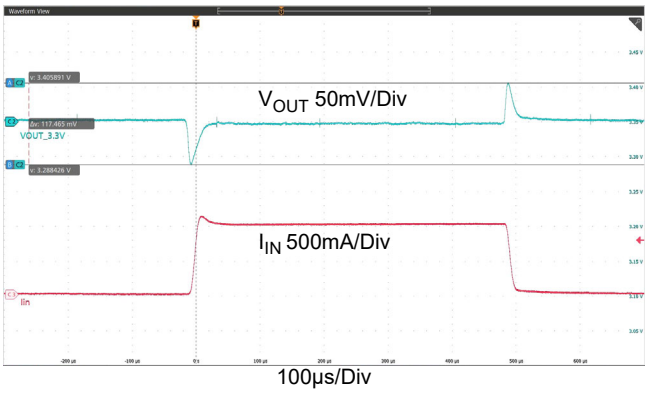


Figure 5. Load Transient Response for 25°C (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1mA to 1A to 1mA at 100mA/µs

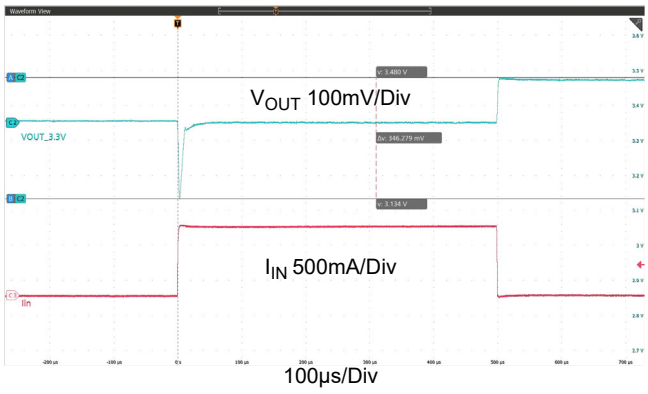


Figure 6. Load Transient Response for 25°C (V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1mA to 1A to 1mA at 1A/µs

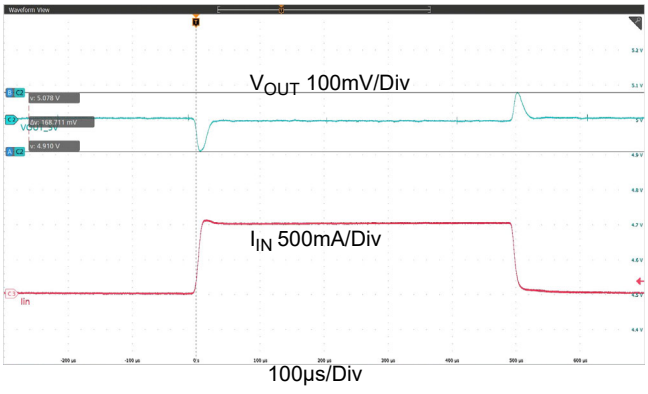


Figure 7. Load Transient Response for 25°C (V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1mA to 1A to 1mA at 100mA/µs

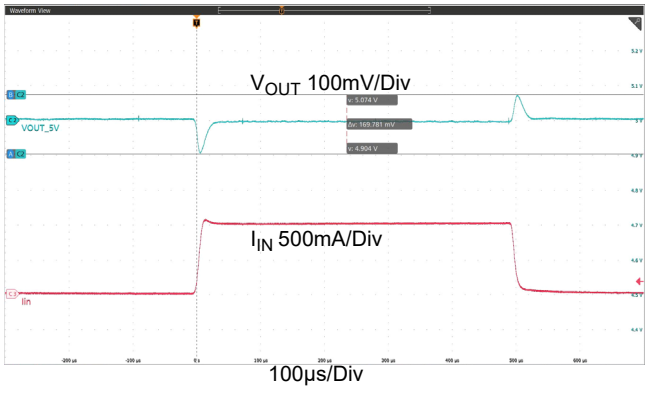


Figure 8. Load Transient Response for 25°C (V_{IN} = 7V, V_{OUT} = 5V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1mA to 1A to 1mA at 100mA/µs

4.2 Line Transient

C_{IN} = 1µF, unless otherwise stated.

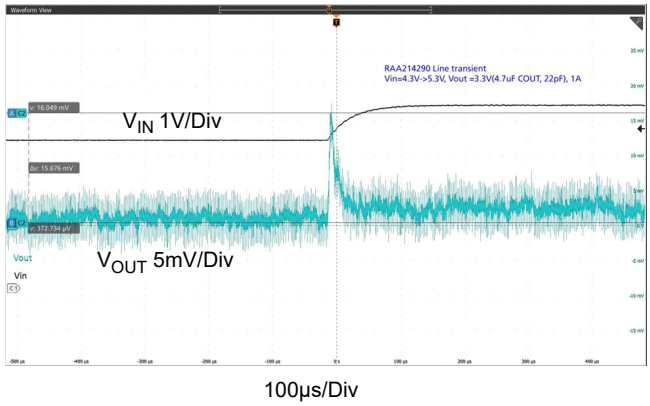


Figure 9. Line Transient Response (ΔV_{IN} = 4.3V to 5.3V at 1V/100µs, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{FF} = 22pF, C_{OUT} = 4.7µF)

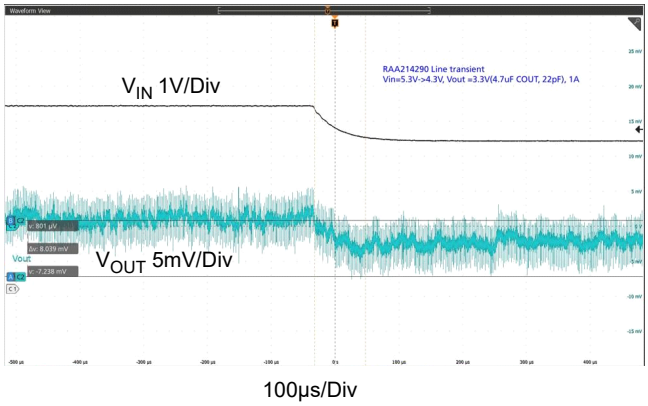


Figure 10. Line Transient Response (ΔV_{IN} = 5.3V to 4.3V at 1V/100µs, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{FF} = 22pF, C_{OUT} = 4.7µF)

4.3 Dropout Voltage

C_{IN} = 10µF, unless otherwise stated.

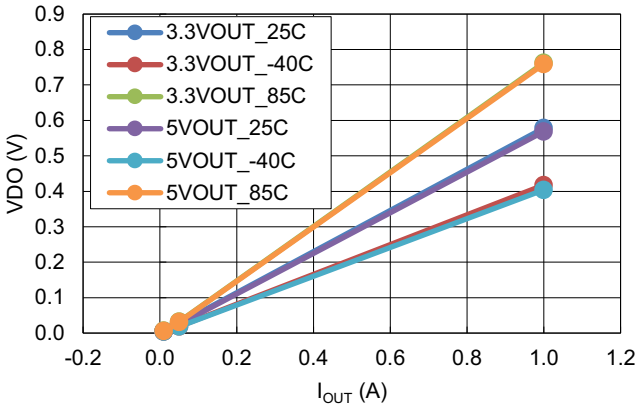


Figure 11. Dropout Voltage vs Output Current for Various Ambient Temperatures (V_{OUT} = 3.3V and 5V) DFN Package

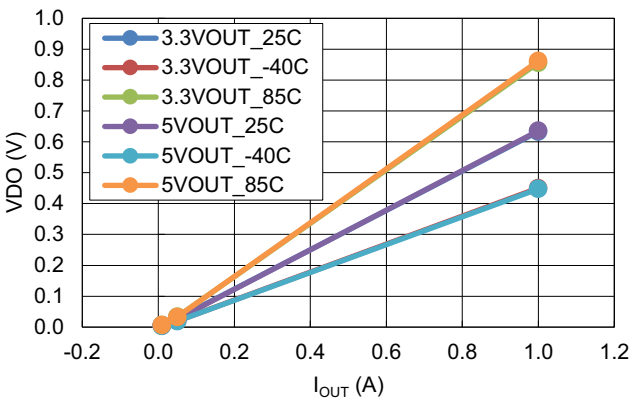


Figure 12. Dropout Voltage vs Output Current for Various Ambient Temperatures (V_{OUT} = 3.3V and 5V) SOIC Package

4.4 Startup

C_{IN} = 10µF, unless otherwise stated.

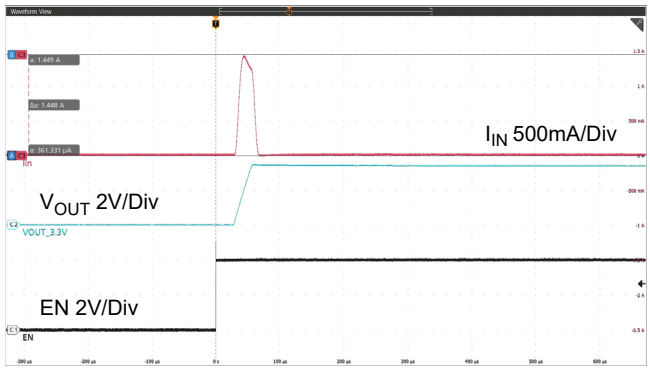


Figure 13. Startup and In-Rush Current for 25°C (V_{IN} = 4.4V, V_{OUT} = 3.3V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 0A)

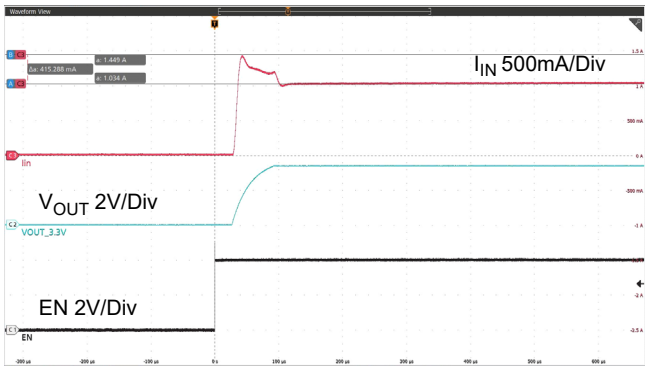


Figure 14. Startup and In-Rush Current for 25°C (V_{IN} = 4.4V, V_{OUT} = 3.3V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1A)

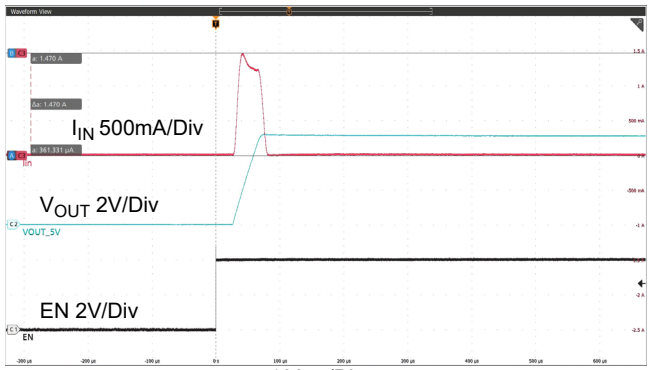


Figure 15. Startup and In-Rush Current for 25°C (V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 0A)

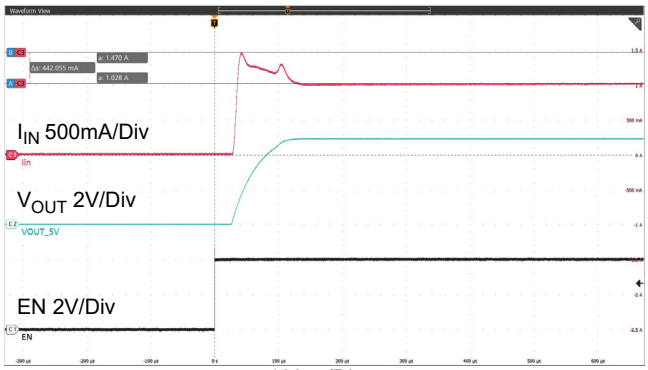


Figure 16. Startup and In-Rush Current for 25°C (V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 10µF, C_{FF} = 22pF, I_{OUT} = 1A)

4.5 General Performance

C_{IN} = 10µF, unless otherwise stated.

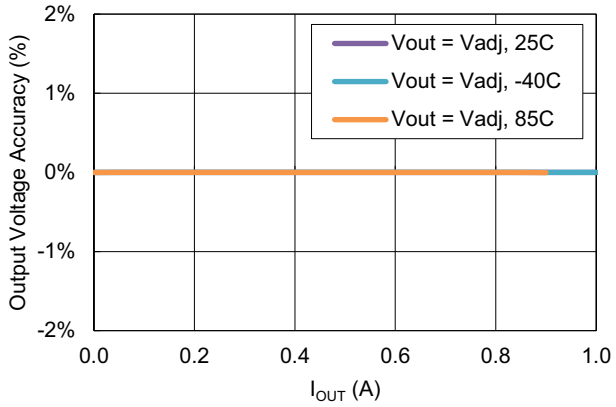


Figure 17. Output Voltage vs Output Current for Various Ambient Temperatures (V_{IN} = 2.5V, V_{OUT} = V_{ADJ})

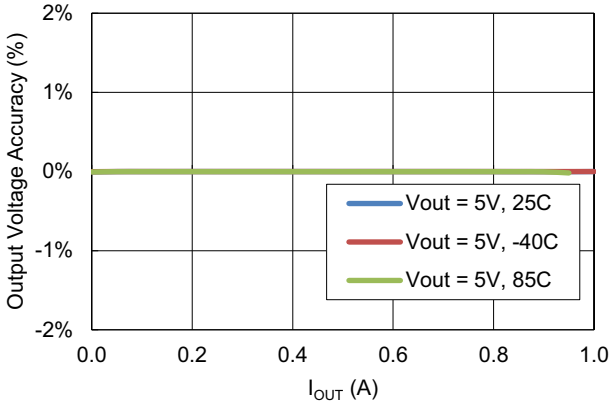


Figure 18. Output Voltage vs Output Current for Various Ambient Temperatures (V_{IN} = 6V, V_{OUT} = 5)

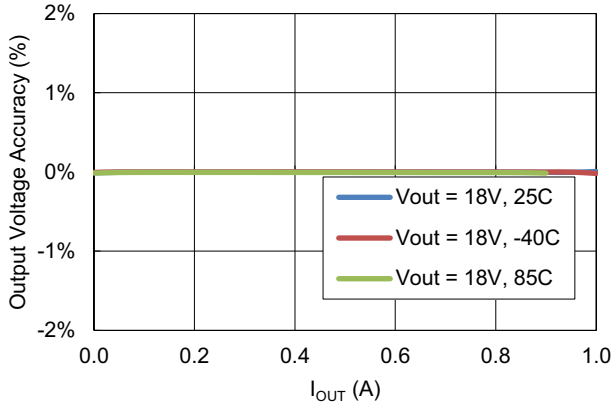


Figure 19. Output Voltage vs Output Current for Various Ambient Temperatures (V_{IN} = 18.7V, V_{OUT} = 18V)

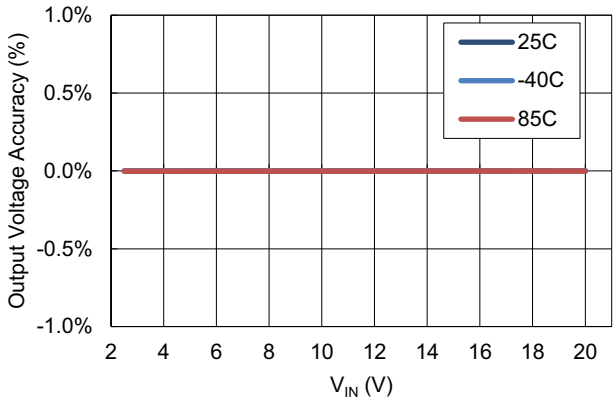


Figure 20. Output Voltage vs Input Voltage for Various Ambient Temperatures (V_{OUT} = V_{ADJ}, I_{OUT} = 1mA)

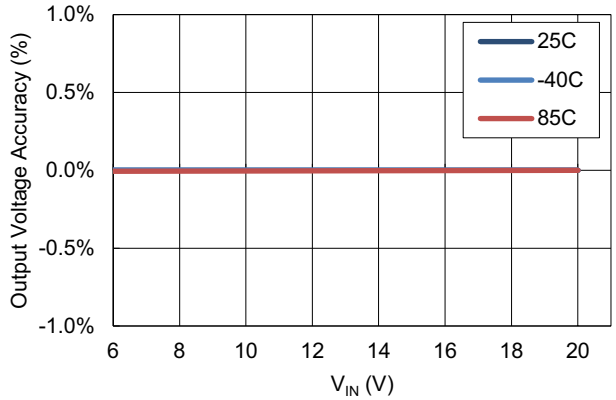


Figure 21. Output Voltage vs Input Voltage for Various Ambient Temperatures (V_{OUT} = 5V, I_{OUT} = 1mA)

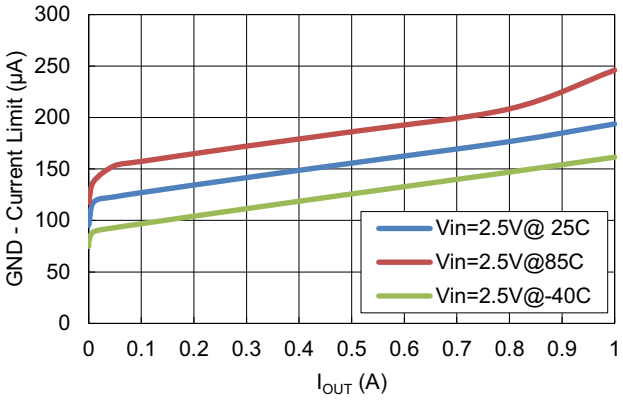


Figure 22. Ground Current for various Ambient Temperatures (V_{IN} = 2.5C, V_{OUT} = V_{ADJ}, V_{EN} = 5V, I_{OUT} = 0A to 1A

C_{IN} = 10µF, unless otherwise stated. (Cont.)

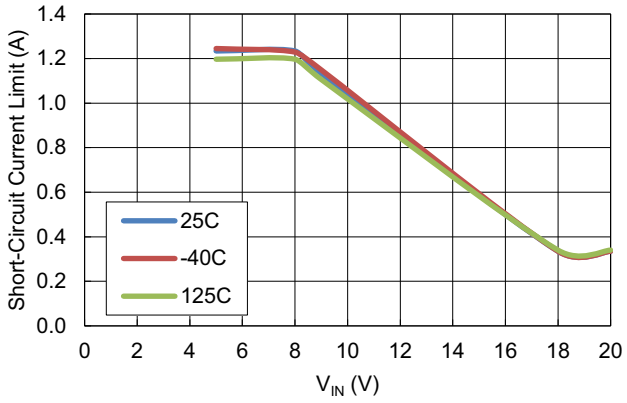


Figure 23. Short-Circuit Current Limit for Various Ambient Temperatures (V_{OUT} = 3.3V)

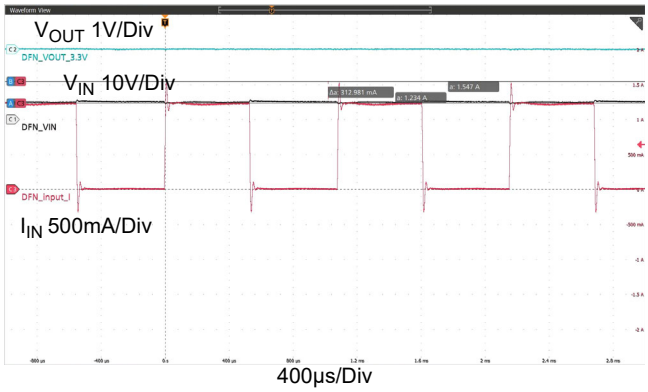


Figure 24. Short-Circuit Current Limit for 25C (V_{IN} = 5V, V_{OUT} = 3.3V)

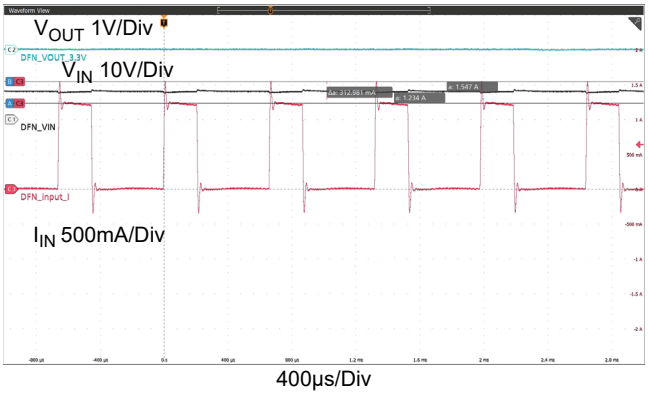


Figure 25. Short-Circuit Current Limit for 25C (V_{IN} = 8V, V_{OUT} = 3.3V)

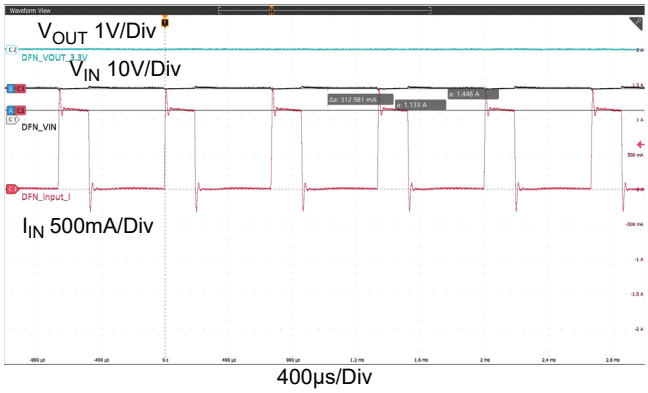


Figure 26. Short-Circuit Current Limit for 25C (V_{IN} = 9V, V_{OUT} = 3.3V)

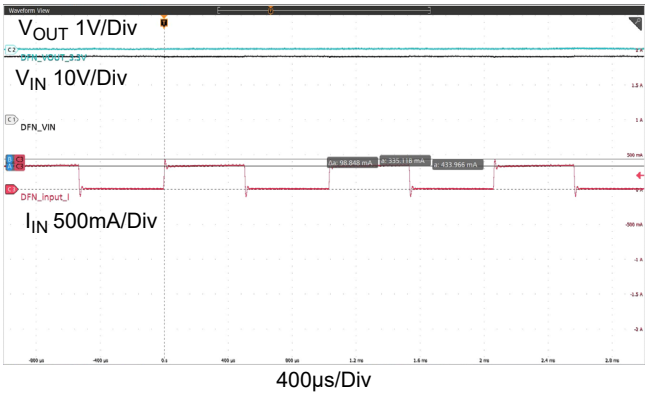


Figure 27. Short-Circuit Current Limit for 25C (V_{IN} = 18V, V_{OUT} = 3.3V)

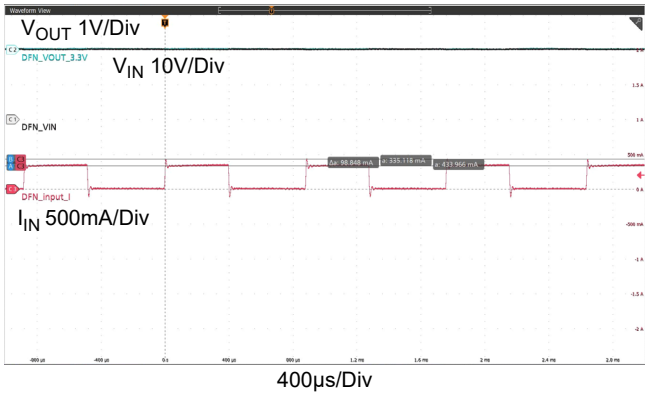


Figure 28. Short-Circuit Current Limit for 25C (V_{IN} = 20V, V_{OUT} = 3.3V)

4.6 Output Noise and PSRR

C_{IN} = 10µF, unless otherwise stated.

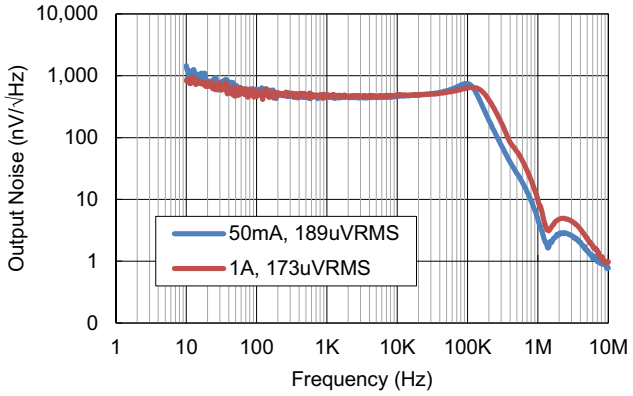


Figure 29. Output Noise vs Frequency for Various I_{OUT} (V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, C_{OUT} = 10µF, C_{FF} = 22pF)

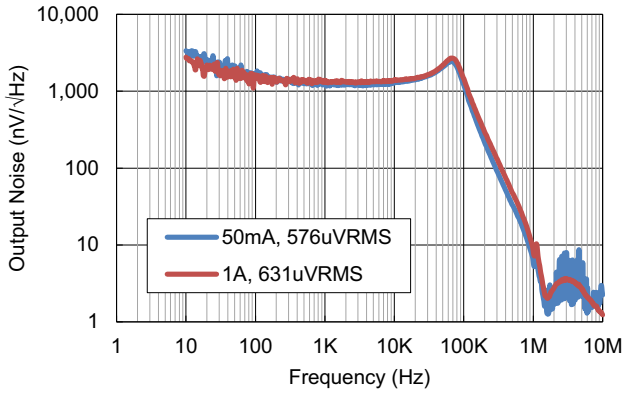


Figure 30. Output Noise vs Frequency for Various I_{OUT} (V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 10µF, C_{FF} = 22pF)

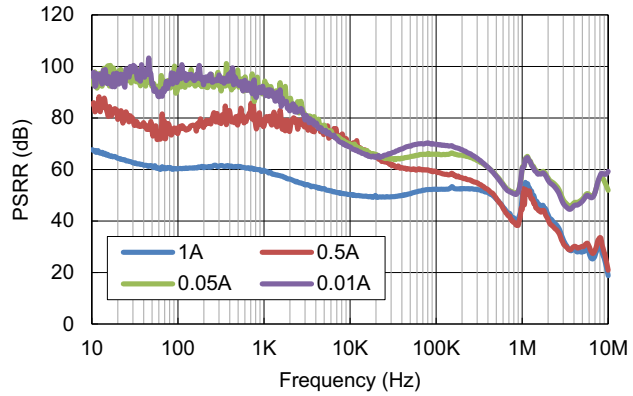


Figure 31. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 8.8V, V_{OUT} = 5V, C_{OUT} = 10µF, C_{FF} = 22pF)

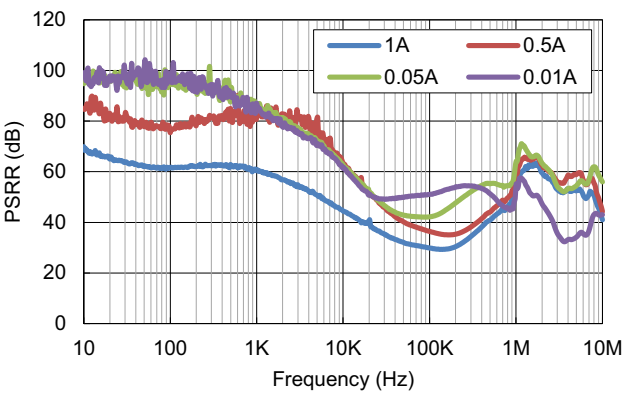


Figure 32. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 7.1V, V_{OUT} = 3.3V, C_{OUT} = 10µF, C_{FF} = 22pF)

5. Application Information

5.1 Function Overview

The RAA214290 is a linear voltage regulator that operates from an input voltage of 2.5V to 20V while sourcing a maximum 1A load. The output voltage is adjustable with external feedback resistors from 1.224V to 18V. It typically draws 80µA of ground current at no load, which drops to 3µA during a shutdown.

The RAA214290 is designed and tested with a 2.2µF minimum output capacitor and a 10µF input capacitor. The LDO is available in a 3x3mm 8-Ld DFN package or an 8-Ld SOIC.

The RAA214290 integrates the following additional features:

- Undervoltage Lockout (UVLO)
- Enable Control
- Short-Circuit Current Limit with Fold-back
- Thermal Shutdown Protection

5.2 Theory of Operation of PMOS LDOs

Like the majority of LDOs with a PMOS pass transistor, the RAA214290 DC output voltage (V_{OUT}) regulation can be modeled with a voltage reference (V_{REF}), PMOS pass-transistor, error amplifier, and feedback (FB) resistors, as shown in Figure 33.

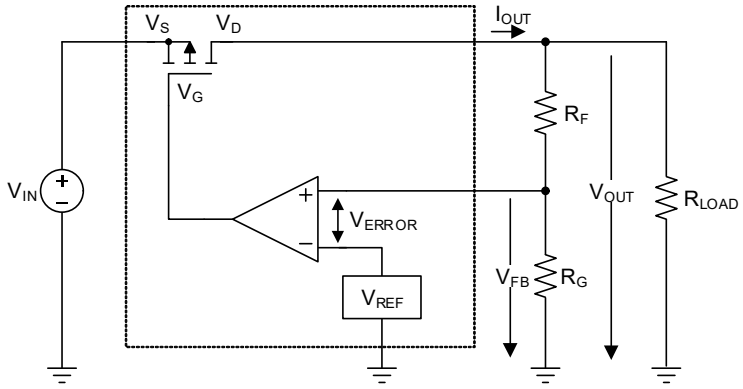


Figure 33. Simple PMOS LDO Regulator Block Diagram

The PMOS pass transistor can be modeled as a variable resistor ($r_{DS(ON)}$) that is controlled by the error amplifier to maintain a constant DC output voltage for changes in load current (I_{OUT}). Assuming the input voltage (V_{IN}) remains constant, the $r_{DS(ON)}$ is adjusted for a given I_{OUT} to set V_{OUT}. This relationship is summarized in Equation 1.

(EQ. 1) $$V_{OUT} = V_{IN} - I_{OUT} \times R_{DS(ON)}$$

V_{OUT} is set using the FB resistor divider, which sets V_{OUT} to a value corresponding to Equation 2.

(EQ. 2) $$V_{OUT} = V_{FB} \times \left(\frac{R_F}{R_G} + 1 \right)$$

The error amplifier compares V_{FB} with the fixed V_{REF} voltage. It minimizes the difference or error voltage between V_{FB} and V_{REF} by changing the PMOS pass transistor's gate voltage and, therefore, the $r_{DS(ON)}$.

If the I_{OUT} suddenly increases because of decreased load resistance, V_{OUT} decreases because the regulator has not responded to the change and the $r_{DS(ON)}$ is too high. V_{FB} decreases and is below the V_{REF} voltage, increasing

the error voltage. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more negatively relative to the FET source to decrease the $r_{DS(ON)}$, which increases the output voltage, bringing it back into regulation.

Similarly, a sudden decrease in I_{OUT} because of increased load resistance causes V_{OUT} to increase because the $r_{DS(ON)}$ is set too low. V_{FB} is then higher than the fixed V_{REF} voltage, increasing the error. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more positively relative to the FET source to increase the $r_{DS(ON)}$, which decreases the output voltage bringing it back into regulation.

For a more detailed explanation of the DC regulation operation of a PMOS LDO regulator, see *R16AN0008: Fundamental Theory of PMOS Low-Dropout Voltage Regulators*.

6. Functional Description

6.1 UVLO

The RAA214290 integrates an internal UVLO circuit to keep the device safely disabled if the input voltage is below the UVLO threshold. This circuit prevents the part from turning on in an unpredictable state.

When the input voltage exceeds the UVLO threshold, the part is enabled, and the output voltage ramps up. The UVLO hysteresis prevents input voltage noise from causing the output to oscillate and prevents input voltage droops due to long input traces and wires from turning off the LDO when it turns on and draws current. Figure 34 illustrates the UVLO operation.

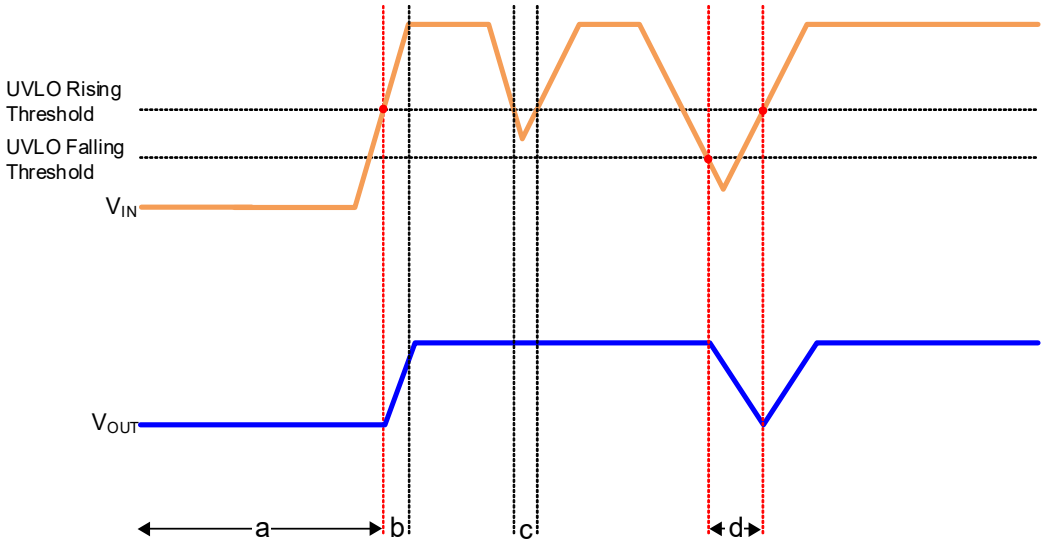


Figure 34. UVLO Operation

- a and d – The LDO is disabled.
- b – The LDO is enabled, and the output starts to rise.
- c – The LDO remains enabled.

6.2 Enable Control

The RAA214290 uses the EN pin voltage (V_{EN}) to enable or disable the LDO. If VEN is less than the V_{EN} threshold, the LDO is disabled. If V_{EN} is greater than the VEN threshold, the LDO is enabled. The V_{EN} hysteresis prevents the enable voltage noise from causing the output to oscillate. When the LDO is disabled, the shutdown current is typically 3µA.

The EN pin can be directly connected to the input voltage for automatic startup or to a logic controller such as an MCU of FPGA. Some logic pins use an open-collector or open-drain transistor to pull LOW and float when HIGH. Connect a 1kΩ or 10kΩ pull-up resistor to ensure proper logic HIGH. The V_{EN} signal source should be capable of swinging above and below the threshold values to ensure proper Enable control operation. The device also has a very accurate and stable Enable threshold, which allows the user to program the Enable voltage through a resistor divider.

6.3 Short-Circuit Current Limit Protection

The Short-Circuit Protection circuitry (I_{LIM}) limits the maximum output current the LDO can source during fault conditions such as short-circuits or startup inrush current. During a short-circuit fault, the LDO becomes a constant current source, and as a result, any decrease in load resistance causes a decrease in the output voltage. This relationship is summarized in Equation 3.

(EQ. 3) $$V_{OUT} = I_{LIM} \times R_{LOAD}$$

The RAA214290 also incorporates fold-back, which reduces the constant current limit to reduce the power dissipation caused during short-circuit events. The fold-back starts when the input voltage is near 13V.

The LDO returns to normal output voltage regulation when the short or overcurrent condition is removed. Because of the high power dissipation caused by overcurrent faults, the LDO may begin to cycle ON and OFF because the die junction temperature (T_J) exceeds thermal fault conditions (+150°C) and subsequently cools down to +130°C when the LDO is disabled.

6.4 Over-Temperature Shutdown (OTSD) Protection

The RAA214290 is protected against thermal overloads caused by current limit protection or high ambient temperature (T_A).

When the die junction temperature (T_J) exceeds +150°C, the thermal shutdown circuit disables the LDO, reducing the output current (I_{OUT}) to 0A and, therefore, reducing the output voltage (V_{OUT}) to 0V, allowing the LDO to cool. A 20°C hysteresis is included to prevent the LDO from uncontrollably heating and cooling.

Prolonged exposure to a T_J exceeding +125°C reduces the long-term stability and life of the LDO. Therefore, the design must consider the T_A the LDO works in, the thermal resistance between T_J and T_A (θ_{JA}), and any fault conditions that can cause the T_J to exceed the recommended operating range. In some applications, a heat sink may need to be implemented. See Power Dissipation and Thermals to determine the maximum junction temperature for an application.

6.5 Voltage Requirements

6.5.1 Input Voltage

The RAA214290 operates with an input voltage of 2.5V to 20V on the VIN pin. The input supply must supply enough current to keep the input voltage from drooping during load steps or high load currents.

For proper voltage regulation, the input voltage must be higher than the sum of the output voltage and the maximum dropout voltage expected for a given application, as expressed in Equation 4.

(EQ. 4) $$V_{IN} > V_{OUT} + V_{DROPOUT(MAX)}$$

The difference between V_{IN} and V_{OUT} required for proper regulation is called the headroom voltage ($V_{HEADROOM}$).

6.5.2 Programming the Output Voltage

The RAA214290 output voltage can be programmed down to 1.224V and up to 18V using external resistors (R_F and R_G) shown in Figure 35.

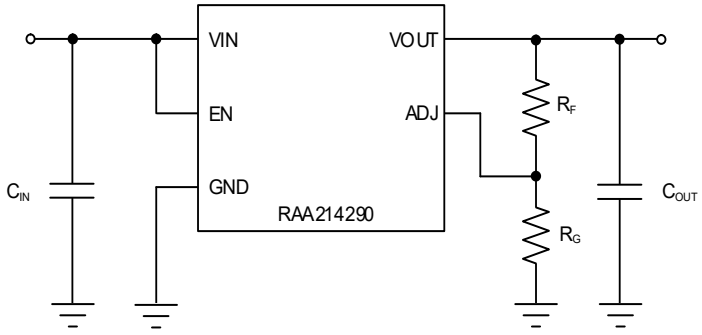


Figure 35. Setting the Output Voltage

V_{OUT} is the required output voltage and can be calculated using Equation 5, where 1.224V is the reference voltage.

(EQ. 5) $$V_{OUT(TARGET)} = 1.224V \times \left(1 + \frac{R_F}{R_G}\right)$$

Similarly, the R_F and R_G resistors are calculated for any target output voltage by rearranging Equation 5 to get Equation 6 and solving for RF.

(EQ. 6) $$R_F = R_G \times \left(\frac{V_{OUT(TARGET)}}{1.224V} - 1\right)$$

Table 1 suggests the FB resistor values to get some common voltage rails with a 0.1% error. These resistors are also commercially available in a 0.1% tolerance. This table is not exhaustive; other R_F and R_G resistor combinations may provide better accuracy.

Table 1. Recommended R_F and R_G Feedback Resistor Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	Error (%)
1.224	0	None	0.0
1.5	100	442	-0.1
1.8	100	210	-0.4
1.9	100	180	-0.2
2.5	100	95.3	-0.3
3	100	68.1	-0.7
3.3	100	59	0.0
4.2	100	41.2	0.1
4.5	100	37.4	0.1
5	100	32.4	0.0
9	100	15.8	0.3
12	100	11.3	-0.5
18	100	7.32	0.3

6.6 External Capacitor Selection

The RAA214290 is stable with C_{IN}, C_{OUT}, and bypass capacitors. For improved load transient, line transient, PSRR, and output noise performance, a feed-forward capacitor (C_{FF}) is recommended, although not required.

Multilayer ceramic capacitors (MLCC) are an excellent choice for bypass capacitors because of their small size, low ESR, low ESL, and wide operating temperature. However, they are not without their problems. Ceramic capacitor values vary with the DC bias voltage, temperature, and tolerance. Therefore, Renesas recommends that they be de-rated.

X5R, X7R, and C0G capacitors are recommended. To ensure the performance of the RAA214290, evaluate the effects of DC bias voltage, temperature, and tolerances for a chosen capacitor. The X7R type is recommended because it has lower capacitance variation over temperature.

Place the bypass capacitors as close as is practical to their respective pins to minimize trace inductance.

6.6.1 Input Capacitor

The recommended minimum input capacitor is 1µF to reduce the negative effects of large input impedances because of long input traces of high source impedances. Renesas recommends connecting this capacitor between VIN and GND. A larger bulk capacitor, such as a 10µF, may need to be added to minimize input voltage drops during large changes in load currents during startup and not affect stability. Larger input capacitors also improve the line transient response.

6.6.2 Output Capacitor

The RAA214290 is stable with an output ceramic capacitor between 2.2µF and 68µF.

A large value output capacitor can help minimize the overshoot and undershoot transient response due to large changes in load current. Larger or multiple output capacitors can be used to improve high-frequency PSRR.

6.6.3 Feed Forward Capacitor

A Feed-Forward Capacitor (CFF) in parallel with the R_F resistor, as shown in Figure 36, can improve the transient, noise, startup, and PSRR performance. However, it is not necessary to use one to achieve stability.

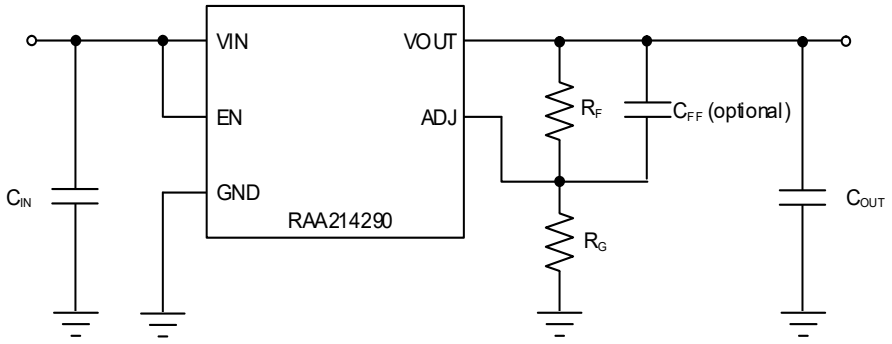


Figure 36. The Feed-Forward Capacitor

Table 2 lists some recommended R_F and R_G resistors and feed-forward capacitor combinations for typical voltage rails. Remember that the R_F and R_G resistor values listed in Table 2 can also be used without a feed-forward capacitor.

Table 2. Recommended R_F and R_G Feedback Resistors and CFF Feed-Forward Capacitors Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	C_{FF} (pF)	Error (%)
1.224	0	None	None	0.0
1.5	13	57.6	43	0.0
1.8	27	57.6	39	0.1
1.9	31.6	57.6	37	0.2
2.5	60.4	57.6	30	-0.3
3	84.5	57.6	25	-0.7
3.3	97.6	57.6	22	0.1
4.2	140	57.6	17	0.0
4.5	154	57.6	16	0.1
5	178	57.6	15	-0.1
9	365	57.6	DNP	0.2
12	511	57.6	DNP	-0.7
18	787	57.6	DNP	0.3

6.7 Power Dissipation and Thermals

To ensure reliable operation, the die junction temperature (T_J) of the RAA214290 must not exceed +125°C. In applications with high ambient temperature (T_A), large headroom voltages ($V_{HEADROOM}$), and large load currents (I_{OUT}), the heat dissipated in the package can become large enough to cause the T_J to exceed the maximum operating temperature of +125°C.

6.7.1 Power Dissipation

Use Equation 7 to calculate Power Dissipation (PD).

(EQ. 7) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times IQ(V_{IN})$$

Because the power dissipation contribution from the quiescent (or ground current) is typically small compared to the current the LDO needs to supply to a load, it can be ignored. Equation 7 then simplifies to Equation 8.

(EQ. 8) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, to lower the power dissipated inside the die, the $V_{HEADROOM}$ and/or the I_{OUT} can be decreased.

6.7.2 The Junction Temperature and Thermal Resistance

The junction temperature (T_J) is the sum of the environmental ambient temperature (T_A) and the temperature rise in the T_J because of power dissipation, which is calculated using Equation 9 if the ambient temperature, Power Dissipation, and θ_{JA} are known.

(EQ. 9) $$T_J = T_A + \theta_{JA} \times PD$$

The θ_{JA} is the thermal resistance between the junction and ambient temperatures and depends largely on the device package and the PCB design. The θ_{JA} includes the thermal resistance of the junction to the bottom thermal pad ($\theta_{JC(BOTTOM)}$) and the resistance of the junction to the top of the package ($\theta_{JC(TOP)}$). The package features, dimensions, areas, thicknesses, and materials determine these two thermal resistances and are therefore fixed.

The remaining thermal resistance that makes up θ_{JA} largely depends on the total PCB copper area, copper weight, location of the thermal planes, and location of the IC on the PCB, amongst other things. Therefore, to compare the θ_{JA} of different products, it is important to ensure the PCB layouts are similar, which is why the JEDEC standard exists.

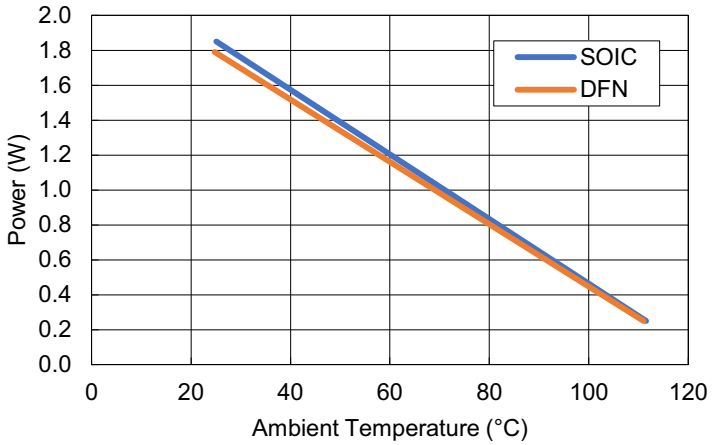


Figure 37. Power Dissipation vs Ambient Temperature for 125°C Junction Temperate on the JEDEC Standard PCB

7. Layout Guidelines

Adhere to the following recommendations for the RAA214290 to achieve optimal performance:

- Place all the required components for the RAA214290 on the same layer as the IC.
- Place a minimum capacitance of 1µF ceramic input capacitor to the VIN and GND pins of the LDO as closely as practical.
- Place a minimum capacitance of 2.2µF ceramic output capacitor to the VOUT and GND pins of the LDO as closely as practical.
- The feedback trace should be short, direct, and away from other noisy traces. Place the feedback resistors as close as possible to the IC.
- The package thermal EPAD is the largest heat conduction path for the package. It should be soldered to a copper pad on the PCB underneath the part. The PCB thermal pad should have as many plated vias to increase the heat flow from the package thermal EPAD to the inner PCB areas and/or the bottom PCB area.
- Keep the vias small but not so small that their inside diameter prevents the solder from wicking through the holes during reflow. For efficient heat transfer, the vias must have low thermal resistance. Do not use thermal relief patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane. The top copper GND layer that the EPAD is connected to is the least thermally resistant path for heat flow. To this end, minimize the components and traces that cut this layer.

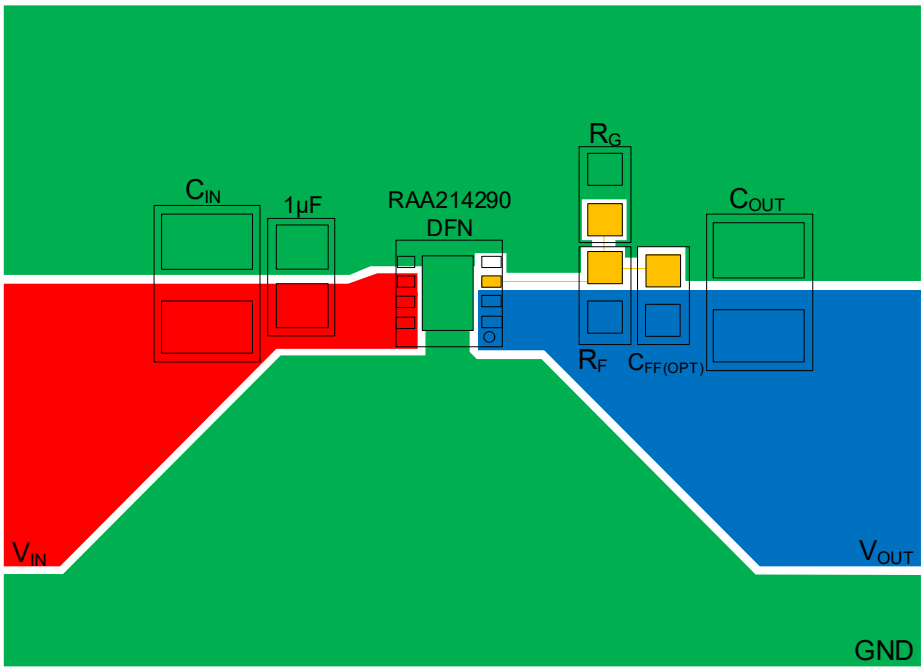


Figure 38. Layout Scheme - DFN

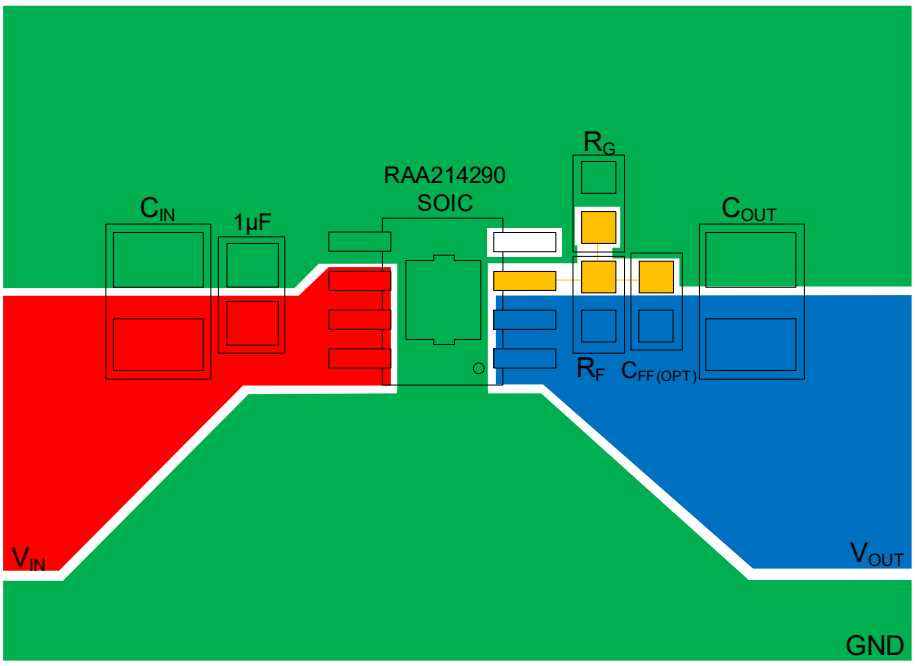


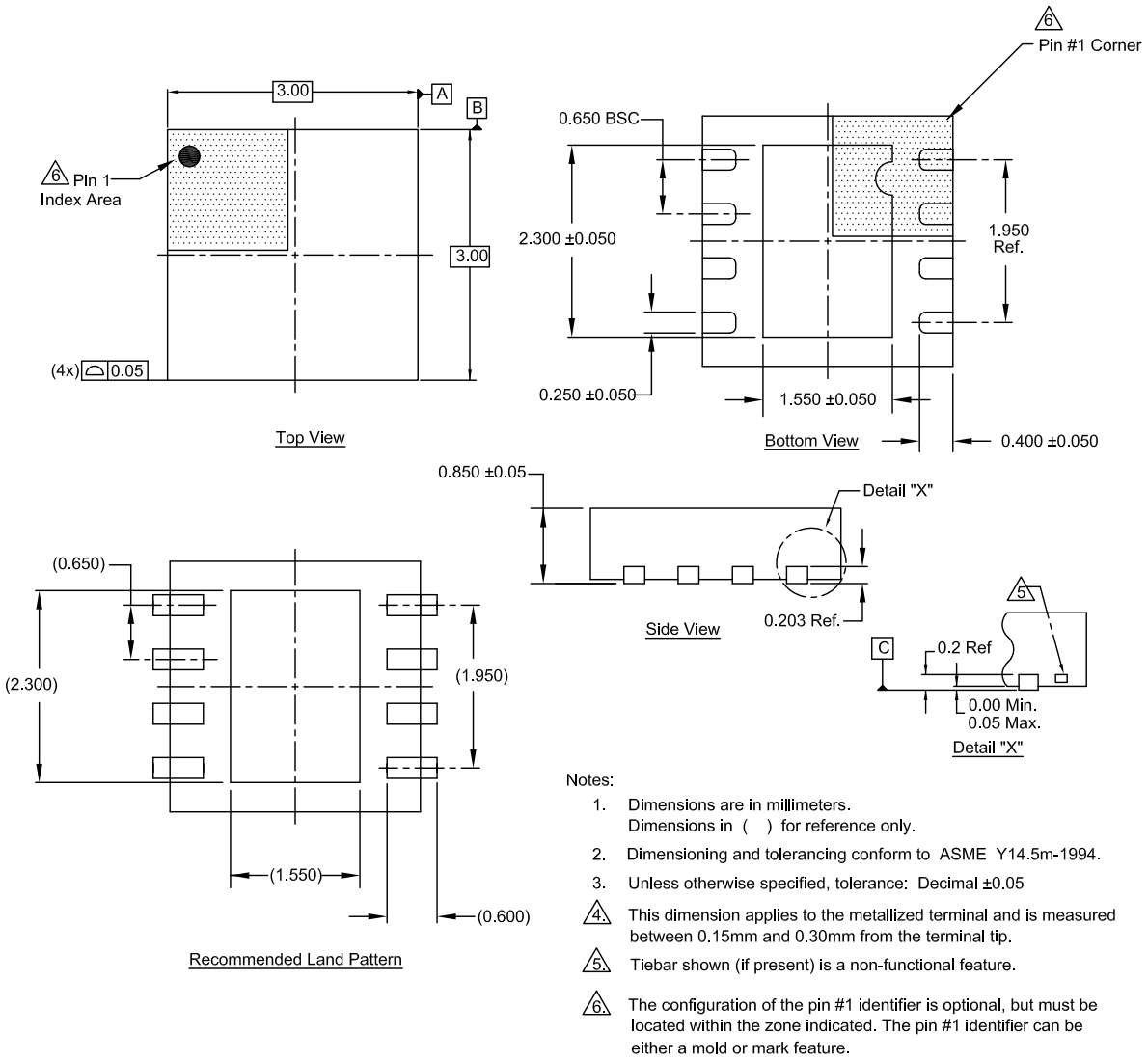
Figure 39. Layout Scheme - SOIC

8. Package Outline Drawings

For the most recent package outline drawing, see L8.3x3L.

L8.3x3L

8 Lead Dual Flat No-Lead Plastic Package (DFN)
Rev 0, 3/20



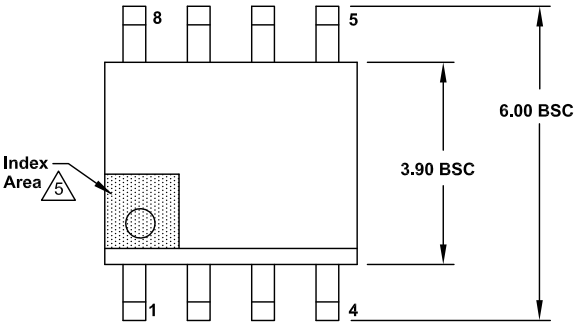
Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.

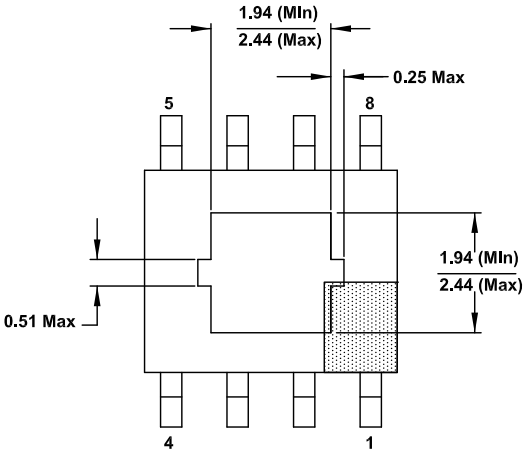
For the most recent package outline drawing, see M8.15H.

M8.15H

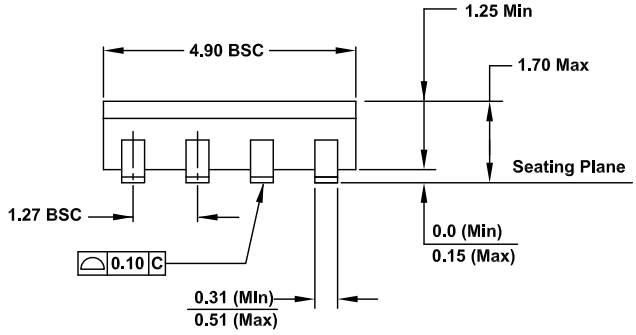
8 Lead Narrow Body Small Outline Exposed Pad Plastic Package (EPSOIC)
Rev 1, 1/20



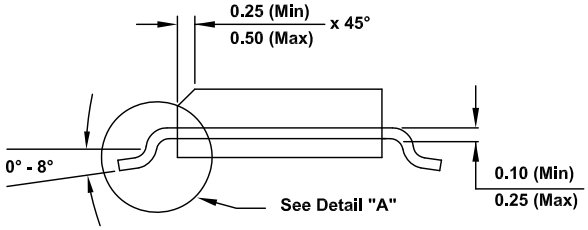
Top View



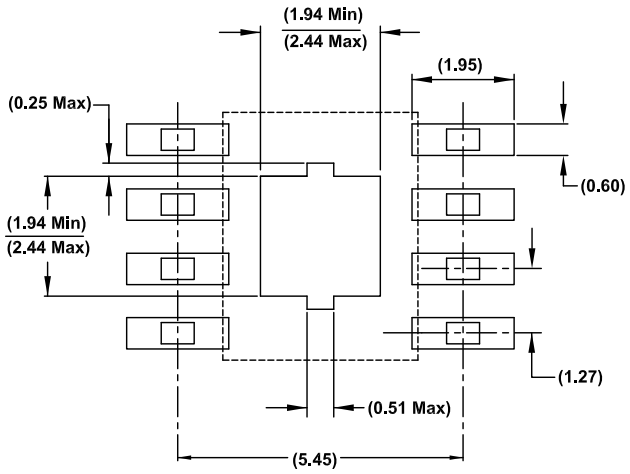
Bottom View



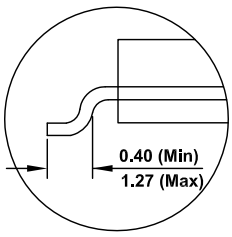
Side View



End View



Typical Recommended Land Pattern



Detail 'A'

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.255mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

9. Ordering Information

Part Number[1]	Part Marking	Package Description[2] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RAA2142904GNP#HC0[4]	214290	8Ld DFN 3×3	L8.3x3L	Reel, 6k	-40°C to 125°C
RAA2142904GSP#HA0[5]		8Ld SOIC	M8.15H	Reel, 2.5k	
RTKA214290DE0010BU	Evaluation Board				

1. For Moisture Sensitivity Level (MSL), refer to the RAA214290 product information pages. For more information about MSL, refer to TB363.
2. For the Pb-Free Reflow Profile, see TB493.
3. See TB347 for details about reel specifications.
4. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
5. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

10. Revision History

Revision	Date	Description
1.03	Mar 29, 2024	Updated Figures 11 and 12 titles.
1.02	Jan 31, 2024	Updated page 1 information. Updated the Dropout Voltage maximum spec from 1050mV to 1150mV.
1.01	Jan 16, 2024	Removed one of the Short-Current Limit specs (middle row). Added Short-Circuit Current Foldback Threshold specification.
1.00	Nov 9, 2023	Initial release.

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