# RAA211650

60V 5A Integrated Switching Regulator

The RAA211650 is an integrated 60V, 5A synchronous buck regulator with adjustable switching frequency from 200kHz up to 2.5MHz. It supports a wide input voltage range from 4.5V to 60V and adjustable output voltage (0.8V to maximum duty cycle * $V_{IN}$). The integrated low $r_{DS(ON)}$ MOSFETs, gate drivers, and the controller make RAA211650 an efficient voltage step-down solution.

The device switches at a default frequency of 500kHz if the RT pin is tied to AVCC, however, it can be programmed to switch from 200kHz to 2.5MHz by using an external resistor on the RT pin. The MODE/SYNC pin can dither the oscillator frequency if the spread-spectrum operation is required. The internal oscillator can also be synchronized to an external clock through the MODE/SYNC pin. The integrated regulator also has options either to use internal fixed compensation or user-selected external compensation.

To limit inrush current during startup, RAA211650 has 2ms fixed internal soft-start time. It can also be programed by an external capacitor.

The RAA211650 provides programmable startup delay time for sequencing purposes. Also, the RAA211650 provides comprehensive protections including undervoltage lockout, overcurrent (positive and negative), overvoltage, and over-temperature.

The device is available in a 28 Ld 4mmx5mm QFN package.

## Features

- 4.5V to 60V input supply range
- Integrated high-side (90mΩ) and low-side (37mΩ) MOSFETs
- 1% accurate voltage reference over temperature
- Fixed-frequency operation with optional spread spectrum and external clock sync
- Adjustable switching frequency from 200kHz to 2.5MHz
- Programmable soft-start timing
- Programmable startup and shutdown delays
- Bidirectional overcurrent protection on both internal FETs
- Extensive voltage and temperature protection
- Compact 28 Ld 4x5mm QFN package

## Applications

- Industrial power supplies
- 12V/48V industrial and computing PoL
- ATM, vending, and gaming machines
- Robotics
- Programmable Logic Controllers
- After-market automotive


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# 1. Overview

## 1.1 Typical Applications

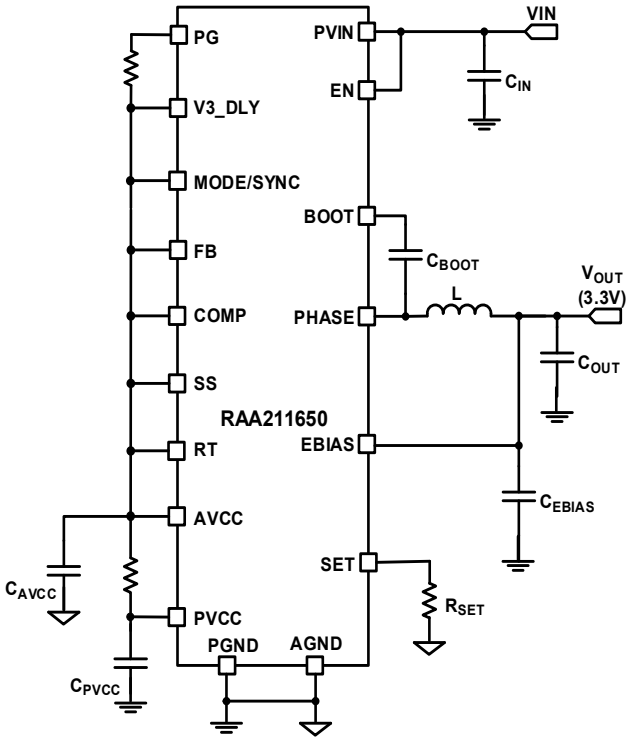



**Figure 1. Typical Application Circuit Diagram for 3.3V $V_{OUT}$ Using Internal Features**

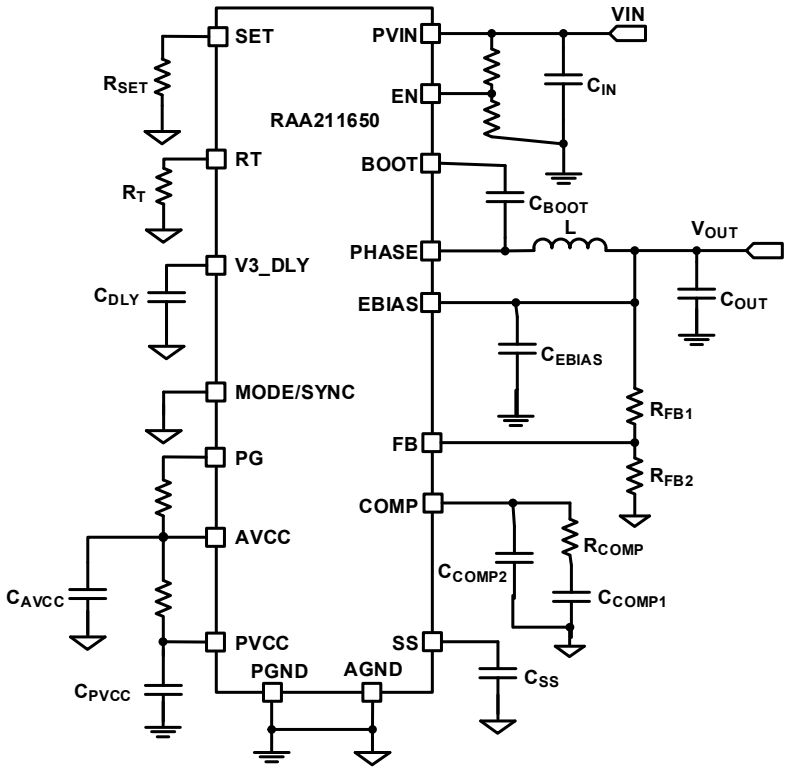



**Figure 2. Typical Application Circuit Diagram with External Features, $V_{OUT}$ < 12V**

## 1.2 Block Diagram

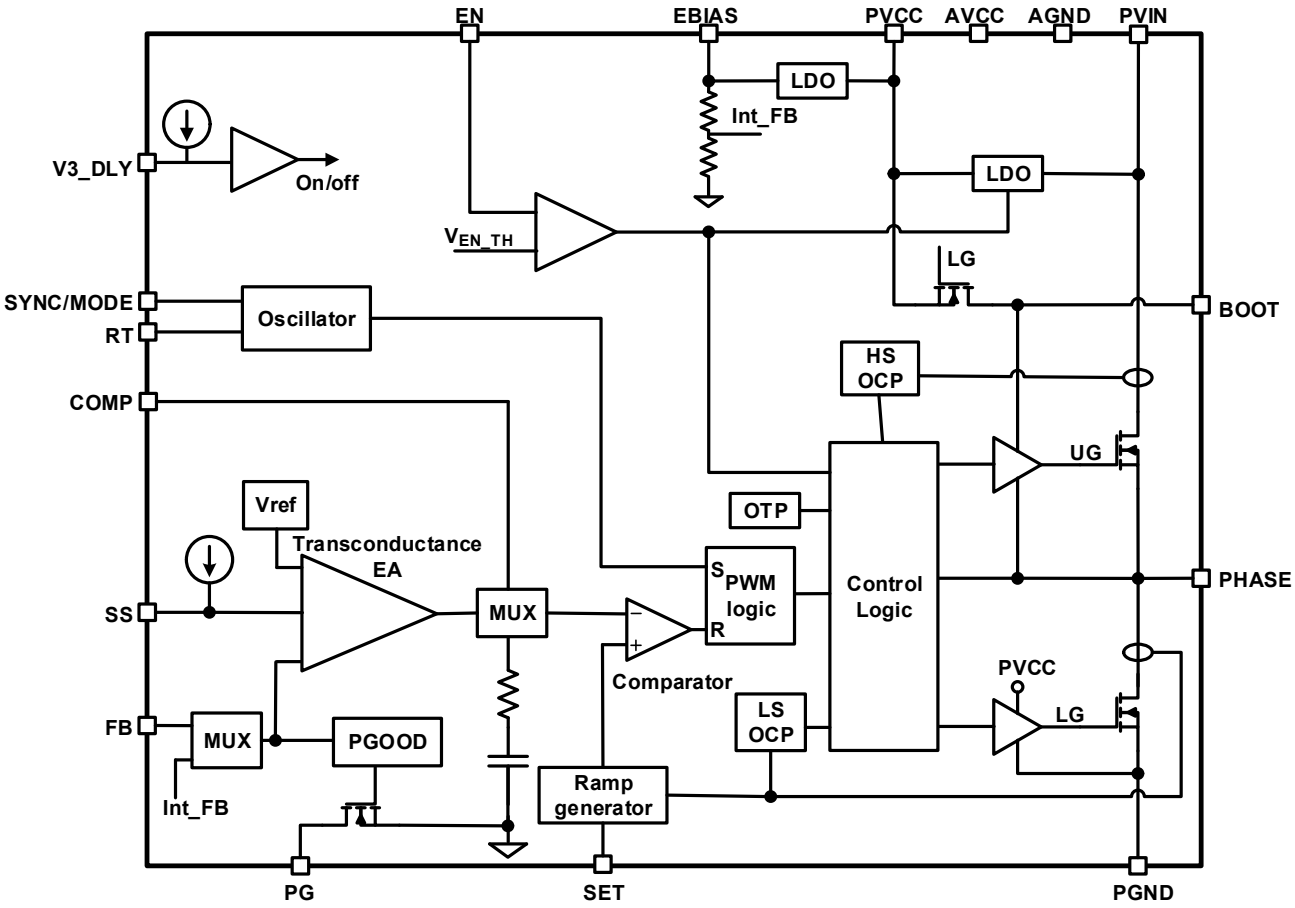
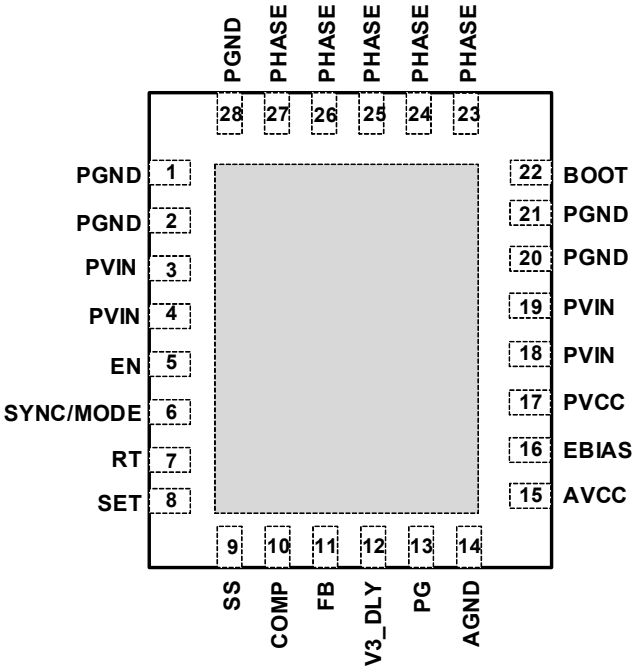



Figure 3. Functional Block Diagram

# 2. Pin Information

## 2.1 Pin Assignments




Top View

## 2.2 Pin Descriptions

| Pin Number | Pin Name | Description |
|---|---|---|
| 1, 2, 20, 21, 28 | PGND | Power ground terminal |
| 3, 4, 18,19 | PVIN | Voltage supply input. The main power input for the IC. Connect to a suitable voltage source within IC operating range. Place a ceramic capacitor from PVIN to PGND close to the IC for decoupling. |
| 5 | EN | Accurate enable signal, accurate to ±5% |
| 6 | SYNC/MODE | The SYNC/MODE pin controls the PWM clock. If SYNC/MODE is tied to AGND, the regulator operates in fixed frequency mode. If SYNC/MODE is tied to AVCC, it operates in fixed frequency mode with spread spectrum enabled. If SYNC/MODE is fed an external clock signal, the external clock signal is divided internally to half its frequency. The regulator operates in fixed frequency mode with its PWM clock synchronized to the divided clock. The PWM clock synchronizes only if the divided external frequency is greater than 110% of the frequency set by RT. |
| 7 | RT | A resistor connected from this pin to AGND sets the switching frequency from 200kHz to 2.5MHz. If SYNC/MODE is tied to AGND, the switching frequency is constant. If SYNC/MODE is tied to AVCC, the resistor connected to RT sets the base switching frequency for spread spectrum operation. Tie RT to AVCC for the internal default 500kHz switching frequency. See RT Switching Frequency for selection of RT. |
| 8 | SET | The resistor connected from SET to AGND programs the slope compensation.<br>**Note:** Do not float this pin. Use the design spreadsheet to calculate resistor value. |
| 9 | SS | Soft-start input. SS controls soft-start. Tie SS to AVCC for internal soft-start of 2ms. A capacitor connected from SS to ground sets the programmable soft-start time. The SS pin sources 5µA in soft-start. When the SS pin voltage reaches 0.8V, the soft-start ramp finishes, regulation starts based on the internal reference of 0.8V. |

| Pin Number | Pin Name | Description |
|---|---|---|
| 10 | COMP | Compensation node. COMP is the output of the transconductance error amplifier. Tie COMP to AVCC to select internal compensation. Connect an RC network from COMP to GND when using external compensation. |
| 11 | FB | Feedback input pin for the regulator. The output voltage is set by an external resistor divider connected to FB. Tie the FB pin to AVCC and the EBIAS pin to VOUT to use internal feedback that regulates an output voltage at 3.3V. |
| 12 | V3_DLY | Delay input pin. Connect a capacitor from V3_DLY to AGND to set a delay time that can be used for sequencing. The delay timer starts when EN is driven to a logic high and ends with the beginning of soft-start. When EN is driven to logic low, the capacitor on V3_DLY adds delay time to the regulator shutdown. A 5µA current is sourced out of the V3_DLY pin, and when the pin voltage crosses 1.2V, the delay period is ended. Tie V3_DLY to AVCC if no delay is required. |
| 13 | PG | Power-good indicator pin. The buck regulator is in normal operation when PG is high. PG goes high when SS is greater than or equal to 1.2V, and the feedback voltage exceeds 91% of VREF. PG goes low if EN is driven low or the FB voltage exceeds the ±12% PG tolerance or any fault conditions exists. This is an open-drain pin. |
| 14 | AGND | Analog/signal ground |
| 15 | AVCC | Analog bias supply. Internal LDOs generate the PVCC. Connect an RC filter from PVCC to AVCC. See Figure 60 for connection example. Renesas recommends using a resistor of 1Ω and capacitor of 1µF for the AVCC filter. |
| 16 | EBIAS | External bias pin. This pin can be connected to an external voltage source ranging from 3.15V to 12V. EBIAS is connected to the internal LDO that generates PVCC. If EBIAS is connected to a voltage source, the IC starts up with the PVCC LDO powered from VIN and switches over to the EBIAS LDO. The EBIAS voltage source can be derived from the output voltage of the switching regulator if it is less than 12V. Using the EBIAS pin reduces power dissipation in the controller, particularly in applications with high VIN voltage. **Note:** If EBIAS is not used, connect the EBIAS pin to the ground. |
| 17 | PVCC | PVCC is the output of the internal 3.3V LDO regulators. When the IC initially starts up, PVCC is supplied by the LDO tied to VIN. If there is voltage available on EBIAS, it switches over to the EBIAS LDO to supply PVCC. PVCC is used as the gate drive supply voltage for the internal MOSFETs. |
| 22 | BOOT | Bootstrap supply pin. Connect a 0.1µF capacitor from BOOT to PHASE. |
| 23, 24, 25, 26, 27 | PHASE | Switch node pins. Connect these pins to the output inductor and the bootstrap capacitor. |
| - | EPAD | The EPAD is connected to PGND. It provides thermal relief for the package. Connect the EPAD to the board ground plane using as many vias as possible. |

# 3. Specifications

## 3.1 Absolute Maximum Ratings

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| PVIN, EN | -0.3 | 65 | V |
| EN | | PVIN+6 | V |
| EBIAS | -0.3 | 15 | V |
| PHASE, SET | -0.3 | PVin+0.3 | V |
| PHASE, 20ns transient | -2 | PVin+0.3 | V |
| BOOT | | Phase+4 | V |
| BOOT to PHASE and PVCC/AVCC to AGND | -0.3 | 4 | V |
| All other pins | -0.3 | AVCC+0.3 | V |
| Human Body Model (Tested per JS-001-2017) | - | 2.5 | kV |
| Charged Device Model (Tested per JS-002-2014) | - | 2 | kV |
| Latch-Up (Tested per JESD78E; Class 2, Level A) | - | 100 | mA |

## 3.2 Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W)[1] | $\theta_{JC}$ (°C/W)[2] |
|---|---|---|
| 28 Ld 4x5 QFN Package | 35 | 1.2 |

1. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For $\theta_{JC}$, the case temperature location is the center of the exposed metal pad on the package underside.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Maximum Junction Temperature | - | +150 | °C |
| Maximum Storage Temperature Range | -65 | +150 | °C |
| Pb-Free Reflow Profile | See TB493 | | |

## 3.3 Recommended Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Input Voltage, PVIN | 4.5 | 60 | V |
| External Bias Voltage | 3.15 | 12 | V |
| Output Voltage, $V_{OUT}$ | 0.8 | Dmax*$V_{IN}$[1] | V |
| Output Current, $I_{OUT}$ | 0 | 5 | A |
| Junction Temperature, $T_J$ | -40 | +125 | °C |

1. Limited by minimum off-time.

## 3.4 Electrical Specifications

$T_J$ = -40°C to +125°C, $V_{IN}$ = 4.5V to 60V, unless otherwise noted. Typical values are at $T_A$ = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**.

| Parameter | Symbol | Test Conditions | Min[1] | Typical | Max[1] | Unit |
|---|---|---|---|---|---|---|
| **Supply voltage** | | | | | | |
| PVIN Voltage Range | PVIN | | **4.5** | | **60** | V |
| PVIN Typical Shutdown Current | $I_{SDN}$ | PVIN = 24V, EN = 0V | | 1 | 4 | µA |
| PVIN Current in Regulation | | PVIN = 24V, FB = AVCC, VOUT/EBIAS = 3.3V, $f_{SW}$ = 500kHz, no load | | 16.5 | | mA |
| PVCC + AVCC Supply Current | | RT = AVCC, EN = 2V, FB = 0.9V, no load | | 1 | | mA |
| | | $f_{SW}$ = 500kHz (RT = AVCC), EN = 2V, FB = 0.77V, no load | | 12 | | mA |
| PVIN Undervoltage Lockout | | PVIN Rising | **3.95** | 4.15 | **4.45** | V |
| PVIN UVLO Hysteresis | | PVIN Falling | | 300 | | mV |
| AVCC Output Voltage using PVIN Linear Regulator | | EBIAS = 0V | **3.1** | 3.3 | **3.5** | V |
| AVCC Output Voltage from EBIAS Linear Regulator | | EBIAS = 5V | **3.1** | 3.3 | **3.5** | V |
| AVCC Undervoltage Lockout | $AVCC_{UV}$ | VCC rising | **2.75** | 2.9 | **3.05** | V |
| AVCC UVLO Hysteresis | | | **125** | 200 | **300** | mV |
| AVCC Current Limit from VIN | | PVIN = 6V | **80** | 115 | **150** | mA |
| AVCC Current Limit from EBIAS | | EBIAS = 6V | **80** | 115 | **150** | mA |
| EBIAS | | | **3.15** | - | **12** | V |
| EBIAS Rising Threshold | | | | 3 | **3.15** | V |
| EBIAS Hysteresis | | | | 170 | | mV |
| **Oscillator** | | | | | | |
| Internal Oscillator Frequency Range[3] | | SYNC/MODE = AVCC | **250** | | **2500** | kHz |

$T_J$ = -40°C to +125°C, $V_{IN}$ = 4.5V to 60V, unless otherwise noted. Typical values are at $T_A$ = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**.(Cont.)

| Parameter | Symbol | Test Conditions | Min[1] | Typical | Max[1] | Unit |
|---|---|---|---|---|---|---|
| Oscillator Frequency | $f_{SW}$ | RT = 40.2k | **1980** | 2160 | **2330** | kHz |
| | | RT = 90.9k | **925** | 1000 | **1075** | kHz |
| | | RT = 499k | **175** | 200 | **225** | kHz |
| Oscillator Fixed Frequency | | RT = AVCC | **465** | 500 | **535** | kHz |
| SYNC Input High Level | | | **2** | | | V |
| SYNC Input Low Level | | | | | **0.4** | V |
| SYNC Frequency Range | | $f_{SW}$ defined by RT[2] | **500** | | **5000** | kHz |
| **Buck Converter** | | | | | | |
| $V_{OUT}$ Voltage Range | $V_{OUT}$ | | **0.8** | | **Dmax*PVIN** | V |
| Feedback Voltage Reference | $V_{REF}$ | | | 0.800 | | V |
| Feedback Voltage Reference Accuracy | | PVIN = 24V, $I_{OUT}$ = 500mA, room temperature | -0.6 | | +0.6 | % |
| | | Over-temperature -40 to 125° | **-1** | | **1** | % |
| Feedback Voltage Line Regulation | | PVIN = 5V to 60V[3] | | 0.1 | | %/V |
| Typical Error Amplifier Transconductance | | External compensation mode | | 2 | | mS |
| Typical Current Sense Gain | | | | 0.06 | | V/A |
| Output Current | | | **5** | | | A |
| Minimum On-Time | | | | 45 | | ns |
| Minimum Off-Time | | | **235** | 265 | **295** | ns |
| Peak Efficiency[3] | | (PVIN = 24V, $V_{OUT}$ = 3.3V, L = 3.3µH, EBIAS = $V_{OUT}$, $C_{OUT}$ = 80µF, $f_{SW}$ = 500kHz) | | 89.7 | | % |
| Efficiency (5A)[3] | | | | 87.6 | | % |
| **Power MOSFETs** | | | | | | |
| Upper FET $r_{DS(ON)}$ | | | | 90 | | mΩ |
| Lower FET $r_{DS(ON)}$ | | | | 37 | | mΩ |
| **Enable Input** | | | | | | |
| Accurate EN/UVLO Threshold | | EN/UV rising | **1.425** | 1.5 | **1.575** | V |
| EN Hysteresis | | | | 140 | | mV |
| Coarse EN/UVLO Rising Threshold | | | **0.85** | 1 | **1.2** | V |
| Coarse EN/UVLO Hysteresis | | | **40** | 110 | **250** | mV |
| **Power-Good Open-Drain Output** | | | | | | |
| PGOOD Logic low | | Sink 2mA | | | 0.3 | V |
| PGOOD Deglitch Filter[3] | | | | 5 | | µs |

$T_J$ = -40°C to +125°C, $V_{IN}$ = 4.5V to 60V, unless otherwise noted. Typical values are at $T_A$ = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**.(Cont.)

| Parameter | Symbol | Test Conditions | Min[1] | Typical | Max[1] | Unit |
|---|---|---|---|---|---|---|
| PG | | Lower PG threshold, VFB falling | **85** | 88 | **91** | % |
| | | Lower PG hysteresis | | 3 | | % |
| | | Upper PG threshold, VFB rising | **109** | 112 | **115** | % |
| | | Upper PG hysteresis | | 3 | | % |
| **Internal Soft-Start Function** | | | | | | |
| Soft-Start Time | $t_{SS}$ | SS = $AV_{CC}$ (internal SS Mode), SS begin to $V_{OUT}$ settled | **1.73** | 2 | **2.33** | ms |
| Internal SS Completion Time | | Internal SS mode (SS begin to PG assert) | **2.6** | 3 | **3.5** | ms |
| **External Soft-Start Function** | | | | | | |
| SS Charge Current | | | **4** | 5 | **6** | µA |
| SS Pull-Down Resistance | | | | 560 | | Ω |
| External SS Completion Threshold[4] | | | | 1.2 | | V |
| **DELAY Function** | | | | | | |
| DELAY Charging Current | | V3_DLY = 0V | **4** | 5 | **6** | µA |
| DELAY Threshold | | | | 1.2 | | V |
| DELAY Pull-Down Resistance | | | | 700 | | Ω |
| **Fault Protection** | | | | | | |
| Valley Current Limit | | | **6** | 7.2 | **9** | A |
| High-Side MOSFET OCP[3] | | | **10** | 12 | | A |
| Negative Current Limit | | | **-4.3** | -3.5 | **-2.9** | A |
| OVP[3] | | VFB rising | **116** | 120 | **128** | % |
| OVP Deglitch[3] | | | | 2 | | µs |
| UVP (Undervoltage Protection, Short-Circuit Protection) | FBUVP | VFB falling after soft-start completed | **65** | 70 | **74** | % |
| Hiccup Timer | $t_{HICUP}$ | | | 200 | | ms |
| Thermal Shutdown[3] | $T_{SD}$ | At junction temperature | | 153 | | °C |
| Thermal hysteresis[3] | $T_{HYS}$ | At junction temperature | | 30 | | °C |

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Specified frequency is the SYNC pin frequency. The regulator switching frequency will be half of the SYNC pin frequency.
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
4. $V_{OUT}$ is settled when the SS pin crosses 0.8V. PG asserts when SS crosses 1.2V.

# 4. Typical Performance Graphs

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.

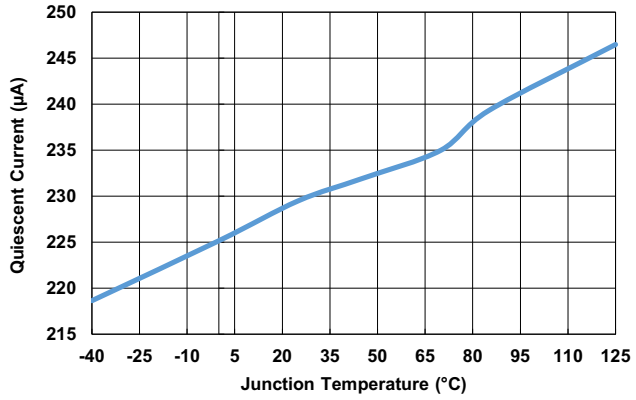



**Figure 4. PVIN Quiescent Current vs Junction Temperature**

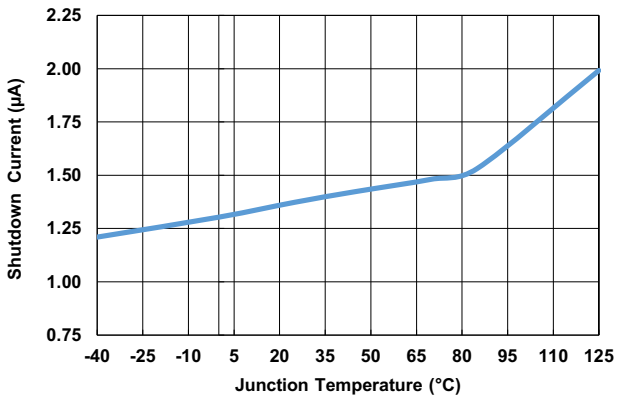



**Figure 5. PVIN Shutdown Current vs Junction Temperature**

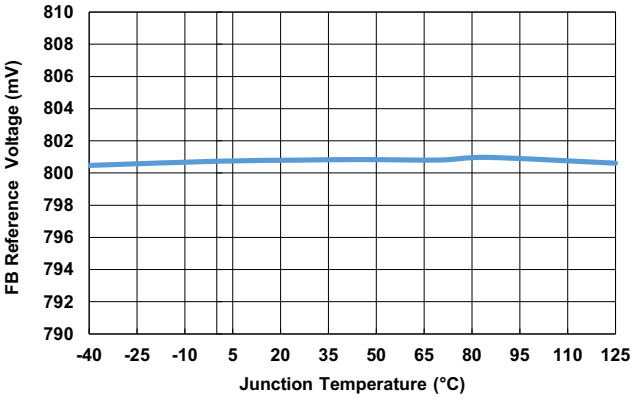



**Figure 6. Feedback Voltage vs Junction Temperature**

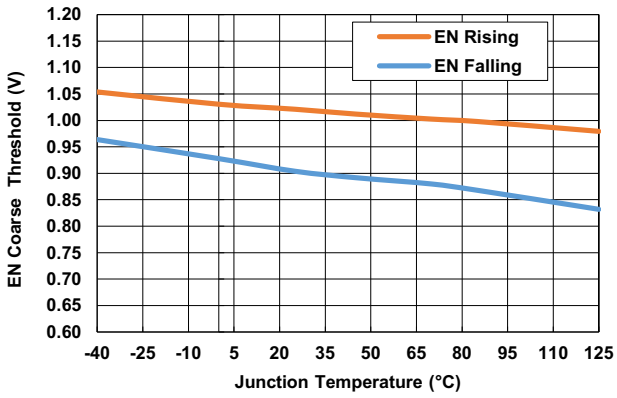



**Figure 7. Enable Coarse Threshold vs Junction Temperature**

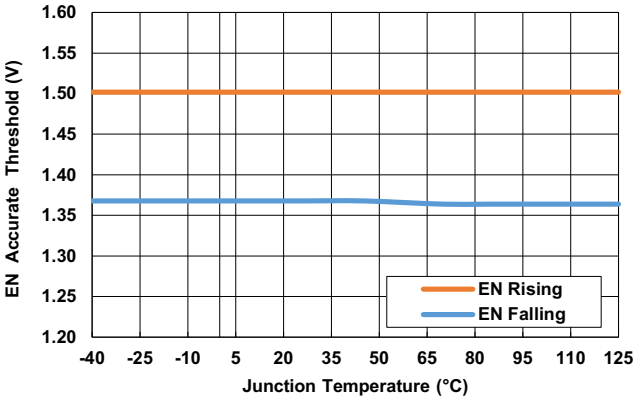



**Figure 8. Enable Accurate Threshold vs Junction Temperature**

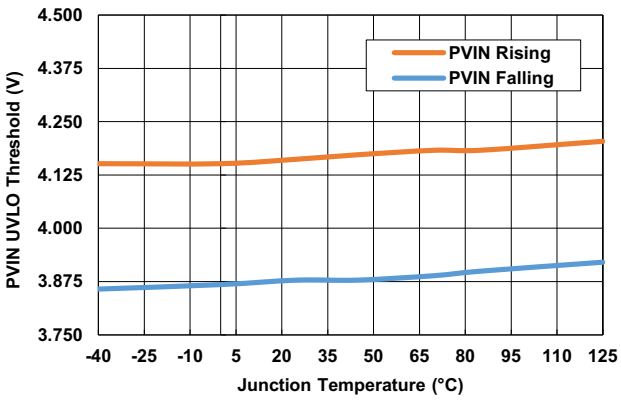



**Figure 9. PVIN UVLO Threshold vs Junction Temperature**

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.(Cont.)

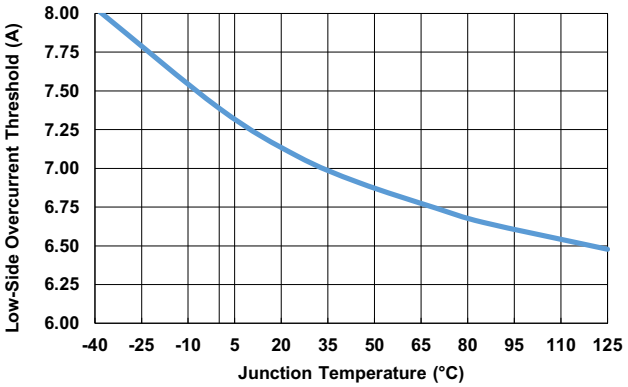



**Figure 10. Low-Side OCP threshold vs Junction Temperature**

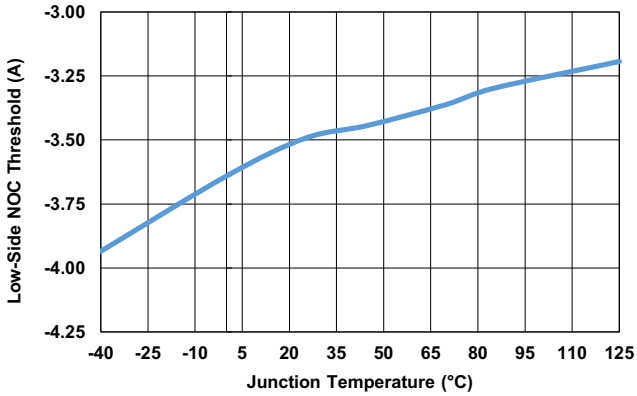



**Figure 11. Low-Side Negative Overcurrent Threshold vs Junction Temperature**

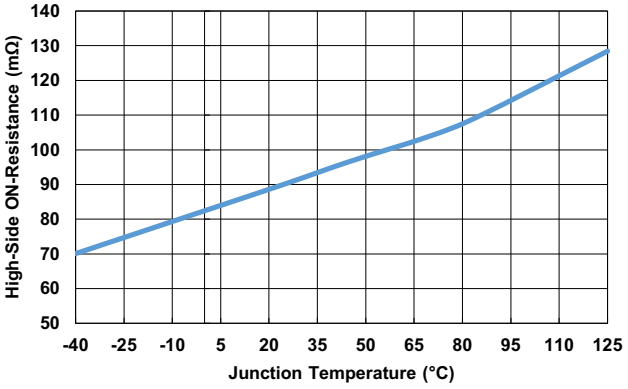



**Figure 12. High-Side $r_{DS(ON)}$ vs Junction Temperature**

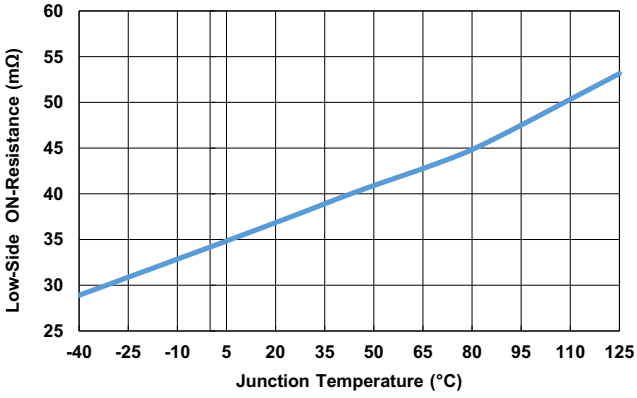



**Figure 13. Low-Side $r_{DS(ON)}$ vs Junction Temperature**

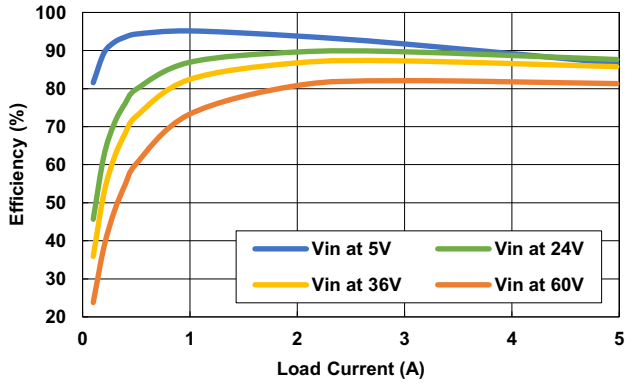



**Figure 14. Efficiency vs Load Current ($V_{OUT}$ = 3.3V)**

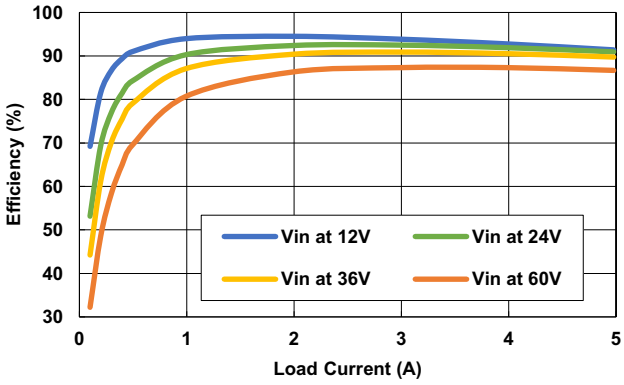



**Figure 15. Efficiency vs Load Current ($V_{OUT}$ = 5V), L = 4.7µH, $C_{OUT}$ = 70µF**

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.(Cont.)

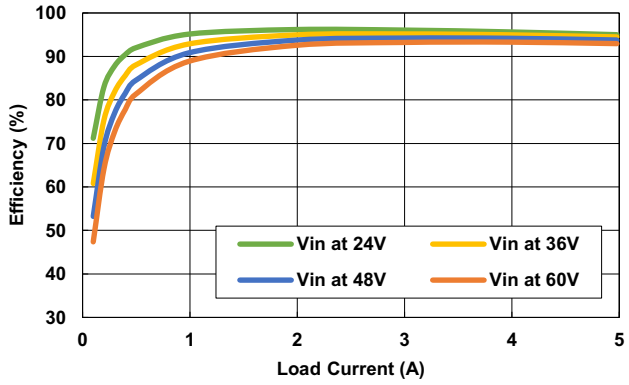



**Figure 16. Efficiency vs Load Current ($V_{OUT}$ = 12V), L = 10µH, $C_{OUT}$ = 50µF**

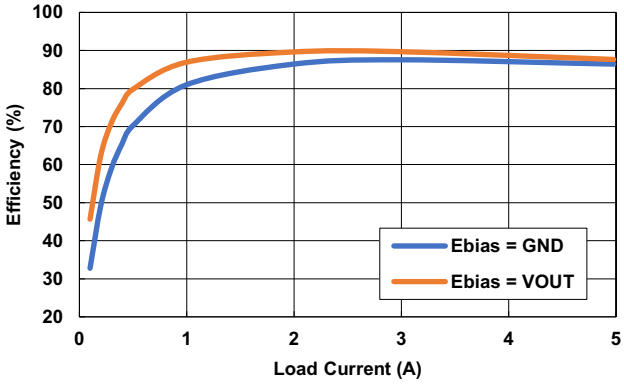



**Figure 17. Efficiency vs Load Current ($V_{OUT}$ = 3.3V) with Ebias = $V_{OUT}$ and Ebias = GND**

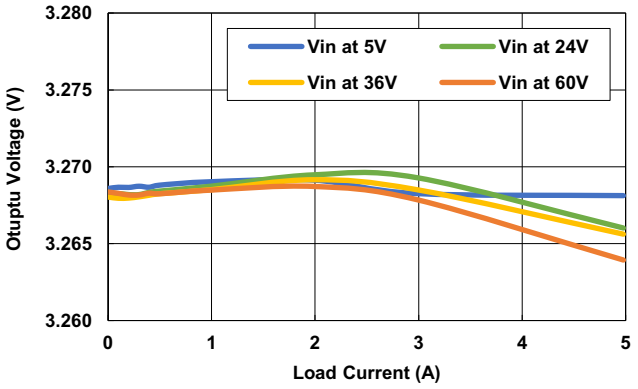



**Figure 18. Load Regulation**

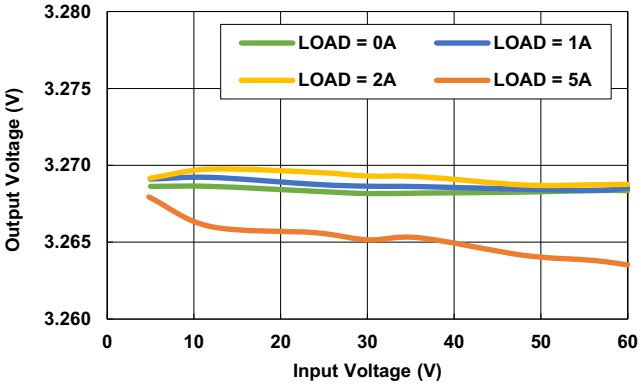



**Figure 19. Line Regulation**

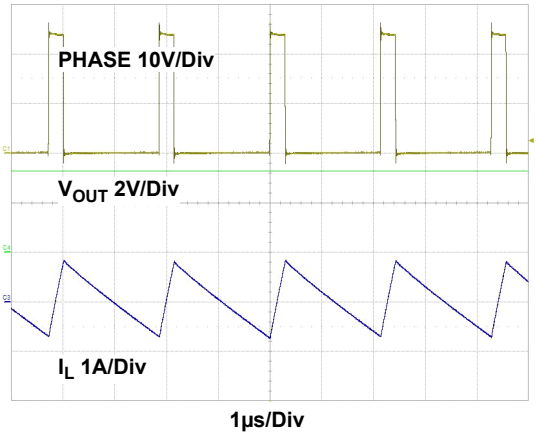



**Figure 20. Steady-State Operation $I_{OUT}$ = 0A**

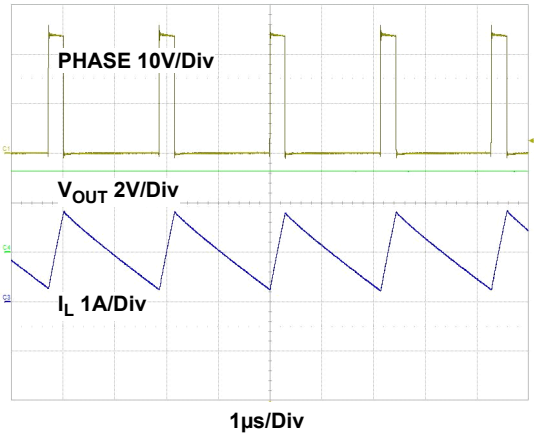



**Figure 21. Steady-State Operation $I_{OUT}$ = 1A**

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.(Cont.)

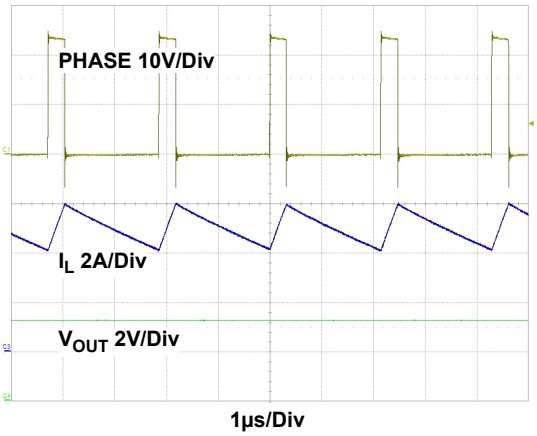



Figure 22. Steady-State Operation $I_{OUT}$ = 5A

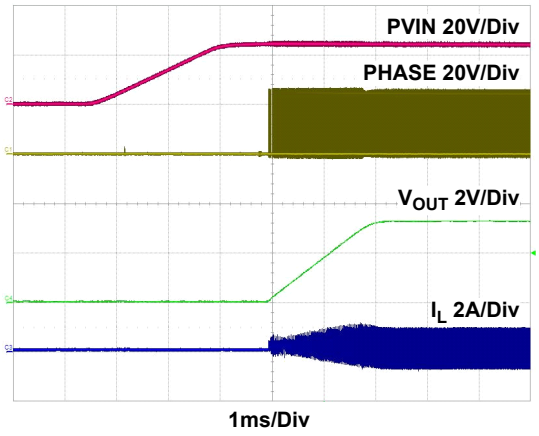



Figure 23. Start-Up through PVIN, $I_{OUT}$ = 0A

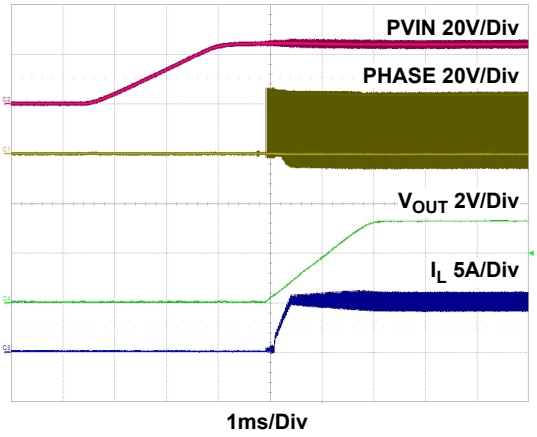



Figure 24. Start-Up through PVIN, $I_{OUT}$ = 5A

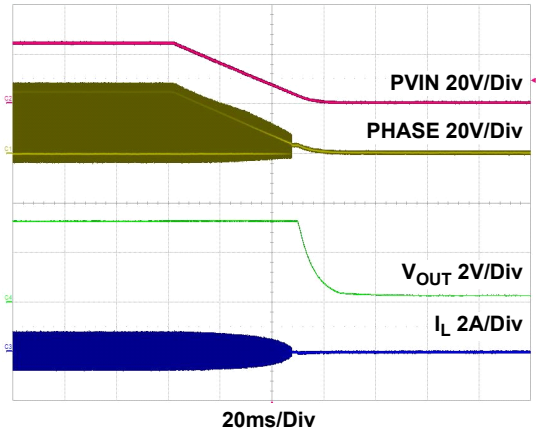



Figure 25. Shutdown through PVIN $I_{OUT}$ = 0A

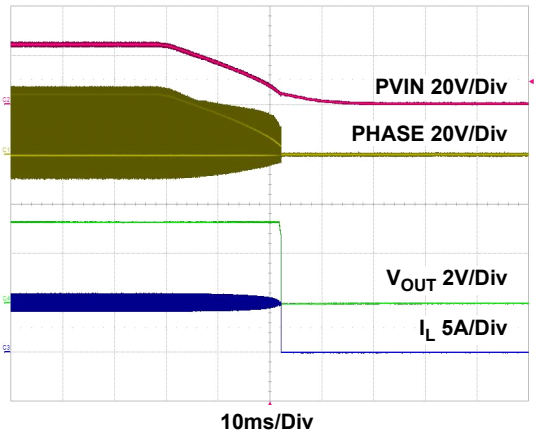



Figure 26. Shutdown through PVIN $I_{OUT}$ = 5A

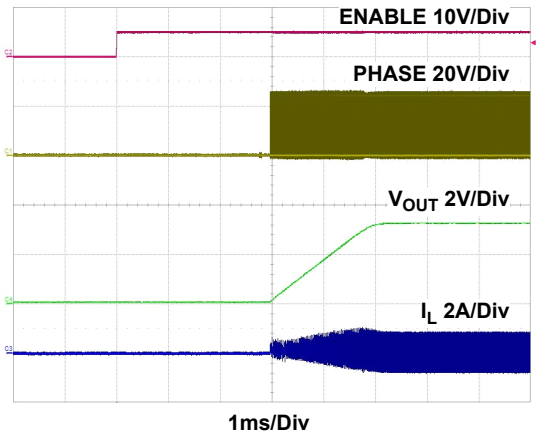



Figure 27. Start-Up through EN, $I_{OUT}$ = 0A

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.(Cont.)

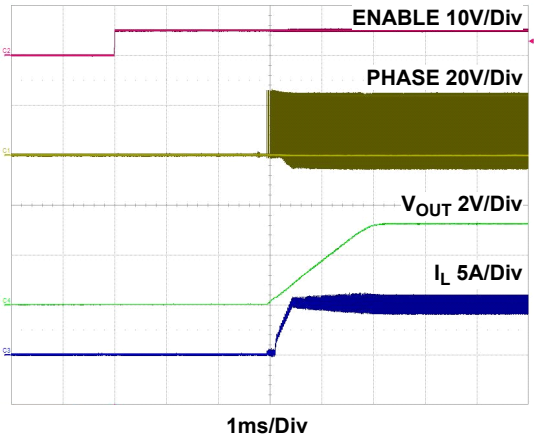



Figure 28. Start-Up through EN, $I_{OUT}$ = 5A

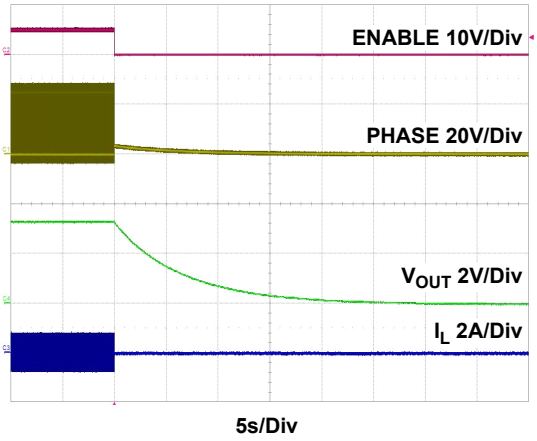



Figure 29. Shutdown through EN, $I_{OUT}$ = 0A

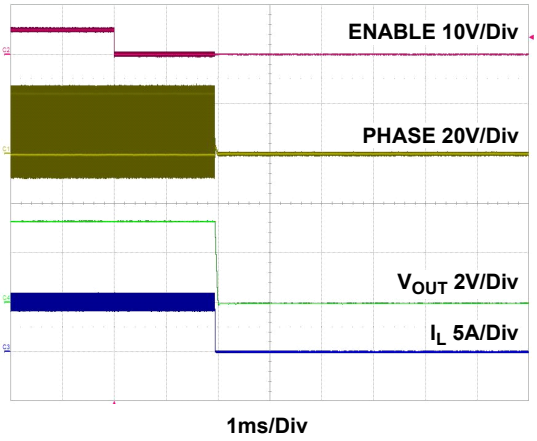



Figure 30. Shutdown through EN, $I_{OUT}$ = 5A

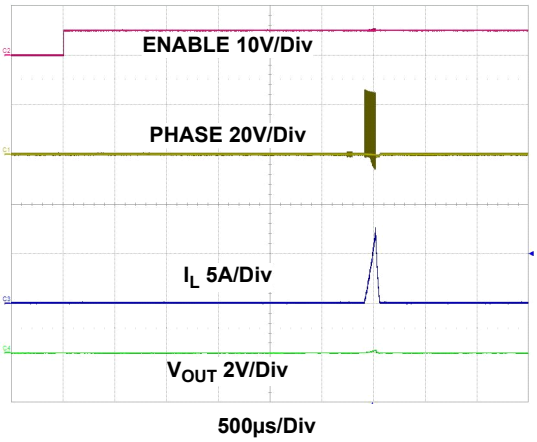



Figure 31. Start-Up with $V_{OUT}$ Short-Circuit

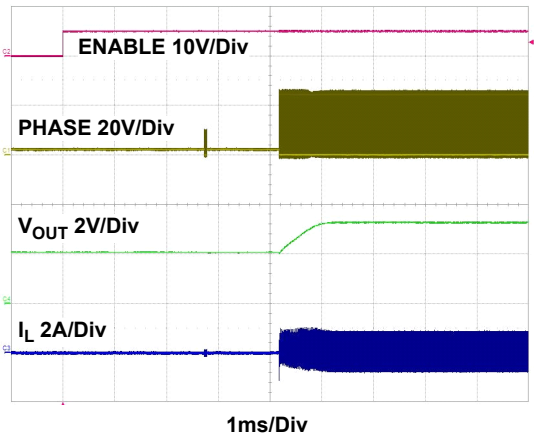



Figure 32. Start-Up with $V_{OUT}$ Pre-Biased to 2V

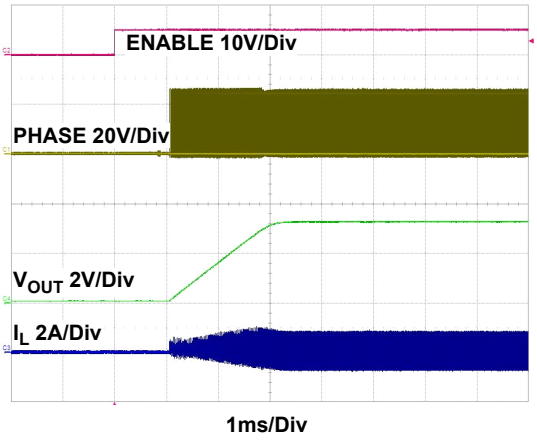



Figure 33. Start-Up without Delay (V3DLY = AVCC)

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.(Cont.)

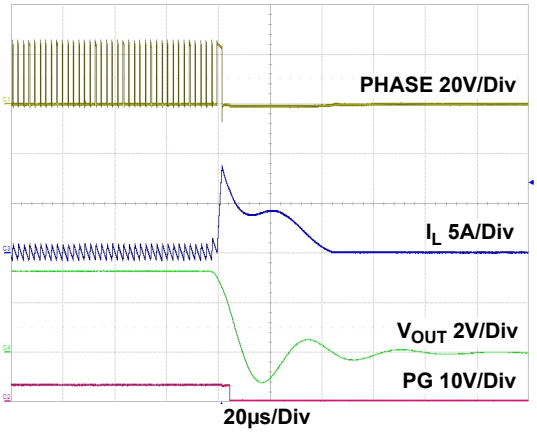



**Figure 34. $I_{OUT}$ = 0A to Short-Circuit (High-Side Overcurrent Protection)**

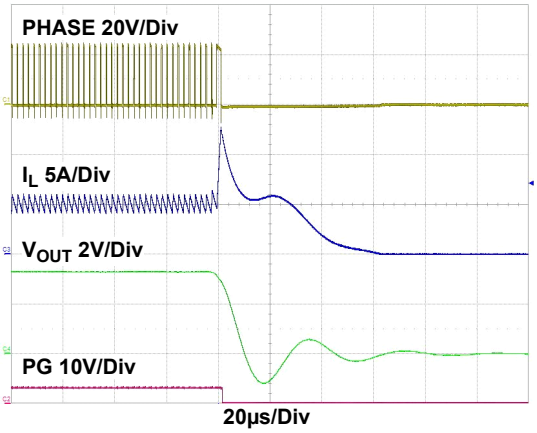



**Figure 35. $I_{OUT}$ = 5A to Short-Circuit (High-Side Overcurrent Protection)**

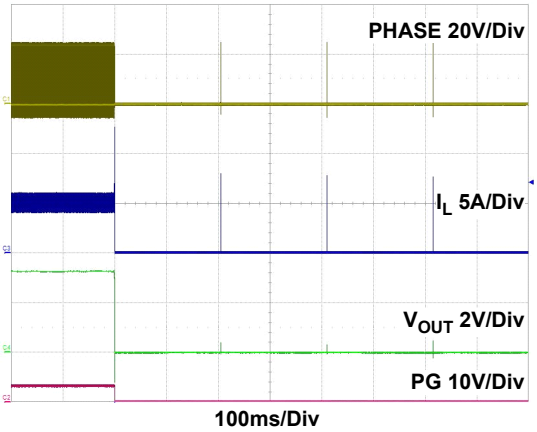



**Figure 36. Hiccup after Output Short-Circuit**

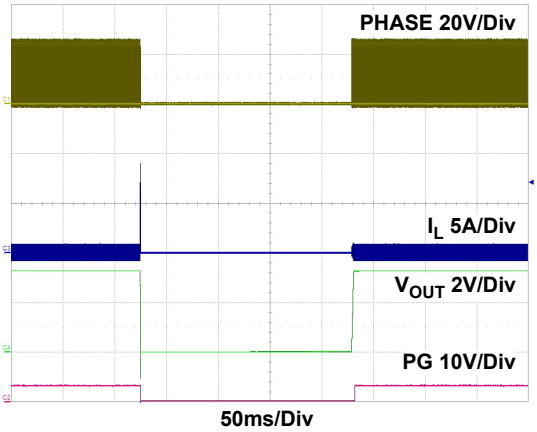



**Figure 37. $I_{OUT}$ = 0A to Short-Circuit to 0A Recovery**

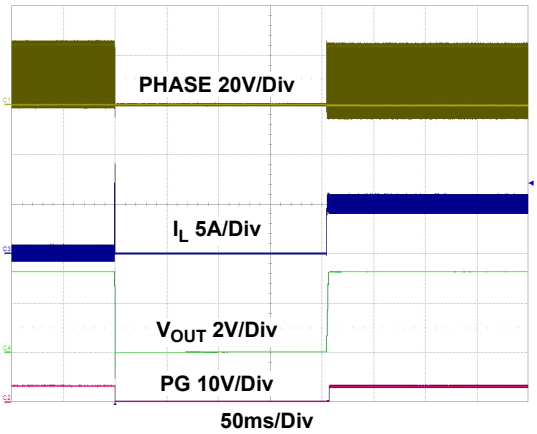



**Figure 38. $I_{OUT}$ = 0A to Short-Circuit to 5A Recovery**

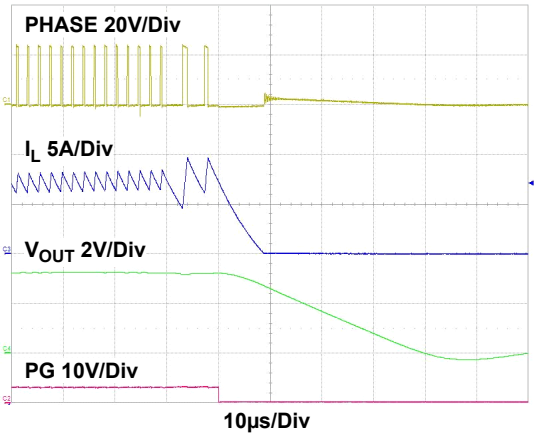



**Figure 39. Low-Side Overcurrent (LSOC) Protection**

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.(Cont.)

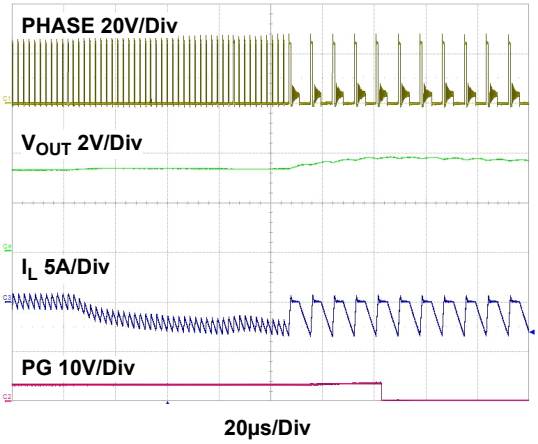



Figure 40. Negative Overcurrent (NOC) Protection

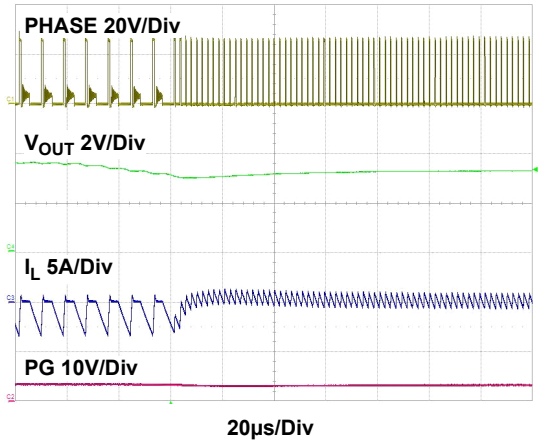



Figure 41. Recovery from Negative Overcurrent (NOC) Protection

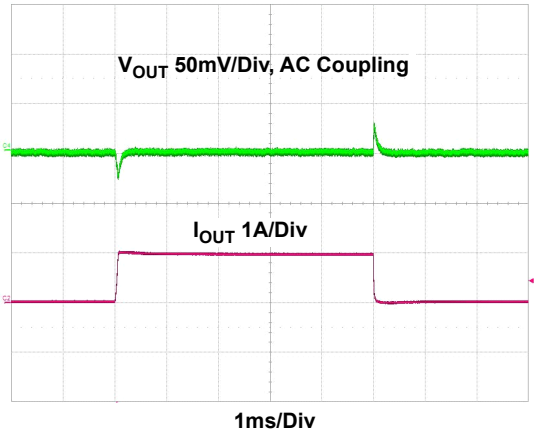



Figure 42. Load Transient $I_{OUT}$ = 0A -> 1A -> 0, Slew Rate 0.5A/µs

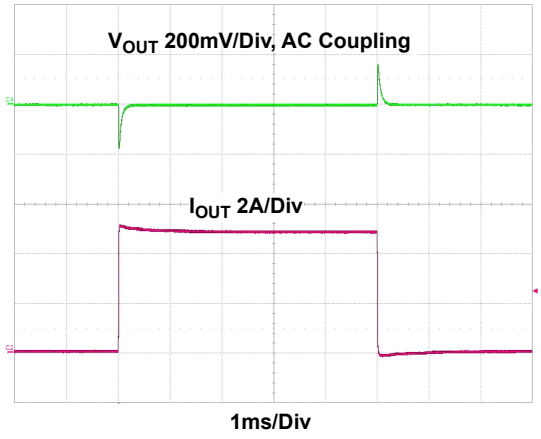



Figure 43. Load Transient $I_{OUT}$ = 0A -> 5A -> 0A, Slew Rate 0.5A/µs

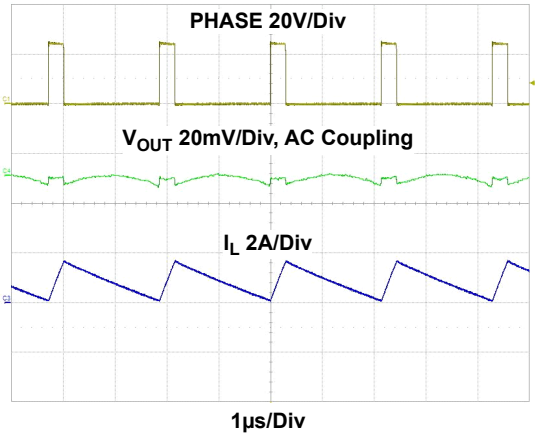



Figure 44. Output Voltage Ripple at $I_{OUT}$ = 1A

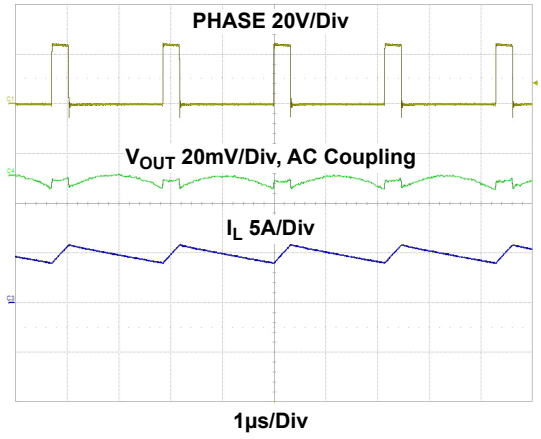



Figure 45. Output Voltage Ripple at $I_{OUT}$ = 5A

PVIN = 24V, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz, L = 3.3µH, $C_{OUT}$ = 80µF, $R_{SET}$ = 30.1kΩ, $T_A$ = +25°C, internal compensation, internal soft-start unless otherwise stated.(Cont.)

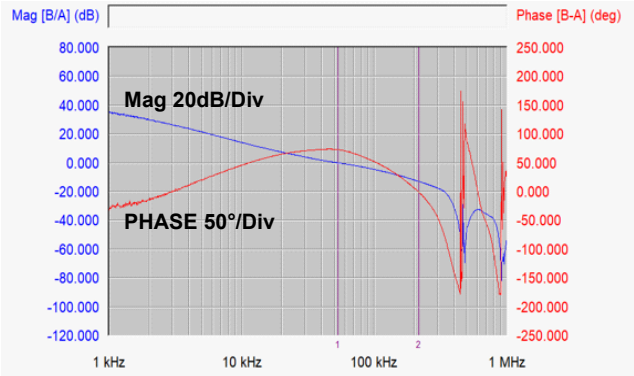



Figure 46. Loop Gain at $I_{OUT}$ = 3A

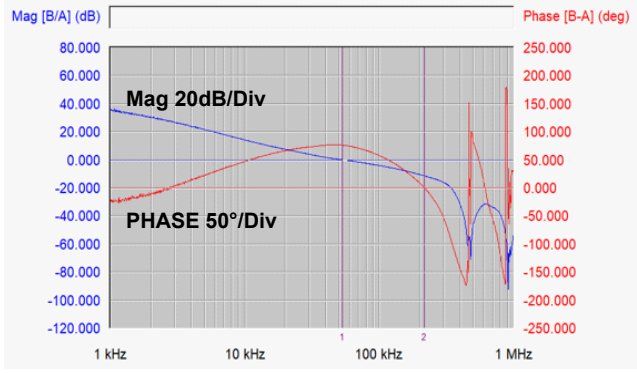



Figure 47. Loop Gain at $I_{OUT}$ = 5A

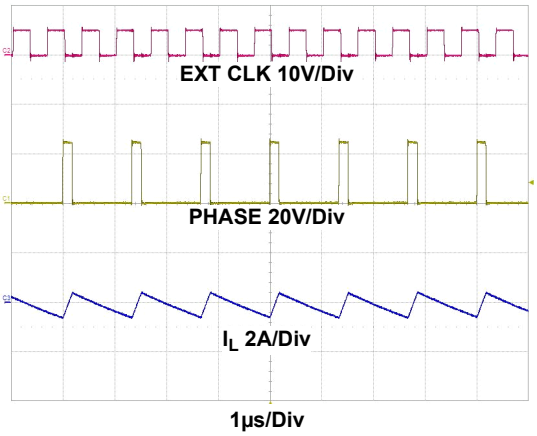



Figure 48. External Clock Synchronization, EXT CLK Frequency = 1.5MHz

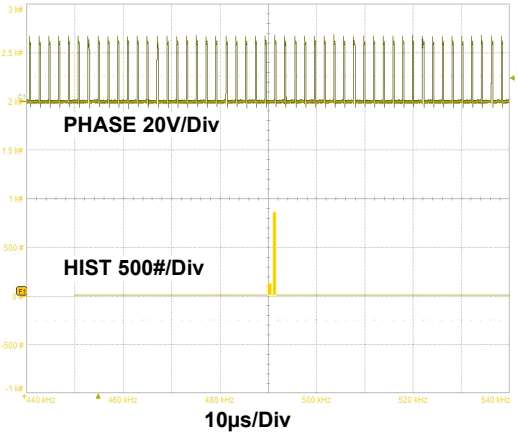



Figure 49. Phase Histogram with No Spread Spectrum (MODE/SYNC = GND)

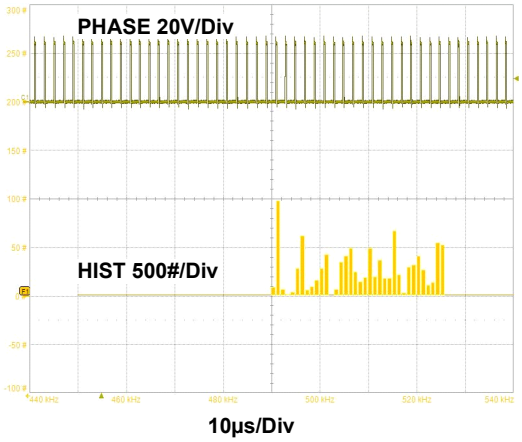



Figure 50. Phase Histogram with Spread Spectrum (MODE/SYNC = AVCC)

# 5. Functional Description

The RAA211650 is a high efficiency integrated synchronous buck regulator. It can operate across a wide input voltage range from 4.5V to 60V delivering load current up to 5A across the -40°C to 125°C temperature range. It has a built-in internal feedback option preset for 3.3V output. The regulator works with fixed frequency pulse width modulation at all loads. Though it is a fixed frequency operation, the IC has the option to dither its switching frequency around the preset switching frequency based on an internal spread spectrum scheme. The regulator works with inductor current always in Continuous Conduction Mode (CCM). The current control architecture is based on Valley Current Sampling (VCS). It is possible to support high input voltage to low output voltage conversion ratios at high switching frequencies using the VCS method because it allows for short on-time pulses. Pulses can be as short as 45ns.

Figure 51 shows the functional block diagram for RAA211650. The output voltage is sensed by a resistor divider from $V_{OUT}$ to the FB pin. An internal transconductance error amplifier (EA) compares FB voltage with the internal 0.8V reference voltage and produces an amplified compensated signal COMP to minimize the error in $V_{OUT}$. The EA has internal compensation, which provides stable operation across the device operating range. EA uses internal compensation when COMP is connected to AVCC. An external RC network can be between the COMP pin and AGND to use external compensation. The COMP signal is compared with the sum of sensed low-side current and the slope compensation generator. At the rising edge of the PWM clock, the high-side MOSFET turns on ramping up the inductor current. The high-side MOSFET is turned off when the sum of the sampled low-side current and compensation generator reaches the COMP signal level or when the maximum duty cycle is reached. When the high-side MOSFET is turned off, the inductor current starts to ramp down initially freewheeling through the low-side MOSFET body diode. After a small dead time, the low-side MOSFET is turned on and the inductor current shifts from the body diode to the low-side MOSFET channel. During each switching cycle when the high-side MOSFET is turned on, the inductor stores the energy, and it is delivered to load when it is turned off. The resistor RT sets the switching frequency for the regulator.

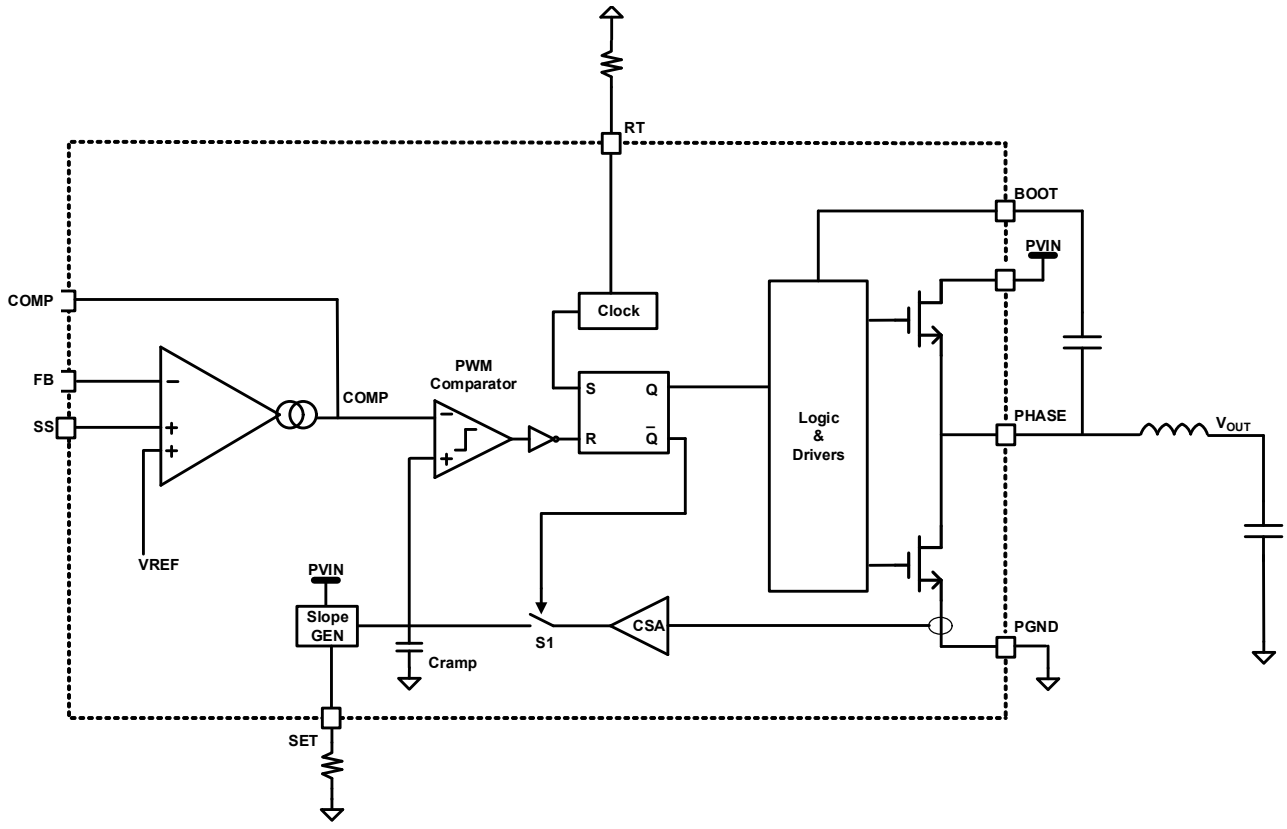



**Figure 51. PWM Fixed Frequency Functional Block Diagram**

In traditional peak current mode control, the PWM comparator compares the inductor upslope signal ($V_{IN}$-$V_{OUT}$)/L with the slope compensation signal, which is typically $V_{OUT}$/L. However, in applications where input voltage can be quite high and short on-time pulses are required, sampling the upslope inductor current can be difficult. Therefore, the RAA211650 adopts a VCS mechanism to overcome this challenge. In VCS, the valley current is sampled and used in the peak current mode modulation scheme. Generate an artificial ramp that replaces the sensed inductor current upslope and slope compensation signal to mimic peak current mode operation. Therefore, the slope of the artificial ramp signal is shown in Equation 1.

**(EQ. 1)** $$\frac{dV}{dt} = R_{CSA}\frac{V_{IN} - V_{OUT}}{L} + R_{CSA}\frac{V_{OUT}}{L} = R_{CSA}\frac{V_{IN}}{L}$$

where the current sense gain $R_{CSA}$ equals 60mV/A.

During low-side MOSFET conduction, S1 is closed and the CRAMP voltage represents the down-sloping valley current. As soon as the clock sets the RS flip-flop, the switch opens, and the slope generator forces current into CRAMP, which is 3pF. This creates an artificial slope that is adjusted by the SET resistor. When the voltage on CRAMP reaches the COMP voltage, the PWM comparator trips and resets the flip-flop, which turns on the low-side MOSFET again, and the regulator waits for the clock signal to the start next cycle.

The regulator has an internal spread spectrum generator. The resistor on RT sets the base PWM switching frequency. Spread spectrum operation is configured by the SYNC/MODE pin. If the SYNC/MODE pin is connected to AVCC, the spread spectrum feature is enabled. If it is connected to AGND, PWM switches at a constant frequency set by the resistor on RT. Figure 52 shows the flow chart for the different possible PWM modes. SYNC/MODE can also be connected to an external clock signal. The external clock signal is divided by half internally and the internal PWM clock synchronizes to the divided external clock signal provided it is 10% above the base switching frequency set by the RT pin. Figure 52 also shows the logic for internal and external compensation.

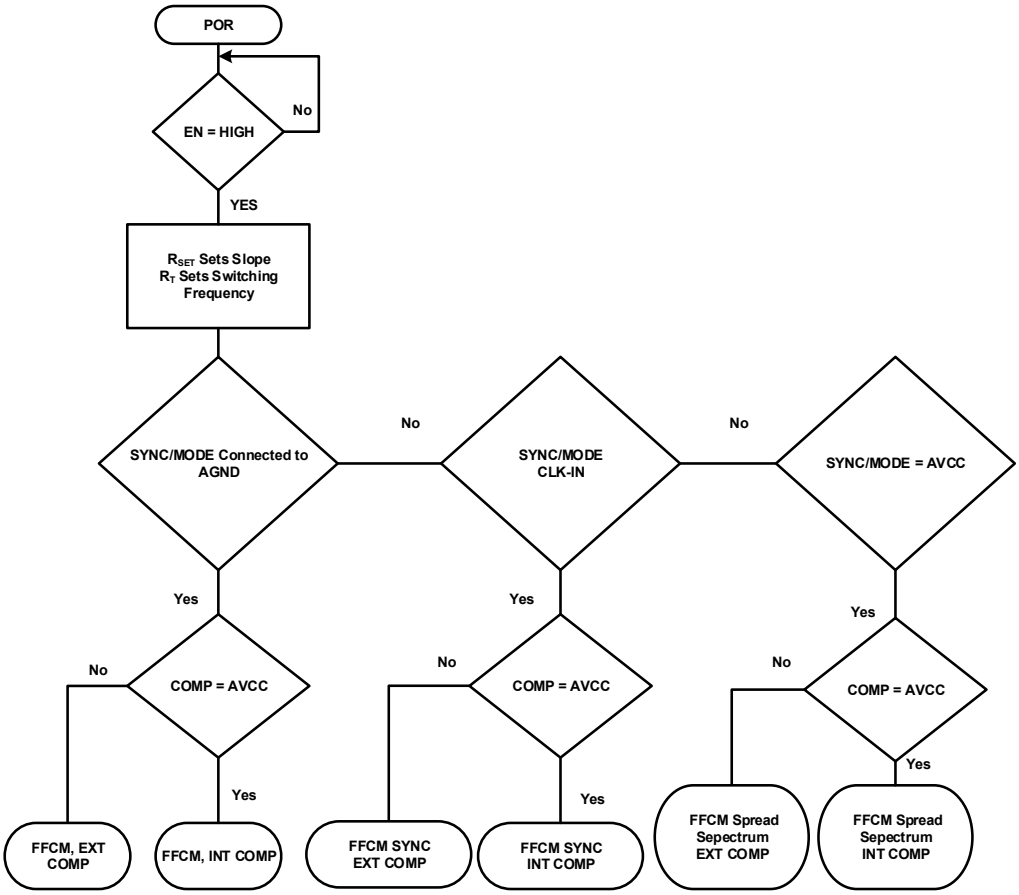



**Figure 52. Different Modes of Operation**

## 5.1 Supported Output Voltage Range

RAA211650 is capable of a low minimum off time, typical 265ns. This allows for high duty cycle operation to regulate high VOUT. Considering the variation on the minimum off time, Figure 53, shows the maximum possible VOUT for three different switching frequencies. At 2.5MHz, with PVIN of 60V, it is possible to get VOUT up to 15.75V while with lower switching frequency higher VOUT is possible. Equation 2 can be used to find the possible maximum VOUT for a selected PVIN and switching frequency.

**(EQ. 2)** $$VOUT_max = (1 - t_{min_off_time} \times f_{SW}) \times PVIN$$

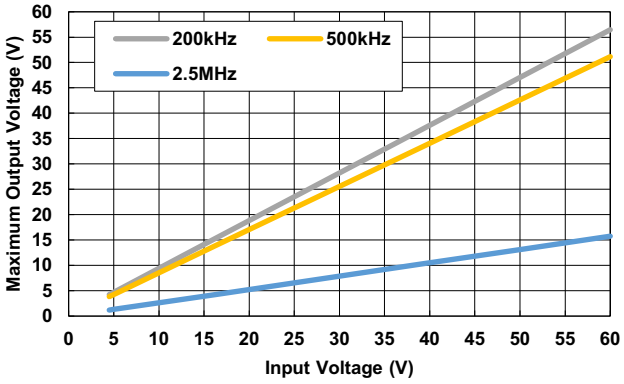



**Figure 53. Maximum Output Voltage Supported vs Input Voltage for Various $f_{SW}$ Values**

RAA211650 has a small minimum on time, typical 45ns. Also, the output voltage cannot be smaller than the feedback reference voltage of 0.8V. Therefore, for a switching frequency and input voltage, the minimum possible output voltage is calculated using Equation 3.

**(EQ. 3)** $$VOUT_min = max(0.8, t_{min_on_time} \times f_{SW} \times PVIN)$$

Figure 54 shows possible minimum output voltage plots for three switching frequencies for the PVIN range.

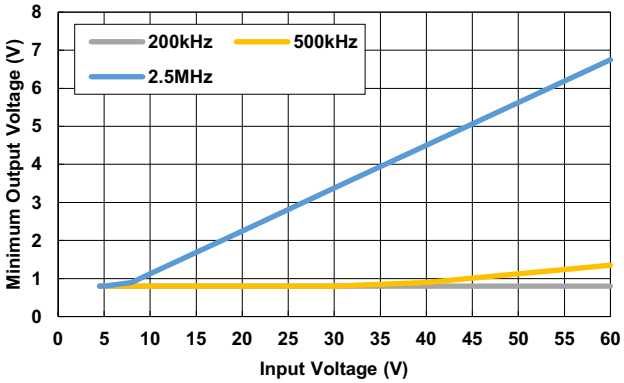



**Figure 54. Minimum Output Voltage Supported vs Input Voltage for Various $f_{SW}$ Values**

To regulate the selected $V_{OUT}$ and proper operation of the regulator, the output inductor, capacitor, and SET resistor must be appropriately selected. Renesas recommends using the design spreadsheet to calculate the component values.

## 5.2 Soft-Start

The RAA211650 has a soft-start (SS) function that provides a ramp reference to the input of the error amplifier. Soft-start prevents high inrush current or output voltage overshoot at startup.

The soft-start ramp can be generated either internally or by an external capacitor on the SS pin. When this pin is tied to AVCC, the SS time is internally set to 2ms. Programmable soft-start is implemented by connecting a capacitor from the SS pin to AGND. SS sources 5µA during soft-start. The SS capacitor is calculated using Equation 4:

**(EQ. 4)** $C_{SS}[nF] = 6.25t_{SS}[ms]$

where $t_{ss}$ is the soft-start time in milliseconds.

When the SS ramp is lower than the 0.8V internal bandgap-referenced voltage, the error amplifier uses the SS voltage as the reference. When it reaches 0.8V, the bandgap-referenced voltage takes over. PGOOD is asserted when SS reaches 1.2V.

## 5.3 Delay

The delay function adds a delay time before the onset of soft-start and shutdown such that the output rail does not ramp up or down before the delay time expires. The time can be set by a capacitor connected between the V3_DLY pin and ground. The capacitor is charged by a 5µA current source at the V3_DLY pin and the delay time is set using Equation 5:

**(EQ. 5)** $C_{DELAY}[nF] = 4.17t_{DELAY}[ms]$

The delay time starts when the EN logic goes high or low. It is complete when the voltage on the capacitor reaches 1.2V, on which ramping of soft-start or shutdown happens. The timing diagram in Figure 55 illustrates the sequence of signals in an EN triggered power up or power down event.

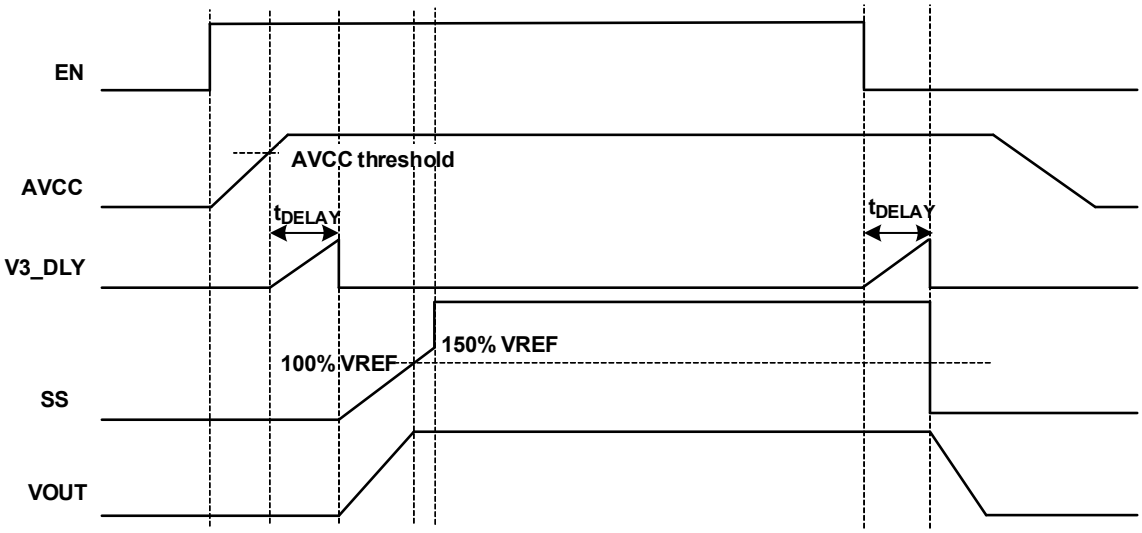



**Figure 55. Delay Function**

The delay function ensures proper power sequencing of two or more supplies. For example, if $V_{OUT1}$ needs to come up before $V_{OUT2}$ and come down after $V_{OUT2}$, and the PG signal of the first buck regulator is used as the EN signal for the second one, the delay time set in the first regulator produces the correct power-up/down sequence of the two outputs as can be seen in Figure 56 (ignoring delay for the second regulator).

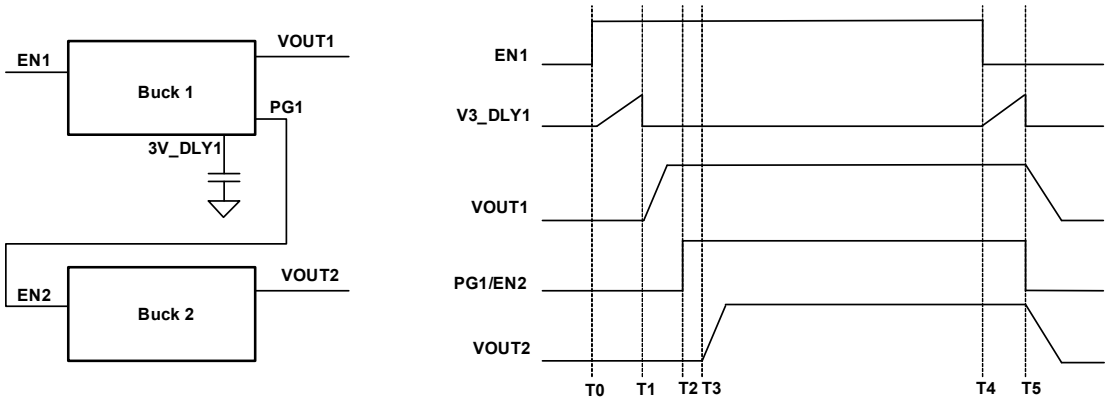



**Figure 56. Delay Function Sequencing Power Supplies with Delay Function**

## 5.4 Power-Good

The RAA211650 provides a power-good (PG) signal that indicates the output voltage is within a specified tolerance of its target level, and a no-fault condition exists. The PG pin is the open drain of a MOSFET. For logic level output voltages, connect it to a voltage source through a pull-up resistor. At power-on, the PG signal is held low before SS is ready, and it is asserted when the SS voltage reaches 1.2V, and FB voltage is within the regulation window. When the FB voltage goes 12% below or 12% above the nominal value, PG is pulled low, as shown in Figure 57. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start.

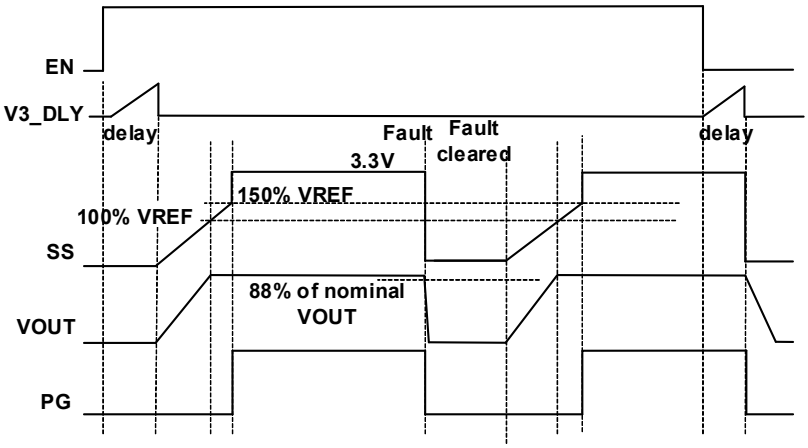



**Figure 57. Power-Good Signal**

## 5.5 RT Switching Frequency

The resistor connected from the RT pin to AGND can program the switching frequency from 200kHz to 2.5MHz. Figure 58 shows the relationship between the RT resistor and switching frequency. Use Equation 6 to calculate the RT resistor value for a given switching frequency.

**(EQ. 6)** $$RT[k\Omega] = \frac{120258}{f_{SW}^{1.044}(kHz)}$$

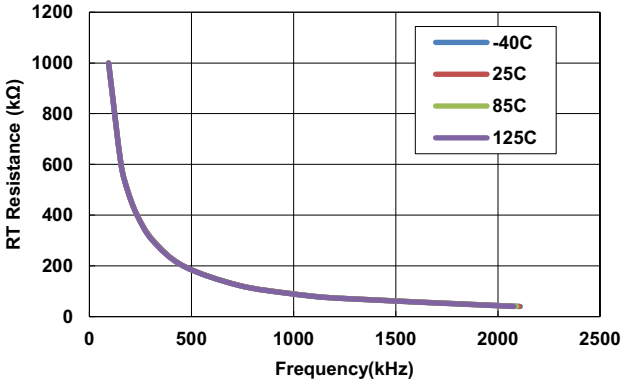



**Figure 58. RT Resistor vs Switching Frequency**

## 5.6 Bias Supply PVCC, AVCC

The regulator has two internal LDOs to generate the 3.3V analog bias power supply. One LDO is connected to VIN and the other LDO is connected to EBIAS. The regulator starts up with the LDO on VIN and switches to the EBIAS LDO if EBIAS voltage is in the 3V to 12V range. The output of the internal LDOs is connected to the PVCC pin. A 2.2µF ceramic capacitor is recommended for decoupling PVCC. AVCC can be generated from PVCC. An RC filter is recommended to keep AVCC is clean. If $V_{OUT}$ is set to 3.3V, connecting EBIAS to $V_{OUT}$ and using the EBIAS LDO results in better overall efficiency.

## 5.7 Pre-Biased Output

The regulator supports the pre-biased start up. When the device starts up into a pre-biased condition, both high-side and low-side MOSFETs are turned off to prevent sinking or sourcing the current into the load. The switching only starts when the output voltage has risen to a pre-biased level or when the soft-start is over.

## 5.8 High-Side Overcurrent (HSOC) Protection

After the regulator starts up, if the current through the internal high-side MOSFET is over 200% of the maximum output current, both the high-side and low-side MOSFETs are turned off. The regulator enters Hiccup mode with a 200ms period. When the high-side MOSFET current is less than 200% of the maximum output current and there are no other faults, the regulator resumes normal operation.

## 5.9 Low-Side Overcurrent (LSOC) Protection

After the regulator starts up, if the current through the internal low-side MOSFET is over the current limit, the device skips the high-side cycles until the LSOC condition clears. A counter monitors the number of cycles skipped. If three cycles are skipped within eight cycles, an LSOC fault is registered. The regulator stops switching and enters Hiccup mode with a 200ms period. When the overcurrent condition has cleared, and there are no other faults, the regulator resumes normal operation.

## 5.10 Low-Side Negative Overcurrent Protection

After the regulator starts up, if the negative current in the low-side MOSFET exceeds the negative current limit, the low-side negative overcurrent protection is latched. The regulator turns off the low-side MOSFET and turns on the high-side MOSFET until the high side current cross zero. Both MOSFETs are then tri-stated until the next PWM clock cycle, and normal operation resumes.

## 5.11 Output Overvoltage Protection

After soft-start completes and the FB voltage is in the regulation range, the PG signal goes high. If the voltage detected on the FB pin is over 120% of the reference voltage, overvoltage protection is activated after a 1µs to 2µs delay time and the regulator enters Hiccup mode with a 200ms period. When the FB voltage is lower than 120% of the reference voltage, the regulator resumes normal operation.

## 5.12 Output Undervoltage Protection

If the voltage detected on the FB pin is below 70% of the reference voltage, and LSOC is also detected, undervoltage protection is activated and the regulator enters hiccup mode with a 200ms period. When the FB voltage is higher than 70% of the reference voltage and the LSOC condition has cleared, the regulator resumes normal operation. **Note:** Both low FB voltage and an LSOC condition are required to trigger the output undervoltage protection fault. Simply having FB lower than 70% of the reference voltage does not trigger a fault.

## 5.13 PVIN UVLO and Enable

The regulator has UVLO on PVIN. The PVIN rising threshold is 4.15V, while the falling threshold is 3.85V. The regulator switches on when the input voltage rises above 4.15V and switches off when it falls below 3.85V. The UVLO set point is programmed through a resistor divider between PVIN and EN, as shown in Figure 59. The resistor values are calculated using Equation 7.

**(EQ. 7)** $$R_{EN1} = R_{EN2}\left(\frac{PVIN_{UVLO}}{V_{ENTH}} - 1\right)$$

where $PVIN_{UVLO}$ is the desired PVIN UVLO level and $V_{ENTH}$ is the EN threshold, which is 1.5V for rising and 1.375V for falling.

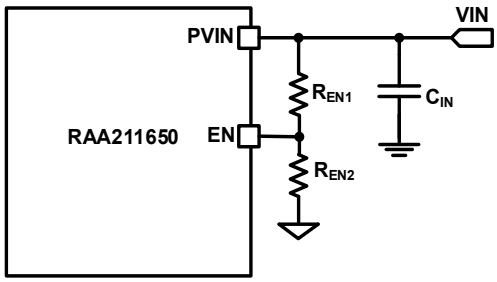



**Figure 59. PVIN UVLO using EN**

## 5.14 Over-Temperature Protection

Over-temperature protection (OTP) limits the maximum junction temperature in the RAA211650. After PG is asserted, if the junction temperature reaches 153°C (typical), the regulator is shut down and PG is held low during this time. There is a 30°C hysteresis for OTP. After the junction temperature drops below 123°C, the RAA211650 resumes operation by stepping through soft-start.

## 5.15 AVCC Undervoltage Protection

RAA211650 has undervoltage lockout protection on AVCC to prevent the regulator from operation with insufficient bias voltage. The AVCC UVLO comparator monitors the AVCC voltage and if it goes below 2.7V, the regulator switches off. It starts up with the normal startup sequence when the AVCC voltage is over 2.9V.

# 6. Application Information

## 6.1 Design Examples

The regulator is designed for the following specifications

**Table 1. Regulator Specifications**

| Parameter | Symbol | Values |
|---|---|---|
| Input Voltage Range | $V_{IN}$ | 24V |
| Output voltage | $V_{OUT}$ | 3.3V |
| Switching frequency | $f_{SW}$ | 500kHz |
| Maximum inductor current ripple | $I_{ripplemax}$ | 50% |
| Maximum Output capacitor voltage ripple | $V_{ripplemax}$ | 5% |
| Maximum output current | $I_{OUTmax}$ | 5A |

### 6.1.1 Design Example 1

The first design example uses the internal compensation, internal soft-start, and internal feedback. The application circuit is shown in Figure 60.

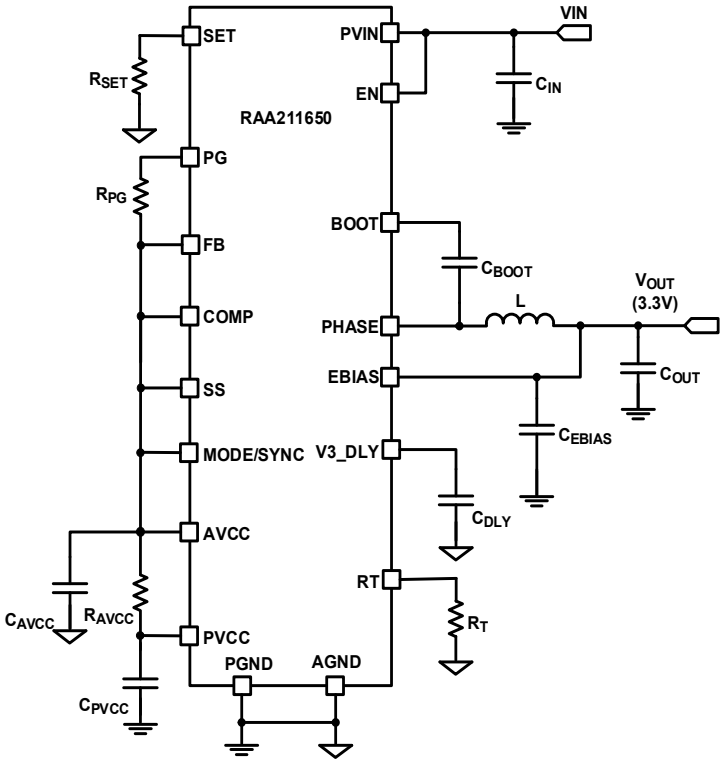



**Figure 60. Application Circuit for Design Example 1**

From the design specification given in Table 1, the maximum inductor current ripple and output voltage ripple are shown in Equation 8 and Equation 9.

**(EQ. 8)** $$\Delta I_{max} = I_{ripplemax} \times I_{OUTmax} = 0.5 \times 5 = 2.5A$$

**(EQ. 9)** $$\Delta V_{OUTmax} = V_{ripplemax} \times V_{OUT} = 0.05 \times 3.3 = 0.165V$$

The design of the inductor depends on the operating frequency, load current, ripple current, output voltage, and input voltage. To keep the design simple for buck converters with a wide input voltage range operating in the Continuous Conduction Mode (CCM), the minimum value of the inductor required is determined using Equation 10.

**(EQ. 10)** $$L_{min} \approx \frac{V_{OUT}}{\Delta I_{max} f_{sw}} = \frac{3.3}{2.5 \times 500 \times 10^3} = 2.64\mu H$$

Select an inductor with a value greater than $L_{min}$. The nearest standard value of 3.3µH is used. The maximum ripple expected with this inductor is shown in Equation 11.

**(EQ. 11)** $$I_{ripplemaxact} = \frac{V_{OUT}(1-D)}{L \times f_{SW}} = \frac{3.3\left(1-\frac{3.3}{24}\right)}{3.3 \times 10^{-6} \times 500 \times 10^3} = 1.725A$$

The peak inductor current is $I_{Lpeak} = I_{OUTmax} + 0.5 \times I_{ripplemaxact} = 5 + 0.863 = 5.863A$

**Note:** To prevent magnetic core saturation, the L selected must have a peak current rating greater than 5.863A. Also, the inductor must have an RMS current rating greater than $I_{OUTmax}$. Selecting an inductor with a conservative current rating results in a bulky inductor.

The output capacitor filters the inductor current ripple and delivers a smooth DC voltage to load. It has to ensure that converter operates stably in all operating conditions with acceptable voltage ripple during load transients. Therefore, the selection of $C_{OUT}$ considers the closed loop unity gain crossover frequency, voltage overshoot, and voltage undershoot requirements during load transient. The $C_{OUT}$ selected should be the largest of all three so that all criteria are met.

**(EQ. 12)** $$C_{OUT} = \max(C_{Linear}, C_{OUT_MIN_STEP_DOWN}, C_{OUT_MIN_STEP_UP})$$

Let $F_T$ be the unity gain crossover frequency and $F_{ratio}$ is $F_T/f_{SW}$. Assuming $F_{ratio} = 0.1$, the output capacitor required is:

**(EQ. 13)** $$C_{Linear} = \frac{V_{REF} G_{mEA} R_{COMP}}{2\pi F_T V_{OUT} R_{CSA}} = \frac{V_{REF} G_{mEA} R_{COMP}}{2\pi F_{ratio} f_{SW} V_{OUT} R_{CSA}} = \frac{0.8 \times 14 \times 10^{-6} \times 0.5 \times 10^6}{2\pi \times 0.1 \times 500 \times 10^3 \times 3.3 \times 60 \times 10^{-3}} = 90.02\mu F$$

With a load step $I_{step}$ = 1A, output capacitance required to keep the overshoot within limit during load step down is:

**(EQ. 14)** $$C_{OUT_MIN_STEP_DOWN} = \frac{L\left(I_{step} + \frac{I_{ripplemaxact}}{2}\right)^2}{2V_{OUT}\Delta V_{OUT_max}} = \frac{3.3 \times 10^{-6} \times (1+0.863)^2}{2 \times 3.3 \times 0.165} = 10.5\mu F$$

With the load step up, the output capacitance required to keep the undershoot within specification is:

**(EQ. 15)** $$C_{OUT_MIN_STEP_UP} = \frac{L\left(I_{step} + \frac{I_{I_{ripplemaxact}}}{2}\right)^2}{2(V_{IN}-V_{OUT})\Delta V_{OUT_max}} = \frac{3.3 \times 10^{-6} \times (1+0.863)^2}{2 \times (24-3.3) \times 0.165} = 1.68\mu F$$

Therefore, a $C_{OUT}$ of 100µF is selected.

$R_{SET}$ is used in ramp generation that is used for slope compensation. Its value is calculated using Equation 16.

**(EQ. 16)** $$R_{SET} = \frac{L}{C_{ramp} \times k_{ratio} \times k_{mirror} \times R_{CSA}} = \frac{3.3 \times 10^{-6}}{3 \times 10^{-12} \times 60 \times 10 \times 60 \times 10^{-3}} = 30.55k\Omega$$

With the calculated RSET, check the peak of the ramp. Renesas recommends keeping the peak of the ramp at least 100mV. If required, reduce the RSET to achieve this. The peak of the ramp is calculated using Equation 17.

**(EQ. 17)** $$V_{ramp_peak}(mV) = \frac{V_{OUT}}{(C_{ramp} \times k_{ratio} \times k_{mirror} \times R_{SET} \times f_{SW})} \times 1000 = \frac{3.3}{(3 \times 10^{-12} \times 60 \times 10 \times 30.55 \times 10^{3} \times 500 \times 10^{3})} \times 1000 = 120mV$$

The resistor $R_T$ programs the PWM clock, which is calculated using Equation 18.

**(EQ. 18)** $$R_T = \frac{120258}{f_{SW}^{1.044}} = \frac{120258}{(500)^{1.044}} = 182.97k\Omega$$

Because, the switching frequency for this design is 500kHz it can also be achieved by pulling the RT pin to AVCC.

For this example, we designed for a delay of 1ms from the time ENABLE goes high to the time the regulator starts switching, the delay capacitor is calculated using Equation 19.

**(EQ. 19)** $$C_{DLY}(nF) = 4.17T_{DELAY}(ms) = 4.17 \times 2 = 8.34nF$$

$C_{BOOT}$ provides the gate drive voltage for the high-side MOSFET. For this design example, we designed for 0.1V drop-on boot voltage each time $C_{BOOT}$ supplies charge to the high-side MOSFET, the required $C_{BOOT}$ is shown in Equation 20.

**(EQ. 20)** $$C_{BOOT} \approx \frac{Q_{gHS}}{\Delta V_{BOOT}} = \frac{10 \times 10^{-9}}{0.1} = 100nF$$

where $Q_{gHS}$ is typical gate charge value for high-side MOSFET.

The input capacitor $C_{IN}$ provides a low impedance voltage source for the regulator. It minimizes input voltage ripple and supplies the pulsating current drawn by the regulator. The minimum input capacitance required to achieve $\Delta V_{INMAX}$ is shown in Equation 21.

**(EQ. 21)** $$C_{INMIN} = \frac{1.5 \times I_{out_max} \times 0.25}{\Delta V_{INMAX} f_{SW}} = \frac{1.5 \times 5 \times 0.25}{0.05 \times 500 \times 10^{3}} = 75\mu F$$

Where 1.5 is a factor used for safety margin. The rms current of the input capacitor is calculated using Equation 22.

**(EQ. 22)** $$I_{CIN_rms_maz} = \frac{1.5 \times I_{out_max}}{2} = \frac{1.5 \times 5}{2} = 3.75A$$

Use an electrolytic capacitor of 68µF rated for input voltage. Place four 10µF ceramic capacitors in parallel and close to the IC input pins.

Renesas recommends using a 1Ω filter resistor for $R_{AVCC}$ between PVCC and AVCC. Capacitances $C_{PVCC}$ = 2.2µF and $C_{AVCC}$ = 1µF are also recommended. If the PG pin monitors PGOOD signal, Renesas recommends pulling this pin to AVCC using a 100kΩ resistor.

### 6.1.2 Design Example 2

The second design example implements using an external compensation, external soft-start, and external feedback. The application circuit is shown in Figure 61.

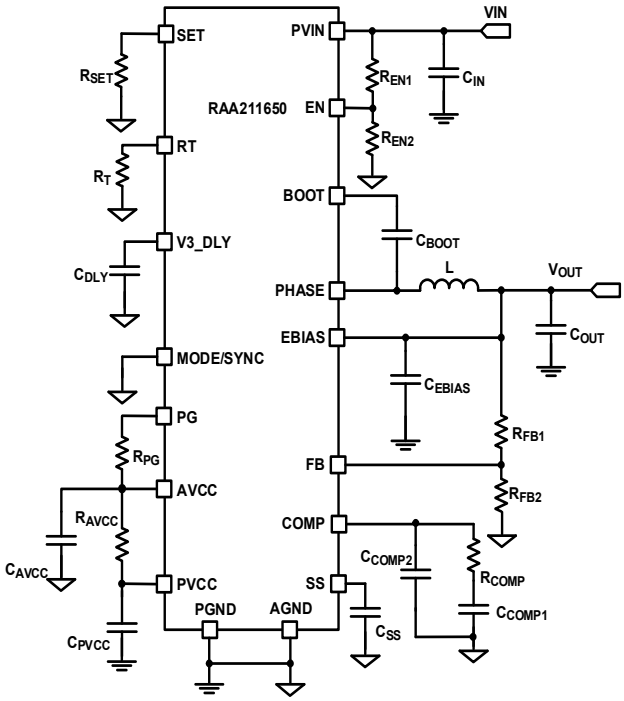



**Figure 61. Application Circuit for Design Example 2**

The calculation of L, $C_{OUT_MIN_STEP_DOWN}$, $C_{OUT_MIN_STEP_UP}$, $R_{SET}$, $R_T$, $C_{DLY}$, $C_{BOOT}$, $C_{IN}$ are the same as in Example 1 and are not repeated here.

The ripple on $V_{OUT}$ is 5%, considering the tolerances the compensation has to be designed targeting a much smaller ripple. Let us assume 1% ripple for a change of 1A load current. The $R_{COMP}$ is shown in Equation 23.

**(EQ. 23)**
$$R_{COMP} = \frac{V_{OUT}R_{CSA}}{V_{REF}G_{m_{EA}}\frac{\Delta V_{OUT}}{\Delta I_{OUT}}} = \frac{3.3 \times 60 \times 10^{-3}}{0.8 \times 2 \times 10^{-3} \times \frac{0.033}{1}} = 3.75k\Omega$$

Assuming $F_{ratio}$ = 0.1 and $F_z$ is 1/10 of $F_T$, the compensation capacitor is shown in Equation 24.

**(EQ. 24)**
$$C_{COMP1} = \frac{1}{2\pi F_z R_{COMP}} = \frac{1}{2\pi \times 5 \times 10^3 \times 3.75 \times 10^3} = 8.5nF$$

The error amplifier gain for external compensation is 2mS. The output capacitor required is shown in Equation 25.

**(EQ. 25)**
$$C_{Linear} = \frac{V_{REF}G_{m_{EA}}R_{COMP}}{2\pi F_T V_{OUT}R_{CSA}} = \frac{V_{REF}G_{m_{EA}}R_{COMP}}{2\pi F_{ratio}f_{SW}V_{VOUT}R_{CSA}} = \frac{0.8 \times 2 \times 10^{-3} \times 3.75 \times 10^3}{2\pi \times 0.1 \times 500 \times 10^3 \times 3.3 \times 60 \times 10^{-3}} = 96.5\mu F$$

Considering the previous $C_{Linear}$ and the $C_{OUT_MIN_STEP_DOWN}$ and $C_{OUT_MIN_STEP_UP}$ from the first design, $C_{OUT}$ of 100µF is selected.

To have a good feedback signal, feedback resistors in the range of a few tens of kΩ are recommended. With $R_{FB2}$ = 20kΩ in the feedback divider, $R_{FB1}$ is calculated using Equation 26.

**(EQ. 26)** $$R_{FB1} = R_{FB2} \times \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) = 20 \times \left( \frac{3.3}{0.8} - 1 \right) = 62.5\text{k}\Omega$$

Soft-start time is controlled by the $C_{SS}$ capacitor. For 1ms soft-start time, its value is shown in Equation 27.

**(EQ. 27)** $$C_{SS}(\text{nF}) = 6.25 T_{SS}(\text{ms}) = 6.25 \times 1 = 6.25\text{nF}$$

$R_{EN1}$ and $R_{EN2}$ can change the $V_{IN}$ UVLO level to a value higher than 4.25V. With $R_{E2}$ = 10kΩ and the part enabled when $V_{IN}$ reaches 6V, the required $R_{E1}$ is shown in Equation 28.

**(EQ. 28)** $$R_{EN1} = R_{EN2} \times \left( \frac{V_{IN_{UVLO}}}{V_{EN_{UVLO}}} - 1 \right) = 10 \times \left( \frac{6}{1.5} - 1 \right) = 30\text{k}\Omega$$

Renesas recommends using the design spreadsheet of the regulator to plot and verify the compensation values and check the gain and phase margins.

## 6.2 PCB Layout Guidelines

A good layout of the printed circuit board (PCB) is essential for proper functioning of the regulator. **Important:** Keep all traces carrying high di/dt currents short and wide. Also, the loops formed by such pulsed currents must be as small as possible. **Important:** Place the noise sensitive analog circuit components away from noise sources. To achieve proper functioning of the regulator, Renesas recommends following the layout guidelines.

- Place the ceramic input capacitor on the same PCB surface layer as the regulator and as close as possible to the pins. A small 0603 package ceramic bypass capacitor, close to the PVIN pin, is recommended.
- Place the ceramic AVCC capacitor on the same PCB surface layer as the regulator and as close as possible to the AVCC and AGND pins.
- Place the ceramic PVCC capacitor on the same PCB surface layer as the regulator and as close as possible to the PVCC and PGND pins.
- Add plenty of thermal vias under the exposed pad of the regulator for better heat dissipation.
- The copper area of the PHASE NODE should not be more than needed. Place the inductor close to regulator.
- Place an output capacitor close to the inductor.
- Route the output voltage feedback signal away from BOOST and PHASE.
- Keep $R_{SET}$ close to the SET pin. Avoid running other analog signals close to the SET pin or $R_{SET}$ resistor.
- Keep feedback resistors close to FB pin.

The recommended PCB board layout example is shown in Figure 62 through Figure 65.

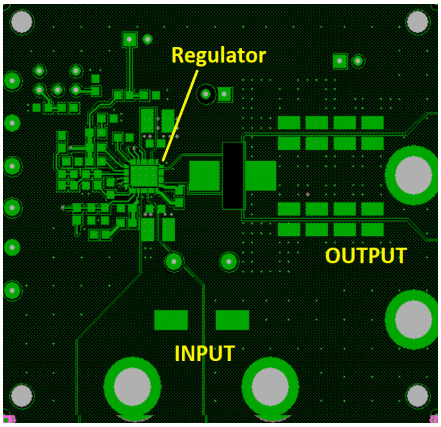



Figure 62. Top Layer

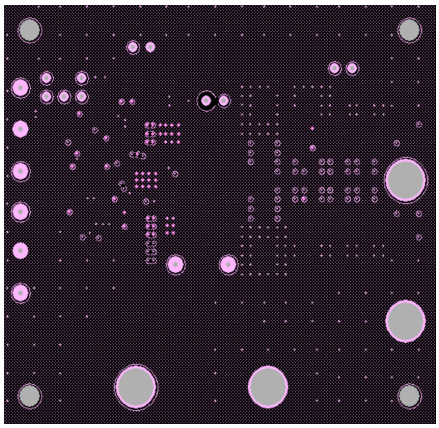


Figure 63. Second Layer

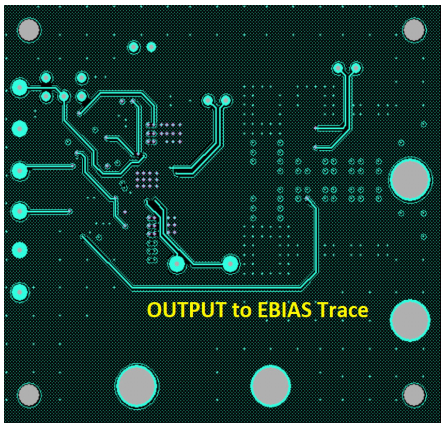



Figure 64. Third Layer

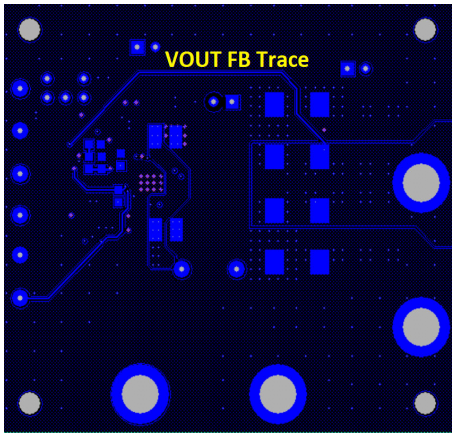



Figure 65. Bottom Layer

# 7. Faults Sensing and Handling

Top Level faults (VIN UVLO, VCC UVLO, OTP) stop $V_{OUT}$ and enter the POR state until the fault is relieved. The IC then starts normally according to EN state.

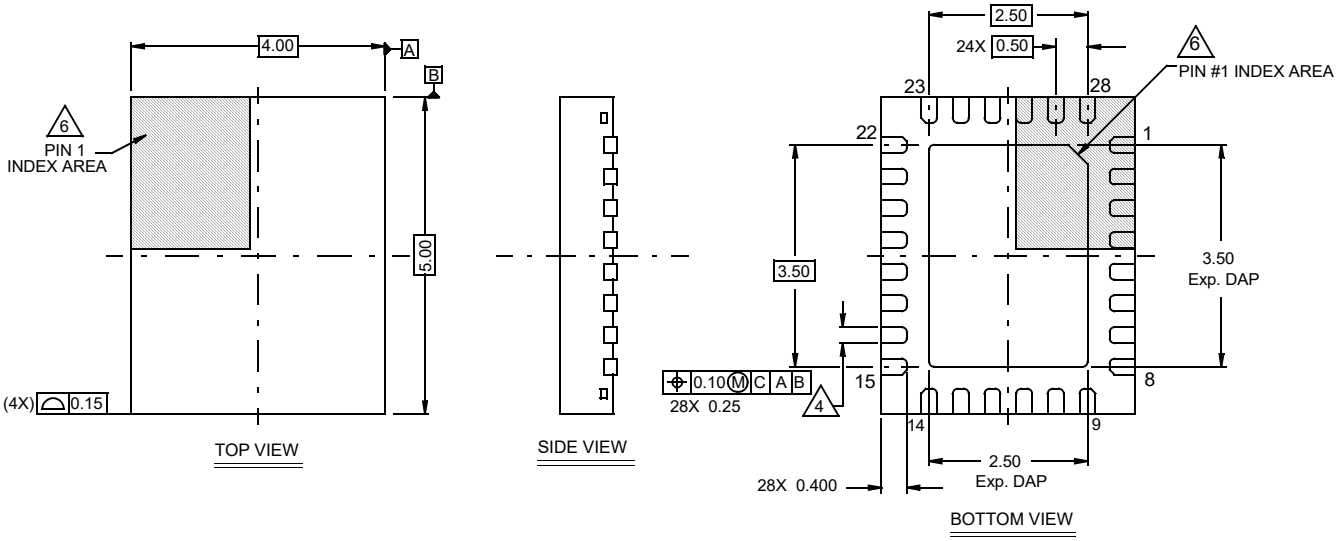
**Table 2. System Level Fault Requirement**

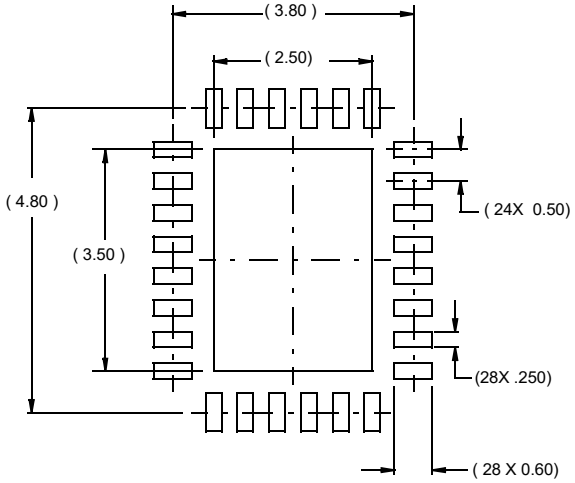
| Fault Type | Detection Activated When | Detection Delay | Design Implementation |
|---|---|---|---|
| PVIN UVLO | EN is higher than threshold | 1µs to 2µs | POR, chip restarts from initial reset state when UVLO is satisfied. |
| Over-Temperature (OT) Shutdown | After soft-start done | N/A | When the over-temperature is detected, switching is stopped until the temperature falls below its hysteresis level. |
| AVCC UVLO | EN is higher than threshold | 1µs to 2µs detection | POR, chip restarts from initial reset state when AVCC UVLO is satisfied. |
| $V_{OUT}$ Overvoltage (OV) | After POR | 1µs to 2µs | If OV is detected after soft-start is done, the device stops switching and enters hiccup every 200ms. |
| $V_{OUT}$ Undervoltage (UV) | After soft-start completes | N/A | If UV fault (VFB -<70%VREF) and low-side overcurrent fault occur simultaneously regulator stops switching and it enters hiccup every 200ms. No fault response for UV or current limit alone. UV is blocked during soft-start. |
| Low-Side Overcurrent (LSOC) Limit | After POR | N/A | If LSOC is detected, the device skips high-side cycles until LSOC goes away. If three cycles have been skipped in the past eight watching cycles, a fault is registered and switching is stopped and the device enters hiccup every 200ms. |
| High-Side Overcurrent (HSOC) | After POR | N/A | When the high-side current is detected as roughly about 200% of maximum $I_{OUT}$, it terminates the switching and enters hiccup every 200ms. |
| Low-Side Negative Overcurrent (LSNOC) | After POR | N/A | When the low-side negative overcurrent is detected, the low-side MOSFET is turned off and high-side MOSFET is turned on to discharge the negative inductor current to zero and the device restarts at the next switching cycle. |

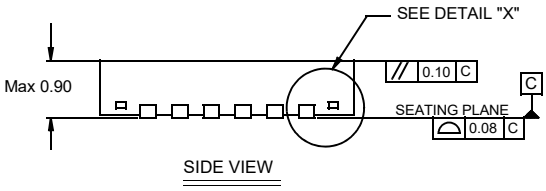
# 8. Package Outline Drawing

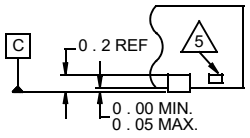
For the most recent package outline drawing, see L28.4x5A.

L28.4x5A
28 Lead Quad Flat No-Lead Plastic Package
Rev 2, 06/08




NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

# 9. Ordering Information

| Part Number[1][2] | Part Marking | Package Description (RoHS Compliant) | Pkg. Dwg. # | Carrier Type[3] | Junction Temp Range |
|---|---|---|---|---|---|
| RAA2116504GNP#HA0 | RA211650 | 28 Ld QFN | L28.4x5A | Reel, 6k | -40 to +125°C |
| RAA2116504GNP#MA0 | | | | Reel, 250 | |
| RTKA211650DE0000BU | Evaluation Board | | | | |

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For moisture sensitivity level (MSL), see the RAA211650 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

**Table 3. Key Comparison between Family of Parts**

| Part Number | Int/Ext Comp | DEM | Int/Ext Soft-Start | Int/Ext Feedback | Programmable Delay | Modulation | Switching Frequency | Ext Freq Sync | Quiescent Current (Switching) |
|---|---|---|---|---|---|---|---|---|---|
| RAA211650 | Yes | No | Yes | Yes | Yes | Valley current sampled fixed frequency PWM | fixed, resistor programmable | Yes | 16.5mA |
| RAA211651 | Yes | Yes | Yes | Yes | Yes | Constant on-time | Load dependent, resistor programmable | No | 19µA |

# 10. Revision History

| Rev. | Date | Description |
|---|---|---|
| 2.00 | Dec 1, 2023 | Corrected typo for the max junction and max storage temp specs by changing them to 150°C. |
| 1.1 | May 6, 2021 | Updated Minimum Off-Time minimum spec from 245 to 235.<br>Added a note reference to OVP line in the spec table. |
| 1.0 | May 3, 2021 | Initial release |

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