RA2L2 Group
Renesas Microcontrollers

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Ultra low power 48 MHz Arm® Cortex®-M23 core, up to 128-KB code flash memory, 16-KB SRAM, USB 2.0 Full-Speed module (USBFS), USB Type-C® interface (USBCC), 12-bit A/D Converter, Security and Safety features.

Features

Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 48MHz
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

Memory

- Up to 128-KB code flash memory
- 4-KB data flash memory (100,000 program/erase (P/E) cycles)
- 16-KB SRAM
- Memory protection units (MPU)
- 128-bit unique ID

Connectivity

- Serial Communications Interface (SCI) × 4
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Simple IIC
  - Simple SPI
  - Smart card interface
- Serial Peripheral Interface (SPI) × 1
- I3C bus interface (I3C) × 1
- USB 2.0 Full-Speed module (USBFS) × 1
- USB Type-C interface (USBCC) × 1
- CAN module (CAN) × 1
- Serial Sound Interface Enhanced (SSIE) × 1
- Serial Interface UARTA (UARTA) × 2

Analog

- 12-bit A/D Converter (ADC12)
- Temperature Sensor (TSN)

Timers

- General PWM Timer 32-bit (GPT32) × 1
- General PWM Timer 16-bit (GPT16) × 6
- Low Power Asynchronous General Purpose Timer (AGTW) × 2
- Watchdog Timer (WDT)

Safety

- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access detection

Security

- True Random Number Generator (TRNG)

System and Power Management

- Low power modes
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

Multiple Clock Sources

- Main clock oscillator (MOSC) (1 to 20 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock out support

Up to 54 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up

Operating Voltage

- VCC: 1.6 to 5.5 V

Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin HWQFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
- Ta = -40°C to +125°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin HWQFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 128-KB code flash memory
- 16-KB SRAM
- USB 2.0 Full-Speed module (USBFS)
- USB Type-C interface (USBCC)
- 12-bit A/D Converter (ADC12)
- Security features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider • Arm Memory Protection Unit (Arm MPU): – Armv8 Protected Memory System Architecture – 8 protect regions • SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 128-KB of code flash memory.
Data flash memory	4-KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with parity bit.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode
Resets	The MCU provides 12 resets (RES pin reset, power-on reset, independent watchdog timer reset, watchdog timer reset, voltage monitor 0/1/2 resets, SRAM parity error reset, bus master/slave MPU error resets, CPU stack pointer error reset, software reset).
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Key Interrupt Function (KINT)	The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt or watchdog timer reset.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.6 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 1 channel and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state

Table 1.6 Timers (2 of 2)

Feature	Functional description
Low power Asynchronous General Purpose Timer (AGTW)	The Low Power Asynchronous General Purpose Timer (AGTW) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGTW register.
Realtime Clock (RTC)	The RTC has two operation modes, normal operation mode and low-consumption clock mode. In each of the operation mode, the RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 4 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I3C bus interface (I3C)	The I3C bus interface (I3C) has one channel. The I3C module conform with and provide a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 1 channel. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
Control Area Network (CAN)	The Controller Area Network (CAN) module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver.
USB 2.0 Full-Speed module (USBFS)	The USB 2.0 Full-Speed module (USBFS) can operate as a device controller. The module supports full-speed transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system.
USB Type-C interface (USBCC)	The module supports for USB Type-C connector of USB 2.0 (Sink/UFP only) as defined in Universal Serial Bus Type-C Cable and Connector Specification Release 2.2, and the module can detect the current supply capability (default /1.5A/3.0A) of VBUS.
Serial interface UARTA (UARTA)	The serial interface UARTA (UARTA) has 2 channels. The UARTA provides full-duplex asynchronous serial communications.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I2S/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 32 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DTC-driven data reception and transmission.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 17 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows the access to specific addresses to be monitored. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

Table 1.10 I/O ports

Feature	Functional description
I/O ports	• I/O ports for the 64-pin LQFP – I/O pins: 51 – Input pins: 3 – Pull-up resistors: 51 – N-ch open-drain outputs: 38 – 5-V tolerance: 7 • I/O ports for the 48-pin LQFP/HWQFN – I/O pins: 35 – Input pins: 3 – Pull-up resistors: 35 – N-ch open-drain outputs: 24 – 5-V tolerance: 7 • I/O ports for the 32-pin LQFP/HWQFN – I/O pins: 21 – Input pins: 3 – Pull-up resistors: 21 – N-ch open-drain outputs: 13 – 5-V tolerance: 5

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

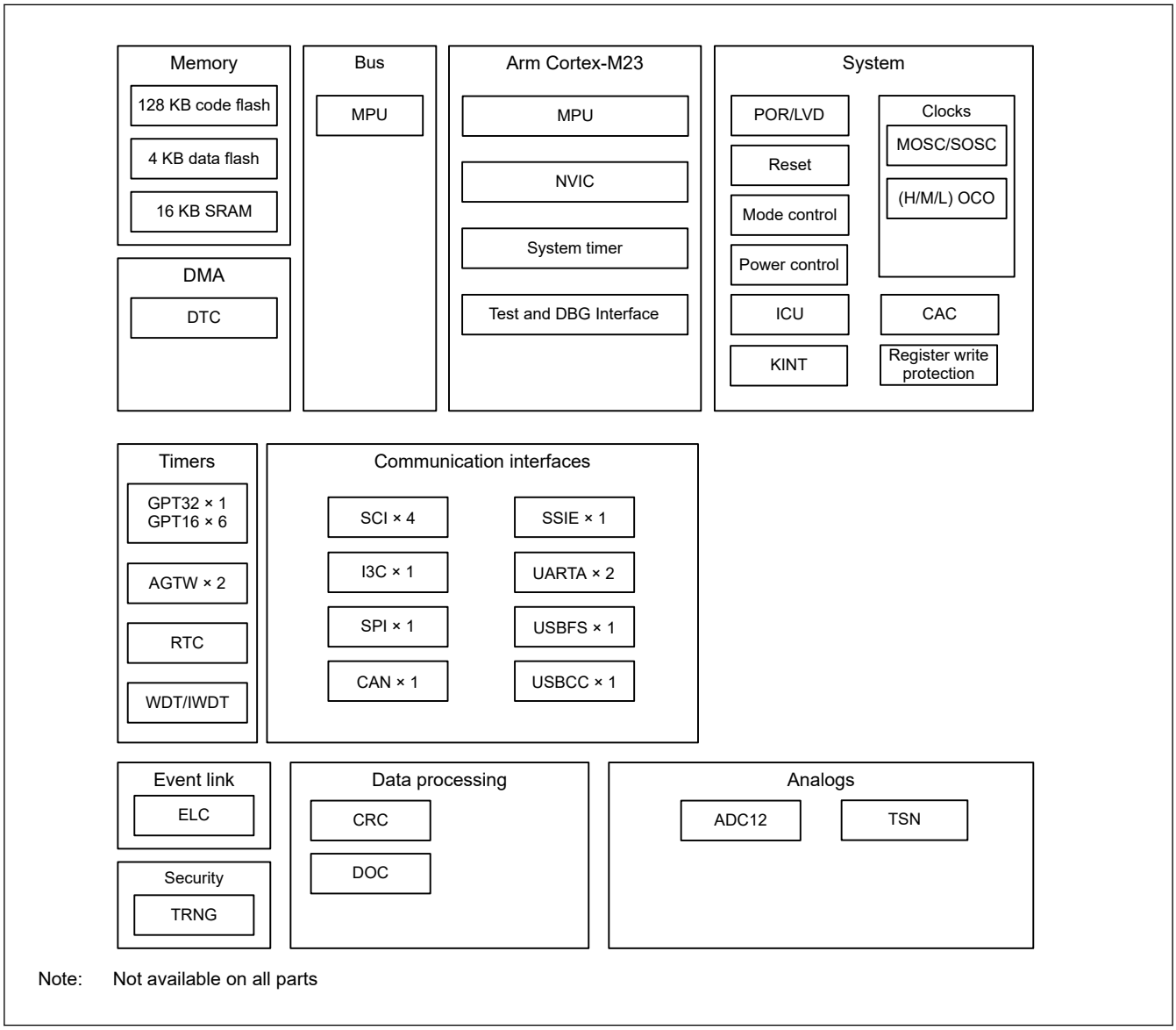


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.11 shows a list of products.

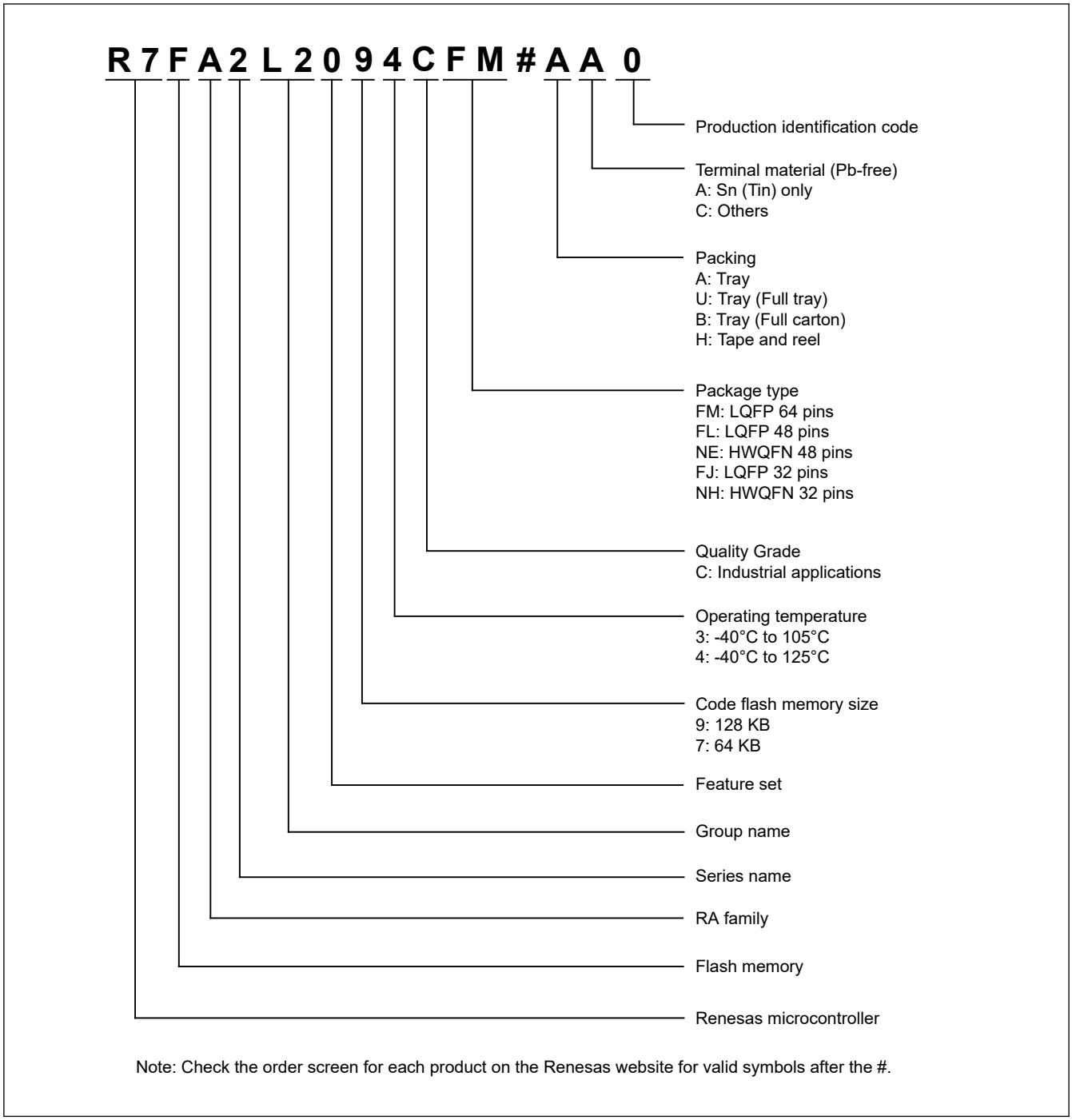


Figure 1.2 Part numbering scheme

Table 1.11 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2L2094CFM	PLQP0064KB-C	128	4	16	-40 to +125°C
R7FA2L2094CFL	PLQP0048KB-B				
R7FA2L2094CFJ	PLQP0032GB-A				
R7FA2L2094CNE	PWQN0048KC-A				
R7FA2L2094CNH	PWQN0032KE-A				
R7FA2L2093CFM	PLQP0064KB-C				-40 to +105°C
R7FA2L2093CFL	PLQP0048KB-B				
R7FA2L2093CFJ	PLQP0032GB-A				
R7FA2L2093CNE	PWQN0048KC-A				
R7FA2L2093CNH	PWQN0032KE-A				
R7FA2L2074CFM	PLQP0064KB-C	64	4	16	-40 to +125°C
R7FA2L2074CFL	PLQP0048KB-B				
R7FA2L2074CFJ	PLQP0032GB-A				
R7FA2L2074CNE	PWQN0048KC-A				
R7FA2L2074CNH	PWQN0032KE-A				
R7FA2L2073CFM	PLQP0064KB-C				-40 to +105°C
R7FA2L2073CFL	PLQP0048KB-B				
R7FA2L2073CFJ	PLQP0032GB-A				
R7FA2L2073CNE	PWQN0048KC-A				
R7FA2L2073CNH	PWQN0032KE-A				

1.4 Function Comparison

Table 1.12 Function Comparison

Parts number		R7FA2L209xCFM	R7FA2L207xCFM	R7FA2L209xCFL R7FA2L209xCNE	R7FA2L207xCFL R7FA2L207xCNE	R7FA2L209xCFJ R7FA2L209xCNH	R7FA2L207xCFJ R7FA2L207xCNH
Pin count		64		48		32	
Package		LQFP		LQFP/HWQFN		LQFP/HWQFN	
Code flash memory		128 KB	64 KB	128 KB	64 KB	128 KB	64 KB
Data flash memory		4 KB		4 KB		4 KB	
SRAM(Parity)		16 KB		16 KB		16 KB	
System	CPU clock	48 MHz		48 MHz		48 MHz	
	Sub clock oscillator	Yes		Yes		Yes	
	ICU	Yes		Yes		Yes	
	KINT	8		5		4	
Event control	ELC	Yes		Yes		Yes	
DMA	DTC	Yes		Yes		Yes	
Timers	GPT32	1 (PWM outputs: 2)		1 (PWM outputs: 2)		1 (PWM outputs: 2)	
	GPT16	6 (PWM outputs: 12)		6 (PWM outputs: 12)		6 (PWM outputs: 7)	
	AGTW	2		2		2	
	RTC	Yes		Yes		Yes	
	WDT/IWDT	Yes		Yes		Yes	
Communication	SCI	4		4		3	
	I3C	1		1		1	
	SPI	1		1		1	
	CAN	1		1		1	
	SSIE	1		1		1	
	UARTA	2		2		2	
	USBFS	1		1		1	
	USBCC	1		1		1	
Analog	ADC12	17		13		10	
	TSN	Yes		Yes		Yes	
Data processing	CRC	Yes		Yes		Yes	
	DOC	Yes		Yes		Yes	
Security		TRNG		TRNG		TRNG	
I/O ports	I/O pins	51		35		21	
	Input pins	3		3		3	
	Pull-up resistors	51		35		21	
	N-ch open-drain outputs	38		24		13	
	5-V tolerance	7		7		5	

1.5 Pin Functions

Table 1.13 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pins
	GTIOCnA (n = 0, 4 to 9), GTIOCnB (n = 0, 4 to 9)	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGTW	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock

Table 1.13 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCKn (n = 0 to 2, 9)	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn (n = 0 to 2, 9)	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn (n = 0 to 2, 9)	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn (n = 0 to 2, 9)	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn (n = 0 to 2, 9)	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn (n = 0 to 2, 9)	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn (n = 0 to 2, 9)	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn (n = 0 to 2, 9)	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn (n = 0 to 2, 9)	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn (n = 0 to 2, 9)	Input	Chip-select input pins (simple SPI mode), active-low
I3C	SCLn (n = 0)	I/O	Input/output pins for the clock
	SDAn (n = 0)	I/O	Input/output pins for data
SPI	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3	Output	Output pins for slave selection
	MOSIA	I/O	Input or output pins for data output from the master
	MISOA	I/O	Input or output pins for data output from the slave
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	USB_DP	I/O	D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
USBCC	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected.
	USB_CC1	Input	Configuration channel 1. The pin can be used to detect connections and configure the interface across the USB Type-C cables and connectors.
	USB_CC2	Input	Configuration channel 2. The pin can be used to detect connections and configure the interface across the USB Type-C cables and connectors.
UARTA	RXDAn (n = 0, 1)	Input	Serial data input pins for serial interfaces.
	TXDAn (n = 0, 1)	Output	Serial data output pins for serial interfaces.
	CLKAn (n = 0, 1)	Output	Clock output pins for serial interfaces.
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins.
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins.
	SSITXD0	Output	Serial data output pin.
	SSIRXD0	Input	Serial data input pin.
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock).

Table 1.13 Pin functions (3 of 3)

Function	Signal	I/O	Description
Analog power supply	AVCC0	Input	Analog power supply pin for the ADC12
	AVSS0	Input	Analog ground pin for the ADC12
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN000 to AN010, AN017 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pin for the external trigger signals that start the A/D conversion, active-low.
KINT	KR00 to KR07	Input	Key interrupt input pins
I/O ports	P000 to P004, P010 to P015	I/O	General-purpose input/output pins
	P100 to P113	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P207, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P912, P913	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments from the top view.

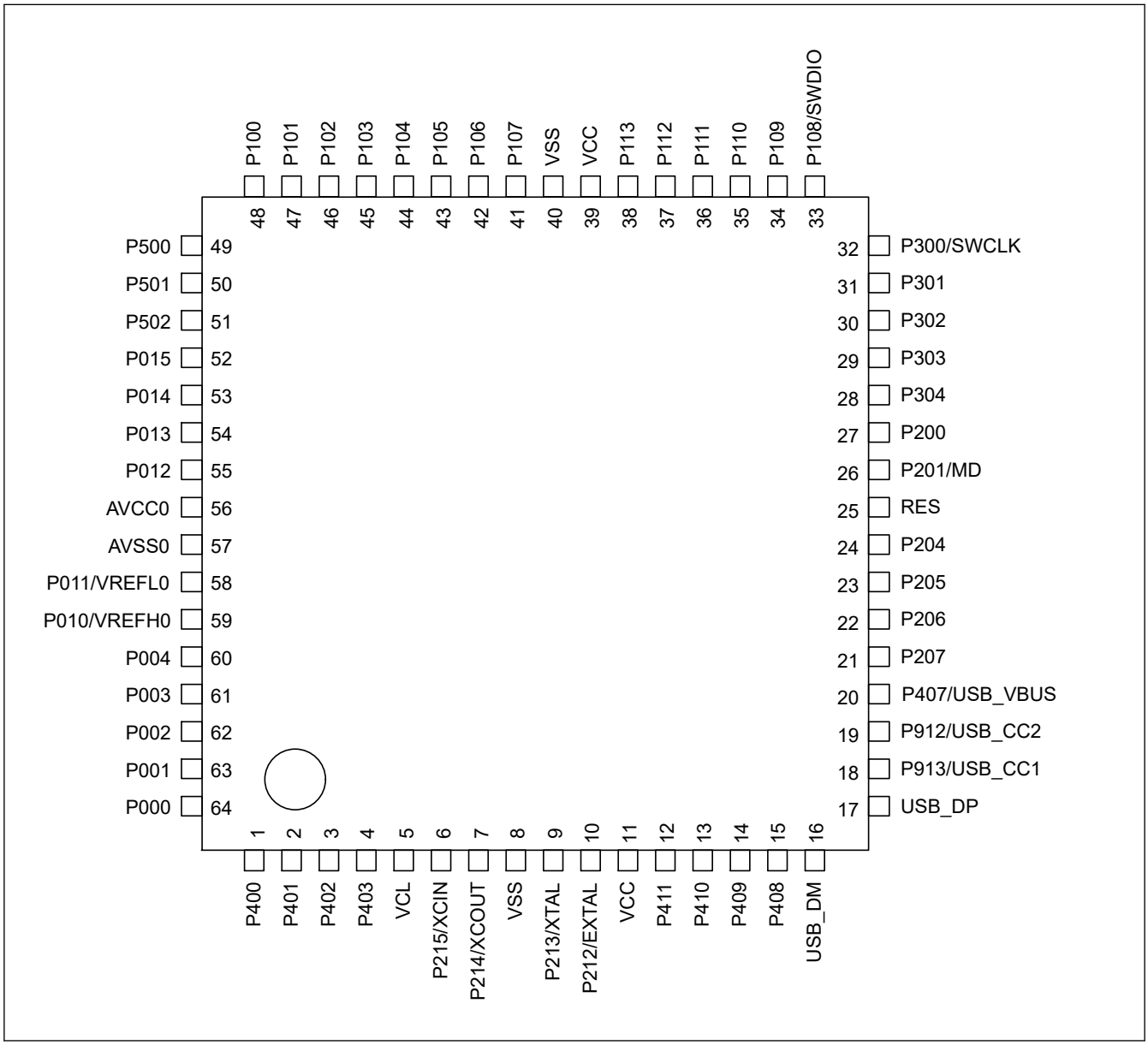


Figure 1.3 Pin assignment for LQFP 64-pin (top view)

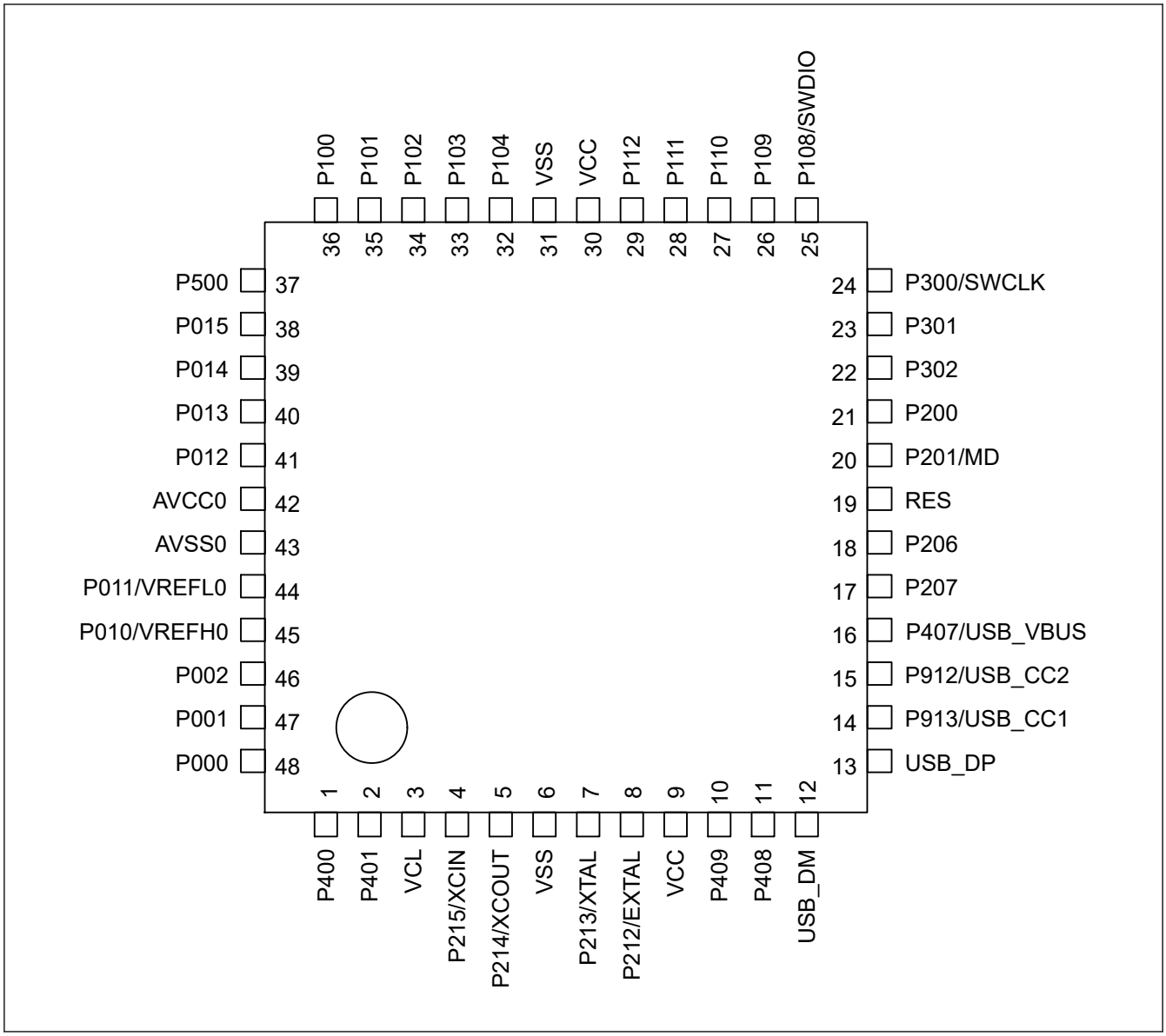


Figure 1.4 Pin assignment for LQFP/QFN 48-pin (top view)

Note: For the product in a QFN package, solder the exposed die pad onto a plated area of the PCB that has no electrical connections.

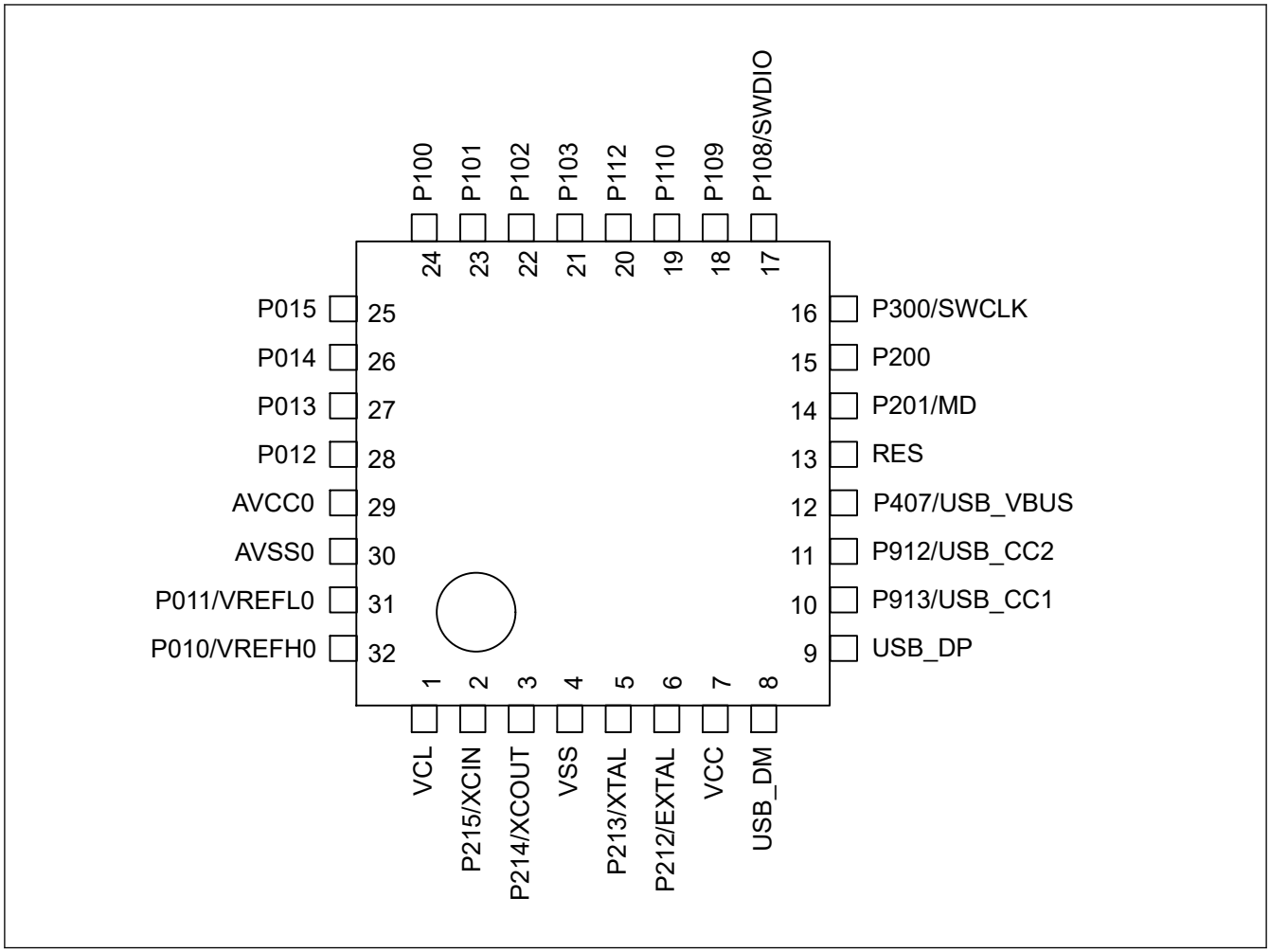


Figure 1.5 Pin assignment for LQFP/QFN 32-pin (top view)

Note: For the product in a QFN package, solder the exposed die pad onto a plated area of the PCB that has no electrical connections.

1.7 Pin Lists

Table 1.14 Pin list (1 of 3)

Pin number					Timers				Communication interfaces							Analogs	HMI
LQFP 64-pin	LQFP/QFN 48-pin	LQFP/QFN 32-pin	Power, System, Clock, Debug, CAC	I/O ports	AGTW	GPT_OPS, POEG	GPT	RTC	CAN	SCI	I3C	SPI	SSIE	UARTA	USBFS, USBCC	ADC	Interrupt
1	1	—	CACREF_C	P400	AGTIO1_C	—	GTIOC9A_A	—	—	SCK0_B/ SCK1_B	SCL0_A	—	—	—	—	—	IRQ_0_A
2	2	—	—	P401	—	GTETRGA_B	GTIOC9B_A	—	CRX0_B	CTS0_RTS 0_B/ SS0_B/ TXD1_B/ MOSI1_B/ SDA1_B	SDA0_A	—	—	CLKA0_B	—	—	IRQ_5
3	—	—	—	P402	AGTIO0_E / AGTIO1_D	—	—	—	CTX0_B	RxD1_B/ MISO1_B/ SCL1_B	—	—	—	RXDA0_B	—	—	IRQ_4
4	—	—	—	P403	AGTIO0_F / AGTIO1_E	—	—	—	—	CTS1_RTS 1_B/ SS1_B	—	—	—	TXDA0_B	—	—	—
5	3	1	VCL	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	4	2	XCIN	P215	—	—	—	—	—	—	—	—	—	—	—	—	—
7	5	3	XCOUT	P214	—	—	—	—	—	—	—	—	—	—	—	—	—
8	6	4	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	7	5	XTAL	P213	—	GTETRGA_D	GTIOC0A_D	—	—	TXD1_A/ MOSI1_A/ SDA1_A	—	—	—	—	—	—	IRQ2_B
10	8	6	EXTAL	P212	AGTEE1	GTETRGB_D	GTIOC0B_D	—	—	RxD1_A/ MISO1_A/ SCL1_A	—	—	—	—	—	—	IRQ3_B
11	9	7	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	—	P411	AGTOA1	GTOVUP_B	—	—	—	TXD0_B/ MOSI0_B/ SDA0_B	—	MOSIA_B	SSIBCK0_A	—	—	—	IRQ4_B
13	—	—	—	P410	AGTOB1	GTOVLO_B	—	—	—	RxD0_B/ MISO0_B/ SCL0_B	—	MISOA_B	SSILRCK0 / SSIFS0_A	CLKA1_B	—	—	IRQ5_B
14	10	—	—	P409	—	GTOWUP_B	—	—	—	—	—	—	SSITXD0_A	RXDA1_B	—	—	IRQ6_B
15	11	—	—	P408	—	GTOWLO_B	—	—	—	CTS1_RTS 1_D/ SS1_D	—	—	SSIRXD0_A	TXDA1_B	—	—	IRQ7_B
16	12	8	—	—	—	—	—	—	—	—	—	—	—	—	USB_DM	—	—
17	13	9	—	—	—	—	—	—	—	—	—	—	—	—	USB_DP	—	—
18	14	10	—	P913	—	—	—	—	CRX0_D	—	SCL0_C	—	—	—	USB_CC1	—	IRQ5_D
19	15	11	—	P912	—	—	—	—	CTX0_D	—	SDA0_C	—	—	—	USB_CC2	—	—
20	16	12	—	P407	AGTIO0_C	—	—	RTCOUT_A	—	CTS0_RTS0_D	—	—	SSIDATA0_B	—	USB_VBUS	ADTRG0_B	
21	17	—	—	P207	—	—	—	—	—	—	—	—	SSIBCK0_B	—	—	—	—
22	18	—	—	P206	—	GTIU_A	—	—	—	RxD0_D/ MISO0_D/ SCL0_D	—	—	SSILRCK0 / SSIFS0_B	—	—	—	IRQ0
23	—	—	CLKOUT_A	P205	AGTO1	GTIV_A	—	—	—	TXD0_D/ MOSI0_D/ SDA0_D/ CTS9_RTS 9_A/ SS9_A	—	—	SSITXD0_B	—	—	—	IRQ1
24	—	—	CACREF_A	P204	AGTIO1_A	GTIW_A	—	—	—	SCK0_D/ SCK9_A	—	—	SSIRXD0_B	—	—	—	—
25	19	13	RES	—	—	—	—	—	—	—	—	—	—	—	—	—	—
26	20	14	MD	P201	—	—	—	—	—	—	—	—	—	—	—	—	—
27	21	15	—	P200	—	—	—	—	—	—	—	—	—	—	—	—	NMI
28	—	—	—	P304	—	—	—	—	—	—	—	—	—	—	—	—	—
29	—	—	—	P303	—	—	—	—	—	—	—	—	—	—	—	—	—
30	22	—	—	P302	—	GTOUUP_A	GTIOC7A_A	—	—	TXD2_A/ MOSI2_A/ SDA2_A	—	—	—	—	—	—	IRQ5_A

Table 1.14 Pin list (2 of 3)

Pin number			Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication interfaces							Analogs	HMI
LQFP 64-pin	LQFP/QFN 48-pin	LQFP/QFN 32-pin			AGTW	GPT_OPS, POEG	GPT	RTC	CAN	SCI	I3C	SPI	SSIE	UARTA	USBFS, USBCC	ADC	Interrupt
31	23	—	—	P301	AGTIO0_D	GTOULO_A	GTIOC7B_A	—	—	RxD2_A/ MISO2_A/ SCL2_A/ CTS9_RTS 9_D/ SS9_D	—	—	—	—	—	—	IRQ6_A
32	24	16	SWCLK	P300	AGTIO0_B	GTOUUP_C	GTIOC0A_A	—	—	—	—	—	—	CLKA0_A	—	—	—
33	25	17	SWDIO	P108	AGTOA1_B	GTOULO_C	GTIOC0B_A	—	—	CTS9_RTS 9_B/ SS9_B	—	—	SSIDATA0_A	RXDA0_A	—	—	—
34	26	18	CLKOUT_B	P109	AGTIO1_B	GTOVUP_A	GTIOC4A_A	—	CRX0_A	SCK1_E/ TXD9_B/ MOSI9_B/ SDA9_B	SCL0_B	—	AUDIO_CLK_A	TXDA0_A	—	—	IRQ5_E
35	27	19	—	P110	AGTOB0_B	GTOVLO_A	GTIOC4B_A	RTCOUT_B	CTX0_A	CTS2_RTS 2_B/ SS2_B/ RxD9_B/ MISO9_B/ SCL9_B	SDA0_B	—	—	—	—	—	IRQ3_A
36	28	—	—	P111	AGTOA0	—	GTIOC6A_A	—	—	SCK2_B/ SCK9_B	—	—	—	—	—	—	IRQ4_A
37	29	20	—	P112	AGTOB0	—	GTIOC6B_A	—	—	SCK1_D/ TXD2_B/ MOSI2_B/ SDA2_B	—	—	AUDIO_CLK_B	—	—	ADTRG0_C	—
38	—	—	—	P113	—	—	—	—	—	—	—	—	—	—	—	—	—
39	30	—	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
40	31	—	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
41	—	—	—	P107	—	—	—	—	—	—	—	—	—	—	—	—	KR07
42	—	—	—	P106	—	—	—	—	—	—	—	SSLA3_A	—	—	—	—	KR06
43	—	—	—	P105	—	GTETRGA_C	GTIOC4A_B	—	—	—	—	SSLA2_A	—	—	—	—	KR05/ IRQ0_B
44	32	—	—	P104	—	GTETRGB_B	GTIOC4B_B	—	—	RxD0_C/ MISO0_C/ SCL0_C	—	SSLA1_A	—	—	—	—	KR04/ IRQ1_B
45	33	21	—	P103	—	GTOWUP_A	GTIOC5A_A	—	CRX0_C	CTS0_RTS 0_A/ SS0_A	—	SSLA0_A	SSIBCK0_C	—	—	AN019	KR03/ IRQ5_F
46	34	22	—	P102	AGTO0	GTOWLO_A	GTIOC5B_A	—	CTX0_C	SCK0_A/ TXD2_D/ MOSI2_D/ SDA2_D	—	RSPCKA_A	SSILRCK0/ SSIFS0_C	—	—	ADTRG0_A /AN020	KR02
47	35	23	—	P101	AGTEE0	GTETRGB_A	GTIOC8A_A	—	—	TXD0_A/ MOSI0_A/ SDA0_A/ CTS1_RTS 1_A/ SS1_A	—	MOSIA_A	SSITXD0_C	—	—	AN021	KR01/ IRQ1_A
48	36	24	—	P100	AGTIO0_A	GTETRGA_A	GTIOC8B_A	—	—	RxD0_A/ MISO0_A/ SCL0_A/ SCK1_A	—	MISOA_A	SSIRXD0_C	—	—	AN022	KR00/ IRQ2_A
49	37	—	—	P500	—	GTIU_B	GTIOC5A_B	—	—	—	—	—	AUDIO_CLK_C	CLKA1_A	—	—	—
50	—	—	—	P501	—	GTIV_B	GTIOC5B_B	—	—	TXD1_C/ MOSI1_C/ SDA1_C	—	—	—	—	—	AN017	—
51	—	—	—	P502	—	GTIW_B	—	—	—	RxD1_C/ MISO1_C/ SCL1_C	—	—	—	—	—	AN018	—
52	38	25	—	P015	—	GTETRGB_E	—	—	—	—	—	—	—	RXDA1_A	—	AN010	IRQ7_A
53	39	26	—	P014	—	GTETRGA_E	—	—	—	—	—	—	—	TXDA1_A	—	AN009	IRQ6_C
54	40	27	—	P013	—	—	—	—	—	—	—	—	—	—	—	AN008	IRQ4_C
55	41	28	—	P012	—	—	—	—	—	—	—	—	—	—	—	AN007	IRQ1_C
56	42	29	AVCC0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
57	43	30	AVSS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
58	44	31	VREFL0	P011	—	—	—	—	—	—	—	—	—	—	—	AN006	IRQ0_C

Table 1.14 Pin list (3 of 3)

Pin number			Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication interfaces							Analogs	HMI
LQFP 64-pin	LQFP/QFN 48-pin	LQFP/QFN 32-pin			AGTW	GPT_OPS, POEG	GPT	RTC	CAN	SCI	I3C	SPI	SSIE	UARTA	USBFS, USBCC	ADC	Interrupt
59	45	32	VREFH0	P010	—	—	—	—	—	—	—	—	—	—	—	AN005	IRQ5_C
60	—	—	—	P004	—	—	—	—	—	—	—	—	—	—	—	AN004	IRQ3
61	—	—	—	P003	—	—	—	—	—	—	—	—	—	—	—	AN003	—
62	46	—	—	P002	—	—	—	—	—	—	—	—	—	—	—	AN002	IRQ2
63	47	—	—	P001	—	—	—	—	—	—	—	—	—	—	—	AN001	IRQ7
64	48	—	—	P000	—	—	—	—	—	—	—	—	—	—	—	AN000	IRQ6

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E and _F. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC[*1] = AVCC0 = 1.6 to 5.5 V, VREFH0 = 1.6 V to AVCC0

VSS = AVSS0 = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.

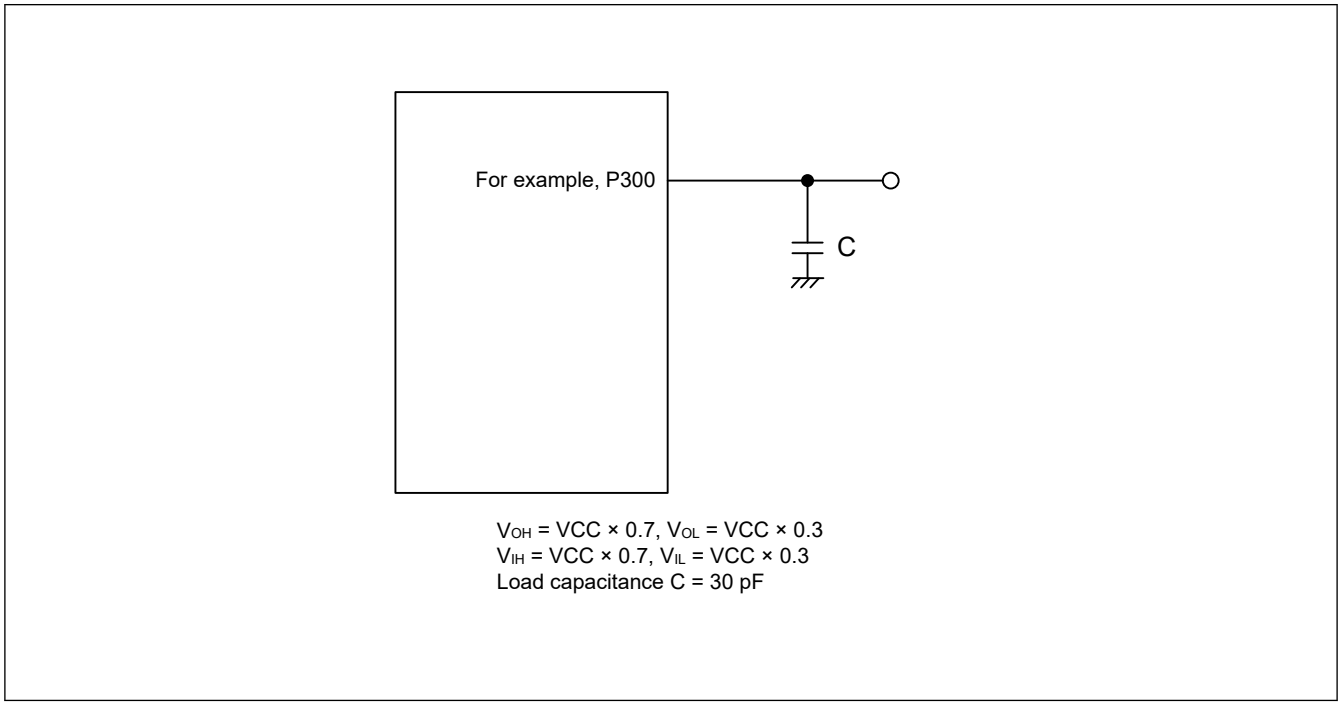


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5V-tolerant ports[*1]	V_{in}	-0.3 to +6.5	V
	P000 to P004, P010 to P015	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
Analog power supply voltage		AVCC0	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN010 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN017 to AN022 are used		-0.3 to VCC + 0.3	V
Operating temperature[*2 *3 *4]		T_{opr}	-40 to +105 -40 to +125	°C

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
Storage temperature	T_{stg}	-55 to +140	°C

Note 1. Ports P400, P401, P407, P109, P110, P912 and P913 are 5V-tolerant.
Note 2. See section 2.2.1. Tj/Ta Definition.
Note 3. Contact Renesas Electronics sales office for information on derating operation under Ta = +105°C to +125°C. Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of the operating temperature is 105°C or 125°C, depending on the product.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- **VCC and VSS: about 0.1 µF**
- **AVCC0 and AVSS0: about 0.1 µF**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC*1 *2		1.6	—	5.5	V
	VCC*1 *2 *3		3.0	—	3.6	V
	VSS		—	0	—	V
Analog power supply voltages	AVCC0*1 *2		1.6	—	5.5	V
	AVSS0		—	0	—	V
	VREFH0	When used as ADC12 Reference	1.6	—	AVCC0	V
	VREFL0		—	0	—	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 = VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pins.
When powering off the VCC and AVCC0 pins, power them off at the same time or the AVCC0 pin first and then the VCC pins.
Note 3. When using the USB 2.0 Full-Speed Module (USBFS) or the USB Type-C Interface.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +125°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	140	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode
			125*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.
Note 1. The upper limit of operating temperature is 125°C or 140°C, depending on the product. If the part number shows the operation temperature at 105°C, then the maximum value of Tj is 125°C, otherwise it is 140°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter	Ports & Functions		Symbol	Min	Max	Unit	Test conditions
Input voltage	Input ports pins P000 to P004, P010 to P015		V_{IH}	AVCC0 × 0.8	—	V	—
			V_{IL}	—	AVCC0 × 0.2		
	Input ports pins except for P000 to P004, P010 to P015		V_{IH}	VCC × 0.8	—		
			V_{IL}	—	VCC × 0.2		
	EXTAL		V_{IH}	VCC × 0.8	—		
			V_{IL}	—	VCC × 0.2		
	5V-tolerant ports*2		V_{IH}	VCC × 0.8	5.8		
			V_{IL}	—	VCC × 0.2		
	RES, NMI, IRQ		V_{IH}	VCC × 0.8	—		
			V_{IL}	—	VCC × 0.2		
			ΔV_T*4	VCC × 0.10	—		VCC = 2.7 to 5.5 V
				VCC × 0.05	—		VCC = 1.6 to 2.7 V
	Peripheral functions	AGT, GPT, SPI, Others *3	V_{IH}	VCC × 0.8	—		—
			V_{IL}	—	VCC × 0.2		
			ΔV_T*4	VCC × 0.10	—		VCC = 2.7 to 5.5 V
				VCC × 0.05	—		VCC = 1.6 to 2.7 V
		I3C (except for SMBus)*1	V_{IH}	VCC × 0.7	5.8		—
			V_{IL}	—	VCC × 0.3		
			ΔV_T*4	VCC × 0.10	—		VCC = 2.7 to 5.5 V
				VCC × 0.05	—		VCC = 1.6 to 2.7 V
		I3C (SMBus)*1	V_{IH}	2.2	—		VCC = 3.6 to 5.5 V
			V_{IL}	2.0	—		VCC = 2.7 to 3.6 V
			V_{IL}	—	0.8		VCC = 3.6 to 5.5 V
			V_{IL}	—	0.5		VCC = 2.7 to 3.6 V

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SDA0_C (total 6 pins)
Note 2. P400, P401, P407, P109, P110, P912 and P913 (total 7 pins)
Note 3. See section x.x Peripheral Select Settings for Each Product.
Note 4. I/O Port with ΔVT has Schmitt Trigger capability when PMR = 1 or ISEL = 1. For peripheral selection, see section x.x Peripheral Select Settings for Each Product.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 4)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value per pin)	Ports P000 to P004, P010 to P015, P212, P213, P407	I_{OH}	—	—	-4.0	mA	—
		I_{OL}	—	—	8.0	mA	—
	Ports P400, P401, P109, P110, P912 and P913	I_{OH}	—	—	-8.0	mA	—
		I_{OL}	—	—	15.0	mA	—
	Other output pins*1	I_{OH}	—	—	-4.0	mA	—
		I_{OL}	—	—	20.0	mA	—

Table 2.5 I/O I_{OH}, I_{OL} (2 of 4)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	64 pin products	Total of ports P000 to P004, P010 to P015	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of ports P204 to P207, P400 to P403, P407 to P411, P912, P913	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of ports P100 to P113, P201, P300 to P304, P500 to P502	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	100		—

Table 2.5 I/O I_{OH}, I_{OL} (3 of 4)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	48 pin products	Total of ports P000 to P002, P010 to P015	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-8		AVCC0 = 1.8 to 2.7 V
				—	—	-4		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		AVCC0 = 2.7 to 5.5 V
				—	—	4		AVCC0 = 1.8 to 2.7 V
				—	—	2		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of ports P206, P207, P400, P401, P407 to P409, P912, P913	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of ports P100 to P104, P108 to P112, P201, P300 to P302, P500	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8		VCC = 1.8 to 2.7 V
				—	—	-4		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 2.7 to 5.5 V
				—	—	4		VCC = 1.8 to 2.7 V
				—	—	2		VCC = 1.6 to 1.8 V
		Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	100		—

Table 2.5 I/O I_{OH}, I_{OL} (4 of 4)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	32 pin products	Total of ports P010 to P015	$\Sigma I_{OH\ (max)}$	—	—	-24	mA	AVCC0 = 2.7 to 5.5 V
				—	—	-6		AVCC0 = 1.8 to 2.7 V
				—	—	-3		AVCC0 = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	48		AVCC0 = 2.7 to 5.5 V
				—	—	3.6		AVCC0 = 1.8 to 2.7 V
				—	—	1.8		AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	$\Sigma I_{OH\ (max)}$	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2		VCC = 1.8 to 2.7 V
				—	—	-1		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	16.0		VCC = 2.7 to 5.5 V
				—	—	1.2		VCC = 1.8 to 2.7 V
				—	—	0.6		VCC = 1.6 to 1.8 V
		Total of other output ports	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 4.0 to 5.5 V
				—	—	-20		VCC = 2.7 to 4.0 V
				—	—	-12		VCC = 1.8 to 2.7 V
				—	—	-6		VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50		VCC = 4.0 to 5.5 V
				—	—	20		VCC = 2.7 to 4.0 V
				—	—	8		VCC = 1.8 to 2.7 V
				—	—	4		VCC = 1.6 to 1.8 V
		Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-54	mA	—
			$\Sigma I_{OL\ (max)}$	—	—	98		—

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Note 2. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015	V_{OH}	AVCC0 - 0.8	—	—	V	I_{OH} = -4.0 mA
	Ports P400, P401, P109, P110, P912, P913	V_{OH}	VCC - 0.27	—	—		I_{OH} = -3.0 mA
			VCC - 0.8	—	—		I_{OH} = -8.0 mA
	Output pins except for P000 to P004, P010 to P015, P400, P401, P109, P110, P912 and P913*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P000 to P004, P010 to P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P212, P213, P407	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P400, P401, P109, P110, P912, P913	V_{OL}	—	—	0.27		I_{OL} = 3.0 mA
			—	—	0.4		I_{OL} = 9.0 mA
			—	—	0.8		I_{OL} = 15.0 mA
	Output pins except for P000 to P004, P010 to P015, P212, P213, P400, P401, P407, P109, P110, P912 and P913*1	V_{OL}	—	—	1.2		I_{OL} = 20.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015	V_{OH}	AVCC0 - 0.8	—	—	V	I_{OH} = -4.0 mA
	Ports P400, P401, P109, P110, P912, P913	V_{OH}	VCC - 0.27	—	—		I_{OH} = -3.0 mA
			VCC - 0.8	—	—		I_{OH} = -8.0 mA
	Output pins except for P000 to P004 and P010 to P015, P400, P401, P109, P110, P912, P913*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P000 to P004, P010 to P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P400, P401, P109, P110, P912, P913	V_{OL}	—	—	0.27		I_{OL} = 3.0 mA
			—	—	0.4		I_{OL} = 9.0 mA
			—	—	0.8		I_{OL} = 15.0 mA
	Output pins except for P000 to P004 and P010 to P015, P400, P401, P109, P110, P912, P913*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = AVCC0 = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015	V_{OH}	AVCC0 - 0.5	—	—	V	I_{OH} = -1.0 mA AVCC0 = 1.8 to 2.7 V
			AVCC0 - 0.5	—	—		I_{OH} = -0.5 mA AVCC0 = 1.6 to 1.8 V
	Output pins except for P000 to P004 and P010 to P015*1	V_{OH}	VCC - 0.5	—	—		I_{OH} = -1.0 mA VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		I_{OH} = -0.5 mA VCC = 1.6 to 1.8 V
	Ports P000 to P004, P010 to P015	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA AVCC0 = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA AVCC0 = 1.6 to 1.8 V
	Output pins except for P000 to P004 and P010 to P015*1	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA VCC = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA VCC = 1.6 to 1.8 V

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.9 I/O other characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200, P214, P215	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200, P214, P215, and 5V-tolerant ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		—	—	15		

Note 1. P400, P401, P407, P109, P110, P912, P913 (total 7 pins)

2.2.5 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 48 MHz	I_{CC}	4.20	—	mA	*7 *11
				ICLK = 32 MHz		3.00	—		*7
				ICLK = 16 MHz		1.85	—		
				ICLK = 8 MHz		1.25	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 48 MHz		—	11.70		*9*11
		Sleep mode	All peripheral clocks disabled*5	ICLK = 48 MHz		1.00	—		*7
				ICLK = 32 MHz		0.80	—		*7
				ICLK = 16 MHz		0.65	—		
				ICLK = 8 MHz		0.55	—		
			All peripheral clocks enabled*5	ICLK = 48 MHz		4.45	—		*9
				ICLK = 32 MHz		3.95	—		*8
				ICLK = 16 MHz		2.20	—		
				ICLK = 8 MHz		1.35	—		
		Increase during BGO operation*6				2.05	—		—

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 24 MHz	I_{CC}	2.30	—	mA	*7
				ICLK = 4 MHz		0.80	—		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 24 MHz		—	7.40		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 24 MHz		0.65	—		*7
				ICLK = 4 MHz		0.55	—		
			All peripheral clocks enabled*5	ICLK = 24 MHz		3.00	—		*8
				ICLK = 4 MHz		0.90	—		
		Increase during BGO operation*6				1.85	—		—
	Low-speed mode*3	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 2 MHz		0.28	—	mA	*7
			All peripheral clocks enabled, code executing from flash*5	ICLK = 2 MHz		—	2.40		*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 2 MHz		0.12	—		*7
			All peripheral clocks enabled*5	ICLK = 2 MHz		0.31	—		*8
	Subosc-speed mode*4	Normal mode	All peripheral clocks enabled, code executing from flash*5	ICLK = 32.768 kHz		—	162	µA	*8
		Sleep mode	All peripheral clocks disabled*5	ICLK = 32.768 kHz		1.90	—		*8
			All peripheral clocks enabled*5	ICLK = 32.768 kHz		4.95	—		*8

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. PCLKB and PCLKD are set to divided by 64.
Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 9. PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.
Note 11. The prefetch buffer is operating.

Table 2.11 Operating and standby current (2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*3	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	Peripheral modules stop	All SRAMs (0x2000_4000 to 0x2000_7FFF) are on	T_a = 25°C	I_{CC}	0.25	1.3	µA	—
				T_a = 55°C		0.45	4.3		
				T_a = 85°C		1.25	15		
				T_a = 105°C		2.80	37		
				T_a = 125°C		6.85	89		
			Only 8KB SRAM (0x2000_4000 to 0x2000_5FFF) is on	T_a = 25°C		0.25	1.3		
				T_a = 55°C		0.45	4.3		
				T_a = 85°C		1.20	15		
				T_a = 105°C		2.70	37		
				T_a = 125°C		6.40	89		
		Increment for RTC operation with low-speed on-chip oscillator*4				0.3	—		—
		Increment for RTC operation in normal operation mode with sub-clock oscillator*4				0.2	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RCR4.ROPSEL is 0 (RTC operation in normal operation mode)
						0.95	—		SOMCR.SODRV[1:0] are 00b (normal mode) RCR4.ROPSEL is 0 (RTC operation in normal operation mode)
		Increment for RTC operation in low-consumption clock mode with sub-clock oscillator*4				0.15	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RCR4.ROPSEL is 1 (RTC operation in low-consumption clock mode)
						0.9	—		SOMCR.SODRV[1:0] are 00b (normal mode) RCR4.ROPSEL is 1 (RTC operation in low-consumption clock mode)

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the low-speed on-chip oscillator or sub-oscillation circuit current.

Table 2.12 Operating and standby current (3) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed A/D conversion mode)	I_{AVCC0}	—	—	1.44	mA	—
	During 12-bit A/D conversion (at low-power A/D conversion mode)		—	—	0.78	mA	—
	Waiting for 12-bit A/D conversion (all units)*1		—	—	1.0	µA	—
Reference power supply current	During 12-bit A/D conversion	I_{REFH0}	—	—	120	µA	—
	Waiting for 12-bit A/D conversion		—	—	60	nA	—

Table 2.12 Operating and standby current (3) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Temperature Sensor (TSN) operating current			I_{TNS}	—	95	—	µA	—
USBFS operating current	Low speed	Operating	I_{USBFS}	—	1.36	6	mA	—
		Standby		—	69	200	µA	
	Full speed	Operating		—	1.68	8	mA	
		Standby		—	551	860	µA	
USBCC operating current	Attach SRC*2		I_{USBCC}	—	0.53	0.73	mA	—
	Attach SRC VRD-3.0*3			—	0.55	0.82	mA	—
	Power Down*4			—	0.01	0.02	µA	—

Note 1. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.
Note 2. Active Block is Regulator + VRADET(CCIO1+CCIO2).
Note 3. Active Block is Regulator + SNKVRD15DET+SNKVRD30DET.
Note 4. When CCC.PDOWN = 0.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.13 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.14 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

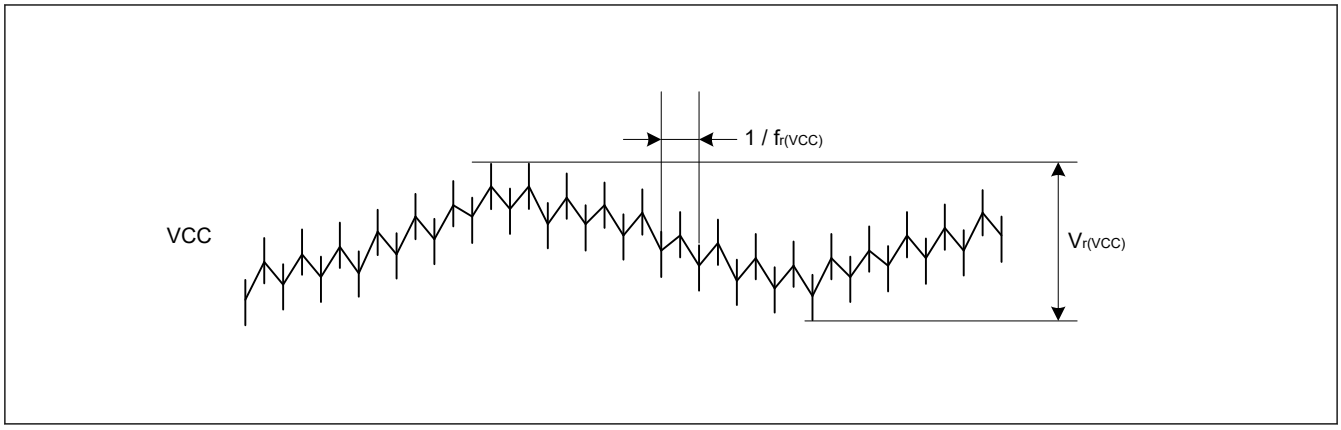


Figure 2.2 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption

  Tj : Junction temperature (°C)

  Ta : Ambient temperature (°C)

  Tt : Top center case temperature (°C)

  θja : Thermal resistance of “Junction”-to-“Ambient” (°C/W)

  Ψjt : Thermal resistance of “Junction”-to-“Top center case” (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (IOL × VOL) / Voltage + Σ (|IOH| × |VCC – VOH|) / Voltage
- Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage

  Cin: Input capacitance

  Cload: Output capacitance

Regarding θja and Ψjt, see Table 2.15.

Table 2.15 Thermal resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal resistance	32-pin HWQFN	θja	22.5	°C/W	JESD 51-2 and 51-7 compliant
	48-pin HWQFN		19.0		
	32-pin LQFP		60.9		
	48-pin LQFP		62.4		
	64-pin LQFP 0.5mm pitch		53.6		
	32-pin HWQFN	Ψjt	0.20	°C/W	JESD 51-2 and 51-7 compliant
	48-pin HWQFN		0.18		
	32-pin LQFP		2.50		
	48-pin LQFP		2.50		
	64-pin LQFP 0.5mm pitch		2.00		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, see the JEDEC standards.

2.3 AC Characteristics

2.3.1 Frequency

Table 2.16 Operation frequency in high-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	48	MHz
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	32	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	64	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20.

Table 2.17 Operation frequency in middle-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20.

Table 2.18 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.6 to 5.5 V	f	0.032768	—	2	MHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	2	
	Peripheral module clock (PCLKD)*3	1.6 to 5.5 V		—	—	2	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20.

Table 2.19 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	37.6832	
	Peripheral module clock (PCLKD)*2	1.6 to 5.5 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.20 Clock timing

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.3
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rising time	t_{Xr}	—	—	5	ns	
EXTAL external clock falling time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL external clock input frequency	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 5.5 V
		—	—	4		1.6 ≤ VCC < 1.8 V
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	1.8 ≤ VCC ≤ 5.5 V
		1	—	4		1.8 ≤ VCC ≤ 5.5 V
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	μs	Figure 2.4
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	μs	—
HOCO clock oscillation frequency	f_{HOCO24}	23.76	24	24.24	MHz	Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 V
	f_{HOCO32}	31.68	32	32.32		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 V
	f_{HOCO48}	47.52	48	48.48		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 V
	f_{HOCO64}	63.36	64	64.64		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 V
HOCO clock oscillation stabilization time*3 *4	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	6.7	7.7	μs	Figure 2.5
Sub-clock oscillator oscillation frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	—	0.5	—	s	Figure 2.6

Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 μs.
Note 4. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

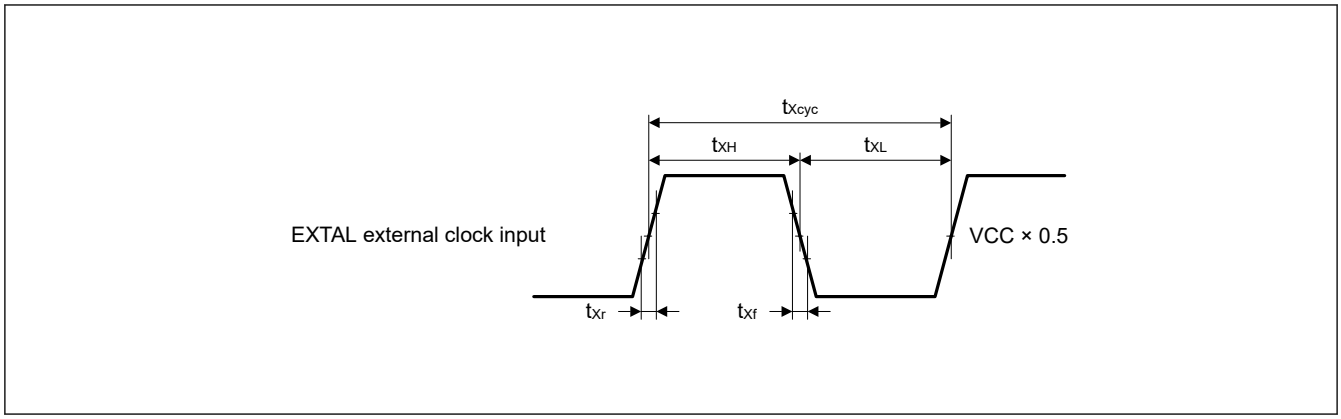


Figure 2.3 EXTAL external clock input timing

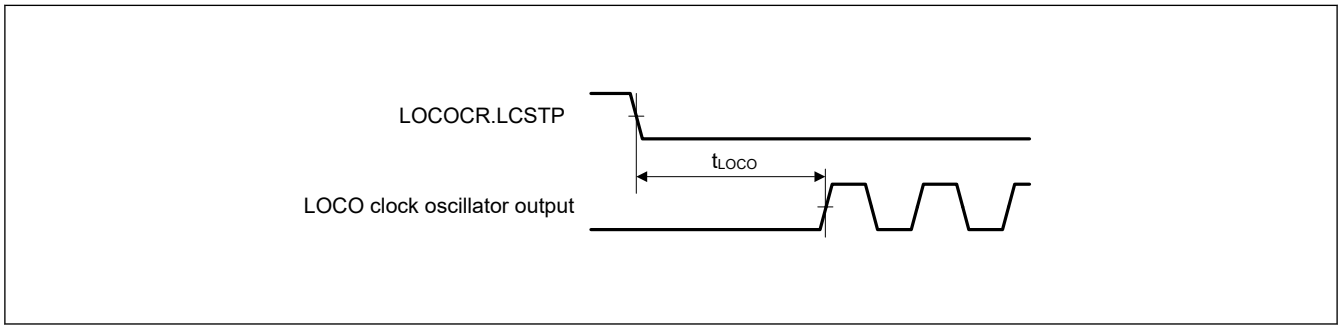


Figure 2.4 LOCO clock oscillation start timing

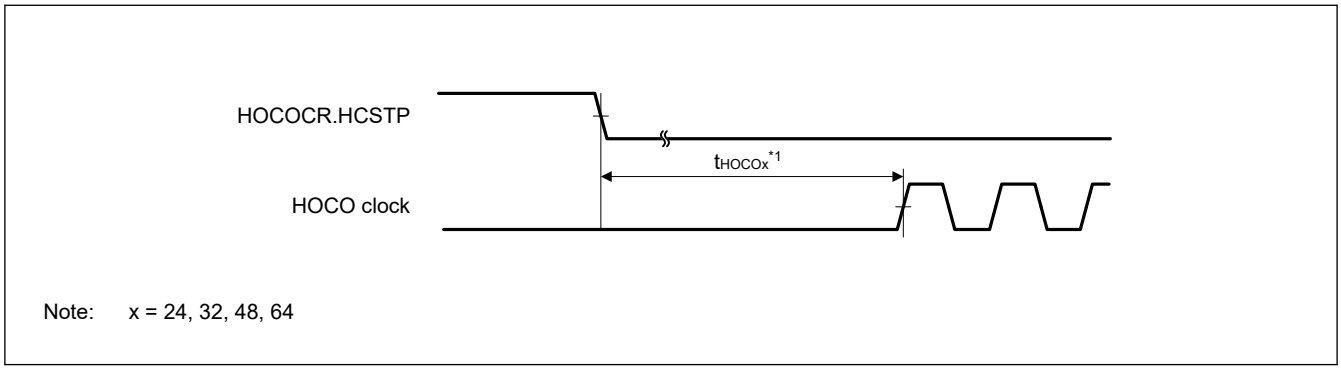


Figure 2.5 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

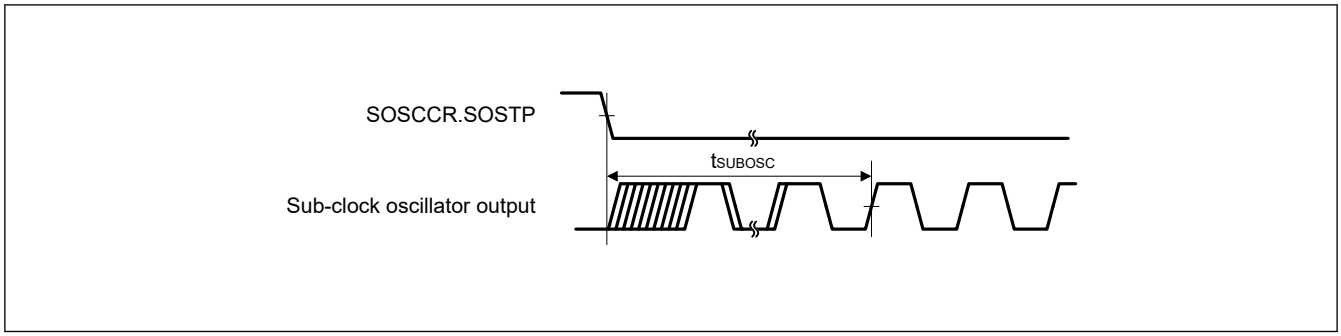


Figure 2.6 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.21 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	10	—	—	ms	Figure 2.7
	Not at power-on	t_{RESW}	30	—	—	μs	Figure 2.8
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 2.7
	LVD0 disabled*2		—	0.2	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.8
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.9
	LVD0 disabled*2		—	0.15	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

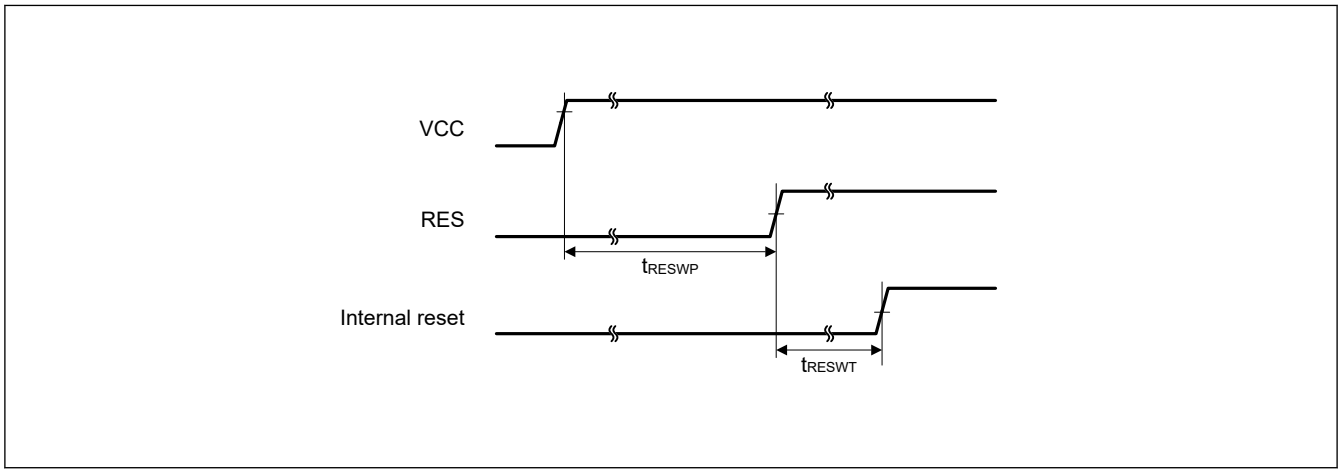


Figure 2.7 Reset input timing at power-on

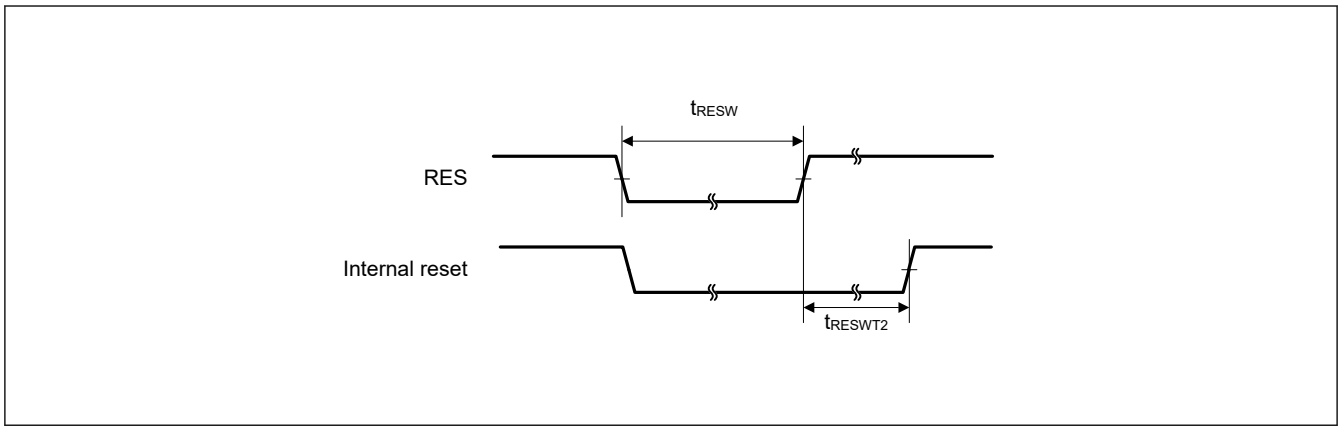


Figure 2.8 Reset input timing (1)

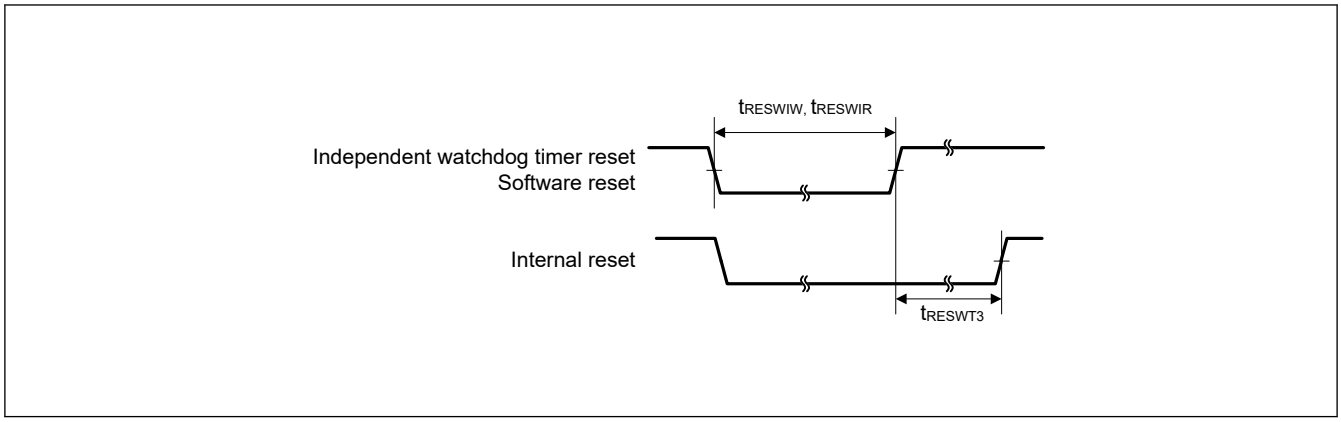


Figure 2.9 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.22 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	—	2.4	3.1	µs	
		System clock source is HOCO (HOCO clock is 32 MHz)*4		t_{SBYHO}	—	7.4	9.1	µs	
		System clock source is HOCO (HOCO clock is 48 MHz)*5		t_{SBYHO}	—	7.3	8.9	µs	
		System clock source is HOCO (HOCO clock is 64 MHz)*4		t_{SBYHO}	—	7.4	9.1	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	4	5	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 32 MHz.
Note 5. The system clock is 48 MHz.

Table 2.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (20 MHz)*3 VCC = 1.6 V to 1.8 V		—	11.7	13		
		System clock source is HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	
			VCC = 1.6 V to 1.8 V	t_{SBYMO}	—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V		—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

Table 2.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Table 2.25 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	—	0.85	1	ms	Figure 2.10
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

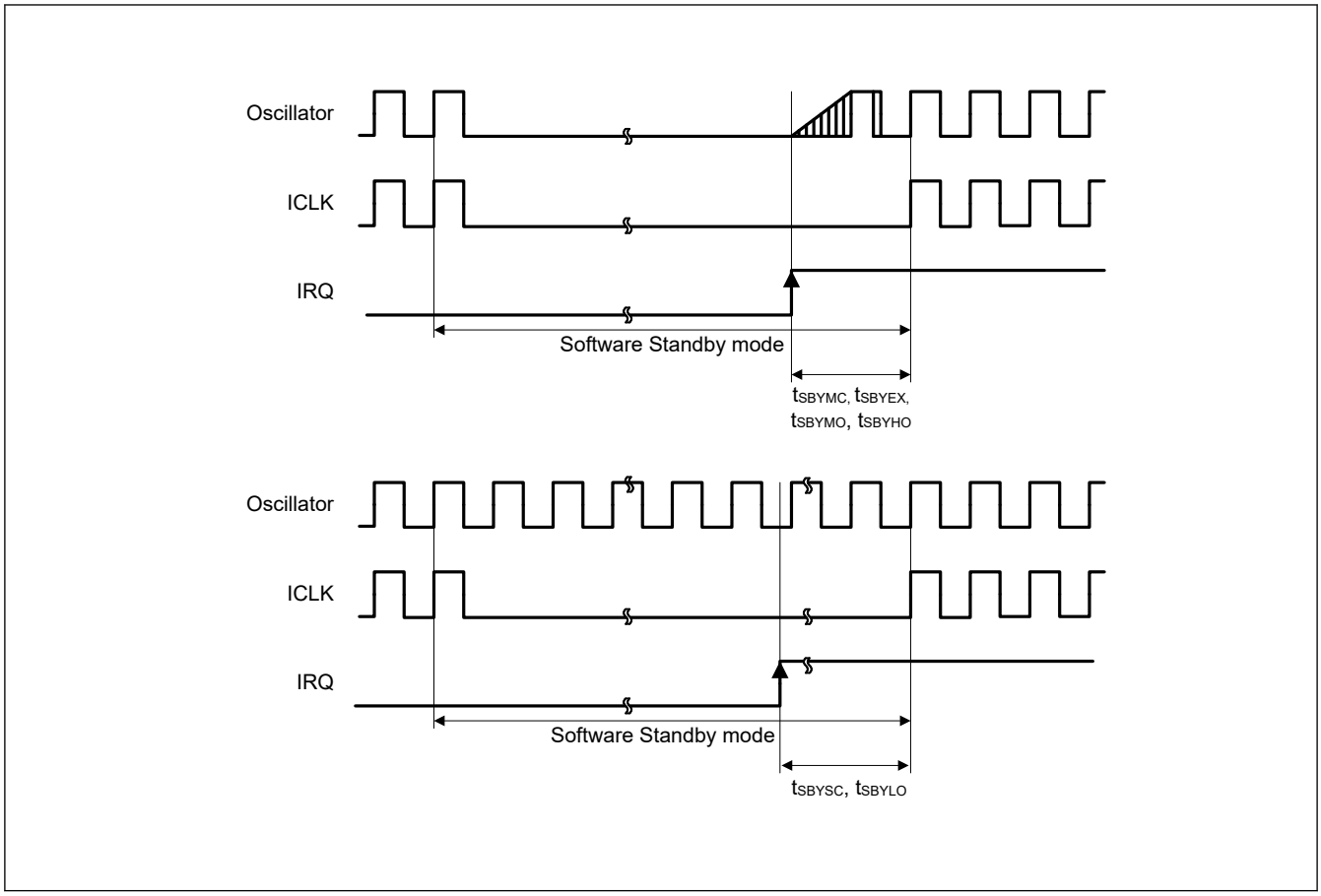
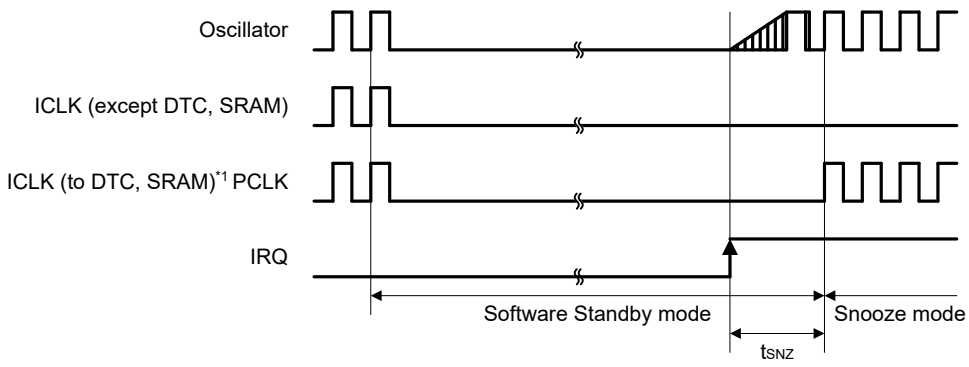


Figure 2.10 Software Standby mode cancellation timing

Table 2.26 Timing of recovery from low power modes (5)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	6.6	8.1	µs	Figure 2.11
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	6.7	8.2	µs	
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	10.8	12.9	µs	
	Low-speed mode System clock source is MOCO (2 MHz)	t_{SNZ}	—	6.7	8.0	µs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.11 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.27 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

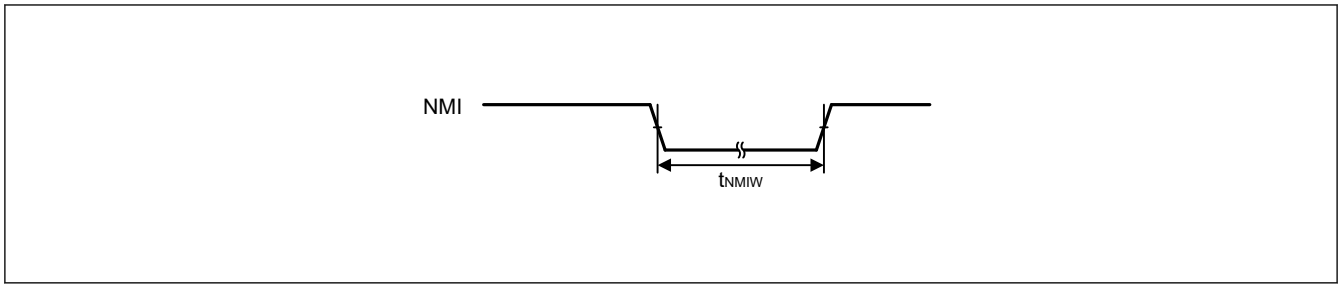


Figure 2.12 NMI interrupt input timing

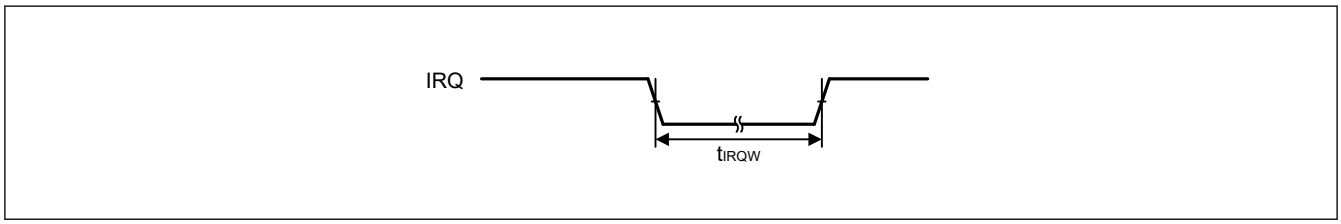


Figure 2.13 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGTW, KINT, and ADC12 Trigger Timing

Table 2.28 I/O Ports, POEG, GPT, AGT, KINT, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.14
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.15
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.16
		Dual edge		2.5	—		
AGTW	AGTIO, AGTEE input cycle	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	—	ns	Figure 2.17
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO, AGTEE input high-level width, low-level width	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 2.17
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.18
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	—	ns	Figure 2.19

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

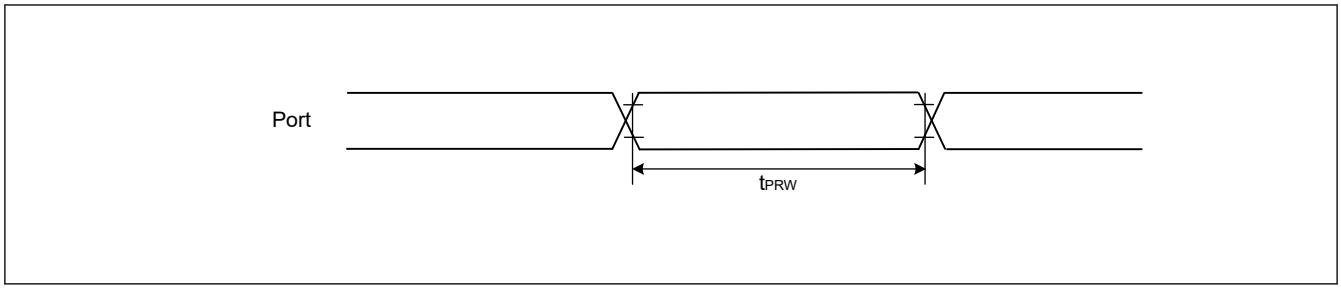


Figure 2.14 I/O ports input timing

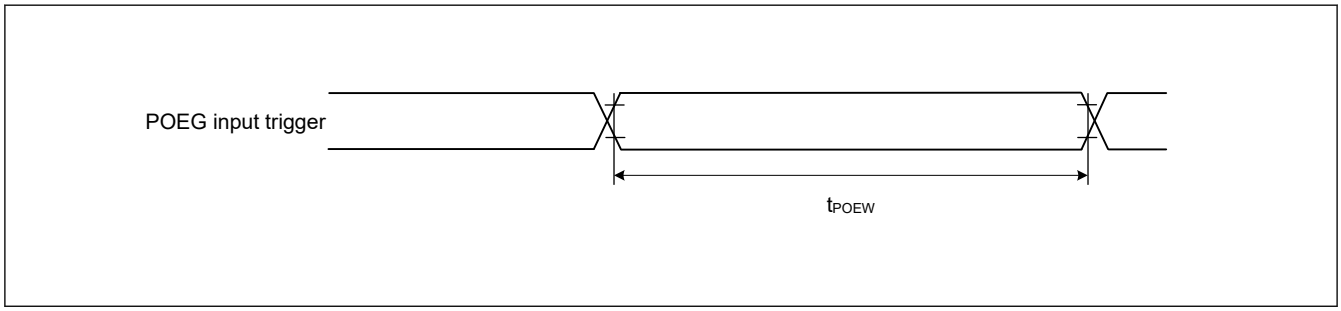


Figure 2.15 POEG input trigger timing

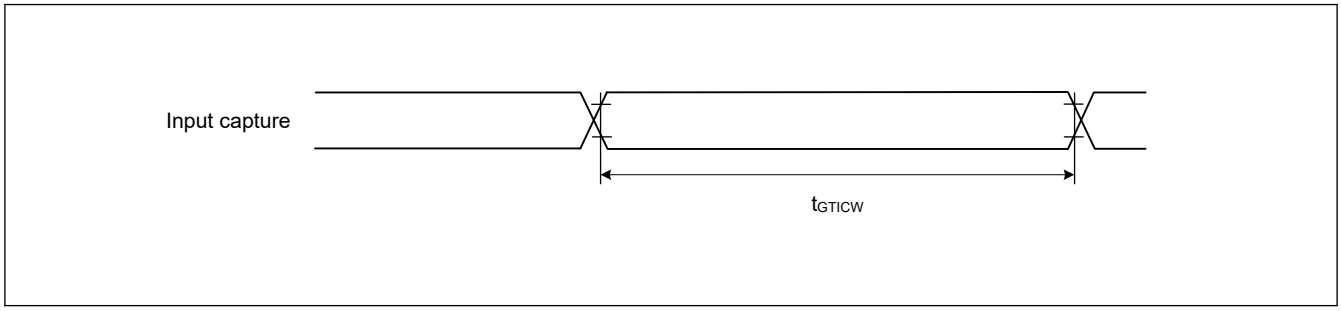


Figure 2.16 GPT input capture timing

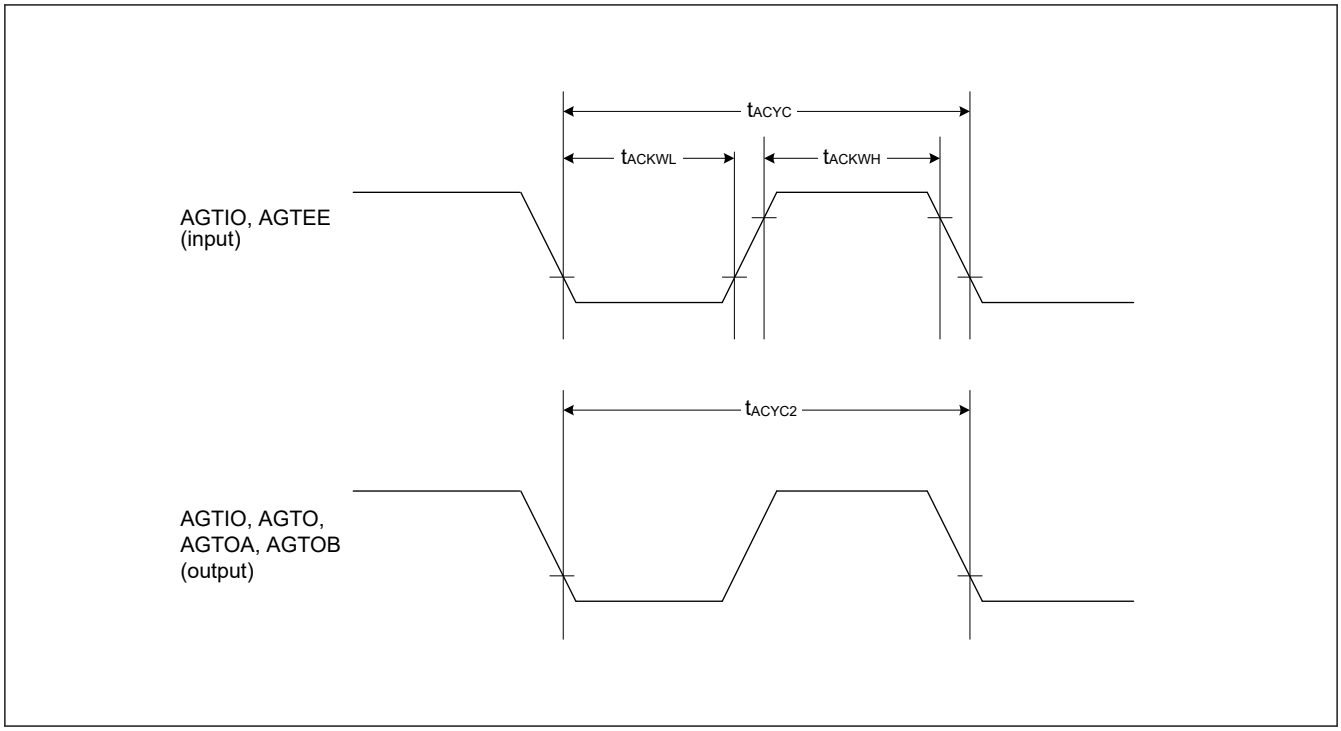


Figure 2.17 AGTW I/O timing

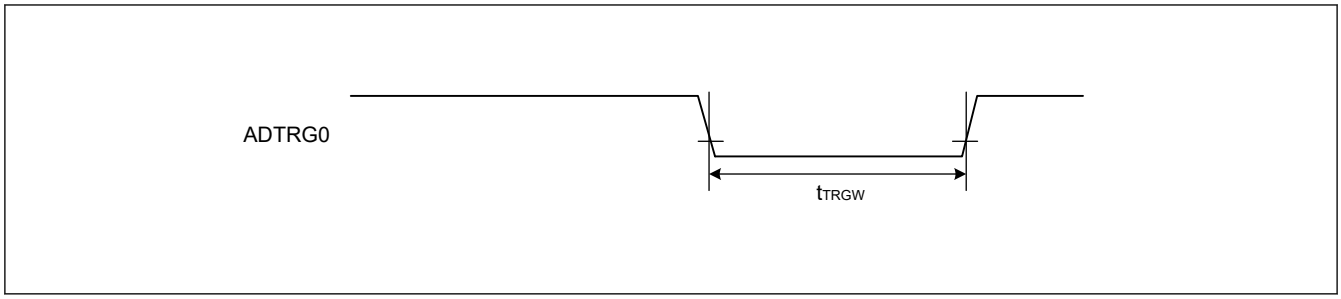


Figure 2.18 ADC12 trigger input timing

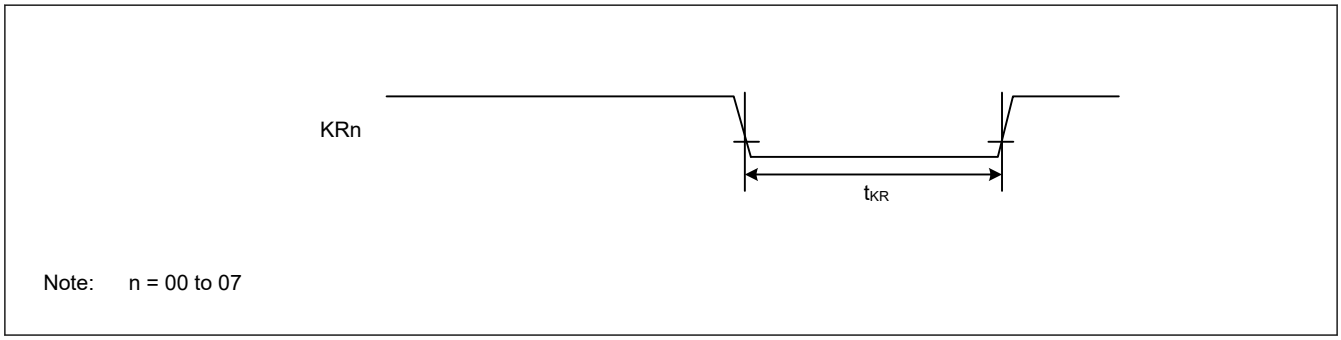


Figure 2.19 Key interrupt input timing

2.3.7 CAC Timing

Table 2.29 CAC timing

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

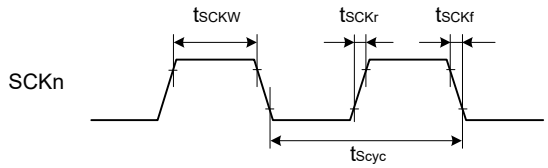
Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{CAC}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.30 SCI timing (1)

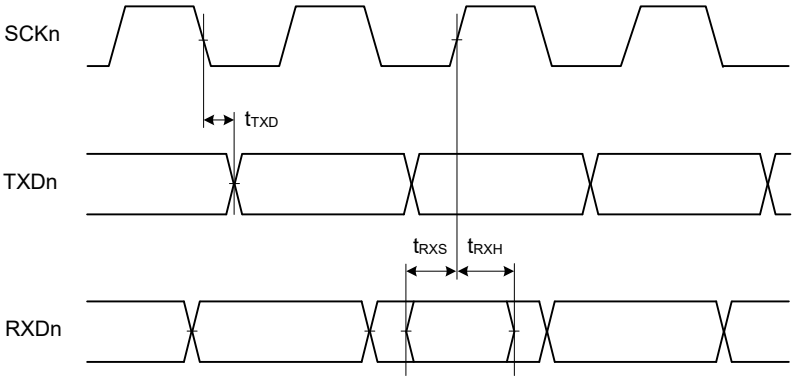
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 2.20
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		125	—		
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Transmit data delay time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 2.21
			1.6 V ≤ VCC < 1.8 V		—	45		
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		90	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Receive data setup time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 2.7 V		45	—		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	—	ns	



Note: n = 0 to 2, 9

Figure 2.20 SCK clock input timing



Note: n = 0 to 2, 9

Figure 2.21 SCI input/output timing in clock synchronous mode

Table 2.31 SCI timing (2) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

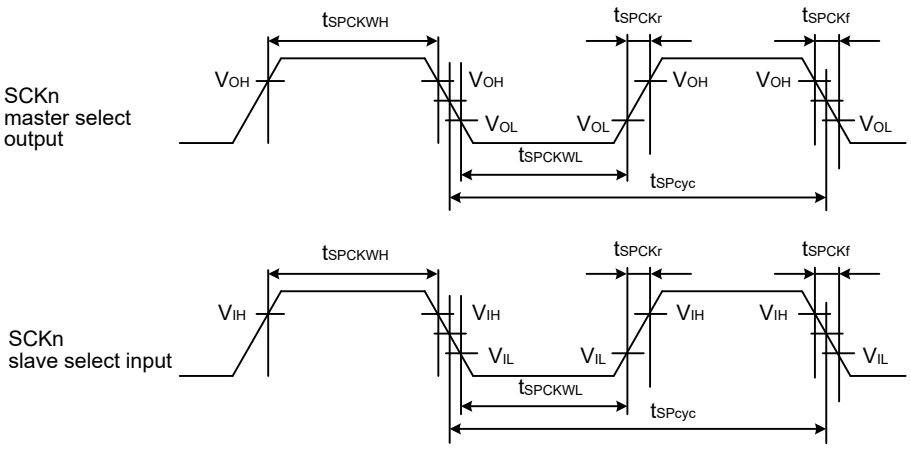
Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 2.22
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK clock cycle input (slave)		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	Figure 2.23 to Figure 2.26
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 2.7 V		45	—		
	Data input hold time	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
			2.4 V ≤ VCC < 2.7 V		-20	—		
			1.8 V ≤ VCC < 2.4 V		-30	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-10	—		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 2.31 SCI timing (2) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 2.26
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

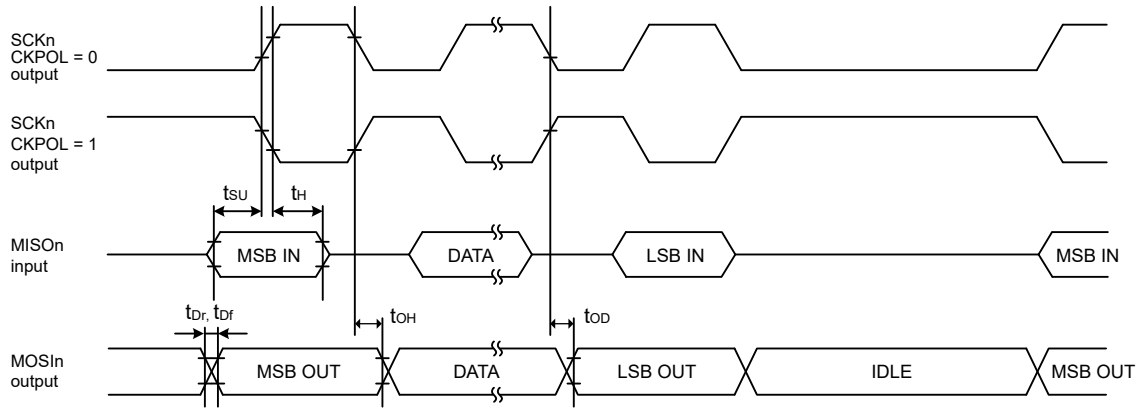
Note 1. t_{Pcyc}: PCLKB cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

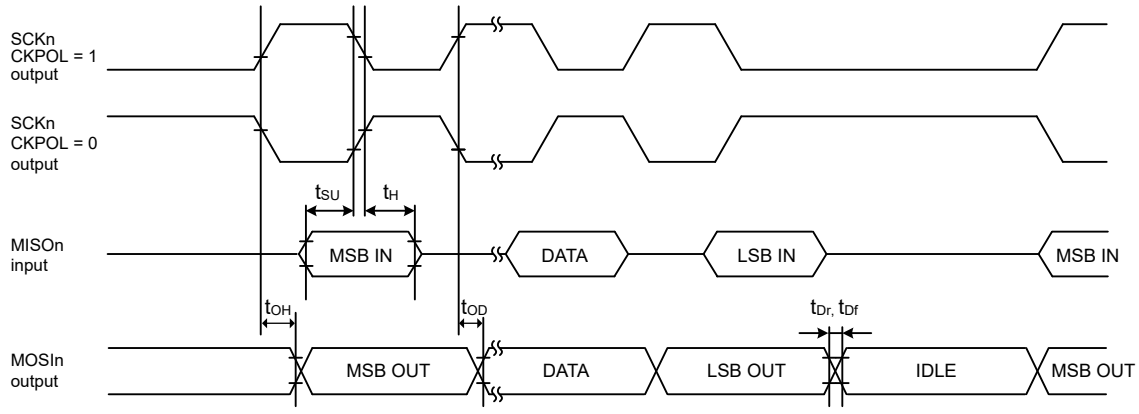
Note: n = 0 to 2, 9

Figure 2.22 SCI simple SPI mode clock timing



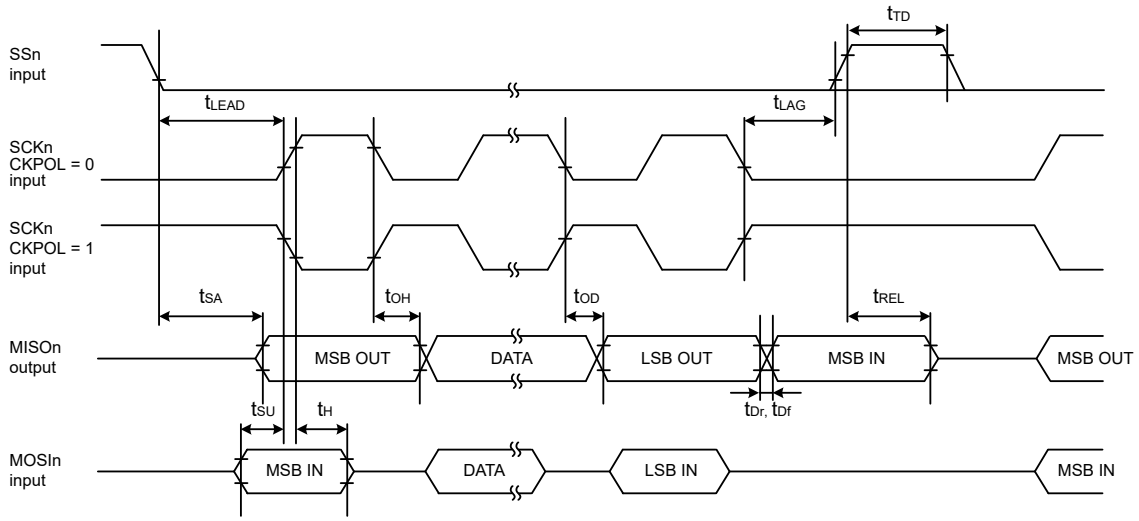
Note: n = 0 to 2, 9

Figure 2.23 SCI simple SPI mode timing (master, CKPH = 1)



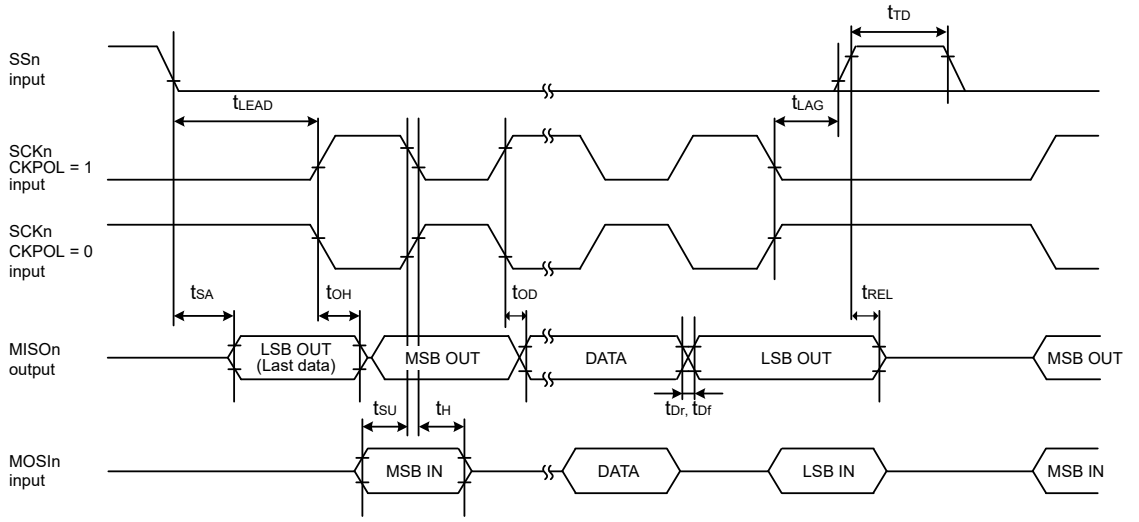
Note: n = 0 to 2, 9

Figure 2.24 SCI simple SPI mode timing (master, CKPH = 0)



Note: n = 0 to 2, 9

Figure 2.25 SCI simple SPI mode timing (slave, CKPH = 1)



Note: n = 0 to 2, 9

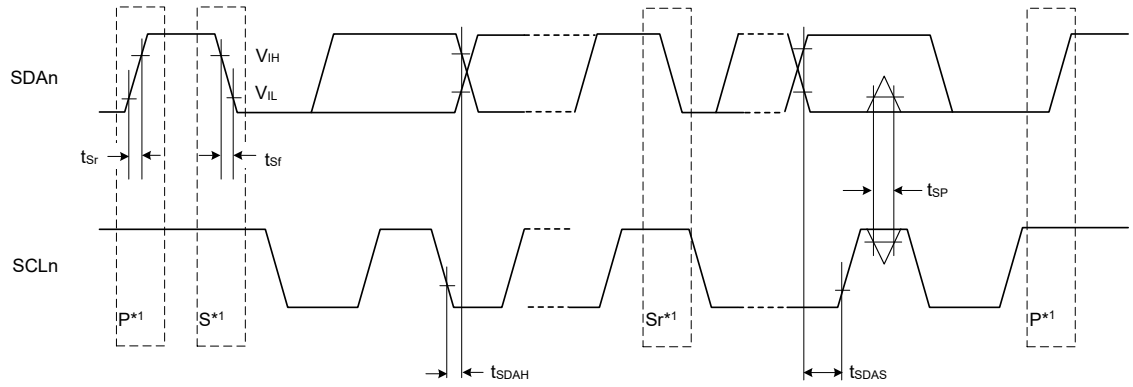
Figure 2.26 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.32 SCI timing (3)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0 to 2, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.27 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.33 SPI timing (1 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	62.5	—	ns	Figure 2.28 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		125	—		
			1.8 V ≤ VCC < 2.4 V		250	—		
			1.6 V ≤ VCC < 1.8 V		500	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC ≤ 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	0.1	µs/V	

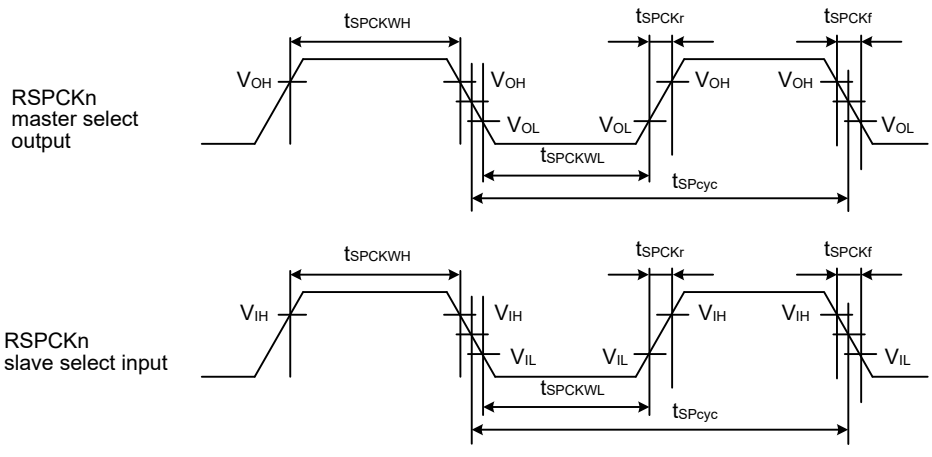
Table 2.33 SPI timing (2 of 3)

Parameter					Symbol	Min	Max	Unit*1	Test conditions
SPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{SU}	10	—	ns	Figure 2.29 to Figure 2.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V	16 MHz < PCLKB ≤ 32 MHz		30	—		
				PCLKB ≤ 16 MHz		10	—		
			1.8 V ≤ VCC < 2.4 V	16 MHz < PCLKB ≤ 32 MHz		55	—		
				8 MHz < PCLKB ≤ 16 MHz		30	—		
				PCLKB ≤ 8 MHz		10	—		
			1.6 V ≤ VCC < 1.8 V			10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V			10	—		
			1.8 V ≤ VCC < 2.4 V			15	—		
			1.6 V ≤ VCC < 1.8 V			20	—		
	Data input hold time	Master (RSPCK is PCLKB/2)			t_{HF}	0	—	ns	
		Master (RSPCK is not PCLKB/2)			t_{H}	t_{Pcyc}	—		
		Slave			t_{H}	20	—		
SPI	SSL setup time	Master	1.8 V ≤ VCC ≤ 5.5 V		t_{LEAD}	-30 + N × t_{SPcyc}*2	—	ns	
			1.6 V ≤ VCC < 1.8 V			-50 + N × t_{SPcyc}*2	—		
		Slave				6 × t_{Pcyc}	—	ns	
	SSL hold time	Master			t_{LAG}	-30 + N × t_{SPcyc}*3	—	ns	
		Slave				6 × t_{Pcyc}	—	ns	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V			—	20		
			1.8 V ≤ VCC < 2.4 V			—	25		
			1.6 V ≤ VCC < 1.8 V			—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V			—	50		
			2.4 V ≤ VCC < 2.7 V			—	60		
			1.8 V ≤ VCC < 2.4 V			—	85		
			1.6 V ≤ VCC < 1.8 V			—	110		
	Data output hold time	Master			t_{OH}	0	—	ns	
		Slave				0	—		
	Successive transmission delay time	Master			t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave				6 × t_{Pcyc}	—		

Table 2.33 SPI timing (3 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	Figure 2.29 to Figure 2.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	Slave access time		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{Pcyc} + 100	ns	Figure 2.33 and Figure 2.34 C = 30 pF
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		
	Slave output release time		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A

Figure 2.28 SPI clock timing

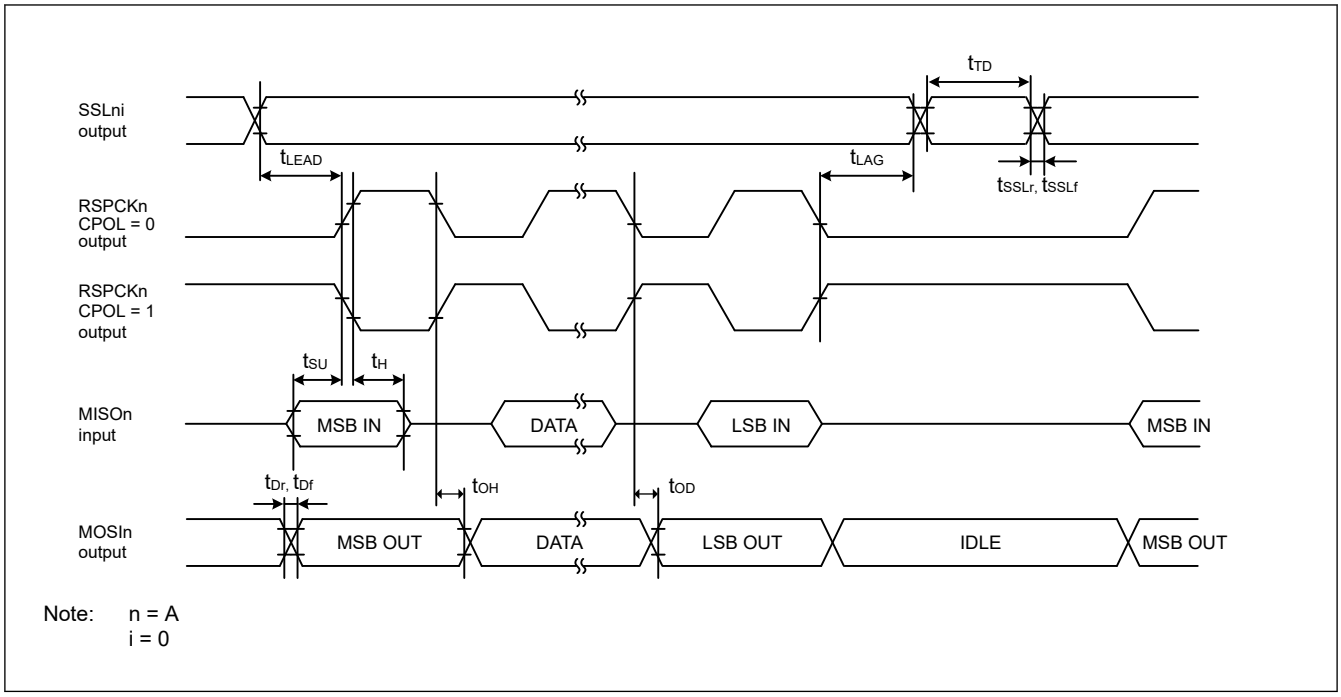


Figure 2.29 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

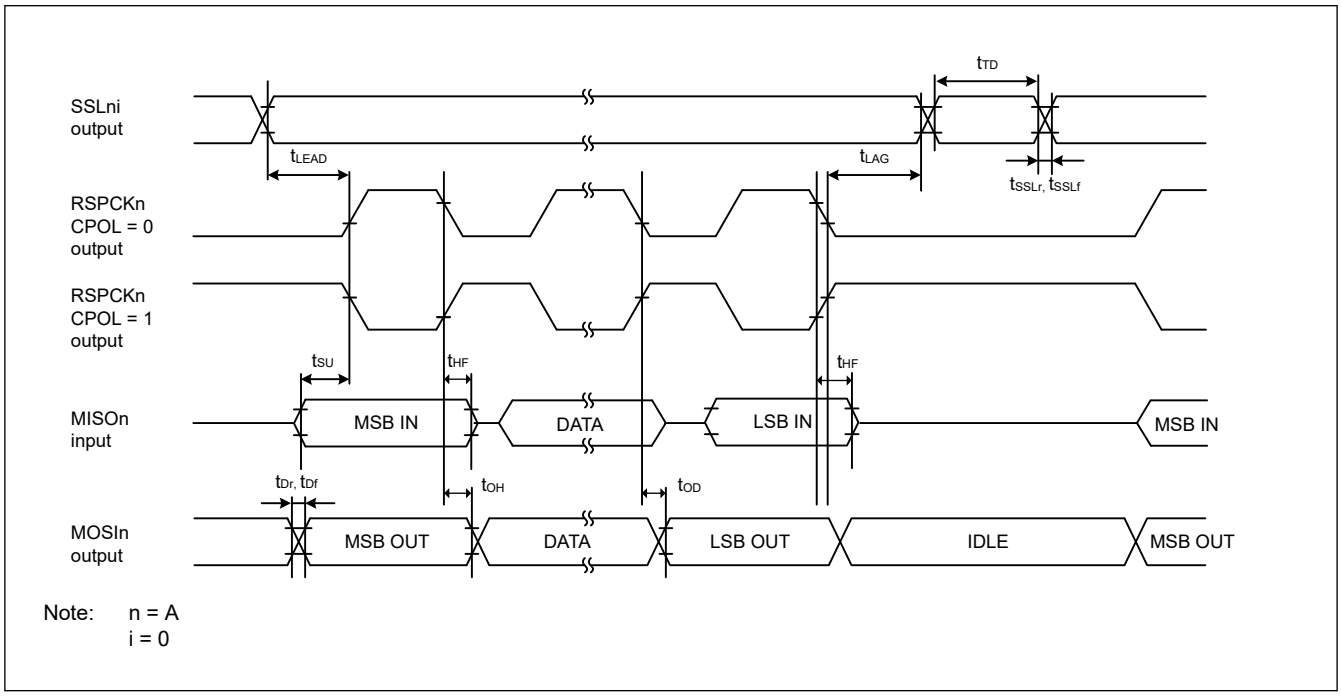


Figure 2.30 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

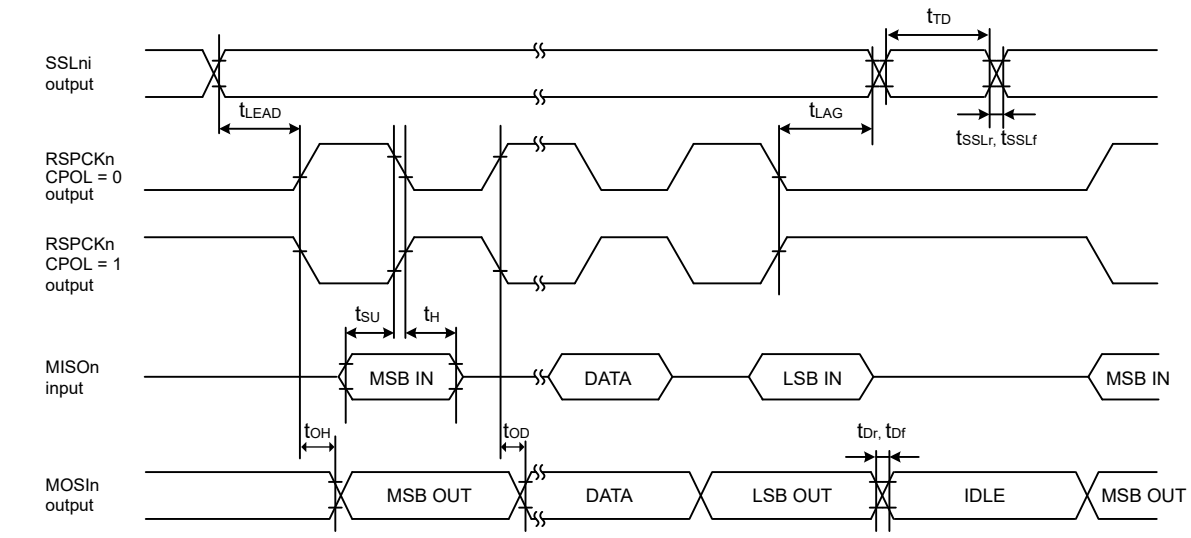


Figure 2.31 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

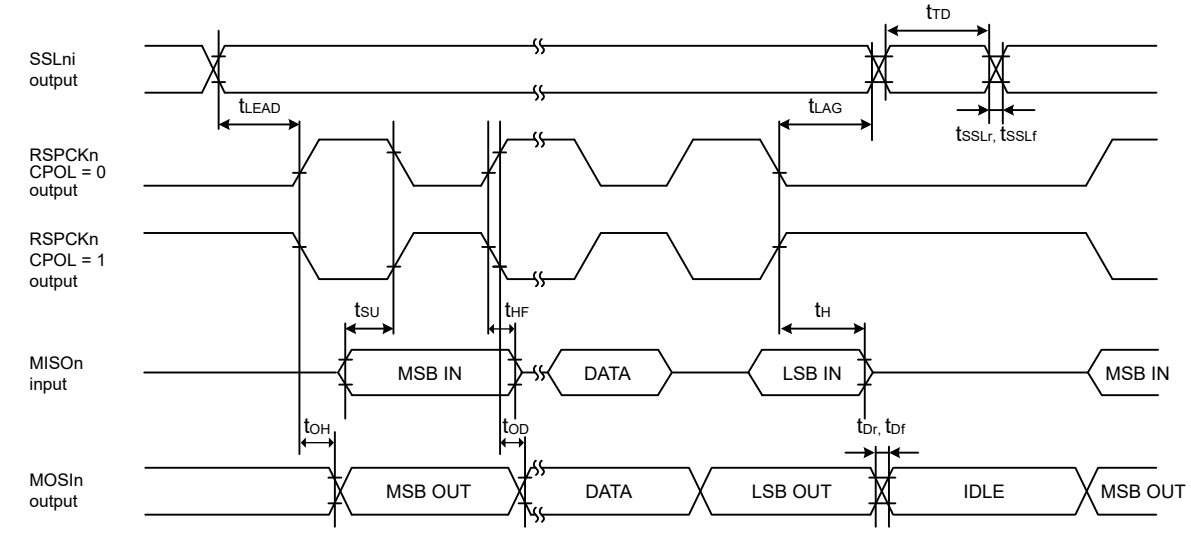


Figure 2.32 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

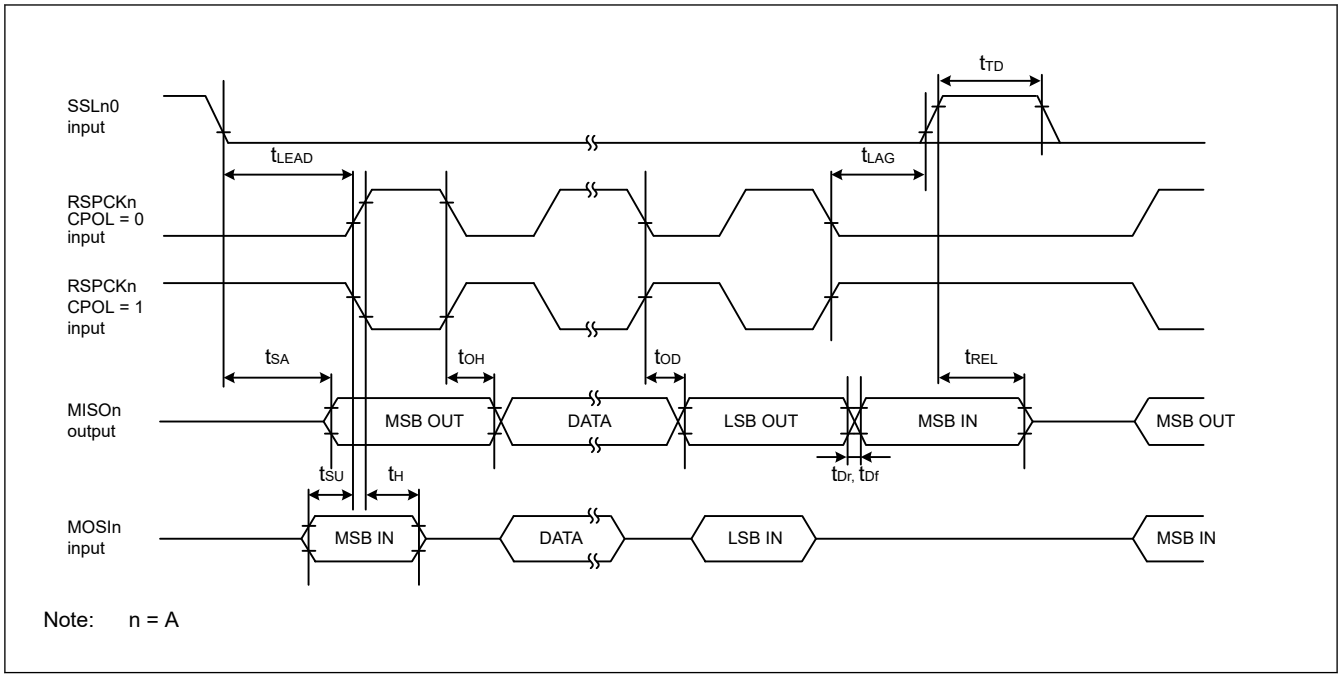


Figure 2.33 SPI timing (slave, CPHA = 0)

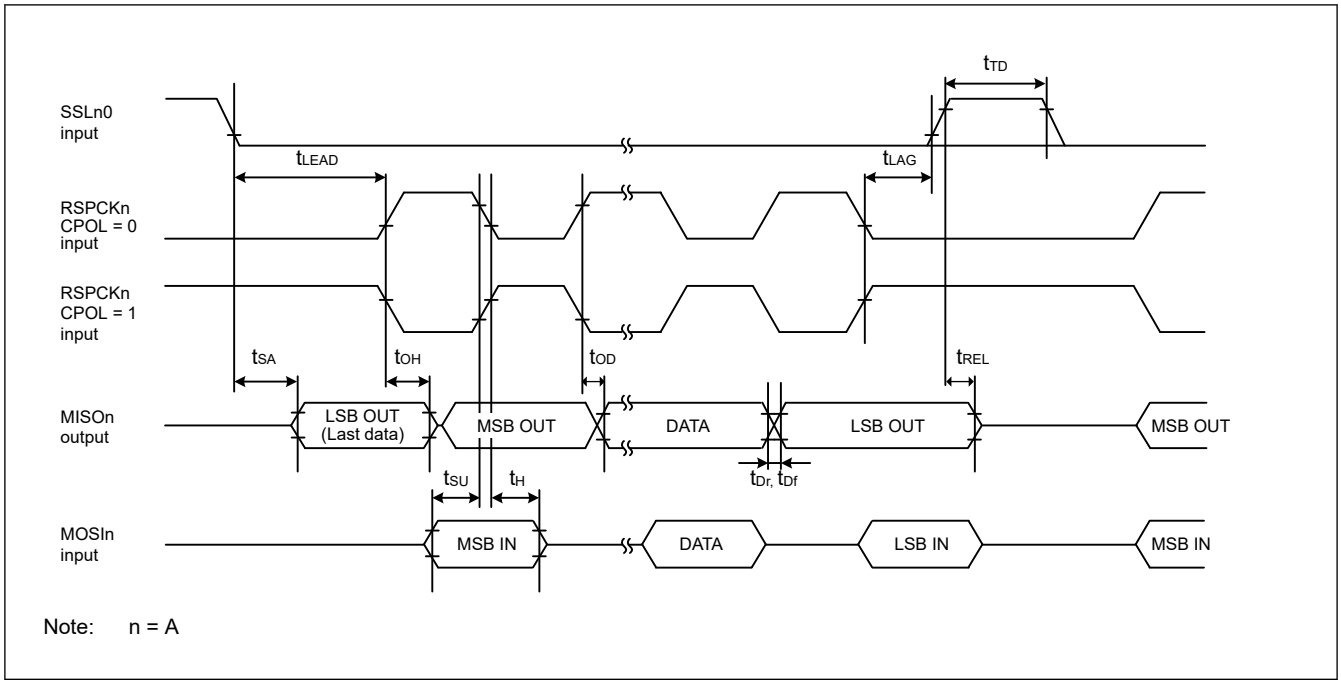


Figure 2.34 SPI timing (slave, CPHA = 1)

2.3.10 I3C Timing

Table 2.34 IIC timing

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 1300	—	ns	Figure 2.35
	SCL high pulse width	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 800	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (16) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	1000	—	ns	
	Setup time for STOP condition	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast mode)	SCL cycle time	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 600	—	ns	Figure 2.35
	SCL high pulse width	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (16) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	300	—	ns	
	Setup time for STOP condition	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with DNFE.DNFE set to 1.

Table 2.35 IIC timing (Fast-mode+)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (Fast-mode+)	SCL cycle time	t_{SCL}	6 (40) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	ns	Figure 2.35
	SCL high pulse width	t_{SCLH}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL low pulse width	t_{SCLL}	3 (20) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL, SDA rise time	t_{Sr}	—	120	ns	
	SCL, SDA fall time	t_{Sf}	—	120	ns	
	SCL, SDA spike pulse removal time	t_{SP}	—	1 (16) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (20) × t_{IICcyc} + 120	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	260	—	ns	
	Setup time for STOP condition	t_{STOS}	260	—	ns	
	Data setup time	t_{SDAS}	50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle.

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1.

Table 2.36 IIC timing (HS mode)

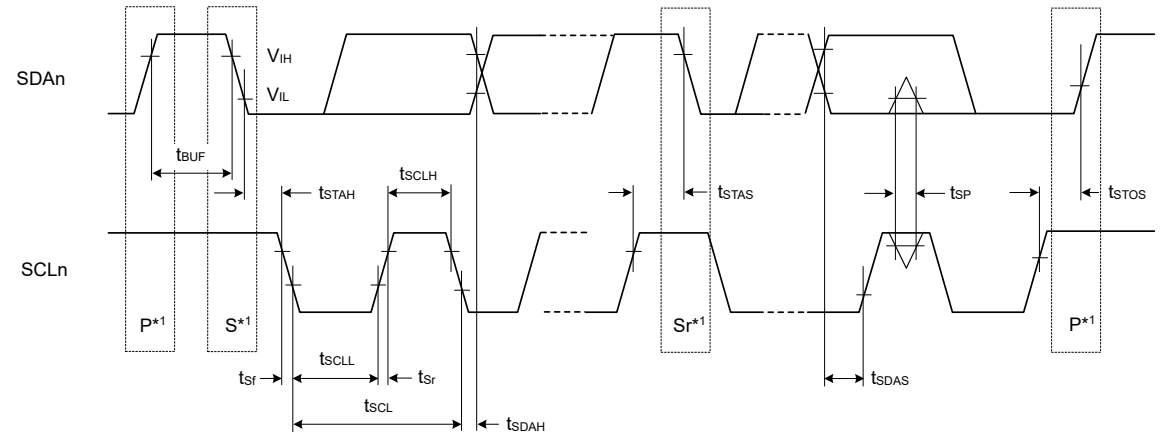
Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Cb = 100 pF		Cb = 400 pF		Unit	Test conditions
			Min*1	Max	Min*1	Max		
IIC (HS mode)	SCL cycle time	t_{SCL}	330 (+ 10 × t_{IICcyc}) when PCLKD = 64 MHz 390 (+ 10 × t_{IICcyc}) when PCLKD = 48 MHz	—	500 (+ 10 × t_{IICcyc}) when PCLKD = 64 MHz *2 560 (+ 10 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	Figure 2.35
	SCL high pulse width	t_{SCLH}	125 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 155 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	140 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 170 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	
	SCL low pulse width	t_{SCLL}	205 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 230 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	320 (+ 5 × t_{IICcyc}) when PCLKD = 64 MHz 350 (+ 5 × t_{IICcyc}) when PCLKD = 48 MHz	—	ns	
	SCL rise time	t_{Sr}	—	40	—	80	ns	
	SCL rise time after a repeated START condition and after an acknowledge bit	t_{Sr}	—	80	—	160	ns	
	SCL fall time	tSf	—	40	—	80	ns	
	SDA fall time	t_{Sf}	—	80	—	160	ns	
	SDA fall time	t_{Sf}	—	80	—	160	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	0	1 (4) × t_{IICcyc}	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	160	—	160	—	ns	
	Setup time for STOP condition	t_{STOS}	160	—	160	—	ns	
	Data setup time	t_{SDAS}	10	—	10	—	ns	
	Data hold time	t_{SDAH}	0	80	0	150	ns	
	SCL, SDA capacitive load	C_b	—	100	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle.

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1.

Note 2. The maximum SCL clock frequency is 1.7MHz.



Note: n = 0
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.35 I²C bus interface input/output timing

Table 2.37 I3C timing (Open Drain Timing Parameters)

Conditions: VCC = 2.97 to 3.63 V

Parameter	Symbol	Timing Diagram	Min	Max	Units	Notes
SCL Clock Low Period	t_{LOW_OD}	Figure 2.38	200	—	ns	1, 2
	$t_{DIG\_OD\_L}$	Figure 2.38	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	—
SDA Signal Fall Time	t_{fDA_OD}	Figure 2.38	t_{CF}	33	ns	—
SDA Data Setup Time Open Drain Mode	t_{SU_OD}	Figure 2.37	4	—	ns	1
		Figure 2.38				
Clock After START (S) Condition	t_{CAS}	Figure 2.38	38.4	For ENTAS0: 1 µ	seconds	5, 6
				For ENTAS1: 100 µ		
				For ENTAS2: 2 m		
				For ENTAS3: 50 m		
Clock Before STOP (P) Condition	t_{CBP}	Figure 2.39	t_{CASmin}	—	seconds	—
Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	Figure 2.44	$t_{DIG\_OD\_Lmin}$	—	ns	—
Bus Available Condition	t_{AVAL}	—	1	—	µs	7
Bus Idle Condition	t_{IDLE}	—	1	—	ms	—
Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	Figure 2.44	$t_{AVALmin}$	—	µs	—

Note:
1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_ODmin}.
2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH.
3. On a Legacy Bus where I²C Devices need to see Start.
4. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
5. On a Mixed Bus with Fm Legacy I²C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 2.38 I3C timing (Push-Pull Timing Parameters for SDR)

Parameter		Symbol	Timing Diagram	Min	Max	Units	Notes
SCL Clock Frequency		f_{SCL}	—	0.01	4.6 (when PCLKD = 64 M) 3.4 (when PCLKD = 48 M)	MHz	1
SCL Clock Low Period		t_{LOW}	Figure 2.36	80 (when PCLKD = 64 M) 104 (when PCLKD = 48 M)	—	ns	—
		t_{DIG_L}	Figure 2.36	88 (when PCLKD = 64 M) 112 (when PCLKD = 48 M)	—	ns	2,4
SCL Clock High Period		t_{HIGH}	Figure 2.36	112 (when PCLKD = 64 M) 148 (when PCLKD = 48 M)	—	ns	—
		t_{DIG_H}	Figure 2.36	120 (when PCLKD = 64 M) 156 (when PCLKD = 48 M)	—	ns	2
Clock in to Data Out for Slave		t_{SCO}	Figure 2.41	—	42	ns	—
SCL Clock Rise Time		t_{CR}	Figure 2.36	—	150 * 1 /f_{SCL} (capped at 60)	ns	—
SCL Clock Fall Time		t_{CF}	Figure 2.36	—	150 * 1 /f_{SCL} (capped at 60)	ns	—
SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP}	Figure 2.40	t_{CR} + 3 and t_{CF} + 3	—	—	4
	Slave	t_{HD_PP}	Figure 2.42	0	—	—	—
SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	Figure 2.40 Figure 2.41	4	N/A	ns	—
Clock After Repeated START (Sr)		t_{CASr}	Figure 2.43	t_{CASmin}	N/A	ns	—
Clock Before Repeated START (Sr)		t_{CBSr}	Figure 2.43	t_{CASmin}	N/A	ns	—
Capacitive Load per Bus Line (SDA/SCL)		C_b	—	—	50	pF	—

Note: 1. FSCL = 1 / (t_{DIG_L} + t_{DIG_H})

2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 2.36)

3. As both edges are used, the hold time must be satisfied for the respective edges, for example, t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

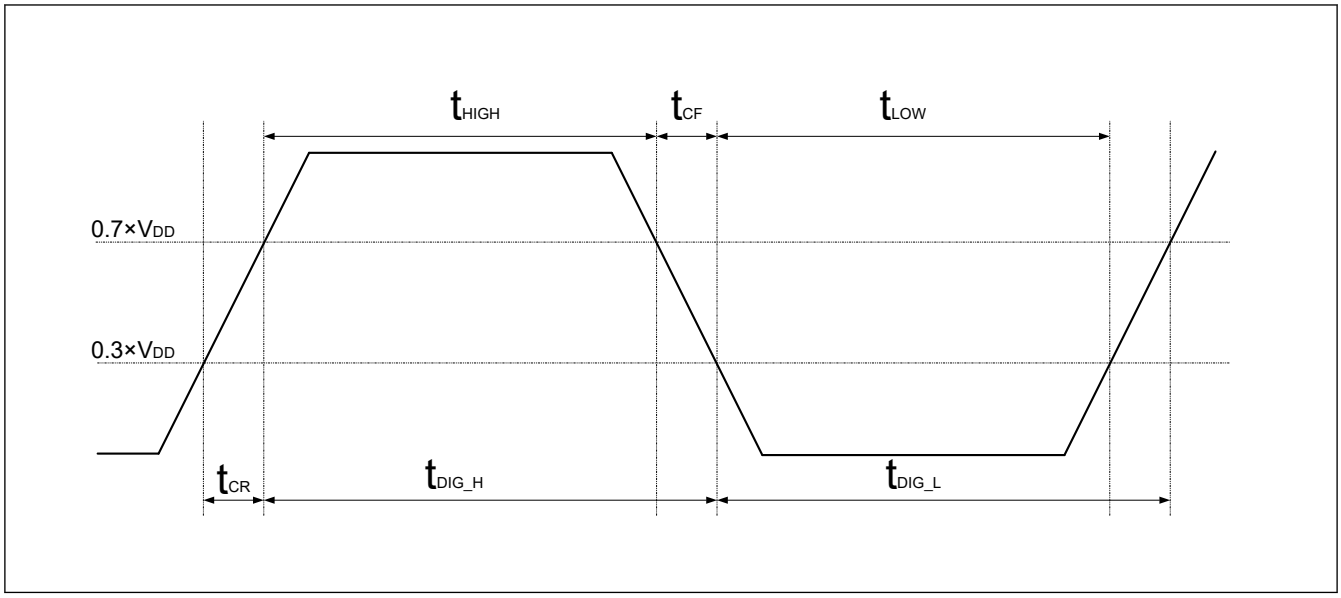


Figure 2.36 t_{DIG_H} and t_{DIG_L}

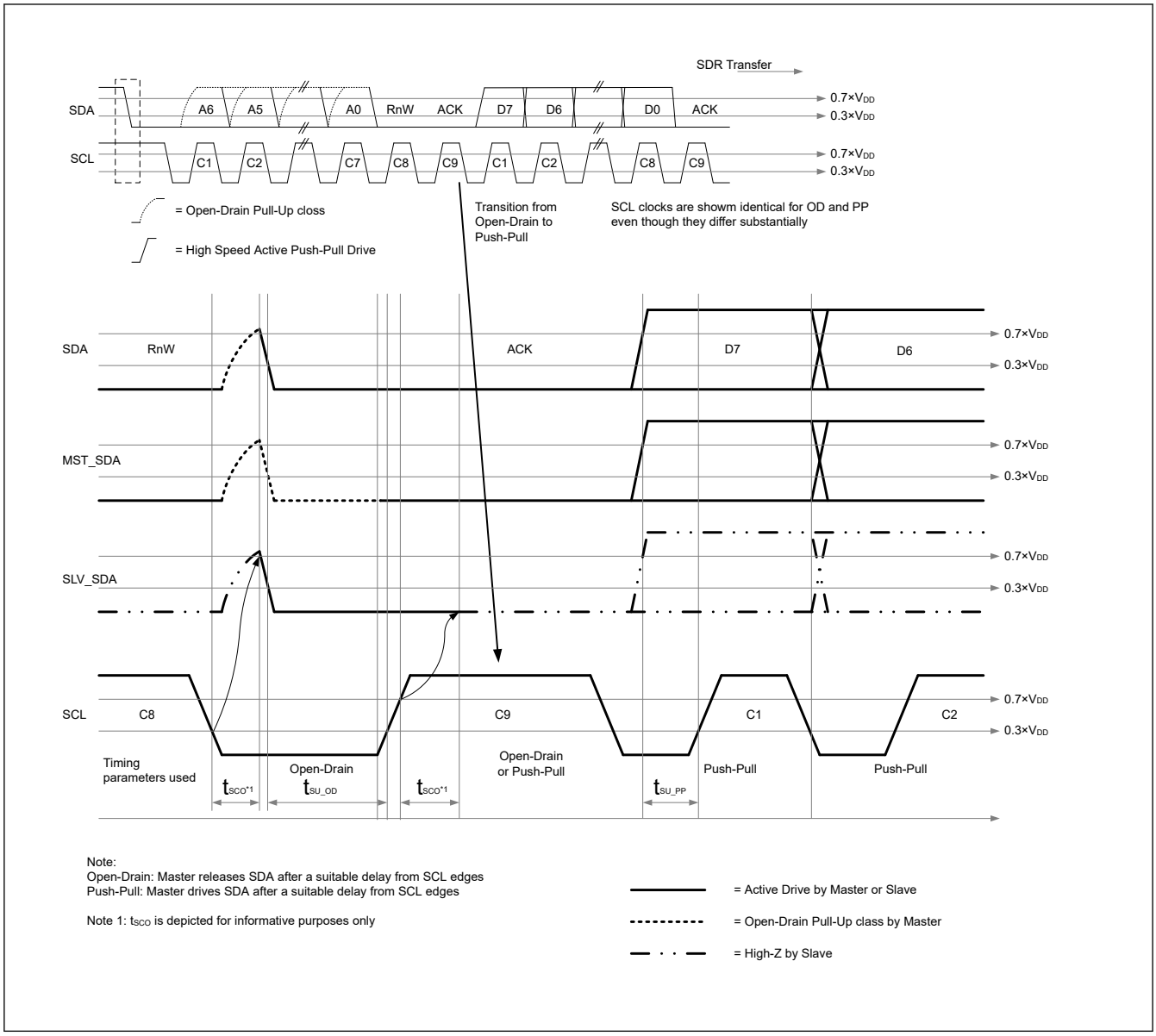


Figure 2.37 I3C Data Transfer – ACK by Slave

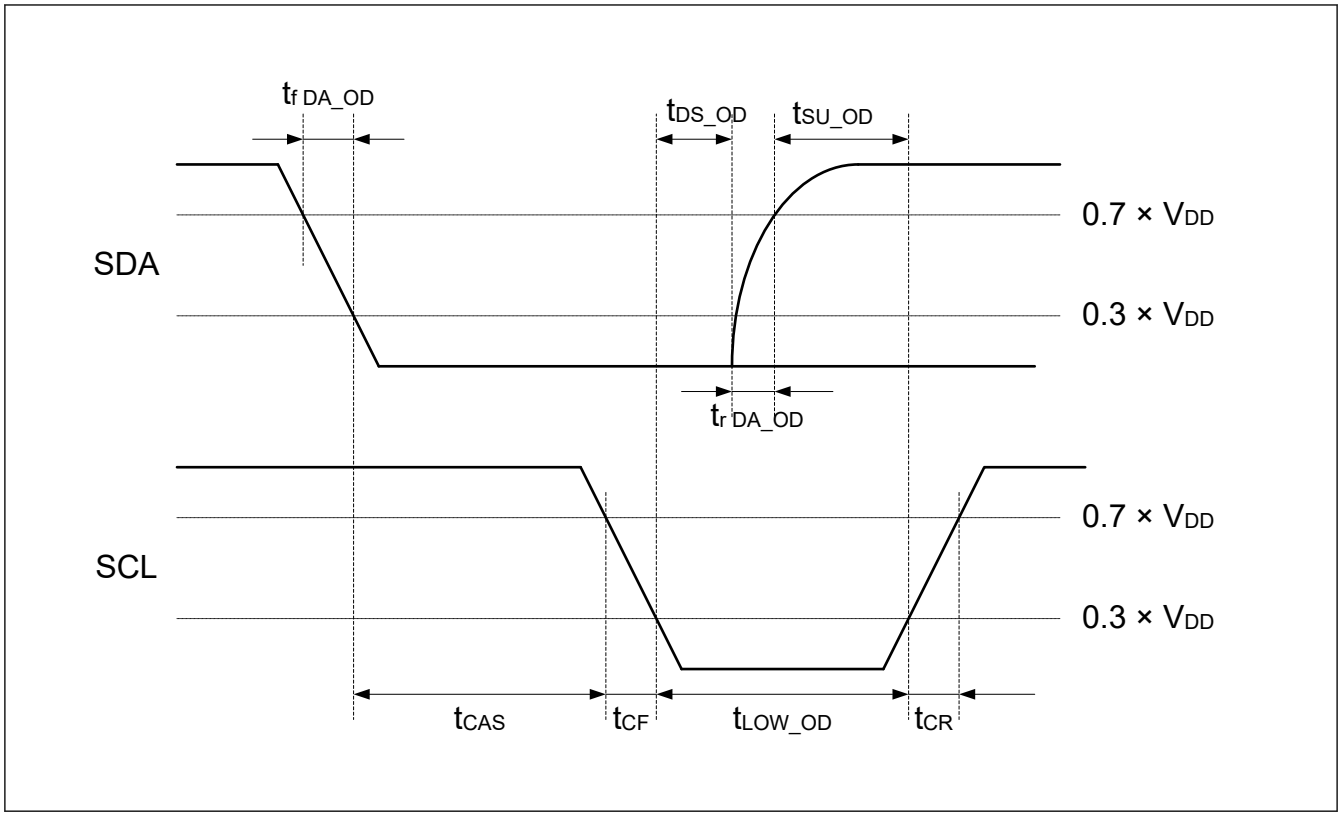


Figure 2.38 I3C START condition Timing

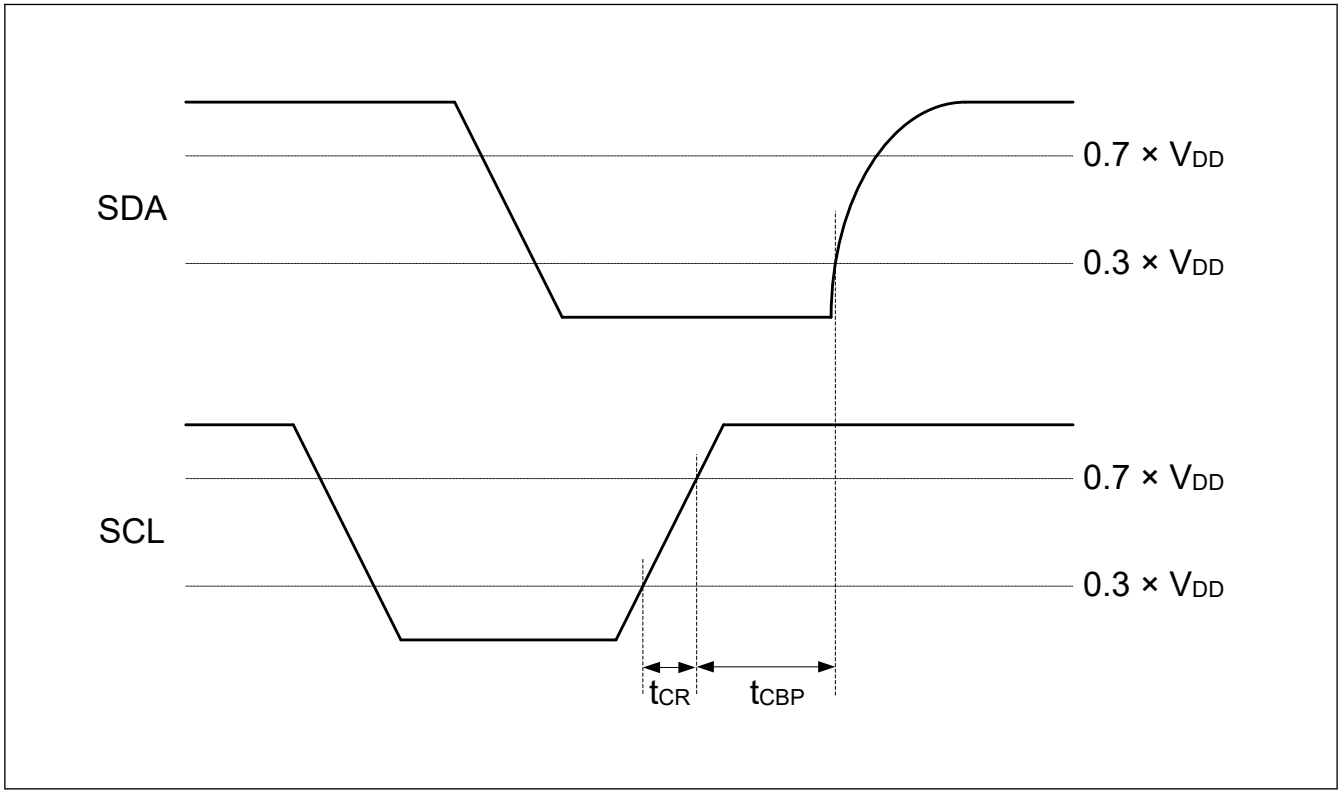


Figure 2.39 I3C STOP condition Timing

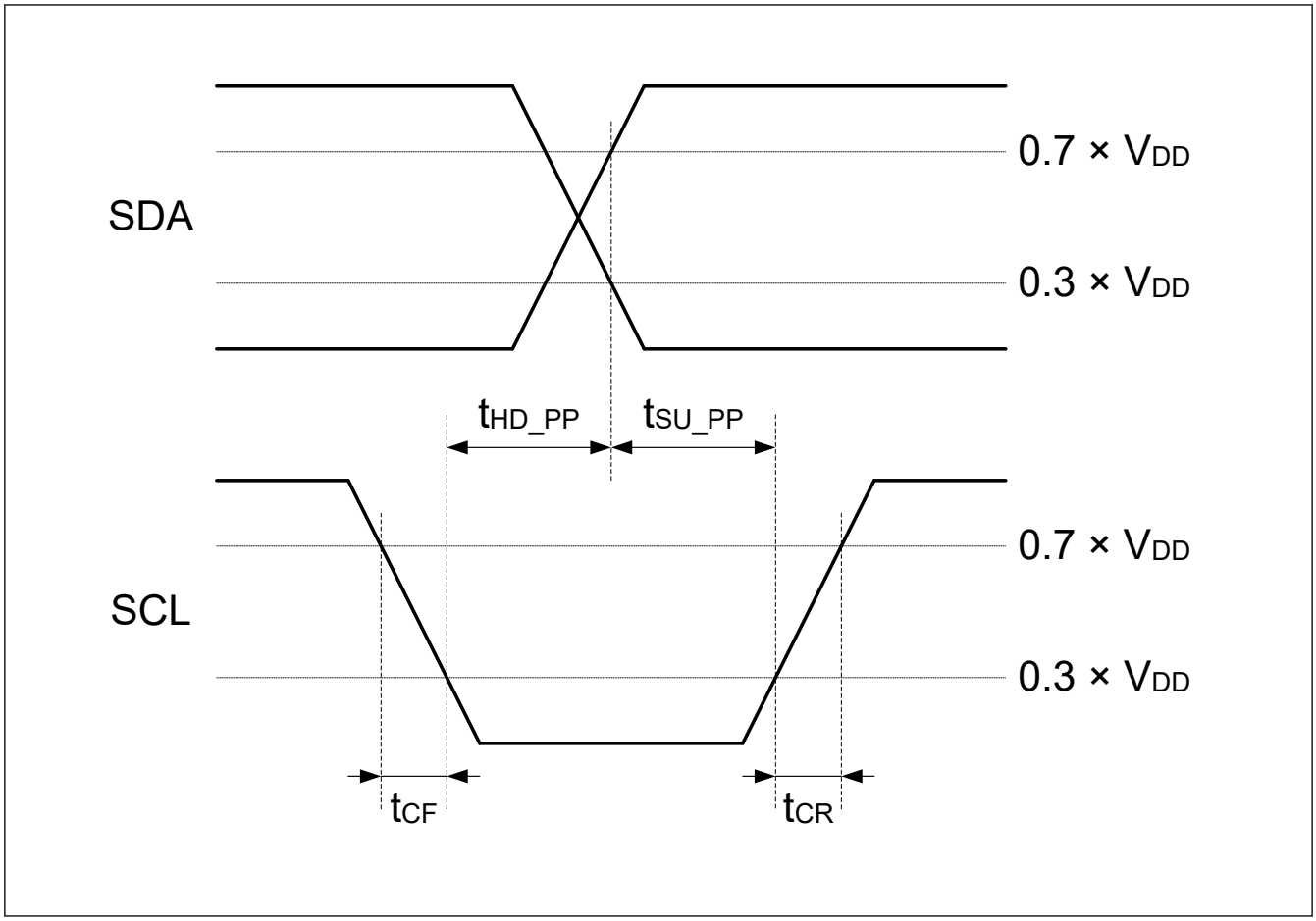


Figure 2.40 I3C Master Out Timing

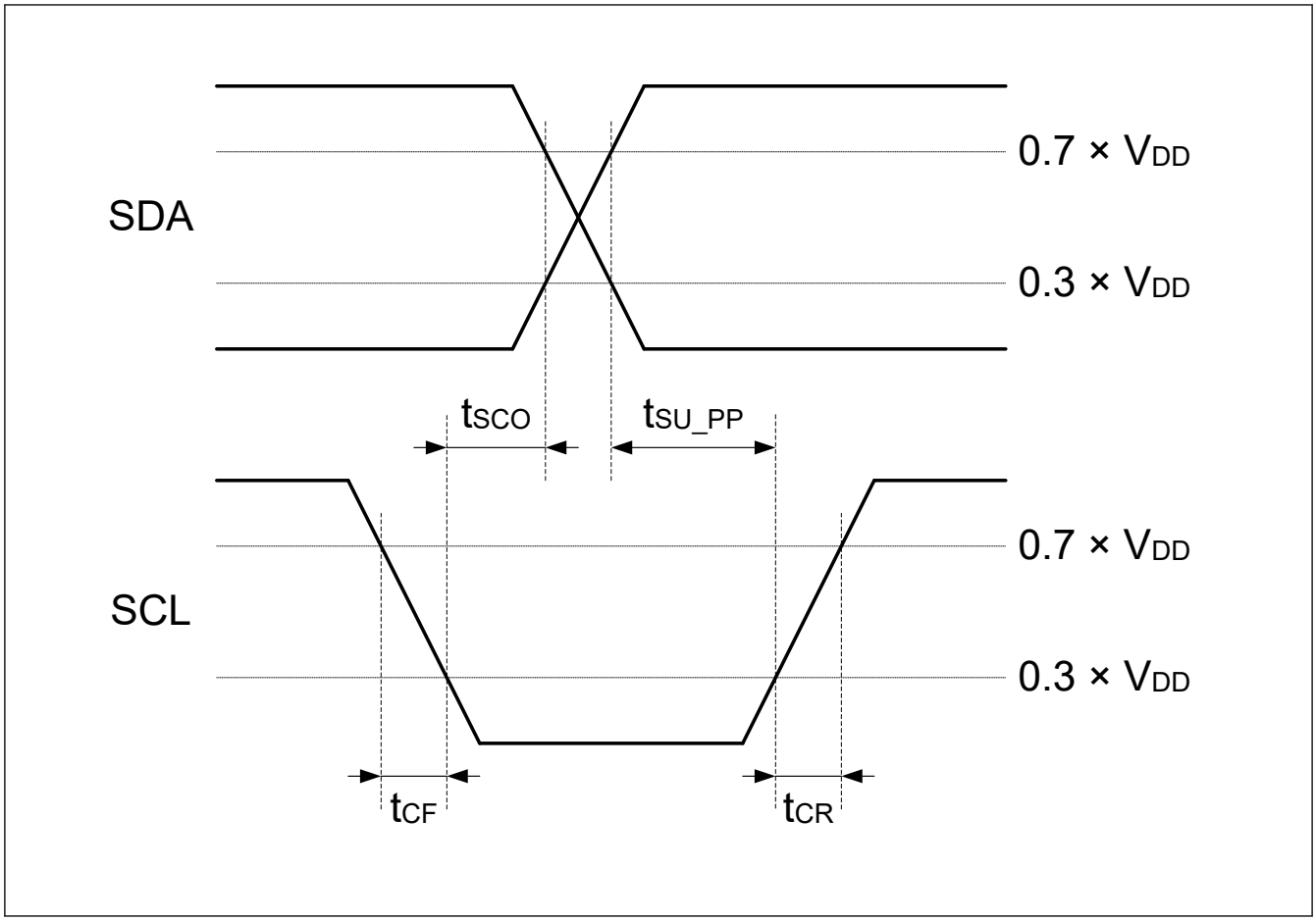


Figure 2.41 I3C Slave Out Timing

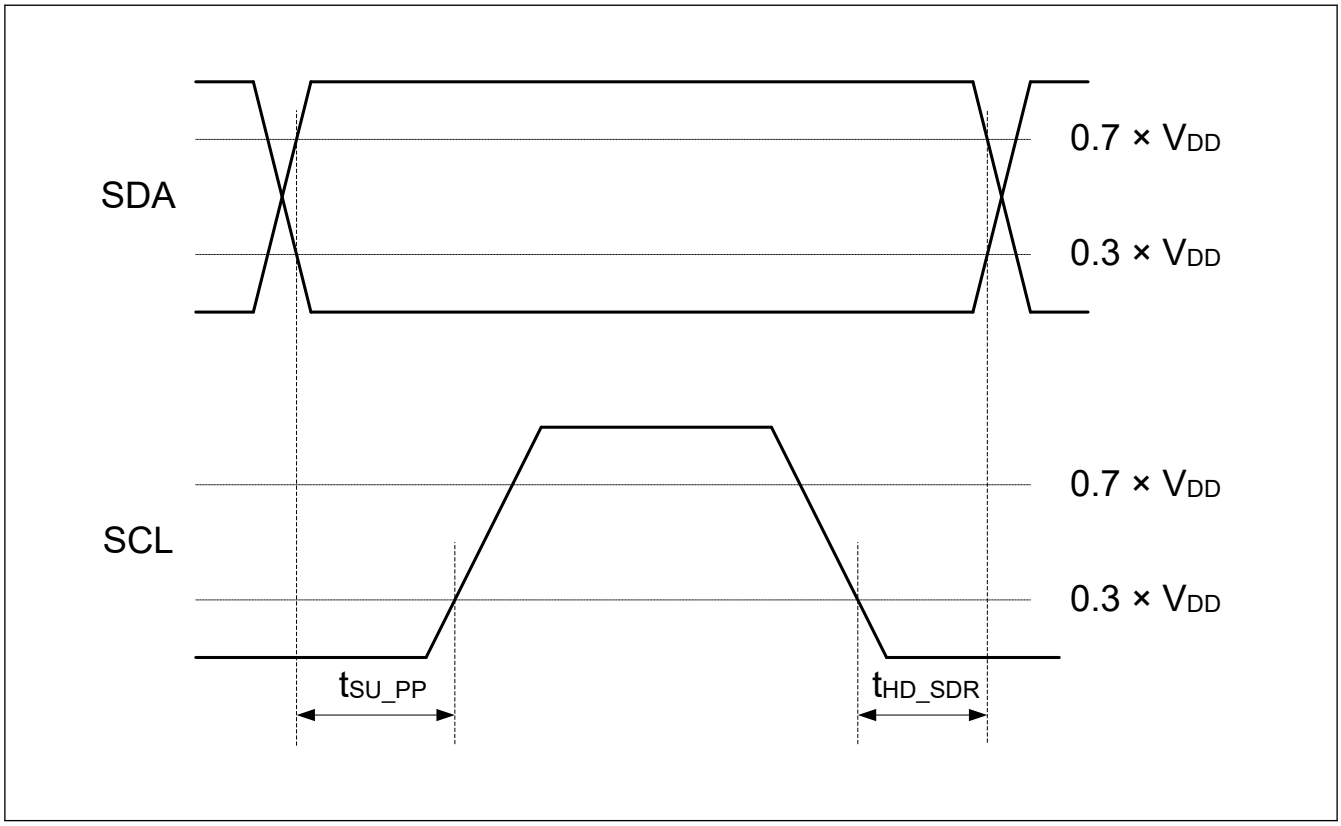


Figure 2.42 Master SDR Timing

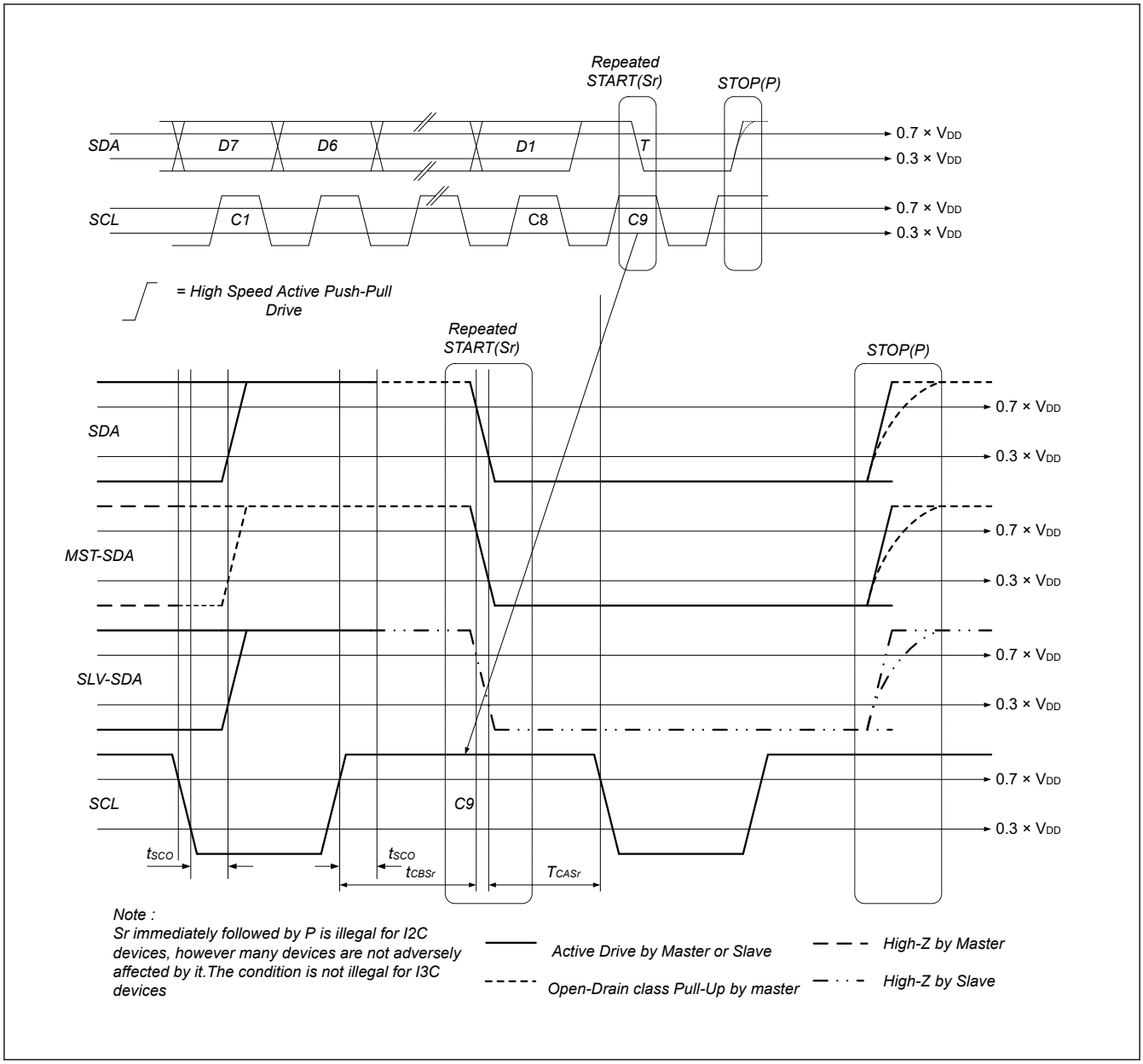


Figure 2.43 T-Bit When Master Ends Read with Repeated START and STOP

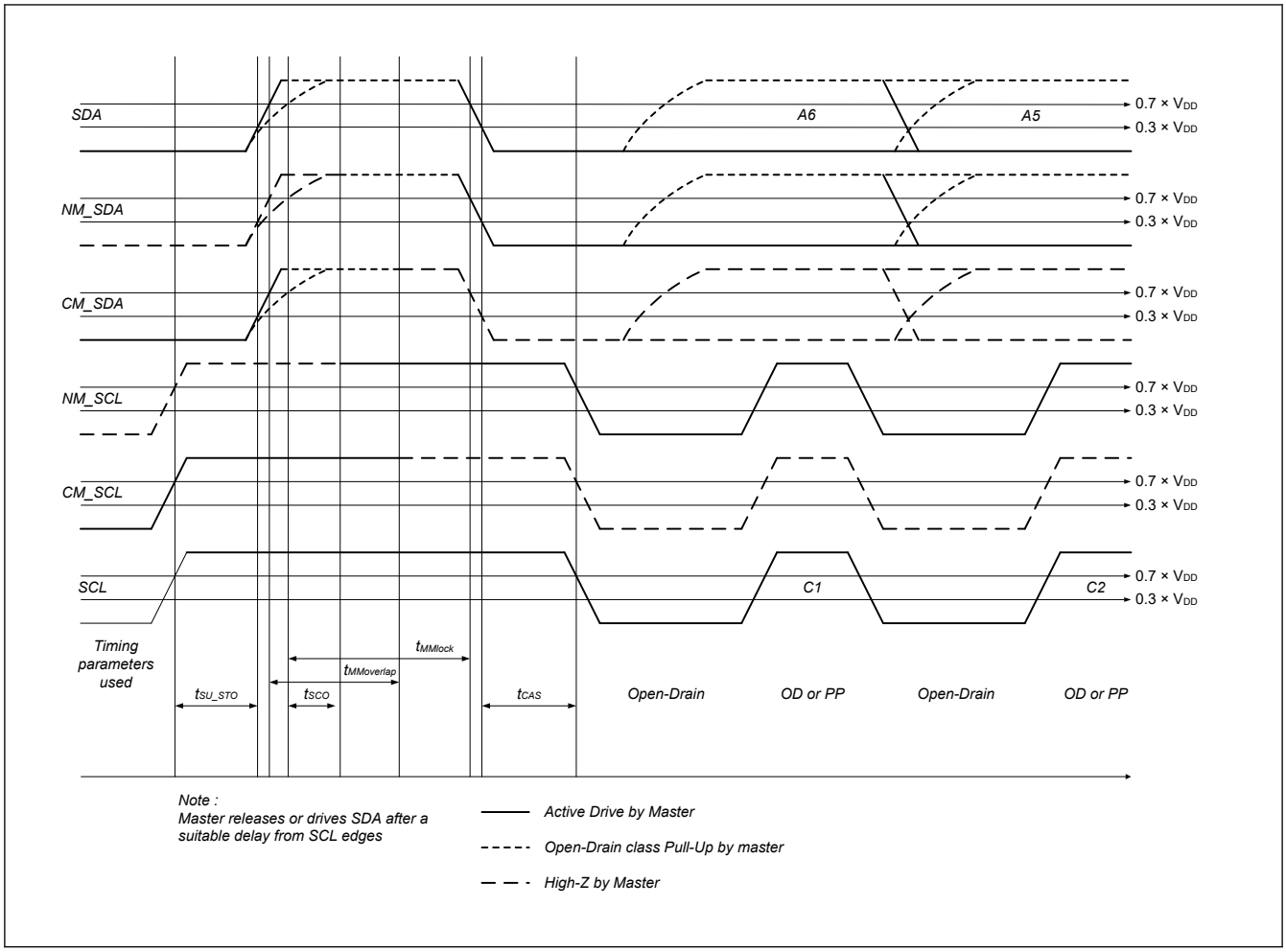


Figure 2.44 I3C Timing

2.3.11 SSIE Timing

Table 2.39 SSIE timing (1 of 2)

Conditions: VCC = 2.7 to 5.5 V
(1) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification		Unit	Test conditions
				Min	Max		
SSIBCK0	Cycle	Master	t_O	187.5	—	ns	Figure 2.45
		Slave	t_I	187.5	—	ns	
	High level/ Low level	Master	t_{HC}/t_{LC}	0.35	—	t_O	
		Slave		0.35	—	t_I	
	Rising time/ falling time	Master	t_{RC}/t_{FC}	—	0.15	t_O / t_I	
		Slave		—	0.15	t_O / t_I	

Table 2.39 SSIE timing (2 of 2)

Conditions: VCC = 2.7 to 5.5 V
(1) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification		Unit	Test conditions
				Min	Max		
SSILRCK0/ SSIFS0, SSITXD0, SSIRXD0	Input set up time	Master	t_{SR}	40	—	ns	Figure 2.47, Figure 2.48
		Slave		12	—	ns	
	Input hold time	Master	t_{HR}	10	—	ns	
		Slave		18	—	ns	
	Output delay time	Master	t_{DTR}	0	20	ns	
		Slave		0	50	ns	
	Output delay time from SSILRCK0/ SSIFS0 change	Slave	t_{DTRW}	0	50	ns	Figure 2.47, Figure 2.48
GTIOC4A, AUDIO_CLK	Cycle		t_{EXcyc}	31.25	—	ns	Figure 2.46
	High level/ Low level		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

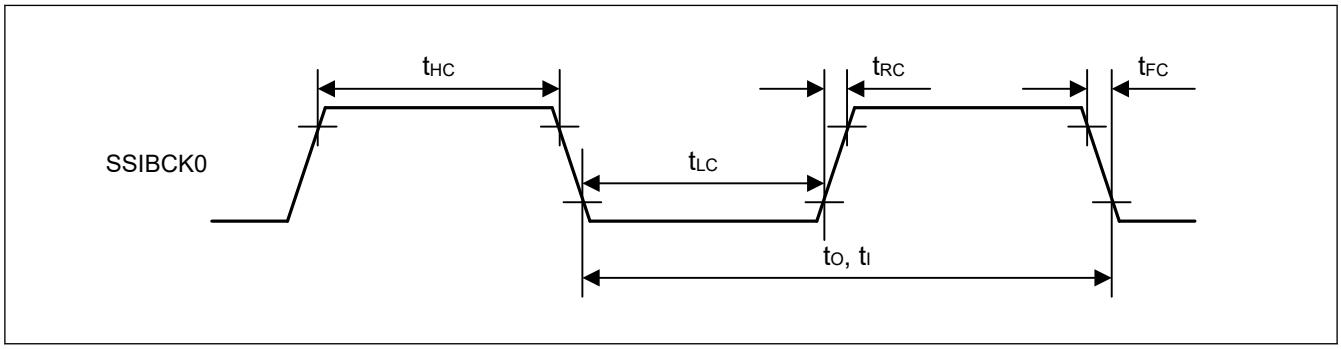


Figure 2.45 SSIE clock input/output timing

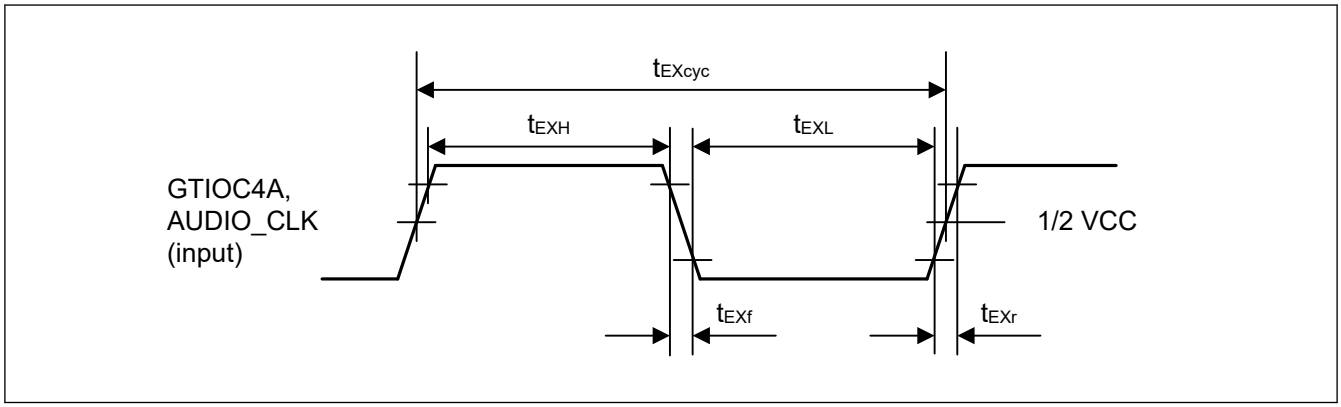


Figure 2.46 Clock input timing

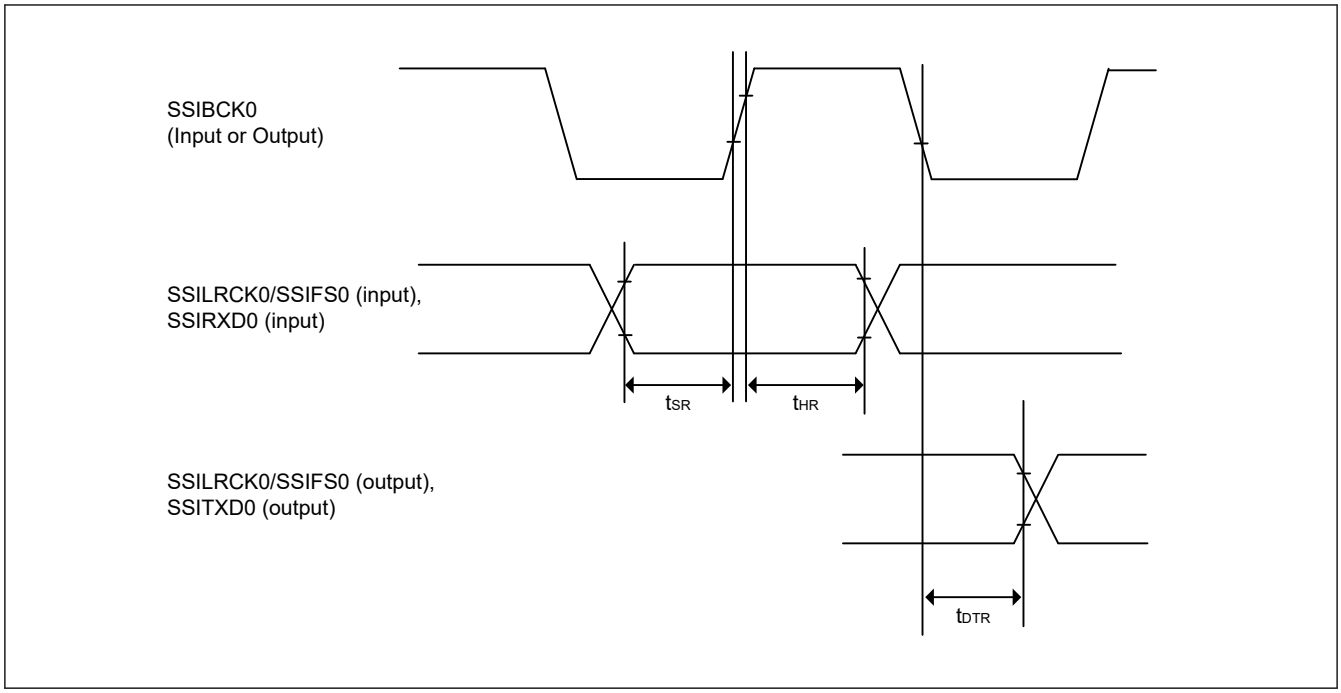


Figure 2.47 SSIE data transmit and receive timing when SSICR.BCKP = 0

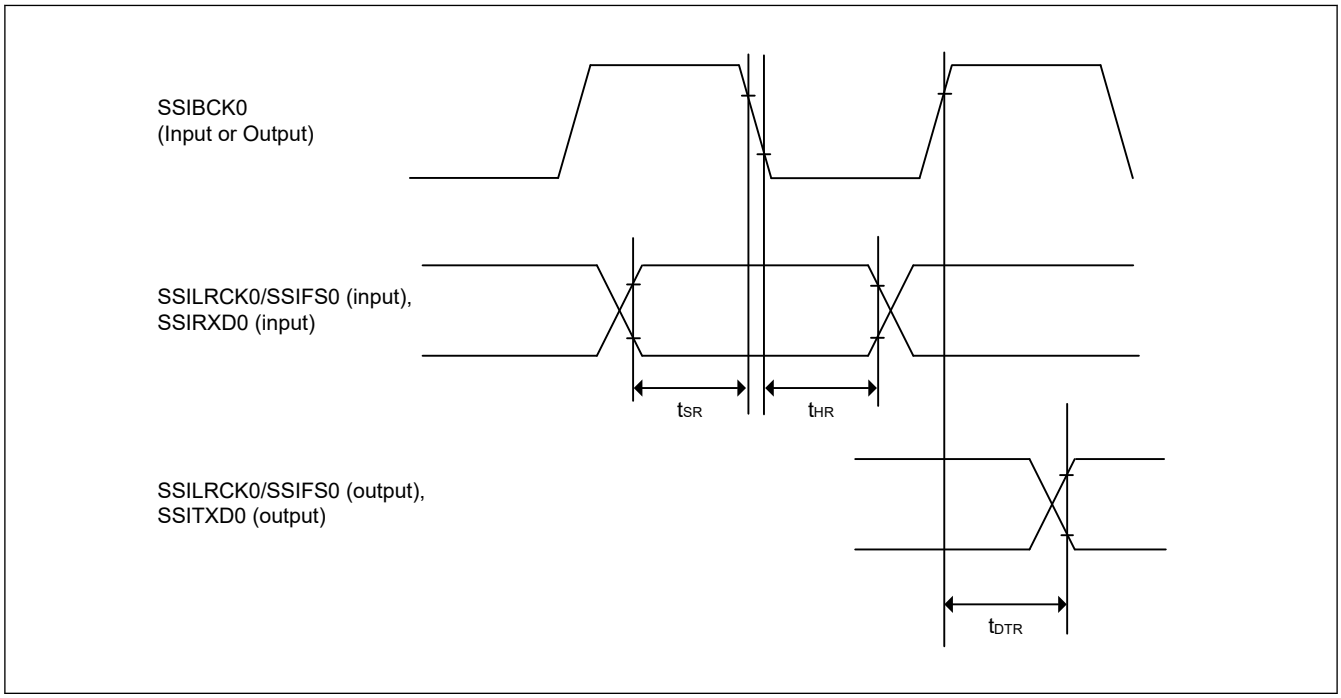
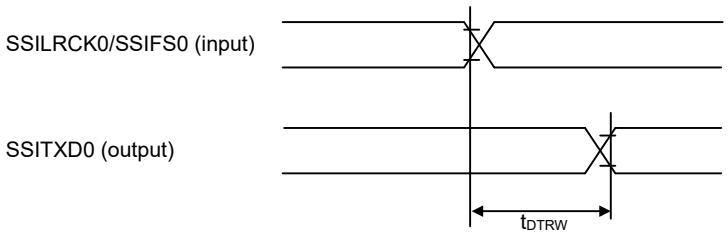


Figure 2.48 SSIE data transmit and receive timing when SSICR.BCKP = 1



MSB bit output delay after SSILRCK0/SSIFS0 change for slave transmitter when DEL = 1, SDTA = 0 or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0] in SSICR.

Figure 2.49 SSIE data output delay after SSILRCK0/SSIFS0 change

2.3.12 UARTA Timing

Table 2.40 UARTA interface timing

Parameter	Symbol	Min.	Max.	Unit	Test conditions
Transfer rate	—	200	153600	bps	—

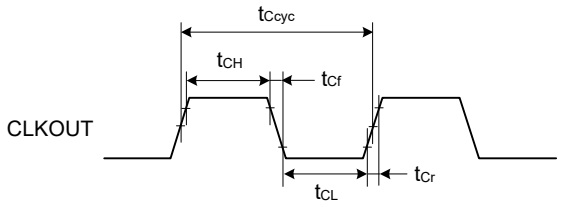
2.3.13 CLKOUT Timing

Table 2.41 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle*1	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.50
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT pin high pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin low pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, specifications in Table 2.41 should be satisfied with 45% to 55% of input duty cycle.

Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.50 CLKOUT output timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.42 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = 3.0 to 3.6, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.51
	Rise time	t_{LR}	4	—	20	ns	
	Fall time	t_{LF}	4	—	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
Pull-up characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	—	1.575	kΩ	During idle state
			1.425	—	3.090	kΩ	During transmission and reception

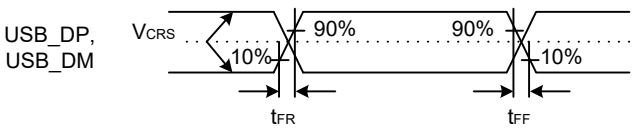


Figure 2.51 USB_DP and USB_DM output timing in full-speed mode

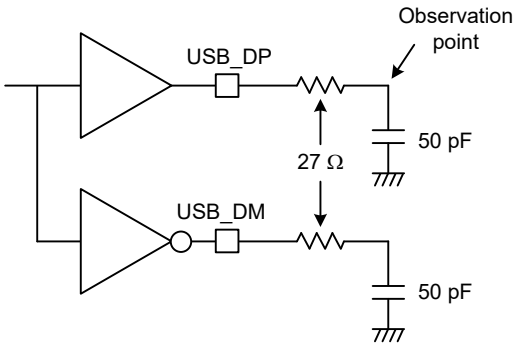


Figure 2.52 Test circuit in full-speed mode

2.4.2 USBCC Characteristics

Table 2.43 USB Type-C interface characteristics

Conditions: VCC = 3.0 to 3.6

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SRC voltage detection threshold	V_{SRC}	0.15	0.20	0.25	V	—
SNK VRD-1.5 voltage detection threshold	V_{VRD15}	0.613	0.66	0.70	V	—
SNK VRD-3.0 voltage detection threshold	V_{VRD30}	1.165	1.23	1.31	V	—
Rd pull-down resistor	Rd	4.6	5.1	5.6	kΩ	—
Rzopen pull-down resistor	Rzopen	126	—	—	kΩ	—

2.5 ADC12 Characteristics

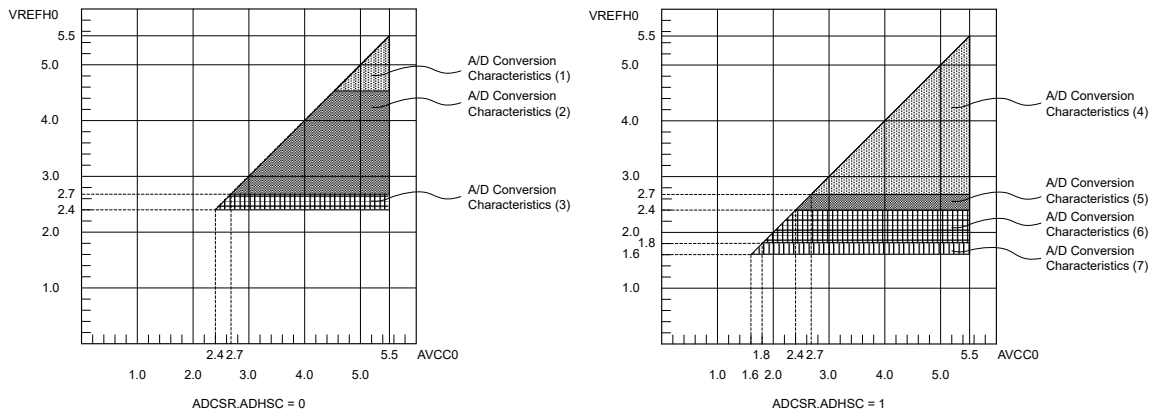


Figure 2.53 AVCC0 to VREFH0 voltage range

Table 2.44 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency	1	—	64	MHz	ADACSR.ADSAC = 0
			48	MHz	ADACSR.ADSAC = 1

Table 2.44 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 4.5 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.3[*3]	kΩ	High-precision channel
		—	—	5.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70 (0.211)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
		1.34 (0.852)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than specified
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.45 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency	1	—	48	MHz	—

Table 2.45 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
		—	—	6.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.46 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
		—	—	7.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.46 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.50	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.47 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
		—	—	6[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1

Table 2.47 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Offset error	—	±1.25	±6.0	LSB	High-precision channel
			±7.5	LSB	Other than specified
Full-scale error	—	±1.25	±6.0	LSB	High-precision channel
			±7.5	LSB	Other than specified
Quantization error	—	±0.5	—	LSB	—
Absolute accuracy	—	±3.25	±7.0	LSB	High-precision channel
			±10.0	LSB	Other than specified
DNL differential nonlinearity error	—	±1.5	—	LSB	—
INL integral nonlinearity error	—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.48 A/D conversion characteristics (5) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
		—	—	7[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—

Table 2.48 A/D conversion characteristics (5) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Absolute accuracy	—	±3.25	±7.0	LSB	High-precision channel
			±10.0	LSB	Other than specified
DNL differential nonlinearity error	—	±1.5	—	LSB	—
INL integral nonlinearity error	—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.49 A/D conversion characteristics (6) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	6[*3]	kΩ	High-precision channel
		—	—	14[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

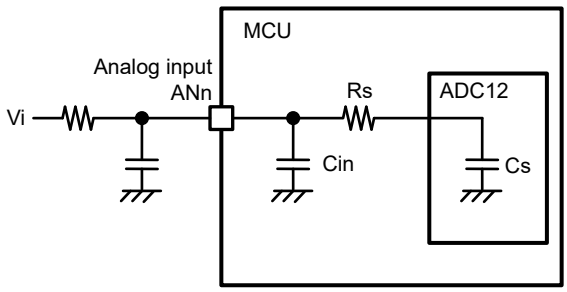
Table 2.50 A/D conversion characteristics (7) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	12*3	kΩ	High-precision channel
		—	—	28*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 2.54 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 2.54 Equivalent circuit for analog input

Table 2.51 12-bit A/D converter channel classification

Classification	Channel	Remarks	Test conditions
High-precision channel	AN000 to AN010	Pins AN000 to AN010 cannot be used as general I/O, TS transmission, when the A/D converter is in use.	AVCC0 = 1.6 to 5.5 V
Normal-precision channel	AN017 to AN022		
Internal reference voltage input channel	Internal reference voltage	—	AVCC0 = 1.8 to 5.5 V
Temperature sensor input channel	Temperature sensor output	—	AVCC0 = 1.8 to 5.5 V

Table 2.52 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 1.8 V.
Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.

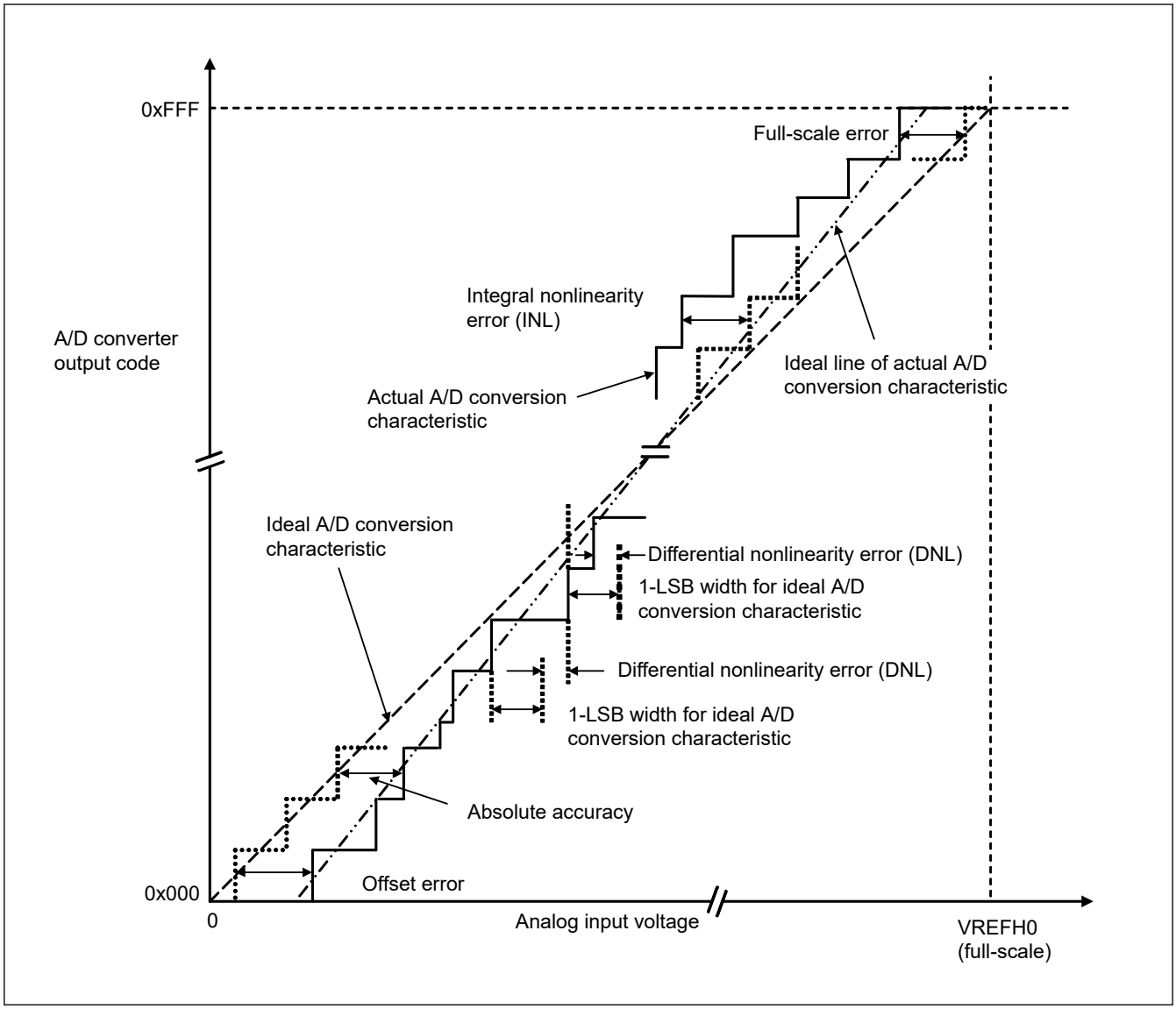


Figure 2.55 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 TSN Characteristics

Table 2.53 TSN characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.5	—	°C	2.4 V or above
		—	± 2.0	—	°C	Below 2.4 V
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

2.7 OSC Stop Detect Characteristics

Table 2.54 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.56

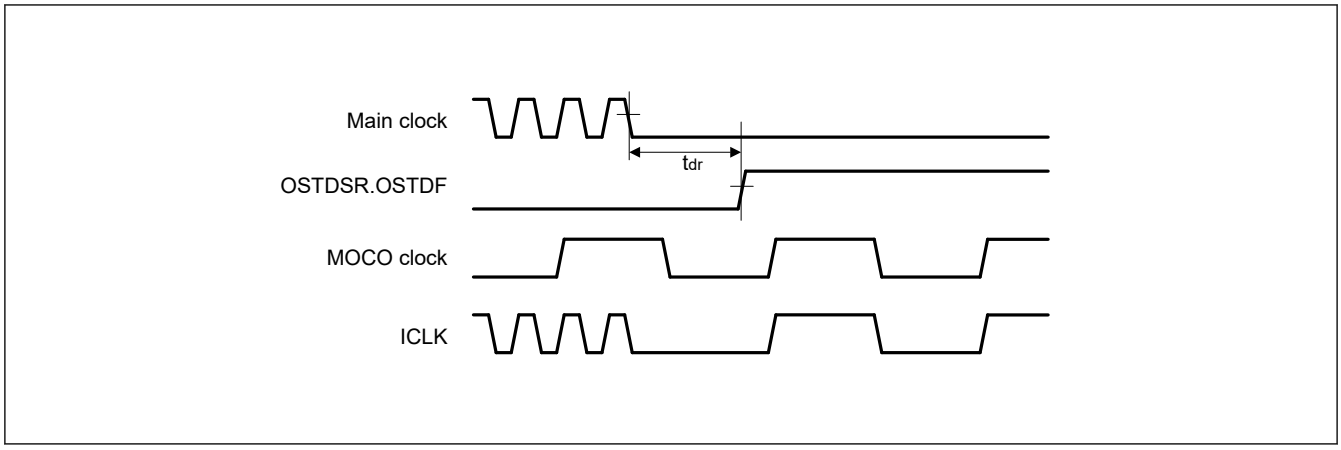


Figure 2.56 Oscillation stop detection timing

2.8 POR and LVD Characteristics

Table 2.55 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 2.57
		When power supply fall	V_{PDR}	1.46	1.50	1.54		Figure 2.58
	Voltage detection circuit (LVD0)*2	When power supply rise	V_{det0_0}	3.74	3.91	4.06	V	Figure 2.59 At falling edge VCC
		When power supply fall		3.68	3.85	4.00		
		When power supply rise	V_{det0_1}	2.73	2.9	3.01		
		When power supply fall		2.68	2.85	2.96		
		When power supply rise	V_{det0_2}	2.44	2.59	2.70		
		When power supply fall		2.38	2.53	2.64		
		When power supply rise	V_{det0_3}	1.83	1.95	2.07		
		When power supply fall		1.78	1.90	2.02		
		When power supply rise	V_{det0_4}	1.66	1.75	1.88		
		When power supply fall		1.60	1.69	1.82		
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_0}	4.23	4.39	4.55	V	Figure 2.60 At falling edge VCC
		When power supply fall		4.13	4.29	4.45		
		When power supply rise	V_{det1_1}	4.07	4.25	4.39		
		When power supply fall		3.98	4.16	4.30		
		When power supply rise	V_{det1_2}	3.97	4.14	4.29		
		When power supply fall		3.86	4.03	4.18		
		When power supply rise	V_{det1_3}	3.74	3.92	4.06		
		When power supply fall		3.68	3.86	4.00		
		When power supply rise	V_{det1_4}	3.05	3.17	3.29		
		When power supply fall		2.98	3.10	3.22		
		When power supply rise	V_{det1_5}	2.95	3.06	3.17		
		When power supply fall		2.89	3.00	3.11		
		When power supply rise	V_{det1_6}	2.86	2.97	3.08		
		When power supply fall		2.79	2.90	3.01		
		When power supply rise	V_{det1_7}	2.74	2.85	2.96		
		When power supply fall		2.68	2.79	2.90		

Table 2.55 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_8}	2.63	2.75	2.85	V	Figure 2.60 At falling edge VCC
		When power supply fall		2.58	2.68	2.78		
		When power supply rise	V_{det1_9}	2.54	2.64	2.75		
		When power supply fall		2.48	2.58	2.68		
		When power supply rise	V_{det1_A}	2.43	2.53	2.63		
		When power supply fall		2.38	2.48	2.58		
		When power supply rise	V_{det1_B}	2.16	2.26	2.36		
		When power supply fall		2.10	2.20	2.30		
		When power supply rise	V_{det1_C}	1.88	2	2.09		
		When power supply fall		1.84	1.96	2.05		
		When power supply rise	V_{det1_D}	1.78	1.9	1.99		
		When power supply fall		1.74	1.86	1.95		
		When power supply rise	V_{det1_E}	1.67	1.79	1.88		
		When power supply fall		1.63	1.75	1.84		
		When power supply rise	V_{det1_F}	1.65	1.7	1.78		
		When power supply fall		1.60	1.65	1.73		
Voltage detection level*1	Voltage detection circuit (LVD2)*4	When power supply rise	V_{det2_0}	4.20	4.40	4.57	V	Figure 2.61 At falling edge VCC
		When power supply fall		4.11	4.31	4.48		
		When power supply rise	V_{det2_1}	4.05	4.25	4.42		
		When power supply fall		3.97	4.17	4.34		
		When power supply rise	V_{det2_2}	3.91	4.11	4.28		
		When power supply fall		3.83	4.03	4.20		
		When power supply rise	V_{det2_3}	3.71	3.91	4.08		
		When power supply fall		3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL0[2:0] bits.
Note 3. # in the symbol $V_{det1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol $V_{det2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.56 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.57, Figure 2.58
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.59
LVD1 response delay time*3		t_{det}	—	—	350	µs	Figure 2.60
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.61
Minimum VCC down time		t_{VOFF}	500	—	—	µs	Figure 2.57, VCC = 1.0 V or above

Table 2.56 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Power-on reset enable time	$t_{W\ (POR)}$	1	—	—	ms	Figure 2.58, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD1 is enabled)	$T_{d\ (E-A)}$	—	—	300	µs	Figure 2.60
LVD2 operation stabilization time (after LVD2 is enabled)	$T_{d\ (E-A)}$	—	—	1200	µs	Figure 2.61
Hysteresis width (POR)	V_{PORH}	—	10	—	mV	—
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	—	60	—	mV	LVD0 selected
		—	110	—		V_{det1_0} to V_{det1_2} selected
		—	70	—		V_{det1_3} to V_{det1_9} selected
		—	60	—		V_{det1_A} to V_{det1_B} selected
		—	50	—		V_{det1_C} to V_{det1_F} selected
		—	90	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

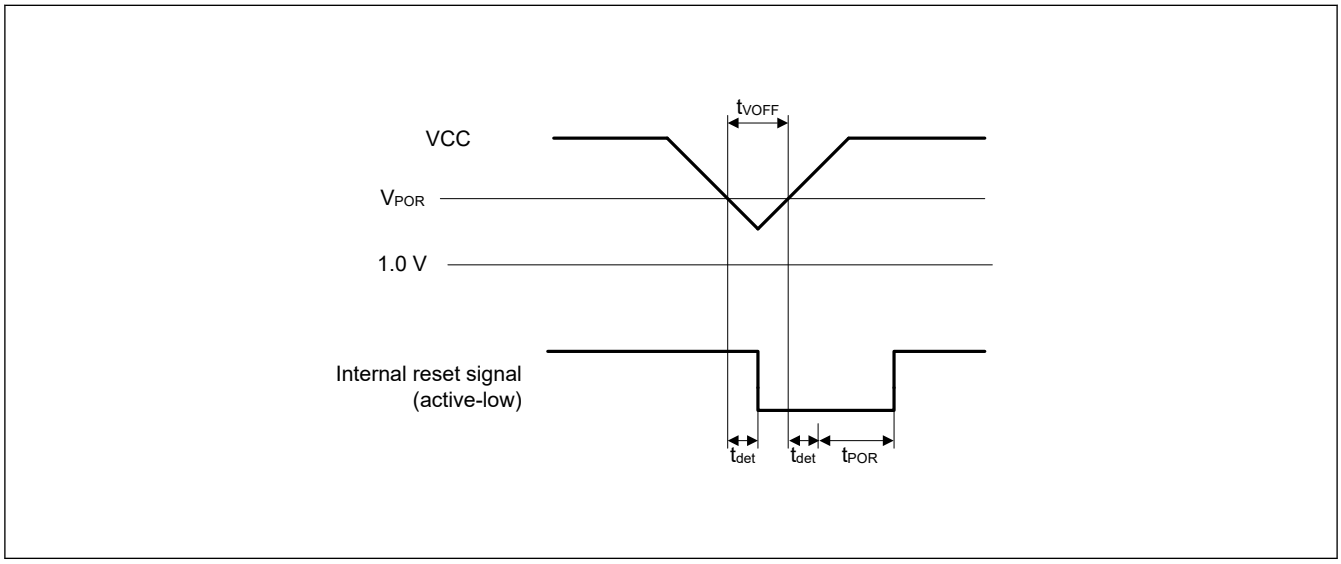
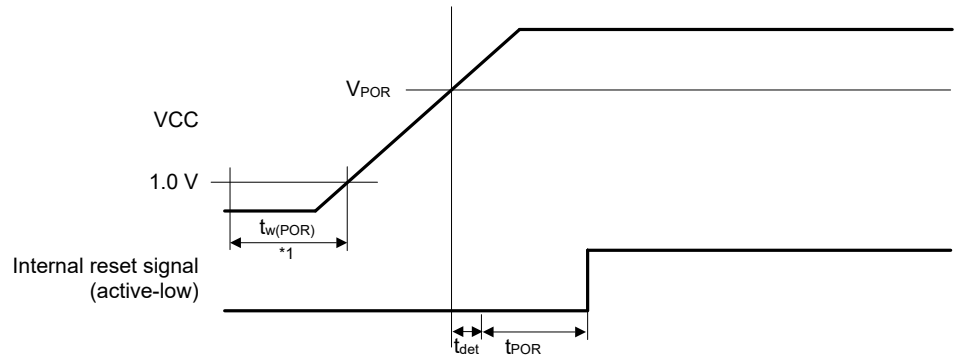


Figure 2.57 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.58 Power-on reset timing

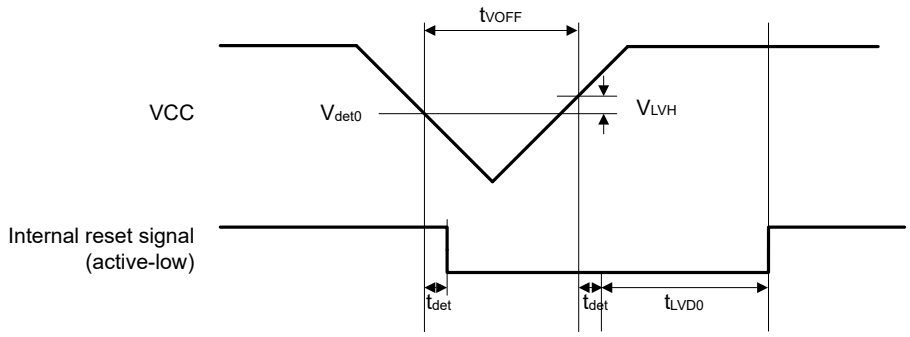


Figure 2.59 Voltage detection circuit timing (V_{det0})

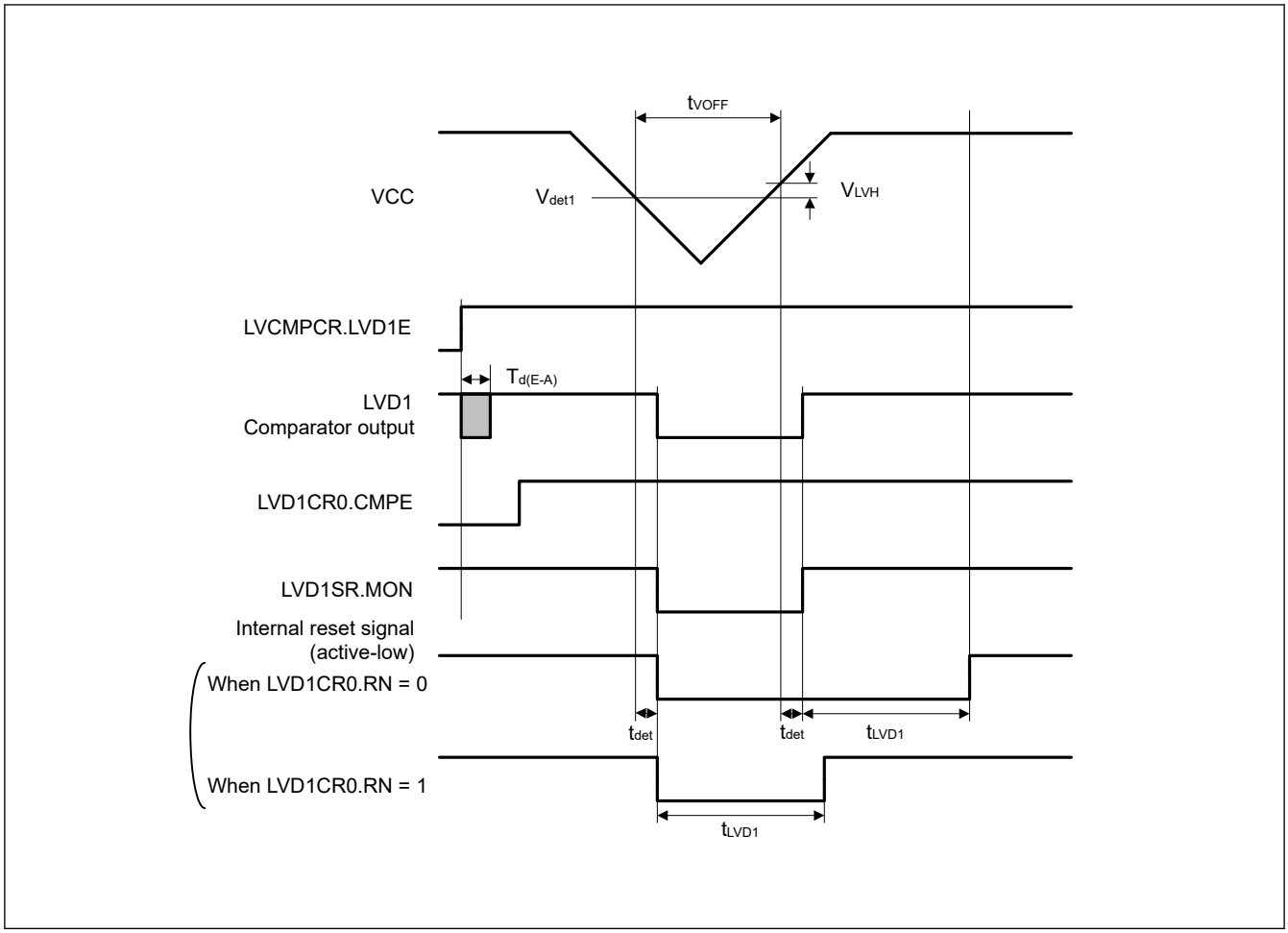


Figure 2.60 Voltage detection circuit timing (V_{det1})

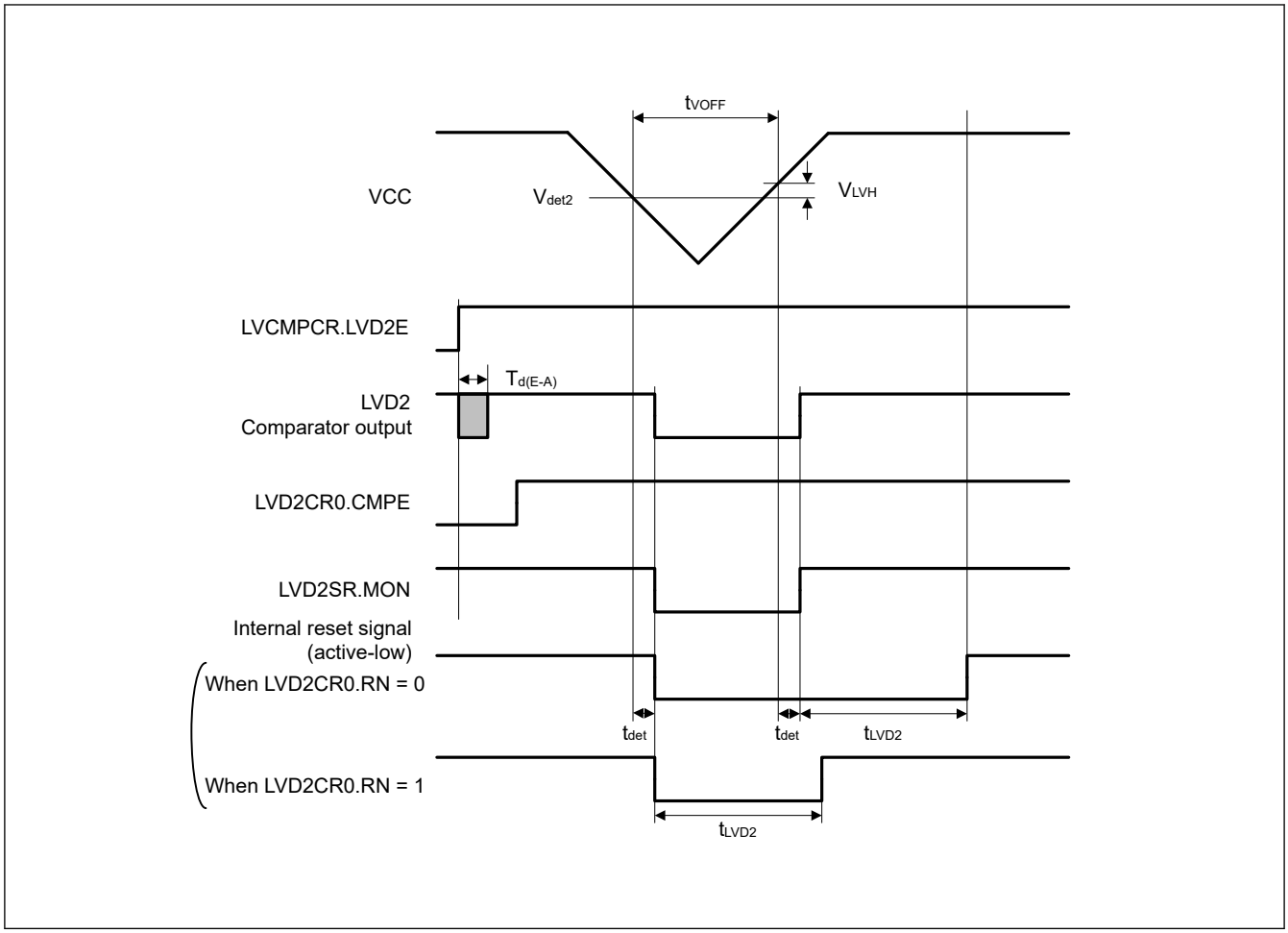


Figure 2.61 Voltage detection circuit timing (V_{det2})

2.9 Flash Memory Characteristics

2.9.1 Code Flash Memory Characteristics

Table 2.57 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20 *2	—	—	Year	T_a = +105°C
			10^{*2}	—	—	Year	T_a = +125°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

Table 2.58 Code flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	34	321	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	5.6	215	ms

Table 2.58 Code flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	8.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	240	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	10.5	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	11.4	423	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

Table 2.59 Code flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	39	356	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	6.2	227	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	11.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	534	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	11.7	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	12.2	435	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	48.7	1740	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.
Note 2. When 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V

Table 2.60 Code flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	57	502	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	8.8	280	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	23.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	1841	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	16.2	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	15.9	491	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	63.5	1964	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

2.9.2 Data Flash Memory Characteristics

Table 2.61 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20 *2	—	—	Year	Ta = +105°C
			10 *2	—	—	Year	Ta = +125°C
	After 100000 times of N_{DPEC}		5 *2	—	—	Year	Ta = +105°C
	After 1000000 times of N_{DPEC}		—	1 *2	—	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,024 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
Note 2. This result is obtained from reliability testing.

Table 2.62 Data flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	34	321	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	6.1	224	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	8.3	µs
	1-KB	t_{DBC1K}	—	—	1832	—	—	466	µs
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	10.5	µs

Table 2.62 Data flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Data flash STOP recovery time	t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.63 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	39	356	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	7.3	248	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	11.3	µs
	1-KB	t_{DBC1K}	—	—	1.84	—	—	1.06	ms
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	11.7	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V

Table 2.64 Data flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	86	732	—	57	502	µs
Erasure time	1-KB	t_{DE1K}	—	19.7	504	—	12.4	354	ms
Blank check time	1-byte	t_{DBC1}	—	—	46.5	—	—	23.3	µs
	1-KB	t_{DBC1K}	—	—	7.3	—	—	3.66	ms
Suspended time during erasing		t_{DSED}	—	—	22.3	—	—	16.2	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 2 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.10 Serial Wire Debug (SWD)

Table 2.65 SWD characteristics (1)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.62
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 2.63
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.66 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.62
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.63
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

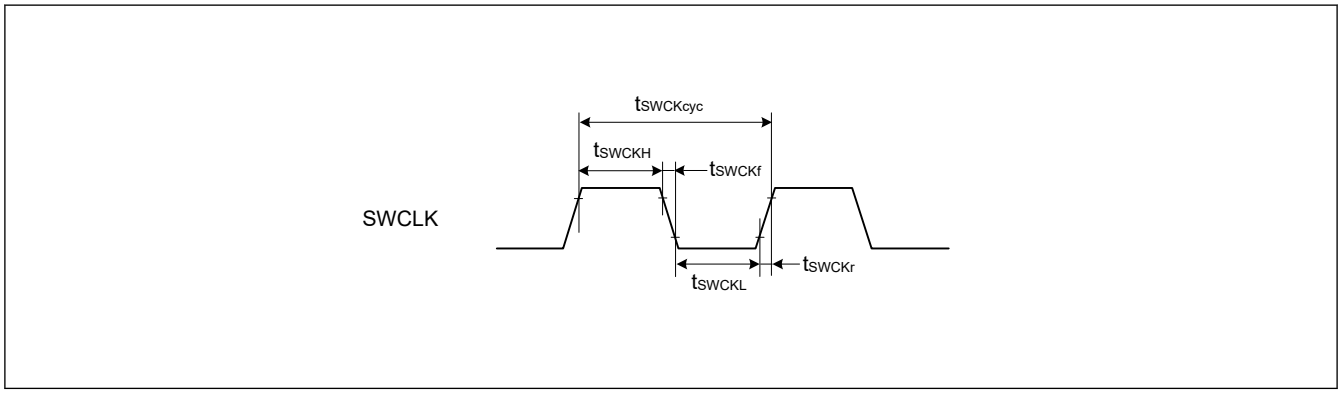


Figure 2.62 SWD SWCLK timing

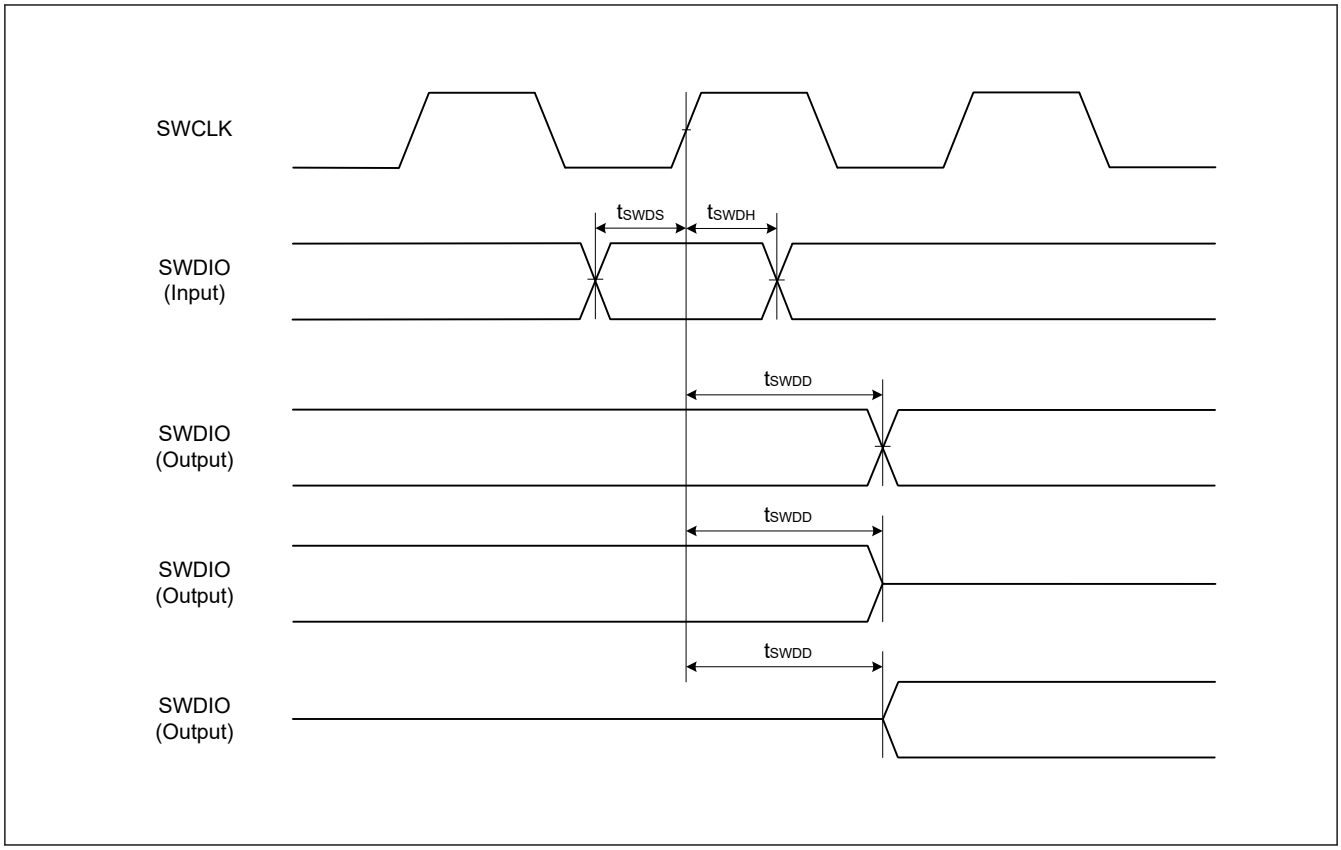


Figure 2.63 SWD input/output timing

Appendix 1. Port States in each Processing Mode

Table A1.1 Port states in each processing mode (1 of 3)

Port name	Reset	Software Standby Mode
P000/AN000/IRQ6	Hi-Z	Keep-O*1
P001/AN001/IRQ7	Hi-Z	Keep-O*1
P002/AN002/IRQ2	Hi-Z	Keep-O*1
P003/AN003	Hi-Z	Keep-O
P004/AN004/IRQ3	Hi-Z	Keep-O*1
P010/AN005/IRQ5_C	Hi-Z	Keep-O*1
P011/AN006/IRQ0_C	Hi-Z	Keep-O*1
P012/AN007/IRQ1_C	Hi-Z	Keep-O*1
P013/AN008/IRQ4_C	Hi-Z	Keep-O*1
P014/AN009/GTETRGA_E/IRQ6_C	Hi-Z	Keep-O*1
P015/AN010/GTETRGB_E/IRQ7_A	Hi-Z	Keep-O*1
P100/AN022/AGTIO0_A/GTETRGA_A/ GTIOC8B_A/RXD0_A/MISO0_A/SCL0_A/ SCK1_A/MISOA_A/SSIRXD0_C/KRM00/ IRQ2_A	Hi-Z	[AGTIO0_A output selected] AGTIO0_A output*2 [Other than the above] Keep-O*1
P101/AN021/AGTEE0/GTETRGB_A/ GTIOC8A_A/TXD0_A/ MOSI0_A/ SDA0_ A/CTS1_RTS1_A/SS1_A/MOSIA_A/ SSITXD0_C/KRM01/IRQ1_A	Hi-Z	Keep-O*1
P102/AN020/ADTRG0_A/AGTO0/ GTOWLO_A/GTIOC5B_A/CTX0_C/ SCK0_A/TXD2_D/ MOSI2_D/SDA2_D/ RSPCKA_A/SSILRCK0/SSIFS0_C/KRM02	Hi-Z	[AGTO0 selected] AGTO0 output*2 [Other than the above] Keep-O*1
P103/AN019/GTOWUP_A/GTIOC5A_A/ CRX0_C/CTS0_RTS0_A/SS0_A/SSLA0_A/ SSIBCK0_C/KRM03/IRQ5_F	Hi-Z	Keep-O*1
P104/GTETRGB_B/GTIOC4B_B/RXD0_C/ MISO0_C/SCL0_ C/SSLA1_A/KRM04/ IRQ1_B	Hi-Z	Keep-O*1
P105/GTETRGA_C/GTIOC4A_B/SSLA2_A/ KRM05/IRQ0_B	Hi-Z	Keep-O*1
P106/SSLA3_A/KRM06	Hi-Z	Keep-O*1
P107/KRM07	Hi-Z	Keep-O*1
P108/SWDIO/AGTOA1_B/GTOULO_C/ GTIOC0B_A/CTS9_RTS9_B/SS9_B/ SSIDATA0_A/RXDA0_A	Pull-up	[AGTOA1_B selected] AGTOA1_B output*2 [RXDA0_A selected] RXDA0_A output*3 [Other than the above] Keep-O
P109/AGTIO1_B/GTOVUP_A/GTIOC4A_A/ CRX0_A/SCK1_E/TXD9_B/MOSI9_B/ SDA9_B/SCL0_B/AUDIO_CLK_A/IRQ5_E/ CLKOUT_B/TXDA0_A/IRQ5_E	Hi-Z	[AGTIO1_B selected] AGTIO1_B output*2 [CLKOUT_B selected] CLKOUT_B output [Other than the above] Keep-O*1
P110/AGTOB0_B/GTOVLO_A/GTIOC4B_A/ RTCOUT_B/CTX0_A/CTS2_RTS2_B/ SS2_B/RXD9_B/MISO9_B/SCL9_B/ SDA0_B/IRQ3_A	Hi-Z	[AGTOB0_B selected] AGTOB0_B output*2 [RTCOUT_B selected] RTCOUT_B output [Other than the above] Keep-O*1

Table A1.1 Port states in each processing mode (2 of 3)

Port name	Reset	Software Standby Mode
P111/AGTOA0/GTIOC6A_A/SCK2_B/ SCK9_B/IRQ4_A	Hi-Z	[AGTOA0 selected] AGTOA0 output*2 [Other than the above] Keep-O*1
P112/ADTRG0_C/AGTOB0/GTIOC6B_A/ TXD2_B/MOSI2_B/SDA2_B/SCK1_D/ AUDIO_CLK_B	Hi-Z	[AGTOB0 selected] AGTOB0 output*2 [Other than the above] Keep-O
P113	Hi-Z	Keep-O
P200/NMI	Hi-Z	Hi-Z
P201/MD	Pull-up	Keep-O
P204/CACREF_A/AGTIO1_A/GTIW_A/ SCK0_D/SCK9_A/SSIRXD0_B	Hi-Z	[AGTIO1_A output selected] AGTIO1_A output*2 [Other than the above] Keep-O*1
P205/AGTO1/GTIV_A/TXD0_D/MOSI0_D/ SDA0_D/CTS9_RTS9_A/SS9_A/ SSITXD0_B/IRQ1/CLKOUT_A	Hi-Z	[AGTO1 selected] AGTO1 output*2 [CLKOUT_A selected] CLKOUT_A output [Other than the above] Keep-O*1
P206/GTIU_A/RXD0_D/MISO0_D/SCL0_D/ SSILRCK0/SSIFS0_B/IRQ0	Hi-Z	Keep-O*1
P207/SSIBCK0_B	Hi-Z	Keep-O
P212/EXTAL/AGTEE1/GTETRGB_D/ GTIOC0B_D/RXD1_A/MISO1_A/SCL1_A/ IRQ3_B	Hi-Z	Keep-O*1
P213/XTAL/GTETRGA_D/GTIOC0A_D/ TXD1_A/MOSI1_A/SDA1_A/IRQ2_B	Hi-Z	Keep-O*1
P214/XCOUT, P215/XCIN	Hi-Z	[Sub-clock Oscillator selected] Sub-clock Oscillator is operating [Other than the above] Hi-Z
P300/SWCLK/AGTIO0_B/GTOUUP_C/ GTIOC0A_A/CLKA0_A	Pull-up	[AGTIO0_B selected] AGTIO0_B output*2 [Other than the above] Keep-O
P301/AGTIO0_D/GTOULO_A/GTIOC7B_A/ RXD2_A/MISO2_A/SCL2_A/ CTS9_RTS9_D/SS9_D/IRQ6_A	Hi-Z	[AGTIO0_D selected] AGTIO0_D output*2 [Other than the above] Keep-O*1
P302/GTOUUP_A/GTIOC7A_A/TXD2_A/ MOSI2_A/SDA2_A/IRQ5_A	Hi-Z	Keep-O*1
P303	Hi-Z	Keep-O
P304	Hi-Z	Keep-O
P400/CACREF_C/AGTIO1_C/GTIOC9A_A/ SCK0_B/SCK1_B/SCL0_A/IRQ0_A	Hi-Z	[AGTIO1_C selected] AGTIO1_C output*2 [Other than the above] Keep-O*1
P401/GTETRGA_B/GTIOC9B_A/CRX0_B/ CTS0_RTS0_B/SS0_B/TXD1_B/MOSI1_B/ SDA1_ B/SDA0_A/IRQ5/CLKA0_B	Hi-Z	Keep-O*1

Table A1.1 Port states in each processing mode (3 of 3)

Port name	Reset	Software Standby Mode
P402/AGTIO0_E/AGTIO1_D/CTX0_B/ RXD1_B/MISO1_B/SCL1_ B/IRQ4/ RXDA0_B	Hi-Z	[AGTIO0_E, AGTIO1_D selected] AGTIO0_E, AGTIO1_D output*2 [RXDA0_B selected] RXDA0_B output*3 [Other than the above] Keep-O*1
P403/AGTIO0_F/AGTIO1_E/ CTS1_RTS1_B/SS1_B	Hi-Z	[AGTIO1_E, AGTIO0_F selected] AGTIO1_E, AGTIO0_F output*2 [Other than the above] Keep-O*1
P407/ADTRG0_B/RTCOUT_A/AGTIO0_C/ CTS0_RTS0_D/SS0_D/SSIDATA0_B/ USB_VBUS	Hi-Z	[AGTIO0_C selected] AGTIO0_C output*2 [CLKOUT_A selected] CLKOUT_A output [Other than the above] Keep-O*1
P408/GTOWLO_B/CTS1_RTS1_D/SS1_D/ SSIRXD0_A/IRQ7_B/TXDA1_B	Hi-Z	Keep-O*1
P409/GTOWUP_B/SSITXD0_A/IRQ6_B/ RXDA1_B	Hi-Z	[RXDA1_B selected] RXDA1_B output*3 [Other than the above] Keep-O*1
P410/AGTOB1/GTOVLO_B/RXD0_B/ MISO0_B/SCL0_B/MISOA_B/SSILRCK0/ SSIFS0_A/IRQ5_B/CLKA1_B	Hi-Z	[AGTOB1 selected] AGTOB1 output*2 [Other than the above] Keep-O*1
P411/AGTOA1/GTOVUP_B/TXD0_B/ MOSI0_B/SDA0_ B/MOSIA_B/SSIBCK0_A/ IRQ4_B	Hi-Z	[AGTOA1 selected] AGTOA1 output*2 [Other than the above] Keep-O*1
P500/GTIU_B/GTIOC5A_B/AUDIO_CLK_C/ CLKA1_A	Hi-Z	Keep-O
P501/AN017/GTIV_B/GTIOC5B_B/TXD1_C/ MOSI1_C/SDA1_C	Hi-Z	Keep-O
P502/AN018/GTIW_B/RXD1_C/MISO1_C/ SCL1_C	Hi-Z	Keep-O
P912/USB_CC2/CTX0_D/SDA0_C	Hi-Z	Keep-O
P913/USB_CC1/CRX0_D/SCL0_C/IRQ5_D	Hi-Z	Keep-O*1

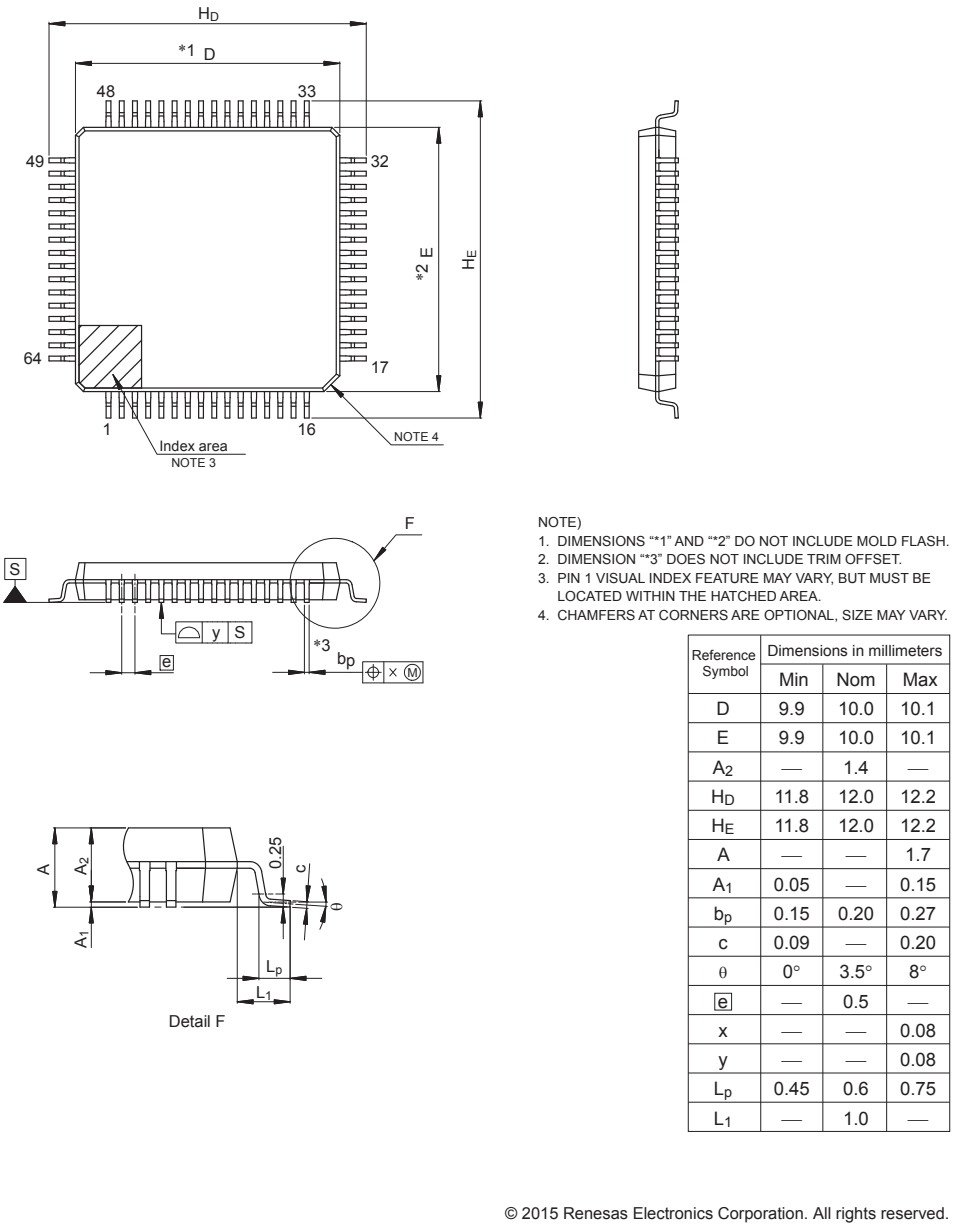
Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.
Note 2. AGTIO output is enabled while LOCO or SOSC is selected as a count source.
Note 3. RXDA output is enabled while 1000b (UARTALOCLK) or 1001b (UARTASCLK) is selected

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



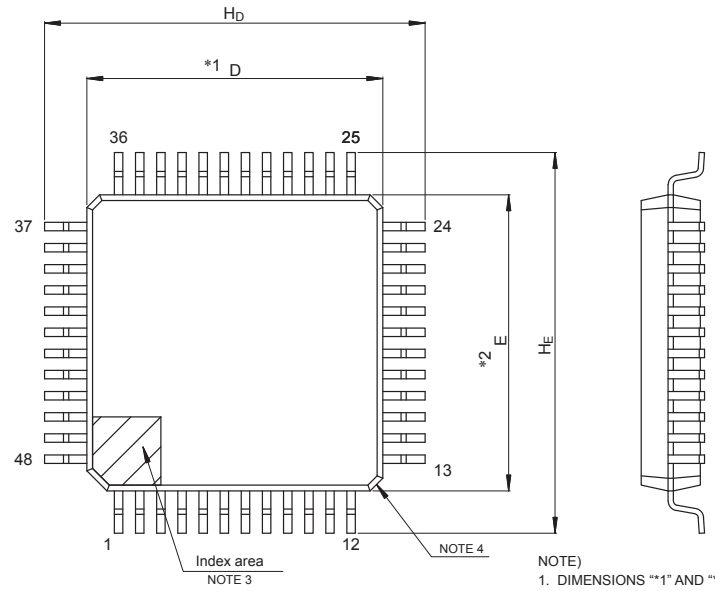
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

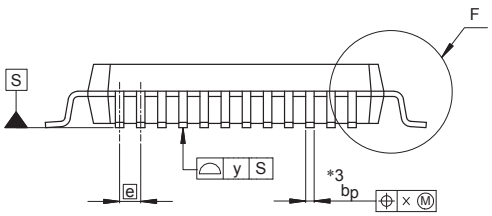
Figure A2.1 LQFP 64-pin 0.5mm pitch

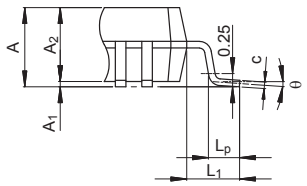
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



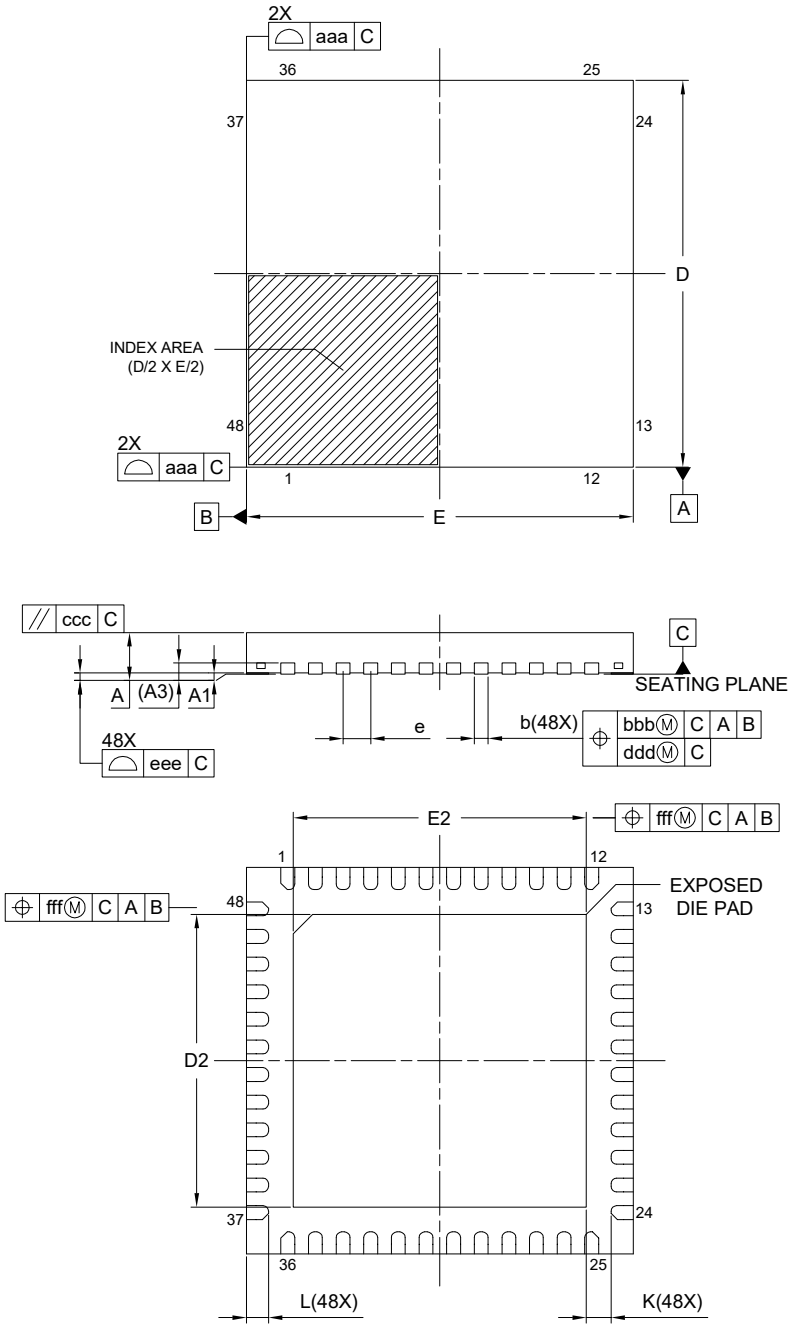


Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A2.2 LQFP 48-pin

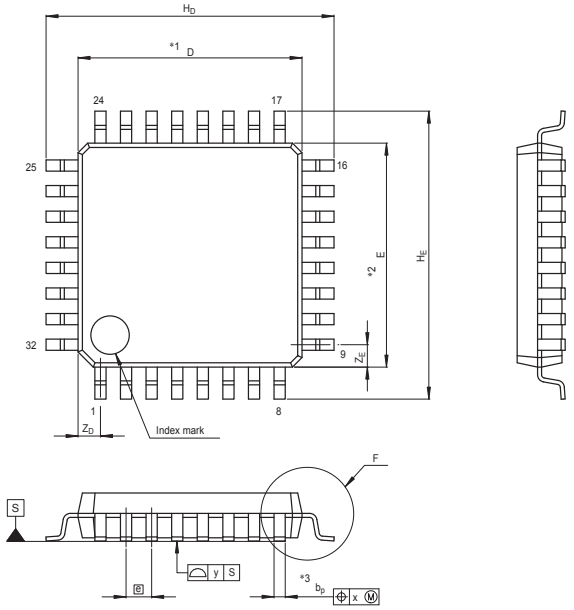
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

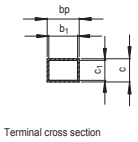


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

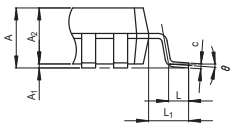
Figure A2.3 HWQFN 48-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g





Terminal cross section



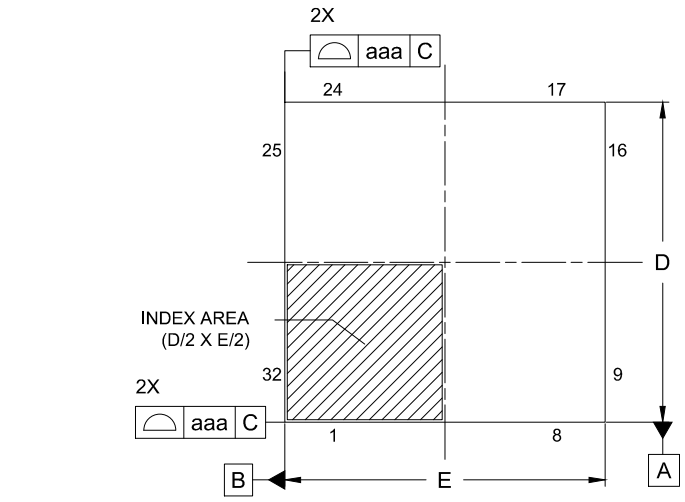
Detail F

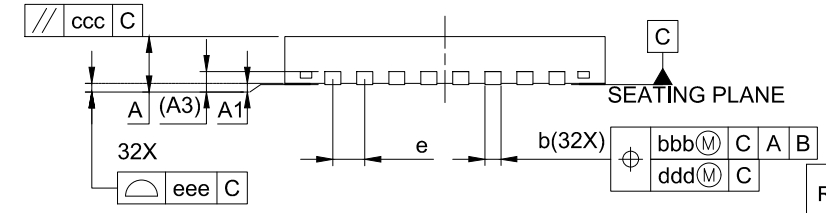
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

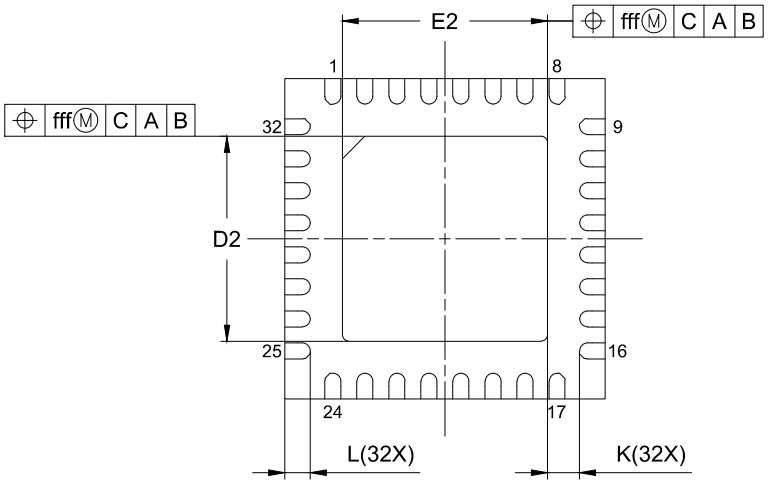
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure A2.4 LQFP 32-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06







Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure A2.5 HWQFN 32-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MPU	Memory Protection Unit	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CPU_DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4004_0000
PORT1	Port 1 Control Registers	0x4004_0020
PORT2	Port 2 Control Registers	0x4004_0040
PORT3	Port 3 Control Registers	0x4004_0060
PORT4	Port 4 Control Registers	0x4004_0080
PORT5	Port 5 Control Registers	0x4004_00A0
PORT9	Port 9 Control Registers	0x4004_0120
PFS	Pmn Pin Function Control Register	0x4004_0800
ELC	Event Link Controller	0x4004_1000
POEG	Port Output Enable Module for GPT	0x4004_2000
RTC	Realtime Clock	0x4004_4000
WDT	Watchdog Timer	0x4004_4200
IWDT	Independent Watchdog Timer	0x4004_4400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4004_4600
MSTP	Module Stop Control B, C, D	0x4004_7000
SSIE0	Serial Sound Interface Enhanced	0x4004_E000
CAN0	Controller Area Network	0x4005_0000
DOC	Data Operation Circuit	0x4005_4100
ADC12	12-bit A/D Converter	0x4005_C000
SCI0	Serial Communication Interface 0	0x4007_0000
SCI1	Serial Communication Interface 1	0x4007_0020
SCI2	Serial Communication Interface 2	0x4007_0040
SCI9	Serial Communication Interface 9	0x4007_0120
SPI0	Serial Peripheral Interface 0	0x4007_2000
CRC	CRC Calculator	0x4007_4000
GPT320	General PWM Timer 0 (32-bit)	0x4007_8000
GPT164	General PWM Timer 4 (16-bit)	0x4007_8400
GPT165	General PWM Timer 5 (16-bit)	0x4007_8500

Table A3.1 Peripheral base address (2 of 2)

Name	Description	Base address
GPT166	General PWM Timer 6 (16-bit)	0x4007_8600
GPT167	General PWM Timer 7 (16-bit)	0x4007_8700
GPT168	General PWM Timer 8 (16-bit)	0x4007_8800
GPT169	General PWM Timer 9 (16-bit)	0x4007_8900
GPT_OPS	Output Phase Switching Controller	0x4007_8FF0
KINT	Key Interrupt Function	0x4008_0000
I3C	I3C Bus Interface	0x4008_3000
AGTW0	Low Power Asynchronous General Purpose Timer 0	0x4008_4000
AGTW1	Low Power Asynchronous General Purpose Timer 1	0x4008_4100
FLCN	Flash I/O Registers	0x407E_C000
USBFS	USB 2.0 Full-Speed Module	0x4009_0000
USBCC	USB type-C Controller 2.0 Module	0x4009_1000
UARTA	Serial Interface UARTA	0x4009_7000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table A3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table A3.2 shows the register access cycles for non-GPT modules.

Table A3.2 Access cycles for non-GPT modules (1 of 2)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle unit	Related function
	From	To	Read	Write	Read	Write		
MPU, SRAM, BUS, DTC, ICU, CPU_DBG	0x4000_2000	0x4001_BFFF	3				ICLK	Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory

Table A3.2 Access cycles for non-GPT modules (2 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
SYSC	0x4001_E000	0x4001_E6FF	4				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
PORTn, PFS, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	0x4004_0000	0x4004_7FFF	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
SSIE0	0x4004_E000	0x4004_EFFF	3		2 to 3		PCLKB	Serial Sound Interface Enhanced
CAN0, DOC, ADC12	0x4005_0000	0x4005_EFFF	3		2 to 3		PCLKB	Controller Area Network Module, Data Operation Circuit, 12-bit A/D Converter
SCIn (n = 0 to 2, 9*2)	0x4007_0000	0x4007_0EFF	5		2 to 3		PCLKB	Serial Communications Interface
SPIn (n = 0)*3	0x4007_2000	0x4007_2FFF	5		2 to 3		PCLKB	Serial Peripheral Interface
CRC	0x4007_4000	0x4007_4FFF	3		2 to 3		PCLKB	CRC Calculator
GPT32n (n = 0), GPT16n (n = 4 to 9), GPT_OPS	0x4007_8000	0x4007_BFFF	See Table A3.3.				PCLKB	General PWM Timer
KINT	0x4008_0000	0x4008_1FFF	3		2 to 3		PCLKB	Key interrupt Function
AGTWn	0x4008_4000	0x4008_4FFF	3		2 to 3		PCLKB	Low Power Asynchronous General Purpose Timer
FLCN	0x407E_C000	0x407E_FFFF	7		7		ICLK	Data Flash, Temperature Sensor, Capacitive Sensing Unit 2, Flash Control
I3C	0x4008_3000	0x4008_33D0	3		2 to 3		PCLKB	I3C Bus Interface
USBFS	0x4009_0000	0x4009_FFFF	3		2 to 3		PCLKB	USB 2.0 Full-Speed Module
USBCC	0x4009_1000	0x4009_101F	3		2 to 3		PCLKB	USB type-C Controller 2.0 Module
UARTA	0x4009_7000	0x4009_7011	3		2 to 3		PCLKB	Serial Interface UARTA

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
Note 2. Regarding n = 0, when accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table A3.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table A3.2.
Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table A3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table A3.2.

Table A3.3 shows register access cycles for GPT modules.

Table A3.3 Access cycles for GPT modules (1 of 2)

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB

Table A3.3 Access cycles for GPT modules (2 of 2)

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

Revision History

Revision 1.00 — November 15, 2024

First edition, issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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