R9A02G021
32-Bit MCU based on RISC-V

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Rev.1.10
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Ultra low power 48 MHz Renesas RISC-V core with 128-KB code flash memory, 16 KB SRAM, 12-bit A/D Converter, and Safety features.

Features

■ RISC-V Core

- Renesas RISC-V instruction-set architecture (RV32I [MACB])
- Maximum operating frequency: 48 MHz
- Debug and Trace: RISC-V External Debug Support
- Debug Port: cJTAG

■ Memory

- 128-KB code flash memory
- 4 KB data flash
- 16 KB SRAM
- 128-bit unique ID

■ Connectivity

- Serial Array Unit (SAU) × 2
  - Simplified SPI × 6
  - UART × 3
  - Simplified I^2C × 6
- I^2C Bus Interface (IICA) × 2
- Serial Interface UARTA (UARTA) × 2
- Remote Control Signal Receiver (REMC)

■ Analog

- 12-bit A/D Converter (ADC12)
- Comparator (CMP) × 2
- 8-bit D/A Converter (DAC8) × 2
- Temperature Sensor (TSN)

■ Timers

- Watchdog Timer (WDT)
- Realtime Clock (RTC)
- Timer Array Unit (TAU) × 8
- 32-bit Interval Timer (TML32)

■ Safety

- SRAM parity and ECC error check
- Flash area protection
- ADC test function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Illegal memory access detection
- True Random Number Generator (TRNG)

■ System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Multiple Clock Sources

- External clock input (EXTAL) (1 to 20 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (24/32/48 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock out support

■ Up to 42 pins for general I/O ports

- Open drain, input pull-up

■ Operating Voltage

- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages

- Ta = -40°C to +125°C
  - 48-pin HWQFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 16-pin WLCSP(1.99 mm × 1.99 mm, 0.4 mm pitch)

1. Overview

The MCU in this series incorporates an energy-efficient Renesas RISC-V 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- 128-KB code flash memory
- 4 KB data flash
- 16 KB SRAM
- 12-bit A/D Converter (ADC12)
- Analog peripherals

1.1 Function Outline

Table 1.1 RISC-V core

Feature	Functional description
RISC-V core	• Maximum operating frequency: up to 48 MHz • Instruction-set architecture (ISA) – RISC-V RV32I base integer instruction set – RISC-V C standard extension for compressed instructions – RISC-V M standard extension for integer multiplication and division – RISC-V A standard extension for atomic instructions – RISC-V Ziscr, Control and Status Register (CSR) instructions – RISC-V Zifencei Instruction-Fetch Fence – RISC-V B standard extension for bit manipulation (Zba, Zbb, Zbs) – Performance monitors, cycle and instruction count Control and Status Registers (CSRs) • Dynamic branch prediction • Privilege mode: Machine mode • Machine timer • RISC-V external debug support – Debug module (DM) • 4 hardware breakpoint/watchpoint registers – Debug transport module (DTM) – Debug port: cJTAG

Table 1.2 Memory

Feature	Functional description
Code flash memory	128-KB of code flash memory.
Data flash memory	4-KB of data flash memory
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	16-KB On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • UART (SAU) boot mode
Resets	The MCU provides 12 resets (RES pin reset, power-on reset, independent watchdog timer reset, watchdog timer reset, voltage monitor 0/1/2 resets, SRAM parity error reset, SRAM ECC error reset, bus error reset, debug reset, software reset).
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	• External clock input (EXTAL) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Core-Local Interrupt Controller (CLIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Key Interrupt Function (KINT)	The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.6 Timers (1 of 2)

Feature	Functional description
Realtime Clock (RTC)	The realtime clock has the following features: • Capable of counting years, months, days of the week, dates, hours, minutes, and seconds, for up to 99 years • Fixed-cycle interrupt (with period selectable from among 0.5 of a second, 1 second, 1 minute, 1 hour, 1 day, or 1 month) • Alarm interrupt (alarm set by day of week, hour, and minute) • Pin output function of 1 Hz

Table 1.6 Timers (2 of 2)

Feature	Functional description
Timer Array Unit (TAU)	The timer array unit has eight 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be used to create a high-accuracy timer.
32-bit Interval Timer (TML32)	The 32-bit interval timer is made up of four 8-bit interval timers (reference as channels 0 to 3). Each is capable of operating independently and in that case, they all have the same functions. Two 8-bit interval timer channels can be connected to operate as a 16-bit interval timer. Four 8-bit interval timer channels can be connected to operate as a 32-bit interval timer.

Table 1.7 Communication interfaces

Feature	Functional description
Serial Array Unit (SAU)	A single serial array unit has up to four serial channels. Each channel can achieve 3-wire serial (simplified SPI), UART, and simplified I^2C communication.
I^2C Bus Interface (IICA)	The I^2C bus interface has the following three modes: ● Operation stop mode ● I^2C bus mode (multi-master supported) ● Wakeup mode
Serial Interface UARTA (UARTA)	The serial interface UARTA supports the following two modes: ● Operation stop mode ● UART mode
Remote Control Signal Receiver (REMC)	The remote control signal receiver can receive data by checking the width and period of an external pulse input signal.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 10 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
Comparator (CMP)	The Comparator (CMP) compares a test voltage with a reference voltage and provides a digital output based on the comparison result. The test voltages can be provided to the comparator from an external. The reference voltages can be provided to the comparator from internal DAC8 output and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.
8-bit D/A Converter (DAC8)	Two channels of 8-bit D/A Converter (DAC8) can be used as comparator reference voltage and can be output externally.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The data operation circuit (DOC) is used to compare, add, and subtract 16 or 32-bit data. An interrupt can be generated when the following conditions apply: ● When the 16 or 32-bit compared values match the detection condition ● When the result of 16 or 32-bit data addition overflows ● When the result of 16 or 32-bit data subtraction underflows
True Random Number Generator (TRNG)	The true random number generator generates 32-bit random number seeds (which are true random numbers).

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

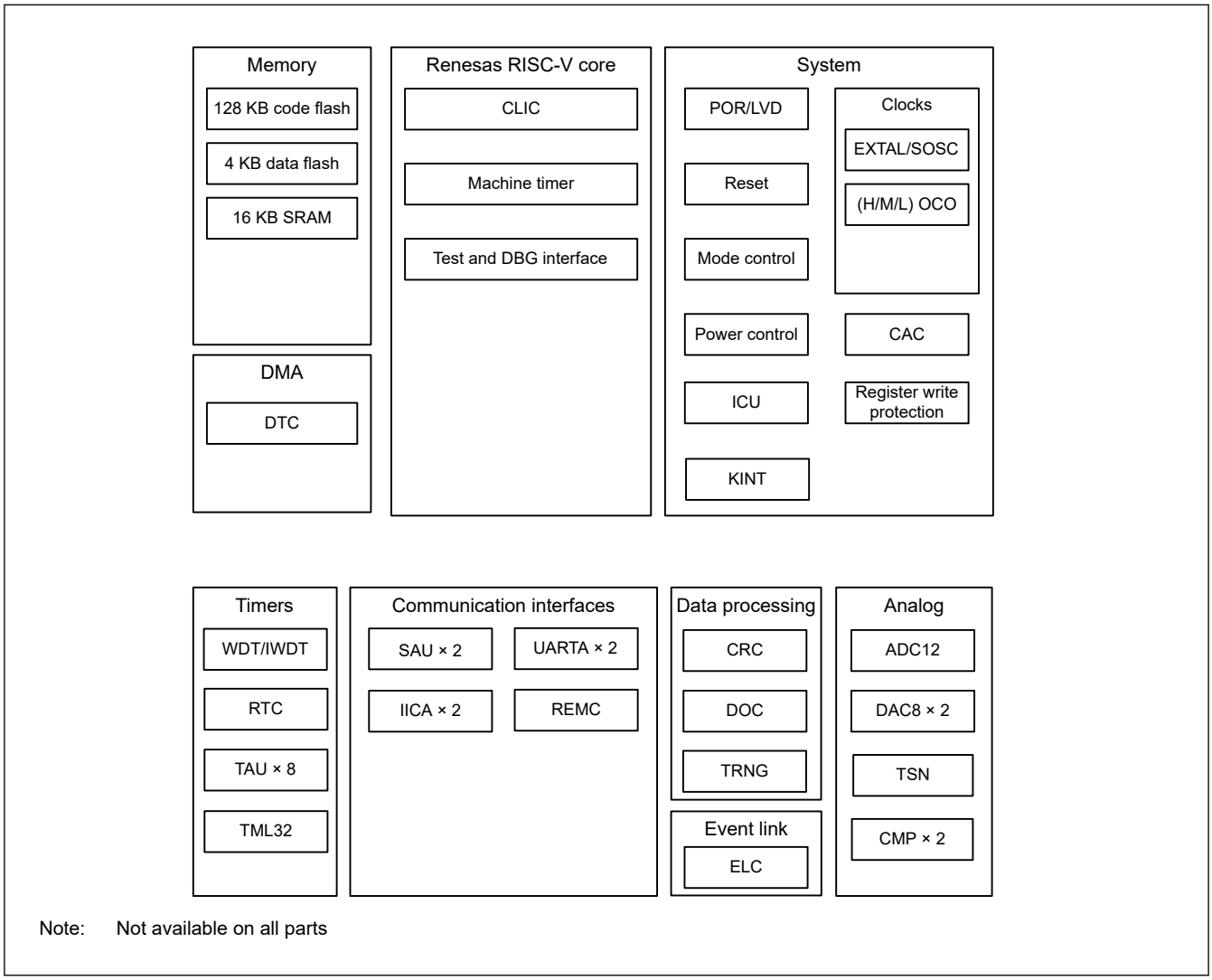


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.10 shows a list of products.

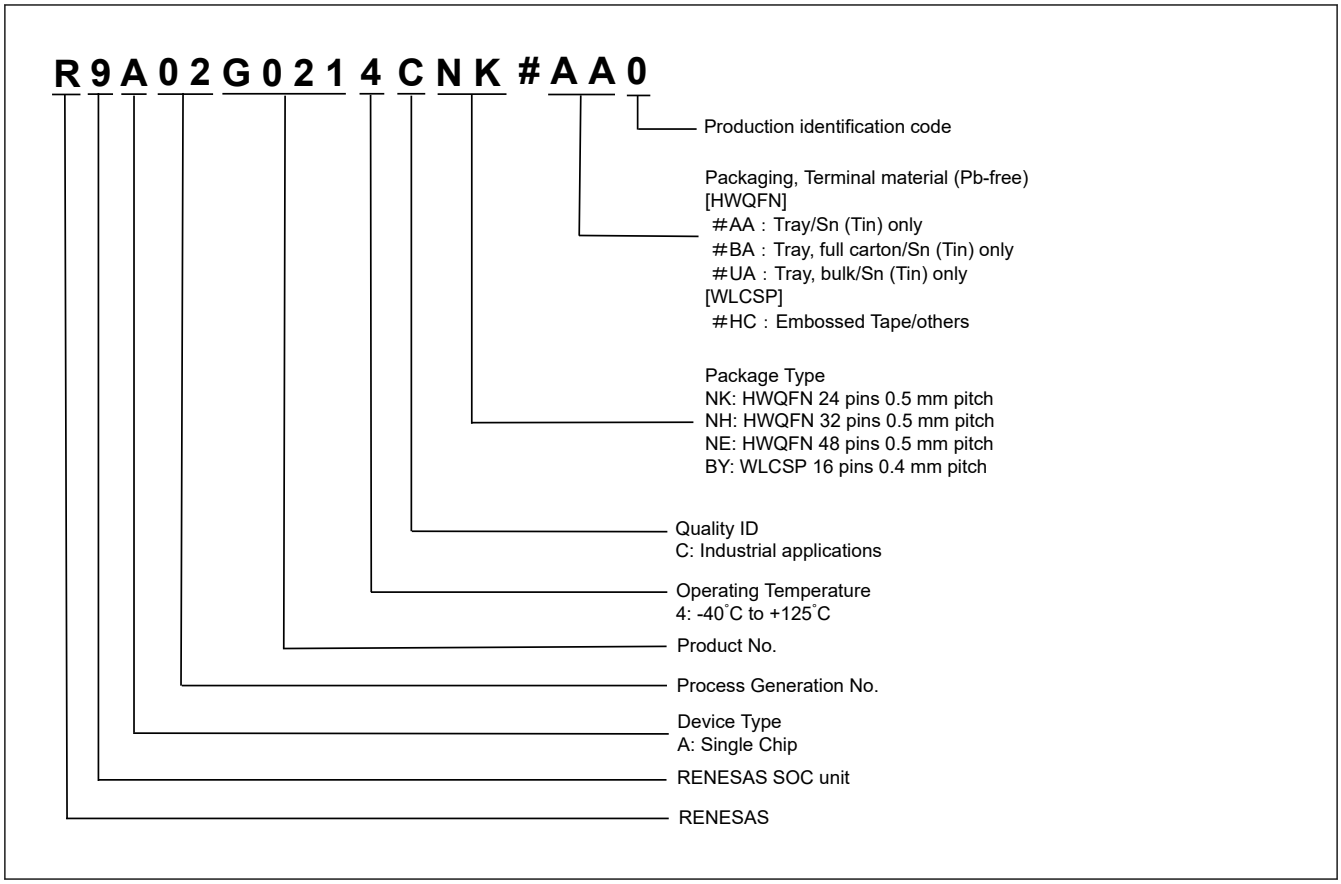


Figure 1.2 Part numbering scheme

Table 1.10 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R9A02G0214CNE	PWQN0048KC-A	128 KB	4 KB	16 KB	-40 to +125°C
R9A02G0214CNH	PWQN0032KE-A				
R9A02G0214CNK	PWQN0024KG-A				
R9A02G0214CBY	SUBG0016LC-A				

1.4 Function Comparison

Table 1.11 Function comparison

Part number		R9A02G0214CNE	R9A02G0214CNH	R9A02G0214CNK	R9A02G0214CBY
Pin count		48	32	24	16
Package		HWQFN	HWQFN	HWQFN	WLCSP
Code flash memory		128 KB	128 KB	128 KB	128 KB
Data flash memory		4 KB	4 KB	4 KB	4 KB
SRAM (Parity)		12 KB	12 KB	12 KB	12 KB
SRAM (ECC)		4 KB	4 KB	4 KB	4 KB
System	CPU clock	48 MHz	48 MHz	48 MHz	48 MHz
	Sub-clock oscillator	Yes	Yes	Yes	No
	ICU	Yes	Yes	Yes	Yes
	CAC	Yes	Yes	Yes	Yes
	KINT	6	2	No	No
ELC control	ELC	Yes	Yes	Yes	Yes
DMA	DTC	Yes	Yes	Yes	Yes
Timers	WDT/IWDT	Yes	Yes	Yes	Yes
	RTC	Yes	Yes	Yes	Yes
	TAU	8	8	8	6
	TML32	Yes	Yes	Yes	Yes
Communication	SAU	6 (Simplified SPI)	3 (Simplified SPI)	3 (Simplified SPI)	1 (Simplified SPI)
		3 (UART)	3 (UART)	3 (UART)	2 (UART)
		6 (Simplified I^2C)	3 (Simplified I^2C)	3 (Simplified I^2C)	1 (Simplified I^2C)
	IICA	2	1	1	1
	UARTA	2	No	No	No
	REMC	Yes	Yes	No	No
Analog	ADC12	10	8	6	4
	CMP	2	2	2	1
	DAC8	2	2	2	2
	TSN	Yes	Yes	Yes	Yes
Data processing	CRC	Yes	Yes	Yes	Yes
	DOC	Yes	Yes	Yes	Yes
	TRNG	Yes	Yes	Yes	Yes
I/O port	General-purpose I/O	42	26	18	12
	Output current control port	3	3	3	3

1.5 Pin Functions

Table 1.12 Pin functions (1 of 2)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	EXTAL	Input	An external clock signal can be input
	XT1	Input	Input/output pins for the sub-clock oscillator Connect a crystal resonator between XT1 and XT2
	XT2	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	TMSC	I/O	On-chip emulator pins
	TCKC	Input	
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
KINT	KR00 to KR05	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
RTC	RTC1HZ	Output	Realtime clock correction clock (1 Hz) output
TAU	TI00 to TI07	Input	The pins for inputting an external count clock/capture trigger to 16-bit timers 00 to 07
	TO00 to TO07	Output	Timer output pins of 16-bit timers 00 to 07
SAU	RxD0 to RxD2	Input	Serial data input pins of serial interfaces UART0, UART1, and UART2
	TxD0 to TxD2	Output	Serial data output pins of serial interfaces UART0, UART1, and UART2
	SCK00, SCK01, SCK10, SCK11,SCK20, SCK21	I/O	Serial clock I/O pins of serial interfaces SPI00, SPI01, SPI10, SPI11, SPI20, and SPI21
	SCL00, SCL01, SCL10, SCL11, SCL20, SCL21	Output	Serial clock output pins of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, and IIC21
	SDA00, SDA01, SDA10, SDA11, SDA20, SDA21	I/O	Serial data I/O pins of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, and IIC21
	SI00, SI01, SI10, SI11, SI20, SI21	Input	Serial data input pins of serial interfaces SPI00, SPI01, SPI10, SPI11, SPI20, and SPI21
	SO00, SO01, SO10, SO11, SO20, SO21	Output	Serial data output pins of serial interfaces SPI00, SPI01, SPI10, SPI11, SPI20, and SPI21
IICA	SCLA0, SCLA1	I/O	Clock I/O pins of I^2C bus interfaces IICA0 and IICA1
	SDAA0, SDAA1	I/O	Serial data I/O pins of I^2C bus interfaces IICA0 and IICA1
UARTA	RxDA0, RxDA1	Input	Serial data input pins of serial interfaces UARTA0 and UARTA1
	TxDA0, TxDA1	Output	Serial data output pins of serial interfaces UARTA0 and UARTA1
	CLKA0, CLKA1	Output	Clock output pins of serial interfaces UARTA0 and UARTA1

Table 1.12 Pin functions (2 of 2)

Function	Signal	I/O	Description
REMC	RIN0	Input	External pulse signal input pin for the remote control signal reception circuit
Analog power supply	AVREFP	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12.
	AVREFM	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12.
ADC12	ANI0 to ANI5, ANI16 to ANI19	Input	Input pins for the analog signals to be processed by the ADC12.
CMP	IVREF0, IVREF1	Input	Reference voltage input pins for comparator
	IVCMP0, IVCMP1	Input	Analog voltage input pins for comparator
	VCOUT0, VCOUT1	Output	Comparator detection result output pins.
DAC8	DACOUT0, DACOUT1	Output	Output pins for the analog signals to be processed by the DAC8.
I/O ports	P000 to P003 , P006 to P011	I/O	General-purpose input/output pins
	P100 to P111	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P207	I/O	General-purpose input/output pins
	P300 to P307	I/O	General-purpose input/output pins
	P400 to P403	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.6 show the pin assignments from the top view.

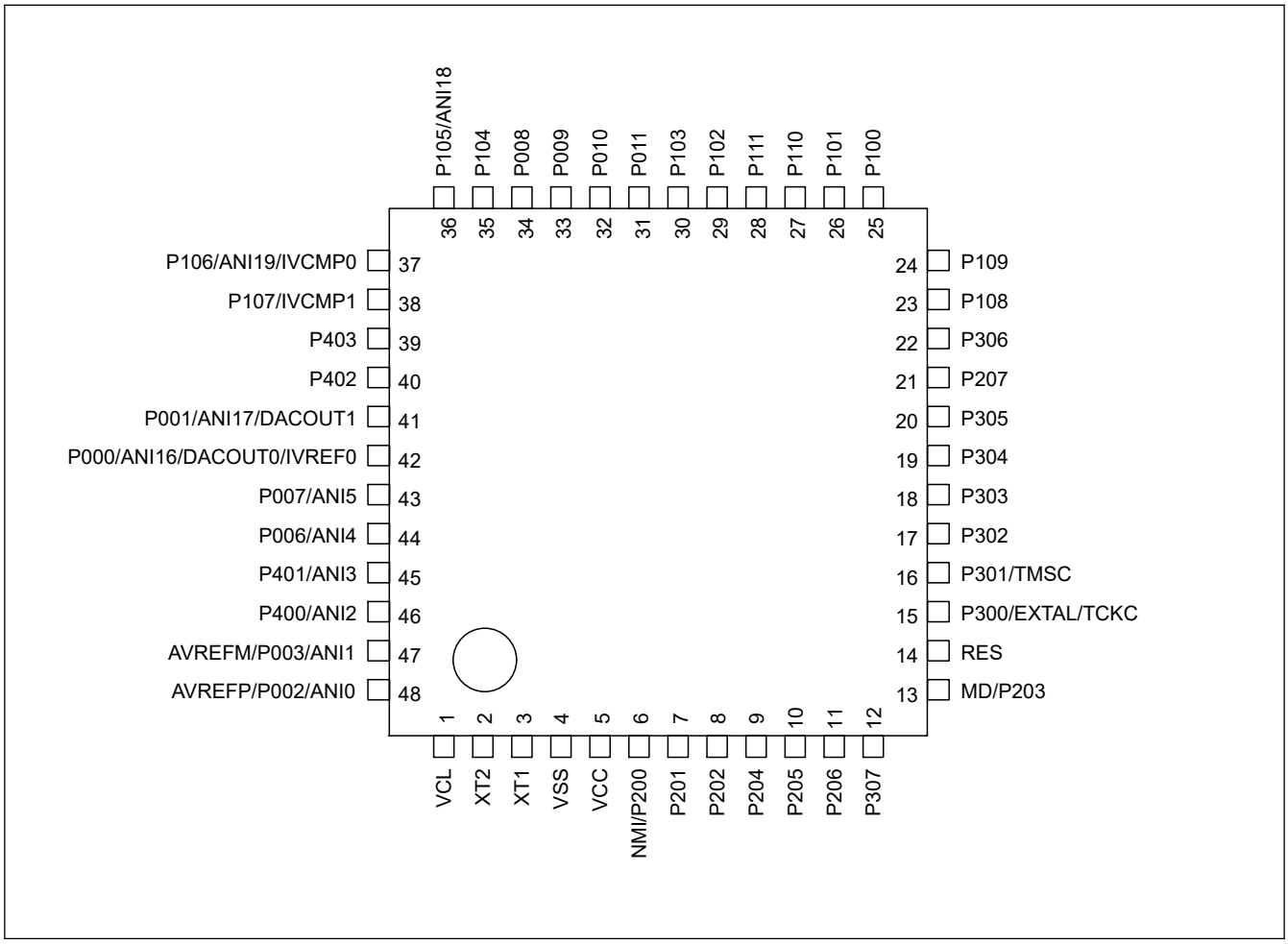


Figure 1.3 Pin assignment for HWQFN 48-pin (top view)

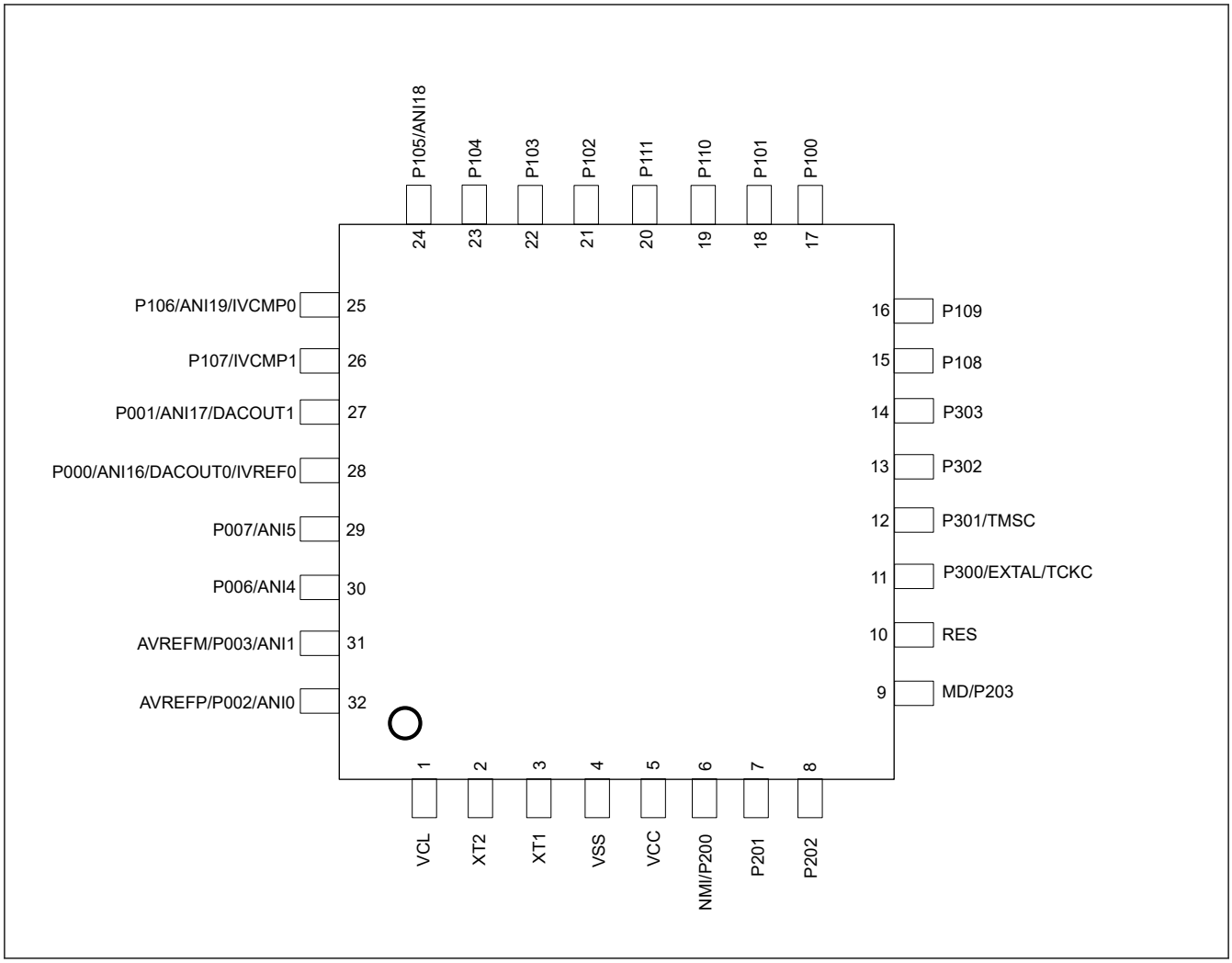


Figure 1.4 Pin assignment for HWQFN 32-pin (top view)

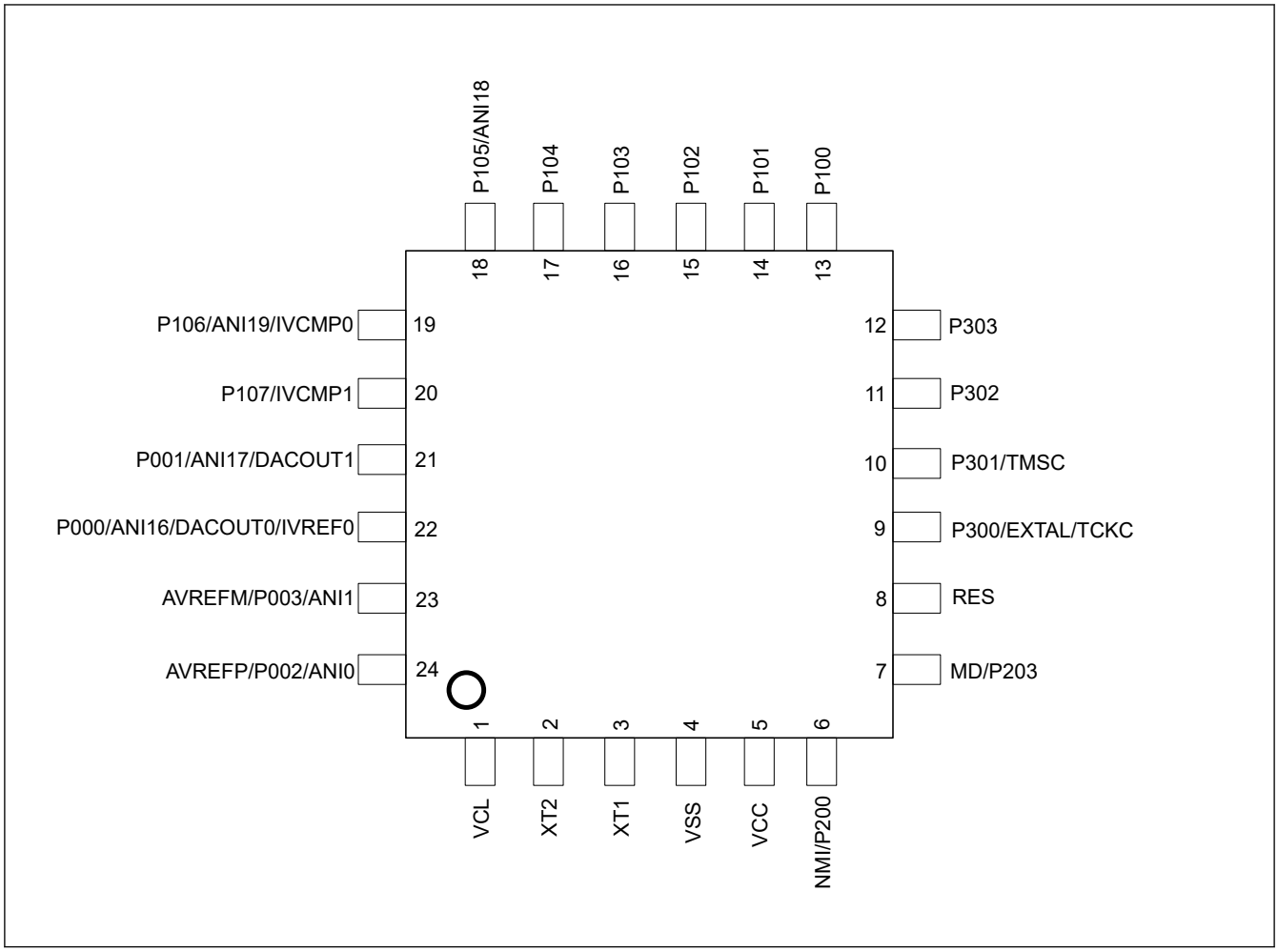


Figure 1.5 Pin assignment for HWQFN 24-pin (top view)

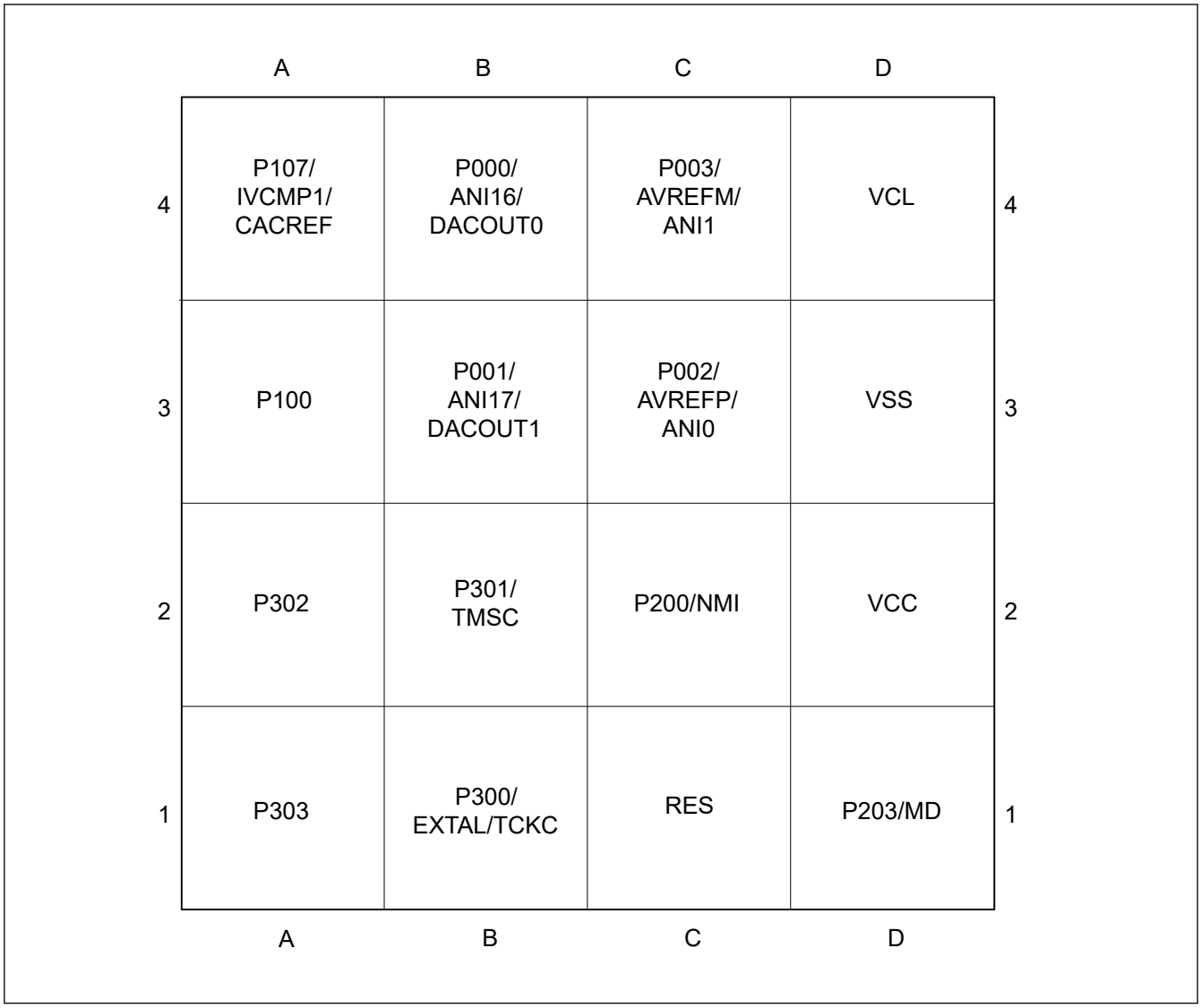


Figure 1.6 Pin assignment for WLCSP 16-pin (top view, pad side down)

1.7 Pin Lists

Table 1.13 Pin list (1 of 2)

Pin number				Power, System, Clock, Debug, CAC	I/O ports	Timers	Communication interfaces		Analogs	Interrupt, KINT
QFN 48-pin	QFN 32-pin	QFN 24-pin	WLCSP 16-pin			TAU, RTC	REMC, IICA, UARTA	SAU	ADC12, DAC8, CMP	
1	1	1	D4	VCL	—	—	—	—	—	—
2	2	2	—	XT2	—	—	—	—	—	—
3	3	3	—	XT1	—	—	—	—	—	—
4	4	4	D3	VSS/AVSS	—	—	—	—	—	—
5	5	5	D2	VCC/AVCC	—	—	—	—	—	—
6	6	6	C2	NMI	P200	—	—	—	—	NMI
7	7	—	—	—	P201	—	—	—	—	IRQ3_C
8	8	—	—	CLKOUT_B	P202	—	RIN0	—	—	IRQ2_C
9	—	—	—	—	P204	—	—	SCK21/SCL21	—	—
10	—	—	—	—	P205	—	—	SI21/SDA21	—	—
11	—	—	—	—	P206	—	—	SO21	—	—
12	—	—	—	—	P307	—	—	—	—	—
13	9	7	D1	MD	P203	—	—	—	—	—
14	10	8	C1	RES#	—	—	—	—	—	—
15	11	9	B1	EXTAL/TCKC	P300	TI07_A/TO07_A	—	SCK00/SCL00	—	IRQ0_A
16	12	10	B2	TMSC	P301	TI06/TO06	—	SI00/SDA00/ RxD0_A	—	IRQ1_A
17	13	11	A2	—	P302	TI03_B/TO03_B	SCLA0_A	TxD0_B	VCOUT1	IRQ3_B
18	14	12	A1	CLKOUT_A	P303	TI04/TO04	SDAA0_A	RxD0_B	—	IRQ2_B
19	—	—	—	—	P304	—	—	SO01	—	KR00
20	—	—	—	—	P305	—	—	SI01/SDA01	—	KR01
21	—	—	—	—	P207	—	—	SCK01/SCL01	—	KR02
22	—	—	—	—	P306	—	—	—	—	KR03
23	15	—	—	—	P108	—	—	—	—	IRQ4_B/KR04
24	16	—	—	—	P109	—	—	—	—	IRQ5_B/KR05
25	17	13	A3	—	P100	TI05/TO05	—	SO00/TxD0_A	—	IRQ6_C
26	18	14	—	—	P101	TI02_B/TO02_B	—	SCK20/SCL20	—	IRQ7_C
27	19	—	—	—	P110	—	—	—	—	IRQ7_B
28	20	—	—	—	P111	—	—	—	—	IRQ6_B
29	21	15	—	—	P102	TI01/TO01	SCLA0_B	SI20/SDA20/ RxD2	—	IRQ2_A
30	22	16	—	—	P103	TI02_A/TO02_A	SDAA0_B	SO20/TxD2	—	—
31	—	—	—	—	P011	TI07_B/TO07_B	SCLA1/CLKA0	—	—	—
32	—	—	—	—	P010	—	SDAA1/RxDA0	—	—	—
33	—	—	—	—	P009	—	TxDA0	SCK10/SCL10	—	—
34	—	—	—	—	P008	—	RxDA1	SI10/SDA10	—	—
35	23	17	—	—	P104	—	—	SCK11/SCL11	IVREF1	—
36	24	18	—	—	P105	RTC1HZ	—	SI11/SDA11	ANI18/VCOUT0	—
37	25	19	—	—	P106	—	—	SO11	ANI19/IVCMP0	—
38	26	20	A4	CACREF	P107	TI03_A/TO03_A	—	—	IVCMP1	—
39	—	—	—	—	P403	—	TxDA1	SO10	—	—
40	—	—	—	—	P402	—	CLKA1	—	—	—
41	27	21	B3	—	P001	TI00	—	TxD1	ANI17/DACOUT1	IRQ5_A
42	28	22	B4	—	P000	TO00	—	RxD1	ANI16/ DACOUT0/ IVREF0*1	IRQ6_A

Table 1.13 Pin list (2 of 2)

Pin number				Power, System, Clock, Debug, CAC	I/O ports	Timers	Communication interfaces		Analogs	Interrupt, KINT
QFN 48-pin	QFN 32-pin	QFN 24-pin	WLCSP 16-pin			TAU, RTC	REMC, IICA, UARTA	SAU	ADC12, DAC8, CMP	
43	29	—	—	—	P007	—	—	—	ANI5	IRQ3_A
44	30	—	—	—	P006	—	—	—	ANI4	IRQ4_A
45	—	—	—	—	P401	—	—	—	ANI3	—
46	—	—	—	—	P400	—	—	—	ANI2	—
47	31	23	C4	AVREFM	P003	—	—	—	ANI1	IRQ7_A
48	32	24	C3	AVREFP	P002	—	—	—	ANI0	—

Note: Several pin names have the added suffix of _A, _B, and _C. The suffix can be ignored when assigning functionality.
Note 1. IVREF0 is not supported in WLCSP 16-pin

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC = 1.6 to 5.5 V

VSS = 0 V, Ta = T_{opr}

Figure 2.1 shows the timing conditions.

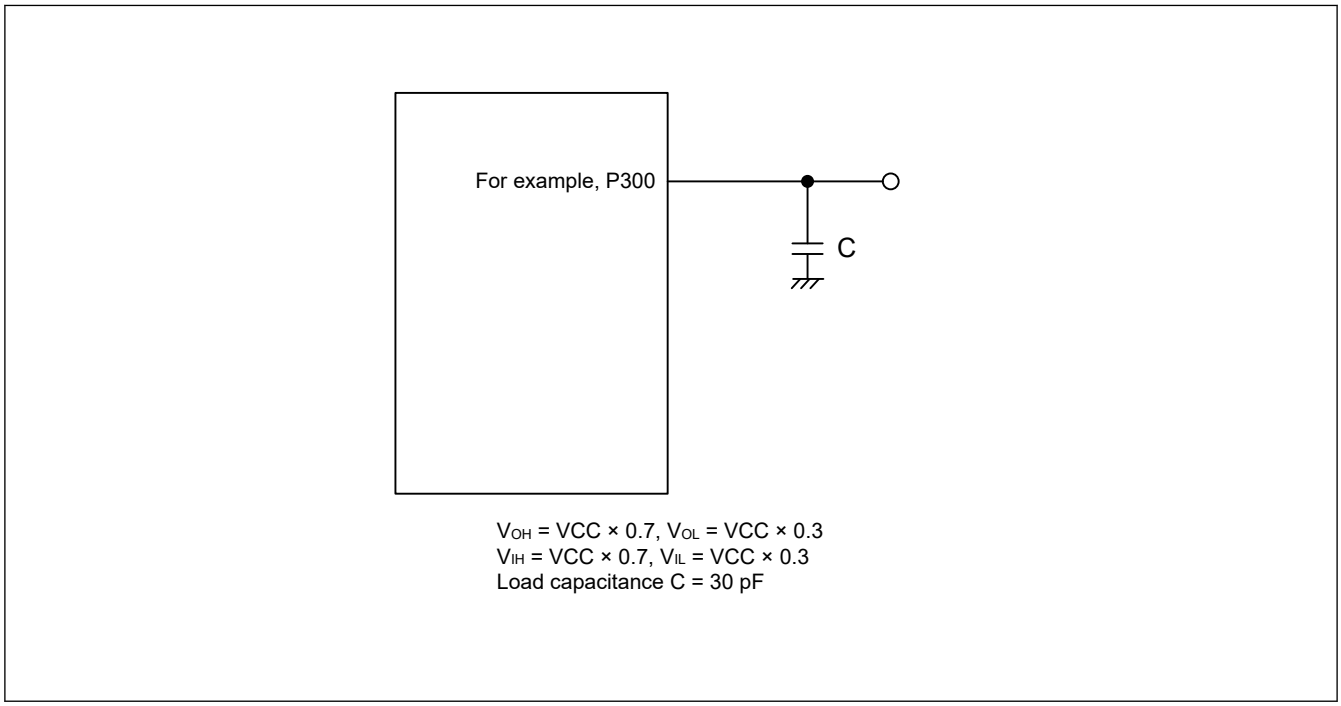


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	-0.5 to +6.5	V
Input voltage	V_{in}	-0.3 to VCC + 0.3	V
Analog input voltage	V_{AN}	-0.3 to VCC + 0.3	V
Operating temperature*1	T_{opr}	-40 to +125	°C
Storage temperature	T_{stg}	-55 to +140	°C

Note 1. See section 2.2.1. Tj/Ta Definition.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, and between the AVREFP and AVREFM pins when AVREFP is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- **VCC and VSS: about 0.1 µF**
- **AVREFP and AVREFM: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	1.6	—	5.5	V
	VSS	—	0	—	V

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	140	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	5V-tolerant ports (P010, P011, P101, P102, P103)	V_{IH}	VCC × 0.7	—	5.8	V	—
		V_{IL}	—	—	VCC × 0.3		
	RES, NMI Other peripheral input pins	V_{IH}	VCC × 0.8	—	—		—
		V_{IL}	—	—	VCC × 0.2		—

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (average value per pin)	ANI0-5 ports (P002 to P003, P006 to P007, P400 to P401)	I_{OH}	—	—	-4.0	mA	—
		I_{OL}	—	—	8.0	mA	
	5V-tolerant ports (P010 to P011, P101 to P103)	I_{OH}	—	—	-4.0	mA	—
		I_{OL}	—	—	8.0	mA	
	Other output pins*1	I_{OH}	—	—	-4.0	mA	—
		I_{OL}	—	—	20.0	mA	

Table 2.5 I/O I_{OH}, I_{OL} (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	Total of ANI0-5 ports (P002 to P003, P006 to P007, P400 to P401)	$\Sigma I_{OH\ (max)}$	—	—	-24.0	mA	VCC = 2.7 to 5.5 V
			—	—	-6.0	mA	VCC = 1.8 to 2.7 V
			—	—	-3.0	mA	VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	48.0	mA	VCC = 2.7 to 5.5V
			—	—	3.6	mA	VCC = 1.8 to 2.7 V
			—	—	1.8	mA	VCC = 1.6 to 1.8 V
	5V-tolerant ports (P010 to P011, P101 to P103)	$\Sigma I_{OH\ (max)}$	—	—	-20.0	mA	VCC = 2.7 to 5.5V
			—	—	-5.0	mA	VCC = 1.8 to 2.7 V
			—	—	-2.0	mA	VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	40.0	mA	VCC = 2.7 to 5.5 V
			—	—	3.0	mA	VCC = 1.8 to 2.7 V
			—	—	1.5	mA	VCC = 1.6 to 1.8 V
	Total of other output ports	$\Sigma I_{OH\ (max)}$	—	—	-30.0	mA	VCC = 2.7 to 5.5 V
			—	—	-12.0	mA	VCC = 1.8 to 2.7 V
			—	—	-6.0	mA	VCC = 1.6 to 1.8 V
		$\Sigma I_{OL\ (max)}$	—	—	50.0	mA	VCC = 2.7 to 5.5 V
			—	—	9.0	mA	VCC = 1.8 to 2.7 V
			—	—	4.5	mA	VCC = 1.6 to 1.8 V
	Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-50.0	mA	—
		$\Sigma I_{OL\ (max)}$	—	—	95.0	mA	

Note 1. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Output pins*1	V_{OH}	VCC - 0.8	—	—	V	I_{OH} = -4.0 mA
	P002 to P003, P006 to P007, P400 to P401	V_{OL}	—		0.8		I_{OL} = 8.0 mA
	P010 to P011, P101 to P103	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Other output pins*1	V_{OL}	—	—	1.2		I_{OL} = 20.0 mA

Note 1. Except for Ports P200, which are input ports, and XT1 and XT2, which are SOSC ports.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Output pins*1	V_{OH}	VCC - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, which are input ports, and XT1 and XT2, which are SOSC ports.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage	Output pins*1	V_{OH}	VCC - 0.5	—	—	V	IOH = -1.0 mA VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		IOH = -0.5 mA VCC = 1.6 to 1.8 V
	Output pins*1	V_{OL}	—	—	0.4		IOL = 0.6 mA VCC = 1.8 to 2.7 V
			—	—	0.4		IOL = 0.3 mA VCC = 1.6 to 1.8 V

Note 1. Except for Ports P200, which are input ports, and XT1 and XT2, which are SOSC ports.

Table 2.9 I/O other characteristics

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Constant low-level current output*1	P100, P302, P303	$CCDI_{OL}$	1.15	2	2.87	mA	PmnPFS.DSCR = b00, VCC = 4.0 V to 5.5 V
			0.97	1.7	2.59	mA	PmnPFS.DSCR = b00, VCC = 2.7 V to 4.0 V
			2.95	5	6.97	mA	PmnPFS.DSCR = b01, VCC = 4.0 V to 5.5 V
			2.64	4.2	6.38	mA	PmnPFS.DSCR = b01, VCC = 3.0 V to 4.0 V
			5.97	10	13.48	mA	PmnPFS.DSCR = b1x, VCC = 4.0 V to 5.5 V
			5.6	8.5	12.38	mA	PmnPFS.DSCR = b1x, VCC = 3.3 V to 4.0 V
Input leakage current	RES, P200, XT1, XT2	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports (P010 to P011, P101 to P103)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200, XT1, XT2 and 5V-tolerant ports)		—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, XT1, XT2)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		—	—	15		

Note 1. The listed currents apply when the output current control function is enabled.

2.2.5 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions *1 *2: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*11	Max	Unit	Test Conditions
Supply current*3	High-speed mode*4	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*7	ICLK = 48 MHz	I_{CC}	7.80	—	mA	*9 *12
				ICLK = 32 MHz		6.45	—		*9
				ICLK = 16 MHz		4.00	—		
				ICLK = 8 MHz		2.70	—		
			All peripheral clocks enabled, code executing from flash*7	ICLK = 48 MHz		—	17.4		*12
		Sleep mode	All peripheral clocks disabled*7	ICLK = 48 MHz		1.80	—		*9
				ICLK = 32 MHz		1.40	—		
				ICLK = 16 MHz		1.00	—		
				ICLK = 8 MHz		0.80	—		
			All peripheral clocks enabled*7	ICLK = 48 MHz		3.70	—		*10
				ICLK = 32 MHz		2.60	—		
				ICLK = 16 MHz		1.65	—		
				ICLK = 8 MHz		1.10	—		
		Increase during BGO operation*8				1.95	—		—
	Middle-speed mode*4	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*7	ICLK = 24 MHz	I_{CC}	4.80	—	mA	*9
				ICLK = 4 MHz		1.35	—		
			All peripheral clocks enabled, code executing from flash*7	ICLK = 24 MHz		—	10.1		*10
		Sleep mode	All peripheral clocks disabled*7	ICLK = 24 MHz		1.20	—		*9
				ICLK = 4 MHz		0.70	—		
			All peripheral clocks enabled*7	ICLK = 24 MHz		2.20	—		*10
		Increase during BGO operation*8				2.05	—		—
	Low-speed mode*5	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*7	ICLK = 1 MHz	I_{CC}	0.35	—	mA	*9
			All peripheral clocks enabled, code executing from flash*7	ICLK = 1 MHz		—	2.8		*10
		Sleep mode	All peripheral clocks disabled*7	ICLK = 1 MHz		0.20	—		*9
			All peripheral clocks enabled*7	ICLK = 1 MHz		0.25	—		*10

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions *1 *2: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*11	Max	Unit	Test Conditions
Supply current*3	Subosc-speed mode*6	Normal mode	All peripheral clocks enabled, code executing from flash*7	ICLK = 32.768 kHz	I_{CC}	—	1.6	mA	*10
		Sleep mode	All peripheral clocks disabled*7	ICLK = 32.768 kHz		2.30	—	µA	*10
			All peripheral clocks enabled*7	ICLK = 32.768 kHz		3.65	—		*10

Note 1. Conditions for high-speed mode are VCC = 1.8 to 5.5 V.
Note 2. Conditions for middle-speed mode are VCC = 1.8 to 5.5 V when ICLK = 24 MHz.
Note 3. Supply current is the total current flowing into VCC, including analog power supply current. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 4. The clock source is HOCO.
Note 5. The clock source is MOCO.
Note 6. The clock source is the sub-clock oscillator.
Note 7. This does not include BGO operation.
Note 8. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 9. PCLKB is set to be divided by 64.
Note 10. PCLKB is the same frequency as that of ICLK.
Note 11. VCC = 3.3 V.
Note 12. The prefetch is operating.

Table 2.11 Operating and standby current (2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*3	Max	Unit	Test conditions
Supply current *1	Software Standby mode*2	Peripheral modules stop	All SRAM (0x2000_0000 to 0x2000_0FFF and 0x2000_4000 to 0x2000_6FFF) is on	T_a = 25°C	I_{CC}	0.30	1.8	µA	—
				T_a = 55°C		0.45	5.1		
				T_a = 85°C		1.15	20		
				T_a = 105°C		2.75	48		
				T_a = 125°C		6.95	112		
			8KB SRAM (0x2000_0000 to 0x2000_0FFF and 0x2000_4000 to 0x2000_4FFF) is on	T_a = 25°C		0.30	1.8		
				T_a = 55°C		0.45	4.8		
				T_a = 85°C		1.15	19		
				T_a = 105°C		2.75	47		
				T_a = 125°C		6.95	108		
		Increment for RTC operation with low-speed on-chip*4				0.65	—		—
		Increment for RTC operation in normal operation mode with sub-clock oscillator*4				0.23	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RTCC0.RTC128EN is 0 (RTC operation in normal operation mode)
						0.97	—		SOMCR.SODRV[1:0] are 00b (normal mode) RTCC0.RTC128EN is 0 (RTC operation in normal operation mode)
		Increment for RTC operation in low-consumption clock mode with sub-clock oscillator*4				0.22	—		SOMCR.SODRV[1:0] are 11b (Low power mode 3) RTCC0.RTC128EN is 1 (RTC operation in low-consumption clock mode)
						0.95	—		SOMCR.SODRV[1:0] are 00b (normal mode) RTCC0.RTC128EN is 1 (RTC operation in low-consumption clock mode)

Note 1. Supply current is the total current flowing into VCC, including analog power supply current. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the low-speed on-chip oscillator or sub-oscillation circuit current.

Table 2.12 Operating and standby current (3)

Conditions *1, *2: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed conversion)	I_{VCCADC}	—	—	1.44	mA	—
	During 12-bit A/D conversion (at low-power conversion)		—	—	0.78	mA	—
	CMP enabled (at high-speed mode, per channel)	I_{VCCCMP}	—	6.0	—	µA	—
	CMP enabled (at low-speed mode, per channel)		—	2.0	—	µA	—
	DAC8 enabled (per channel)*1	I_{VCCDAC}	—	—	0.5	mA	—
Reference power supply current	During 12-bit A/D conversion	I_{REFH}	—	—	0.15	mA	—
Temperature Sensor (TSN) operating current*2		I_{TSN}	—	0.13	—	mA	—
12-bit A/D converter internal reference voltage current*2		I_{ADREF}	—	0.13	—	mA	—
Output current control operating current	CCDE register is not 0x00	I_{CCDA}	—	120*3	—	µA	—
	Per single output current control port*4	I_{CCDP}	—	30	—		Setting of the low-level output current: Hi-Z
			—	200	—		Setting of the low-level output current: 2 to 15 mA

Note 1. Conditions for DAC8 use are VCC = 2.7 to 5.5 V
Note 2. Conditions for TSN and internal reference voltage use are VCC = 1.8 to 5.5 V
Note 3. This current is added to the supply current when the output voltage control port is set at CCDIOL typical current CCTRM.IADJ setting if VCC = 4 V
Note 4. This current does not include the current flowing into the I/O port pins

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.13 Rise and fall gradient characteristics

Conditions: VCC = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1				—		

Note 1. When OFS1.LVDAS = 0.

Table 2.14 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

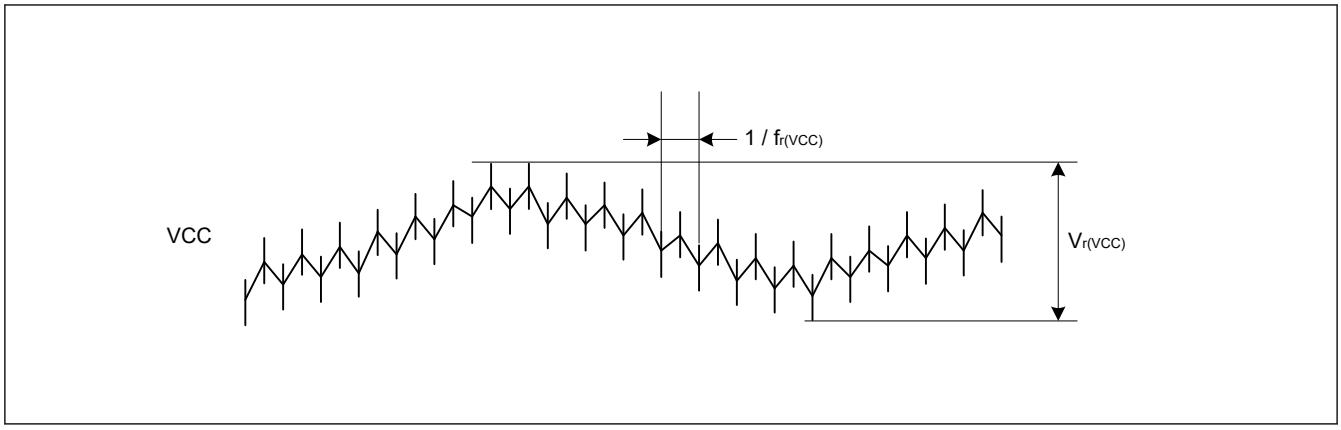


Figure 2.2 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.15 Operation frequency in high-speed mode

Conditions: VCC = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*3	Unit
Operation frequency	System clock (ICLK)*1 *2	1.8 to 5.5 V	f	0.032768	—	48	MHz
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	48	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.19.

Table 2.16 Operation frequency in middle-speed mode

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*3	Unit
Operation frequency	System clock (ICLK)*1 *2	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.19.

Table 2.17 Operation frequency in low-speed mode

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*3	Unit
Operation frequency	System clock (ICLK)*1 *2	1.6 to 5.5 V	f	0.032768	—	1	MHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ± 1.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.19.

Table 2.18 Operation frequency in Subosc-speed mode

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)	1.6 to 5.5 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.

2.3.2 Clock Timing

Table 2.19 Clock timing

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.3
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	—
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	—
EXTAL external clock rising time	t_{Xr}	—	—	5	ns	—
EXTAL external clock falling time	t_{Xf}	—	—	5	ns	—
EXTAL external clock input wait time*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL external clock input frequency	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		—	—	4	MHz	1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	μs	Figure 2.4
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	μs	—
HOCO clock oscillation frequency*5	f_{HOCO24}	23.64	24	24.36	MHz	Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO32}	31.52	32	32.48		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5
	f_{HOCO48}	47.28	48	48.72		Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*3 *4	t_{HOCO24} t_{HOCO32} t_{HOCO48}	—	6.7	7.7	μs	Figure 2.5
Sub-clock oscillator oscillation frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	—	0.5	—	s	Figure 2.6

Note 1. Time until the clock can be used after the external clock input stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 μs.
Note 4. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.
Note 5. Accuracy at production test.

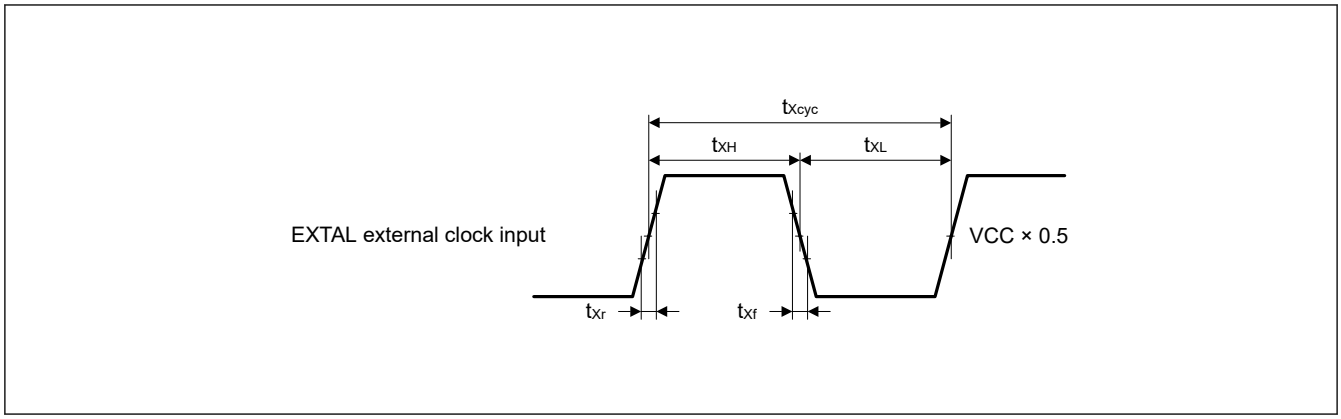


Figure 2.3 EXTAL external clock input timing

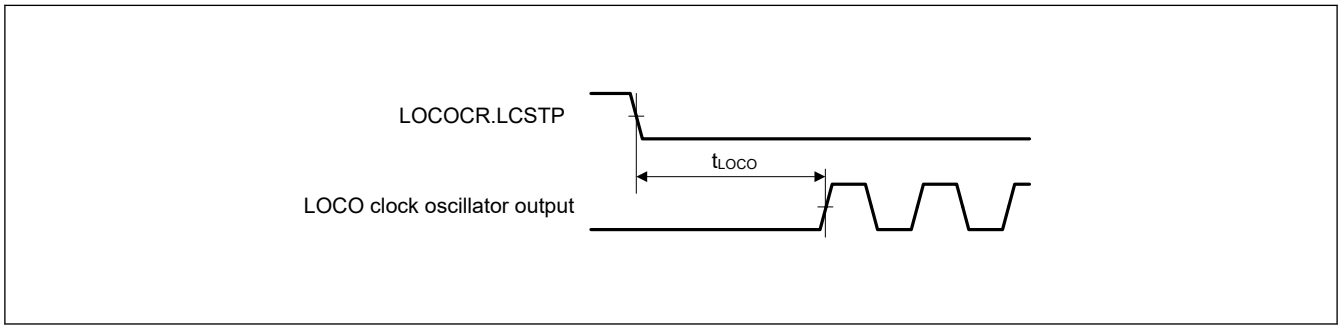


Figure 2.4 LOCO clock oscillation start timing

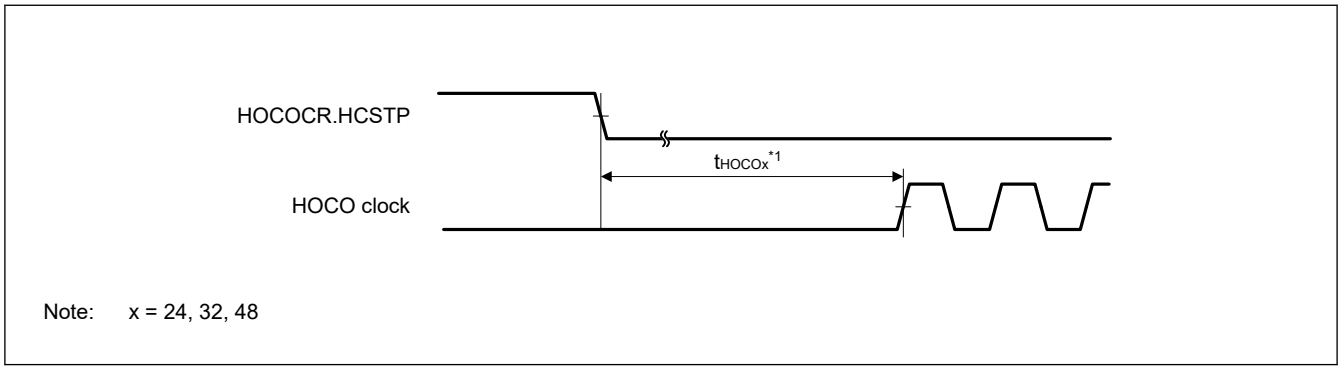


Figure 2.5 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

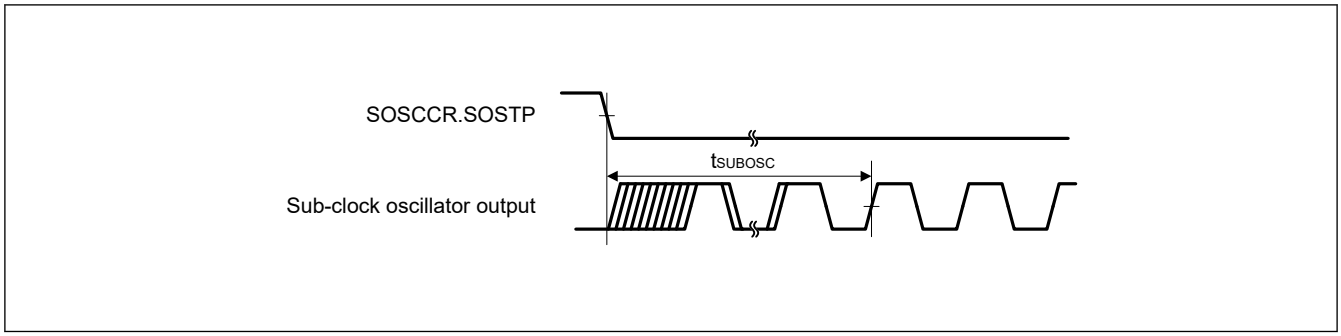


Figure 2.6 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.20 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	10	—	—	ms	Figure 2.7
	Not at power-on	t_{RESW}	30	—	—	μs	Figure 2.8
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 2.7
	LVD0 disabled*2		—	0.2	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.8
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus error reset, debug reset, software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.9
	LVD0 disabled*2		—	0.2	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

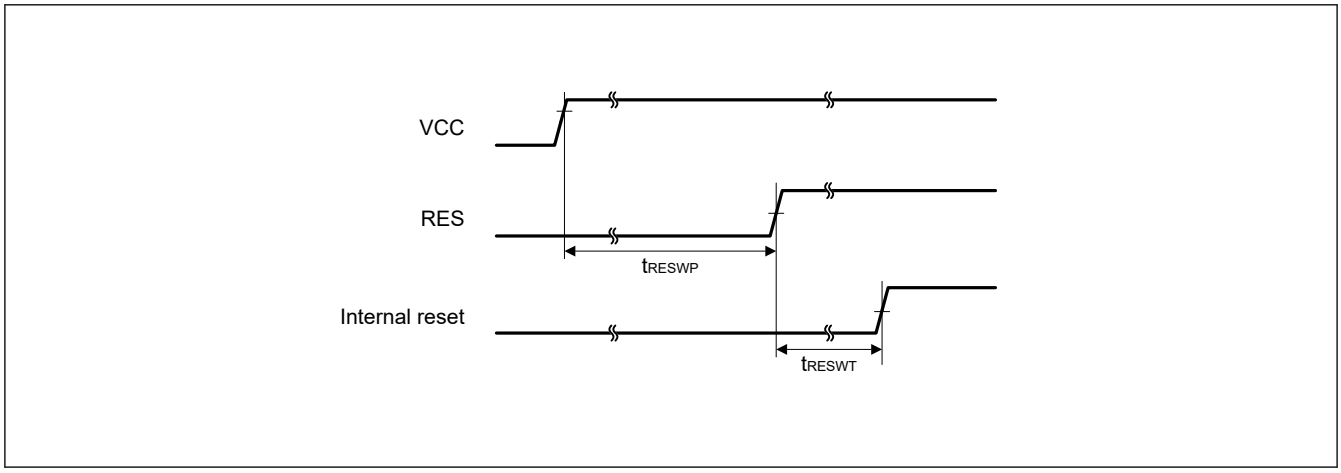


Figure 2.7 Reset input timing at power-on

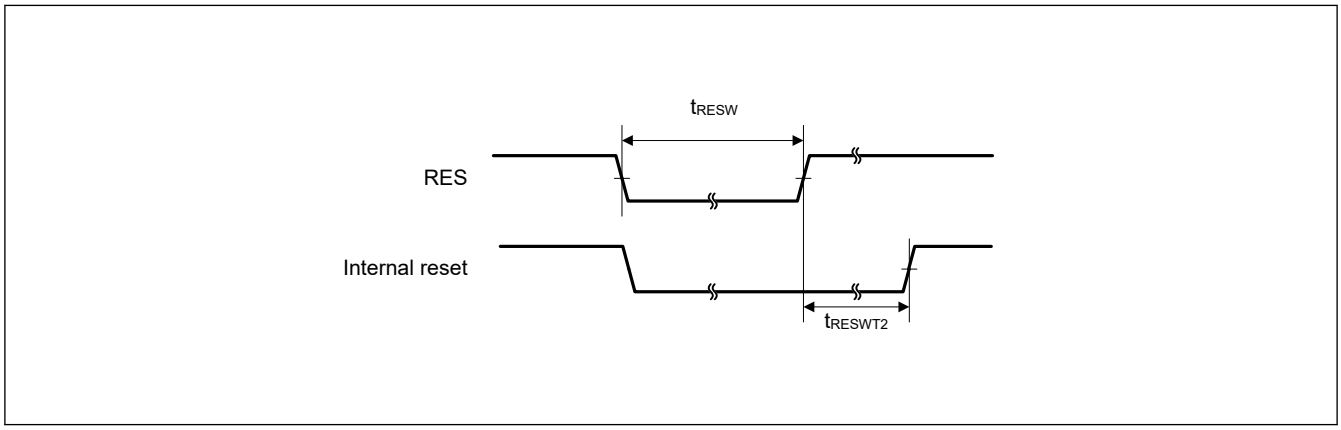


Figure 2.8 Reset input timing (1)

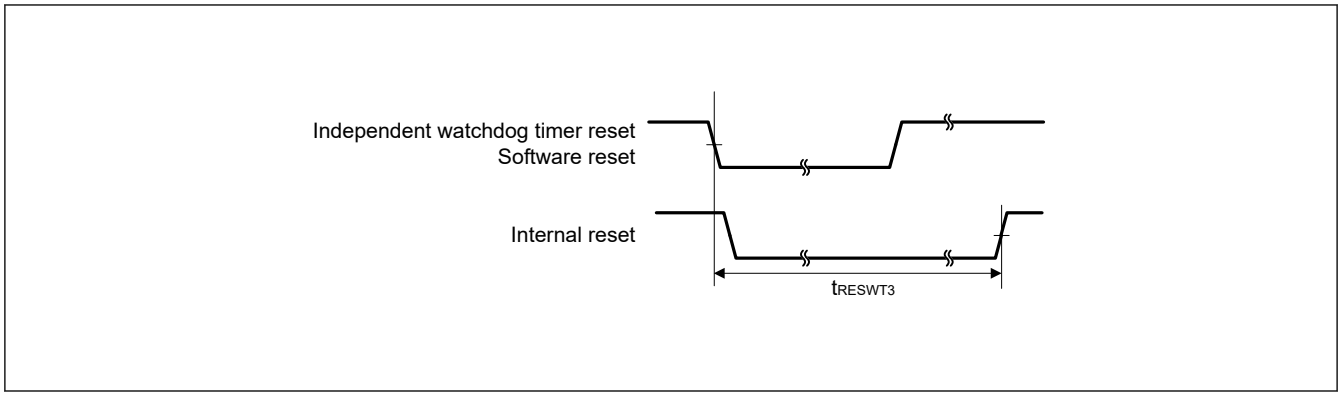


Figure 2.9 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.21 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	External clock input	System clock source is external clock input (20 MHz)	t_{SBYEX}	—	2.4	3.1	µs	Figure 2.10
		System clock source is HOCO (HOCO clock is 32 MHz)*2		t_{SBYHO}	—	7.4	9.1	µs	
		System clock source is HOCO (HOCO clock is 48 MHz)*3				7.2	8.9	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	4	5	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 32 MHz.
Note 3. The system clock is 48 MHz.

Table 2.22 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	External clock input	System clock source is external clock input (20 MHz) VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	Figure 2.10
			System clock source is external clock input (20 MHz) VCC = 1.6 V to 1.8 V		—	11.7	13		
		System clock source is HOCO*2	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 24 MHz.

Table 2.23 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	External clock input	System clock source is external clock input (1 MHz)	t_{SBYEX}	—	25	40	µs	Figure 2.10
		System clock source is MOCO (1 MHz)		t_{SBYMO}	—	26	40	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Table 2.24 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	—	0.85	1	ms	Figure 2.10
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

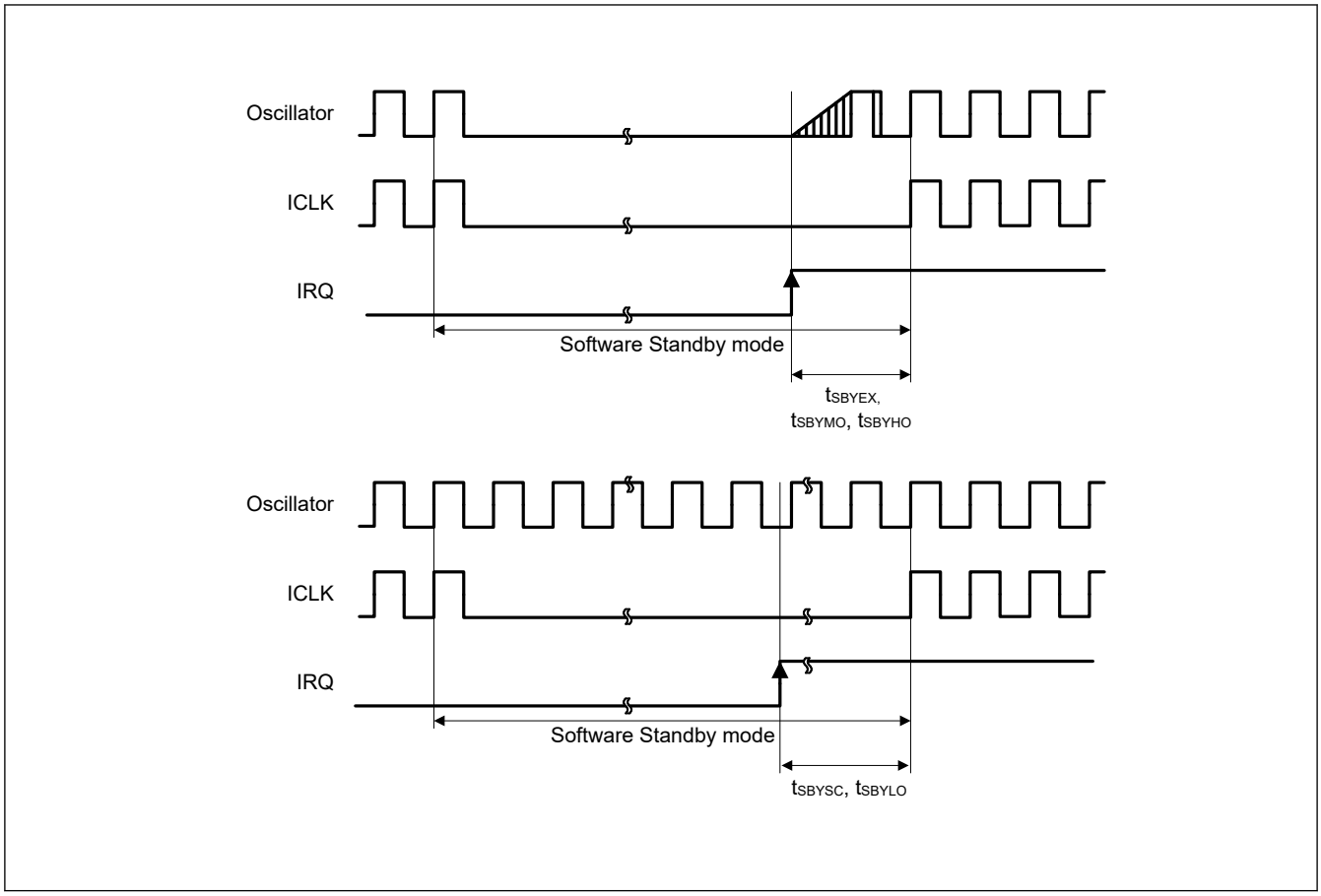
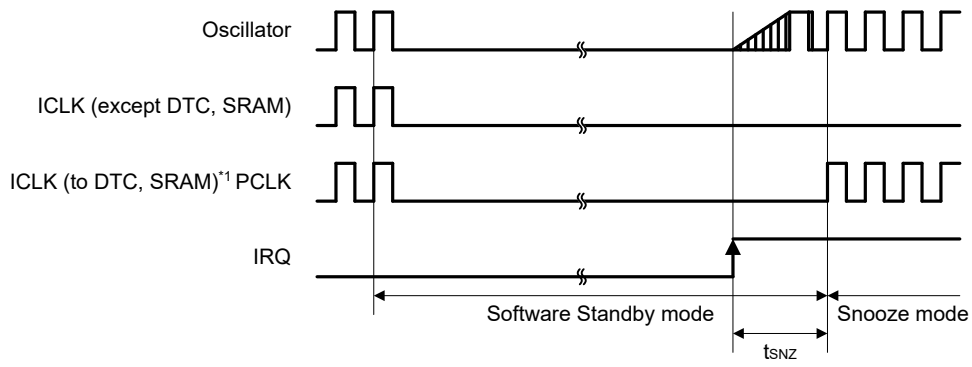


Figure 2.10 Software Standby mode cancellation timing

Table 2.25 Timing of recovery from low power modes (5)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	6.6	8.1	µs	Figure 2.11
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	6.7	8.2	µs	
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	10.8	12.9	µs	
	Low-speed mode System clock source is MOCO (1 MHz)	t_{SNZ}	—	9.2	16	µs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.11 Recovery time from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.26 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

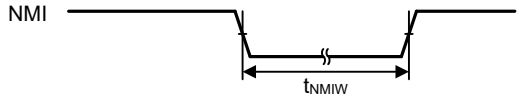


Figure 2.12 NMI interrupt input timing

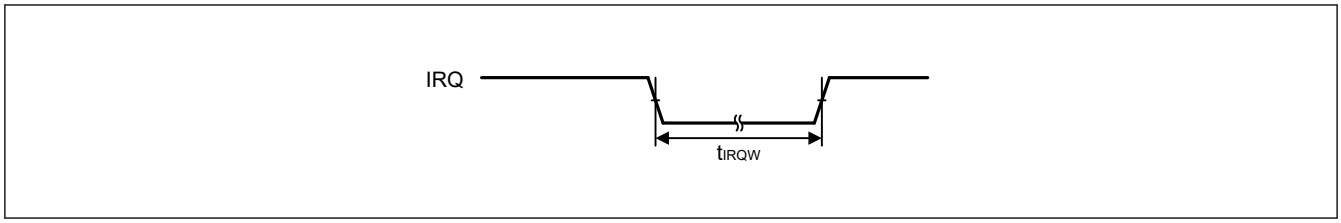


Figure 2.13 IRQ interrupt input timing

2.3.6 I/O Ports, KINT and ADC12 Trigger Timing

Table 2.27 I/O Ports, KINT and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit*1	Test conditions
I/O Ports	Input data pulse width	1.6 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.14
KINT	KRn (n = 00 to 05) pulse width		t_{KR}	250	—	ns	Figure 2.15

Note: If the clock source is being switched, add 4 clock cycles to the switched source.
Note 1. t_{Pcyc}: PCLKB cycle

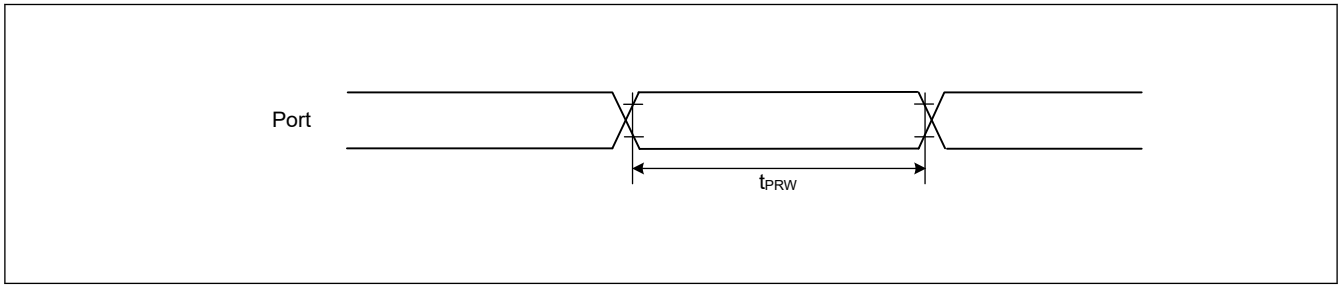


Figure 2.14 I/O ports input timing

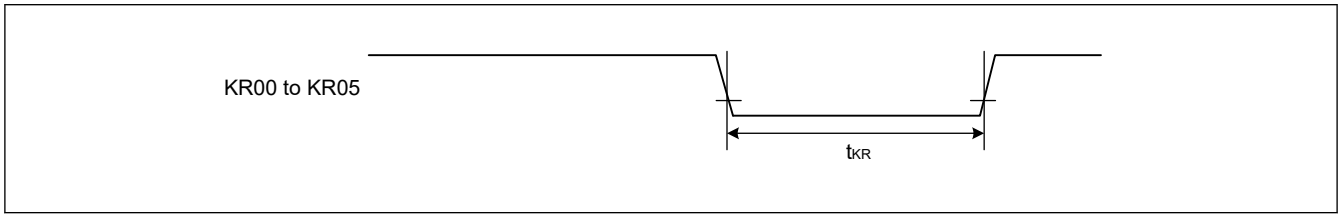


Figure 2.15 KINT input timing

2.3.7 TAU Timing

Table 2.28 TAU timing

Conditions: Ta = -40 to +125°C, VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
TI00 to TI07 input high-level width			t_{TIH}	$1/f_{MCK}$ + 10	—	—	ns	Figure 2.16
TI00 to TI07 input low-level width			t_{TIL}		—	—		
TO00 to TO07 output frequency	High-speed mode	2.7 V ≤ VCC ≤ 5.5 V	f_{TO}	—	—	24	MHz	
		2.4 V ≤ VCC ≤ 2.7 V		—	—	12		
		1.8 V ≤ VCC ≤ 2.4 V		—	—	6		
	Middle-speed mode	2.7 V ≤ VCC ≤ 5.5 V		—	—	24		
		2.4 V ≤ VCC ≤ 2.7 V		—	—	12		
		1.8 V ≤ VCC ≤ 2.4 V		—	—	6		
		1.6 V ≤ VCC ≤ 1.8 V		—	—	2		
	Low-speed mode	1.6 V ≤ VCC ≤ 5.5 V		—	—	1		

Note: f_{MCK}: Timer array unit operating clock frequency.

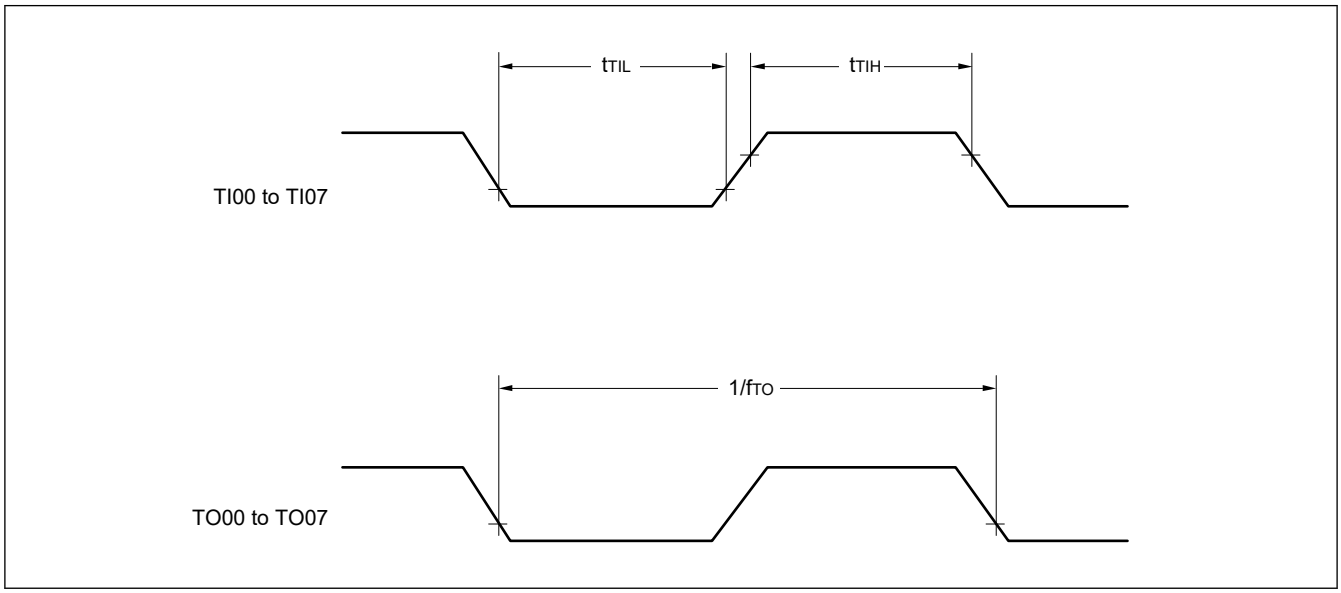


Figure 2.16 TAU input/output timing

2.3.8 CAC Timing

Table 2.29 CAC timing

Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{CAC}: CAC count clock source cycle.

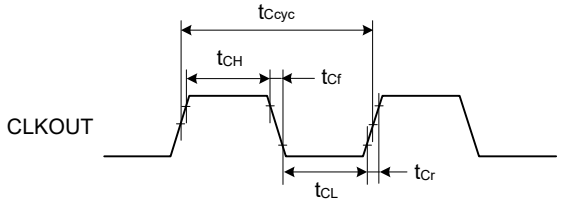
2.3.9 CLKOUT Timing

Table 2.30 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle*1	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.17
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT pin high pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin low pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

Note 1. When the EXTAL external clock input is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, specifications in Table 2.30 should be satisfied with 45% to 55% of input duty cycle.

Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.17 CLKOUT output timing

2.3.10 Serial Array Unit (SAU)

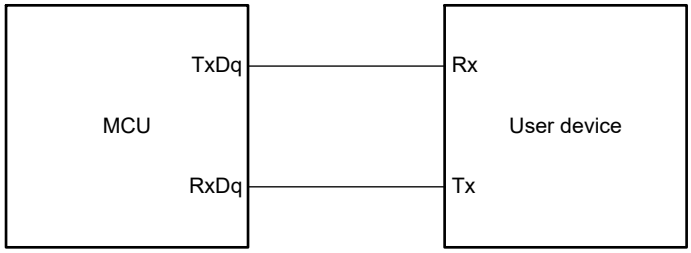
Table 2.31 UART communication

Conditions: T_a = -40 to +125°C, VCC = 1.6 to 5.5 V, VSS = 0 V

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate*1	1.6 V ≤ VCC ≤ 5.5 V		—	—	f_{MCK}/6	—	f_{MCK}/6	—	f_{MCK}/6	bps	Figure 2.18 Figure 2.19
		Theoretical value of the maximum transfer rate f_{MCK} = PCLKB*2		—	5.3	—	4	—	0.16	Mbps	

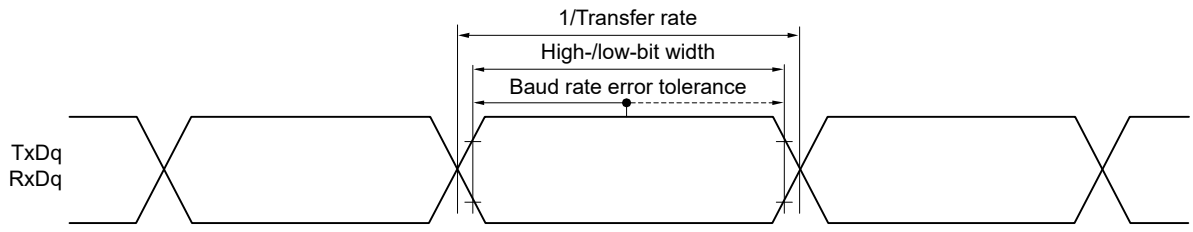
Note: Select the CMOS output for the TxDq pin by using NCODR bit in Port gh Pin Function Select Register (PghPFS).
Note:
- q: UART number (q = 0 to 2), gh: Port number (g = 0 to 4, h = 00 to 15)
- f_{MCK}: Serial array unit operation clock frequency

Note 1. The transfer rate in the Snooze mode is within the range from 4800 to 9600 bps.
Note 2. The maximum operating frequencies of PCLKB are as follows:
High-speed mode: 32 MHz (1.8 V ≤ VCC ≤ 5.5 V)
Middle-speed mode: 24 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Low-speed mode: 1 MHz (1.6 V ≤ VCC ≤ 5.5 V)



Note: q: UART number (q = 0 to 2)

Figure 2.18 Connection in the UART communications



Note: q: UART number (q = 0 to 2)

Figure 2.19 Bit width in the UART communications

Table 2.32 Simplified SPI communication in master mode (only for SPI00)

Conditions: T_a = -40 to +125°C, VCC = 2.7 to 5.5 V, VSS = 0 V

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 2/ PCLKB	4.0 V ≤ VCC ≤ 5.5 V	t_{KCY1}	62.5	—	83.3	—	1000	—	ns	Figure 2.21 Figure 2.22
		2.7 V ≤ VCC ≤ 5.5 V		83.3	—	125	—	1000	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	t_{KCY1}/2 - 7	—	t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY}1/2 - 10	—	t_{KCY1}/2 - 15	—	t_{KCY1}/2 - 50	—	ns	
SIp setup time (to SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	23	—	33	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			33	—	50	—	110	—	ns	
SIp hold time (from SCKp↑)*1	2.7 V ≤ VCC ≤ 5.5 V		t_{KSI1}	10	—	10	—	10	—	ns	
Delay time from SCKp↓ to SOp output*2	C = 20 pF*3		t_{KSO1}	—	10	—	10	—	10	ns	

Note: Select the CMOS output for the SOp pin and SCKp pin by using NCODR bit in Port gh Pin Function Select Register (PghPFS).
Note: p: SPI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), gh: Port number (g = 0 to 4, h = 00 to 15).
Note 1. The setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time changes to SCKp↓ and that for the SIp hold time changes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.
Note 2. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output changes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.
Note 3. C is the load capacitance of the SCKp and SOp output lines.

Table 2.33 Simplified SPI communication in master mode (except for SPI00)

Conditions: T_a = -40 to +125°C, VCC = 1.6 to 5.5 V, VSS = 0 V

Parameter			Symbol	High-speed mode*1		Middle-speed mode		Low-speed mode		Unit	Test conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 4/ PCLKB	2.7 V ≤ VCC ≤ 5.5 V	t_{KCY1}	125	—	166	—	2000	—	ns	Figure 2.21 Figure 2.22
		2.4 V ≤ VCC ≤ 5.5 V		250	—	250	—	2000	—	ns	
		1.8 V ≤ VCC ≤ 5.5 V		500	—	500	—	2000	—	ns	
		1.6 V ≤ VCC ≤ 5.5 V		—	—	1000	—	2000	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	t_{KCY1}/2 - 12	—	t_{KCY1}/2 - 21	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 18	—	t_{KCY1}/2 - 25	—	t_{KCY1}/2 - 50	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 38	—	t_{KCY1}/2 - 38	—	t_{KCY1}/2 - 50	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			—	—	t_{KCY1}/2 - 100	—	t_{KCY1}/2 - 100	—	ns	
SIp setup time (to SCKp↑)*2	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	44	—	54	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			44	—	54	—	110	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			75	—	75	—	110	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			110	—	110	—	110	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			—	—	220	—	220	—	ns	
SIp hold time (from SCKp↑)*2	1.6 V ≤ VCC ≤ 5.5 V		t_{KSI1}	19	—	19	—	19	—	ns	
Delay time from SCKp↓ to SOp output*3	1.6 V ≤ VCC ≤ 5.5 V C = 30 pF*4		t_{KSO1}	—	25	—	25	—	25	ns	

Note: Select the CMOS output for the SOp pin and SCKp pin by using NCODR bit in Port gh Pin Function Select Register (PghPFS).

Note: p: SPI number (p = 00, 01, 10, 11, 20, 21), m: Unit number, n: Channel number (mn = 00 to 03, 10 to 11), gh: Port number (g = 0 to 4, h = 00 to 15).

Note 1. Operating voltages in high-speed mode are 1.8 V ≤ VCC ≤ 5.5 V.

Note 2. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time changes to SCKp↓ and that for the SIp hold time changes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 3. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output changes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Table 2.34 Simplified SPI communication in slave mode

Conditions: T_a = -40 to +125°C, VCC = 1.6 to 5.5 V, VSS = 0 V

Parameter			Symbol	High-speed mode*1		Middle-speed mode		Low-speed mode		Unit	Test conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time*2	4.0 V ≤ VCC ≤ 5.5 V	20 MHz < f_{MCK}	t_{KCY2}	8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	Figure 2.21 Figure 2.22
		f_{MCK} ≤ 20 MHz		6/f_{MCK}	—	6/f_{MCK}	—	6/f_{MCK}	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V	16 MHz < f_{MCK}		8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 16 MHz		6/f_{MCK}	—	6/f_{MCK}	—	6/f_{MCK}	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			6/f_{MCK} + 500	—	6/f_{MCK} + 500	—	6/f_{MCK} + 500	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			6/f_{MCK} + 750	—	6/f_{MCK} + 750	—	6/f_{MCK} + 750	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			—	—	6/f_{MCK} + 1500	—	6/f_{MCK} + 1500	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH2}, t_{KL2}	t_{KCY2}/2 - 7	—	t_{KCY2}/2 - 7	—	t_{KCY2}/2 - 7	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY2}/2 - 8	—	t_{KCY2}/2 - 8	—	t_{KCY2}/2 - 8	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 18	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			—	—	t_{KCY2}/2 - 66	—	t_{KCY2}/2 - 66	—	ns	
SIp setup time (to SCKp↑)*3	2.7 V ≤ VCC ≤ 5.5 V		t_{SIK2}	1/f_{MCK} + 20	—	1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			—	—	1/f_{MCK} + 40	—	1/f_{MCK} + 40	—	ns	
SIp hold time (from SCKp↑)*3	1.8 V ≤ VCC ≤ 5.5 V		t_{KSI2}	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			—	—	1/f_{MCK} + 250	—	1/f_{MCK} + 250	—	ns	
Delay time from SCKp↓ to SOp output*4	C = 30 pF*5	2.7 V ≤ VCC ≤ 5.5 V	t_{KSO2}	—	2/f_{MCK} + 44	—	2/f_{MCK} + 110	—	2/f_{MCK} + 110	ns	
		2.4 V ≤ VCC ≤ 5.5 V		—	2/f_{MCK} + 75	—	2/f_{MCK} + 110	—	2/f_{MCK} + 110	ns	
		1.8 V ≤ VCC ≤ 5.5 V		—	2/f_{MCK} + 110	—	2/f_{MCK} + 110	—	2/f_{MCK} + 110	ns	
		1.6 V ≤ VCC ≤ 5.5 V		—	—	—	2/f_{MCK} + 220	—	2/f_{MCK} + 220	ns	

Note: Select the CMOS output for the SOp pin by using NCODR bit in Port gh Pin Function Select Register (PghPFS).

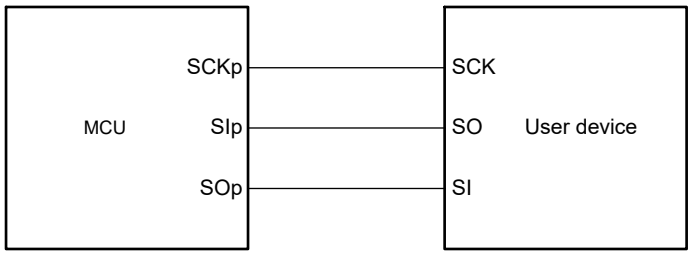
Note:
- p: SPI number (p = 00, 01, 10, 11, 20, 21), m: Unit number, n: Channel number (mn = 00 to 03, 10 to 11), gh: Port number (g = 0 to 4, h = 00 to 15)
- f_{MCK}: Serial array unit operation clock frequency

Note 1. Operating voltages in high-speed mode are 1.8 V ≤ VCC ≤ 5.5 V.

Note 2. Transfer rate in the Snooze mode is 0.5 Mbps at the maximum.

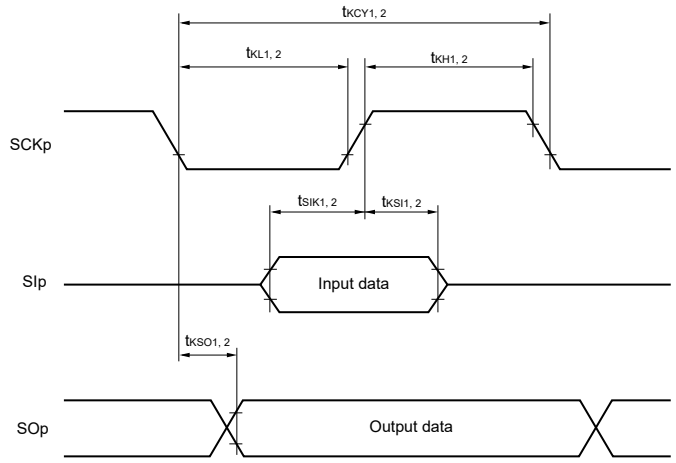
Note 3. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time changes to SCKp↓ and that for the SIp hold time changes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 4. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output changes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.
Note 5. C is the load capacitance of the SOp output line.



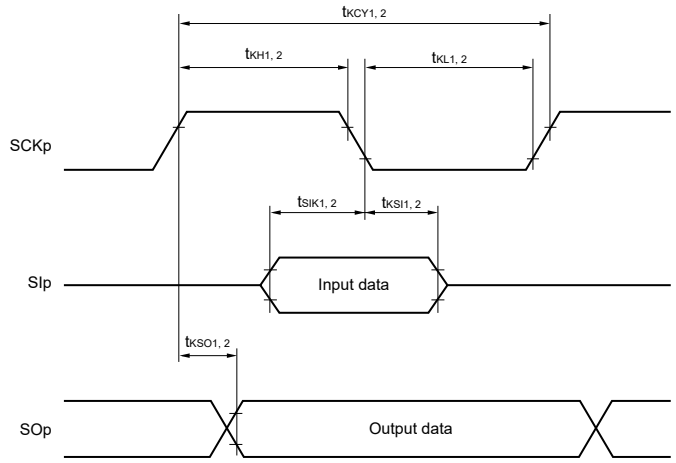
Note: p: SPI number (p = 00, 01, 10, 11, 20, 21)

Figure 2.20 Connection in the simplified SPI communications



Note:
- p: SPI number (p = 00, 01, 10, 11, 20, 21)
- m: Unit number, n: Channel number (mn = 00 to 03, 10 to 11)

Figure 2.21 Timing of serial transfer in the simplified SPI communications when SCRmn.DCP[1:0] = 00b or 11b



Note:
- p: SPI number (p = 00, 01, 10, 11, 20, 21)
- m: Unit number, n: Channel number (mn = 00 to 03, 10 to 11)

Figure 2.22 Timing of serial transfer in the simplified SPI communications when SCRmn.DCP[1:0] = 01b or 10b

Table 2.35 Simplified I²C communication

Conditions: T_a = -40 to +125°C, VCC = 1.6 to 5.5 V, VSS = 0 V

Parameter		Symbol	High-speed mode*1		Middle-speed mode		Low-speed mode		Unit	Test conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SCLr clock frequency	2.7 V ≤ VCC ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	f_{SCL}	—	1000*2	—	1000*2	—	400*2	kHz	Figure 2.23 Figure 2.24
	1.8 V ≤ VCC ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		—	400*2	—	400*2	—	400*2	kHz	
	1.8 V ≤ VCC < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		—	300*2	—	300*2	—	300*2	kHz	
	1.6 V ≤ VCC < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—	—	—	250*2	—	250*2	kHz	
Hold time when SCLr is low	2.7 V ≤ VCC ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	t_{LOW}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—	—	1850	—	1850	—	ns	
Hold time when SCLr is high	2.7 V ≤ VCC ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	t_{HIGH}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—	—	1850	—	1850	—	ns	
Data setup time (reception)	2.7 V ≤ VCC ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	$t_{SU:DAT}$	$1/f_{MCK}$ + 85*3	—	$1/f_{MCK}$ +85*3	—	$1/f_{MCK}$ +145*3	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		$1/f_{MCK}$ + 145*3	—	$1/f_{MCK}$ + 145*3	—	$1/f_{MCK}$ +145*3	—	ns	
	1.8 V ≤ VCC < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		$1/f_{MCK}$ + 230*3	—	$1/f_{MCK}$ + 230*3	—	$1/f_{MCK}$ + 230*3	—	ns	
	1.6 V ≤ VCC < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—	—	$1/f_{MCK}$ + 290*3	—	$1/f_{MCK}$ + 290*3	—	ns	
Data hold time (transmission)	2.7 V ≤ VCC ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	1.8 V ≤ VCC ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		0	405	0	405	0	405	ns	
	1.6 V ≤ VCC < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—	—	0	405	0	405	ns	

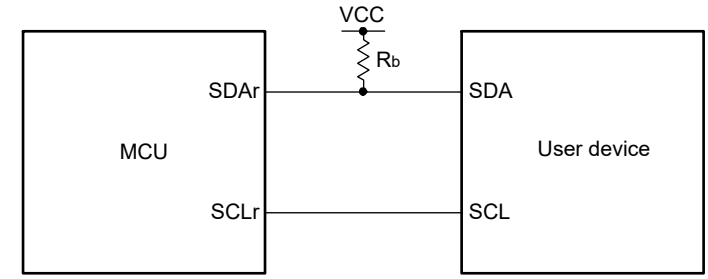
Note: Select the NMOS open-drain output for the SDAr pin and the CMOS output for the SCLr pin by using NCODR bit in Port gh Pin Function Select Register (PghPFS).

Note:
- r: IIC number (r = 00, 01, 10, 11, 20, 21), gh: Port number (g = 0 to 4, h = 00 to 15)
- f_{MCK}: Serial array unit operation clock frequency
- Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

Note 1. Operating voltages in high-speed mode are 1.8 V ≤ VCC ≤ 5.5 V.

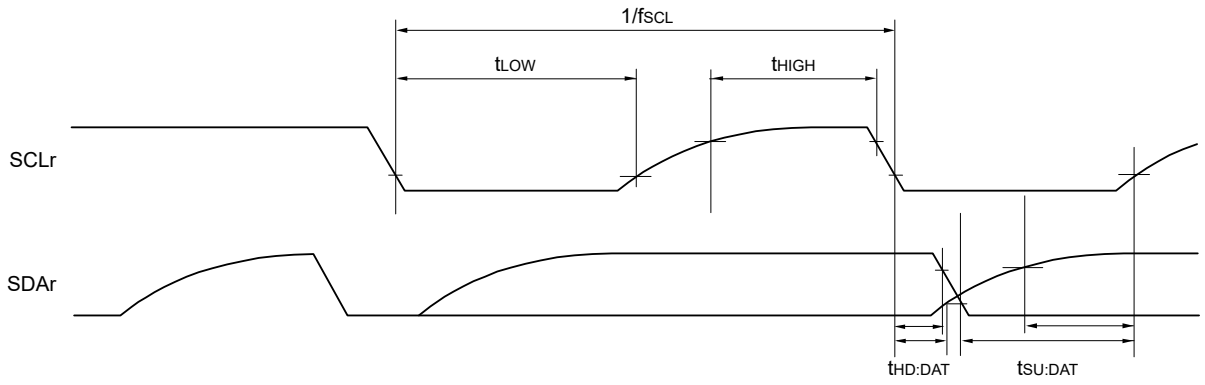
Note 2. The listed times must be no greater than $f_{MCK}/4$.

Note 3. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.



Note: r: IIC number (r = 00, 01, 10, 11, 20, 21)

Figure 2.23 Connection in the simplified I²C communications



Note: r: IIC number (r = 00, 01, 10, 11, 20, 21)

Figure 2.24 Timing of serial transfer in the simplified I²C communications

2.3.11 Serial Interface UARTA (UARTA)

Table 2.36 UARTA communications

Conditions: T_a = -40 to +125°C, VCC = 1.6 to 5.5 V, VSS = 0 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Transfer rate	—	200	—	153600	bps	—

Note: Select the CMOS output for the TxDAn pin by using NCODR bit in Port gh Pin Function Select Register (PghPFS).
Note: n: Unit number (n = 0, 1), gh: Port number (g = 0 to 4, h = 00 to 15).

2.3.12 I²C Bus Interface (IICA)

Table 2.37 I²C standard mode

Conditions: T_a = -40 to +125°C, VCC = 1.6 to 5.5 V, VSS = 0 V

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Standard mode: PCLKB ≥ 1 MHz	f_{SCL}	0	—	100	kHz	Figure 2.25
Setup time of restart condition	—	$t_{SU:STA}$	4.7	—	—	µs	
Hold time*1	—	$t_{HD:STA}$	4	—	—	µs	
Hold time when SCLAn is low	—	t_{LOW}	4.7	—	—	µs	
Hold time when SCLAn is high	—	t_{HIGH}	4	—	—	µs	
Data setup time (reception)	—	$t_{SU:DAT}$	250	—	—	ns	
Data hold time (transmission)*2	—	$t_{HD:DAT}$	0	—	3.45	µs	
Setup time of stop condition	—	$t_{SU:STO}$	4	—	—	µs	
Bus-free time	—	t_{BUF}	4.7	—	—	µs	

Note: n = 0, 1
Note: The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
Cb = 400 pF, Rb = 2.7 kΩ
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

Table 2.38 I²C fast mode

Conditions: T_a = -40 to +125°C, VCC = 1.8 to 5.5 V, VSS = 0 V

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Fast mode: PCLKB ≥ 3.5 MHz	f_{SCL}	0	—	400	kHz	Figure 2.25
Setup time of restart condition	—	$t_{SU:STA}$	0.6	—	—	µs	
Hold time*1	—	$t_{HD:STA}$	0.6	—	—	µs	
Hold time when SCLAn is low	—	t_{LOW}	1.3	—	—	µs	
Hold time when SCLAn is high	—	t_{HIGH}	0.6	—	—	µs	
Data setup time (reception)	—	$t_{SU:DAT}$	100	—	—	ns	
Data hold time (transmission)*2	—	$t_{HD:DAT}$	0	—	0.9	µs	
Setup time of stop condition	—	$t_{SU:STO}$	0.6	—	—	µs	
Bus-free time	—	t_{BUF}	1.3	—	—	µs	

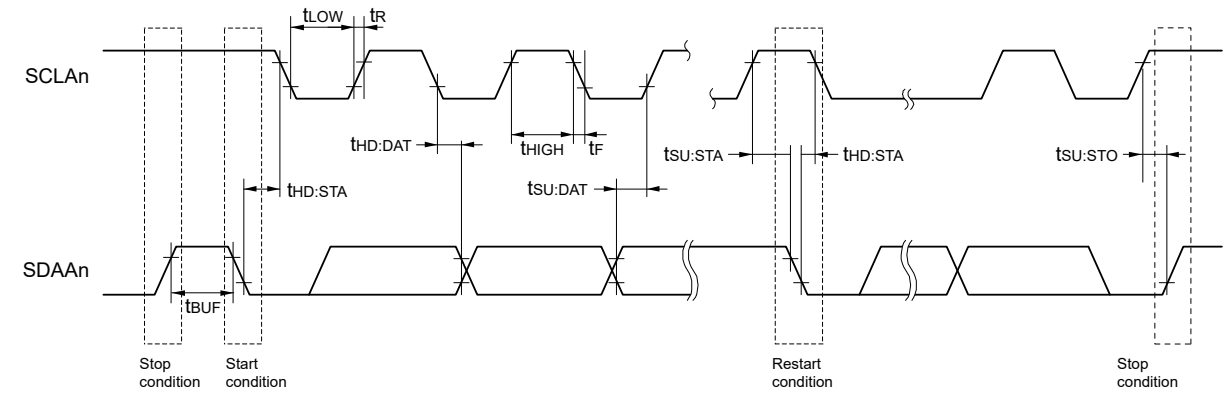
Note: n = 0, 1
Note: The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
Cb = 320 pF, Rb = 1.1 kΩ
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

Table 2.39 I^2C fast mode plus

Conditions: T_a = -40 to +125°C, VCC = 2.7 to 5.5 V, VSS = 0 V

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Fast mode plus: PCLKB ≥ 10 MHz	f_{SCL}	0	—	1000	kHz	Figure 2.25
Setup time of restart condition	—	$t_{SU:STA}$	0.26	—	—	µs	
Hold time*1	—	$t_{HD:STA}$	0.26	—	—	µs	
Hold time when SCLAn is low	—	t_{LOW}	0.5	—	—	µs	
Hold time when SCLAn is high	—	t_{HIGH}	0.26	—	—	µs	
Data setup time (reception)	—	$t_{SU:DAT}$	50	—	—	ns	
Data hold time (transmission)*2	—	$t_{HD:DAT}$	0	—	0.45	µs	
Setup time of stop condition	—	$t_{SU:STO}$	0.26	—	—	µs	
Bus-free time	—	t_{BUF}	0.5	—	—	µs	

Note: n = 0, 1
Note: The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
Cb = 120 pF, Rb = 1.1 kΩ
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.



Note: n = 0, 1

Figure 2.25 I^2C serial transfer timing

2.4 ADC12 Characteristics

Table 2.40 A/D conversion characteristics (1) in normal modes 1 and 2 (1 of 2)

Conditions: VCC = AVREFP = 4.5 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversion: ANI2 to ANI5, internal reference voltage, and temperature sensor output voltage

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bit	—
Conversion clock (fAD)	1	—	48	MHz	—
Conversion time*4	1.33	—	—	µs	—
Offset error*1 *2 *3	—	—	±7.0	LSB	—
Full-scale error*1 *2 *3	—	—	±7.0	LSB	—
Absolute accuracy*1 *2 *3	—	—	±7.5	LSB	—

Table 2.40 A/D conversion characteristics (1) in normal modes 1 and 2 (2 of 2)

Conditions: VCC = AVREFP = 4.5 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversion: ANI2 to ANI5, internal reference voltage, and temperature sensor output voltage

Parameter	Min	Typ	Max	Unit	Test conditions
DNL differential nonlinearity error*1	—	±1.0	—	LSB	—
INL integral nonlinearity error*1 *3 *3	—	—	±3.0	LSB	—
Analog input voltage range	0	—	AVREFP	V	—

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).
Note 2. When pins ANI16 to ANI19 are selected as the target pins for conversion, the maximum values are as follows:
Absolute accuracy: Add ± 3 LSB to the maximum value.
Offset/full-scale error: Add ± 2 LSB to the maximum value.
Note 3. When AVREFP < VCC, the maximum values are as follows:
Absolute accuracy/Offset error/full-scale error: Add (± 0.75 LSB × (VCC voltage (V) - AVREFP voltage (V)) to the maximum value.
INL integral nonlinearity error: Add (± 0.2 LSB × (VDD voltage (V) - AVREFP voltage (V)) to the maximum value.
Note 4. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use normal mode 2 and fAD = 32 MHz or less with the longer sampling time.

Table 2.41 A/D conversion characteristics (2) in normal modes 1 and 2

Conditions: VCC = AVREFP = 2.7 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversions: ANI2 to ANI5, internal reference voltage, and temperature sensor output voltage

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bit	—
Conversion clock (fAD)	1	—	48	MHz	—
Conversion time*4	1.33	—	—	µs	—
Offset error*1 *2 *3	—	—	±8.5	LSB	—
Full-scale error *1 *2 *3	—	—	±8.5	LSB	—
Absolute accuracy*1 *2 *3	—	—	±9.0	LSB	—
DNL differential nonlinearity error*1	—	±1.0	—	LSB	—
INL integral nonlinearity error*1 *3	—	—	±3.0	LSB	—
Analog input voltage range	0	—	AVREFP	V	—

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).
Note 2. When pins ANI16 to ANI19 are selected as the target pins for conversion, the maximum values are as follows:
Absolute accuracy: Add ± 3 LSB to the maximum value.
Offset/full-scale error: Add ± 2 LSB to the maximum value.
Note 3. When AVREFP < VCC, the maximum values are as follows:
Absolute accuracy/Offset error/full-scale error: Add (± 0.75 LSB × (VCC voltage (V) - AVREFP voltage (V)) to the maximum value.
INL integral nonlinearity error: Add (± 0.2 LSB × (VDD voltage (V) - AVREFP voltage (V)) to the maximum value.
Note 4. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use normal mode 2 and fAD = 32 MHz or less with the longer sampling time.

Table 2.42 A/D conversion characteristics (3) in normal modes 1 and 2 (1 of 2)

Conditions: VCC = AVREFP = 2.4 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversions: ANI2 to ANI5, internal reference voltage, and temperature sensor output voltage

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bit	—
Conversion clock (PCLKB)	1	—	32	MHz	—

Table 2.42 A/D conversion characteristics (3) in normal modes 1 and 2 (2 of 2)

Conditions: VCC = AVREFP = 2.4 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversions: ANI2 to ANI5, internal reference voltage, and temperature sensor output voltage

Parameter	Min	Typ	Max	Unit	Test conditions
Conversion time*4	2.0	—	—	µs	—
Offset error*1 *2 *3	—	—	±9.0	LSB	—
Full-scale error *1 *2 *3	—	—	±9.0	LSB	—
Absolute accuracy*1 *2 *3	—	—	±9.5	LSB	—
DNL differential nonlinearity error*1	—	±1.0	—	LSB	—
INL integral nonlinearity error*1 *3	—	—	±3.0	LSB	—
Analog input voltage range	0	—	AVREFP	V	—

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).
Note 2. When pins ANI16 to ANI19 are selected as the target pins for conversion, the maximum values are as follows:
Absolute accuracy: Add ± 3 LSB to the maximum value.
Offset/full-scale error: Add ± 2 LSB to the maximum value.
Note 3. When AVREFP < VCC, the maximum values are as follows:
Absolute accuracy/Offset error/full-scale error: Add (± 0.75 LSB × (VCC voltage (V) - AVREFP voltage (V)) to the maximum value.
INL integral nonlinearity error: Add (± 0.2 LSB × (VDD voltage (V) - AVREFP voltage (V)) to the maximum value.
Note 4. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use normal mode 2 and fAD = 32 MHz or less with the longer sampling time.

Table 2.43 A/D conversion characteristics (1) in Low-voltage modes 1 and 2

Conditions: VCC = AVREFP = 2.7 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversion: ANI2 to ANI5, internal reference voltage*4, and temperature sensor output voltage*4

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bit	—
Conversion clock (fAD)	1	—	24	MHz	—
Conversion time*5	3.33	—	—	µs	—
Offset error*1 *2 *3	—	—	±8.5	LSB	—
Full-scale error *1 *2 *3	—	—	±8.5	LSB	—
Absolute accuracy*1 *2 *3	—	—	±9.0	LSB	—
DNL differential nonlinearity error*1	—	±1.5	—	LSB	—
INL integral nonlinearity error*1 *3	—	—	±4.0	LSB	—
Analog input voltage range	0	—	AVREFP	V	—

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).
Note 2. When pins ANI16 to ANI19 are selected as the target pins for conversion, the maximum values are as follows:
Absolute accuracy: Add ± 3 LSB to the maximum value.
Offset/full-scale error: Add ± 2 LSB to the maximum value.
Note 3. When AVREFP < VCC, the maximum values are as follows:
Absolute accuracy/Offset error/full-scale error: Add (± 0.75 LSB × (VCC voltage (V) - AVREFP voltage (V)) to the maximum value.
INL integral nonlinearity error: Add (± 0.2 LSB × (VDD voltage (V) - AVREFP voltage (V)) to the maximum value.
Note 4. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.
Note 5. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use a low-voltage mode 2 and fAD = 16 MHz or less with the longer sampling time.

Table 2.44 A/D conversion characteristics (2) in Low-voltage modes 1 and 2

Conditions: VCC = AVREFP = 2.4 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversions: ANI2 to ANI5, internal reference voltage*4, and temperature sensor output voltage*4

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bit	—
Conversion clock (fAD)	1	—	16	MHz	—
Conversion time*5	5.0	—	—	µs	—
Offset error*1 *2 *3	—	—	±9.0	LSB	—
Full-scale error*1 *2 *3	—	—	±9.0	LSB	—
Absolute accuracy*1 *2 *3	—	—	±9.5	LSB	—
DNL differential nonlinearity error*1	—	±1.5	—	LSB	—
INL integral nonlinearity error*1 *3	—	—	±4.0	LSB	—
Analog input voltage range	0	—	AVREFP	V	—

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).
Note 2. When pins ANI16 to ANI19 are selected as the target pins for conversion, the maximum values are as follows:
Absolute accuracy: Add ± 3 LSB to the maximum value.
Offset/full-scale error: Add ± 2 LSB to the maximum value.
Note 3. When AVREFP < VCC, the maximum values are as follows:
Absolute accuracy/Offset error/full-scale error: Add (± 0.75 LSB × (VCC voltage (V) - AVREFP voltage (V)) to the maximum value.
INL integral nonlinearity error: Add (± 0.2 LSB × (VDD voltage (V) - AVREFP voltage (V)) to the maximum value.
Note 4. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.
Note 5. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use low-voltage mode 2 and fAD = 16 MHz or less with the longer sampling time.

Table 2.45 A/D conversion characteristics (3) in Low-voltage modes 1 and 2

Conditions: VCC = AVREFP = 1.8 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversion: ANI2 to ANI5, internal reference voltage*4, and temperature sensor output voltage*4

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bit	—
Conversion clock (fAD)	1	—	8	MHz	—
Conversion time*5	10.0	—	—	µs	—
Offset error*1 *2 *3	—	—	± 13.0	LSB	—
Full-scale error*1 *2 *3	—	—	± 13.0	LSB	—
Absolute accuracy*1 *2 *3	—	—	± 13.5	LSB	—
DNL differential nonlinearity error*1	—	± 2.0	—	LSB	—
INL integral nonlinearity error*1 *3	—	—	± 4.5	LSB	—
Analog input voltage range	0	—	AVREFP	V	—

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).
Note 2. When pins ANI16 to ANI19 are selected as the target pins for conversion, the maximum values are as follows:
Absolute accuracy: Add ± 3 LSB to the maximum value.
Offset/full-scale error: Add ± 2 LSB to the maximum value.
Note 3. When AVREFP < VCC, the maximum values are as follows:
Absolute accuracy/Offset error/full-scale error: Add (± 0.75 LSB × (VCC voltage (V) - AVREFP voltage (V)) to the maximum value.
INL integral nonlinearity error: Add (± 0.2 LSB × (VDD voltage (V) - AVREFP voltage (V)) to the maximum value.
Note 4. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.

Note 5. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use low-voltage mode 2 and fAD = 16 MHz or less with the longer sampling time.

Table 2.46 A/D conversion characteristics (4) in Low-voltage modes 1 and 2

Conditions: VCC = AVREFP = 1.6 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM
Target pins for conversion: ANI2 to ANI5, internal reference voltage*4, and temperature sensor output voltage*4

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bit	—
Conversion clock (PCLKB)	1	—	4	MHz	—
Conversion time*5	20.0	—	—	µs	—
Offset error*1 *2 *3 *4	—	—	±13.5	LSB	—
Full-scale error*1 *2 *3 *4	—	—	±13.5	LSB	—
Absolute accuracy*1 *2 *3 *4	—	—	±14.0	LSB	—
DNL differential nonlinearity error*1	—	±2.0	—	LSB	—
INL integral nonlinearity error*1 *3 *4	—	—	±4.5	LSB	—
Analog input voltage range	0	—	AVREFP	V	—

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).
Note 2. When pins ANI16 to ANI19 are selected as the target pins for conversion, the maximum values are as follows:
Absolute accuracy: Add ± 3 LSB to the maximum value.
Offset/full-scale error: Add ± 2 LSB to the maximum value.
Note 3. When AVREFP < VCC, the maximum values are as follows:
Absolute accuracy/Offset error/full-scale error: Add (± 0.75 LSB × (VCC voltage (V) - AVREFP voltage (V)) to the maximum value.
INL integral nonlinearity error: Add (± 0.2 LSB × (VDD voltage (V) - AVREFP voltage (V)) to the maximum value.
Note 4. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.
Note 5. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use low-voltage mode 2 and fAD = 16 MHz or less with the longer sampling time.

Table 2.47 A/D conversion characteristics in Low-voltage modes 1 and 2 when the internal reference voltage is selected as reference voltage (+)

Conditions: VCC = 1.8 to 5.5 V, VSS = AVREFM = 0 V
Reference voltage (+) = internal reference voltage, Reference voltage (-) = AVREFM

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	8	Bit	—
Conversion clock (fAD)	1	—	2	MHz	—
Offset error*1	—	—	2	LSB	—
DNL differential nonlinearity error*1	—	1	—	LSB	—
INL integral nonlinearity error*1	—	—	2	LSB	—
Analog input voltage range	0	—	VBGR	V	

Note: These specification values apply during A/D conversion operation, while CPU is in Sleep mode and peripheral modules other than A/D in module standby.
If CPU is running or peripheral modules other than A/D are running during A/D conversion, values might not fall within the indicated ranges.
Note 1. This value does not include the quantization error (± 1/2 LSB).

Table 2.48 12-bit A/D converter channel classification (1 of 2)

Classification	Channel	Conditions	Remarks
High-precision channel	ANI0 to ANI5	VCC = 1.6 to 5.5 V	Pins ANI0 to ANI5 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Normal-precision channel	ANI16 to ANI19		—

Table 2.48 12-bit A/D converter channel classification (2 of 2)

Classification	Channel	Conditions	Remarks
Internal reference voltage input channel	Internal reference voltage	VCC = 1.8 to 5.5 V	—
Temperature sensor input channel	Temperature sensor output		—

Table 2.49 A/D internal reference voltage characteristics

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*1	1.40	1.47	1.54	V	—
Sampling time*2	5.0	—	—	µs	—

Note 1. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 2. When the internal reference voltage is converted.

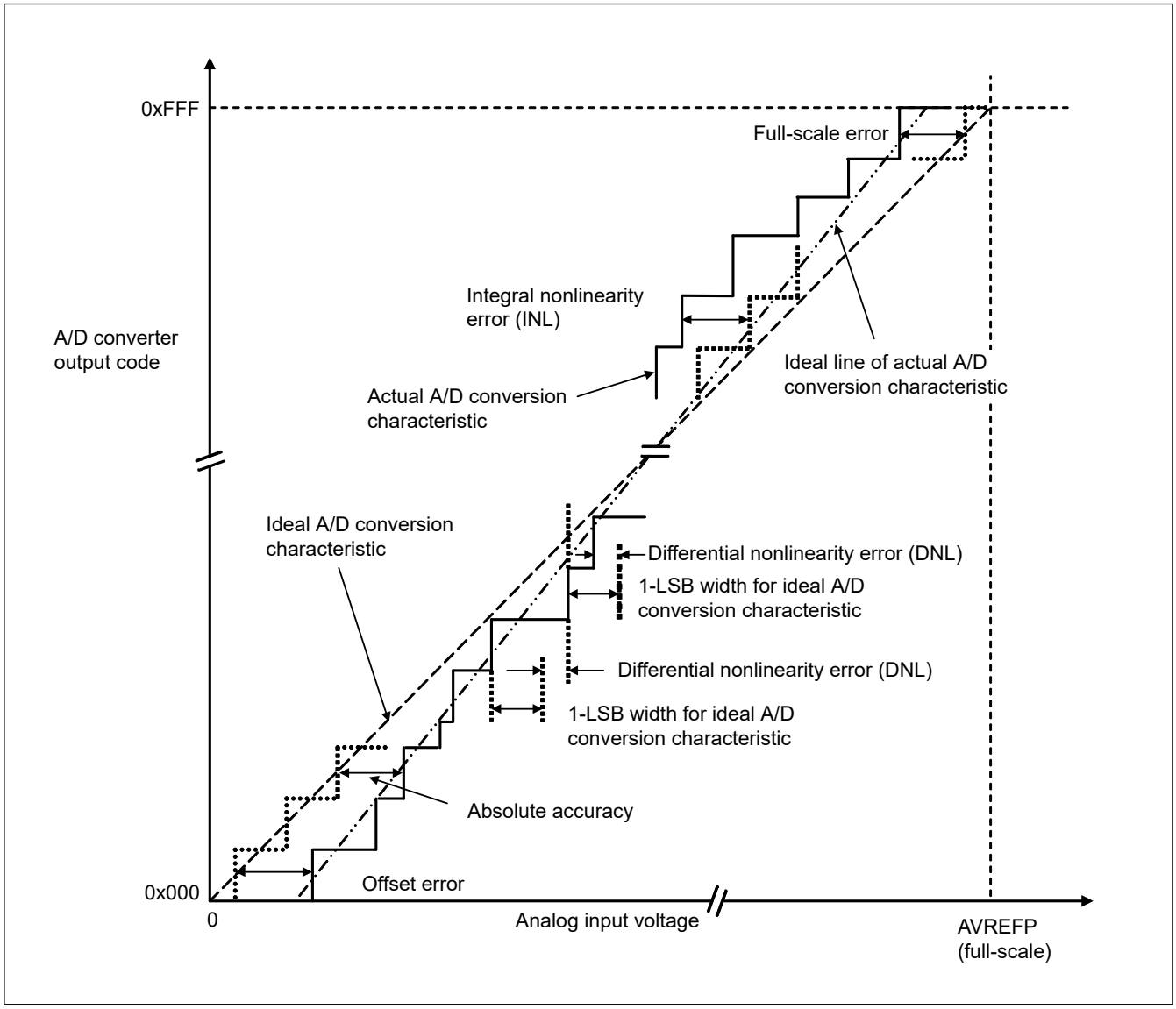


Figure 2.26 Example of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage AVREFP = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 CMP Characteristics

Table 2.50 CMP characteristics

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range		IVREF	0	—	VCC − 1.4	V	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0
			1.4	—	VCC		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1
		IVCMP	−0.3	—	VCC + 0.3		Input to the IVCMP0 and IVCMP1 pins
Output delay	High-speed mode	—	—	—	1.5	µs	VCC = 3.0 V Input slew rate > 1 V/us
	Low-speed mode		—	3.0	—		
Offset voltage	High-speed mode	—	—	—	50	mV	—
	Low-speed mode		—	—	40		
Operation stabilization wait time		t_{CMP}	30	—	—	µs	—
Internal reference voltage*1		—	1.34	1.44	1.54	V	—

Note 1. The internal reference voltage can be selected as CMP reference voltage only when 1.8 V ≤ VCC ≤ 5.5 V.

2.6 DAC8 Characteristics

Table 2.51 D/A conversion characteristics

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	—	8	bit	—
Conversion time	t_{DCONV}	—	—	3.0	µs	—
Absolute accuracy	—	—	—	±3.0	LSB	—
Resistive load	—	4	—	—	MΩ	—
Capacitive load*1	—	—	—	35	pF	—
Output resistance	—	—	9.0	—	kΩ	—

Note 1. Including IO input capacitance of 15 pF.

2.7 TSN Characteristics

Table 2.52 TSN characteristics

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Temperature slope	—	—	−3.3	—	mV/°C	—
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Sampling time	—	5.0	—	—	µs	—

2.8 POR and LVD Characteristics

Table 2.53 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 2.27
		When power supply fall	V_{PDR}	1.46	1.50	1.54		Figure 2.28
	Voltage detection circuit (LVD0)*2	When power supply rise	V_{det0_0}	3.74	3.91	4.06	V	Figure 2.29 At falling edge VCC
		When power supply fall		3.68	3.85	4.00		
		When power supply rise	V_{det0_1}	2.73	2.9	3.01		
		When power supply fall		2.68	2.85	2.96		
		When power supply rise	V_{det0_2}	2.44	2.59	2.70		
		When power supply fall		2.38	2.53	2.64		
		When power supply rise	V_{det0_3}	1.83	1.95	2.07		
		When power supply fall		1.78	1.90	2.02		
		When power supply rise	V_{det0_4}	1.66	1.75	1.88		
		When power supply fall		1.60	1.69	1.82		

Table 2.53 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_0}	4.23	4.39	4.55	V	Figure 2.30 At falling edge VCC
		When power supply fall		4.13	4.29	4.45		
		When power supply rise	V_{det1_1}	4.07	4.25	4.39		
		When power supply fall		3.98	4.16	4.30		
		When power supply rise	V_{det1_2}	3.97	4.14	4.29		
		When power supply fall		3.86	4.03	4.18		
		When power supply rise	V_{det1_3}	3.74	3.92	4.06		
		When power supply fall		3.68	3.86	4.00		
		When power supply rise	V_{det1_4}	3.05	3.17	3.29		
		When power supply fall		2.98	3.10	3.22		
		When power supply rise	V_{det1_5}	2.95	3.06	3.17		
		When power supply fall		2.89	3.00	3.11		
		When power supply rise	V_{det1_6}	2.86	2.97	3.08		
		When power supply fall		2.79	2.90	3.01		
		When power supply rise	V_{det1_7}	2.74	2.85	2.96		
		When power supply fall		2.68	2.79	2.90		
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_8}	2.63	2.75	2.85	V	Figure 2.30 At falling edge VCC
		When power supply fall		2.58	2.68	2.78		
		When power supply rise	V_{det1_9}	2.54	2.64	2.75		
		When power supply fall		2.48	2.58	2.68		
		When power supply rise	V_{det1_A}	2.43	2.53	2.63		
		When power supply fall		2.38	2.48	2.58		
		When power supply rise	V_{det1_B}	2.16	2.26	2.36		
		When power supply fall		2.10	2.20	2.30		
		When power supply rise	V_{det1_C}	1.88	2	2.09		
		When power supply fall		1.84	1.96	2.05		
		When power supply rise	V_{det1_D}	1.78	1.9	1.99		
		When power supply fall		1.74	1.86	1.95		
		When power supply rise	V_{det1_E}	1.67	1.79	1.88		
		When power supply fall		1.63	1.75	1.84		
		When power supply rise	V_{det1_F}	1.65	1.7	1.78		
		When power supply fall		1.60	1.65	1.73		
Voltage detection level*1	Voltage detection circuit (LVD2)*4	When power supply rise	V_{det2_0}	4.20	4.40	4.57	V	Figure 2.31 At falling edge VCC
		When power supply fall		4.11	4.31	4.48		
		When power supply rise	V_{det2_1}	4.05	4.25	4.42		
		When power supply fall		3.97	4.17	4.34		
		When power supply rise	V_{det2_2}	3.91	4.11	4.28		
		When power supply fall		3.83	4.03	4.20		
		When power supply rise	V_{det2_3}	3.71	3.91	4.08		
		When power supply fall		3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL0[2:0] bits.

Note 3. # in the symbol $V_{det1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol $V_{det2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.54 Power-on reset circuit and voltage detection circuit characteristics (2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.27, Figure 2.28
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.29
LVD1 response delay time*3		t_{det}	—	—	350	µs	Figure 2.30
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.31
Minimum VCC down time		t_{VOFF}	500	—	—	µs	Figure 2.27, VCC = 1.0 V or above
Power-on reset enable time		$t_{W\ (POR)}$	1	—	—	ms	Figure 2.28, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD1 is enabled)		$T_{d\ (E-A)}$	—	—	300	µs	Figure 2.30
LVD2 operation stabilization time (after LVD2 is enabled)		$T_{d\ (E-A)}$	—	—	1200	µs	Figure 2.31
Hysteresis width (POR)		V_{PORH}	—	10	—	mV	—
Hysteresis width (LVD0, LVD1 and LVD2)		V_{LVH}	—	60	—	mV	LVD0 selected
			—	110	—		V_{det1_0} to V_{det1_2} selected
			—	70	—		V_{det1_3} to V_{det1_9} selected
			—	60	—		V_{det1_A} to V_{det1_B} selected
			—	50	—		V_{det1_C} to V_{det1_F} selected
			—	90	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

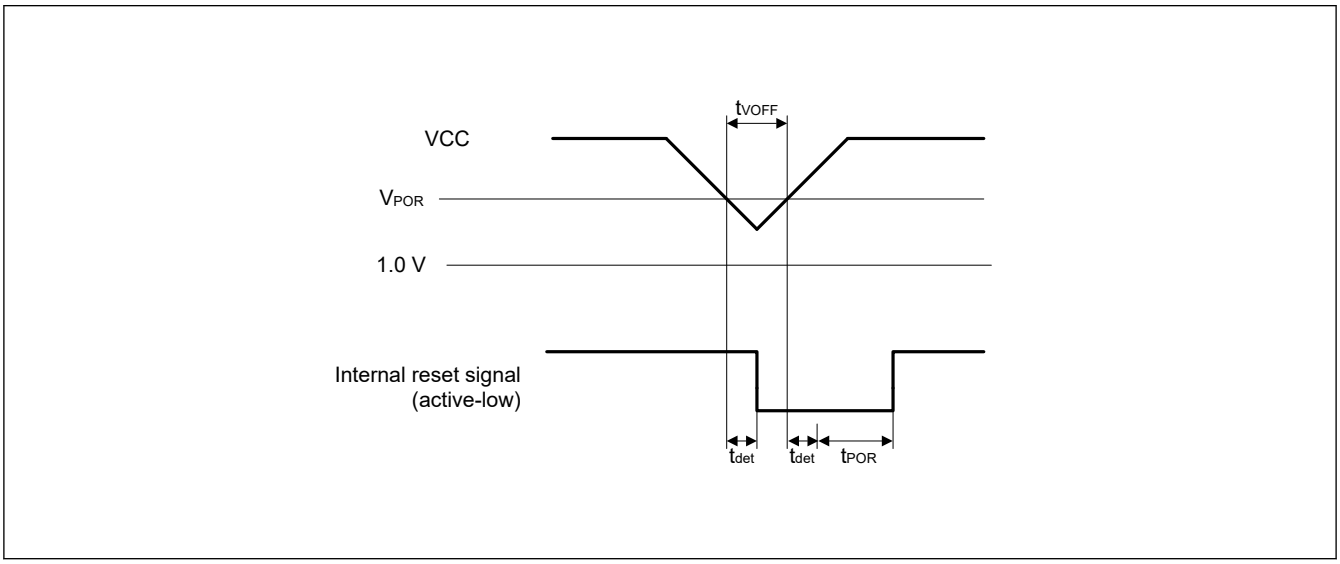
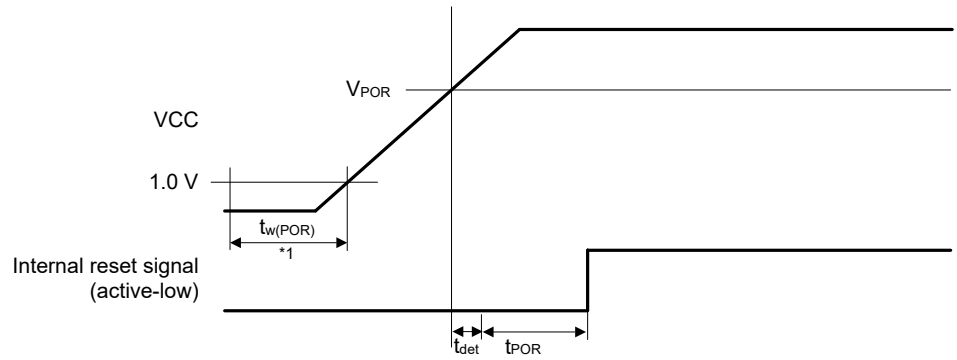


Figure 2.27 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.28 Power-on reset timing

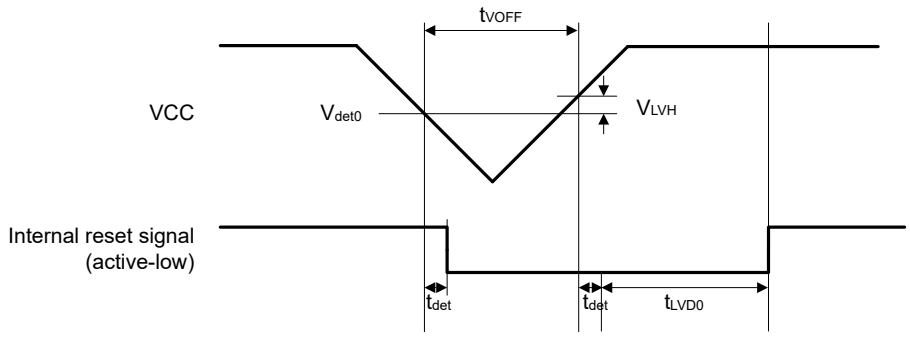


Figure 2.29 Voltage detection circuit timing (V_{det0})

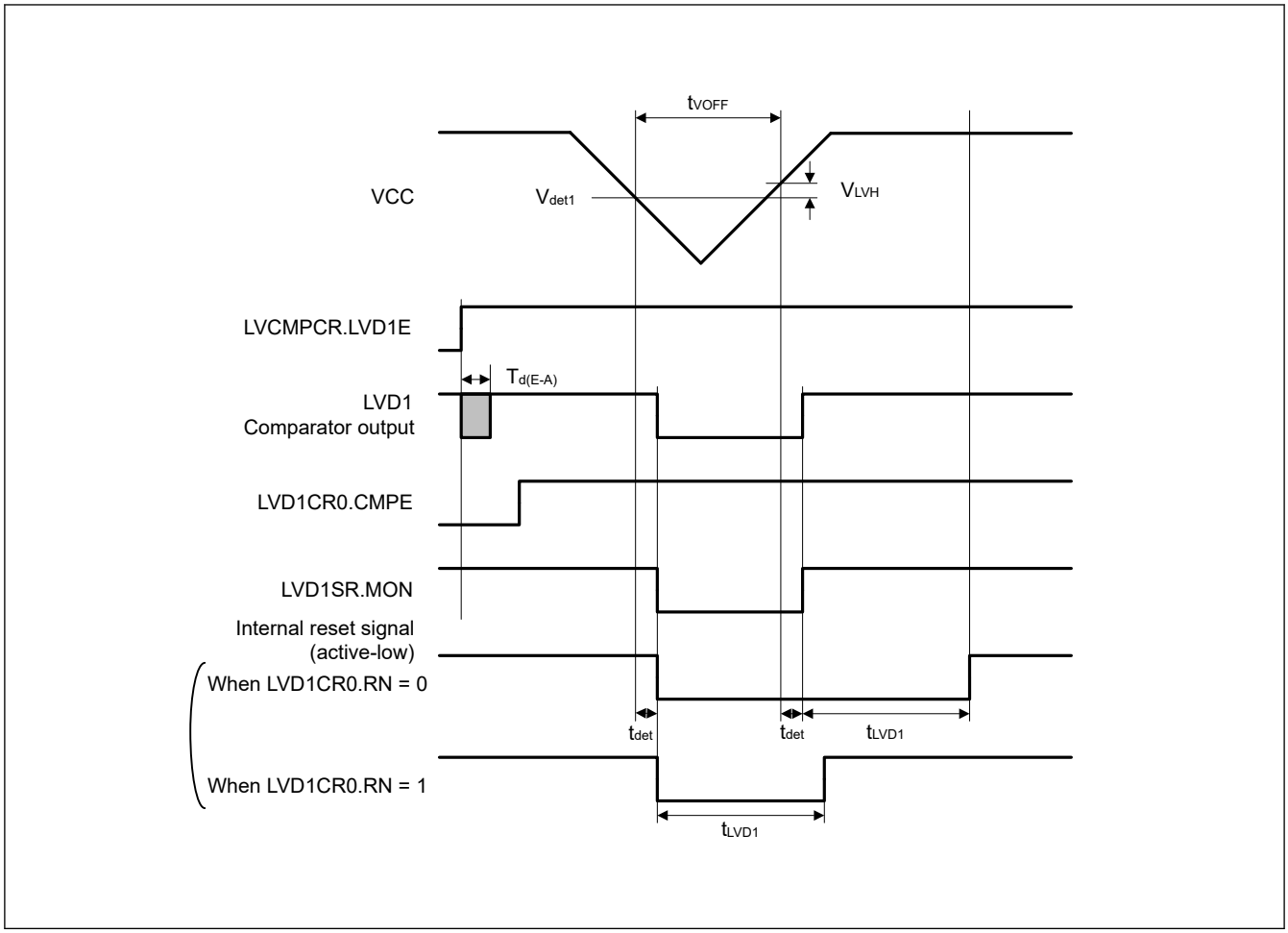


Figure 2.30 Voltage detection circuit timing (V_{det1})

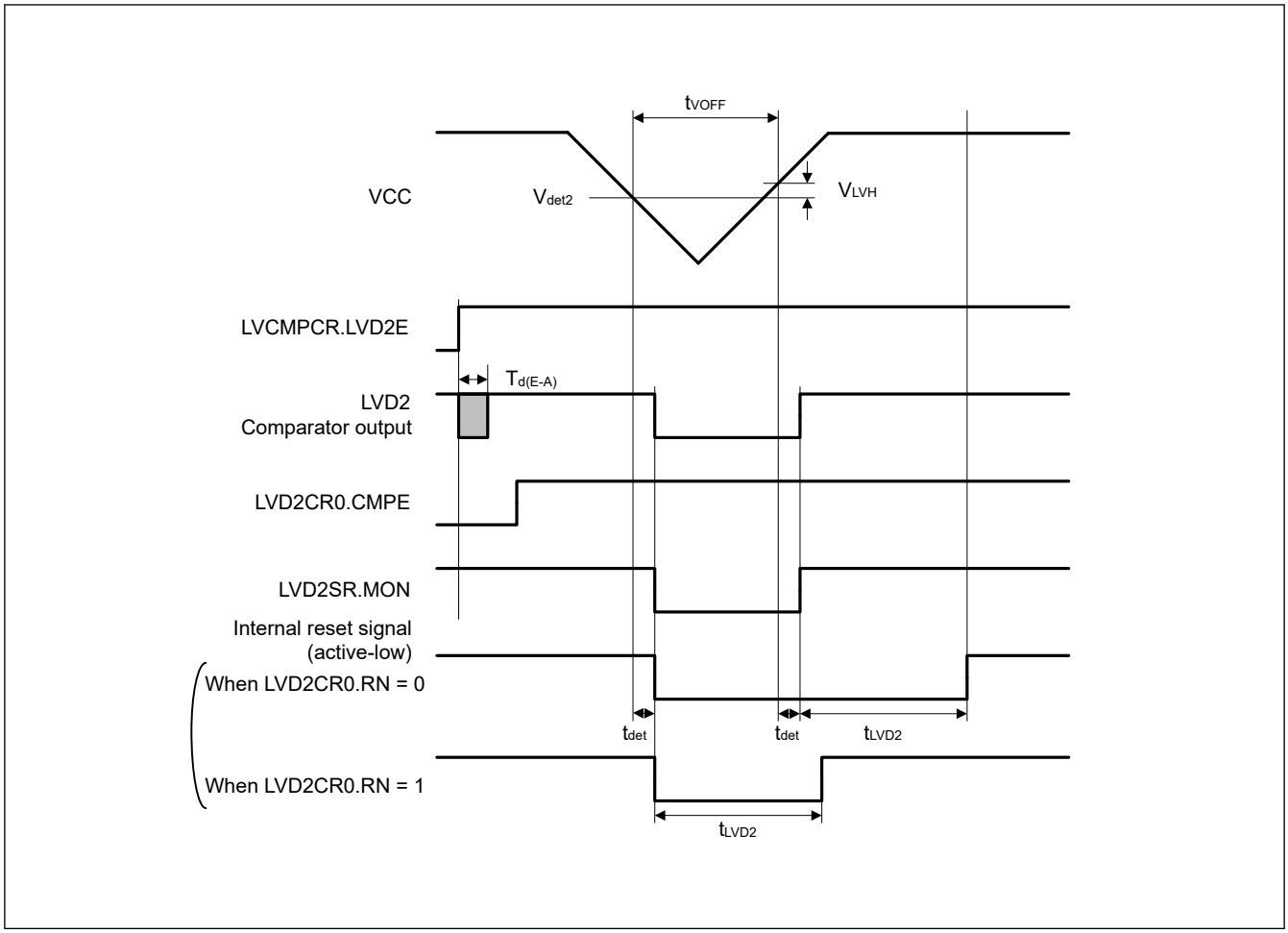


Figure 2.31 Voltage detection circuit timing (V_{det2})

2.9 Flash Memory Characteristics

2.9.1 Code Flash Memory Characteristics

Table 2.55 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	10000	—	—	Times	—
Data hold time	After 10000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = 105°C
			10	—	—		T_a = 125°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,0000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is target spec, may changed after reliability testing.

Table 2.56 Code flash characteristics (2) (1 of 2)

High-speed mode
Conditions: VCC = 1.8 to 5.5 V, T_a = −40°C to 125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P4}	—	97	843	—	47	446	µs
Erasure time	2-KB	t_{E2K}	—	8.7	282	—	5.7	221	ms

Table 2.56 Code flash characteristics (2) (2 of 2)

High-speed mode
Conditions: VCC = 1.8 to 5.5 V, T_a = −40°C to 125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Blank check time	8-byte	t_{BC4}	—	—	45	—	—	8.7	µs
	2-KB	t_{BC2K}	—	—	3239	—	—	235	µs
Erase suspended time		t_{SED}	—	—	22.8	—	—	11.0	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	16.3	509	—	11.8	444	ms
OCD/serial programmer ID setting time		t_{OSIS}	—	65.1	2036	—	46.9	1773.9	µs
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.57 Code flash characteristics (3)

Middle-speed mode
Conditions: VCC = 1.6 to 5.5 V, T_a = −40°C to 125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P4}	—	97	843	—	48	450	µs
Erasure time	2-KB	t_{E2K}	—	8.7	282	—	5.7	220	ms
Blank check time	8- byte	t_{BC4}	—	—	45	—	—	9.1	µs
	2-KB	t_{BC2K}	—	—	3239	—	—	236	µs
Erase suspended time		t_{SED}	—	—	22.8	—	—	11.2	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	16.3	509	—	11.4	442	ms
OCD/serial programmer ID setting time[*1]		t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 5.5 V

Table 2.58 Code flash characteristics (4)

Low-speed mode
Conditions: VCC = 1.6 to 5.5 V, T_a = −40°C to 125°C

Parameter		Symbol	ICLK = 1 MHz			Unit
			Min	Typ	Max	
Programming time	8-byte	t_{P4}	—	97	843	µs
Erasure time	2-KB	t_{E2K}	—	8.7	282	ms
Blank check time	8-byte	t_{BC4}	—	—	45	µs
	2-KB	t_{BC2K}	—	—	3239	µs
Erase suspended time		t_{SED}	—	—	22.8	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	16.3	509	ms
OCD/serial programmer ID setting time		t_{OSIS}	—	65.1	2036	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.9.2 Data Flash Memory Characteristics

Table 2.59 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of NDPEC	t_{DDRP}	20*2 *3	—	—	Year	T_a = 105°C
			10	—	—	Year	T_a = 125°C
	After 100000 times of NDPEC		5*2 *3	—	—	Year	
	After 1000000 times of NDPEC		—	1*2 *3	—	Year	Ta = 25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,024 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. These results are target spec, and may changed after reliability testing.

Table 2.60 Data flash characteristics (2)

High-speed mode
Conditions: VCC = 1.8 to 5.5 V, T_a = −40°C to 125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	84	708	—	36	336	µs
Erasure time	1-KB	t_{DE1K}	—	8.6	281	—	6.3	234	ms
Blank check time	1-byte	t_{DBC1}	—	—	14.8	—	—	8.7	µs
	1-KB	t_{DBC1K}	—	—	1602	—	—	450	µs
Suspended time during erasing		t_{DSED}	—	—	22.8	—	—	11.0	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.61 Data flash characteristics (3)

Middle-speed mode
Conditions: VCC = 1.6 to 5.5 V, T_a = −40℃ to 125℃

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	84	708	—	40	365	µs
Erasure time	1-KB	t_{DE1K}	—	8.6	281	—	7	249	ms
Blank check time	1- byte	t_{DBC1}	—	—	14.8	—	—	11.2	µs
	1-KB	t_{DBC1K}	—	—	1602	—	—	806	µs
Suspended time during erasing		t_{DSED}	—	—	22.8	—	—	11.2	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC ≤ 5.5 V

Table 2.62 Data flash characteristics (4)

Low-speed mode
Conditions: VCC = 1.6 to 5.5 V, T_a = −40℃ to 125℃

Parameter		Symbol	ICLK = 1 MHz			Unit
			Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	84	708	µs
Erasure time	1-KB	t_{DE1K}	—	8.6	281	ms
Blank check time	1-byte	t_{DBC1}	—	—	14.8	µs
	1-KB	t_{DBC1K}	—	—	1602	µs
Suspended time during erasing		t_{DSED}	—	—	22.8	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.10 Compact JTAG (cJTAG)

Table 2.63 cJTAG Characteristics

Conditions: VCC = 2.7 to 5.5 V

No.	Parameter	Symbol	Min	Max	Unit
1	TCKC clock cycle time	$t_{CTCKcyc}$	160	—	ns
1a	TCKC clock high pulse width	t_{CTCKH}	70	—	ns
1b	TCKC clock low pulse width	t_{CTCKL}	70	—	ns
2	TMSC setup time	t_{CTMSS}	14	—	ns
3	TMSC hold time	t_{CTMSH}	2	—	ns
4	Delay time, TCKC to TMSC valid/disable	$t_{d(CTCKL-CTMS)}$	5	60	ns

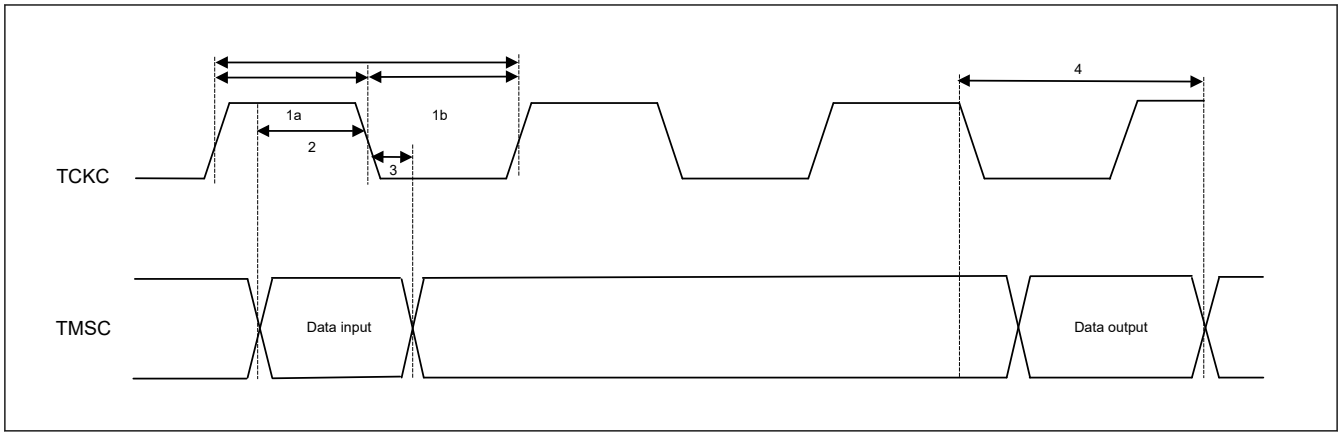


Figure 2.32 cJTAG timing

Appendix 1. Port States in Each Processing Mode

Table 1.1 Port states in each processing mode

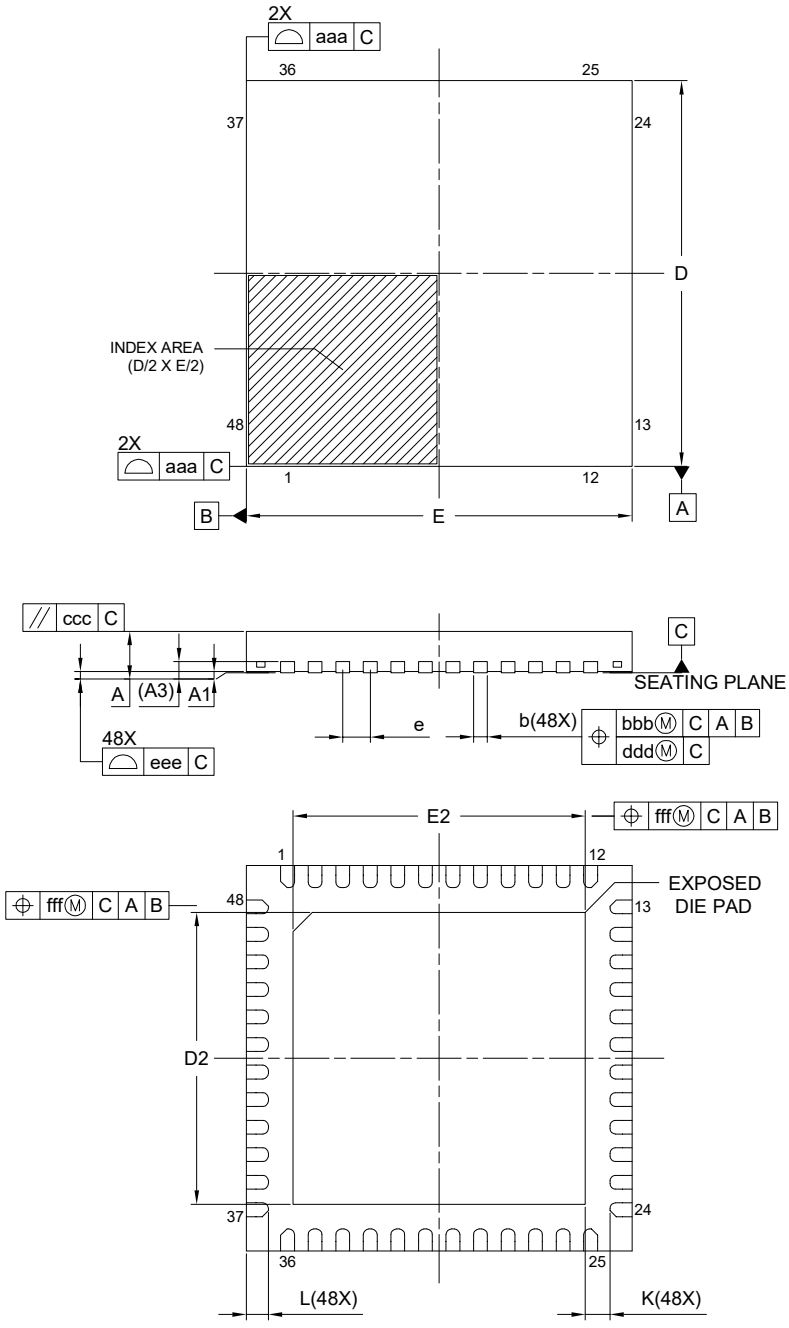
Function	Pin function	Reset	Software Standby mode
Mode	MD	Pull-up	Keep-O
cJTAG	TMSC/TCKC	Pull-up	Keep-O
IRQ	IRQn	Hi-Z	Keep-O*1 *2
	NMI	Hi-Z	Hi-Z*3
SOSC	XT1, XT2	Hi-Z	[Sub-clock Oscillator selected] Sub-clock Oscillator is operating [Other than the above] Hi-Z
KINT	KR0n	Hi-Z	Keep-O*1 *2
SAU	[UART mode] RXD0, RXD2 [SPI mode] SCK00, SCK20	Hi-Z	Keep-O*2
IICA	SCLAn/SDAAn	Hi-Z	Keep-O*1
UARTA	TxDAn/RxDAn/CLKAn	Hi-Z	Keep-O*1
REMC	RIN0	Hi-Z	Keep-O*2
RTC	RTC1HZ	Hi-Z	[RTC selected] RTC1HZ output
CLKOUT	CLKOUT_A/B	Hi-Z	[CLKOUT selected] CLKOUT output
CMP	VCOUTn	Hi-Z	[VCOUT selected] VCOUT output
DAC8	DACOUTn	Hi-Z	[DACOUTn output (DAOE = 1)] D/A output retained
P303	—	Pull-up	Keep-O
Others	—	Hi-Z	Keep-O

Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.
Note 2. Input is enabled if the pin is specified as the snooze mode request trigger in software Standby mode while it is used as an external interrupt pin.
Note 3. Input is enabled.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in packages on the Renesas Electronics Corporation website.

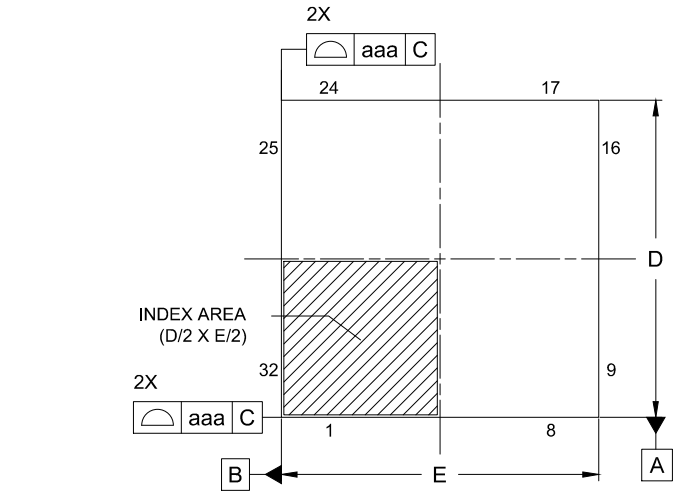
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

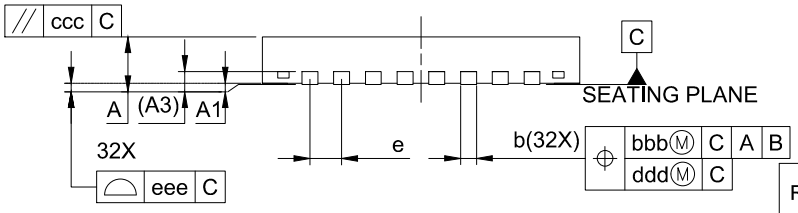


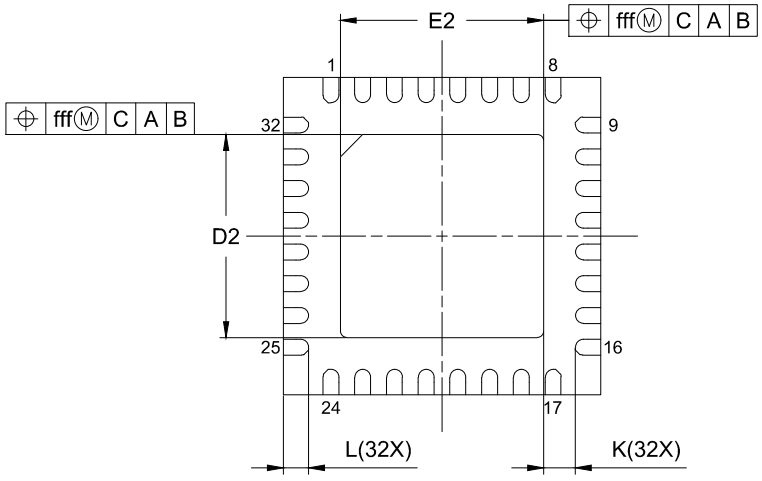
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.1 HWQFN 48-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



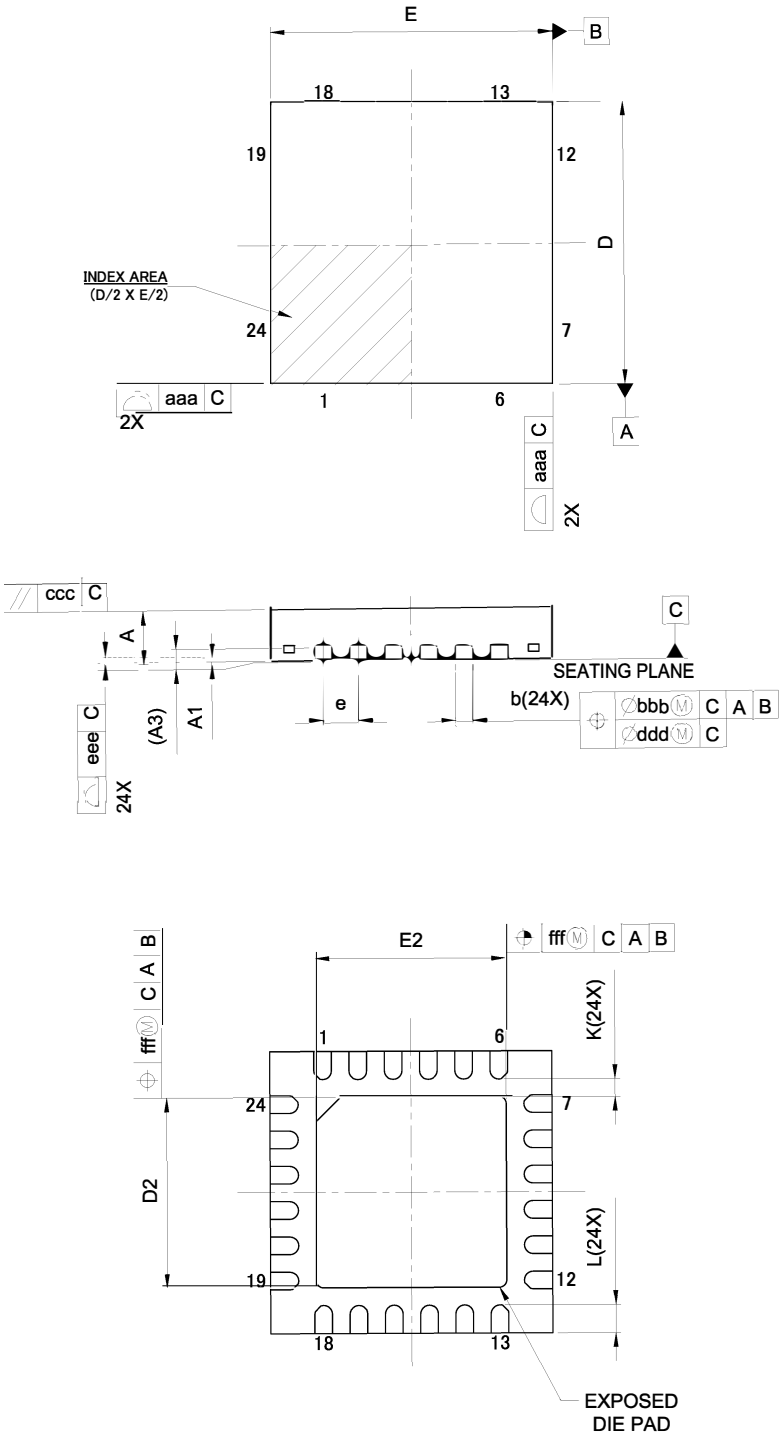




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.2 HWQFN 32-pin

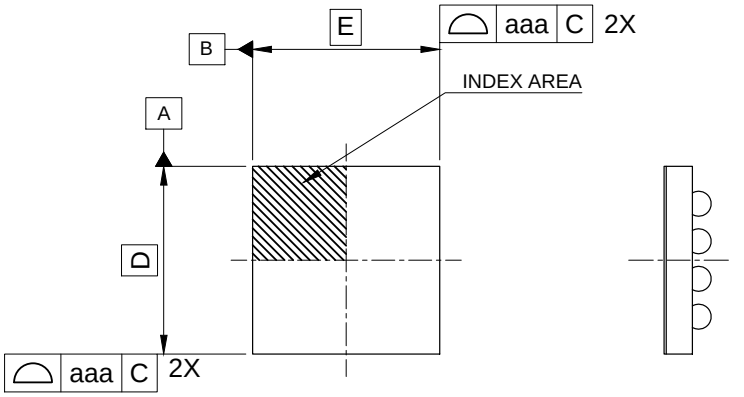
JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HWQFN24-4×4-0.50	PWQN0024KG-A	0.04



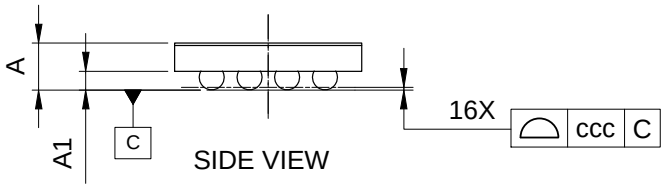
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	2.65	2.70	2.75
E_2	2.65	2.70	2.75
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.3 HWQFN 24-pin

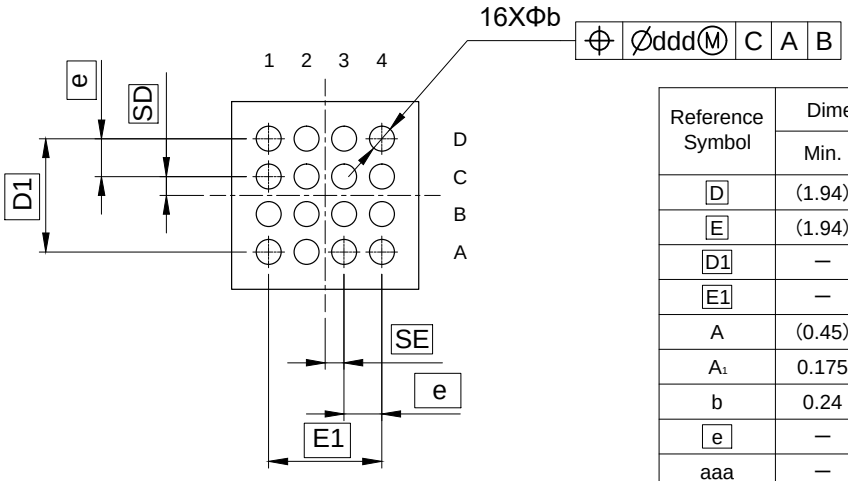
JEITA Package code	RENESAS code	MASS(TYP.)[g]
S-UFBGA16-1.99x1.99-0.40	SUBG0016LC-A	0.01



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	(1.94)	1.99	(2.04)
E	(1.94)	1.99	(2.04)
D1	—	1.20	—
E1	—	1.20	—
A	(0.45)	(0.50)	0.55
A_1	0.175	0.20	0.225
b	0.24	0.265	0.29
e	—	0.40	—
aaa	—	—	0.05
ccc	—	—	0.05
ddd	—	—	0.05
SD	—	0.200	—
SE	—	0.200	—

Figure 2.4 WLCSP 16-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CPU_AUX	CPU Auxiliary Registers	0x4001_A000
CPU_DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4004_0000
PORT1	Port 1 Control Registers	0x4004_0020
PORT2	Port 2 Control Registers	0x4004_0040
PORT3	Port 3 Control Registers	0x4004_0060
PORT4	Port 4 Control Registers	0x4004_0080
PFS	Pmn Pin Function Control Register	0x4004_0800
ELC	Event Link Control	0x4004_1000
WDT	Watchdog Timer	0x4004_4200
IWDT	Independent Watchdog Timer	0x4004_4400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4004_4600
MSTP	Module Stop Control B, C, D	0x4004_7000
DAC8	8-bit D/A Converter	0x4005_E000
CRC	CRC Calculator	0x4007_4000
KINT	Key Interrupt Function	0x4008_0000
DOC	Data Operation Circuit	0x4008_5F00
PORGA	Product Organize Register	0x4009_1000
TRNG	True Random Number Generator	0x4009_1100
CMP	Comparator	0x4009_1200
RTC	Realtime Clock	0x4009_2000
REMC	Remote Control Signal Receiver	0x4009_2100
TML32	32-bit Interval Timer	0x4009_2200
IICA0	I^2C Bus Interface 0	0x4009_3000
IICA1	I^2C Bus Interface 1	0x4009_3100
SAU0	Serial Array Unit 0	0x4009_4000
SAU1	Serial Array Unit 1	0x4009_4100
TAU	Timer Array Unit	0x4009_5000
UARTA	Serial Interface UARTA	0x4009_6000
ADC12	12-bit A/D Converter	0x4009_C000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
FLCN	Flash I/O Registers	0x407E_C000
CLIC	Core-Local Interrupt Controller	0xE200_0000
IMT	Machine Timer	0xE600_0000
DBG	Debug Module	0xE680_0000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table 3.2 shows the register access cycles.

Table 3.2 Access cycles (1 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RAM, BUS, DTC, ICU, CPU_AUX, CPU_DBG	0x4000_0000	0x4001_BFFF	2				ICLK	Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU
SYSC*2	0x4001_E000	0x4001_EFFF	4				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
PORT, PFS, ELC	0x4004_0000	0x4004_1FFF	3*3	3	2 to 4*3	2 to 4	PCLKB	I/O Ports, Event Link Control
WDT, IWDT, CAC, MSTP, DAC8	0x4004_2000	0x4005_FFFF	3		2 to 4		PCLKB	Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control, Data Operation Circuit, 12-bit A/D Converter, 8-bit D/A Converter
CRC	0x4007_4000	0x4007_40FF	3		2 to 4		PCLKB	CRC Calculator
KINT	0x4008_0000	0x4008_00FF	2		2	1 to 3	PCLKB	Key Interrupt Function
DOC	0x4008_5F00	0x4008_5FFF	3		3	2 to 4	PCLKB	Data Operation Circuit

Table 3.2 Access cycles (2 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
PORGA	0x4009_1000	0x4009_10FF	2		1 to 3		PCLKB	Product Organize Register
TRNG	0x4009_1100	0x4009_11FF	3		2 to 4		PCLKB	True Random Number Generator
CMP, RTC	0x4009_1200	0x4009_20FF	2		2	1 to 3	PCLKB	Comparator, Realtime Clock
REMC, TML32	0x4009_2100	0x4009_22FF	2		1 to 3		PCLKB	Remote Control Signal Receiver, 32-bit Interval Timer
IICA, SAU, TAU, UARTA, ADC12	0x4009_3000	0x4009_C0FF	2		1 to 3		PCLKB	I^2C Bus Interface, Serial Array Unit, Timer Array Unit, Serial Interface UARTA, 12-bit A/D Converter
FLCN	0x407E_0000	0x407F_FFFF	3				ICLK	Temperature Sensor, Flash Control
CLIC, IMT, DBG	0xE200_0000	0xE680_0FFF	2				ICLK	CPU

Note: When accessing the 16-bit register (RDRHL, TDRHL, and CDR), access is 2 cycles more than the value in Table 3.2.
Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
Note 2. These values indicate the minimum numbers of cycles for access by the CPU. They do not include the cycles required for changes in the source of the ICLK clock and frequency after changes to the SCKSCR and SCKDIVCR registers.
Note 3. When reading the PCNTR2, PIDR, and PmnPFS* registers, access is (setting value of the PRWCNTR register) cycles more than this value.

Revision History

Revision 1.00 — Nov 15, 2023

Initial release

Revision 1.10 — February 29, 2024

Features:
- Updated information for Connectivity and Timers.

1. Overview:
- Updated Figure 1.1 Block diagram.

2. Electrical Characteristics:
- Updated Table 2.4 I/O VIH, VIL.
- Updated values in the Typ column of Table 2.10 Operating and standby current (1).
- Updated the Note in Table 2.11 Operating and standby current (2).
- Updated Table 2.12 Operating and standby current (3).
- Updated Table 2.56 Code flash characteristics (2).
- Updated Table 2.57 Code flash characteristics (3).
- Updated Table 2.58 Code flash characteristics (4).
- Updated Table 2.60 Data flash characteristics (2).
- Updated Table 2.61 Data flash characteristics (3).
- Updated Table 2.62 Data flash characteristics (4).

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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