R2A20114BFP

R03DS0101EJ0100
Rev.1.00
Nov. 8, 2016

Continuous Conduction Mode Interleaving PFC Control IC

Description

R2A20114BFP is a boost converter IC with PFC (Power Factor Correction). Based on R2A20114AFP, R2A20114BFP has improved usability such as built-in PFC boost voltage control, current detecting amplifier with differential inputs, independent and high-functional error output pin, timer reset of OFF latch, and partial switch for PFC.

Interleaving control of the boost converters, namely, producing 180 degrees phase shift between the output signals (GD1,2) driving the boost converters, enables the system to perform high conversion efficiency and low switching noises and, at the same time, to reduces ripple currents in input and output current and then this allows use of smaller components such as boost inductors, input filters and output capacitors.

R2A20114BFP integrates a various kinds of protection circuits, such as the detection circuit of breaking of wire in feedback loop, two modes of over voltage protection circuits, over current protection circuit and error output circuit (*1), which improve the reliability of the power supply system and reduce the number of component parts on the system.

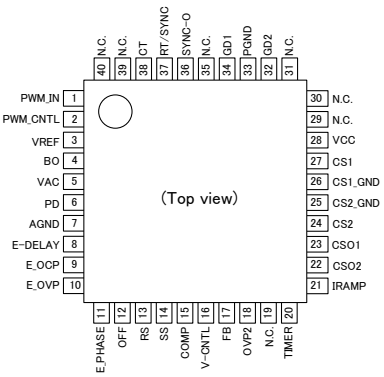
Functions

- Boost converter control with continuous conduction mode
- Interleaving control
- Brownout
- Phase drop
- External clock synchronization input
- External clock synchronization output
- Two modes of over voltage protection
  - Mode 1: Dynamic OVP preventing over voltage after sudden variation of load
  - Mode 2: Static OVP preventing over voltage in the period of normal operation
- Dual over voltage protection circuits: FB and OVP2 terminals
- Feedback loop wire breaking/open detector
- Current balance control
- Phase 1 and Phase 2 independent over current protection
- Variable PFC output voltage

Features

<Maximum Ratings>
Supply voltage Vcc: 24V
Operating ambient temperature Ta-opr: -40 to 125℃
Junction temperature Tj: -40 to 150℃
<Electrical Characteristics>
VFB Feedback voltage VFB: 2.5V ± 1.5%
UVLO operating start voltage VH: 10.4V ± 0.7V
UVLO operation shutdown voltage VL: 8.9V ± 0.5V
UVLO hysteresis voltage Hysuv1: 1.5V ± 0.5V
<Package>
Pb-free LQPF-

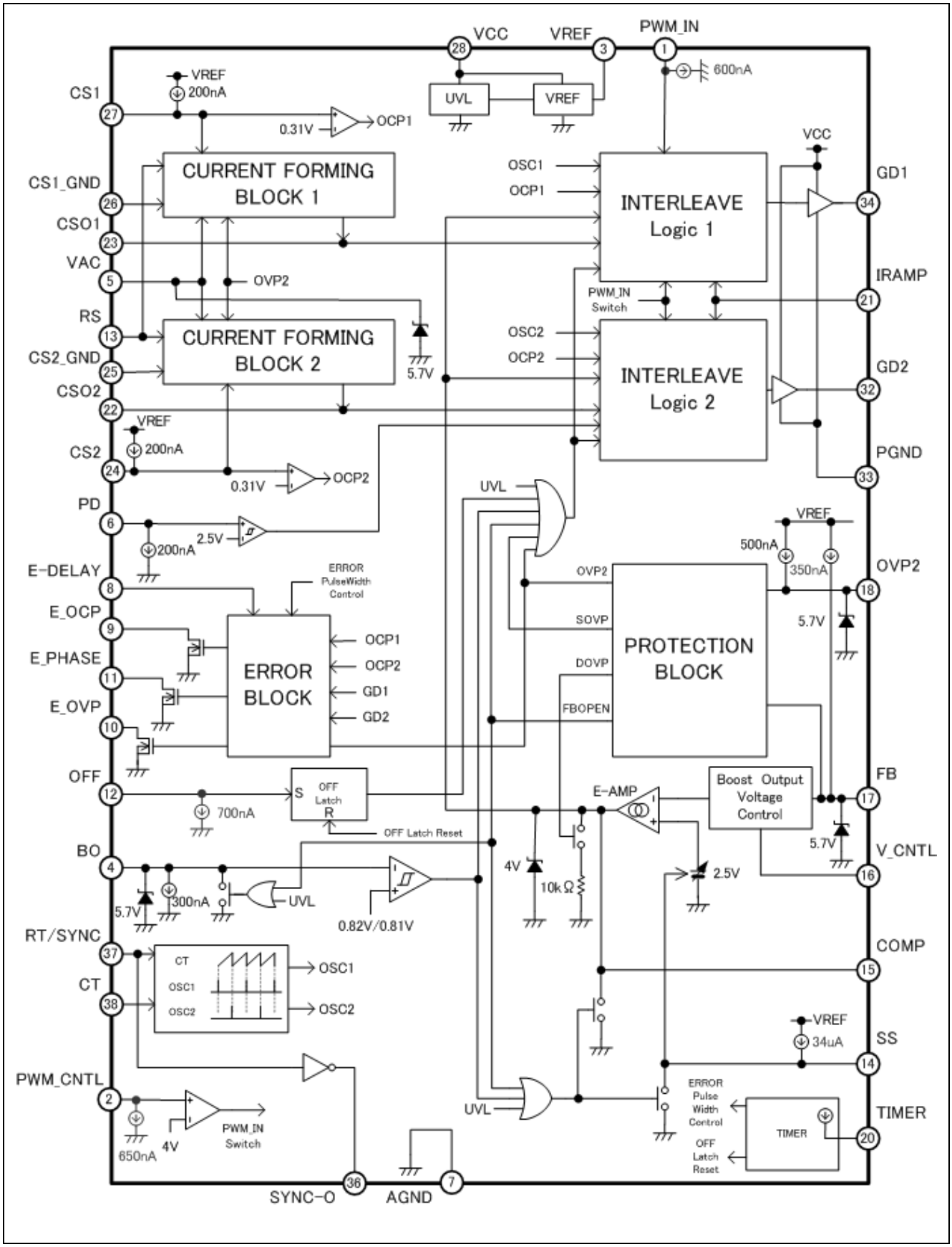
Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
1	PWM_IN	PWM signal input terminal
2	PWM_CNTL	PWM signal input mode switching terminal
3	VREF	Reference voltage output terminal
4	BO	Brownout input terminal
5	VAC	AC voltage input terminal
6	PD	Phase drop input terminal
7	AGND	Analog ground
8	E-DELAY	Delay of the error signal setting terminal
9	E_OCP	OCP error signal output terminal
10	E_OVP	OVP2 error signal output terminal
11	E_PHASE	PHASE error signal output terminal
12	OFF	Shutdown terminal
13	RS	Current correction setting resistor connecting terminal
14	SS	Soft start setting capacitor connecting terminal
15	COMP	Error amplifier output terminal (to be phase-compensated)
16	V_CNTL	DC voltage input terminal to control PFC boost voltage
17	FB	Error amplifier output terminal (feedback voltage input terminal)
18	OVP2	OVP2 input terminal
19	N.C.	Open
20	TIMER	ERROR pulse width & OFF latch auto-reset time setting capacitor connecting terminal
21	IRAMP	Ramp waveform setting resistor connecting terminal
22	CSO2	Current sense amplifier 2 output terminal (to be phase-compensated)
23	CSO1	Current sense amplifier 1 output terminal (to be phase-compensated)
24	CS2	Current sense 2 ＋input terminal
25	CS2_GND	Current sense 2 －input terminal
26	CS1_GND	Current sense 1 －input terminal
27	CS1	Current sense 1 ＋input terminal
28	VCC	Supply voltage terminal
29-31	N.C.	Open
32	GD2	Converter 2 power MOSFET drive terminal
33	PGND	Power ground
34	GD1	Converter 1 power MOSFET drive terminal
35	N.C.	Open
36	SYNC-O	Synchronization signal output terminal
37	RT/SYNC	Frequency setting resistor connecting/Sync. Signal input terminal
38	CT	Frequency setting capacitor connecting terminal
39,40	N.C.	Open

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Supply voltage		VCC	-0.3 to +24	V	3
GD1 and GD2	Peak current	Ipk-gd1, Ipk-gd2	±0.2	A	3, 4
	DC current	Idc-gd1, Idc-gd2	±0.02	A	3
Vref terminal current		Iref	-10	mA	3
Terminal current		It-group	±1	mA	3, 5
RS terminal current		Irs	-500	μA	3
RT terminal current		Irt	-200	μA	3
IRAMP terminal current		Iramp	-200	μA	3
Terminal clamp current		Iclamp	300	μA	6
Terminal voltage		Vt-group	-0.3 to Vref	V	3, 7
Vref terminal voltage		Vt-ref	-0.3 to Vref+0.3	V	3
CS1 terminal, CS2 terminal voltage		Vt-cs	-1 to +1	V	3
Power dissipation		Pt	1	W	3, 8
Operating ambient temperature		Ta-opr	-40 to +125	°C	
Junction temperature		Tj	-40 to +150	°C	9
Storage temperature		Tstg	-55 to +150	°C	

Notes

1. Rated voltages are with reference to the AGND and PGND terminals
2. For the direction of rated current, (+) denotes the current flowing into and (-) denotes the current flowing out of the IC
3. Ambient temperature Ta is 25 degrees centigrade.
4. Transient current when driving a capacitive load
5. Rated current for terminals COMP, CSO1, CSO2
6. Rated current for terminals VAC, FB, BO OVP2
7. Rated current for terminals CS1_GND, CS2_GND, RS, PD, E_OCP, E_OVP, E_PHASE, E-DELAY, OFF, PWM_IN, PWM_CNTL, RT/SYNC, IRAMP, SYNC-O, CT, COMP, CSO1, CSO2, TIMER, V_CNTL, SS
8. Thermal resistance θ ja = 85.3° C/W When the IC is mounted on glass epoxy board of 50 x 50 x 1.6 (mm)
9. Stress over the absolute maximum ratings may give a fatal damage to the IC. These values are ratings of the stress and functional operation of the IC exceeding recommended operating temperature is not included. Leaving in the conditions of the absolute maximum ratings long time may impact the reliability of the IC.

Electrical Characteristics

(Ta=25℃, VCC=12V, CT=1000pF, RT=27kΩ, CS1,CS2=GND, CS1_GND,CS2_GND=GND, V_CNTL=0V, IRAMP=10kΩ, BO=1V, VAC=0V, RS=220kΩ, FB=COMP)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	UVLO turn-on threshold	Vuvlh	9.7	10.4	11.1	V	
	UVLO turn-off threshold	Vuvll	8.4	8.9	9.4	V	
	UVLO hysteresis	Hysuvl	1	1.5	2	V	
	Standby current	Istby	-	100	160	μA	VCC = 8.9 V
	Operating current	Icc	-	5	7.5	mA	
VREF	Output voltage	Vref	4.85	5	5.15	V	Isource = –1 mA
	Line regulation	Vref-line	-	5	20	mV	Isource = –1 mA, VCC = 10 V to 24 V
	Load regulation	Vref-load	-	5	20	mV	Isource = –1 mA to -10 mA
	Temperature stability	dVref	-	±80	-	ppm/°C	Ta = –40 to 125°C (*1)
Error amplifier	Feedback voltage	Vfb	2.462	2.5	2.538	V	FB-COMP Short
	Input bias current	Ifb	–0.8	–0.4	–0.2	μA	Measured pin: FB
	Open loop gain	Av	-	40	-	dB	(*1)
	Upper clamp voltage	Vclamp-comp	3.8	4	4.3	V	FB = 2.0 V, COMP: Open
	Low voltage	Vl-comp	0	0.1	0.3	V	FB = 3.0 V, COMP: Open
	Source current	Isrc-comp	–190	–135	–80	μA	FB = 1.5 V, COMP = 2.5 V
	Sink current 1	Isnk-comp1	-	120	-	μA	(*1)
	Sink current 2	Isnk-comp2	220	320	420	μA	FB =3.5 V, COMP = 2.5 V
	Transconductance	gm	120	200	290	μs	FB = 2.45 V ↔ 2.55 V, COMP = 2.5 V
Brownout	PFC enable voltage	Von-pfc	0.74	0.82	0.9	V	Input pin: BO
	PFC disable voltage	Voff-pfc	0.73	0.81	0.89	V	Input pin: BO
Oscillator	Initial accuracy	fout	70	78	86	kHz	Measured pin: OUT
	fout temperature stability	dfout/dTa	-	±0.1	-	%/°C	Ta = –40 to 125°C (*1)
	fout voltage stability	fout-line	–1.5	0.5	1.5	%	VCC = 12 V to 18 V
	CT top voltage	Vct-H	-	3.6	4	V	(*1)
	RT voltage	Vrt	1.15	1.25	1.35	V	
Synchroni-zation	SYNC threshold voltage(rising)	Vsync	2	3	4	V	
	SYNC Min. pulse	Psync	2	-	-	μs	
	SYNC-OUT Low Voltage	Vol-sync-o	-	-	0.3	V	Isink=1mA
	SYNC-OUT High Voltage	Voh-sync-o	4.4	-	-	V	Isource=-1mA

Note) *1 Design specification (data for reference)

(Ta=25℃, VCC=12V, CT=1000pF, RT=27kΩ, CS1,CS2=GND, CS1_GND,CS2_GND=GND, V_CNTL=0V, IRAMP=10kΩ, BO=1V, VAC=0V, RS=220kΩ, FB=COMP)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current slope	RS output voltage 1	Vrs1	0.42	0.51	0.6	V	VAC = 0 V, VOVP2 = 2.5 V
	RS output voltage 2	Vrs2	–0.1	0	0.1	V	VAC = 2.5 V, VOVP2 = 0 V
	VAC bias current	Ivac	–0.4	–0.2	–0.05	µA	Measured pin: VAC
Soft start	Source current	Iss	–48	–34	–20	µA	SS = 2 V
Phase drop	Phase drop threshold voltage	Vpd	2.4	2.5	2.6	V	
	Phase drop hysteresis	Hya-pd	150	200	250	mV	
	PD bias current	Ipd	0.05	0.2	0.5	µA	Measured pin: PD
PWM_IN	Input Voltage	Vpwm_in_h	3.5	-	-	V	
		Vpwm_in_l	-	-	1.5	V	
	PWM_IN Bias current	Ipwm_in	0.3	0.6	1.2	µA	
	Delay to output	Td-pwm_in	-	100	250	Ns	
	PWM_CNTL Threshold voltage	Vpwm_cntl	3.3	4.0	4.7	V	Measured pin : PWM_CNTL
	PWM_CNTL Bias current	Ipwm_cntl	0.32	0.65	1.3	µA	Measured pin : PWM_CNTL
AMP1, 2	CSO offset voltage1	Voffset	0.60	0.85	1.1	V	Vcs = 0 V
	CSO offset voltage2	Vcaoh	2.7	3	3.3	V	Vcs = 0.24 V
	CS Bias current	Ics-r	–0.4	–0.2	–0.05	µA	Measured pin: CS1, 2
Gate drive 1 and 2	Gate drive rise time	tr-gd	-	30	100	ns	CL = 100 pF
	Gate drive fall time	tf-gd	-	30	100	ns	CL = 100 pF
	Gate drive low voltage	Vol1-gd	-	0.05	0.3	V	Isink = 2 mA
		Vol2-gd	-	1	1.25	V	Isink = 0.05 mA, VCC = 5 V
	Gate drive high voltage	Voh-gd	11.5	11.9	-	V	Isource = –2 mA
	Minimum duty cycle	Dmin-out	-	-	0	%	
	Maximum duty cycle	Dmax-out	90	95	98	%	

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Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Over voltage protection	Dynamic OVP Threshold voltage	Vdovp	VFB× 1.025	VFB× 1.04	VFB× 1.055	V	
	Static OVP Threshold voltage	Vsovp	VFB× 1.065	VFB× 1.08	VFB× 1.095	V	COMP = OPEN
	Static OVP Hysteresis	Hys-sovp	50	100	150	mV	COMP = OPEN
	OVP2 Threshold voltage	Vovp2	VFB× 1.065	VFB× 1.08	VFB× 1.095	V	COMP = OPEN
	OVP2 Hysteresis	Hys-ovp2	50	100	150	mV	COMP = OPEN
	OVP2 Bias current	Iovp2	-0.7	–0.35	–0.17	μA	Measured pin: OVP2
	FB Open Detect Threshold voltage	Vfbopen	0.45	0.5	0.55	V	
	FB Open Detect hysteresis	Vfbopen	0.16	0.2	0.24	V	
Over current protection	OCP Threshold voltage	VCL	0.28	0.31	0.34	V	
	Delay to output	td-CL	-	100	250	ns	
V_CNTL	Input Range	Vcntl	0	-	3.5	V	
	V_CNTL Disable voltage	Vcntl_dis	-	0.2	-	V	
	V_CNTL Limit voltage	Vcntl_clamp	-	4	-	V	
	VFB Control voltage 1	Vfb_cntl1	2.371	2.445	2.519	V	V_CNTL=0.3V
	VFB Control voltage 2	Vfb_cntl2	1.571	1.645	1.769	V	V_CNTL=3.5V
	Discharge Current	Icntl	0.87	1.75	3.50	μA	

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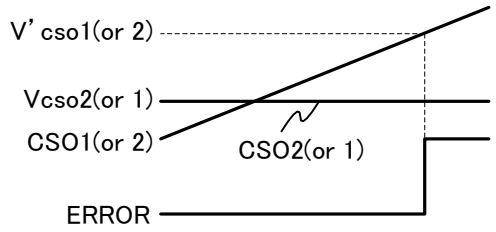
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Error signal	ERROR shunt current	Ierror-s	1	-	-	mA	
	ERROR leakage current	Ierror-l	-	-	1	μA	
	Phase error detect point	Perror	1.1	1.35	1.6	-	Vcso1 or 2 = 2.5 V, Vcso2 or 1: sweep (*1)
	OFF threshold voltage	Voff	3.3	4	4.7	V	
	OFF terminal Input bias current	Ioff	0.35	0.7	1.4	μA	
	OFF Latch Reset Threshold voltage	Vres_lat	3.8	4.0	4.2	V	Measured pin : TIMER
	ERROR timer Reset Threshold voltage	Vres_err	1.9	2.0	2.1	V	Measured pin : TIMER
	TIMER terminal current	Itim_off	-90	-60	-30	μA	
		Itim_ocp	-3.2	-2.0	-1.2	mA	
		Itim_ovp	-1.6	-1.0	-0.6	mA	
		Itim_phase	-800	-500	-300	μA	
	E-DELAY charge current	Ied-c	–55	–36	–20	μA	
	E-DELAY discharge current	Ied-d	20	36	55	μA	
	E-DELAY threshold voltage	Vdelay	2.35	2.45	2.55	V	

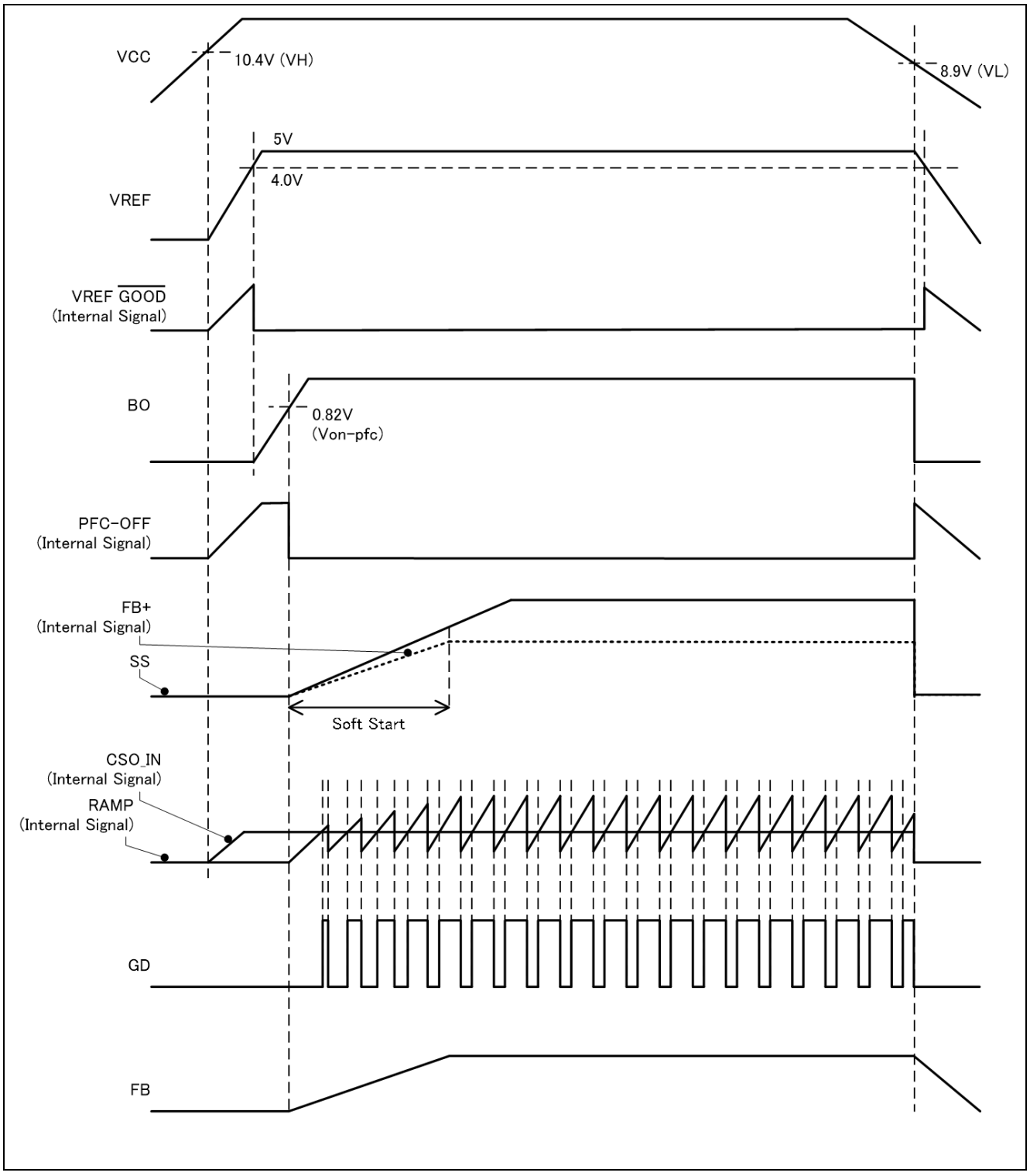
Note) *1



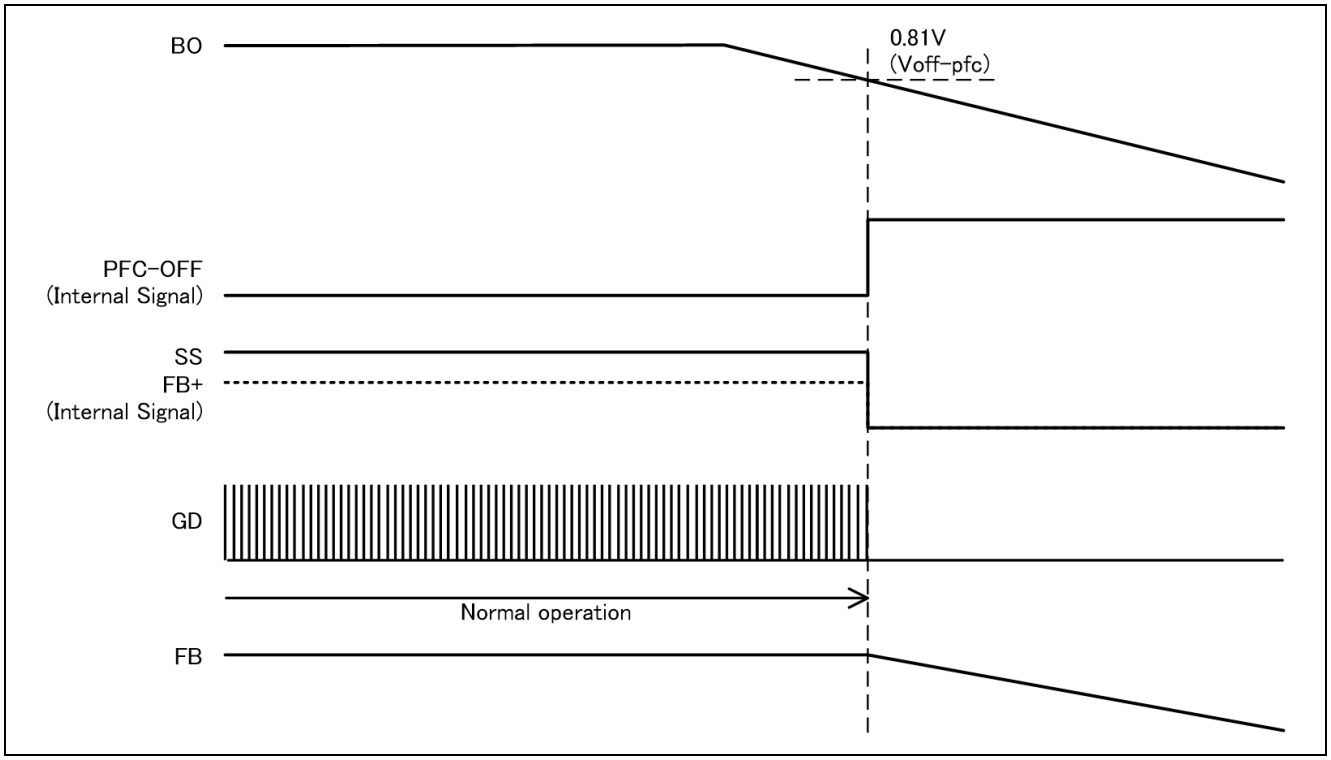
$$P_{error} = \frac{V'_{cso1(or\,2)}[V] - 0.65[V]}{V_{cso2(or\,1)}[V] - 0.65[V]}$$

Timing Chart

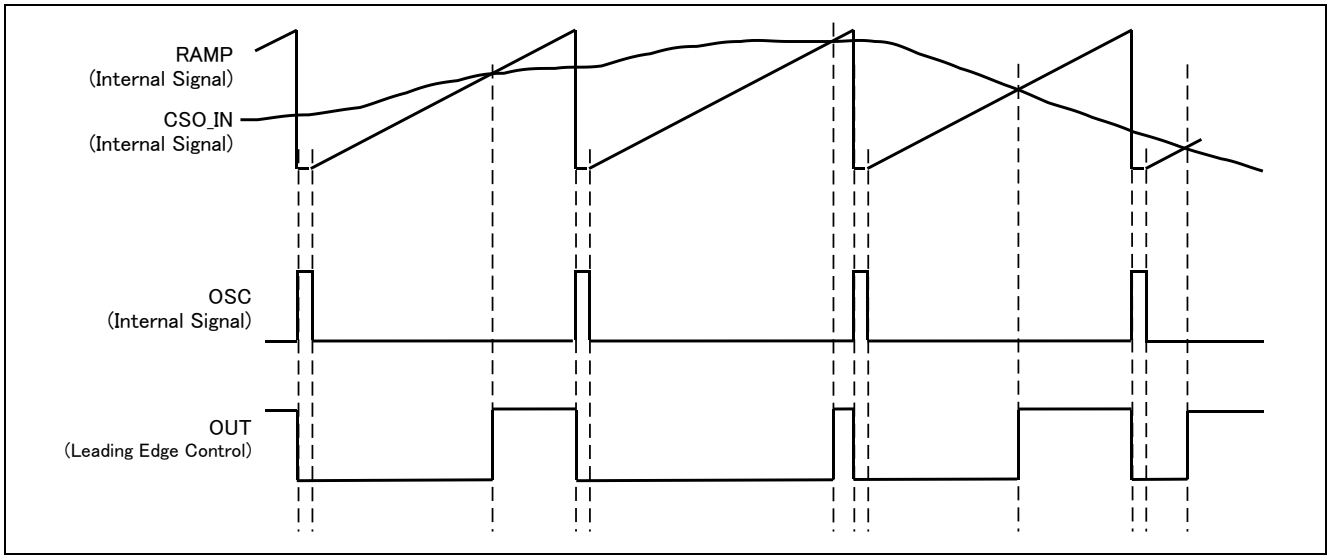
Vcc Start-up and Stop timing



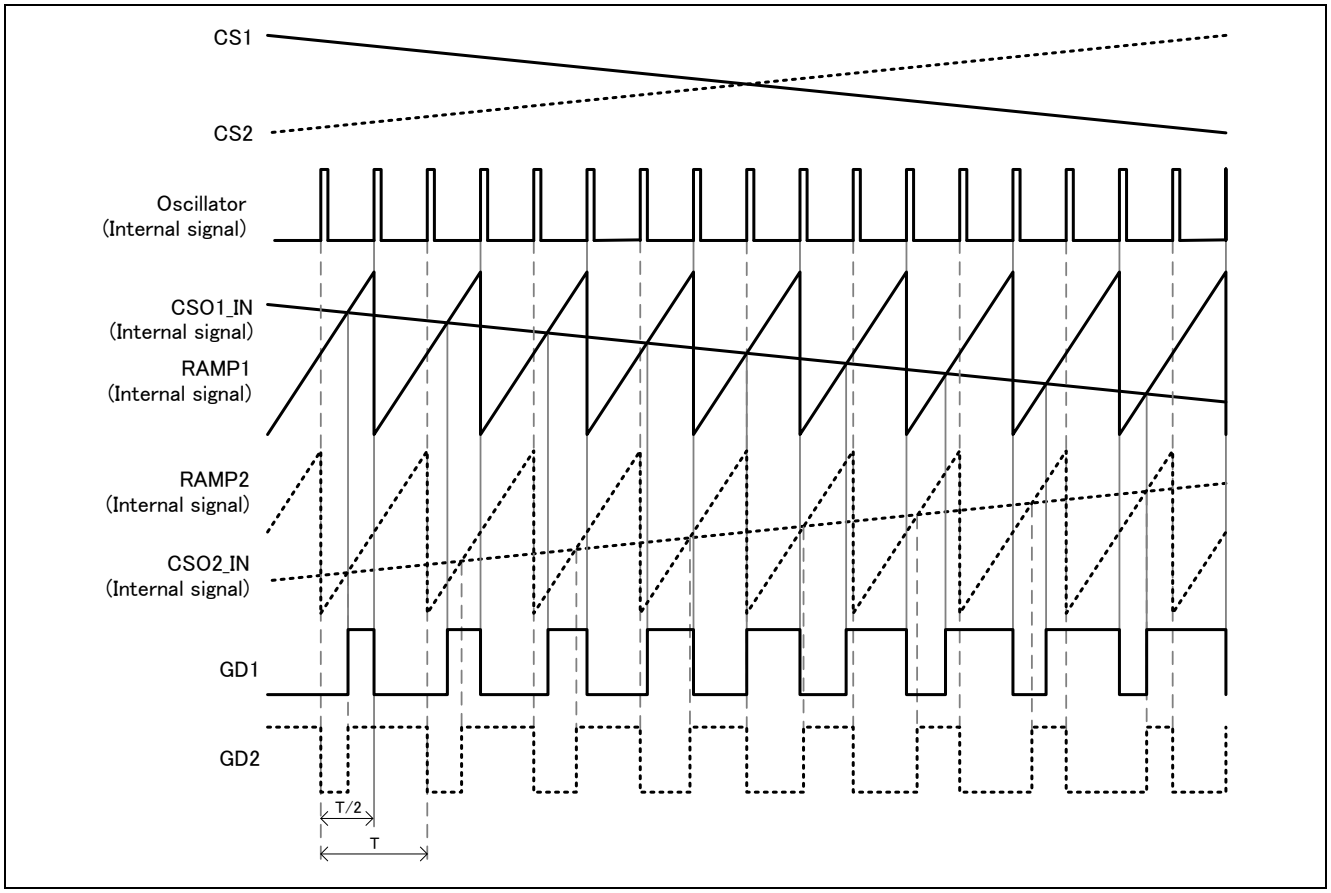
Stop timing



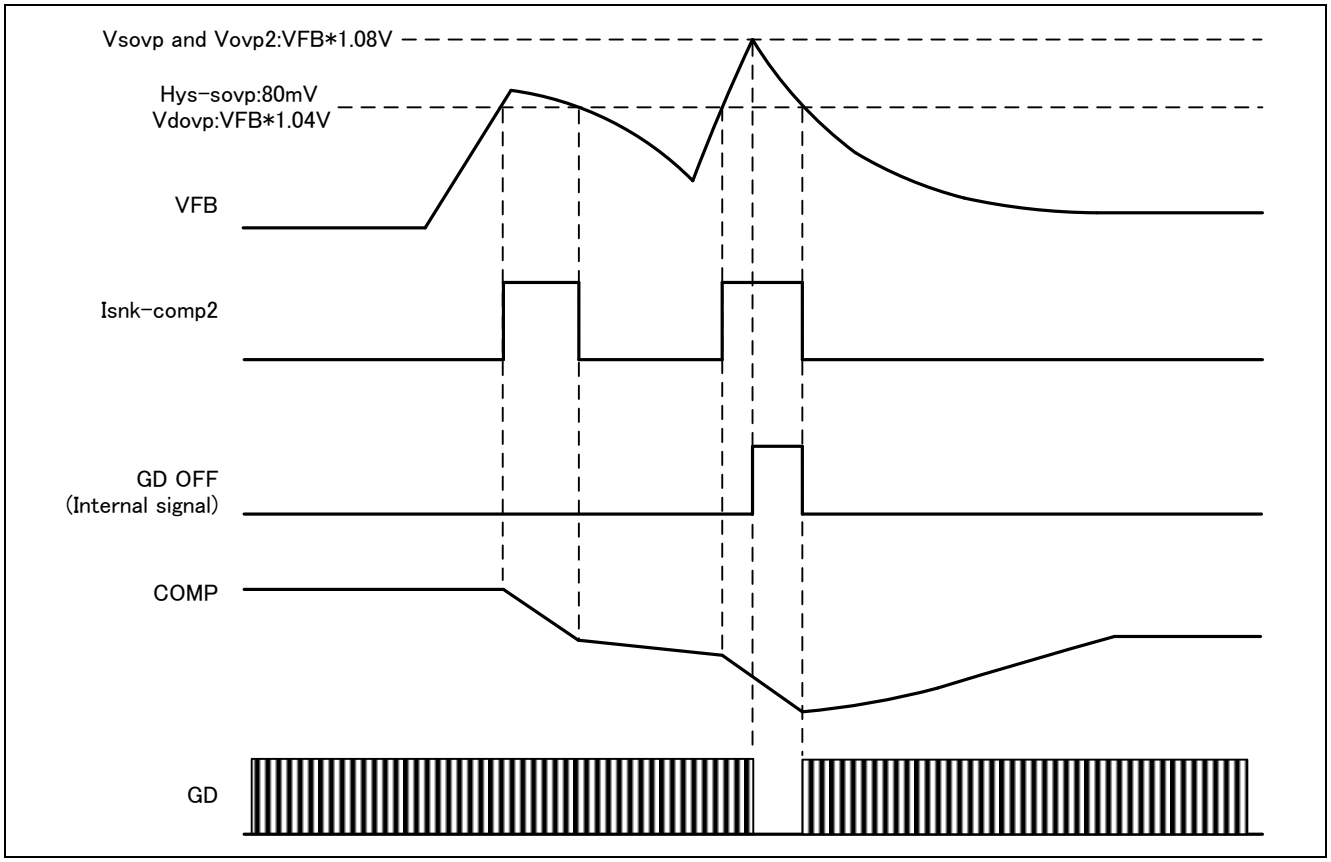
Oscillator, Gate Drive Output



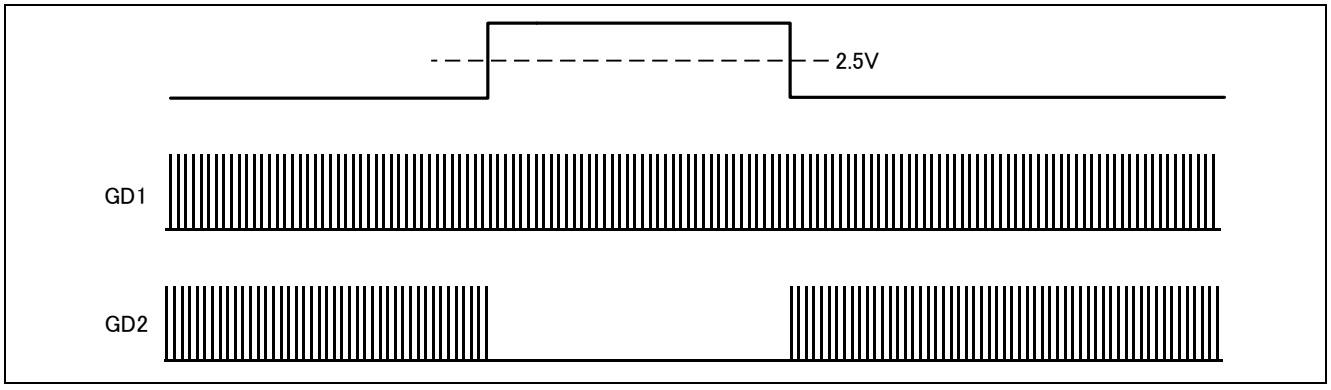
Current share



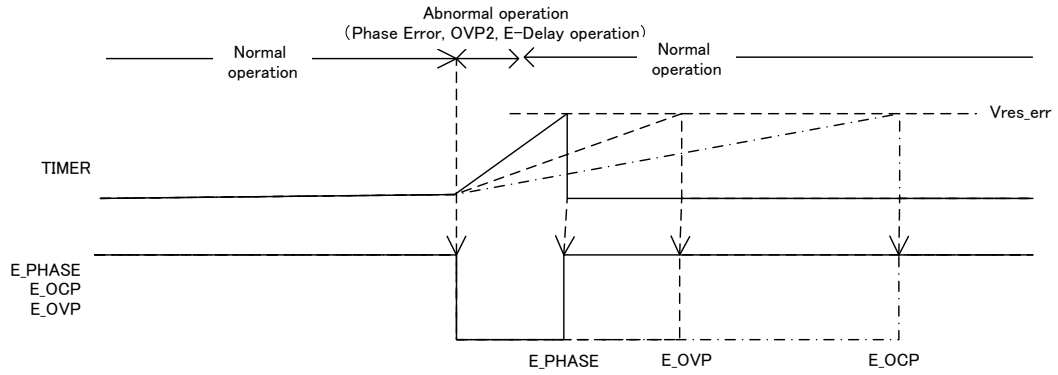
Overvoltage protection (OVP)



Phase drop

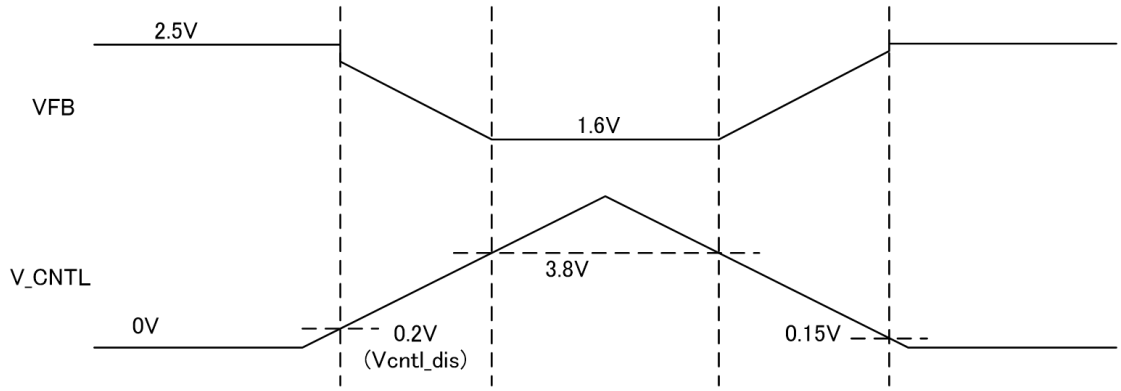


E_PHASE, E_OCP, E_OVP

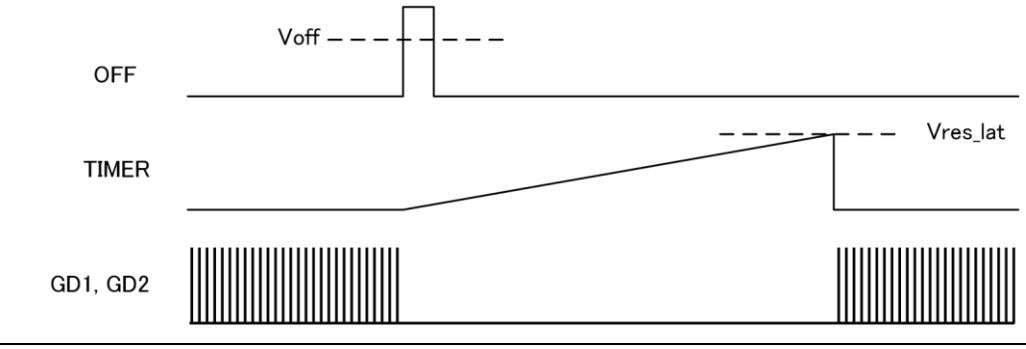


The pulse width which occurs is different depending on the kinds of ERROR.

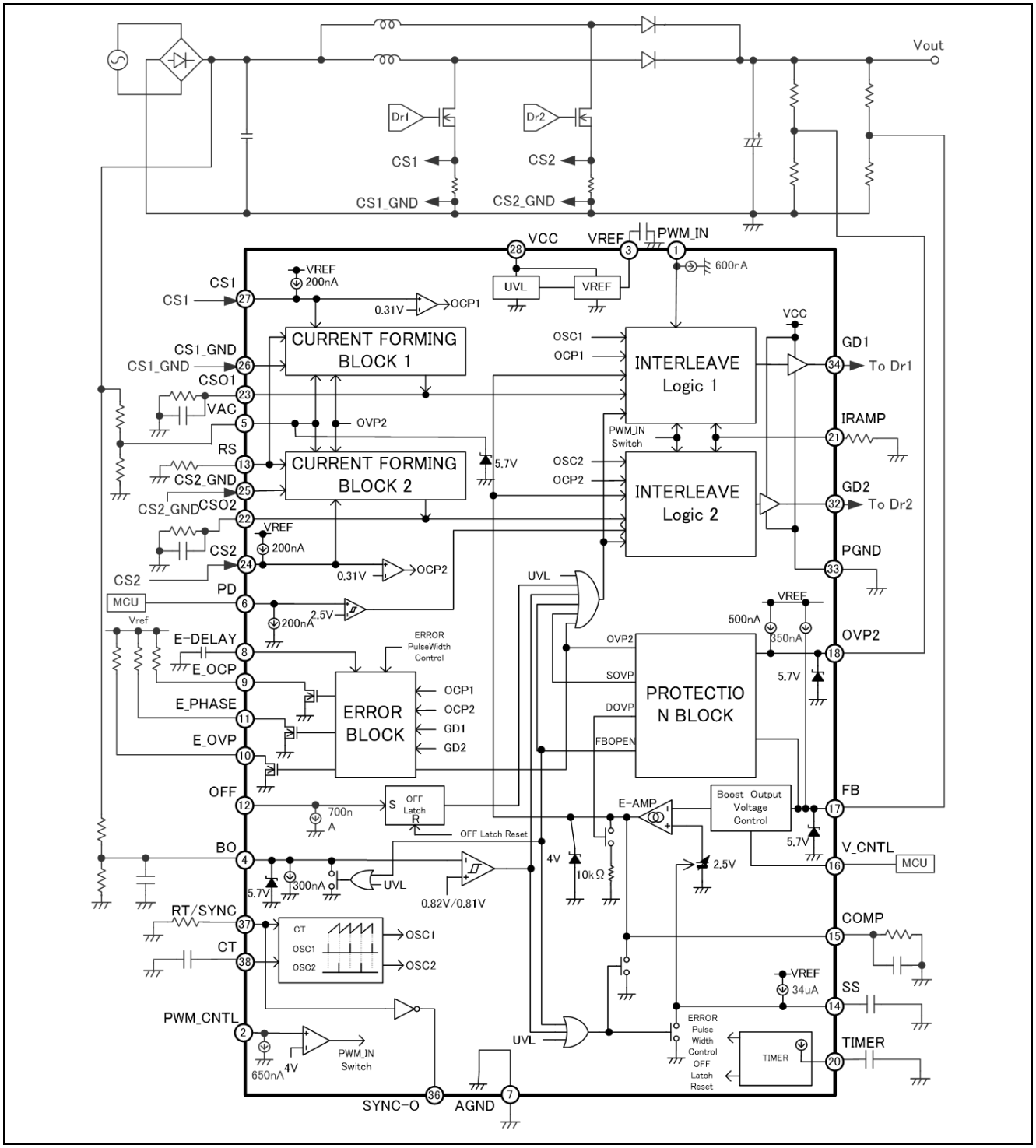
Programmable boost output voltage



Off latch

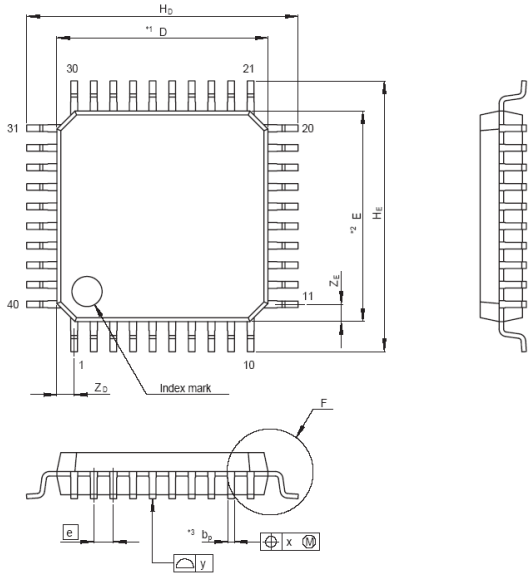


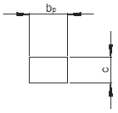
System Diagram



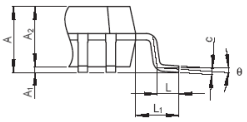
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP40-7x7-0.65	PLQP0040JB-C	FP-40EV	0.2g





Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2"
DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
A_2	—	1.40	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.70
A_1	0.08	0.13	0.22
b_p	0.17	0.22	0.27
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—
L	0.40	0.50	0.60
L_1	—	1.0	—

Revision History	R2A20114BFP Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 8, 2016	-	New

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