PTX205R

Mid-Power NFC Controller Supporting NFC Forum Applications

Description

The PTX205R is a highly integrated, mid-power NFC controller for NFC Forum applications, supporting reader/writer, card emulation and peer to peer mode. Its patented Switched-Cap Power Amplifier (SCPA) architecture enables a sine-wave driver that simplifies system integration and supports compact antenna designs, while ensuring best-in-class interoperability with existing NFC ecosystems.

The modular NFC Soft Controller (NSC) architecture, combined with the advanced Split Stack software framework, enables separation of time-critical operations, executed on the on-chip MCU, from high-level functionality running on the host controller. The result is a streamlined design that ensures real-time responsiveness while enabling implementation on cost-efficient host systems.

Features

RF Communication

- ISO/IEC 14443-A/B reader/writer mode (up to 848kBit/s)
- ISO18092 reader/writer mode (FeliCa™, 212/424 kbit/s)
- ISO/IEC 15693 reader/writer mode (up to 53kBit/s)
- Supports reading/writing of NFC Tag Type 2/3/4A/4B/5
- ISO/IEC 14443-A/B Card Emulation mode
- ISO/IEC 18092-FeliCa Card Emulation mode
- NFC Forum Peer-to-Peer (ISO 18092) Initiator/Target
- NFC Forum Certification compliant

Advanced Features

- Low Power Card Detection (LPCD)
- Low Power Field Detection (LPFD)
- Digital Dynamic Power Control (DDPC)
- Supports reading/writing of MIFARE® card family including MIFARE Classic® (without crypto) [1]
- Supports Apple ECP "Enhanced Contactless Polling" (feature only available for customers with Apple formal authorization)
- Transparent mode allowing implementation of customer protocols based on low-level commands (for example, B')

High-Performance Hardware

- Host interface: SPI, I^{2}C, I3C, UART [2]
- Efficient power transmission with accurate digital programmability of the output power, RF carrier amplitude and modulation shape
- Fractional-N PLL to support input clock frequency from 13.56MHz to 54.24MHz

Flexible Software Architecture

- SDK composed of firmware and software integrated in a Split Stack architecture allows complete firmware update from the host processor:
  - Modular SW stack running on the host architecture
  - FW running on the on-chip MCU for timing critical operations
- Product Support Library (PSL) with Antenna diagnostic functions such as Antenna Tunning Check
- Reader Universal Library (RUL) SDK in C for easy integration into host controllers (for example, Windows®, Linux®, bare metal MCU, RTOS)

Package

- 44-STQFN
- 33-WLCSP [3]

Applications

- IoT and NFC reader
- Access control
- Gaming
- Wearable

1. MIFARE is a registered trademark of NXP B.V

[2] Available on QFN-44 package
[3] Customer samples available, release planned later

Benefits

PTX205R Reader IC enables key improvements in customer care, such as:

RF Performance

- Patented groundbreaking architecture enables efficient power transmission for state-of-the-art reader performance and a consistently reliable user experience even in electrically noisy, metallic and space constrained integration environments
- Unique SCPA architecture combined with best-in-class receiver sensitivity simplifies antenna design, supports smaller and more compact antenna form factors, and ensures robust communication performance with minimal tuning effort

Interoperability

- All-digital RF transmitter delivers precise modulation shaping, ensuring smooth certification and consistent, standards-compliant performance
- Sine-wave driver allows efficient power output while receiver’s direct antenna connection ensures high-input sensitivity, together resulting in an extended operating range and optimal interoperability with wide range of contactless cards and mobile phones
- SCPA-based power control ensures high RF efficiency without LDO or DC-DC losses, providing stable output power in all operating conditions

Manufacturability

- Product Support Library (PSL) supports diagnostic functions such as Antenna Tuning Check, enabling early detection of assembly-related issues and helping ensure consistent RF performance across devices
- Optimized RF architecture reduces reliance on additional matching components, minimizing performance variations across production units and improving overall manufacturability

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1.1 Block Diagrams

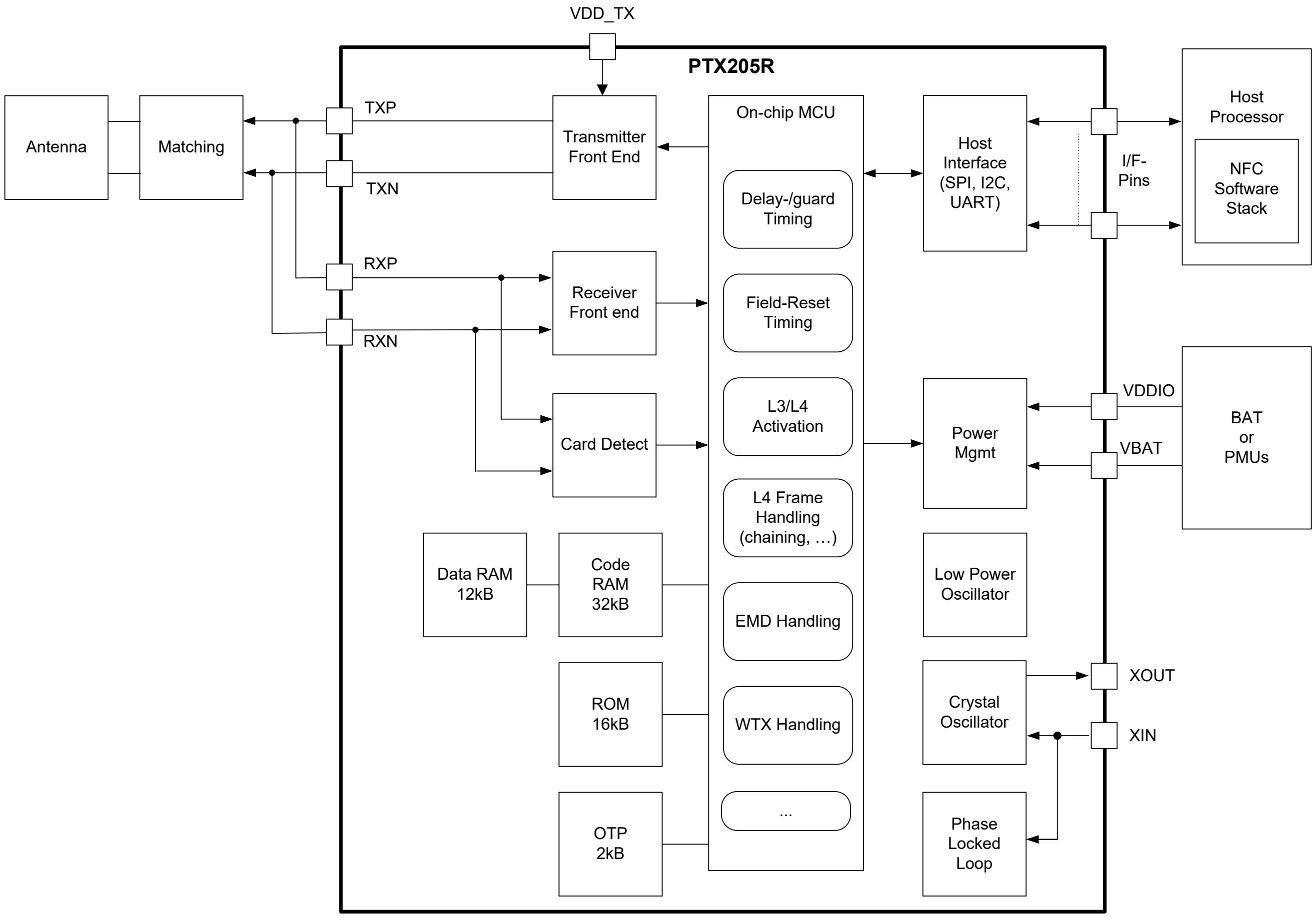


Figure 1. Hardware Block Diagram

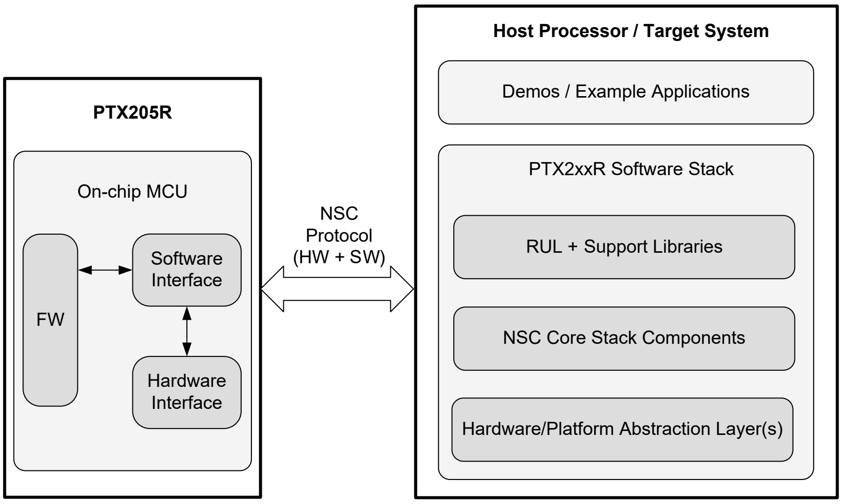


Figure 2. Software Block Diagram

2. Pin Information

2.1 Pin Assignments

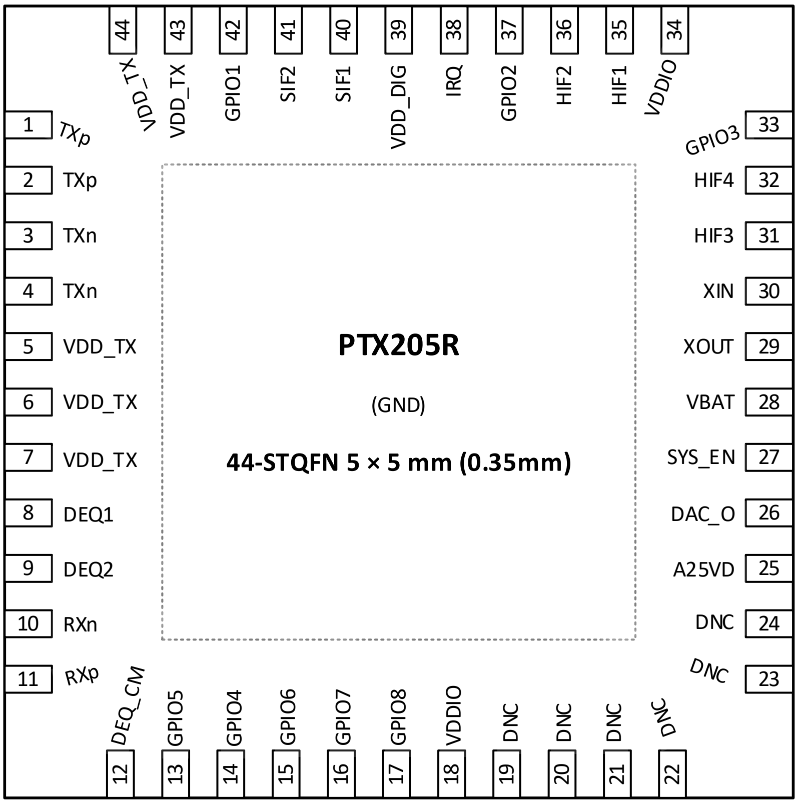


Figure 3. 44-STQFN Pin Assignments – Top View

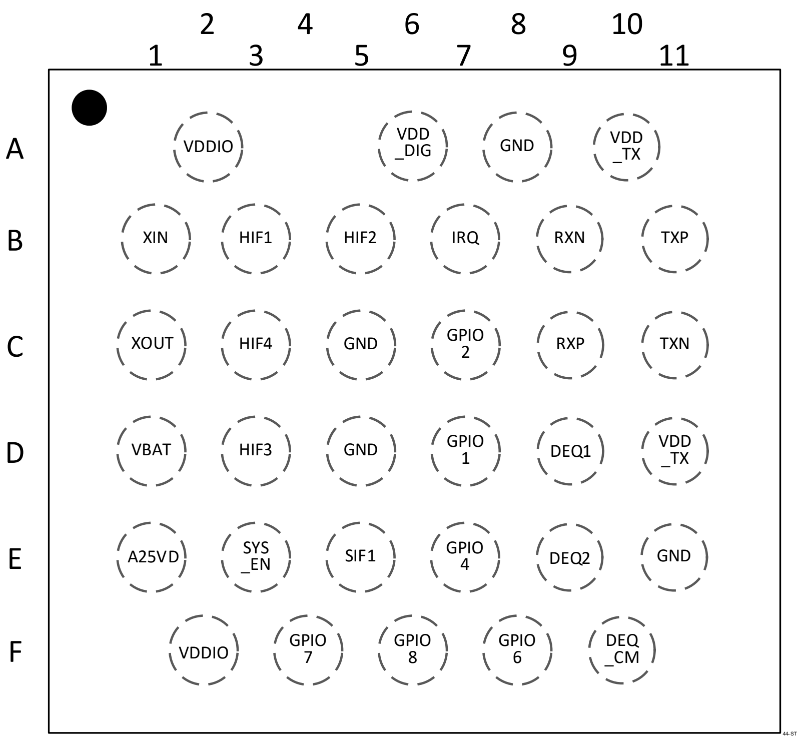


Figure 4. 33-WLCSP Pin Assignments – Top View

2.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number		Pin Name	Signal Type	Description
44-STQFN	33-WLCSP			
1, 2	B11	TXp	Analog output	Transmitter output pin, positive side.
3, 4	C11	TXn	Analog output	Transmitter output pin, negative side.
5, 6, 7, 43, 44	A10, D11	VDD_TX	Supply	Power supply for transmitter block.
8	D9	DEQ1	Analog IO	De-Qing switch circuit; leave open if not used.
9	E9	DEQ2	Analog IO	De-Qing switch circuit; leave open if not used.
10	B9	RXn	Analog IO	Receiver input, negative side.
11	C9	RXp	Analog IO	Receiver input, positive side.
12	F10	DEQ_CM	Analog output	De-Qing switch circuit common mode voltage output; leave open if not used.
13	-	GPIO5	Digital IO	General purpose digital IO pin.
14	E7	GPIO4	Digital IO	General purpose digital IO pin.
15	F8	GPIO6	Digital IO	General purpose digital IO pin.
16	F4	GPIO7	Digital IO	General purpose digital IO pin.
17	F6	GPIO8	Digital IO	General purpose digital IO pin.
18, 34	A2, F2	VDDIO	Supply	Pad supply.
19-24	-	DNC	-	Do not connect; leave open.
25	E1	A25VD	Supply	Decoupling pin for internal analog supply.
26	-	DAC_O	Analog output	AUX-DAC output.
27	E3	SYS_EN	Analog input	System enable pin.
28	D1	VBAT	Supply	Power supply for internal blocks, except transmitter.
29	C1	XOUT	Analog output	Xtal oscillator output.
30	B1	XIN	Analog input	Xtal oscillator input / Reference clock input.
31	D3	HIF3	Digital IO	I^2C/I3C: ADDR0; SPI: NSS.
32	C3	HIF4	Digital IO	I^2C/I3C: ADDR1; SPI: SCK.
33	-	GPIO3	Digital IO	General purpose digital IO pin.
35	B3	HIF1	Digital IO	I^2C/I3C: SCL; SPI: MISO; UART: TXD.
36	B5	HIF2	Digital IO	I^2C/I3C: SDA; SPI: MOSI; UART: RXD.
37	C7	GPIO2	Digital IO	General purpose digital IO pin / Reference clock input.
38	B7	IRQ	Digital output	Interrupt request to host, active high polarity.
39	A6	VDD_DIG	Supply	Decoupling pin for internal digital supply.
40	E5	SIF1	Digital input	Select interface type, bit 1.
41	-	SIF2	Digital input	Select interface type, bit 2.
42	D7	GPIO1	Digital IO	General purpose digital IO pin.
-	A8, C5, D5, E11	GND	Supply	The exposed pad is used as GND on QNF44 package.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
VBAT, VDD_TX Supply Range	-	-0.5	6	V
VDDIO, SYS_EN Supply Range	-	-0.5	3.8	V
Storage Temperature Range	T_s	-50	150	°C
Junction Temperature Range	T_j	-50	125	°C
Total Power Dissipation allowed in the Chip	P_{TOT}	-	0.6	W
Maximum Supply Current into VBAT	-	-	50	mA
Maximum Supply Current into VDD_TX	-	-	550	mA
Maximum Carrier Signal on Receiver Input Pins (differential)	$V_{IN\_RX\_diff\_MAX}$	-	76	Vpp
Maximum Input Voltage range on Digital IO Pins	V_{IN_MAX}	-0.3	3.8	V
Maximum Current into Digital IO Pins	I_{iomax}	-	4	mA
ESD Human Body Model (HBM), RF pins (TXp/TXn, RXp/RXn, DEQ1/2) 1500Ω, 100pF; JEDEC JS-001	$V_{ESD\_HBM\_RF}$	-	750	V
ESD Human Body Model (HBM), non-RF pins 1500Ω, 100pF; JEDEC JS-001	V_{ESD_HBM}	-	1500	V
ESD Charge Device Model (CDM) 1500Ω, 100pF; JEDEC JS-002	V_{ESD_CDM}	-	1000	V
Latch-Up, JESD78F	I_{LU}	100	-	mA

3.2 Thermal Specifications

Table 3. Thermal Specifications

Parameter	Package	Symbol	Condition	Typical Value	Unit
Thermal Resistance [1]	44-STQFN	θ_{JA_QFN}	Junction to ambient	31	°C/W
	33-WLCSP	θ_{JA_CSP}		26	°C/W

1. Thermal Resistance data is based on simulation of JEDEC 4-layer PCB with 9 thermal vias; for reference only

3.3 Electrical Specifications

Recommended operating conditions unless otherwise noted. VBAT = 3.3V, VDD_TX = 3.3V, Fref_clk = 27.12MHz, Typical values are at T_A = +25°C, unless otherwise specified.

Table 4. Electrical Specifications

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Temperature Range						
Ambient Temperature	T_A	-	-40	-	105	°C
Junction Temperature	T_J	-	-40	-	125	°C
Supply Voltage						
Supply Voltage on VBAT Pin	VBAT	-	2.7	3.3	5.5	V
Supply Voltage on VDD_TX Pin	VDD_TX	-	2.7	-	5.5	V
Supply Voltage on VDDIO [1]	VDDIO	Smaller or equal to VBAT	3.0	3.3	3.6	V
			1.62	1.8	1.98	V
Current Consumption						
Power-down Current Consumption	I_{PD}	VBAT = 3.3V	-	5	110[2]	uA
Standby Current Consumption on VBAT pin	I_{SB}	VBAT = 3.3V	-	8	140[2]	uA
Active Current Consumption without RF communication	I_{ACT}	VBAT = 3.3V	-	10	-	mA
Low Power Card Detection Current Consumption, 3Hz Duty-cycle[3]	I_{SB_LPCD}	VBAT = 3.3V	-	35	-	uA
Other Voltage						
System Enable (SYS_EN) Pin High-level Voltage Range	V_{SEN_H}	-	0.99	-	VDDIO	V
System Enable (SYS_EN) Pin Low-level Voltage Range	V_{SEN_L}	-	-0.3	-	0.2	V
GPIO/HIF Pins High-level Input Voltage	V_{IH}	-	VDDIO × 0.8	-	VDDIO	V
GPIO/HIF Pins Low-level Input Voltage	V_{IL}	-	-0.3	-	VDDIO × 0.2	V
GPIO/HIF Pins Low-level Output Voltage[4]	V_{OL}	-	0	-	0.45	V
GPIO/HIF Pins High-level Output Voltage[5]	V_{OH}	VDDIO = 1.8V	1.35	-	VDDIO	V
		VDDIO = 3.3V	2.4	-	VDDIO	V
GPIO Pins Output Sink Current	I_{O_L}	VDDIO = 1.8V	-	-	2	mA
		VDDIO = 3.3V	-	-	4	mA
GPIO Pins Output Source Current	I_{O_H}	VDDIO = 1.8V	-	-	2	mA
		VDDIO = 3.3V	-	-	4	mA
Receiver / Transmitter						
Maximum Signal on Transmitter Output Pins[6]	$V_{OUT\_TX\_diff}$	Differential carrier	-	-	70	V_{pp_diff}
Maximum Signal on Receiver Input Pins[6]	$V_{IN\_RX\_diff}$	Differential carrier	-	-	70	V_{pp_diff}
Transmitter Serial Output Capacitance[6]	C_{out_tx}	Differential serial equivalent	-	245	-	pF

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Test Condition</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr>
<tr><td colspan="7">Oscillator</td></tr>
<tr><td>Reference Clock Input Frequency</td><td>-</td><td>-</td><td>-</td><td>27.12</td><td>-</td><td>MHz</td></tr>
<tr><td>Reference Clock Frequency Tolerance[2]</td><td>-</td><td>-</td><td>-</td><td>±50</td><td>-</td><td>ppm</td></tr>
<tr><td>Equivalent Serial Resistance[2]</td><td>ESR</td><td>-</td><td>-</td><td>-</td><td>150</td><td>Ohm</td></tr>
<tr><td rowspan="2">Load Capacitance Programmable Range [6]</td><td>C_{L_min}</td><td rowspan="2">Programable, 0.5pF step</td><td>-</td><td>3.7</td><td>-</td><td rowspan="2">pF</td></tr>
<tr><td>C_{L_max}</td><td>-</td><td>19.2</td><td>-</td></tr>
<tr><td colspan="7">Reference Input Frequency</td></tr>
<tr><td>Reference Clock Input Frequency [6]</td><td>-</td><td></td><td>13.56</td><td>-</td><td>54.24</td><td>MHz</td></tr>
<tr><td rowspan="2">Reference Clock Input Voltage Low
(square wave)</td><td rowspan="2">$V_{ref\_clk\_low}$</td><td>XIN as reference input [6]</td><td>0</td><td>-</td><td>0.22</td><td>V</td></tr>
<tr><td>GPIO2 as reference input</td><td>-0.3</td><td>-</td><td>VDDIO × 0.2</td><td>V</td></tr>
<tr><td rowspan="2">Reference Clock Input Voltage High
(square wave)</td><td rowspan="2">$V_{ref\_clk\_high}$</td><td>XIN as reference input [6]</td><td>0.88</td><td>-</td><td>1.2</td><td>V</td></tr>
<tr><td>GPIO2 as reference input</td><td>VDDIO × 0.8</td><td>-</td><td>VDDIO</td><td>V</td></tr>
<tr><td>Reference Clock Frequency Tolerance</td><td>-</td><td>-</td><td>-</td><td>±50</td><td>-</td><td>ppm</td></tr>
</table>

1. The VDDIO voltage should always be smaller or equal to VBAT voltage.
2. Specified by design, not tested in production.
3. Current consumption in LPCD mode highly depends on the matching impedance and the output power configured. For more information, see the PTX205R Low Power Card Detection Application Note.
4. V_{OL} measurement condition: 2mA source current with VDDIO = 1.8V; 4mA source current with VDDIO = 3.3V.
5. V_{OH} measurement condition: 2mA sink current with VDDIO = 1.8V; 4mA sink current with VDDIO = 3.3V.
6. Evaluated by characterization, not tested in production.

4. Functional Description

The PTX205R is a high-performance NFC controller with best-in-class receiver sensitivity. Its patented sine-wave output architecture and Direct Antenna Connection (DiRAC) technology enable highly efficient RF power transfer to the NFC antenna. In addition, DiRAC significantly improves the Signal-to-Noise Ratio (SNR) at the receiver input, enhancing overall system robustness. These unique capabilities make the PTX205R an ideal choice for applications requiring superior RF performance, extended operating range, and strong interoperability.

In addition to the NFC Reader/Writer functionality, the PTX205R also supports Card Emulation (CE) and Peer-to-Peer modes.

4.1 System Features

As an NFC controller, the PTX205R offers a comprehensive set of system features that support customer system development, enable performance and power optimization, simply standards compliance, and facilitate system-level production testing.

4.1.1 Digital Dynamic Power Control (DDPC)

The device's Digital Dynamic Power Control (DDPC) feature dynamically adjusts the RF field strength to maintain stable system performance while optimizing overall power consumption. This feature also helps streamline the standard compliance process, reducing the need for extensive manual tuning during certification.

When DDPC is enabled, the PTX205R automatically applies predefined output levels based on the measured Received Signal Strength Indicator (RSSI). The RSSI value reflects the loading effect introduced by the counterpart device in the reader's RF field, allowing the system to adjust output behavior accordingly.

With the Configuration Tool provided by Renesas, users can easily define the high and low switching thresholds as well as hysteresis parameters.

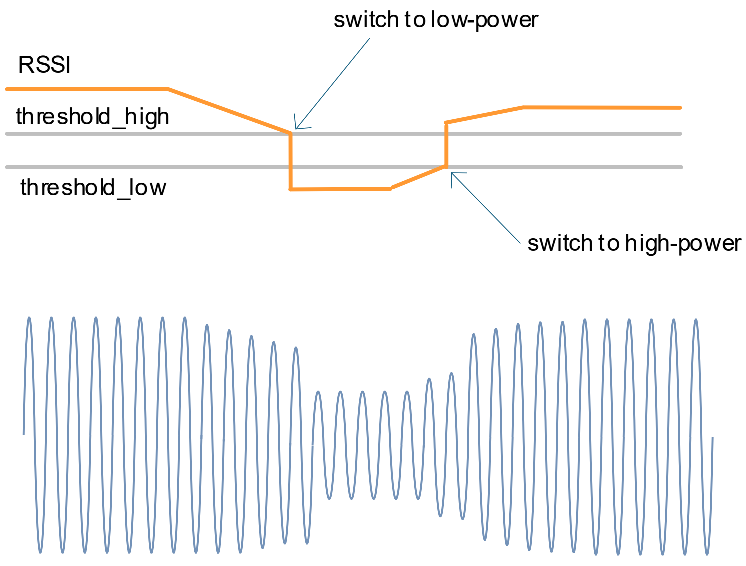


Figure 5. DDPC Concept

For more information, see the PTX2xxR Config Tool User Manual.

4.1.2 Digital Wave Shaping

The Wave Shaping feature is used to fine-tune the rising and falling edges of the modulation envelope for dedicated customer antenna systems. This allows easy compliance with various standards and helps correct common waveform issues such as overshoot, undershoot, and humps.

For each modulation edge, the PTX205R provides seven shaping cycles for precise adjustment. Leveraging the device's innovative sine-wave transmitter architecture, the wave-shaping effect is applied directly to the signal at the antenna, ensuring highly accurate control of the wave modulation envelope.

4.1.3 Low Power Card Detection (LPCD)

To optimize the power consumption for low-power applications, the PTX205R supports the Low Power Card Detection (LPCD) feature (see Figure 6), which enables the device to determine whether a counterpart NFC device or PICC (Proximity Inductive Coupling Card) is within communication range without initiating a full, power-intensive polling sequence. Normal polling is only started when a PICC is detected; otherwise, the PTX205R returns to Standby mode. The interval for LPCD is a configurable parameter and can be optimized for different applications.

During LPCD operation, only a subset of the RF front-end hardware blocks is activated. Additionally, the active time of the Transmitter (the most power consuming block) is kept to minimum. Comparing with normal polling mode, which executes communication commands according to standard and requires the Transmitter to be active for at least several milliseconds, the transmitter in LPCD mode is only active for less than 50µs.

With the split-stack architecture of PTX205R, LPCD is performed by the device autonomously. Once LPCD mode is configured, the Host MCU can enter its own low-power state. If a PICC is detected, the PTX205R automatically notifies the host. Depending on the application, the system can also be configured to notify the host whenever an object enters or leaves the operating area, without requiring a full polling cycle.

Power consumption in LPCD mode can be further optimized by adjusting key parameters such as the RF output amplitude during detection and the LPCD interval, providing additional flexibility for energy-constrained systems.

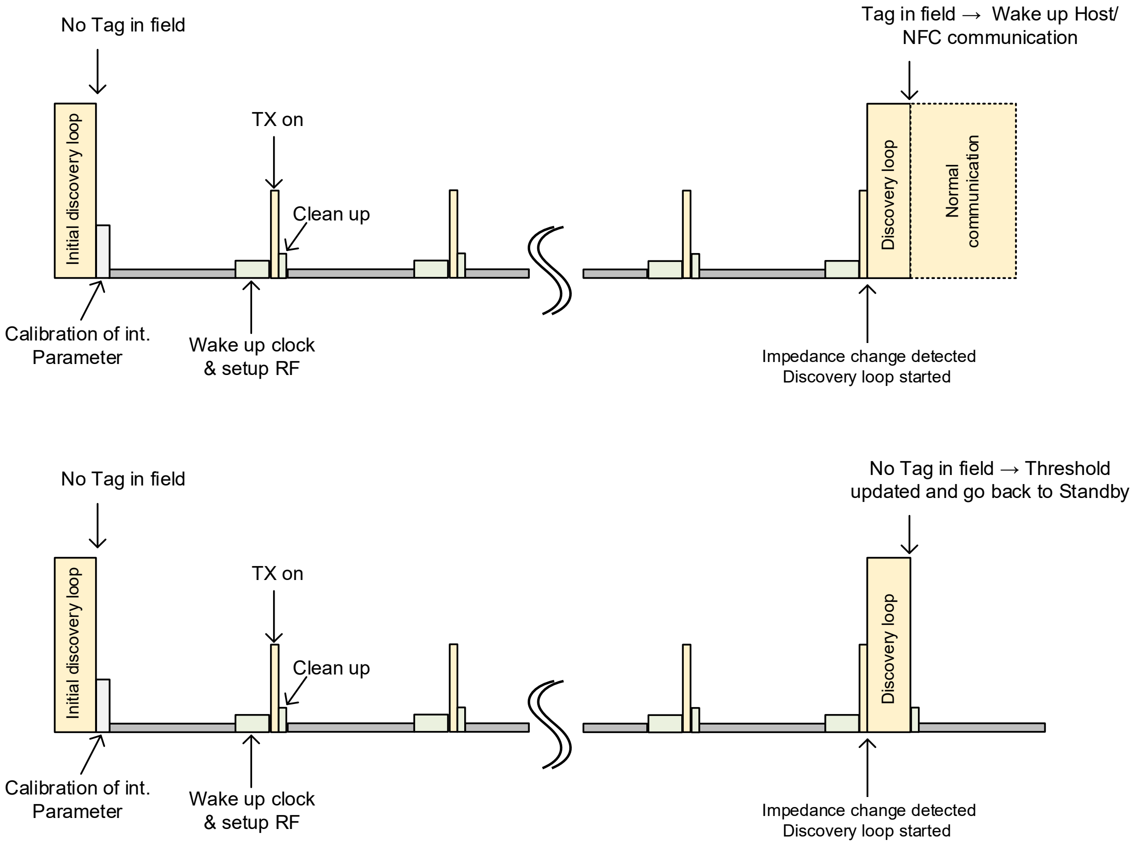


Figure 6. Low-Power Card Detection Examples

4.1.4 Low Power Presence Check

Together with LPCD, the Low Power Presence Check (LPPC) feature is also supported by the PTX205R. LPPC is essential for applications requiring continuous monitoring to ensure that a PICC remains within the communication range after the initial connection has been established.

On the PTX205R, the LPPC function is implemented by adjusting the LPCD detection threshold and masking out the already-detected PICC once initial communication is complete. This approach enables verification of the physical presence of the PICC without maintaining active NFC communication, resulting in significantly reduced power consumption.

While the PICC remains within the RF field, the PTX205R performs periodic LPCD cycles. Only when the PICC is removed or a new PICC enters the field, the device detects this change and report it to the host.

Figure 7 shows how the Low Power Presence Check works on PTX205R.

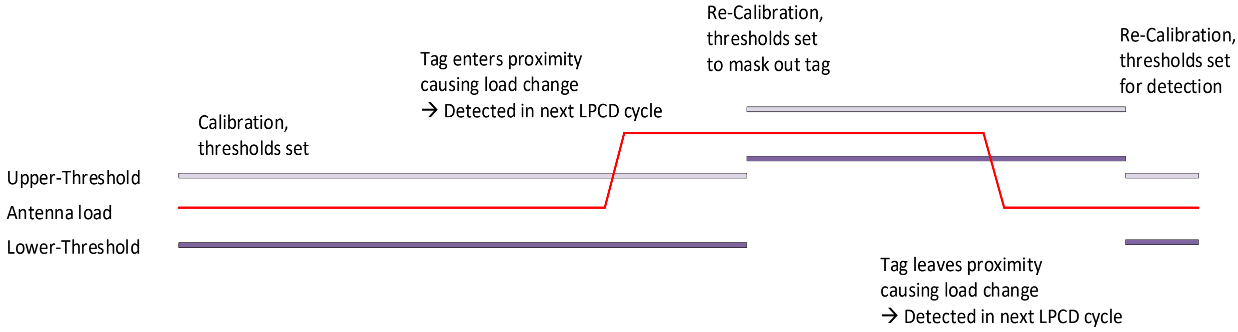


Figure 7. Low Power Presence Check

4.1.5 Antenna Tuning Check

The PTX205R is equipped with a Product Support Library (PSL) that enables advanced customer support features, including antenna diagnostic functions such as Antenna Tuning Check. It can be used to determine the resonant frequency and Q-factor for the complete system, including the attached antenna and matching components.

Antenna Tuning Check allows users to determine the resonant frequency and Q-factor of the entire system, including the connected antenna and all matching components. In addition, Antenna Matching Check allows evaluation of the received signal strength at carrier frequency.

With Antenna Tuning Check feature, the correct antenna connection and tuning in final application can be ensured without the need for external measurement equipment.

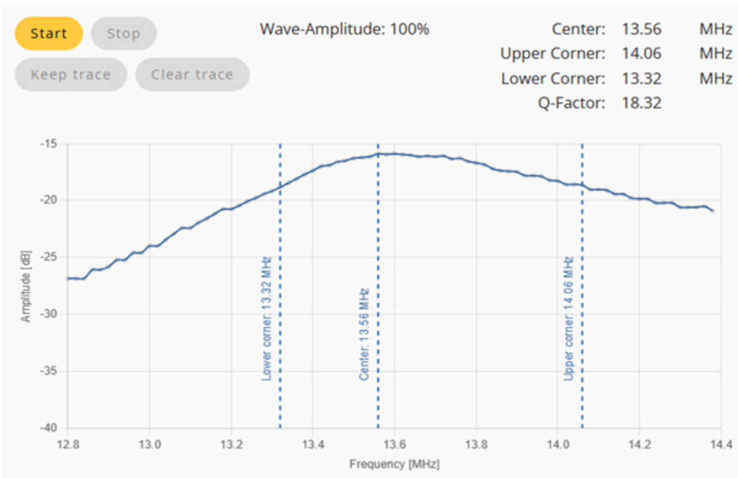


Figure 8. Antenna Q-Measurement Example using Renesas Config Tool

4.1.6 Low Power Field Detection (LPFD)

In Card Emulation (CE) mode, the PTX205R features an ultra-low power Wake-Up Receiver (WURX) block for RF field detection. This feature allows the device to keep high-power blocks disabled until a valid RF field is detected, significantly reducing overall power consumption. The WURX is frequency-selective and responds only to 13.56MHz RF signals, ensuring accurate and reliable activation.

Additionally, the detection threshold is user-configurable, enabling further optimization for specific applications.

4.1.7 De-Qing Feature

To optimize Card Mode performance and simplify standard compliance without compromising on Reader performance, the PTX205R features a frequency tuning circuit to change the antenna center frequency and the quality factor on dedicated customer antenna systems.

4.1.8 Over-Temperature Protection

The PTX205R integrates an on-chip temperature sensor that continuously monitors the die temperature as a safety mechanism. In case an over-temperature event occurs, the transmitter is automatically disabled. Additionally, the PTX205R notifies the Host and goes to Reset state.

4.2 System Architecture

The PTX205R is an NFC controller that includes both hardware and software components. It uses a split-stack software architecture, enabling flexible adaptation to the requirements of different target applications. This flexibility is achieved through an optimized software interface and ready-to-use Software Stack running on the Host Controller.

The Reader Universal Library (RUL) provided by Renesas offers a single, universal API supporting a broad range of NFC functionalities. IoT applications (see Figure 9) run on the host controller and make use of the function provided by the Renesas RUL, which abstracts all interactions with the NFC hardware through the RUL API.

The Renesas solution is fully modular, portable across multiple platforms, and can be extended with additional capabilities to support custom features when required.

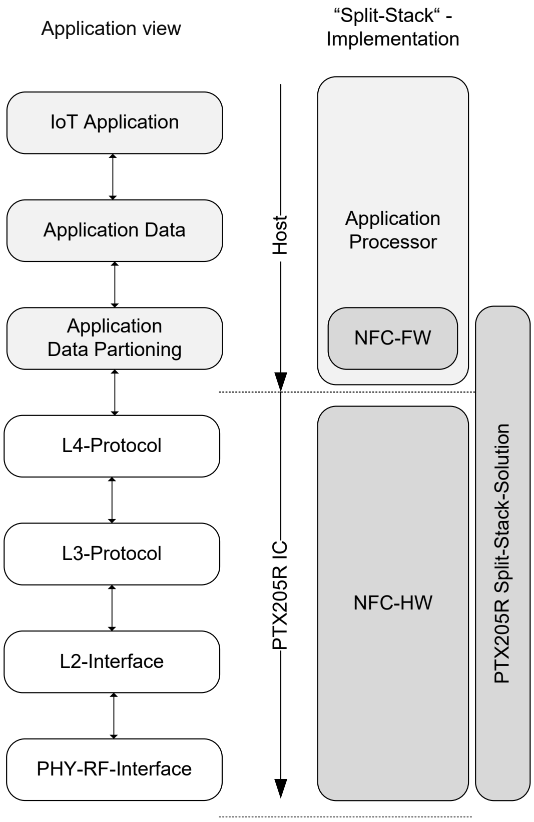


Figure 9. System Architecture to Show Interface with PTX205R for IoT Application

4.3 Power Management

The power management unit (PMU) is the central circuit of the PTX205R, responsible for generating all required internal supply voltages and reference currents. It also manages transitions between the device's various energy states, ensuring efficient operation under different system conditions.

4.3.1 Power Supply Concept

The PTX205R has five externally accessible supply domains, three of which must be externally supplied and two are used for connection to decoupling capacitors:

4.3.1.1 VBAT

VBAT is the main supply pin from which all internal functional blocks, except the transmitter, are supplied. To operate the IC, this supply must always be present. In battery-based systems this pin would normally be connected to the battery.

4.3.1.2 VDD_TX

VDD_TX is the exclusive power supply pin to the transmitter. The voltage required on this pin is proportional to the output power of the transmitter block. In battery-based systems, this pin can be connected to a battery or to a DC-DC converter to supply a constant voltage, thus providing constant transmitter output power.

The current on VDD_TX is dependent on the output amplitude configuration and impedance of the matching circuit together with antenna. The voltage supplied on VDD_TX is completely independent of the voltage on VBAT.

4.3.1.3 VDDIO

VDDIO is the supply pin for the digital IO pads, DIG1-DIG8 and the HIF/SIF-pins. It must be present during start-up for proper host interface definition and afterward for host interface communication.

In power-down mode, the voltage can be removed from these pins to save system power. The state of the SYS_EN pin is ignored when VDDIO is unpowered, and the previous chip state is maintained.

Note: The VDDIO pin supply voltage must never exceed VBAT.

4.3.1.4 A25VD

This internally generated intermediate analog supply is routed to pin A25VD and must be connected to an external decoupling capacitor. No external load should be connected to this pin.

4.3.1.5 VDD_DIG

The internally generated core supply is routed to pin VDD_DIG and is to be connected to an external decoupling capacitor. No external load should be connected to this pin.

4.3.2 Supply Ramp-Up Sequence

The PTX205R does not require a special power supply sequencing. VBAT and VDDIO can be enabled simultaneously, while VDD_TX can be applied later. The following graph shows how the different supplies can be applied.

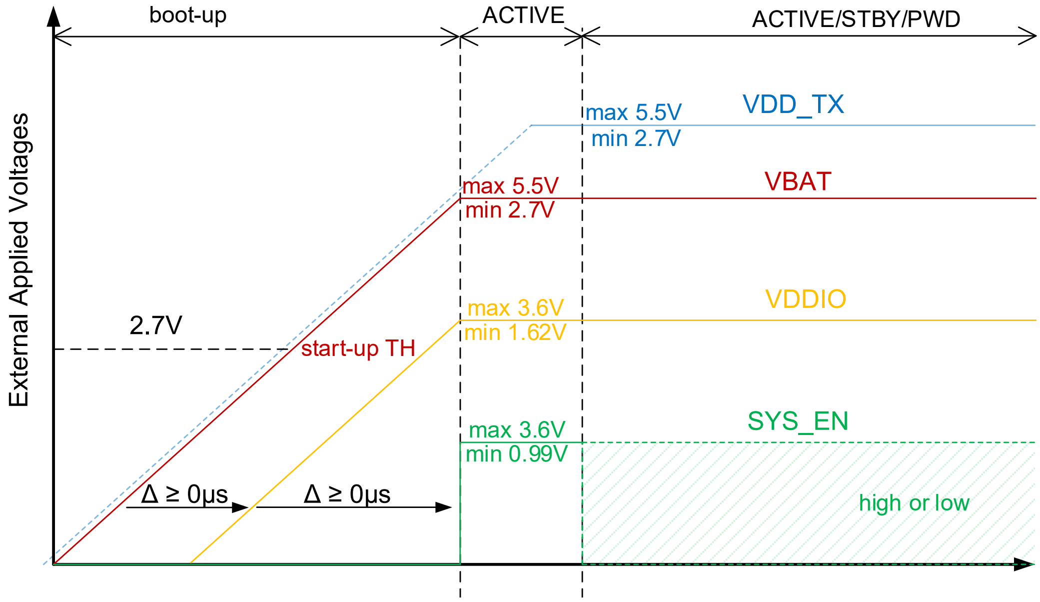


Figure 10. Supply Ramp-Up Sequence

4.3.3 Energy States

To support the implementation of flexible system power consumption profiles, the PTX205R offers different energy states, each being a trade-off between functionality and power consumption (see Figure 11).

4.3.3.1 Active Mode

This is the main operating mode of the PTX205R in which all internal supply domains are powered and all internal clocks are running. This mode is initially activated by applying a logic-high level at SYS_EN pin while VDDIO is powered.

4.3.3.2 Power-Down (PD) Mode

For maximum power saving, the PTX205R can be set to power-down mode by applying a logic-low at the SYS_EN pin while having VDDIO powered. In this mode, the device consumes its lowest power and does not react to any external event. In power-down mode, the internal state of the PTX205R is held in reset.

To exit PD, VDDIO must be powered and then the SYS_EN pin driven high. This causes the device to enter active mode.

4.3.3.3 Standby (STBY) Mode

Standby mode is autonomously enabled by the device's firmware configurations. In this mode, the device has low power consumption and can be woken up by selected external events and subsequently enters Active mode. In standby mode, the internal state and memory content are retained.

Events triggering the wakeup of the device from standby mode include (see Figure 11):

- Activity on Host interface
- Timer for Polling/LPCD procedure
- RF field detection in HCE mode

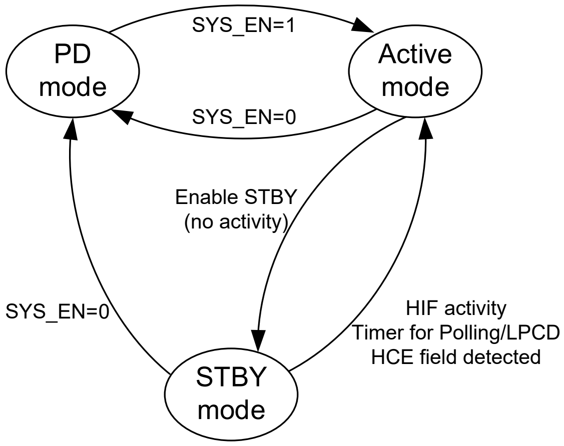


Figure 11. Energy State Diagram

4.3.4 SYS_EN

The SYS_EN pin is used to determine the PTX205R's power state between active and power-down mode.

SYS_EN features an integrated glitch filter to prevent unintentional power-state transitions. To reliably enter power-down mode, SYS_EN must be held low for a minimum duration of 40µs.

Note: The SYS_EN pin input voltage must never exceed VDDIO.

4.4 Clock Concept

The clock concept of the PTX205R features two main clock domains: the system clock in active mode generated from a frac-N PLL and the standby clock from an internal low-power oscillator.

4.4.1 Phase Locked Loop (PLL)

A fractional-N PLL produces the core clock that is used to derive all the needed internal clocks. This clock must be accurately synthesized for the device to communicate with other NFC devices. The PLL is designed to lock to an external reference clock.

The reference clock for the PLL can be provided either from an external clock source, or from the internal crystal oscillator.

4.4.1.1 External Reference Clock

An external reference clock, when used, can be connected either to the XIN pin or to GPIO2 depending on the voltage range. Frequencies in the range from 13.56MHz to 54.24MHz are supported.

Note: The PTX205R will boot without the external reference clock being available.

4.4.1.2 Crystal Oscillator (XOSC)

The internal crystal oscillator is designed for crystal types with a resonant frequency of 27.12MHz. To use it, the crystal should be placed between the XIN and XOUT pins. The oscillator will also work with other crystals around this frequency. For additional support, contact Renesas.

The PTX205R features programmable internal load capacitors on XIN and XOUT to support a wide range of crystals while reducing the number of required external components.

4.5 Contactless Interface

On the PTX205R, lower-level functionalities up to communication framing are available through the Contactless frontend, and higher-level functionalities are implemented via the RF-subsystem of the on-chip MCU (see section 4.7).

The contactless frontend of PTX205R consists of a transmitter and receiver. While the transmitter generates the RF field and amplitude-modulates the commands on the 13.56MHz RF carrier according to the selected communication type, the receiver is responsible for reception, demodulation, and signal processing of incoming commands and data.

4.5.1 Transmitter

The PTX205R supports fine adjustment of transmitter output sinusoidal amplitude independent from the transmitter supply voltage.

The transmitter supports both differential and single-ended antenna configurations, giving maximum implementation flexibility for customer applications.

4.5.2 Receiver

The receiver is based on an I/Q-architecture in the RF domain, followed by a single-baseband programmable gain amplifier (PGA), a high-performance ADC and sophisticated Digital Signal Processing (DSP). The received information is then extracted on a bit- and frame-level in digital domain to finally obtain the transmitted command/data.

Using the Configuration Tool provided by Renesas, the above mentioned parameters such as Transmitter amplitude and Receiver PGA gain can be easily optimized based on the target application.

4.6 Host Interface

The PTX205R supports SPI, I^{2}C, I3C, and UART communication interfaces, while only one interface can be enabled at a time.

The supported speed for each interface is as following:

- SPI up to 10Mbps
- I^{2}C up to 3.4Mbps
- I3C up to 12.5Mbps
- UART up to 3.4Mbps

The Host Interface of the PTX205R is designed for typical interface supply voltages used by micro-controllers at 1.8V and 3.3V, which must be supplied by the host via the VDDIO pins.

4.6.1 Host Interface Selection

The Host Interface selection is done via the configuration pins SIF1 and SIF2 at startup. A change of the pin state after boot does not have any effect on the selected interface type.

Table 5 describes the selection of the Host Interface with respect to the value at the SIF pins.

Table 5. Host Interface Selection

Host Interface	SIF2	SIF1
SPI	0	0
I^{2}C/I3C	0	1
UART [1]	1	0
RFU	1	1

1. UART interface is not supported on WLCSP-33 package.

4.6.2 Host Interface Assignment

Four pins (HIF1-HIF4) are used for the Host Interface communication. Depending on the selection, configuration and application, at least two HIF pins and up to all four are used.

Table 6 specifies the pin assignment for the Host Interface. For UART communication, only two of the four HIF pins are used during the communication.

Table 6. Host Interface Pin Assignment

Pin	SPI	I²C/I3C	UART	Internal State in Standby/Power-Down
HIF1	MISO	SCL	TXD	Pull-Up
HIF2	MOSI	SDA	RXD	Pull-Up
HIF3	NSS	ADDR0	-	HiZ
HIF4	SCK	ADDR1	-	HiZ

4.6.3 IRQ

Every communication is driven by the Host. To initiate a transfer from the PTX205R to the Host, a dedicated IRQ pin (active High) is available, which the device uses to notify the Host of its intent to communicate.

In Standby and Power Down mode, the IRQ pin is internally pulled low.

4.6.4 SPI

The PTX205R implements a standard SPI interface supporting SPI mode 0 (CPOL = 0, CPHA = 0). Four signal lines are used for communication:

- Not-Slave-Select (NSS) – Active-low input to select the device. A communication is initiated by pulling NSS low. When NSS is high the data output MISO is disabled.
- Serial Clock (SCK) – Clock input for the SPI interface.
- Master-Out-Slave-In (MOSI) – Serial data line from host (master) to the PTX205R. Data is registered at positive edge of the clock.
- Master-In-Slave-Out (MISO) – Serial data line from the PTX205R to host (master). Data is shifted on negative edge of the clock.

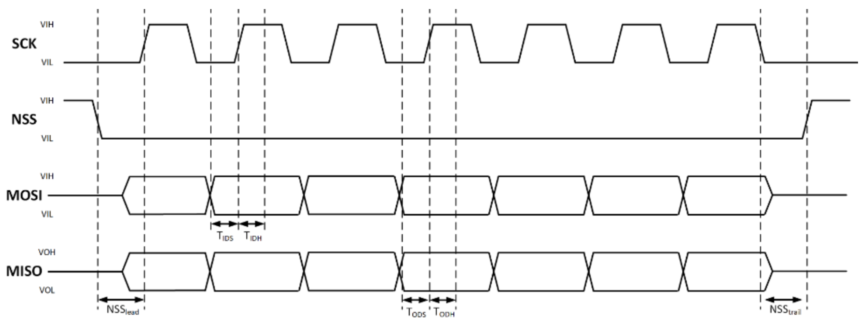


Figure 12. SPI Mode

Data transfers must always be byte aligned, in other words, the number of bits transmitted is a multiple of 8. Furthermore, the minimum numbers of bytes per frame are 3 (1 header byte + 2 length byte) and frames must be transmitted at once – without pulling NSS high in between.

Further timing characteristics for the SPI interface are specified in Table 7.

Table 7 SPI Timing Characteristics

Symbol	Description	Minimum	Typical	Maximum	Unit
F_{sck}	SPI Clock frequency	-	-	10	MHz
DC_{SCK}	SPI clock input duty cycle	40	-	60	%
NSS_{lead}	NSS setup time	50	-	-	ns
NSS_{trail}	NSS hold time	50	-	-	ns
T_{ODS}	Data output setup time	10	-	-	ns
T_{ODH}	Data output hold time	10	-	-	ns
T_{IDS}	Data input setup time	10	-	-	ns
T_{IDH}	Data input hold time	10	-	-	ns

1. Timing in Table 7 is based on characterization; valid for SPI mode 0 with VDDIO = 1.8V and 3.3V.

4.6.5 I²C and I3C

The PTX205R supports both I²C and I3C communications. While the I²C interface operates up to 3.4Mbps, the I3C interface operates up to 12.5Mbps.

Selection of communication protocol is handled by the I²C/I3C Controller as specified in the MIPI I3C standard.

4.6.5.1 I²C

The I²C interface provided by PTX205R is according to the revision 6 of NXP I²C-bus specification. The following modes are supported by the device:

- Standard-mode (Sm), with a bit rate up to 100kbps
- Fast-mode (Fm), with a bit rate up to 400kbps
- Fast-mode Plus (Fm+), with a bit rate up to 1Mbps
- High-speed mode (Hs-mode), with a bit rate up to 3.4Mbps

The PTX205R supports static 7-bit addressing, where the two LSBs of the device's I²C address can be configured via the pins HIF3 and HIF4 at start-up. In contrast, the upper 5 bits are fixed to 10011(b), resulting in an address between 0x4C and 0x4F.

Table 8. I²C Address Selection Depending on HIF Pin Setting

7bit I²C Address	HIF4	HIF3
0x4C	0	0
0x4D	0	1
0x4E	1	0
0x4F	1	1

4.6.5.2 I3C

The PTX205R has an I3C interface that operates up to 12.5Mbps. The implementation is according to MIPI I3C specification and supports all mandatory I3C target features.

The I3C interface of PTX205R supports only SDR mode (HDR is not supported).

4.6.5.3 I²C/I3C Selection

The PTX205R supports I²C/I3C interface selection upon boot by the system's SIF pins. By default, a static address is assigned, and the device answers to I²C messages with the matching address.

To operate in I3C mode, a dynamic address must be assigned by the host controller. Once assigned to a dynamic address, the PTX205R operates in I3C mode until system reset.

4.6.6 UART

The PTX205R with QFN package supports 2-wire UART communication (together with IRQ line) up to 3.4Mbps. Since there is no common clock reference for the UART interface, the data-rate reference must be very accurate.

A transaction from the Host must start with a Start-of-Frame (SOF) symbol (that is, one byte with value 0x55). The response from the PTX205R does not contain SOF.

After boot, baud-rate detection is enabled and accepts data rates of 9.6kbps or 115.2kbps. Once the clock system is configured correctly, data rate up to 3.4Mbps can be used.

4.7 On-Chip MCU

To meet both present and future requirements of contactless systems, especially regarding transaction time, the PTX205R provides a broad set of higher-level features, including ISO-DEP frame composition/decomposition, automatic frame retransmission, WTX handling, EMD handling, and more.

These functions are implemented in the firmware, which is downloaded to the PTX205R's code-memory and executed on the on-chip MCU.

In combination with the Software Stack running on the Host, this split-stack architecture delivers excellent execution speed while maintaining flexibility through support for updates and upgrades.

4.7.1 Device Control Firmware

4.7.1.1 FW Download Mechanism

Before enabling the on-chip MCU, the device's firmware must be downloaded to the code-memory of the PTX205R. This is done by the Software Stack via the Host Interface during boot-up.

4.7.1.2 On-Chip MCU Enable

Activation of the on-chip MCU is achieved by writing the corresponding command to the device. Once enabled, it has access to all internal status information as well as the configuration mechanisms.

The on-chip MCU accepts NSC (NFC-Soft-Controller) commands for handling internal tasks. This is managed automatically by the Software Stack provided by Renesas.

4.7.1.3 Soft-Reset

The PTX205R provides a soft-reset functionality that resets all digital blocks and disables all analog blocks (that is, the same condition as after boot).

4.8 NFC Soft-Controller (NSC) Interface

To provide functions for device configuration as well as data communication, an optimized on-chip software interface, referenced as NSC interface, is implemented. The NSC interface is implemented by the firmware and is command-response based. The data packages between the PTX205R and the host are called NSC messages, and the protocol related header bytes are added by the on-chip MCU automatically.

The NSC interface is only used internally and its functions are called by the upper layer SW-stacks. Renesas provides these SW-stacks (Reader Universal Library) on top of the NSC interface, which enables a quick and easy integration of the PTX205R into the target applications.

4.9 Software Interface: Reader Universal Library (RUL)

The Reader Universal Library (RUL) is an API-based Software Development Kit (SDK) controlling all functions of the PTX205R hardware and provides ready-to-go high-level contactless protocol implementations. The SDK is delivered in C-source code that can be easily integrated into the customer end-application software implementation. It delivers compact and integrated C-functions (APIs) to run the specified protocols and all relevant hardware configurations of the IC along with administrative commands.

The architecture of the PTX205R RUL SDK consists of two components:

- The RUL C-library function calls (APIs) running on the host MCU and built on top of the on-chip NSC interface software functions.
- The NSC on-chip firmware (fixed in binary format), downloaded to the PTX205R and implements all timing-critical processes and functions. The firmware is an integrated part of the RUL SDK and is loaded to the PTX205R by dedicated RUL functions.

Both components together build the advanced Split Stack Software architecture to provide compact code and memory size, while delivering optimized overall system performance.

The RUL is interfacing to the native NSC command set of the PTX205R via the supported hardware interfaces (for example, SPI).

4.9.1 RUL Software Architecture

The RUL software architecture is split into three major blocks (see Figure 13):

- **Component** – Contains the Hardware Abstraction Layer (HAL) which abstracts the low-level access to the platform-dependent HW-peripherals of the target platform. This includes abstraction of the used host interfaces (for example, SPI) as well as access to GPIOs, timers, and certain MCU-features like enabling or disabling IRQs.
- **Product APIs** – Contains the RUL API implementation which is the main interface of the RUL SDK.
- **Application / Demos and Examples** – Contains mainly example applications to demonstrate the proper usage of the RUL and add-on APIs.

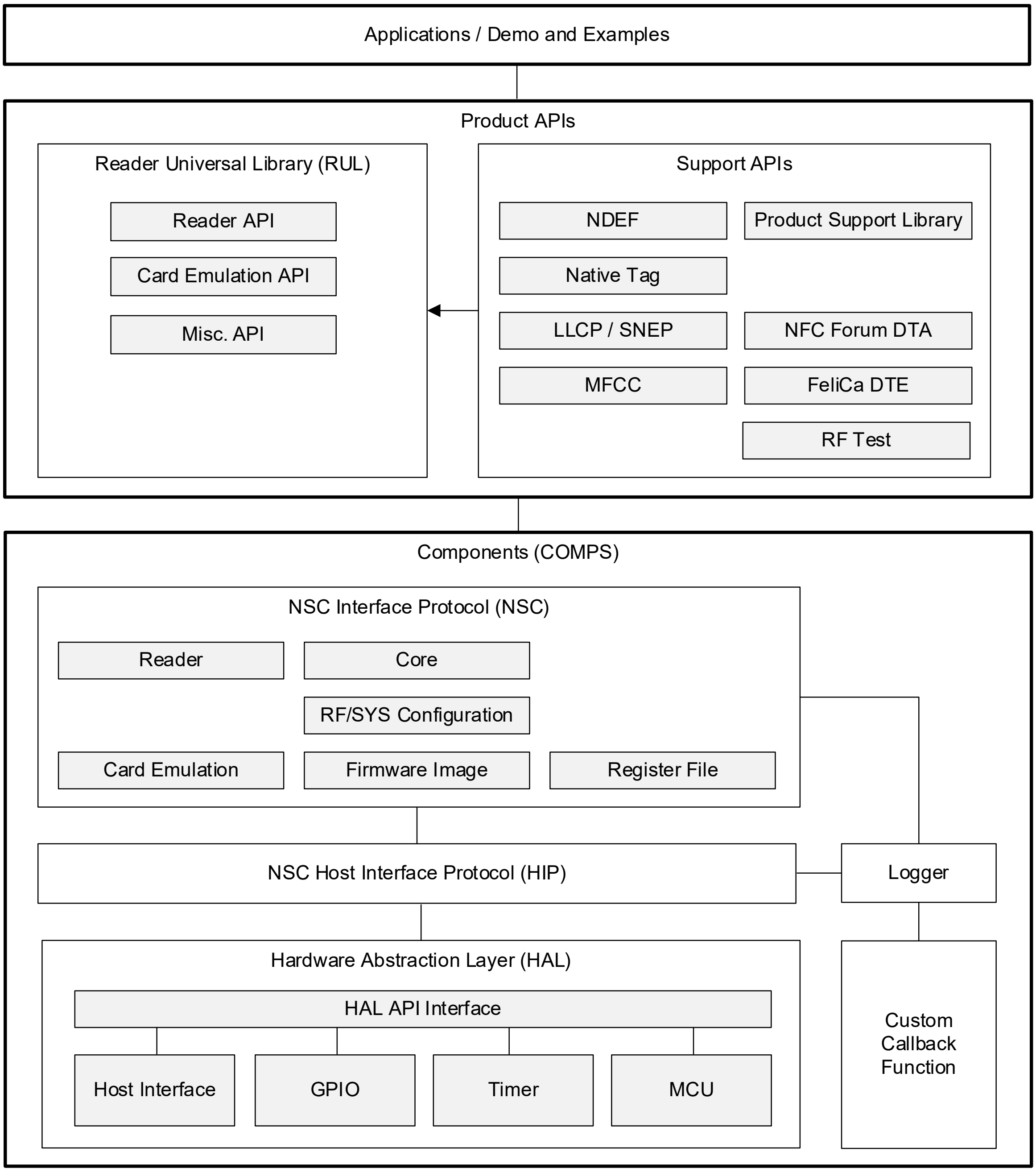


Figure 13. RUL Software Architecture

4.9.2 Protocols, Interfaces, and Features Implemented in the RUL SDK

The RUL software stack supports a large set of contactless and NFC protocols like ISO/IEC14443 Type A/B, MIFARE Classic reader interface (MFCC), ISO18092 (FeliCa), ISO/IEC15693, NFC Tag Types, and other protocols. The RUL software stack protocol implementations are based on international and industry standards and is optimized for compact-size MCU architectures.

The RUL software stack also provides functions and parameters to manage the system features such as Low Power Card Detection (LPCD), Low Power Field Detection (LPFD), Advanced Digital Wave Shaping, Digital Dynamic Power Control (DDPC), etc.

Advanced Split-Stack architecture together with the RUL software stack provide compatibility to the latest specifications, protocols, and features using the PTX205R hardware. Further developed RUL software stack, including the detailed specification and documentation of protocols and functions, are provided in the form of the RUL SDK and Software Integration notes.

4.9.3 Delivery of the RUL SDK, Software Porting, and Documentation

The RUL SDK is delivered in generic, portable C-source code that includes the fixed firmware binary code.

The RUL SDK is developed as a reference implementation on a specific target platform (for example, Renesas RA4M2 MCU series based on Arm® Cortex®-M33 core).

Detailed documentation for the RUL is provided in the form of a Software User Manual.

5. Simplified Application Schematic

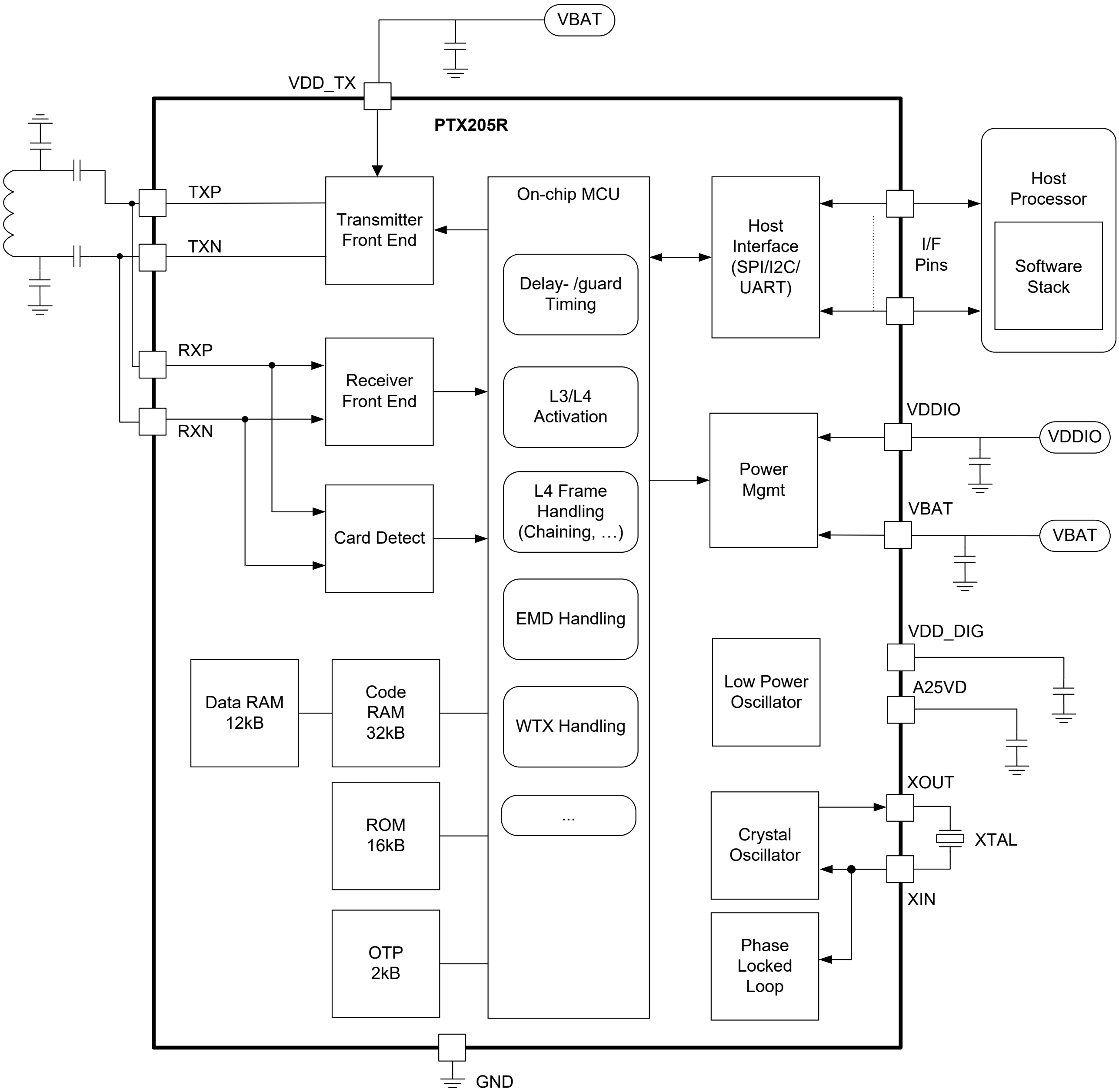


Figure 14. Simplified Application Schematic

6. Package Information

6.1 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, use a vacuum pick-up tool. In extreme cases, use plastic tweezers. However, metal tweezers are not acceptable because contact may easily damage the silicon chip.

Important: Removal will cause damage to the solder balls; therefore a removed sample cannot be reused.

WLCSP is sensitive to visible and infrared light. Take precautions to properly shield the chip in the final product.

6.2 Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

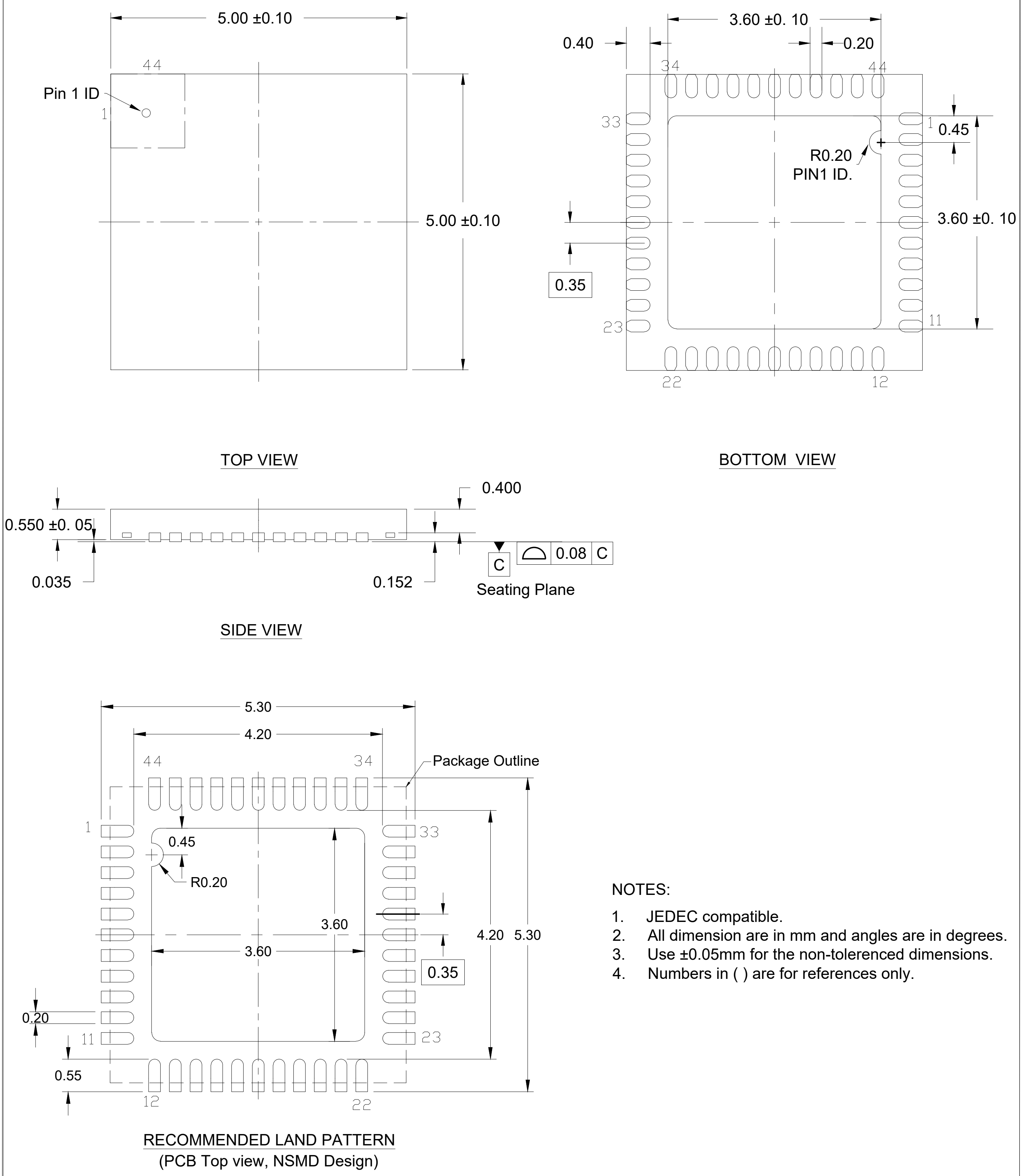
Part Number	Package Description	MSL	Carrier Type	Temperature Range
PTX205RCQ44D13	44-STQFN	3	Tape and Reel	-40°C to 105°C
PTX205RCC33D7	33-WLCSP	1	Tape and Reel	-40°C to 105°C

8. Revision History

Revision	Date	Description
1.00	Jun 10, 2026	Initial release of final datasheet.

Package Outline Drawing

Package Code:QU0044AA
44-STQFN 5.0 x 5.0 x 0.55 mm Body, 0.35mm Pitch
PSC-5041-01, Revision: 00, Date Created: Nov 17, 2023

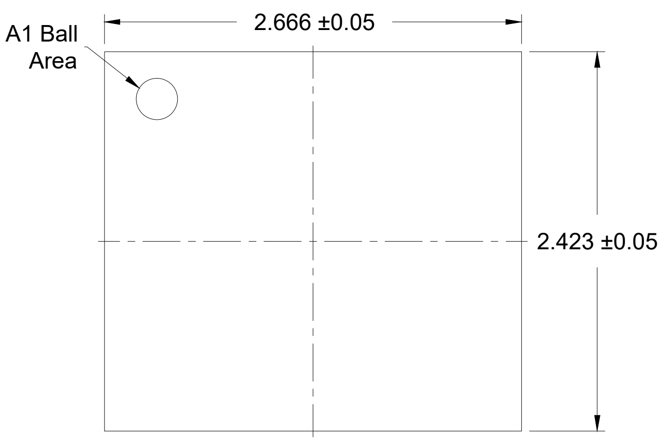


NOTES:

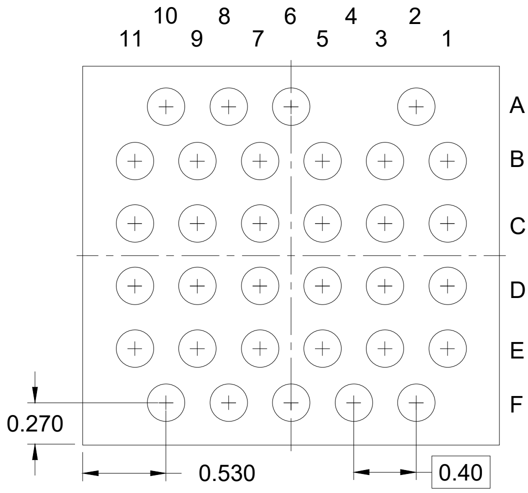
1. JEDEC compatible.
2. All dimension are in mm and angles are in degrees.
3. Use ±0.05mm for the non-tolerenced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

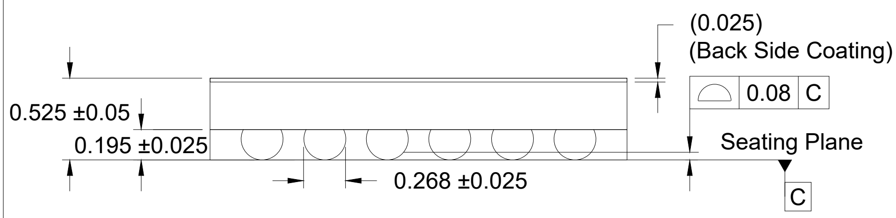
PSC-5156-01
WB0033AA
33-WLCSP 2.666 x 2.423 x 0.575 mm Body, 0.400 mm Pitch
Rev.0, Apr 09, 2025



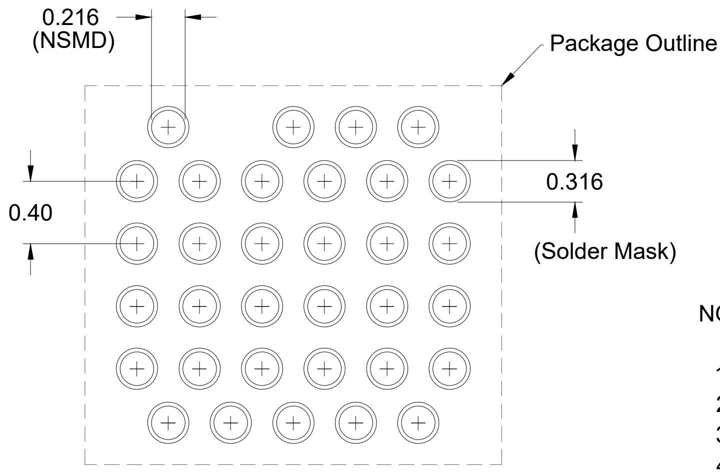
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solder ball diameter is Ø0.25 mm.
6. UBM diameter is Ø0.24 mm.

Corporate Headquarters

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Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.