PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD1615A(A), μPD1615B(A), μPD1615F(A), μPD1616F(A)

8-BIT SINGLE-CHIP MICROCONTROLLER

Description

The μPD1615A(A) Series is a member of the 78K/0 series microcontrollers. Besides a high speed, high performance CPU, these microcontrollers have on-chip ROM, RAM, I/O ports, 8-bit resolution A/D converter, timer, VAN-interface, serial interface, interrupt control, LCD-controller/driver and various other peripheral hardware.

The μPD16F15A device includes a FLASH EEPROM which can operate in the same power supply voltage range as the mask ROM version.

The details of the functions are described in the following user manuals. Be sure to read it before starting design.

μPD1615A, Subseries User's Manual : U14993EE
78K/0 Series User's Manual - Instructions : U12326EJ

Features

- Internal high capacity ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	LCD Display RAM	Internal Expansion RAM	
μPD1615A(A)	60K bytes	1024 bytes	40 bytes	1024 bytes	80-pin plastic QFP (fine pitch)
μPD1615B(A)	48K bytes	1024 bytes	40 bytes	512 bytes	80-pin plastic QFP (fine pitch)
μPD1615F(A)	32K bytes	768 bytes	40 bytes	512 bytes	80-pin plastic QFP (fine pitch)
μPD1616F(A)	32K bytes	768 bytes	–	512 bytes	80-pin plastic QFP (fine pitch)

- Instruction execution time can be changed from high speed (0.25 μs) to ultra low speed
- I/O ports: 57
- 8-bit resolution A/D converter : 4 channels
- Sound generator
- LCD-controller / driver
- VAN-Interface
- Serial interface : 2 channels
  - 3-wire mode : 1 channel
  - UART mode : 1 channel
- Timer : 5 channels
- Supply voltage : V_{DD} = 4.0 to 5.5 V

Application

Multifunction display, steering control , climate control etc.

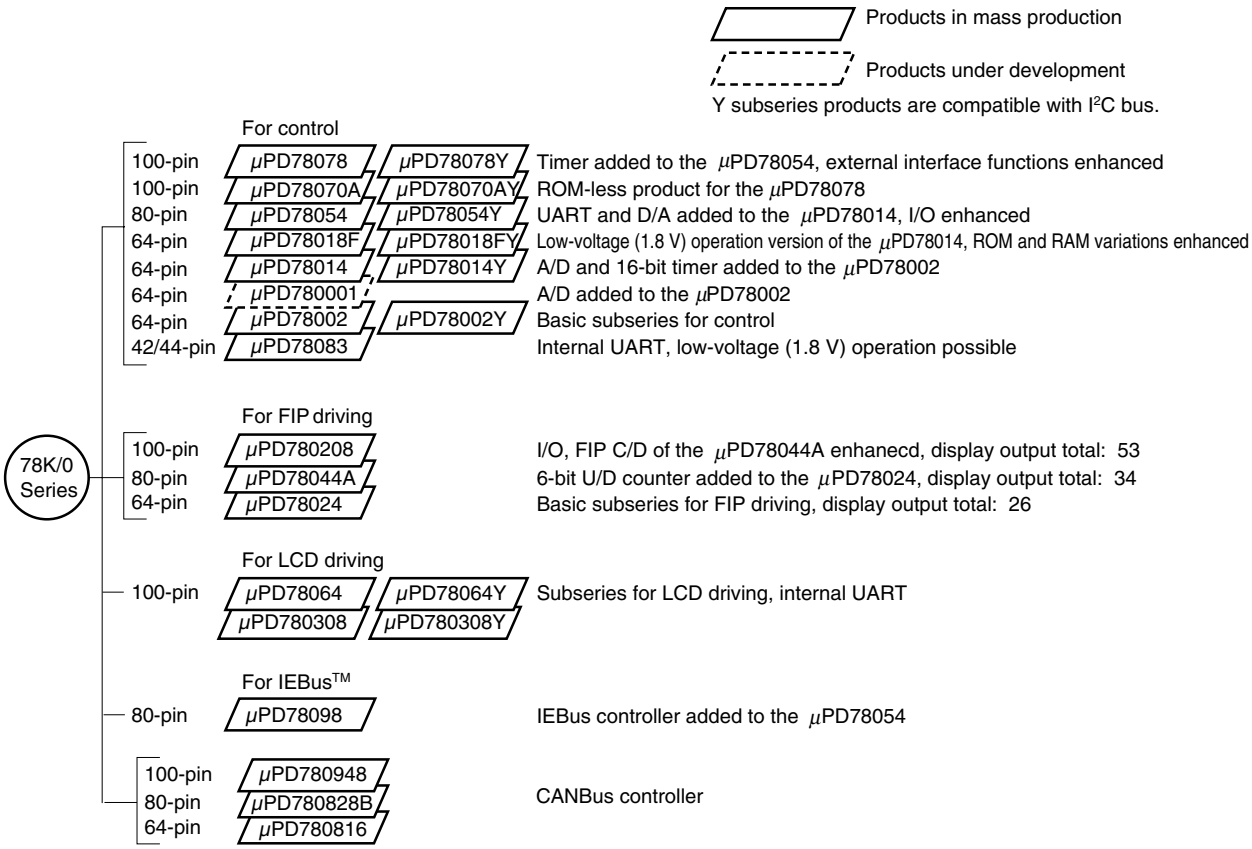
Document No. U14981EE1V0DS00
Date : November 2000

Ordering Information

Part Number	Package
μPD1615AGC(A)-xxx-8BT	80-pin plastic QFP (14 x 14 mm, resin thickness 1.4 mm)
μPD1615BGC(A)-xxx-8BT	80-pin plastic QFP (14 x 14 mm, resin thickness 1.4 mm)
μPD1615FGC(A)-xxx-8BT	80-pin plastic QFP (14 x 14 mm, resin thickness 1.4 mm)
μPD1616FGC(A)-xxx-8BT	80-pin plastic QFP (14 x 14 mm, resin thickness 1.4 mm)

78K/0 Series Development

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Overview of Functions

Item \ Part Number		μPD1615A	μPD1615B	μPD1615F	μPD1616F
Internal memory	ROM	60 Kbytes	48 Kbytes	32 Kbytes	32 Kbytes
	Internal high-speed RAM	1024 bytes	1024 bytes	768 bytes	768 bytes
	LCD Display RAM	40 bytes	40 bytes	40 bytes	-
	Internal Expansion RAM	1024 bytes	512 bytes	512 bytes	512 bytes
Memory space		64 Kbytes			
General registers		8 bits x 32 registers (8 bits x 8 registers x 4 banks)			
Instruction cycle		On-chip instruction execution time selective function			
	When main system clock selected	0.25 μs/0.5 μs/1 μs/2 μs/4 μs (at 8 MHz)			
	When subsystem clock selected	122 μs (approx. 32 KHz)			
Instruction set		• 16-bit operation • Multiplication/division (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD adjustment, etc.			
I/O ports		Total : 57 • CMOS input : 4 • CMOS I/O : 53			
A/D converter		• 8 bit resolution x 4 channels			
Serial Interface		• 3-wire mode : 1 channel • UART mode : 1 channel			
Timer		• 16 bit timer / event counter : 1 channel • 8 bit timer / event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel			
Timer output		2 (8-bit PWM output x 2)			
Clock output		62.5 KHz, 125 KHz, 250 KHz, 500 KHz, 1 MHz, 2 MHz, 4 MHz, 8 MHz (at main system clock of 8.0 MHz)			
Sound Generator		1 channel (as separate or composed output)			
LCD Controller/Driver		40 seg x 4 COM (only μPD1615A/1615B/1615F)			
VAN		1 channel			
Vectored interrupts	Maskable interrupts	Internal : 15 External : 3			
	Non-maskable interrupts	Internal : 1			
	Software interrupts	Internal : 1			
Supply voltage		V_{DD} = 4.0 V to 5.5 V			
Package		80-pin plastic QFP (14 mm x 14 mm)			

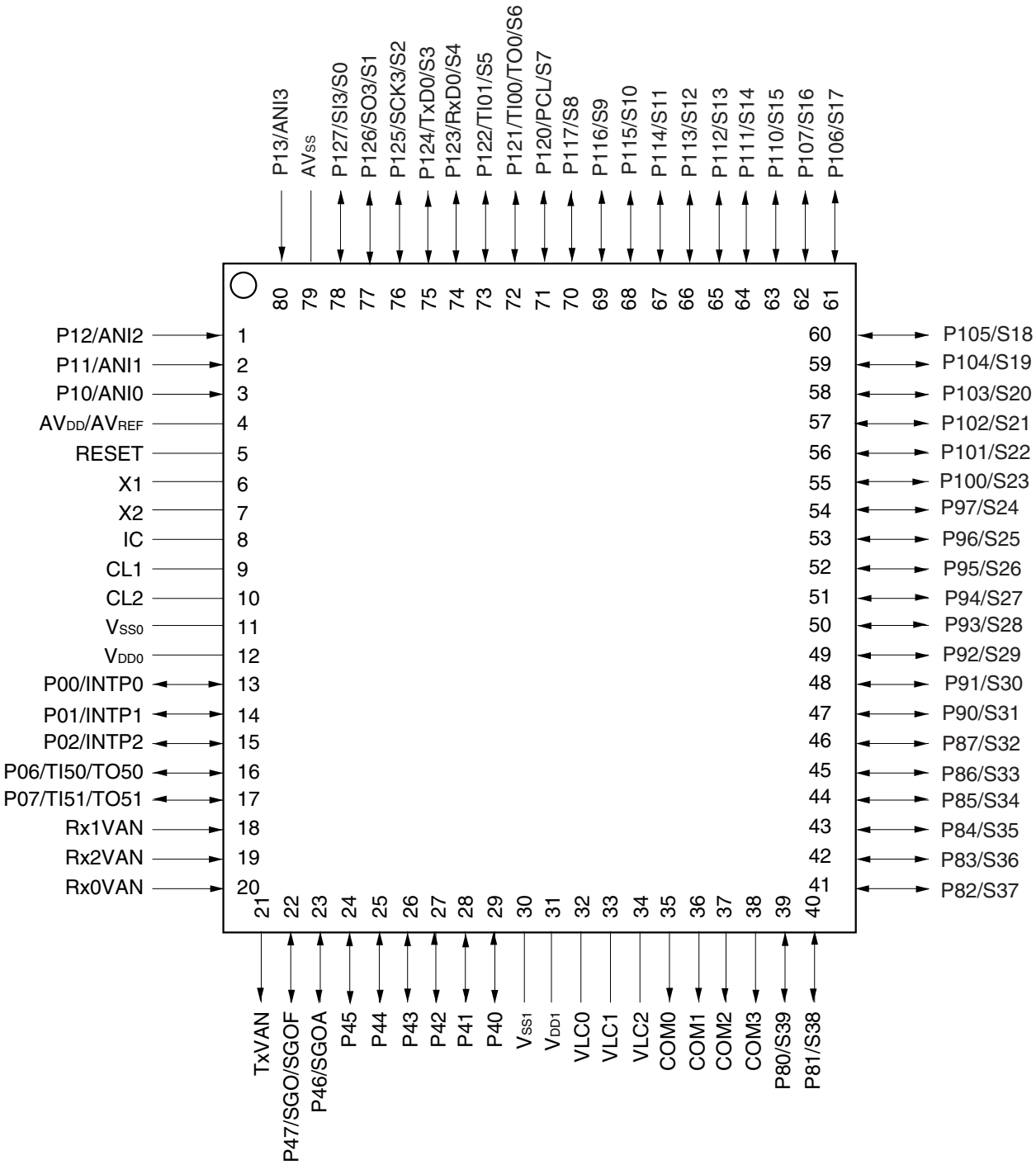
Contents

1. Pin Configuration (Top View)

80-pin plastic QFP (14 x 14 mm)

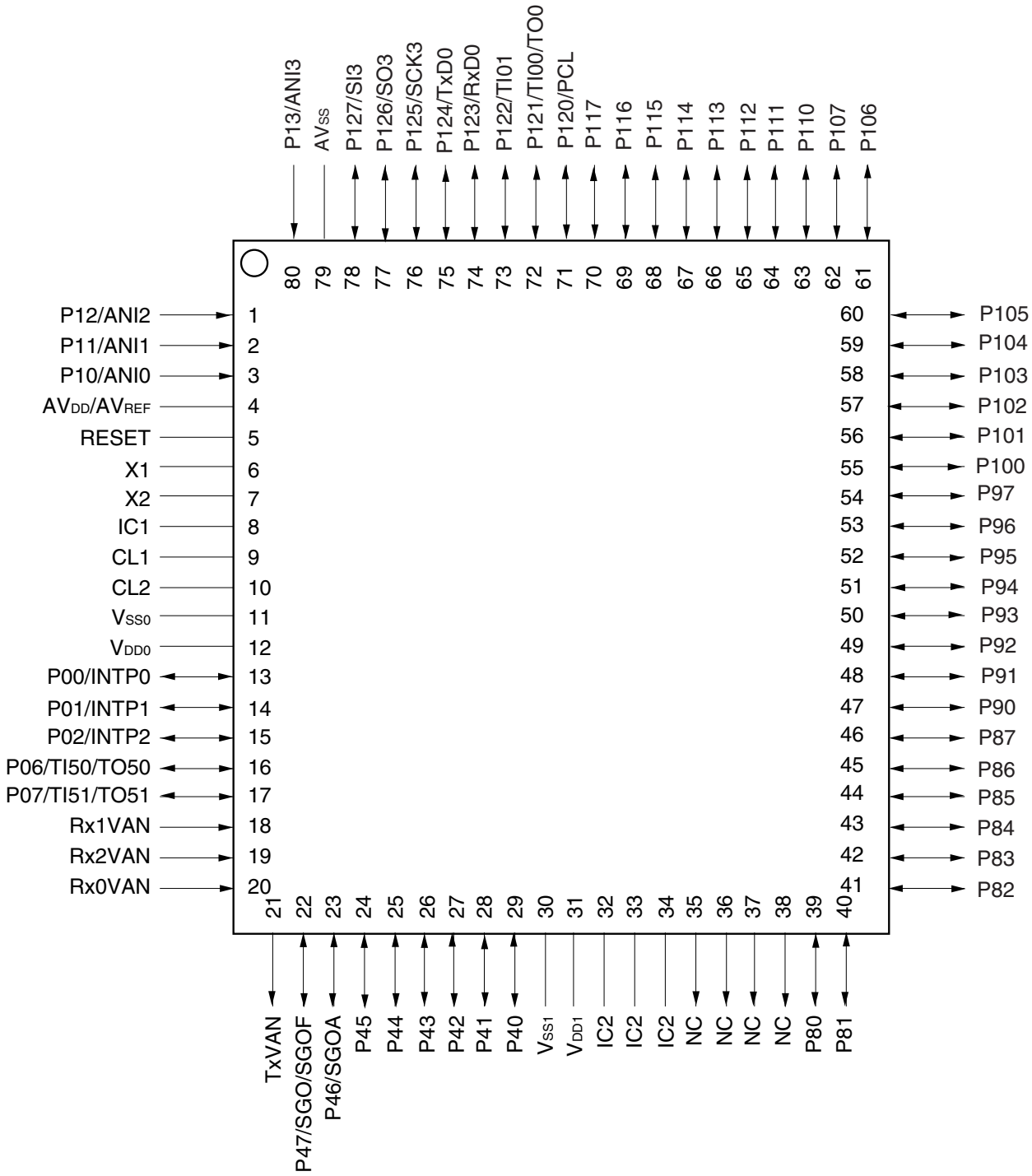
μPD1615AGC(A)-xxx-8BT
μPD1615BGC(A)-xxx-8BT
μPD1615FGC(A)-xxx-8BT
μPD1616FGC(A)-xxx-8BT

Figure 1-1: Pin Configuration μPD1615A(A), μPD1615B(A), μPD1615F(A)



Cautions: 1. Connect IC (internally connected) pin directly to V_{SS}.
2. AV_{SS} pin should be connected to V_{SS}.
3. AV_{DD}/AV_{REF} pin should be connected to V_{DD}.

Figure 1-2: Pin Configuration μPD1616F(A)



Cautions:
1. **Connect IC1 (internally connected) pin directly to V_{SS}.**
2. **AV_{SS} pin should be connected to V_{SS}.**
3. **AV_{DD}/AV_{REF} pin should be connected to V_{DD}.**
4. **Connect IC2 (internally connected) pin directly to V_{DD}.**
5. **NC (not connected).**

Pin Identifications

P00 to P02, P06, P07 : Port0
P10 to P13 : Port1
P40 to P47 : Port4
P80 to P87 : Port8
P90 to P97 : Port9
P100 to P107 : Port10
P110 to P117 : Port11
P120 to P127 : Port12
INTP0 to INTP2 : External Interrupts
TI00, TI01, TI50, TI51 : Timer Input
TO0 , TO51, TO52 : Timer Output
Rx0VAN, Rx1VAN, Rx2VAN : VAN Receive Data
TxVAN : VAN Transmit Data
SO3 : Serial Output
SI3 : Serial Input
SCK3 : Serial Clock

RxD0 : Receive Data
TxD0 : Transmit Data
SGO : Sound Generator Output
SGOA : Sound Generator Amplitude
SGOF : Sound Generator Frequency
PCL : Programmable Clock Output
S0 to S39 : Segment Output
COM0 to COM3: Common Output
VLC0 to VLC2 : LCD output voltage pins
X1, X2 : Crystal (Main System Clock)
CL1, CL2 : RC (Subsystem Clock)
$\overline{\text{RESET}}$: Reset
ANI0 to ANI3 : Analog Input
AV_{SS} : Analog Ground
AV_{DD}/AV_{REF} : Analog Power Supply and Reference Voltage
V_{DD0}, V_{DD1} : Power Supply
V_{SS0}, V_{SS1} : Ground
IC, IC1, IC2 : Internally Connected
NC : Not Connected

2. Block Diagram

Figure 2-1: Block Diagram μPD1615A(A), μPD1615B(A), μPD1615F(A)

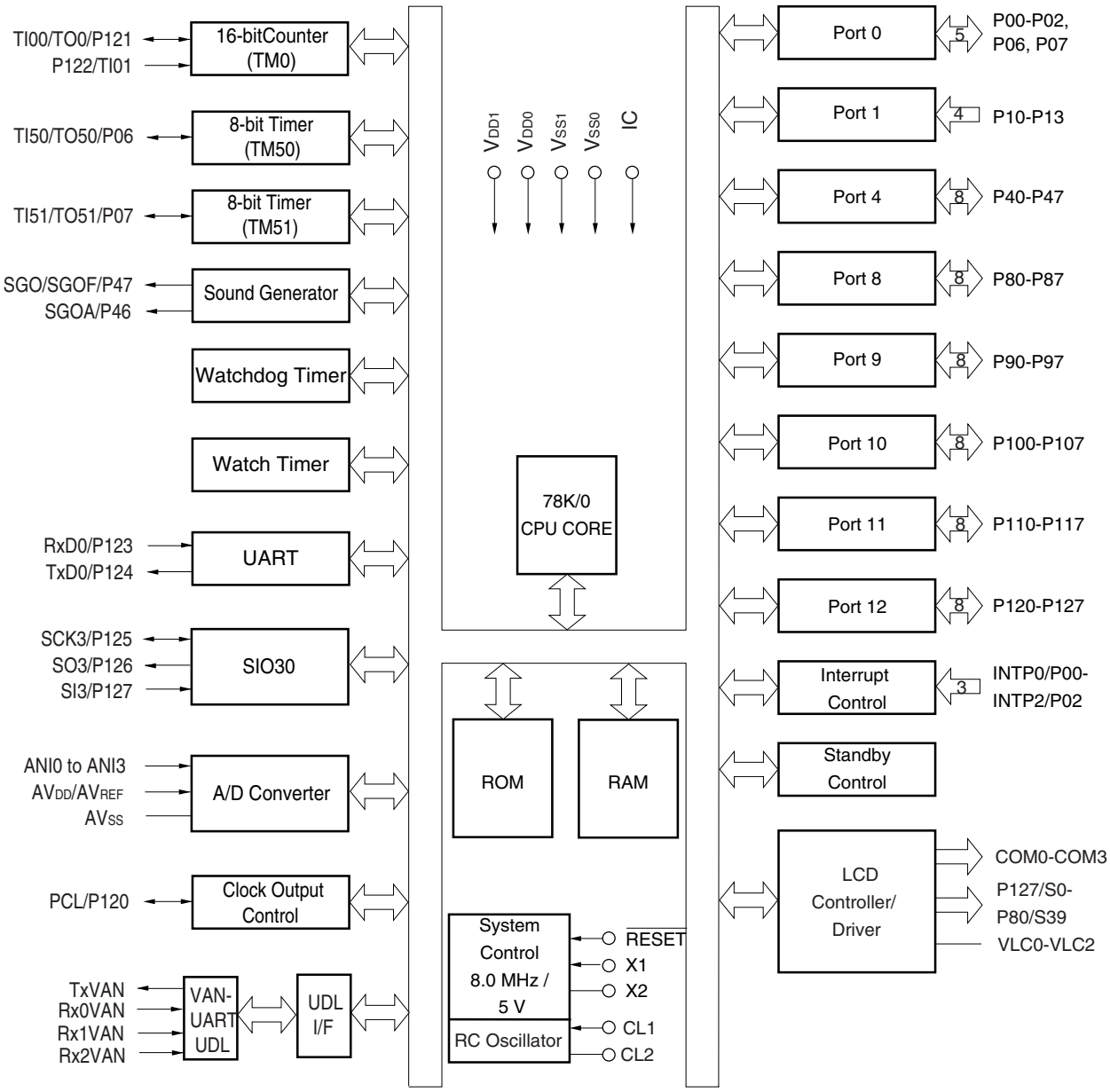
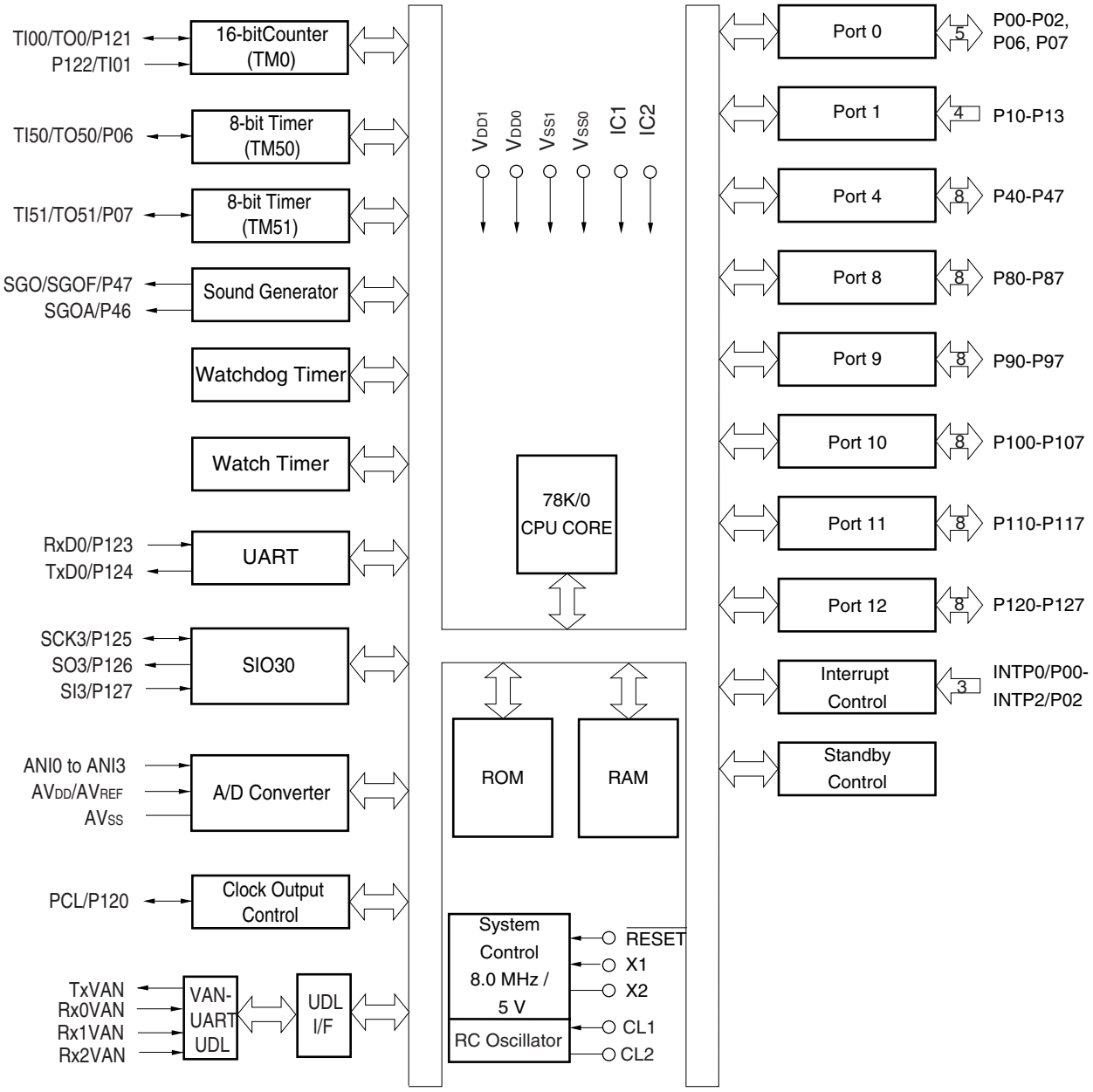


Figure 2-2: Block Diagram μPD1616F(A)



3. Pin Functions

3.1 Normal Operating Mode Pins / Pin Input/Output Types

Table 3-1-1: Pin Input/Output Types (μPD1615A(A), μPD1615B(A), μPD1615F(A))

Input / Output	Pin Name	Function	Alternate Function	After Reset
Input / Output	P00	Port 0 5 bit input / output port Input / output mode can be specified bit-wise	INTP0	Input
	P01		INTP1	Input
	P02		INTP2	Input
	P06		TI50/TO50	Input
	P07		TI51/TO51	Input
Input	P10-P13	Port 1 4 bit input port Input mode can be specified bit-wise	ANI0-ANI3	Input
Input / Output	P40	Port 4 8 bit input/output port Input / output mode can be specified bit-wise	-	Input
	P41		-	Input
	P42		-	Input
	P43		-	Input
	P44		-	Input
	P45		-	Input
	P46		SG0A	Input
	P47		SG0/SG0F	Input
Input/ Output	P80-P87	Port 8 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	S39 - S32	Input
Input/ Output	P90-P97	Port 9 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	S31 - S24	Input
Input/ Output	P100-P107	Port 10 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	S23 - S16	Input
Input/ Output	P110-P117	Port 11 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	S15 - S8	Input
Input/ Output	P120	Port 12 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	PCL/S7	Input
	P121		TI00/TO0/S6	
	P122		TI01/S5	
	P123		RxD0/S4	
	P124		TxD0/S3	
	P125		SCK3/S2	
	P126		SO3/S1	
	P127		SI3/S0	

Table 3-1-2: Pin Input/Output Types (μPD1616F(A))

Input / Output	Pin Name	Function	Alternate Function	After Reset
Input / Output	P00	Port 0 5 bit input / output port Input / output mode can be specified bit-wise	INTP0	Input
	P01		INTP1	Input
	P02		INTP2	Input
	P06		TI50/TO50	Input
	P07		TI51/TO51	Input
Input	P10-P13	Port 1 4 bit input port Input mode can be specified bit-wise	ANI0-ANI3	Input
Input / Output	P40	Port 4 8 bit input/output port Input / output mode can be specified bit-wise	-	Input
	P41		-	Input
	P42		-	Input
	P43		-	Input
	P44		-	Input
	P45		-	Input
	P46		SG0A	Input
	P47		SG0/SG0F	Input
Input/ Output	P80-P87	Port 8 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	-	Input
Input/ Output	P90-P97	Port 9 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	-	Input
Input/ Output	P100-P107	Port 10 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	-	Input
Input/ Output	P110-P117	Port 11 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	-	Input
Input/ Output	P120	Port 12 8 bit input / output port Input / output mode can be specified bit-wise This port can be used as segment signal output port or an I/O port in 1-bit units by setting port function register	PCL	Input
	P121		TI00/TO0	
	P122		TI01	
	P123		RxD0	
	P124		TxD0	
	P125		SCK3	
	P126		SO3	
	P127		SI3	

3.2 Non-Port Pins

Table 3-2-1: Non-Port Pins (μPD1615A(A), μPD1615B(A), μPD1615F(A))

Pin Name	I/O	Function	After Reset	Alternate Function Pin
INTP0	Input	External interrupts with specifiable valid edges (rising edge, falling edge, both rising and falling edges)	Input	P00
INTP1				P01
INTP2				P02
SI3	Input	Serial interface serial data input	Input	P127/S0
SO3	Output	Serial interface serial data output	Input	P126/S1
SCK3	Input/ Output	Serial interface serial clock input / output	Input	P125/S2
RxD0	Input	Asynchronous serial interface data input	Input	P123/S4
TxD0	Output	Asynchronous serial interface data output	Input	P124/S3
Rx0VAN, Rx1VAN, Rx2VAN	Input	VAN serial data input	Input	-
TxVAN	Output	VAN serial data output	Output	-
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P121/TO0/S6
TI01				P122/S5
TI50		External count clock input to 8-bit timer (TM50)		P06/TO50
TI51		External count clock input to 8-bit timer (TM51)		P07/TO51
TO0	Output	16-bit timer output	Input	P121/TI00/S6
TO50		8-bit timer output (also used for PWM output)		P06/TI50
TO51		8-bit timer output (also used for PWM output)		P07/TI51
PCL	Output	Clock output	Input	P120/S7
S0 to S7	Output	Segment signal output of LCD controller / driver	Input	P127 to P120
S8 to S15				P117 to P110
S16 to S23				P107 to P100
S24 to S31				P97 to P90
S32 to S39				P87 to P80
COM0-COM3	Output	Common signal output of LCD controller/driver	Output	-
V_{LC0} to V_{LC2}	-	LCD drive voltage	-	-
SGO	Output	Sound generator output	Input	P47/SGOF
SGOA	Output	Sound generator amplitude output	Input	P46
SGOF	Output	Sound generator frequency output	Input	P47/SGO
ANI0 to ANI3	Input	A/D Converter analog input	Input	P10 P13
AV_{DD}/ AV_{REF}	-	A/D Converter reference voltage input and power supply	-	-
AV_{SS}	-	A/D Converter ground potential. Connect to V_{SS}.	-	-
$\overline{RESET}$	Input	System reset input	-	-
X1	-	Connection for main system clock	-	-
X2	-	Connection for main system clock	-	-
CL1	Input	RC connection for subsystem clock	-	-
CL2	-	RC connection for subsystem clock	-	-
V_{DD1}, V_{DD2}	-	Positive power supply	-	-
V_{SS1}, V_{SS2}	-	Ground potential	-	-
IC	-	Internal connection. Connect directly to V_{SS} (only MaskROM version)	-	-

Table 3-2-2: Non-Port Pins (μPD1616F(A))

Pin Name	I/O	Function	After Reset	Alternate Function Pin
INTP0	Input	External interrupts with specifiable valid edges (rising edge, falling edge, both rising and falling edges)	Input	P00
INTP1				P01
INTP2				P02
SI3	Input	Serial interface serial data input	Input	P127
SO3	Output	Serial interface serial data output	Input	P126
SCK3	Input/ Output	Serial interface serial clock input / output	Input	P125
RxD0	Input	Asynchronous serial interface data input	Input	P123
TxD0	Output	Asynchronous serial interface data output	Input	P124
Rx0VAN, Rx1VAN, Rx2VAN	Input	VAN serial data input	Input	-
TxVAN	Output	VAN serial data output	Output	-
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P121/TO0
TI01				P122
TI50		External count clock input to 8-bit timer (TM50)		P06/TO50
TI51		External count clock input to 8-bit timer (TM51)		P07/TO51
TO0	Output	16-bit timer output	Input	P121/TI00
TO50		8-bit timer output (also used for PWM output)		P06/TI50
TO51		8-bit timer output (also used for PWM output)		P07/TI51
PCL	Output	Clock output	Input	P120
SGO	Output	Sound generator output	Input	P47/SGOF
SGOA	Output	Sound generator amplitude output	Input	P46
SGOF	Output	Sound generator frequency output	Input	P47/SGO
ANI0 to ANI3	Input	A/D Converter analog input	Input	P10 P13
AV_{DD}/ AV_{REF}	-	A/D Converter reference voltage input and power supply	-	-
AV_{SS}	-	A/D Converter ground potential. Connect to V_{SS}.	-	-
$\overline{RESET}$	Input	System reset input	-	-
X1	-	Connection for main system clock	-	-
X2	-	Connection for main system clock	-	-
CL1	Input	RC connection for subsystem clock	-	-
CL2	-	RC connection for subsystem clock	-	-
V_{DD1}, V_{DD2}	-	Positive power supply	-	-
V_{SS1}, V_{SS2}	-	Ground potential	-	-
IC1	-	Internal connection. Connect directly to V_{SS}	-	-
IC2	-	Internal connection. Connect directly to V_{DD}	-	-
NC	-	Not connected	-	-

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in the following table.
For the input/output circuit configuration of each type, see table.

Table 3-3-1: Types of Pin Input/Output Circuits (μPD1615A(A), μPD1615B(A), μPD1615F(A)) (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00/INTP0	8	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P01/INTP1			
P02/INTP2			
P06/TI50/TO50			
P07/TI51/TO51			
P10/ANI0	9	I	Connect directly to V_{DD} or V_{SS}
P11/ANI1			
P12/ANI2			
P13/ANI3			
P40	5	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P41			
P42			
P43			
P44			
P45			
P46/SGOA			
P47/SGO/SGOF			
P80/S39	17	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P81/S38			
P82/S37			
P83/S36			
P84/S35			
P85/S34			
P86/S33			
P87/S32			
P90/S31	17	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P91/S30			
P92/S29			
P93/S28			
P94/S27			
P95/S26			
P96/S25			
P97/S24			

Table 3-3-1: Types of Pin Input/Output Circuits (μPD1615A(A), μPD1615B(A), μPD1615F(A)) (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P100/S23	17	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P101/S22			
P102/S21			
P103/S20			
P104/S19			
P105/S18			
P106/S17			
P107/S16			
P110/S15	17	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P111/S14			
P112/S13			
P113/S12			
P114/S11			
P115/S10			
P116/S9			
P117/S8			
P120/S7/PCL	17	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P121/S6/TI00/TO0	17-C		
P122/S5/TI01	17-C		
P123/S4/RxD0	17-C		
P124/S3/TxD0	17		
P125/S2/SCK3	17-C		
P126/S1/SO3	17		
P127/S0/SI3	17-C		
COM0 COM3	18	O	Leave open
V_{LC0} V_{LC2}	-	-	Connect to V_{DD}
Rx0VAN, Rx1VAN, Rx2VAN	2	I	-
TxVAN	19	O	-
CL1	-	I	Connect to V_{DD} or V_{SS} via a resistor individually
CL2	-	-	Leave open
$\overline{\text{RESET}}$	2	I	-
AV_{DD} / AV_{REF}	-	I	Connect to V_{DD}
AV_{SS}	-	-	Connect to V_{SS}
IC	1	-	Connect directly to V_{SS}
X1, X2	-	-	-

Table 3-3-2: Types of Pin Input/Output Circuits (μPD1616F(A)) (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00/INTP0	8	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P01/INTP1			
P02/INTP2			
P06/TI50/TO50			
P07/TI51/TO51			
P10/ANI0	9	I	Connect directly to V_{DD} or V_{SS}
P11/ANI1			
P12/ANI2			
P13/ANI3			
P40	5	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P41			
P42			
P43			
P44			
P45			
P46/SGOA			
P47/SGO/SGOF			
P80	5	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P81			
P82			
P83			
P84			
P85			
P86			
P87			
P90	5	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P91			
P92			
P93			
P94			
P95			
P96			
P97			

Table 3-3-2: Types of Pin Input/Output Circuits (μPD1616F(A)) (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P100	5	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P101			
P102			
P103			
P104			
P105			
P106			
P107			
P110	5	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P111			
P112			
P113			
P114			
P115			
P116			
P117			
P120/ PCL	5	I/O	Connect to V_{DD} or V_{SS} via a resistor individually
P121/TI00/TO0	8		
P122/TI01	8		
P123/RxD0	8		
P124/ TxD0	5		
P125/ SCK3	8		
P126/SO3	5		
P127/SI3	8		
COM0 COM3	18	O	Leave open
V_{LC0} V_{LC2}	-	-	Connect to V_{DD}
Rx0VAN, Rx1VAN, Rx2VAN	2	I	-
TxVAN	19	O	-
CL1	-	I	Connect to V_{DD} or V_{SS} via a resistor individually
CL2	-	-	Leave open
$\overline{\text{RESET}}$	2	I	-
AV_{DD} / AV_{REF}	-	I	Connect to V_{DD}
AV_{SS}	-	-	Connect to V_{SS}
IC1	-	-	Connect directly to V_{SS}
IC2	-	-	Connect directly to V_{DD}
NC	-	-	Leave open
X1, X2	-	-	-

Figure 3-1: Pin Input/Output Circuits (1/2)

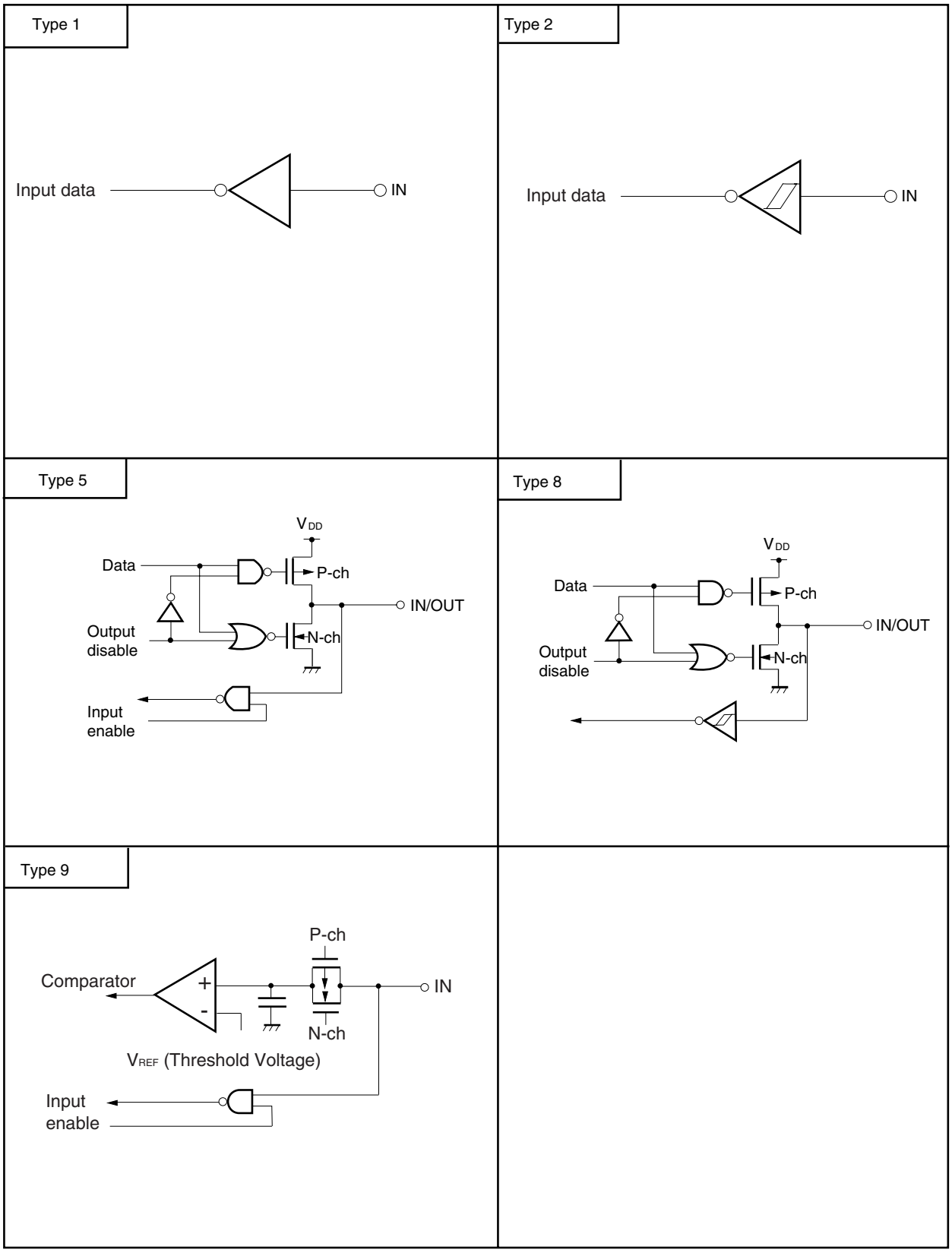
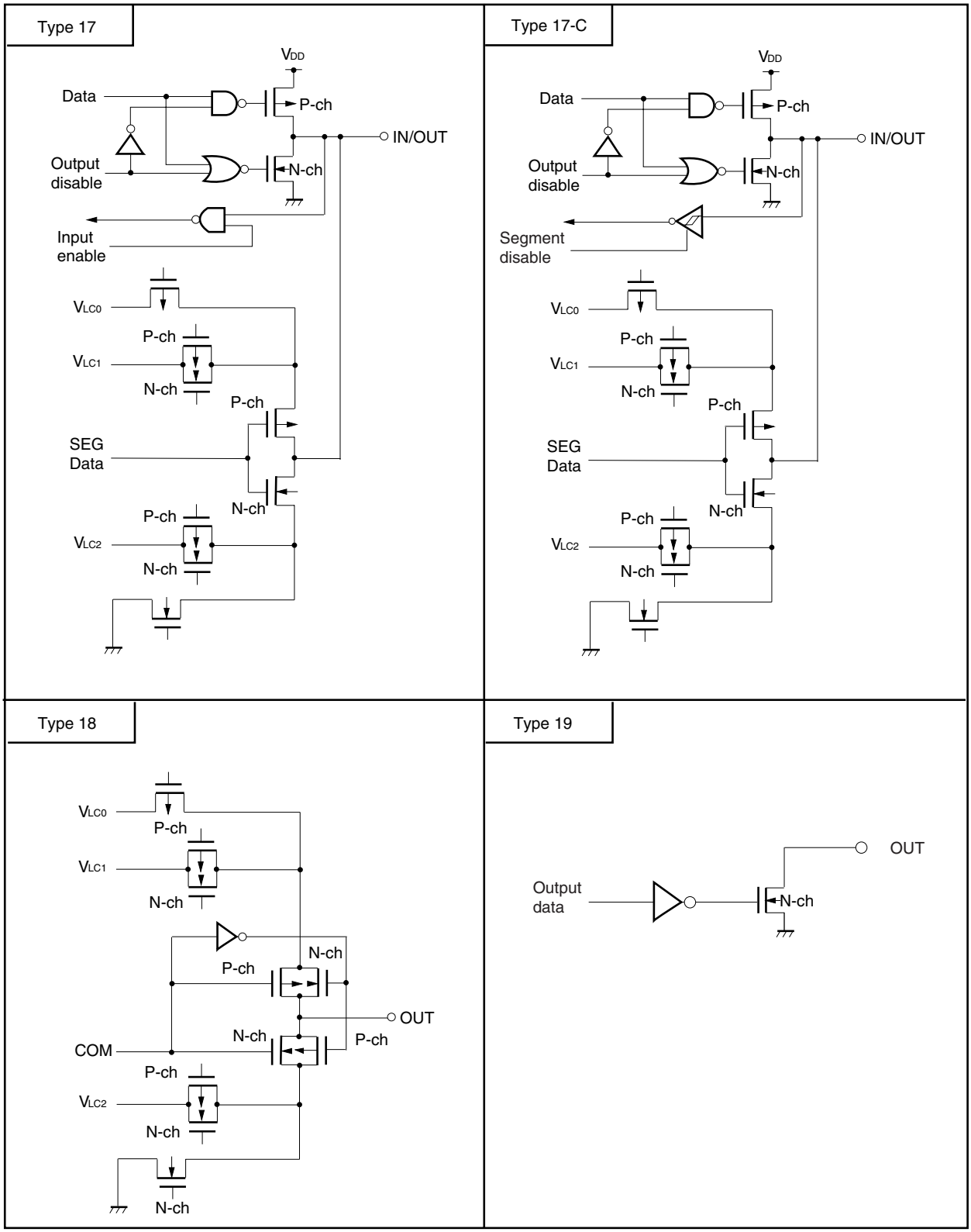


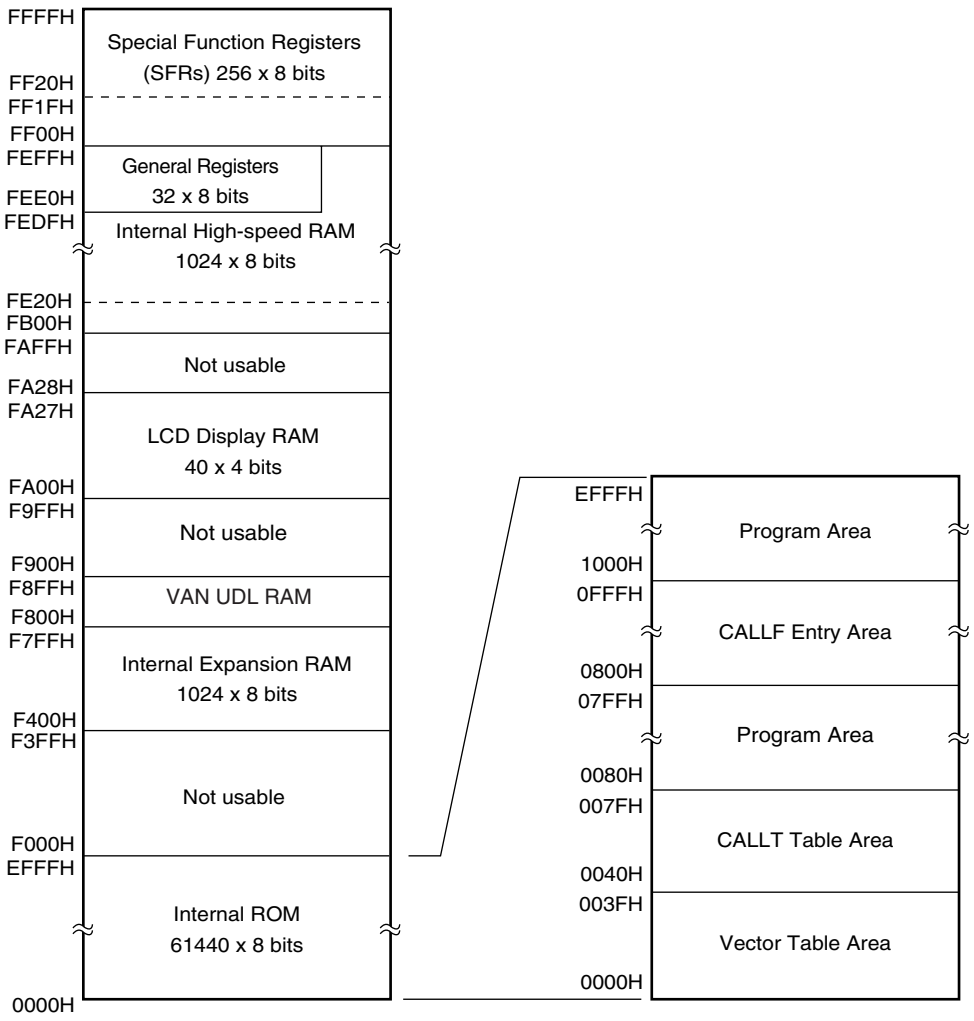
Figure 3-1: Pin Input/Output Circuits (2/2)



4. Memory Space

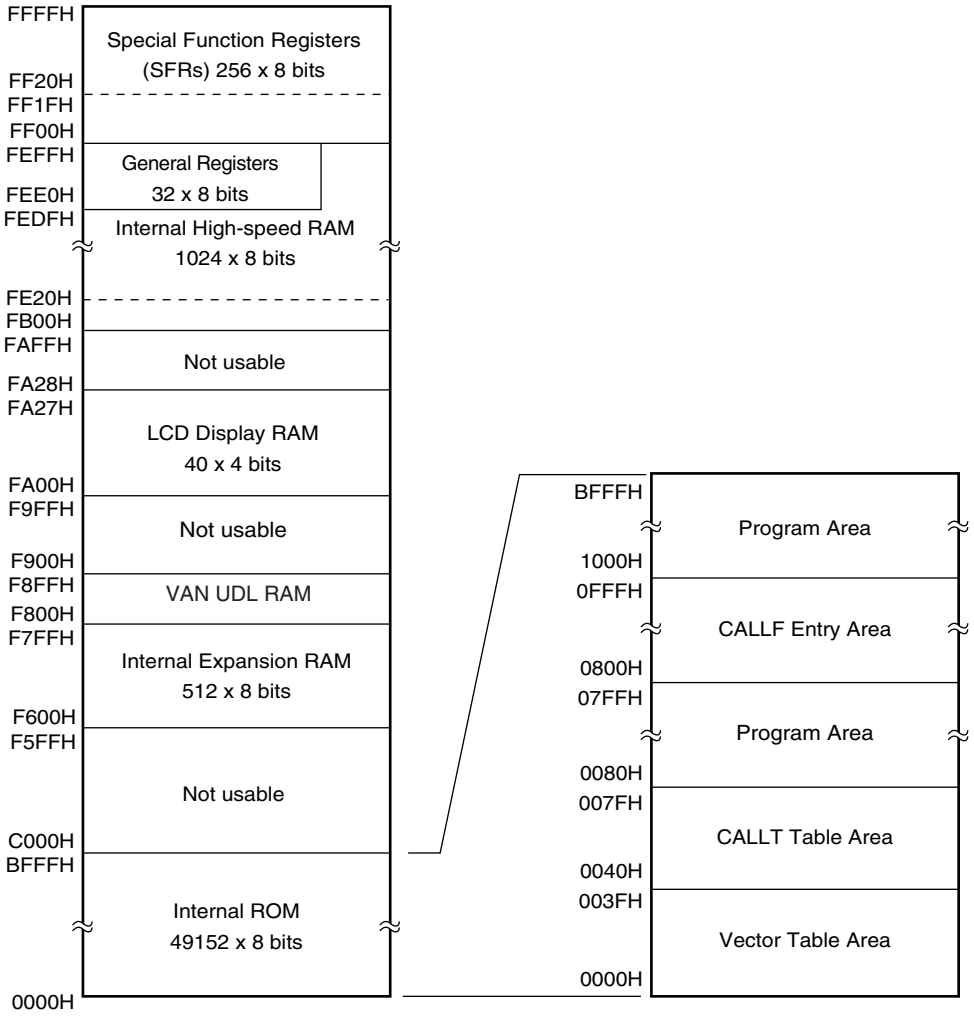
The memory map of the μPD1615A(A) is shown in Figure 4-1.

Figure 4-1: Memory Map (μPD1615A(A))



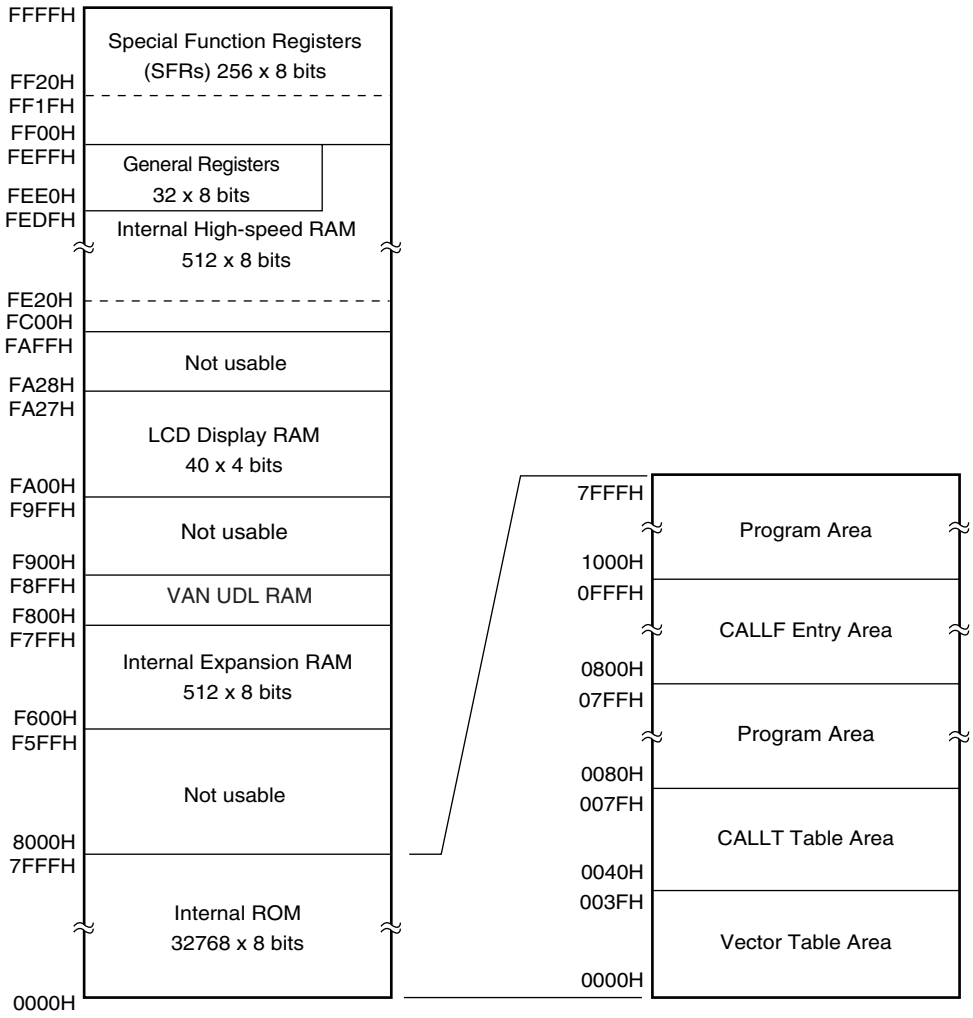
The memory map of the μPD1615B(A) is shown in Figure 4-2.

Figure 4-2: Memory Map (μPD1615B(A))



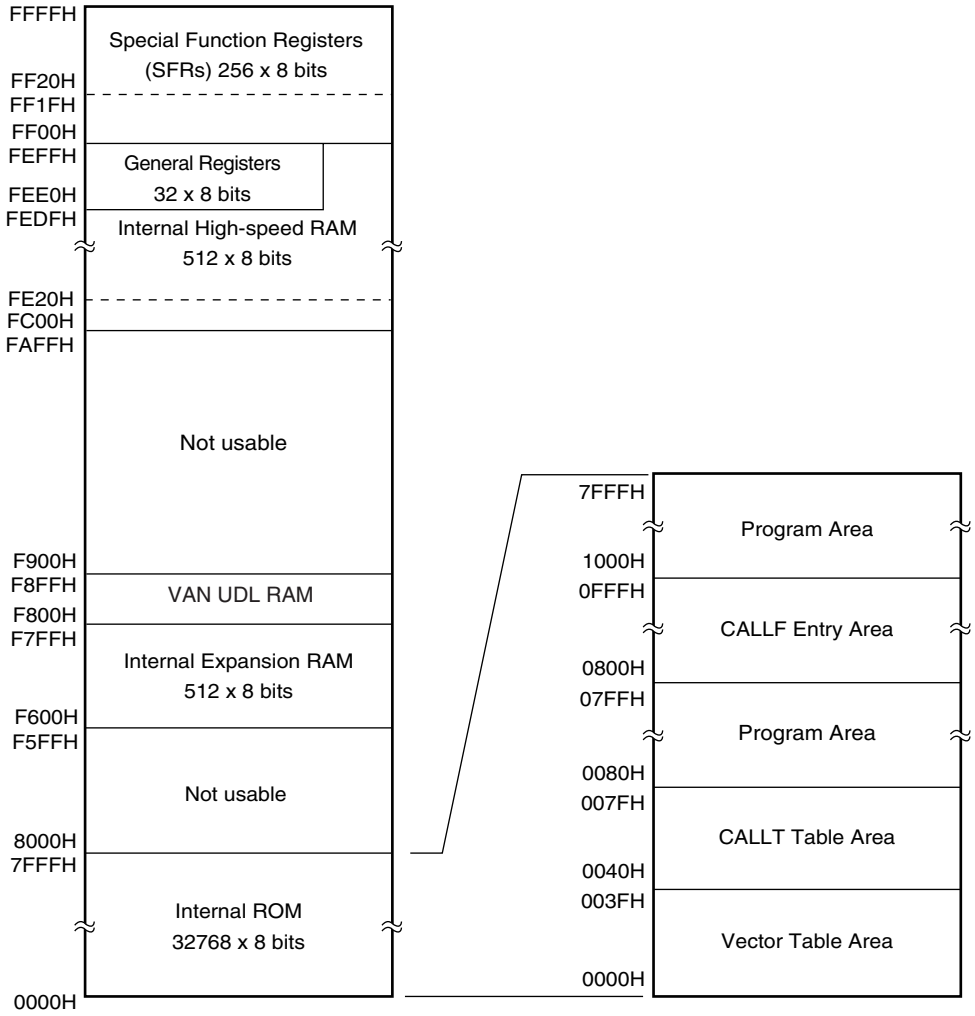
The memory map of the μPD1615F(A) is shown in Figure 4-3.

Figure 4-3: Memory Map (μPD1615F(A))



The memory map of the μPD1616F(A) is shown in Figure 4-4.

Figure 4-4: Memory Map (μPD1616F(A))



5. Peripheral Hardware Function

5.1 Ports

Input/output ports are classified into three types.

- CMOS input/output (Port 0, Port 4, Port 8 to Port 12) : 53
- Input (P10 to P14) : 4

Total : 57

Table 5-1: Functions of Ports

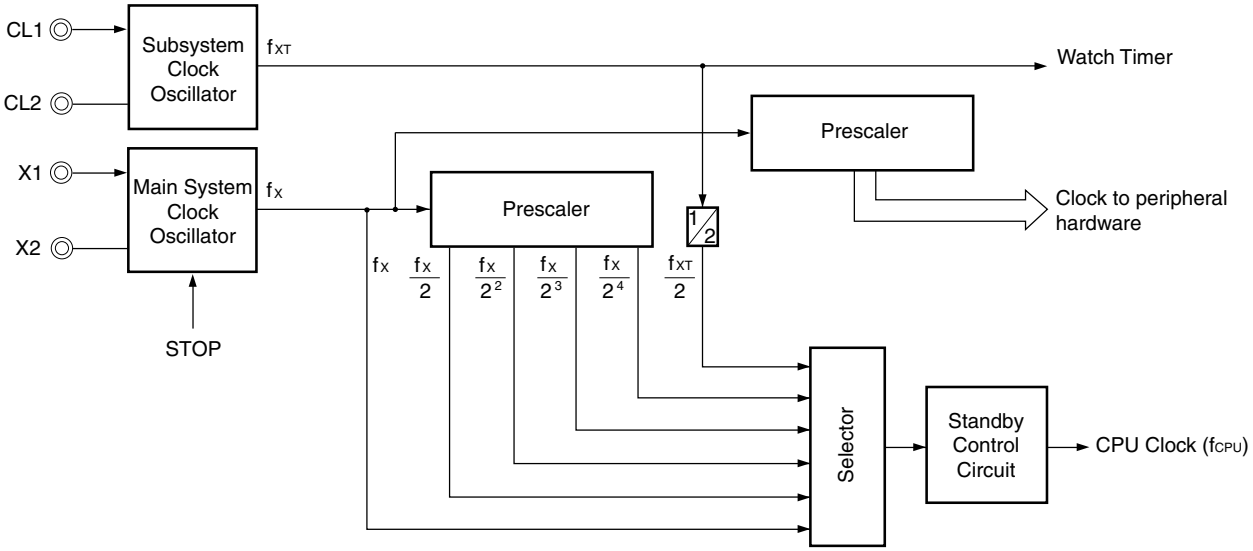
Port Name	Pin Name	Function
Port 0	P00 to P02 P06, P07	Input/output port, input/output can be specified bit-wise.
Port 1	P10 to P13	Input port.
Port 4	P40 to P47	Input/output port, input/output can be specified bit-wise.
Port 8	P80 to P87	Input/output port, input/output can be specified bit-wise. When used as an input port, port function can be specified by software.
Port 9	P90 to P97	Input/output port, input/output can be specified bit-wise. When used as an input port, port function can be specified by software.
Port 10	P100 to P 107	Input/output port, input/output can be specified bit-wise. When used as an input port, port function can be specified by software.
Port 11	P110 to P 117	Input/output port, input/output can be specified bit-wise. When used as an input port, port function can be specified by software.
Port 12	P120 to P127	Input/output port, input/output can be specified bit-wise. When used as an input port, port function can be specified by software.

5.2 Clock Generator

There are two kinds of clock generators: main system and subsystem clock generators.
It is possible to change the instruction execution time.

- 0.25 μs/0.5 μs/1 μs/2 μs/4 μs (at main system clock frequency of 8.0 MHz)
- 122 μs (at subsystem clock frequency of approx. 32 KHz)

Figure 5-1: Clock Generator Block Diagram

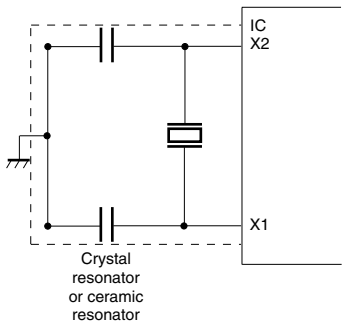


5.3 Main system clock oscillator

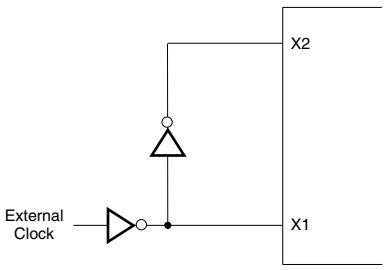
The main system clock oscillator oscillates with a crystal or a ceramic resonator connected to the X1 and X2 pins.

Figure 5-2: Oscillator Circuit

(a) Crystal and ceramic oscillation



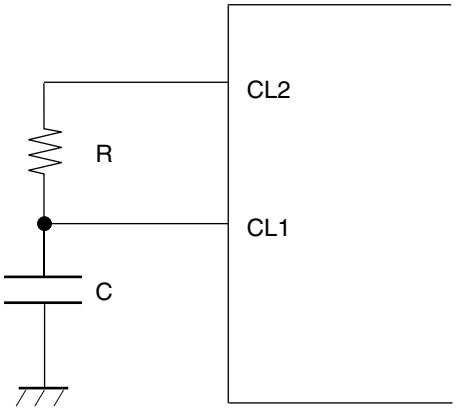
(b) External clock



5.4 Subsystem Clock Oscillator

Subsystem clock oscillator is for RC oscillation with low frequency.

Figure 5-3: Oscillator Circuit



5.5 Timer/Event Counter

There are the following seven timer/event counter channels:

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2: Types and Functions of Timer/Event Counters

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	2 channels	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	—	—
Function	Timer output	1 output	2 outputs	—	—
	PWM output	1 output	2 outputs	—	—
	Pulse with measurement	2 inputs	—	—	—
	Square wave output	1 output	2 outputs	—	—
	Interrupt request	2	2	2	1

Figure 5-4: 16-bit Timer TM0

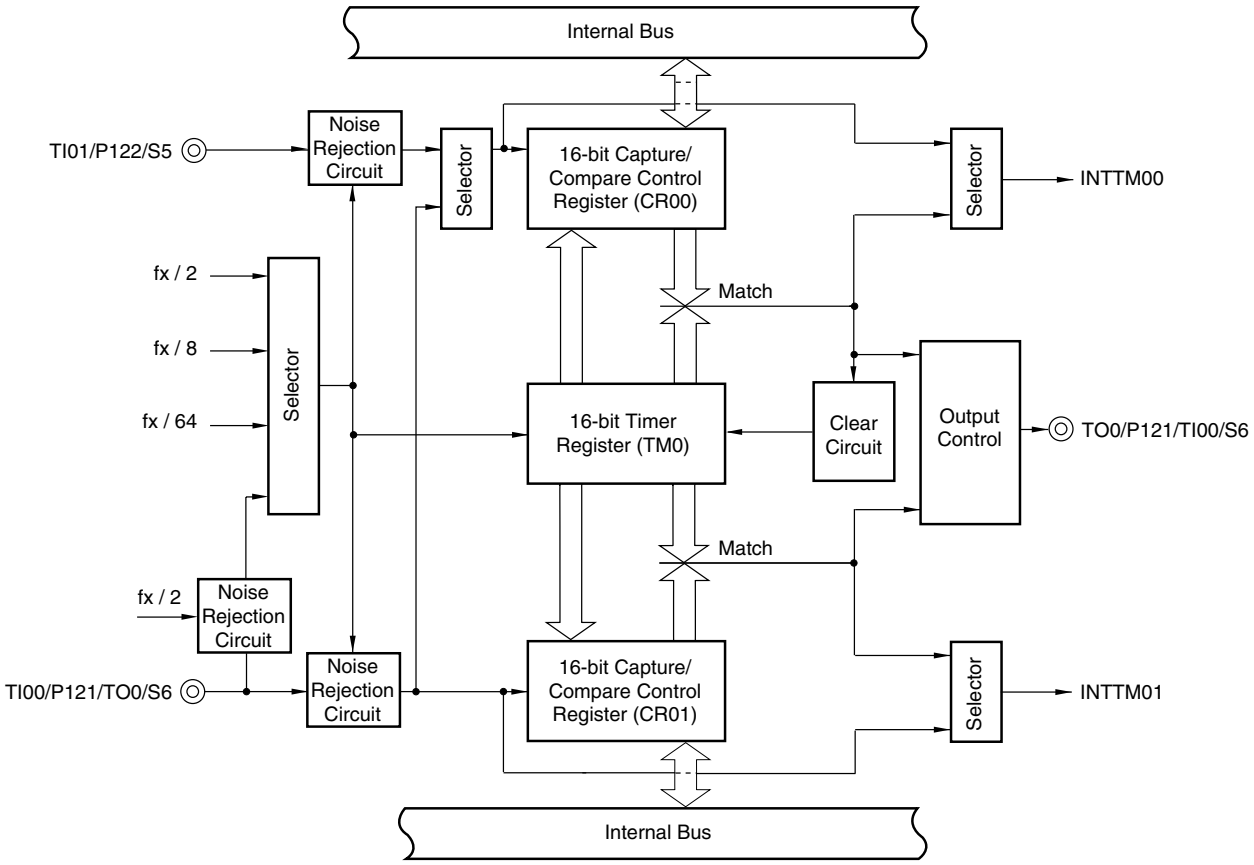


Figure 5-5: 8-Bit Timer/Event Counter 51 Block Diagram

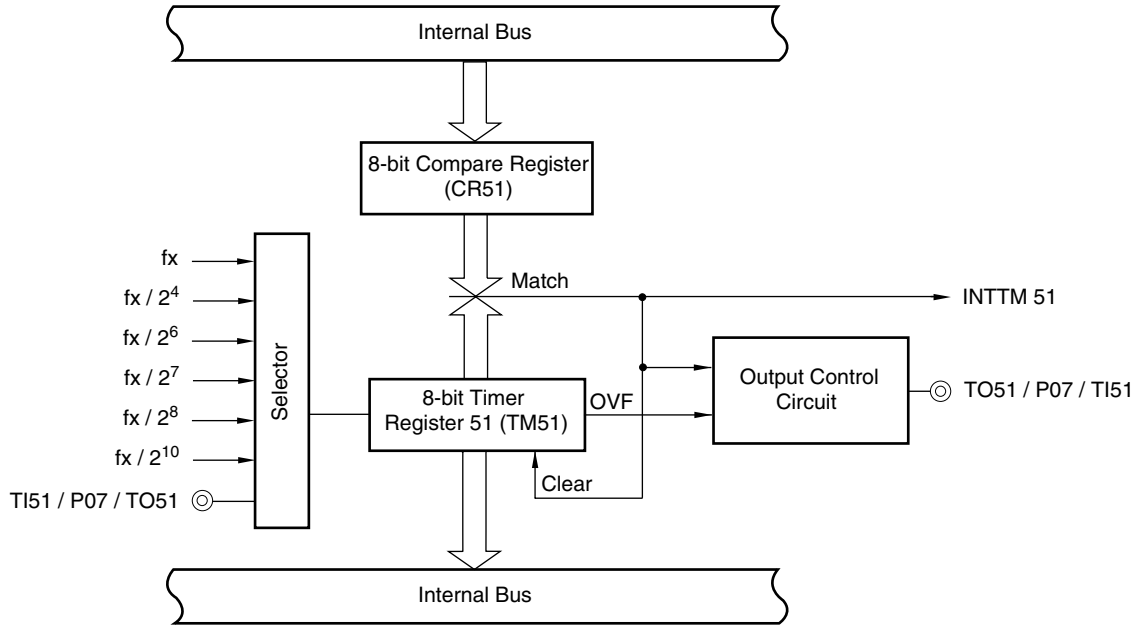


Figure 5-6: 8-Bit Timer/Event Counter 50 Block Diagram

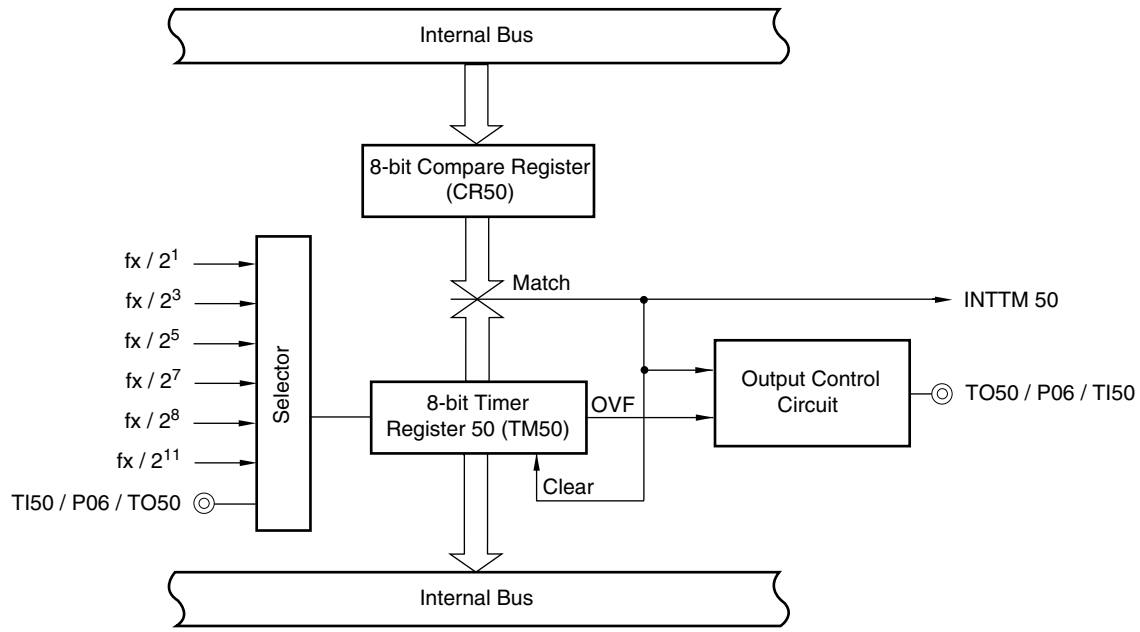


Figure 5-7: Watch Timer Block Diagram

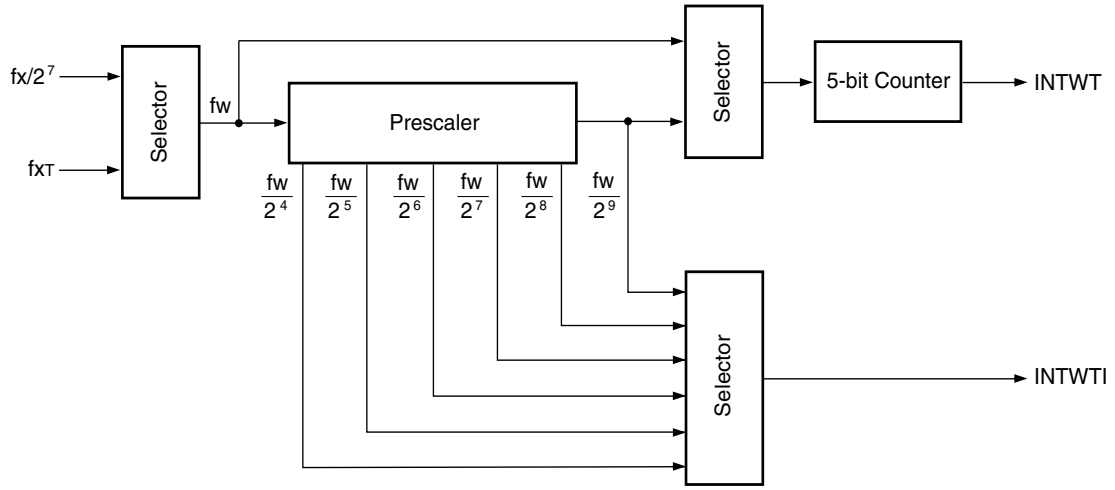
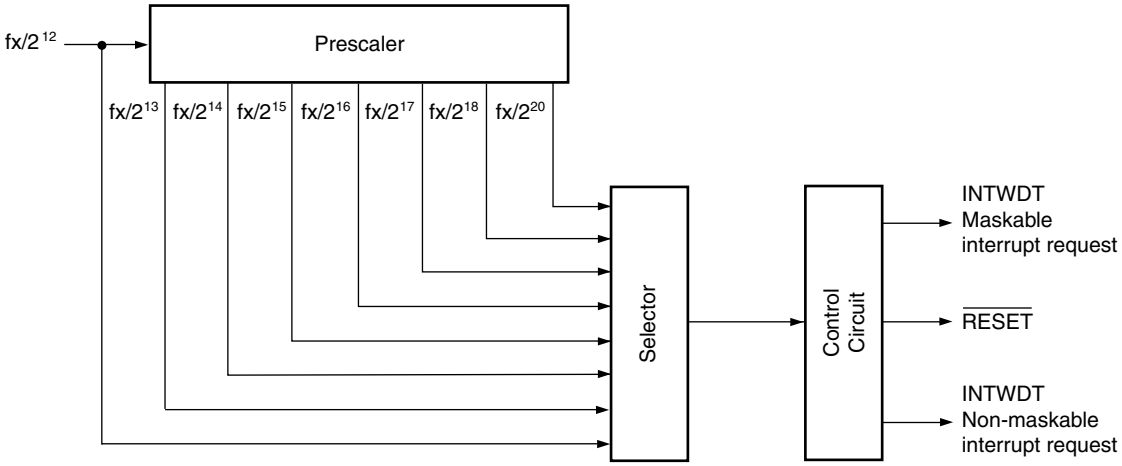


Figure 5-8: Watchdog Timer Block Diagram

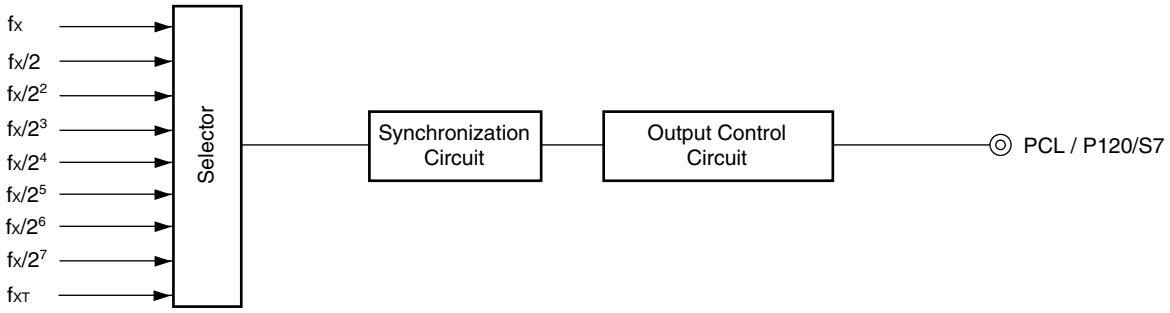


5.6 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 62.5 KHz / 125 KHz / 250 KHz / 500 KHz / 1 MHz / 2 MHz / 4 MHz / 8 MHz (at main system clock frequency of 8.0 MHz)

Figure 5-9: Clock Output Control Circuit Block Diagram

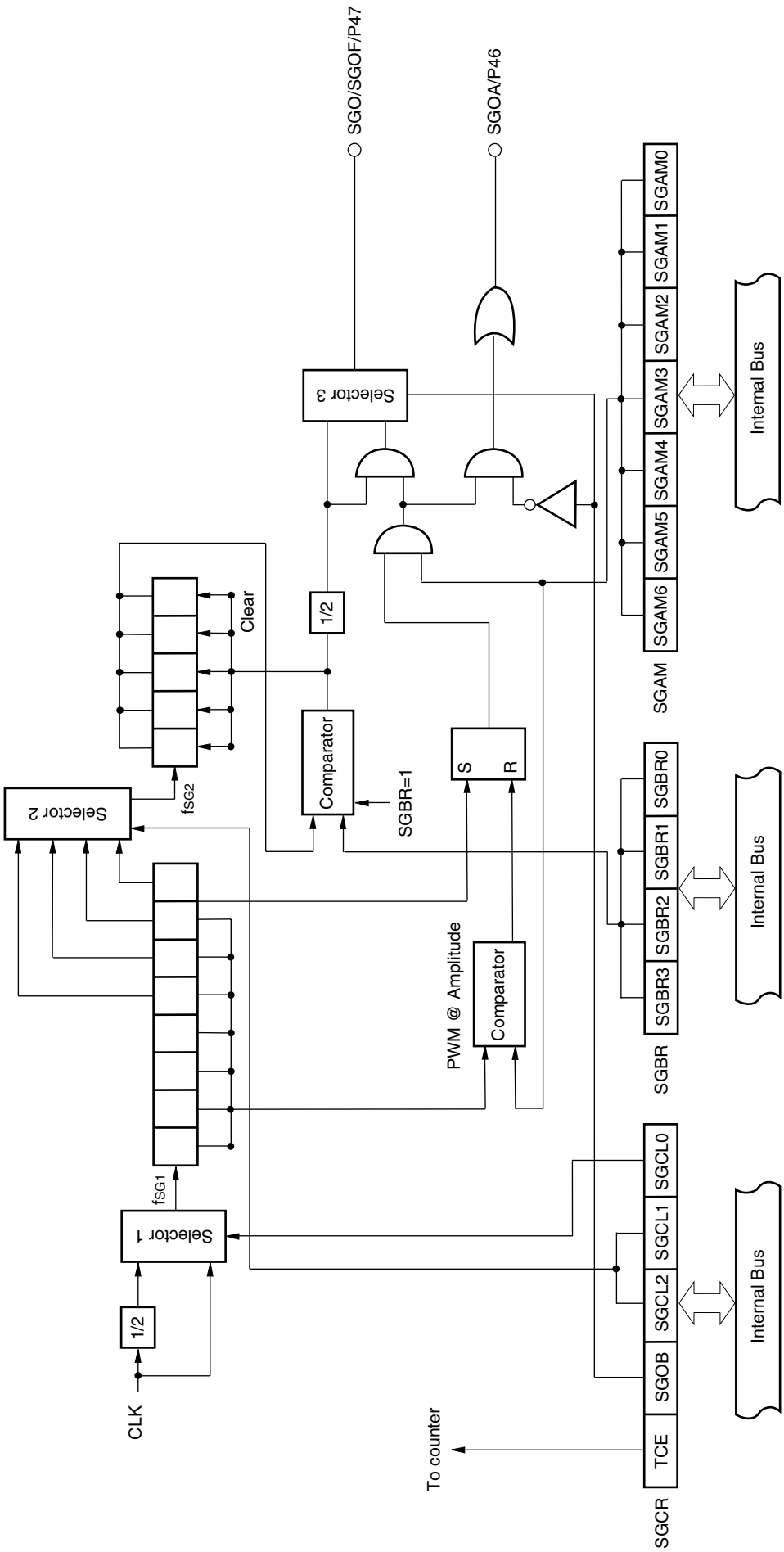


Note: The segment output is only valid on the μPD1615A(A), μPD1615B(A), and μPD1615F(A).

5.7 Sound Generator

The sound generator will produce sounds composed of a rectangular frequency signal and a PWM signal for volume control.

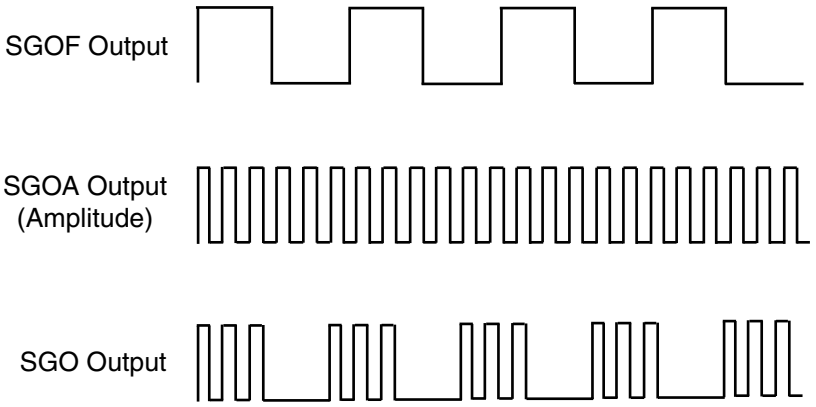
Figure 5-10: Block Diagram of the Sound Generator



The sound generator output is selectable as separate frequency-/volume-output SGOF/SGOA or as composed signal SGO.

The output signal at the composed output has the following principle shape:

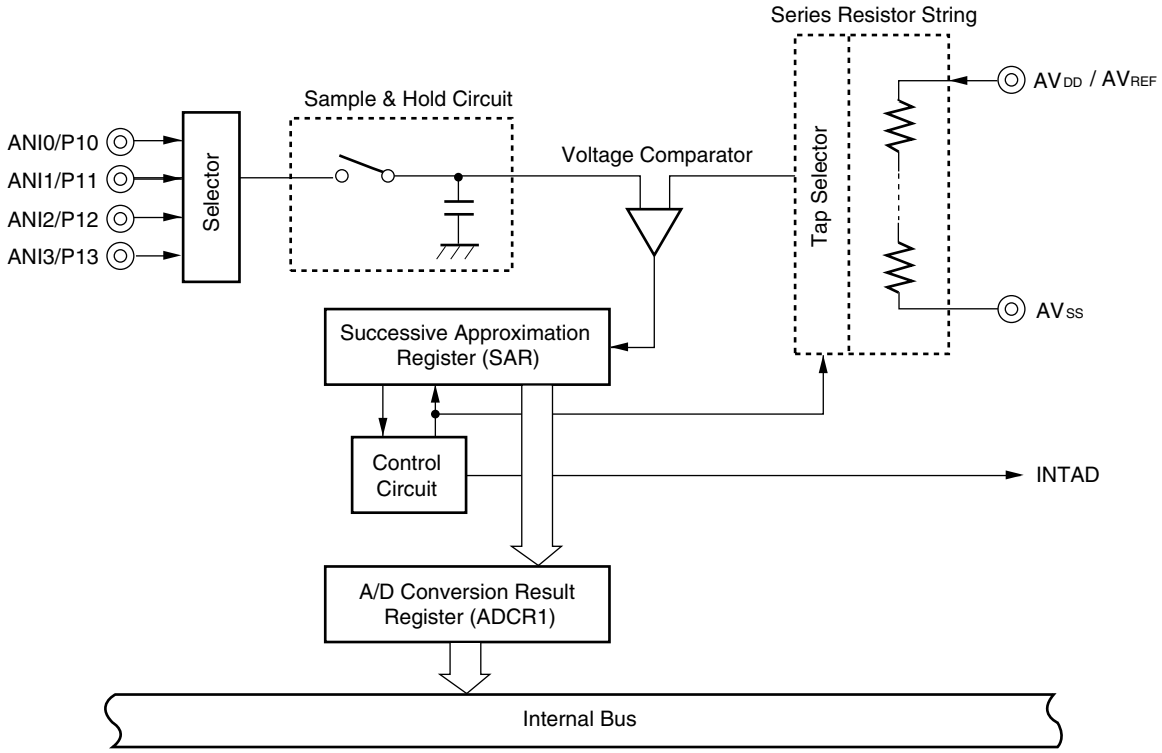
Figure 5-11: Composed Sound Generator Output SGO



5.8 A/D Converter

The A/D converter consists of four 8-bit resolution channels.
A/D conversion can be started by software.

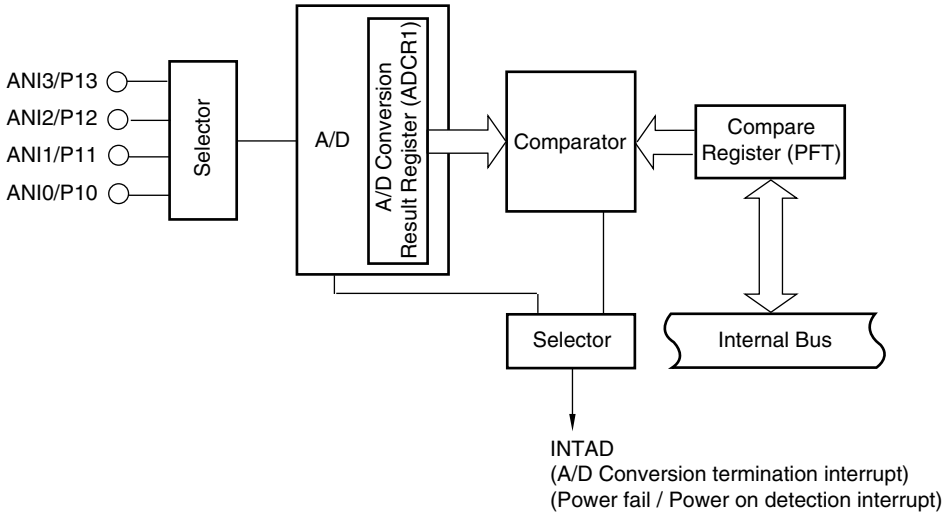
Figure 5-12: A/D Converter Block Diagram



5.9 Power Fail Detector

The block diagram of the power fail detector is shown in figure 5-13.

Figure 5-13: Block Diagram Power Fail Detector



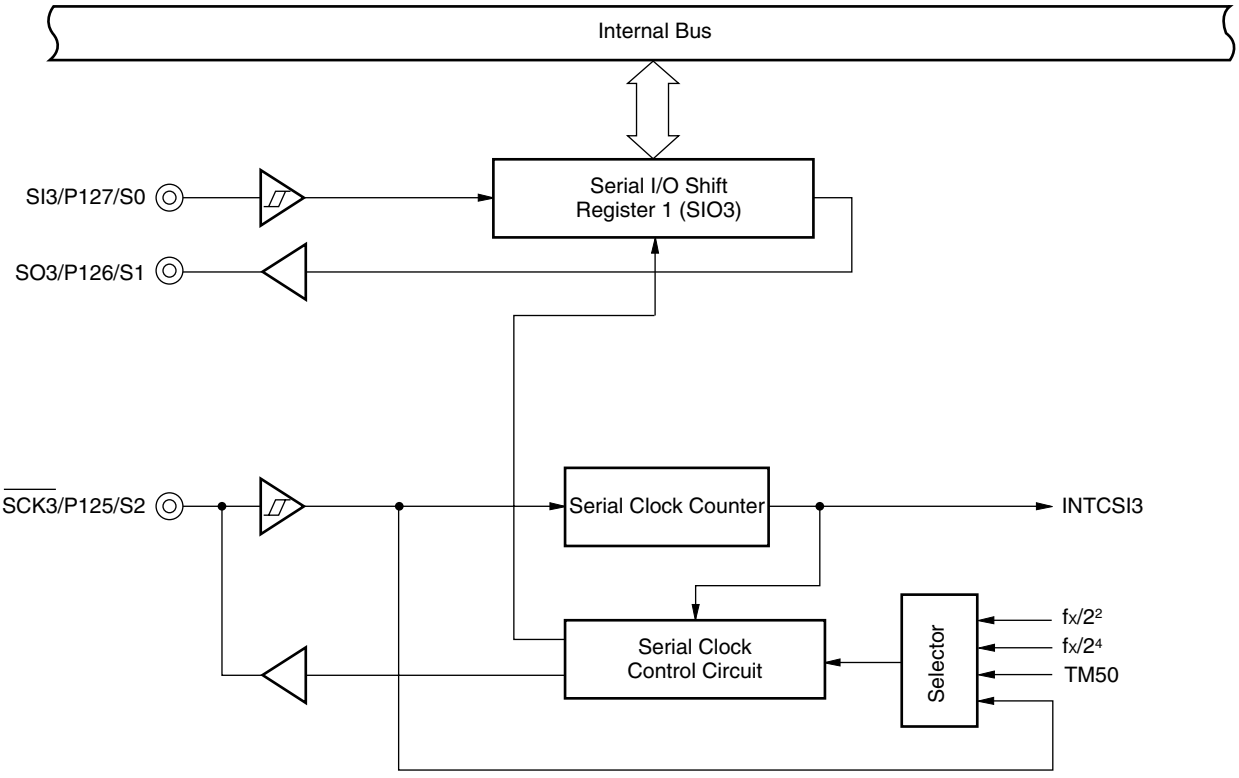
5.10 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:
- Serial interface channel - CSI
- Serial interface channel - UART

Table 5-3: Types and Functions of Serial Interfaces

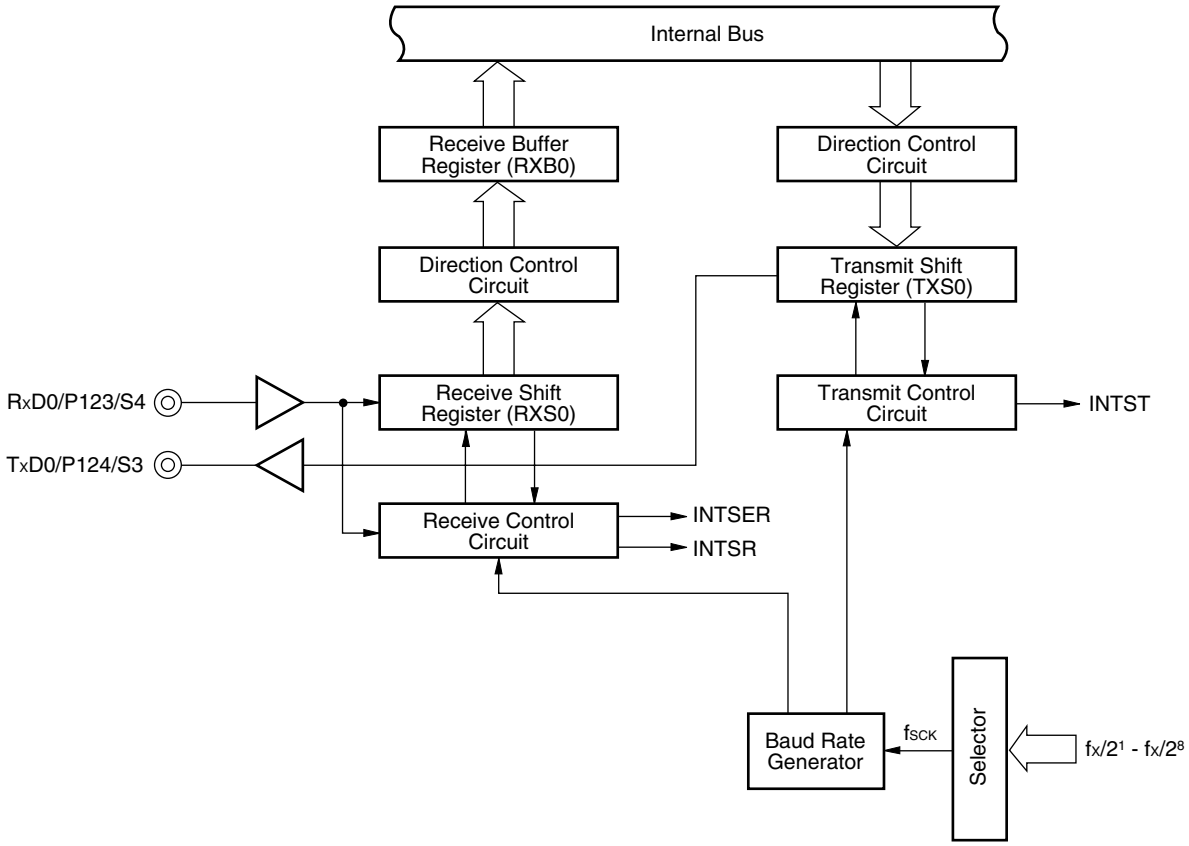
Function	Serial Interface Channel CSI	Serial Interface Channel UART
3-wire serial I/O mode	○(MSB first)	-
Asynchronous serial interface (UART) mode	-	(On-chip dedicated baud rate generator)

Figure 5-14: Serial Interface Channel CSI (SIO3) Block Diagram



Note: The segment output is only valid for the μPD1615A(A), μPD1615B(A), and μPD1615F(A).

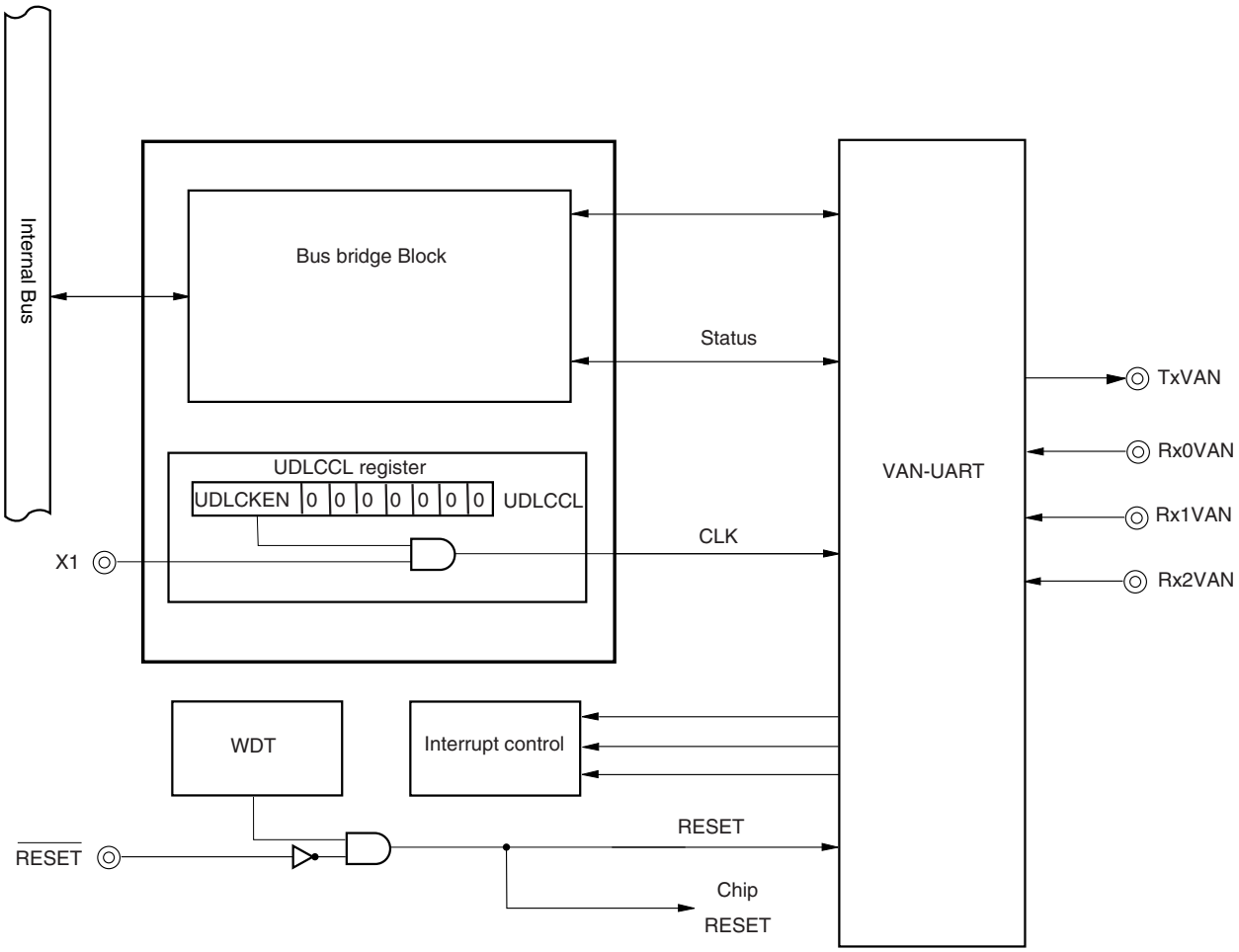
Figure 5-15: Serial Interface UART Block Diagram



Note: The segment output is only valid on the μPD1615A(A), μPD1615B(A), and μPD1615F(A).

5.11 VAN-Bus Interface

Figure 5-16: VAN-Bus Interface

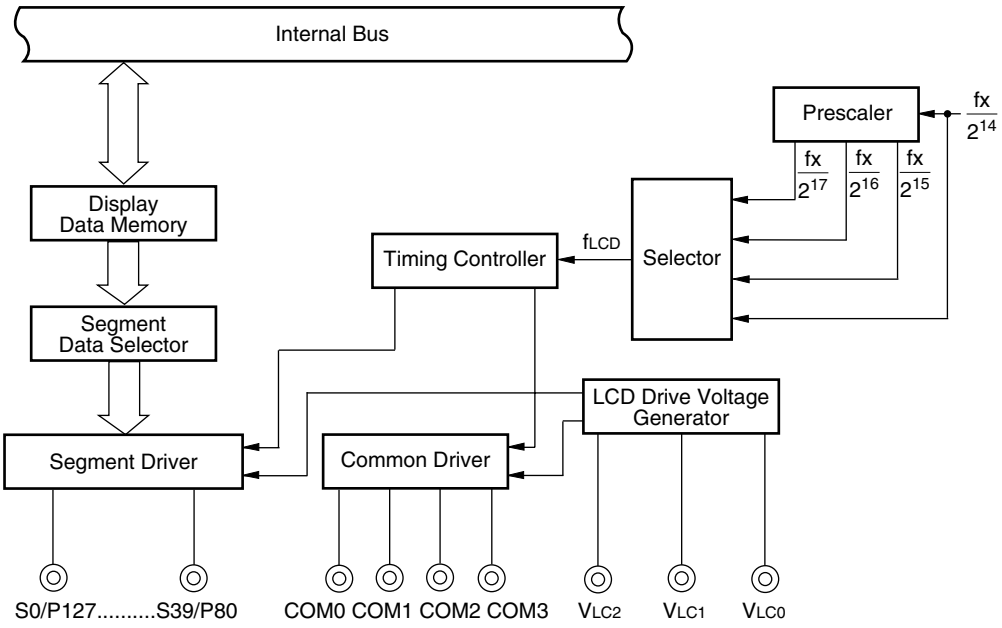


5.12 LCD Controller/Driver

Table 5-4: Display Mode Types and Maximum Number of Display Pixels

Bias Method	Time Multiplexing	Common Signal used	Maximum Number of Display Pixels
1/3	4	COM0 to COM3	160 (40 segments x 4 commons)
1/3	3	COM0 to COM2	120 (40 segments x 3 commons)
1/2	3	COM0 to COM2	120 (40 segments x 3 commons)
1/2	2	COM0 to COM1	80 (40 segments x 2 commons)
-	static	COM0	40 (40 segments x 1 common)

Figure 5-17: LCD Controller/Driver Block Diagram



Note: The LCD controller/driver pins are only valid on the μPD1615A(A), μPD1615B(A), and μPD1615F(A).

6. Interrupt Functions and Test Functions

6.1 Interrupt Functions

A total of 19 interrupt functions are provided, divided into the following three types.

- Non-maskable interrupt : 1
- Maskable interrupt : 17
- Software interrupt : 1

Table 6-1: Interrupt Vector Table

Interrupt type	Priority (default)	Interrupt request source		Vector code address	Basic structure type
Resetting	-	RESET	Reset input	0000H	
Non-maskable	-	INTWDT	Watchdog timer overflow (when non-maskable interrupt is selected)	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer is selected)		(B)
	1	INTVE	INTVE → VAN-End of Message	0006H	
	2	INTVT	INTVT → VAN-Emission	0008H	
	3	INTVR	INTVR → VAN-Reception	000AH	
	4	INTP0	External interrupt pin input edge detection	000CH	(C)
	5	INTP1		000EH	
	6	INTP2		0010H	
	7	INTTM00	Agreement between TM00 and CR000 (when compare register is specified) TI001 valid edge detection (when capture register is specified)	0012H	(B)
	8	INTTM01	Agreement between TM00 and CR001 (when compare register is specified) TI000 valid edge detection (when capture register is specified)	0014H	
	9	INTTM50	Agreement between TM50 and CR50	0016H	
	10	INTTM51	Agreement between TM51 and CR51	0018H	
	11	INTWTI	Watch timer interval interrupt	001AH	
	12	INTWT	Watch interrupt	001CH	
	13	INTCSI3	SIO30 transfer completion	001EH	
	14	INTSER	UART0 reception error occurrence	0020H	
	15	INTSR	UART0 reception completion	0022H	
	16	INTST	UART0 transmission completion	0024H	
	17	INTAD	A/D conversion end	0026H	
Software	-	BRK	Execution of BRK instruction	003EH	(D)

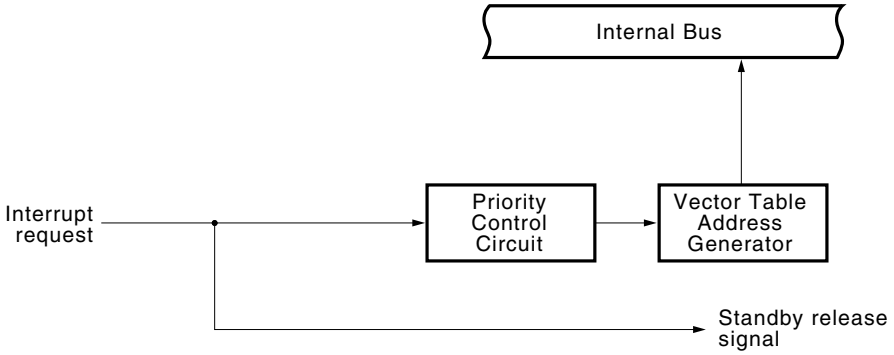
Notes: **1.** Default priority is the priority order when several maskable interruptions are generated at the same time. 0 is the highest order and 20 is the lowest order.

2. Basic structure types (A) to (D) correspond to (A) to (D) in Figure 6-1.

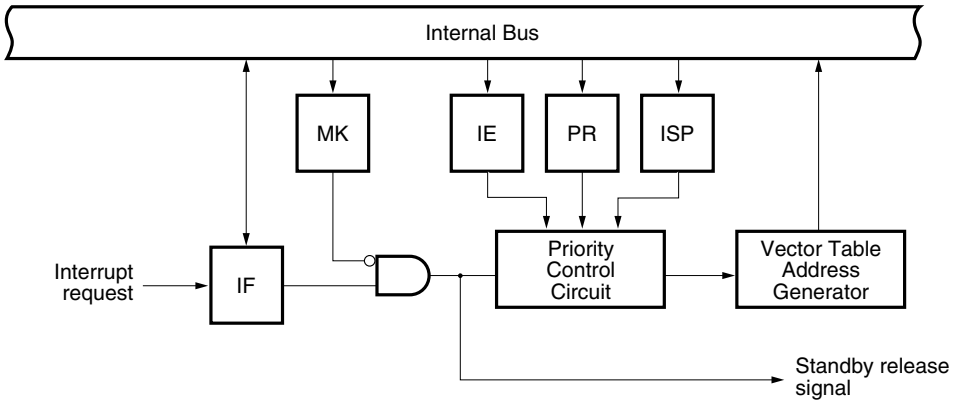
6.2 Interrupts

Figure 6-1: Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt

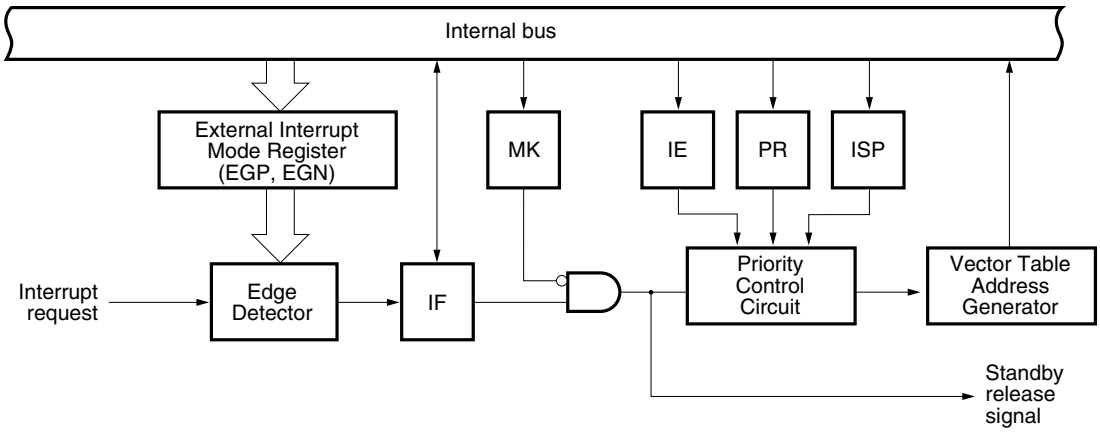
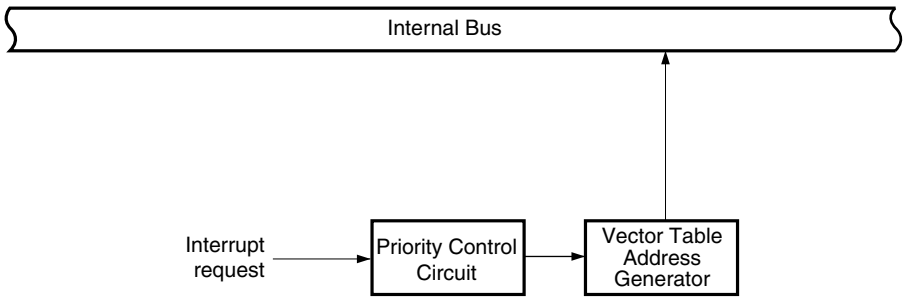


Figure 6-1: Interrupt Function Basic Configuration (2/2)

(D) Software interrupt

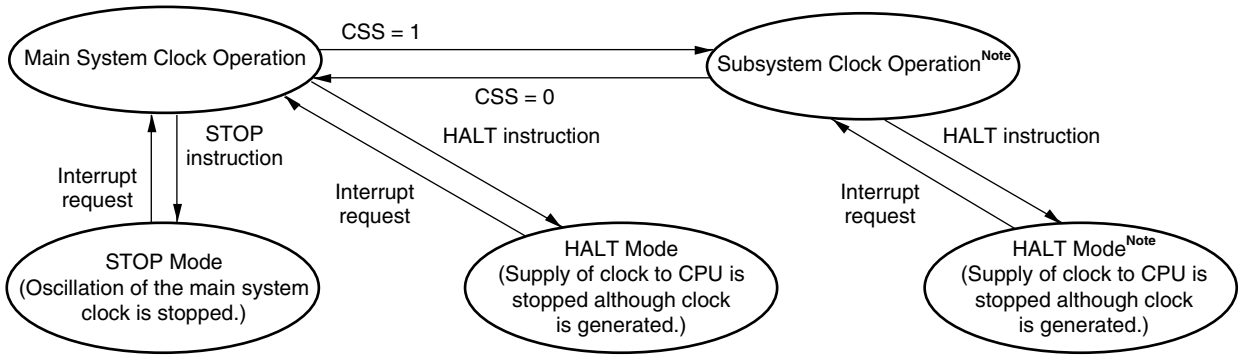


7. Standby Function

The standby function intends to reduce current consumption. It has the following two modes:

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used for extremely small power consumption.

Figure 7-1: Standby Function



Note: Current consumption is reduced by shutting off the main system clock.
If the CPU is operating on subsystem clock, shut off the main system clock by setting MCC.

Caution: When switching back to the main system clock while the subsystem clock has been used and the main system clock has been stopped, be sure to provide enough time for the oscillator to be stable before resuming the program execution of the main system clock.

8. Reset Function

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

9. Instruction Set

(1) 8-Bit Instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ.

Table 9-1: 8-Bit Instructions

1st Operand \ 2nd Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOVU	ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP										DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note: Except r = A

(2) 16-Bit Instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW.

Table 9-2: 16-Bit Instructions

1st Operand \ 2nd Operand	#word	AX	rp	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW[Note]						
SP	MOVW	MOVW						

Note: Only when rp = BC, DE, HL

(3) Bit Manipulation Instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR.

Table 9-3: Bit Manipulation Instructions

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ.

Table 9-4: Call Instructions/Branch Instructions

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP.

10. Electrical Specifications

Absolute Maximum Ratings (T_A = 25° C)

Table 10-1: Absolute Maximum Ratings

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			-0.3 to +6.5	V
	AV_{DD}/AV_{REF}			-0.3 to V_{DD} +0.3	
	AV_{SS}			-0.3 to +0.3	
Input voltage	V1	P00 to P02, P06, P07, P40 to P46, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, X1, X2, CL1, $\overline{RESET}$		-0.3 to V_{DD} +0.3	
Output voltage	V0			-0.3 to V_{DD} +0.3	
Analog input voltage	V_{AN}	P10 to P13	Analog input pin	AV_{SS} -0.3 to AV_{DD} +0.3	
High level output current	I_{OH}	1 pin (except P47)		-10	mA
		P47		-30	
		P00 to P02, P06, P07, P40 to P46, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127		-30	
Low level output Current	I_{OL} Note	P00 to P02, P06, P07, P40 to P46, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127 1 pin (except P47)	Peak value	20	
			Effective value	10	
		P47	Peak value	30	
			Effective value	20	
		TxVAN 1 pin	Peak value	30	
			Effective value	15	
		P00 to P02, P06, P07, P40 to P46, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127 Total	Peak value	65	
			Effective value	50	
Operating ambient temperature	T_{OPT}			-40 to +85	°C
Storage temperature	T_{STG}			-65 to +150	

Note: Effective value should be calculated as follows: [Effective value] = [Peak value] x $\sqrt{duty}$

Caution: Product quality may suffer if the absolute maximum ratings are exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Capacitance (T_A = 25° C, V_{DD} = V_{SS} = 0 V)

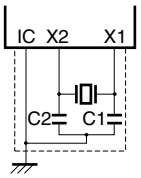
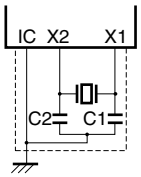
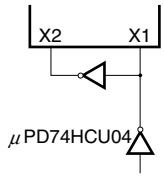
Table 10-2: Capacitance

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input capacity	C_{IN}	f = 1 MHz Pins not measured = 0 V	RESET, P10 - P13, Rx0VAN, Rx1VAN, Rx2VAN			15	pF
Output capacity	C_O	f = 1 MHz Pins not measured = 0 V	TxVAN			15	pF
Input/output capacity	C_{IO}	f = 1 MHz Pins not measured = 0 V	P00 - P02, P06, P07, P40 - P46, P80 - P87, P90 - P97, P100 - P107, P110 - P117, P120 - P127			15	pF
			P47			30	pF

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Main System Clock Oscillation Circuit Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Table 10-3: Main System Clock Oscillation Circuit Characteristics

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) Note 1	V_{DD} = 4.0 to 5.5 V	3.9	8.0	8.1	MHz
		Oscillation stabilization time Note2	After V_{DD} reaches oscillator voltage range MIN. 4.0 V			4	ms
Crystal resonator		Oscillator frequency (fx) Note 1	V_{DD} = 4.0 to 5.5 V	3.9	8.0	8.1	MHz
		Oscillation stabilization time Note2	After V_{DD} reaches oscillator voltage range MIN. 4.0 V			10	ms
External clock		X1 input frequency (fx) Note 1	V_{DD} = 4.0 to 5.5 V	3.9	8.0	8.1	MHz
		X1 input high/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.0 to 5.5 V	58		125	ns

Notes: **1.** Indicates only oscillation circuit characteristics. Refer to “AC Characteristics” for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

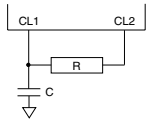
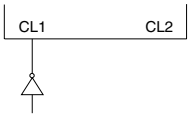
Cautions: **1. When using the main system clock oscillation circuit, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillation circuit capacitor ground should always be the same as that of V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillation circuit.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Table 10-4: Subsystem Clock Oscillation Circuit Characteristics

Resonator	Recommended circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
RC osc.		Oscillator frequency (fxt)	4.0 V ≤ V_{DD} ≤ 5.5 V R = 518 kΩ C = 33 pF	32	40	50	KHz
External clock		CL1 Input [Note] frequency (fxt)	4.0 V ≤ V_{DD} ≤ 5.5 V	32		50	KHz
		CL1 Input high/low level width (t_{XTH}, t_{XTL})	4.0 V ≤ V_{DD} ≤ 5.5 V	9		15.7	μs

Note: Only oscillator circuit characteristics are shown. Regarding instruction execute time, please refer to AC characteristics.

Cautions:

1. When using the subsystem clock oscillation circuit, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillation circuit capacitor ground should always be the same as that of V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillation circuit.**

2. The subsystem clock oscillation circuit is designed to be a circuit with a low amplification level, for low power consumption more prone to misoperation due to noise than that of the main system clock. Therefore, when using the subsystem clock, take special cautions for wiring methods.

DC Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Table 10-5: DC Characteristics

Item	Symbol	Conditions		MIN.	TYP	MAX.	Unit
High-level input voltage	V_{IH1}	P10 - P13, P40 - P47, P80 - P87, P94 - P97, P100 - P107, P110 - P117, P120, P124, P126, Rx0VAN, Rx1VAN, Rx2VAN		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P00 - P02, P06, P07, P121 - P123, P125, P127		0.8 V_{DD}			
	V_{IH3}	X1, X2, CL1, CL2		V_{DD} - 0.5			
Low-level input voltage	V_{IL1}	P10 - P13, P40 - P47, P80 - P87, P94 - P97, P100 - P107, P110 - P117, P120, P124, P126, Rx0VAN, Rx1VAN, Rx2VAN		0		0.3 V_{DD}	
	V_{IL2}	$\overline{RESET}$, P00 - P02, P06, P07, P121 - P123, P125, P127		0		0.2 V_{DD}	
	V_{IL3}	X1, X2, CL1, CL2		0		0.4	
High-level output voltage	V_{OH1}	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -1 mA		V_{DD} - 1.0		V_{DD}	
		I_{OH} = -100 μA		V_{DD} - 0.5			
		P47	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -20 mA	V_{DD} - 0.5		V_{DD}	
Low-level output voltage	V_{OL1}	TxVAN	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15 mA		0.4	2.0	
	V_{OL2}	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.6 mA				0.4	
	V_{OL3}	I_{OL} = 400 μA				0.5	
	V_{OL4}	P47	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = 20 mA			0.5	
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Except X1, X2, CL1 and CL2			3	μA
	I_{LIH2}		X1, X2, CL1, CL2			20	
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Except X1, X2, CL1 and CL2			-3	
	I_{LIL2}		X1, X2, CL1, CL2			-20	
High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}				3	
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				-3	

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

DC Characteristics (T_A = -40 to +85° C, V_{DD} = 4.0 to 5.5 V)

Mask ROM Version

Table 10-6: DC Characteristics MASK ROM Version

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Power supply Note 1 current	I_{DD1}	8.0 MHz crystal oscillation operating mode (PLC = 00H)	V_{DD} = 5 V ± 10%		8	24	mA
	I_{DD2}	8.0 MHz crystal oscillation HALT mode	V_{DD} = 5 V ± 10%		1.6	4.8	mA
	I_{DD3}	RC oscillation operating mode (fx_T = 40 KHz)	V_{DD} = 5 V ± 10%		180	360	μA
	I_{DD4}	RC oscillation HALT mode (fx_T = 40 KHz)	V_{DD} = 5 V ± 10%		60	180	μA
	I_{DD5}	STOP mode	V_{DD} = 5 V ± 10%		1 Note 2	30 Note 2	μA

Notes: **1.** The AV_{DD}/AV_{REF} current, port current and the VAN UDL current are not included and PCC is set to 00h.
2. The subclock is not used.

Remarks: **1.** fx: Main system clock oscillator frequency.
2. f_{XT}: Subsystem clock oscillator frequency.

DC Characteristics (T_A = -10 to +85° C, V_{DD} = 4.0 to 5.5 V)

LCD C/D Static Method

Table 10-7: DC Characteristics Static Method

Parameter	Symbol	Test Conditions		MIN	TYP	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD output voltage deviation Note (common)	V_{ODC}	I_O = ± 5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD}	0		±0.2	V
LCD output voltage deviation Note (segment)	V_{ODS}	I_O = ± 1 μA		0		±0.2	

Note: The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDN}; n = 0, 1, 2).

LCD C/D 1/2 Bias Method

Table 10-8: DC Characteristics 1/2 Bias Method

Parameter	Symbol	Test Conditions		MIN	TYP	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD output voltage deviation Note (common)	V_{ODC}	I_O = ± 5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} x 1/2 V_{LCD2} = V_{LCD} x 1/2	0		±0.2	V
LCD output voltage deviation Note (segment)	V_{ODS}	I_O = ± 1 μA		0		±0.2	

Note: The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDN}; n = 0, 1, 2).

LCD C/D 1/3 Bias Method

Table 10-9: DC Characteristics 1/3 Bias Method

Parameter	Symbol	Test Conditions		MIN	TYP	MAX.	Unit
LCD drive voltage	V_{LCD}			3.0		V_{DD}	V
LCD output voltage deviation Note (common)	V_{ODC}	I_O = ± 5 μA	3.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} x 2/3 V_{LCD2} = V_{LCD} x 1/3	0		±0.2	V
LCD output voltage deviation Note (segment)	V_{ODS}	I_O = ± 1 μA		0		±0.2	

Note: The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDN}; n = 0, 1, 2).

The LCD controller/driver is only available in the μPD1615.

AC Characteristics

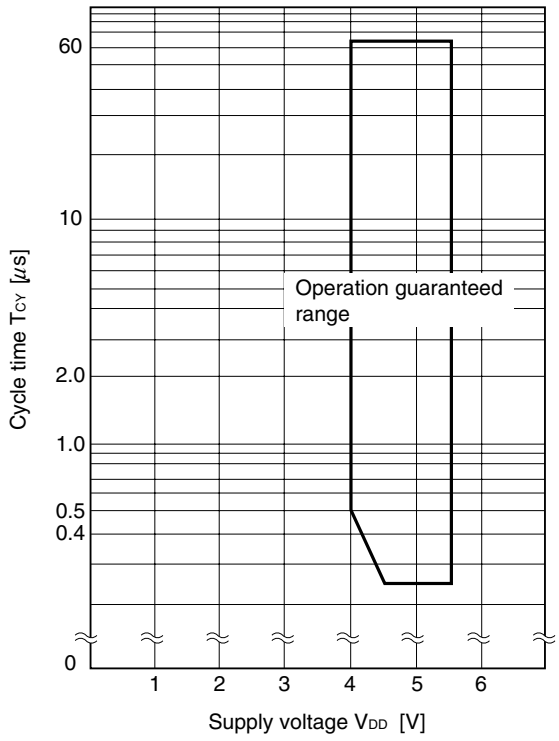
(1) Basic Operation (T_A = -40 to +85° C, V_{DD} = 4.0. to 5.5 V)

Table 10-10: AC Characteristics Basic Operation

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (min. instruction execution time)	t_{CY}	4.5 V ≤ V_{DD} ≤ 5.5 V	0.25		8	μs
		4.0 V ≤ V_{DD} ≤ 5.5 V	0.5		8	
		During subsystem clock operation	80	100	125	
TI50, TI51 input frequency	f_{TI5}		0		4	MHz
TI50, TI51 input high/low level width	t_{TIH5}, t_{TIL5}		100			ns
TI00, TI01 input high/low level width	t_{TI0}		2/ f_{SMP0} + 0.1 **Note 1**			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INTP0-2	10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}		10			μs

Note: The sampling is performed when using the count clock selected by PRM01-00 (f_{SMP0} = fx/2, fx/8, fx/64). When the TI00 valid edge is selected for the count clock, f_{SMP0} is found by f_{SMP0} = fx/8.

Figure 10-1: T_{CY} vs V_{DD}



(3) Serial Interface (T_A = -40 to +85° C, V_{DD} = 4.0. to 5.5 V)

(a) Serial Interface Channel SIO30

Table 10-11: 3-wire serial I/O mode ($\overline{SCK3}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY1}		800		ns
$\overline{SCK3}$ high/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 - 50		
SI3 setup time (to $\overline{SCK3}$) ↑	t_{SIK1}		100		
SI3 hold time (from $\overline{SCK3}$) ↑	t_{KSI1}		400		
SO3 output delay time (from $\overline{SCK3}$) ↓	t_{KSO1}	C = 100 pF [Note]		300	

Note: C is the load capacitance of SO3, $\overline{SCK3}$ output line

Table 10-12: 3-wire serial I/O mode ($\overline{SCK3}$... External clock output)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY2}		800		ns
$\overline{SCK3}$ high/low-level width	t_{KH2}, t_{KL2}		400		
SI3 setup time (to $\overline{SCK3}$) ↑	t_{SIK2}		100		
SI3 hold time (from $\overline{SCK3}$) ↑	t_{KSI2}		400		
SO3 output delay time (from $\overline{SCK3}$) ↓	t_{KSO2}	C = 100 pF [Note]		300	

Note: C is the load capacitance of SO3, $\overline{SCK3}$ output line.

(b) Serial Interface Channel UART0

Table 10-13: UART Mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP	MAX.	Unit
Transfer rate			260		125000	bps

Figure 10-2: AC Timing Test Points (excluding X1, CL1 inputs)

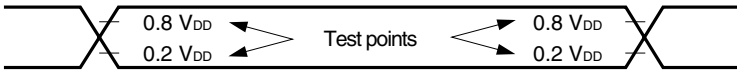


Figure 10-3: Clock Timing

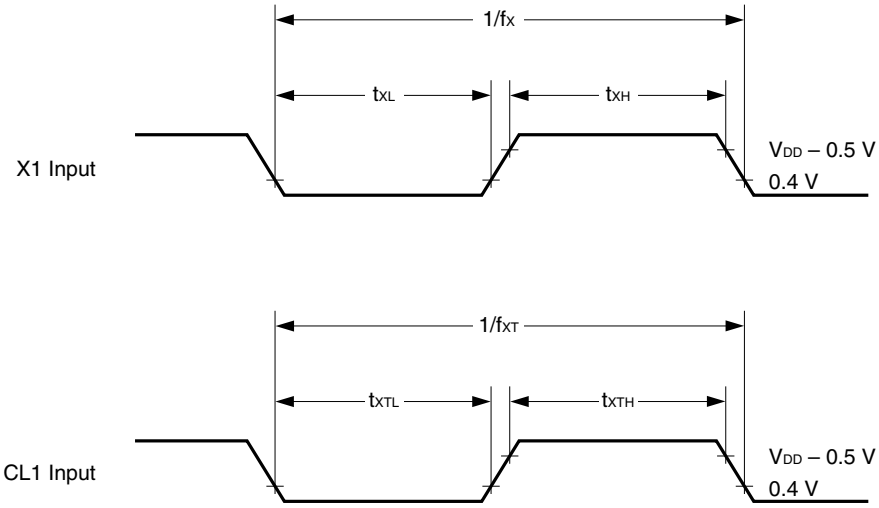
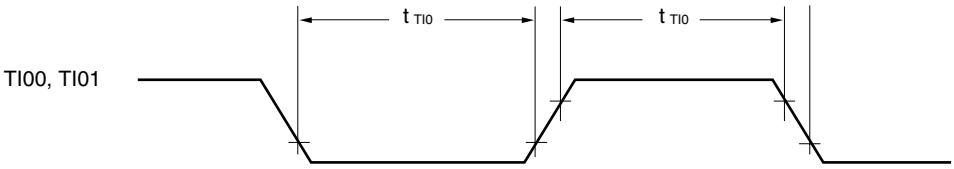
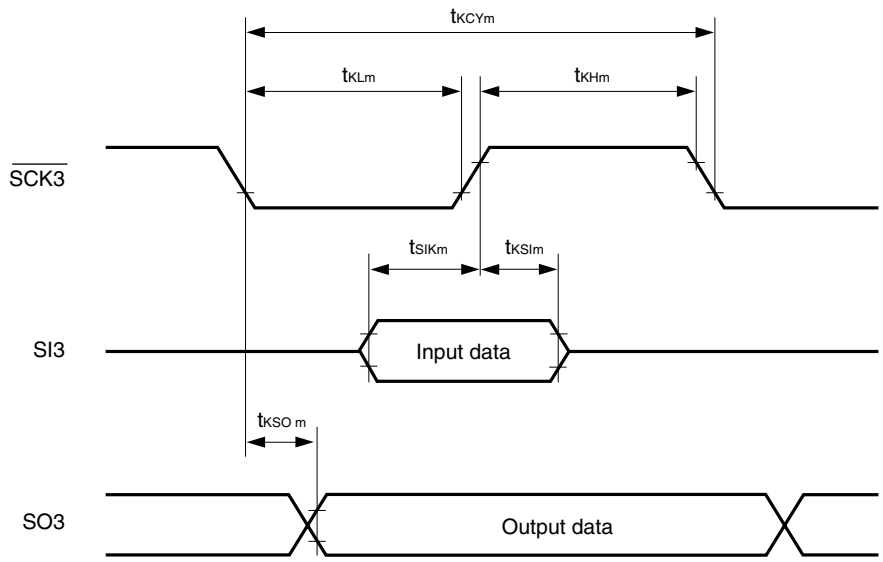


Figure 10-4: TI Timing



Serial Transfer Timing

Figure 10-5: 3-wire serial I/O mode



Remark: m=1

A/D Converter Characteristics

(T_A = -40 to +85° C, V_{DD} = AV_{DD}/AV_{REF} = 4.0 to 5.5 V, AV_{SS} = V_{SS} =0 V, fx = 8 MHz)

Table 10-14: A/D Converter Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error					± 0.6	%
Conversion time	t_{CONV}		15		72	μs
Analog input voltage	V_{IAN}		0		AV_{DD}/AV_{REF}	V_{REF}
Reference voltage	AV_{DD}/AV_{REF}		V_{DD} - 0.3		V_{DD} + 1.3	
AV_{DD}/AV_{REF} current	I_{ADD}	ADC running		1.0	2.0	mA
		ADC stopped		1.0	10	μA

Note: Overall error excluding quantization error (± 1/2 LSB). It is indicated as a ratio to the full-scale value.

Remark: fx: Main system clock oscillation frequency

Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85° C)

Table 10-15: Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V Note 2		0.1	10	μA
Release signal set time	t_{SREL}		0			μS
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt		**Note 1**		

Notes: **1.** In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of 212/fx and 214/fx to 217/fx is possible.
2. fx:RC oscillator is not used.

Remark: fx: Main system clock oscillation frequency

Figure 10-6: Data Retention Timing (STOP mode release by RESET)

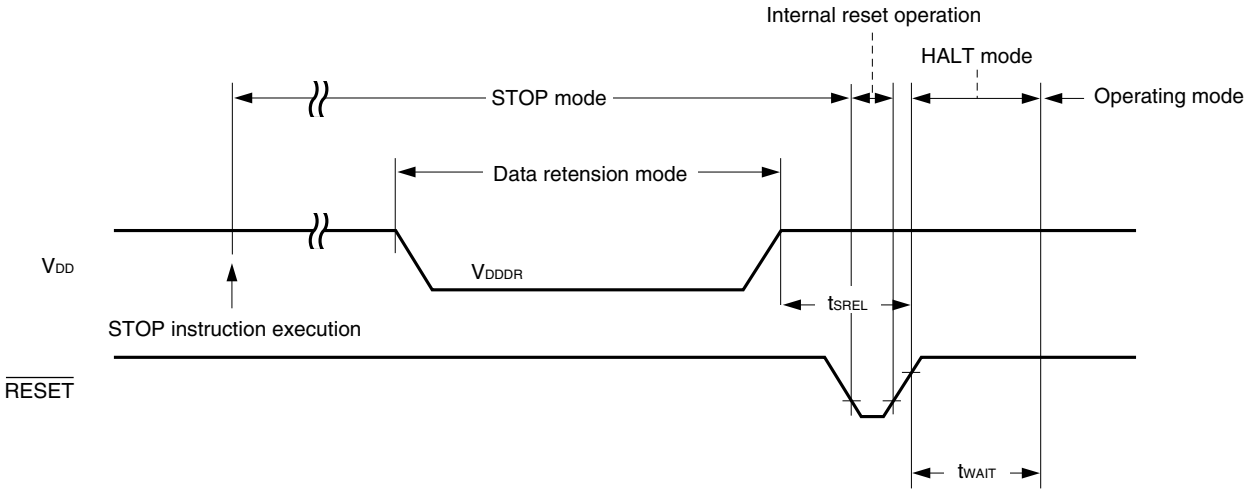


Figure 10-7: Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

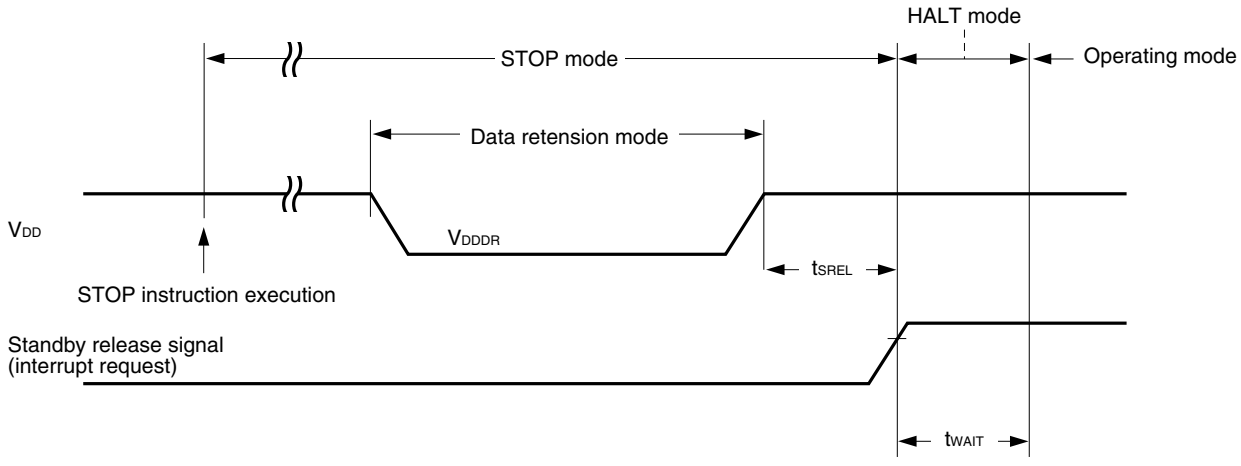


Figure 10-8: Interrupt Input Timing

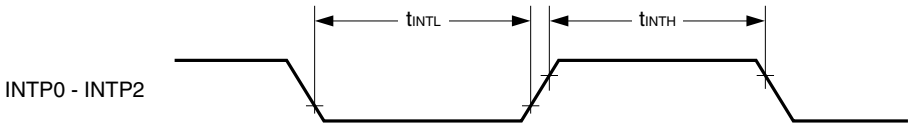
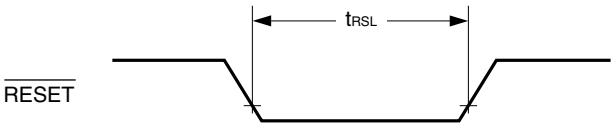


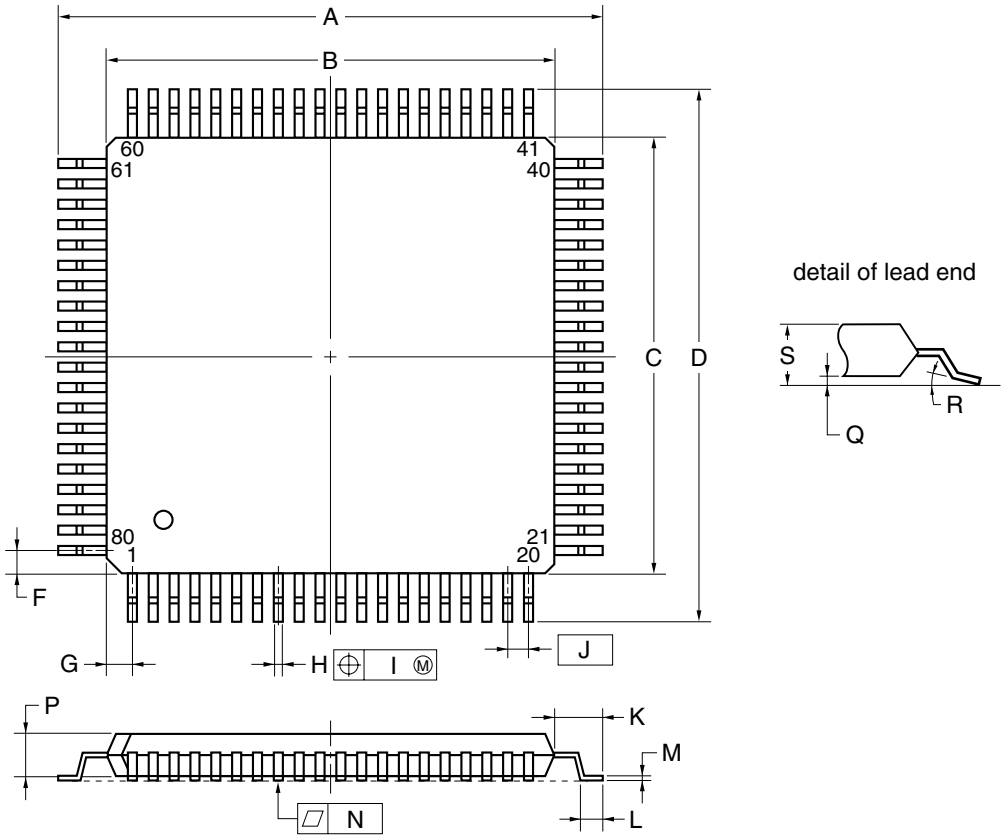
Figure 10-9: $\overline{\text{RESET}}$ Input Timing



11. Package Drawing

Figure 11-1: Package Drawing

80 PIN PLASTIC QFP (14×14)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

Remark: The shape and material of the ES product is the same as the mass produced product.

12. Recommended Soldering Conditions

The μPD1615A should be soldered and mounted under the conditions in the table below. For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (IEI-1207)**.
For soldering methods and conditions other than those recommended below, consult our sales personnel.

μPD1615AGC(A)-XXX-8BT : 80-pin plastic QFP (14 x 14 mm)
μPD1615BGC(A)-XXX-8BT : 80-pin plastic QFP (14 x 14 mm)
μPD1615FGC(A)-XXX-8BT : 80-pin plastic QFP (14 x 14 mm)
μPD1616FGC(A)-XXX-8BT : 80-pin plastic QFP (14 x 14 mm)

Table 12-1: Surface Mounting Type Soldering Conditions

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above). Number of times: twice max. <Precautions> (1) The second reflow schold be started after the first reflow device temperature has retumed to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 210 °C or above). Number of times: twice max. <Precautions> (3) The second reflow schold be started after the first reflow device temperature has retumed to the ordinary state. (4) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Wave soldering	Soldering bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: once, Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per device side).	-

Caution: Use of more than one soldering method should be avoided (exept in the case of pin part heating).

Appendix A. Development Tools

The following tools are available for system development using the μPD1615A(A).

Language Processing Software

NEC Software

RA78K0	Assembler package used in common for the 78K0 series
CC78K0	C compiler package used in common for the 78K0 series
DF1615A	Device file used for the μPD1615A Subseries
CC78K0-L	C compiler library source file used in common for the 78K0 series

IAR Software

A78000	Assembler package used for the 78K0 series
ICC78000	C compiler package used for the 78K0 series
XLINK	Linker package used for the 78K0 series

Flash EEPROM Writing Tools

*flash*MASTER	Dedicated flash writer for micro controllers with on-chip flash memory
FA-80GC-8BT	Programmer adapter connected to the *flash*MASTER

Debugging Tools

IE-78K0-NS-A	In-circuit emulator used in common for the 78K0 series
IE-70000-98-IF-C	Interface adapter when PC9800 series (except for notebooks) is used as host machine
IE-70000-PC-IF-C	Interface adapter when IBM PC/AT or its compatibles is used as host machine
IE-70000-PCI-IF-A	PCI Interface adapter when IBM PC/AT or its compatibles is used as host machine
IE-70000-CD-IF-A	PCI Interface adapter when IBM PC/AT or its compatibles is used as host machine
IE-78K0-NS-P04	Emulation board for the μPD1615A(A) Subseries
IE-1615-NS-EM4	Probe board for the μPD1615A(A) Subseries
NP-80GC-TQ	Emulation probe used in common for the μPD1615A(A) Subseries
NQPACK080SB	Socket for soldering on the target
YQPACK080SB	Adapter socket for connecting the probe to the NQPACK080SB
HQPACK080SB	Lid socket for connecting the device to the NQPACK080SB
YQSOCKET080SBF	Height adapter between the YQPACK080SB and the probe
ID78K0-NS	Integrated debugger for the IE-78K0-NS-A
SM78K0	System simulator used in common for the 78K0 series
DF1615A	Device file used for the μPD1615A(A) Subseries

Real-Time OS

RX78K0	Real-time OS used for the 78K0 series
MX78K0	OS used for the 78K0 series

Appendix B. Related Documents

Documents Related to Devices

Document	Document No.	
	Japanese	English
78K0 Series User s Manual-Instruction	IEU-849	IEU-1372
78K0 Series Instruction Table	IEM-5522	-
78K0 Series Instruction Set	IEM-5521	-
78K0 Series Application Note-Fundamental (III)	IEA-767	To be prepared

Documents on Development Tools (User's Manuals)

Document		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Reprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler Application Note	Programming Know-how	EEU-618	To be prepared
CC78K Series Library Source File		EEU-777	-
IE-78K0-NS-A		TBD	TBD
IE-78K0-NS-P04 IE-1615-NS-EM4		-	U13359E
NP-80GC-TQ		-	-
SM78K0 System Simulator	Reference	-	U10181
IBM PC/AT (PC DOS) Base	External Port Specification	-	U10092
ID78K0-NS Integrated Debugger IBM PC/AT (PC DOS) Base		U14379	U14379

Caution: The above documents are subject to change without notice. Be sure to use the latest documents for design or for any other similar purpose.

Documents on Embeded Software (User's Manuals)

Document		Document No.	
		Japanese	English
78K0 Series Real-time OS	Basic	EEU-912	-
	Installation	EEU-911	-
	Technical	EEU-913	-
78K0 Series OS MX78K0	Fundamental	EEU-5010	-
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEA-862	EEU-1444
78K0 Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K0 Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	-
Electrostatic Discharge (ESD) Test	MEM-539	-
Semiconductor Device Quality Assurance Guide	MEI-603	MEI-1202
Microcontroller-Related Product Guide - Third Party Products -	MEI-604	-

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Notes for CMOS Devices

① Precaution against ESD for Semiconductors

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② Handling of unused input pins for CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ Status before initialization of MOS devices

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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