PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

LAKI (µPD98503)

COMMUNICATION CONTROLLER

LAKI is a high performance controller which can perform TCP/IP and USB protocol stacks or other application system related software. It includes high performance MIPS™ based 64-bit RISC processor VR4120A™ CPU core, Ethernet™ controller, USB controller block, general purpose input/output functions and a memory/system-bus interface.

Detailed function descriptions are provided in the LAKI user's manual. Be sure to read the manual before designing.

FEATURES

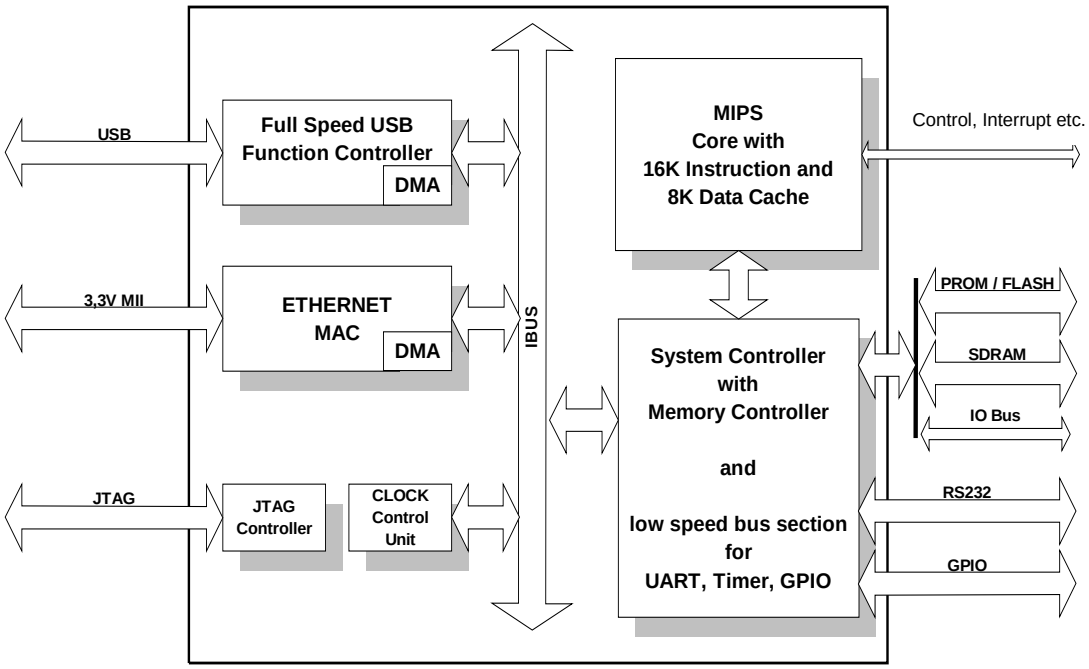
- Includes high performance MIPS based 64-bit RISC processor VR4120A
- Can perform RTOS and network middleware (M/W) on the chip
- Includes interface for PROM and flash ROM used for storing boot program
- Includes 10/100 Mbps Ethernet controllers compliant to IEEE802.3, IEEE802.3u and IEEE802.3x
- Can directly connect external Ethernet PHY device through 3.3-V MII interface
- Includes USB full speed function controller compliant to USB specification 1.1
- Supports operation conforming to the USB Communication Device Class Specification
- Can directly connect 64M-bit and 128M-bit SDRAM as external memory
- Includes boundary scan function (JTAG) compliant to IEEE 1149.1
- Includes Micro Wire™ interface
- Includes 2-channel general purpose timers
- Includes 16 general purpose input/output pins
- Using advanced CMOS technology
- Supply voltage 2.5 V (Required 3.3-V supply for 3.3-V interface)
- Package 256-pin Tape-BGA

ORDERING INFORMATION

Part Number	Package
µPD98503N7-B6	256-pin Tape BGA

Document No. S15581EE1V2DS00 (preliminary edition v1.2)
Date Published April 2001

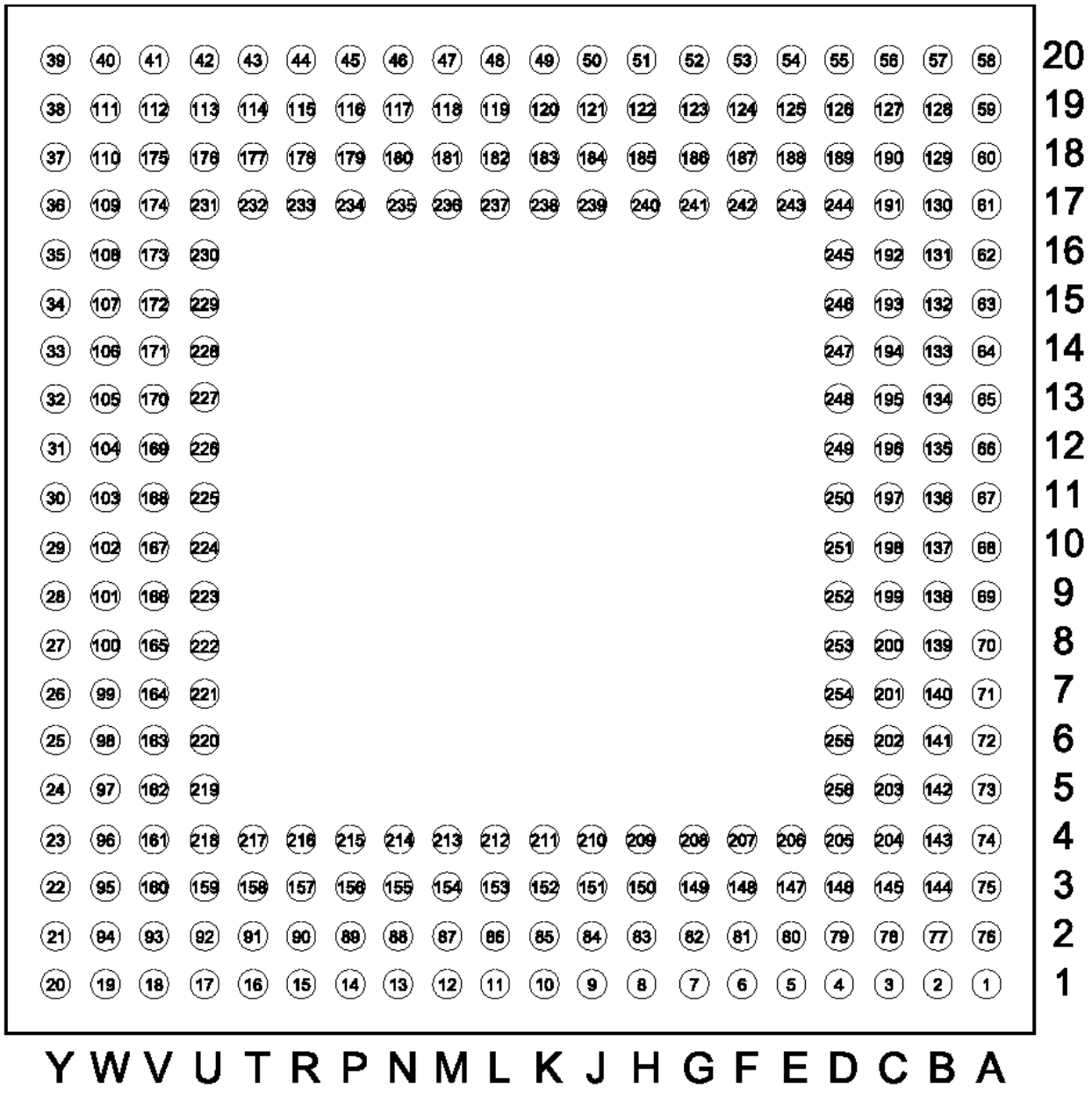
BLOCK DIAGRAM



PIN CONFIGURATION (Bottom View)

- **256-pin Tape-BGA**

(BOTTOM VIEW)



Pin Name

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A01	IC-PDn	C13	URDSR	H01	GND	P17	GND	V13	VDD2
A02	IC-Open	C14	VDD2	H02	VDD2	P18	VDD2	V14	VDD2
A03	ENDCEN	C15	URSDI	H03	GND	P19	SMD7	V15	SMD31
A04	RMSL0	C16	SMA4	H04	VDD3	P20	SMD6	V16	SMD27
A05	GPIO0	C17	SMA6	H17	VDD3	R01	MIRD3	V17	SMD24
A06	GPIO4	C18	VDD2	H18	GND	R02	MIRER	V18	VDD2
A07	GPIO6	C19	SMA12	H19	SEXCS2	R03	MIRDV	V19	SMD18
A08	GPIO8	C20	SMA14	H20	SDCS	R04	MITD0	V20	SMD16
A09	EXNMI	D01	GND	J01	IC-PDn	R17	SMD11	W01	MITER
A10	GPIO13	D02	IC-Open	J02	IC-PDn	R18	SMD10	W02	MITE
A11	GPIO14	D03	IC-Open	J03	IC-Open	R19	SMD9	W03	GND
A12	MWDI	D04	GND	J04	IC-Open	R29	SMD8	W04	JDI
A13	MWDO	D05	VDD3	J17	SDCKE1	T01	MITD1	W05	RSTB
A14	URDCD	D06	GPIO1	J18	SDRAS	T02	MITD2	W06	CLKSL
A15	URDTR	D07	GND	J19	SDCKE0	T03	MICRS	W07	SCLK
A16	SMA1	D08	VDD3	J20	SDCLK0	T04	GND	W08	PSAGND
A17	SMA3	D09	GPIO9	K01	IC-PDn	T17	VDD3	W09	PUAVD
A18	SMA5	D10	GND	K02	IC-PDn	T18	SMD14	W10	PUSTBY
A19	SMA8	D11	VDD3	K03	GND	T19	SMD12	W11	IC-PDn
A20	SMA9	D12	MWSK	K04	VDD2	T20	GND	W12	USBDP
B01	IC-PUp	D13	URRTS	K17	GND	U01	MITD3	W13	IC-Open
B02	IC-PDn	D14	GND	K18	VDD2	U02	MIRCLK	W14	IC-PDn
B03	IC-PDn	D15	SMA0	K19	SDCLK1	U03	IC-PDn	W15	IC-PDn
B04	IC-PDn	D16	VDD3	K20	GND	U04	GND	W16	GND
B05	RMSL1	D17	GND	L01	IC-PUp	U05	JDO	W17	SMD26
B06	GPIO3	D18	SMA13	L02	IC-PDn	U06	IC-Pup	W18	SMD23
B07	GPIO5	D19	SMA15	L03	VDD2	U07	GND	W19	SMD21
B08	GPIO7	D20	SMA16	L04	GND	U08	IC-Open	W20	SMD19
B09	GPIO11	E01	GND	L17	SDWE	U09	PSDVD	Y01	MIMCLK
B10	GPIO12	E02	VDD2	L18	IC-PDn	U10	PUDGND	Y02	IC-Open
B11	GPIO15	E03	IC-Open	L19	VDD3	U11	GND	Y03	JMS
B12	MWCS	E04	IC-Open	L20	SDCAS	U12	VDD3	Y04	JRSTB
B13	URCTS	E17	VDD3	M01	IC-PDn	U13	GND	Y05	IC-PUp
B14	URCLK	E18	GND	M02	IC-PDn	U14	GND	Y06	IC-PDn
B15	URSDO	E19	SMA17	M03	VDD2	U15	SMD30	Y07	PSTBY
B16	SMA2	E20	SMA18	M04	GND	U16	VDD3	Y08	PSAVD
B17	GND	F01	IC-PDn	M17	GND	U17	GND	Y09	PUAGND
B18	SMA7	F02	IC-PDn	M18	SMD2	U18	SMD17	Y10	IC-Open
B19	SMA10	F03	IC-PDn	M19	SMD1	U19	SMD15	Y11	USBCLK
B20	SMA11	F04	IC-Open	M20	SMD0	U20	SMD13	Y12	VDD3
C01	IC-Open	F17	SMA19	N01	GND	V01	MITCLK	Y13	IC-Open
C02	IC-PDnR	F18	SMA20	N02	MIMD	V02	MICOL	Y14	IC-Open
C03	VDD2	F19	SRMOE	N03	MIRD0	V03	VDD2	Y15	IC-PDn
C04	GND	F20	SRMCS	N04	VDD3	V04	JCK	Y16	SMD29
C05	BIG	G01	IC-PDn	N17	VDD3	V05	VDD3	Y17	SMD28
C06	GPIO2	G02	IC-PDn	N18	SMD5	V06	IC-PUp	Y18	SMD25
C07	VDD2	G03	VDD2	N19	SMD4	V07	VDD2	Y19	SMD22
C08	GND	G04	GND	N20	SMD3	V08	PSDGND	Y20	SMD20
C09	GPIO10	G17	GND	P01	MIRD1	V09	PUDVD		
C10	VDD2	G18	VDD2	P02	MIRD2	V10	IC-PDn		
C11	EXINT	G19	SEXCS0	P03	VDD2	V11	VDD2		
C12	GND	G20	SEXCS1	P04	GND	V12	USBDM		

Unnamed pins are internally connected and shall be unconnected in the system

Special pin name description:

IC-PDn: Pull Down

IC-PDnR: Pull Down with Resistor

IC-PUp: Pull Up

IC-PUpR: Pull Up with Resistor

IC-Open: Test output shall be left open

Remark In this document, XXX_B stands for active low pin.

CONTENTS

1. PIN FUNCTIONS

Symbol of I/O column indicates following status in this section.

I :Input
O :Output
I/O :Bidirection
I/OZ :Bidirection (Include Hi-Z state)
I/OD :Bidirection (Open drain output)
OZ :Output (Include Hi-Z state)
OD :Output (Open drain)

1.1 Power Supply

Pin Name	Pin No.	I/O	Active Level	Function
GND	4,5,8,13,43,49,95,108,130,150,152,185,188,196,200,204,205,208,212,213,215,217,218,221,225,227,228,231,234,236,238,241,244,247,251,254			GND (0 V)
IVDD	80,83,145,149,153,154,156,160,164,168,170,171,175,179,183,186,190,194,198,201,211			Internal logic core power supply (+2.5 V)
EVDD	31,119,162,209,214,226,230,232,235,240,243,245,250,253,256			External (I/O) power supply (+3.3 V)

1.2 System PLL Power Supply

(4 Pins)

Pin Name	Pin No.	I/O	Active Level	Function
PSAGND	100			Analog ground
PSAVD	27			Analog power supply (+2.5V)
PSDGND	165			Digital ground
PSDVD	223			Digital power supply (+2.5V)

The power supply pins of the System PLL shall be blocked with capacitors separately as closed to the device as possible.

1.3 USB PLL Power Supply

(4 pins)

Pin Name	Pin No.	I/O	Active Level	Function
PUAGND	28			Analog ground
PUAVD	101			Analog power supply (+2.5V)
PUDGND	224			Digital ground
PUDVD	166			Digital power supply (+2.5V)

The power supply pins of the USB PLL shall be blocked with capacitors separately as closed to the device as possible.

1.4 System Control Interface

(11 pins)

Pin Name	Pin No.	I/O	Active Level	Function
SCLK	99	I		System clock (33MHz)
CLKSL	98	I		Clock select (100MHz/66MHz)
PSTBY	26	I	H	System PLL standby mode control input
PUSTBY	102	I	H	USB PLL Standby mode control
BIG	203	I	H	V_R4120A Bigendian mode
ENDCEN	75	I		Big Endian mode enable
EXINT_B	197	I	L	External interrupt
EXNMI_B	69	I	L	External non-maskable interrupt
RST_B	97	I	L	System reset
ROMSEL0	74	I		ROM access bus width
ROMSEL1	142	I		(ROMSEL1/0=L/L;32bit, L/H;16bit, H/L;8bit)

1.5 Memory Interface

(66 pins)

(1/2)

Pin Name	Pin No.	I/O	Active Level	Function
SDCLK0	50	O		SDRAM Clock
SDCLK1	120	O		SDRAM Clock
SDCKE0	121	O	H	SDRAM Clock Enable
SDCKE1	239	O	H	SDRAM Clock Enable
SDCS_B	51	O	L	SDRAM Chip select
SDRAS_B	184	O	L	SDRAM Row address strobe
SDCAS_B	48	O	L	SDRAM Column address strobe
SDWE_B	237	O	L	SDRAM/PROM/FLASH write enable
SRMCS_B	53	O	L	PROM/FLASH chip select
SRMOE_B	124	O	L	PROM/FLASH output enable
SEXCS0_B	123	O	L	Extended Chip Select 0
SEXCS1_B	52	O	L	Extended Chip Select 1
SEXCS2_B	122	O	L	Extended Chip Select 2
SMA0	246	O		System Bus Address
SMA1	62	O		System Bus Address
SMA2	131	O		System Bus Address
SMA3	61	O		System Bus Address
SMA4	192	O		System Bus Address
SMA5	60	O		System Bus Address
SMA6	191	O		System Bus Address
SMA7	129	O		System Bus Address
SMA8	59	O		System Bus Address
SMA9	58	O		System Bus Address
SMA10	128	O		System Bus Address
SMA11	57	O		System Bus Address
SMA12	127	O		System Bus Address
SMA13	189	O		System Bus Address
SMA14	56	O		System Bus Address
SMA15	126	O		System Bus Address
SMA16	55	O		System Bus Address
SMA17	125	O		System Bus Address
SMA18	54	O		System Bus Address
SMA19	242	O		System Bus Address
SMA20	187	O		System Bus Address

(2/2)

Pin Name	Pin No.	I/O	Active Level	Function
SMD0	47	I/O		System Bus data
SMD1	118	I/O		System Bus data
SMD2	181	I/O		System Bus data
SMD3	46	I/O		System Bus data
SMD4	117	I/O		System Bus data
SMD5	180	I/O		System Bus data
SMD6	45	I/O		System Bus data
SMD7	116	I/O		System Bus data
SMD8	44	I/O		System Bus data
SMD9	115	I/O		System Bus data
SMD10	178	I/O		System Bus data
SMD11	233	I/O		System Bus data
SMD12	114	I/O		System Bus data
SMD13	42	I/O		System Bus data
SMD14	177	I/O		System Bus data
SMD15	113	I/O		System Bus data
SMD16	41	I/O		System Bus data
SMD17	176	I/O		System Bus data
SMD18	112	I/O		System Bus data
SMD19	40	I/O		System Bus data
SMD20	39	I/O		System Bus data
SMD21	111	I/O		System Bus data
SMD22	38	I/O		System Bus data
SMD23	110	I/O		System Bus data
SMD24	174	I/O		System Bus data
SMD25	37	I/O		System Bus data
SMD26	109	I/O		System Bus data
SMD27	173	I/O		System Bus data
SMD28	36	I/O		System Bus data
SMD29	35	I/O		System Bus data
SMD30	229	I/O		System Bus data
SMD31	172	I/O		System Bus data

1.6 Ethernet Interface

(18 pins)

Pin Name	Pin No.	I/O	Active Level	Function
MIRCLK	92	I		MII - Receive clock (25MHz)
MIMCLK	20	O		MII - management clock
MIMD	88	I/O		MII - management
MICOL	93	I		MII - Collision
MICRS	158	I		MII - carrier Sense
MIRDV	157	I		MII - Receive data valid
MIRER	90	I		MII - Receive error
MIRD0	155	I		MII - Receive data
MIRD1	14	I		MII - Receive data
MIRD2	89	I		MII - Receive data
MIRD3	15	I		MII - Receive data
MITCLK	18	I		MII - Transmit clock (25MHz)
MITE	94	O		MII - Transmit enable
MITER	19	O		MII - Transmit error
MITD0	216	O		MII - Transmit data
MITD1	16	O		MII - Transmit data
MITD2	91	O		MII - Transmit data
MITD3	17	O		MII - Transmit data

1.7 UART and Micro Wire Interface

(12 pins)

Pin Name	Pin No.	I/O	Active Level	Function
URCLK	133	I		UART external Clock
URSDO	132	O		UART serial data output
URSDI	193	I		UART serial data input
URDTR_B	63	O	L	UART data terminal ready
URRTS_B	248	O	L	UART data request to send
URCTS_B	134	I	L	UART clear to send
URDCD_B	64	I	L	UART data carrier detect
URDSR_B	195	I	L	UART data set ready
MWDI	66	I		Micro Wire data in
MWSK	249	O		Micro Wire SK
MWCS	135	O		Micro Wire chip select
MWDO	65	O		Micro Wire data out

1.8 USB Interface

(3 pins)

Pin Name	Pin No.	I/O	Active Level	Function
USBCLK	30	I		External USB clock
USBDM	169	I/O		USB data (-)
USBDP	104	I/O		USB data (+)

1.9 Parallel Port Interface

(16 pins)

Pin Name	Pin No.	I/O	Active Level	Function
GPIO0	73	I/O		General Purpose Input/Output
GPIO1	255	I/O		General Purpose Input/Output
GPIO2	202	I/O		General Purpose Input/Output
GPIO3	141	I/O		General Purpose Input/Output
GPIO4	72	I/O		General Purpose Input/Output
GPIO5	140	I/O		General Purpose Input/Output
GPIO6	71	I/O		General Purpose Input/Output
GPIO7	139	I/O		General Purpose Input/Output
GPIO8	70	I/O		General Purpose Input/Output
GPIO9	252	I/O		General Purpose Input/Output
GPIO10	199	I/O		General Purpose Input/Output
GPIO11	138	I/O		General Purpose Input/Output
GPIO12	137	I/O		General Purpose Input/Output
GPIO13	68	I/O		General Purpose Input/Output
GPIO14	67	I/O		General Purpose Input/Output
GPIO15	136	I/O		General Purpose Input/Output

1.10 Boundary Scan Interface

(5 pins)

Pin Name	Pin No.	I/O	Active Level	Function
JCK	161	I		B-SCAN clock
JDI	96	I		B-SCAN input-data
JDO	219	OZ		B-SCAN output-data
JMS	22	I		B-SCAN mode select
JRSTB_B	23	I	L	B-SCAN reset

In general all above specified functional pins (and no kind of power supply pins) are included in the boundary scan chain, with the following exceptions: USBDM, USBDP, SDCLK0, SDCLK1

Beside the above specified functional pins, the scan chain includes some of the non-specified test-pins.

The boundary scan device part number is 0503 (hex)

1.11 I.C. - Open

Pin Name	Pin No.	I/O	Active Level	Function
IC-Open	*3,21,29,32,33,76,79,105,146,147,151,206, 207,210,222*	O		Test output pins which *must be left unconnected*

1.12 I.C. - Pull Down

Pin Name	Pin No.	I/O	Active Level	Function
IC-PDn	*25,167,159,*34,107,106,*103,* 1,77,*144,86,143,12,87,* 6,7,9,10,81,82,84,85,148,182	I		Test input pins which a) *must be connected* b) shall be connected to GND

1.13 I.C. - Pull Down with Resistor (50Kohm)

Pin Name	Pin No.	I/O	Active Level	Function
IC-PDnR	78,	I/O		Test inputs which shall be connected externally to GND through a resistor

1.14 I.C. - Pull Up

Pin Name	Pin No.	I/O	Active Level	Function
IC-Pup	*24,*11,*2,*163,220	I		Test input pins which a) *must be connected* b) shall be connected to EVDD

1.15 I.C. - Pull Up with Resistor (50Kohm)

Pin Name	Pin No.	I/O	Active Level	Function
IC-PupR	N/a	I/O		Test inputs which shall be connected externally to EVDD through a resistor

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	IV_{DD}	Internal logic core	–0.5 to +3.6	V
	EV_{DD}	I/O buffer	–0.5 to +4.6	V
Input/output voltage	V_{I1}/V_{O1}	LVTTL-level pin	–0.5 to +4.6	V
	V_{I2}/V_{O2}	LVTTL-level 5V-torelant pin	–0.5 to +7.3	V
	V_{I3}/V_{O3}	USB I/O buffer	–0.5 to +4.6	V
Output current	I_{O1}	LVTTL-level pin, I_{OL} = 9 mA	30	mA
	I_{O2}	LVTTL-level 5V-torelant pin	T.B.D.	mA
	I_{O3}	USB I/O buffer, I_{OL} = 18 mA	55	mA
Storage temperature	T_{stg}		–60 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	IV_{DD}		2.3	2.5	2.7	V
	EV_{DD}		3.0	3.3	3.6	V
Low level input voltage	V_{IL1}	LVTTL-level pin	0		0.8	V
	V_{IL2}	LVTTL-level pin, 5V-torelant pin	–1.8		0.8	V
	V_{IL3}	USB I/O/ buffer (Single-end operation)			0.8	V
High level input voltage	V_{IH1}	LVTTL-level pin	2.0			V
	V_{IH2}	LVTTL-level pin, 5V-torelant pin	2.0			V
	V_{IH3}	USB I/O/ buffer (Single-end operation)	2.0			V
USB differential input voltage	V_{IDF}	USB I/O buffer (Differential operation)	0.2			V
Operating ambient temperature	T_A		0		70	°C

DC Characteristics (IV_{DD} = 2.5 ± 0.2 V, EV_{DD} = 3.3 ± 0.3 V, T_A = 0 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	II_{DD}			T.B.D.	650	mA
Supply current	EI_{DD}			T.B.D.	100	mA
Input leakage current	I_{LI}	V_I = EV_{DD} or GND			±10	μA
Off state output current	I_{OZ}	V_O = V_{DD} or GND			±10	mA
Low level output voltage	V_{OL1}	LVTTL-level pin, I_{OL} = 9 mA			0.4	V
	V_{OL2}	LVTTL-level 5V-tolerant pin, I_{OL} = 4 mA			0.5	V
	V_{OL3}	USB I/O buffer, Pull up with resistor (1.5 kΩ) to EV_{DD}			0.3	V
High level output voltage	V_{OH1}	LVTTL-level pin, I_{OL} = 9mA	2.4			V
	V_{OH2}	LVTTL-level 5V-tolerant pin, I_{OL} = 4 mA	2.4			V
	V_{OH3}	USB I/O buffer, Pull down with resistor (15 kΩ) to GND	2.8		EV_{DD}	V

Pin Classifications

NOTE: I/O pins are listed twice - in the input and in the output section !

Input pins

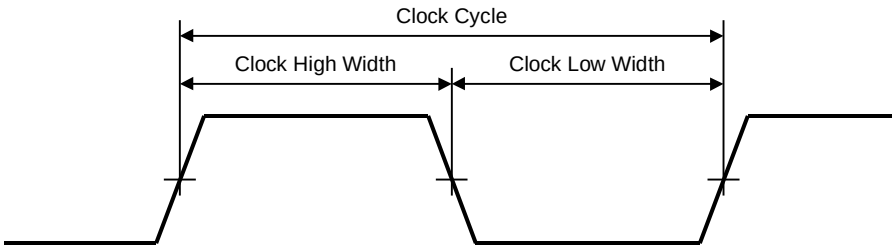
Category		Application Pins	Number of Pins
LVTTL-level pin	V_{I1}, V_{IL1}/V_{IH1}	SCLK, CLKSL, PSTBY, PUSTBY, BIG, ENDCEN, EXINT_B, EXNMI_B, RST_B, ROMSEL[1:0], SMD[31:0], USBCLK, URCLK, URSDI, MWDI, URCTS_B, URDCD_B, URDSR_B, GPIO[15:0], JCK, JDI, JMS, JRSTB_B,	70
LVTTL-level 5V-tolerant pin	V_{I2}, V_{IL2}/V_{IH2}	MIRCLK, MIMD, MICOL, MICRS, MIRDV, MIRER, MIRD[3:0], MITCLK	11
USB I/O buffer	V_{I3}, V_{IL3}/V_{IH3}, V_{IDF}	USBDP, USBDM	2

Output pins

Category			Application Pins	Number of Pins
LVTTL-level pin	I_{O1}	V_{O1}, V_{OL1}/V_{OH1}	SDCLK0, SDCLK1, SDCKE0, SDCKE1, SDCS_B, SDRAS_B, SDCAS_B, SDWE_B, SRMCS_B, SRMOE_B, SEXCS0_B, SEXCS1_B, SEXCS2_B, SMA[20:0], SMD[31:0], URSDO, URDTR_B, URRTS_B, MWSK, MWCS, MWDO, GPIO[15:0], JDO	89
LVTTL-level 5V-tolerant pin	I_{O2}	V_{O2}, V_{OL2}/V_{OH2}	MIMCLK, MIMD, MITE, MITER, MITD[3:0]	8
USB I/O buffer	I_{O3}	V_{O3}, V_{OL3}/V_{OH3}	USBDP, USBDM	2

AC Characteristics (IV_{DD} = 2.5 ± 0.2 V, EV_{DD} = 3.3 ± 0.3 V, T_A = 0 to +70 °C)

(1) Clock Parameter



(1)-1 Clock Input

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLK Input Cycle	t_{CYSCK}		30.00	40.00	ns
SCLK Input High Width	t_{WHSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
SCLK Input Low Width	t_{WLSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
MITCLK Input Cycle	t_{CYMTK}		40.00	400.00	ns
MITCLK Input High Width	t_{WHMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
MITCLK Input Low Width	t_{WLMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
MIRCLK Input Cycle	t_{CYMRK}		40.00	400.00	ns
MIRCLK Input High Width	t_{WHMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
MIRCLK Input Low Width	t_{WLMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
USBCLK Input Cycle	t_{CYUBK}		83.12	84.54	ns
USBCLK Input High Width	t_{WHUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
USBCLK Input Low Width	t_{WLUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
JCK Input Cycle	t_{CYJCK}		200.00	1000.00	ns
JCK Input High Width	t_{WHJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns
JCK Input Low Width	t_{WLJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns

Note:

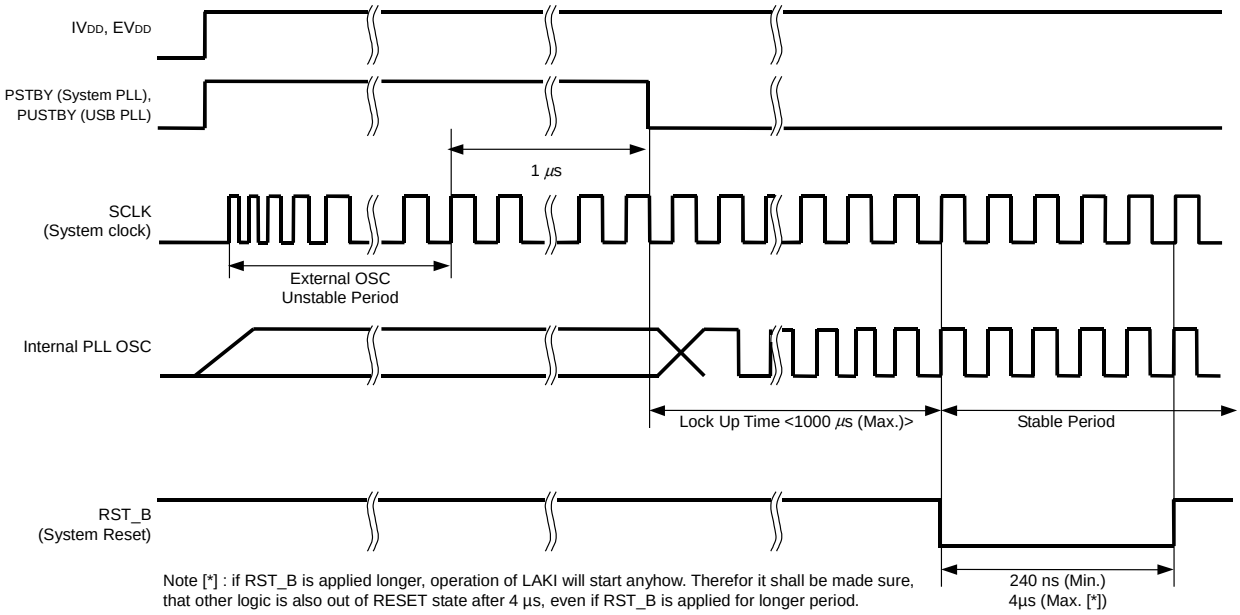
- for SCLK, USBCLK usage of a 100ppm oscillator circuit is recommended
- for MITCLK/MIRCLK the required stability normally depends on the used Ethernet PHY. In many cases 100ppm oscillators are recommended
- The PLL clock input signals (USBCLK and SCLK) shall be derived from a dedicated driving device to ensure short rise and fall times. Normally the clock signals shall not be passed through a resistor.

(1)-2 Clock Output

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCLK0 Output Cycle	t_{CYSK0}	Load 30 pF	10.00	15.00	ns
SDCLK0 Output High Width	t_{WHSK0}	Load 30 pF	$0.4 \times t_{CYSK0}$	$0.6 \times t_{CYSK0}$	ns
SDCLK0 Output Low Width	t_{WLSK0}	Load 30 pF	$0.4 \times t_{CYSK0}$	$0.6 \times t_{CYSK0}$	ns
SDCLK1 Output Cycle	t_{CYSK1}	Load 30 pF	10.00	15.00	ns
SDCLK1 Output High Width	t_{WHSK1}	Load 30 pF	$0.4 \times t_{CYSK1}$	$0.6 \times t_{CYSK1}$	ns
SDCLK1 Output Low Width	t_{WLSK1}	Load 30 pF	$0.4 \times t_{CYSK1}$	$0.6 \times t_{CYSK1}$	ns
MIMCLK Output Cycle	t_{CYMCK}	Load 50 pF	420.00		ns
MIMCLK Output High Width	t_{WHMCK}	Load 50 pF	$0.4 \times t_{CYMCK}$		ns
MIMCLK Output Low Width	t_{WLMCK}	Load 50 pF	$0.4 \times t_{CYMCK}$		ns

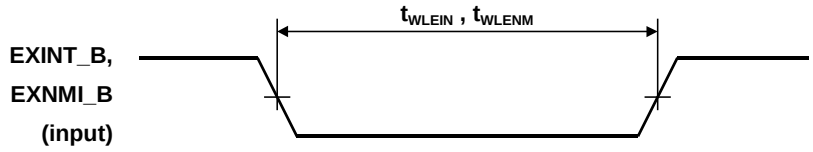
Note: The value $t_{CYSDCLK}$ which is referenced later on in this document refers to the cycle time of the signals SDCLK0/1 defined in above table.

(2) Reset Parameter



Note [*] : if RST_B is applied longer, operation of LAKI will start anyhow. Therefor it shall be made sure, that other logic is also out of RESET state after 4 µs, even if RST_B is applied for longer period.

(3) Interrupt Interface Parameter



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
EXINT_B Input Low Width	t_{WLEIN}		$4 \times t_{CYSK0/1}$		ns
EXNMI_B Input Low Width	t_{WLENM}		$4 \times t_{CYSK0/1}$		ns

(4) Clock Control Parameter

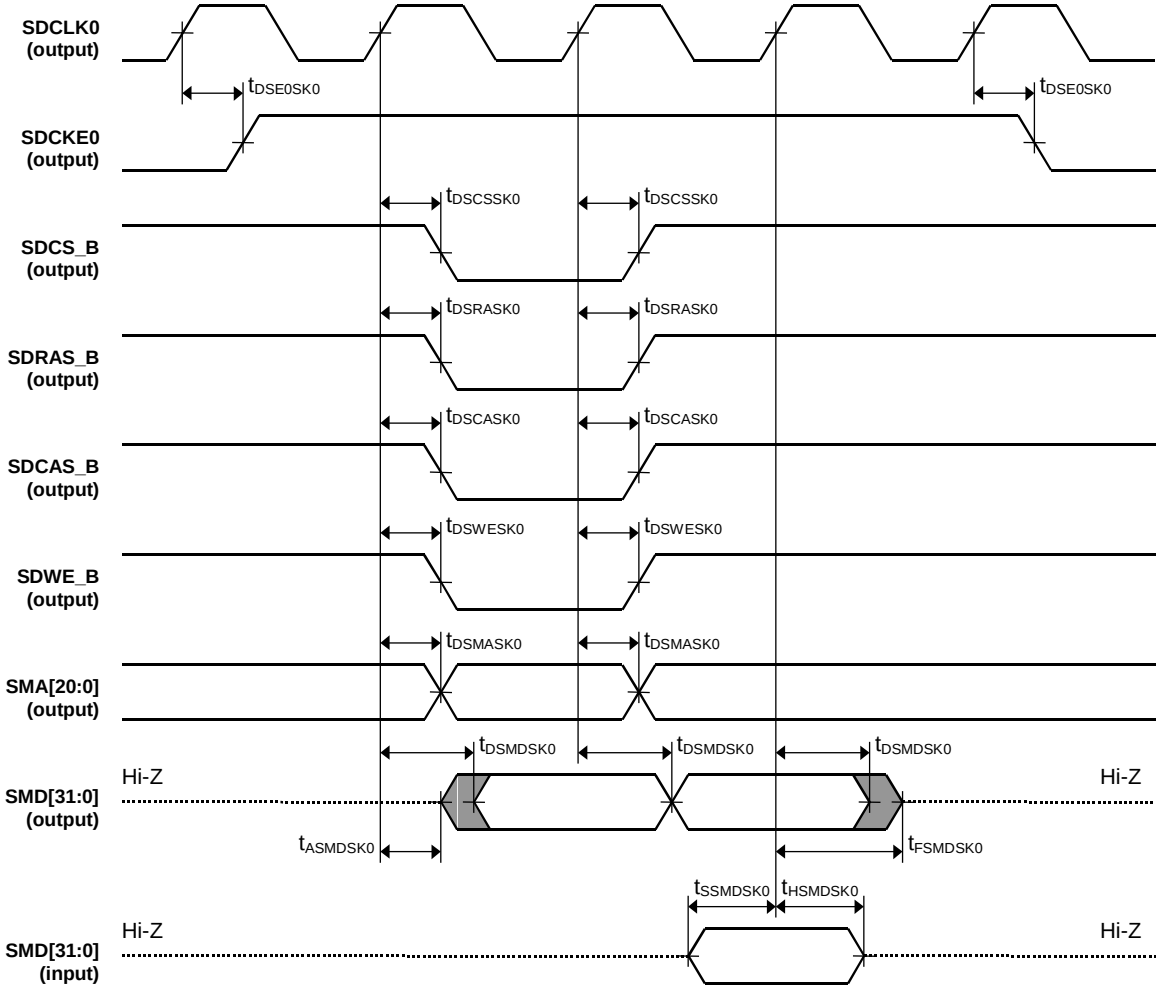
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CLKSL Setup Time	t_{SCKS}	None, static signal			ns
CLKSL Hold Time	t_{HCKS}	None, static signal			ns

(5) System Interface Parameter

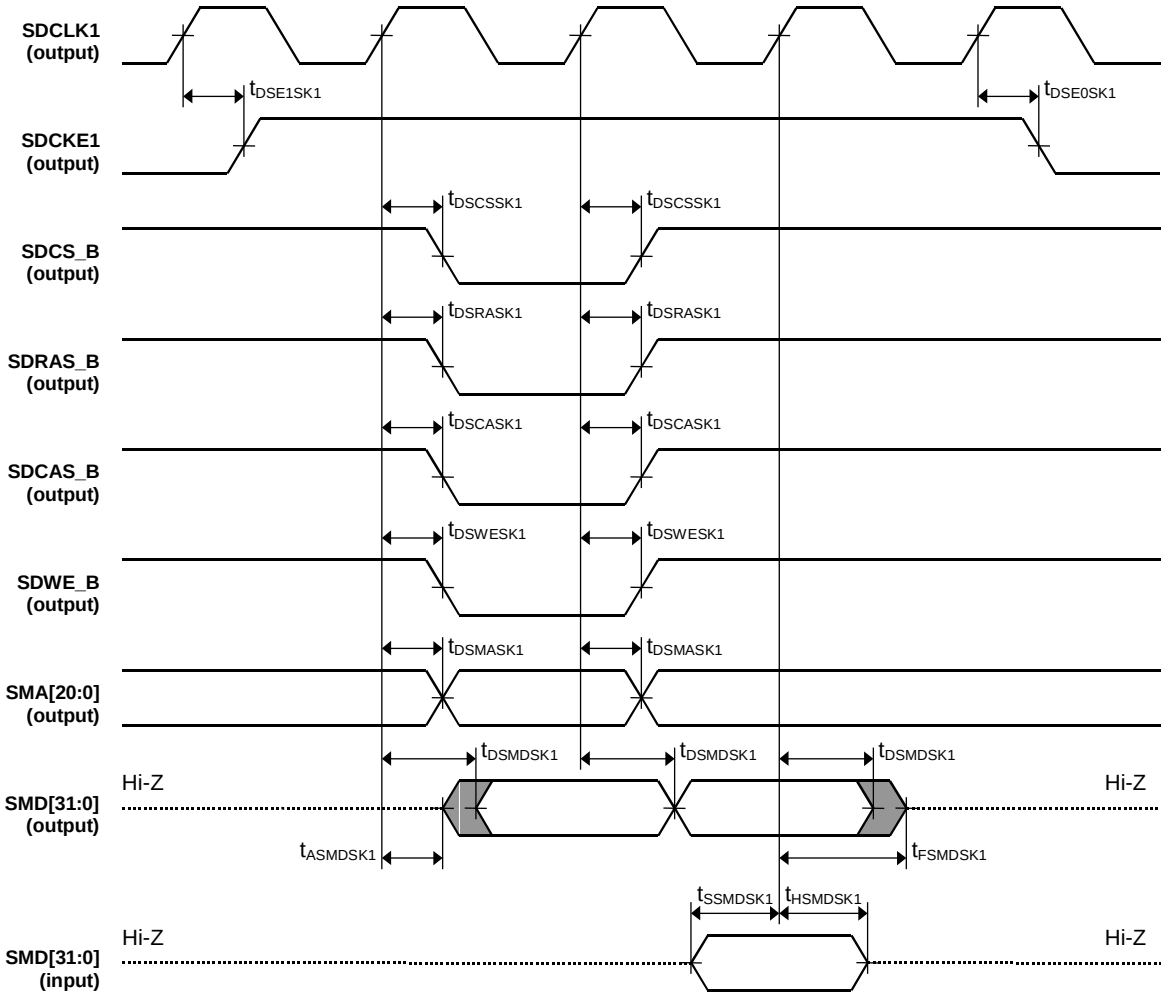
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
BIG Setup Time	t_{SBIG}	None, static signal			ns
BIG Hold Time	t_{HBIG}	None, static signal			ns
ENDCEN Setup Time	t_{SEND}	None, static signal			ns
ENDCEN Hold Time	t_{HEND}	None, static signal			ns

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ROMSEL[1:0]		None, static signal			ns

(6) System Bus - SDRAM interface parameter



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCKE0 Output Delay from SDCLK0	$t_{DSE0SK0}$	Load 30 pF	1.00	8.00	ns
SDCS_B Output Delay from SDCLK0	$t_{DSCSSK0}$	Load 30 pF	1.00	8.00	ns
SDRAS_B Output Delay from SDCLK0	$t_{DSRASK0}$	Load 30 pF	1.00	8.00	ns
SDCAS_B Output Delay from SDCLK0	$t_{DSCASK0}$	Load 30 pF	1.00	8.00	ns
SDWE_B Output Delay from SDCLK0	$t_{DSWESK0}$	Load 30 pF	1.00	8.00	ns
SMA[20:0] Output Delay from SDCLK0	$t_{DSMASK0}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Floating to Active Delay from SDCLK0	$t_{ASMDSK0}$	Load 30 pF	1.00		ns
SMD[31:0] Output Delay from SDCLK0	$t_{DSMDSK0}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Active to Floating Delay from SDCLK0	$t_{FSMDSK0}$	Load 30 pF		8.00	ns
SMD[31:0] Input Setup to SDCLK0	$t_{SSMDSK0}$		4.00		ns
SMD[31:0] Input Hold from SDCLK0	$t_{HSMDSK0}$		1.00		ns

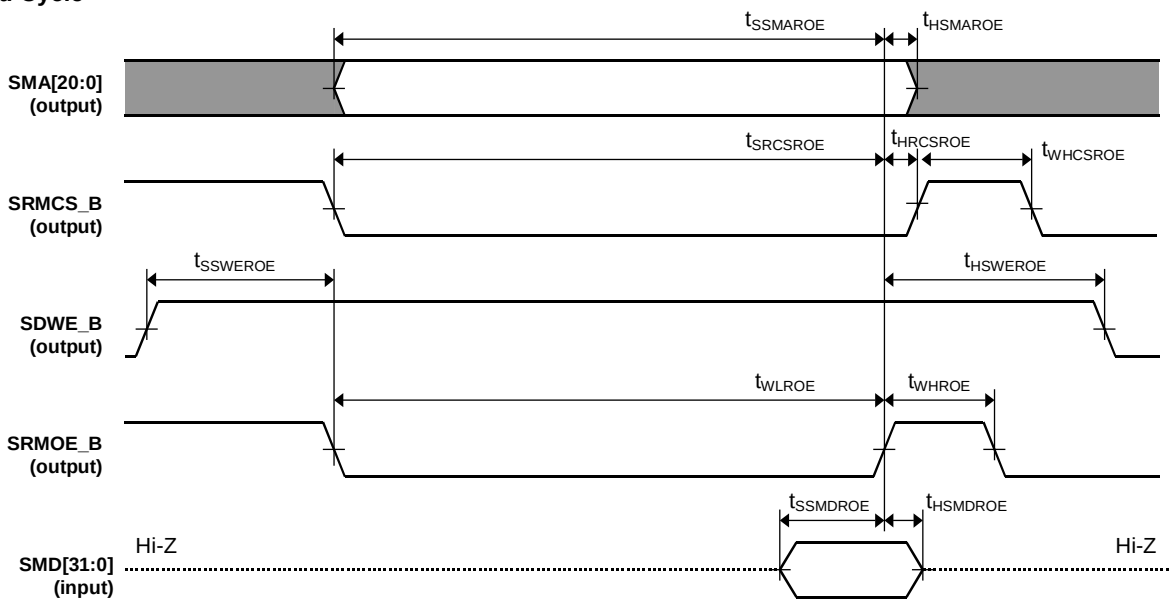


Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCKE1 Output Delay from SDCLK1	$t_{DSE1SK1}$	Load 30 pF	1.00	8.00	ns
SDCS_B Output Delay from SDCLK1	$t_{DSCSSK1}$	Load 30 pF	1.00	8.00	ns
SDRAS_B Output Delay from SDCLK1	$t_{DSRASK1}$	Load 30 pF	1.00	8.00	ns
SDCAS_B Output Delay from SDCLK1	$t_{DSCASK1}$	Load 30 pF	1.00	8.00	ns
SDWE_B Output Delay from SDCLK1	$t_{DSWESK1}$	Load 30 pF	1.00	8.00	ns
SMA[20:0] Output Delay from SDCLK1	$t_{DSMASK1}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Floating to Active Delay from SDCLK1	$t_{ASMDSK1}$	Load 30 pF	1.00		ns
SMD[31:0] Output Delay from SDCLK1	$t_{DSMDSK1}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Active to Floating Delay from SDCLK1	$t_{FSMDSK1}$	Load 30 pF		8.00	ns
SMD[31:0] Input Setup to SDCLK1	$t_{SSMDSK1}$		4.00		ns
SMD[31:0] Input Hold from SDCLK1	$t_{HSMDSK1}$		1.00		ns

(7) System Bus - Flash ROM Interface Parameter

Note: FAT timing parameter and bus width selection is equivalent for Flash ROM (SRMCS_B area) and IO Bus (SEXCS[2..0]_B area) access.

<Read Cycle>



Parameter	Symbol	Condition	MIN.	MAX.	Unit
SMA[20:0] Setup to SRMOE_B	$t_{SSMAROE}$	Load 30 pF	(FAT+1) × $t_{CYSDCLK}$ – 3		ns
SMA[20:0] Hold from SRMOE_B	$t_{HSMAROE}$	Load 30 pF	1 × $t_{CYSDCLK}$ – 3		ns
SRMCS_B Setup to SRMOE_B	$t_{SRCSROE}$	Load 30 pF	(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SRMCS_B Hold from SRMOE_B	$t_{HRCSROE}$	Load 30 pF	-1		ns
SRMCS_B High Pulse Width	$t_{WHCSROE}$	Load 30 pF	1 × $t_{CYSDCLK}$ – 2 [(a)] 7 × $t_{CYSDCLK}$ – 2 [(b)]		ns
SDWE_B Setup Time to SRMOE_B	$t_{SSWEROE}$	Load 30 pF	2 × $t_{CYSDCLK}$ – 3		ns
SDWE_B Hold Time from SRMOE_B	$t_{HSWEROE}$	Load 30 pF	7 × $t_{CYSDCLK}$ – 2		ns
SRMOE_B Low Pulse Width	t_{WLROE}	Load 30 pF	(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SRMOE_B High Pulse Width	t_{WHROE}	Load 30 pF	1 × $t_{CYSDCLK}$ – 2 [(a)] 7 × $t_{CYSDCLK}$ – 2 [(b)]		ns
SMD[31:0] Setup to SRMOE_B	$t_{SSMDROE}$		11		ns
SMD[31:0] Hold from SRMOE_B	$t_{HSMDROE}$		-1		ns

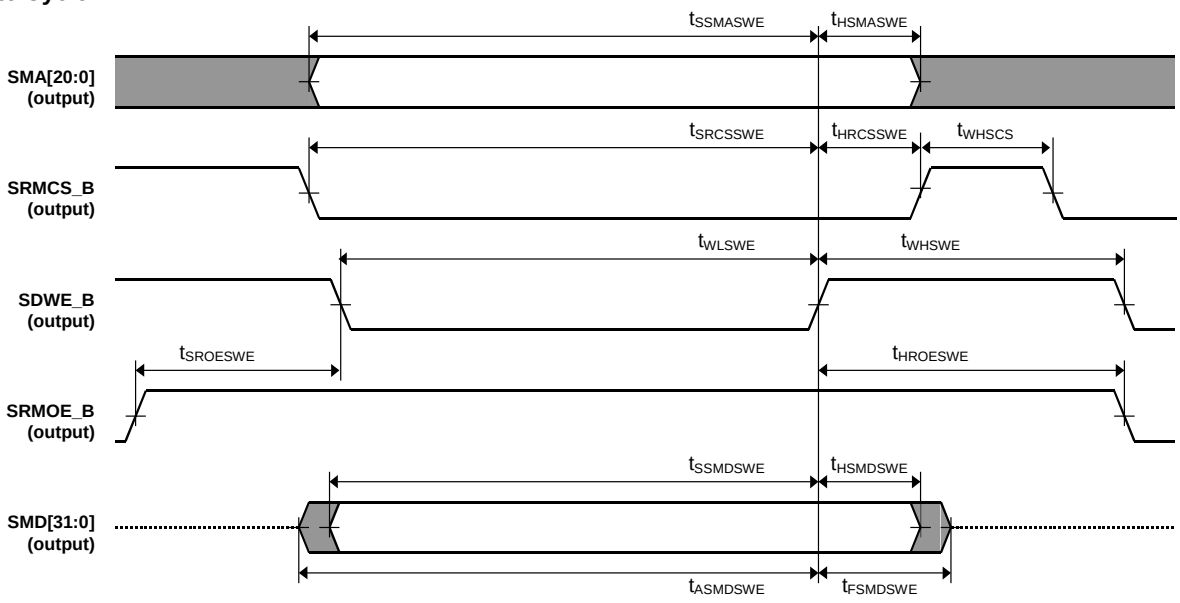
(a) in case of burst transfers

(b) in case of subsequent non-burst single word transfers (only possible for 32bit bus width)

NOTE: FAT is programmed in register RMATR according the following table

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

<Write Cycle>



Parameter	Symbol	Condition	MIN.	MAX.	Unit
SMA[20:0] Setup to SDWE_B	$t_{SSMASWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SMA[20:0] Hold from SDWE_B	$t_{HSMASWE}$	Load 30 pF	2 × $t_{CYSDCLK}$ - 4		ns
SRMCS_B Setup to SDWE_B	$t_{SRCSSWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SRMCS_B Hold from SDWE_B	$t_{HRCSSWE}$	Load 30 pF	1 × $t_{CYSDCLK}$ - 4		ns
SDMCS_B High Pulse Width	t_{WHSCS}	Load 30 pF	1 × $t_{CYSDCLK}$ – 2 (c)		ns
SRMOE_B Setup Time to SDWE_B	$t_{SROESWE}$	Load 30 pF	7 × $t_{CYSDCLK}$ – 2		ns
SRMOE_B Hold Time from SDWE_B	$t_{HROESWE}$	Load 30 pF	2 × $t_{CYSDCLK}$ – 3		ns
SDWE_B Low Pulse Width	t_{WLSWE}	Load 30 pF	(FAT-1) × $t_{CYSDCLK}$ – 2		ns
SDWE_B High Pulse Width	t_{WHSWE}	Load 30 pF	3 × $t_{CYSDCLK}$ – 2 (a) 6 × $t_{CYSDCLK}$ – 2 (b)		ns
SMD[31:0] Setup to SDWE_B	$t_{SSMDSWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SMD[31:0] Hold from SDWE_B	$t_{HSMDSWE}$	Load 30 pF	1 × $t_{CYSDCLK}$ - 4	1 × $t_{CYSDCLK}$ + 2	ns
SMD[31:0] Output Hi-Z to Valid Delay	$t_{ASMDSWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SMD[31:0] Output Valid to Hi-Z Delay	$t_{FSMDSWE}$	Load 30 pF	1 × $t_{CYSDCLK}$ - 5	1 × $t_{CYSDCLK}$ + 2	ns

(a) in case of burst transfers

(b) in case of subsequent non-burst single word transfers (only possible for 32bit bus width)

(c) To extend this short timing, it is recommended to insert a read access to the RMMDR register after a bus write access, which is directly followed by a bus read access cycle.

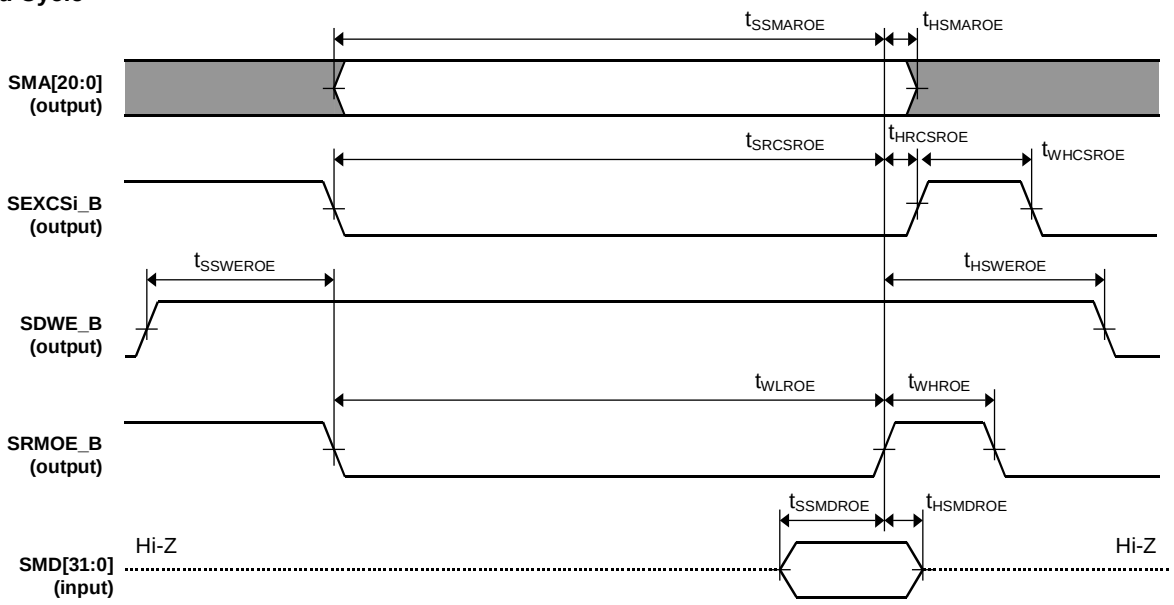
NOTE: FAT is programmed in register RMATR according the following table

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

(8) System Bus - Extended Chip Select Interface Parameter

Note: FAT timing parameter and bus width selection is equivalent for Flash ROM (SRMCS_B area) and IO Bus (SEXCS[2..0]_B area) access.

<Read Cycle>



Parameter	Symbol	Condition	MIN.	MAX.	Unit
SMA[20:0] Setup to SRMOE_B	$t_{SSMAROE}$	Load 30 pF	(FAT+1) × $t_{CYSDCLK}$ – 3		ns
SMA[20:0] Hold from SRMOE_B	$t_{HSMAROE}$	Load 30 pF	1 × $t_{CYSDCLK}$ – 3		ns
SEXCSi_B Setup to SRMOE_B	$t_{SRCSROE}$	Load 30 pF	(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SEXCSi_B Hold from SRMOE_B	$t_{HRCSROE}$	Load 30 pF	-1		ns
SEXCSi_B High Pulse Width	$t_{WHCSROE}$	Load 30 pF	1 × $t_{CYSDCLK}$ – 2 [(a)] 7 × $t_{CYSDCLK}$ – 2 [(b)]		ns
SDWE_B Setup Time to SRMOE_B	$t_{SSWEROE}$	Load 30 pF	2 × $t_{CYSDCLK}$ – 3		ns
SDWE_B Hold Time from SRMOE_B	$t_{HSWEROE}$	Load 30 pF	7 × $t_{CYSDCLK}$ – 2		ns
SRMOE_B Low Pulse Width	t_{WLROE}	Load 30 pF	(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SRMOE_B High Pulse Width	t_{WHROE}	Load 30 pF	1 × $t_{CYSDCLK}$ – 2 [(a)] 7 × $t_{CYSDCLK}$ – 2 [(b)]		ns
SMD[31:0] Setup to SRMOE_B	$t_{SSMDROE}$		11		ns
SMD[31:0] Hold from SRMOE_B	$t_{HSMDROE}$		-1		ns

(a) in case of burst transfers

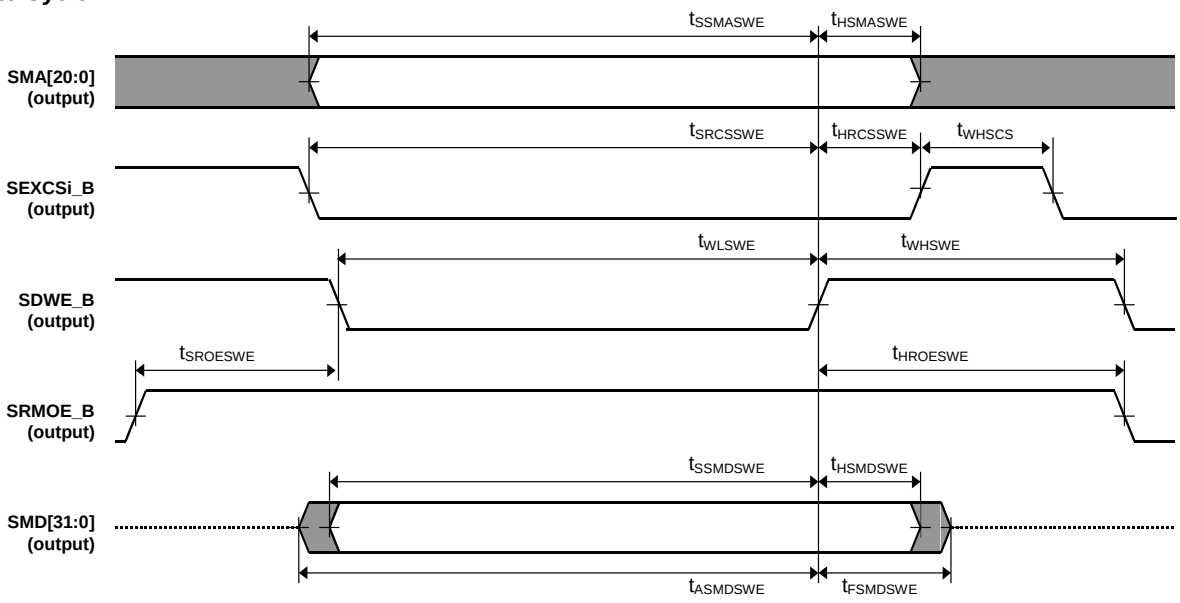
(b) in case of subsequent non-burst single word transfers (only possible for 32bit bus width)

NOTE: i=0,1,2

NOTE: FAT is programmed in register RMATR according the following table

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

<Write Cycle>



Parameter	Symbol	Condition	MIN.	MAX.	Unit
SMA[20:0] Setup to SDWE_B	$t_{SSMASWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SMA[20:0] Hold from SDWE_B	$t_{HSMASWE}$	Load 30 pF	2 × $t_{CYSDCLK}$ - 4		ns
SEXCSi_B Setup to SDWE_B	$t_{SRCSSWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SEXCSi_B Hold from SDWE_B	$t_{HRCSSWE}$	Load 30 pF	2 × $t_{CYSDCLK}$ - 4		ns
SEXCSi_B High Pulse Width	t_{WHSCS}	Load 30 pF	1 × $t_{CYSDCLK}$ – 2 (c)		ns
SRMOE_B Setup Time to SDWE_B	$t_{SROESWE}$	Load 30 pF	7 × $t_{CYSDCLK}$ – 2		ns
SRMOE_B Hold Time from SDWE_B	$t_{HROESWE}$	Load 30 pF	2 × $t_{CYSDCLK}$ – 3		ns
SDWE_B Low Pulse Width	t_{WLSWE}	Load 30 pF	(FAT-1) × $t_{CYSDCLK}$ – 2		ns
SDWE_B High Pulse Width	t_{WHSWE}	Load 30 pF	3 × $t_{CYSDCLK}$ – 2 (a) 6 × $t_{CYSDCLK}$ – 2 (b)		ns
SMD[31:0] Setup to SDWE_B	$t_{SSMDSWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SMD[31:0] Hold from SDWE_B	$t_{HSMDSWE}$	Load 30 pF	1 × $t_{CYSDCLK}$ - 4	1 × $t_{CYSDCLK}$ + 2	ns
SMD[31:0] Output Hi-Z to Valid Delay	$t_{ASMDSWE}$	Load 30 pF	FAT × $t_{CYSDCLK}$ – 2		ns
SMD[31:0] Output Valid to Hi-Z Delay	$t_{FSMDSWE}$	Load 30 pF	1 × $t_{CYSDCLK}$ - 4	1 × $t_{CYSDCLK}$ + 2	ns

(a) in case of burst transfers

(b) in case of subsequent non-burst single word transfers (only possible for 32bit bus width)

(c) To extend this short timing, it is recommended to insert a read access to the RMMDR register after a bus write access, which is directly followed by a bus read access cycle.

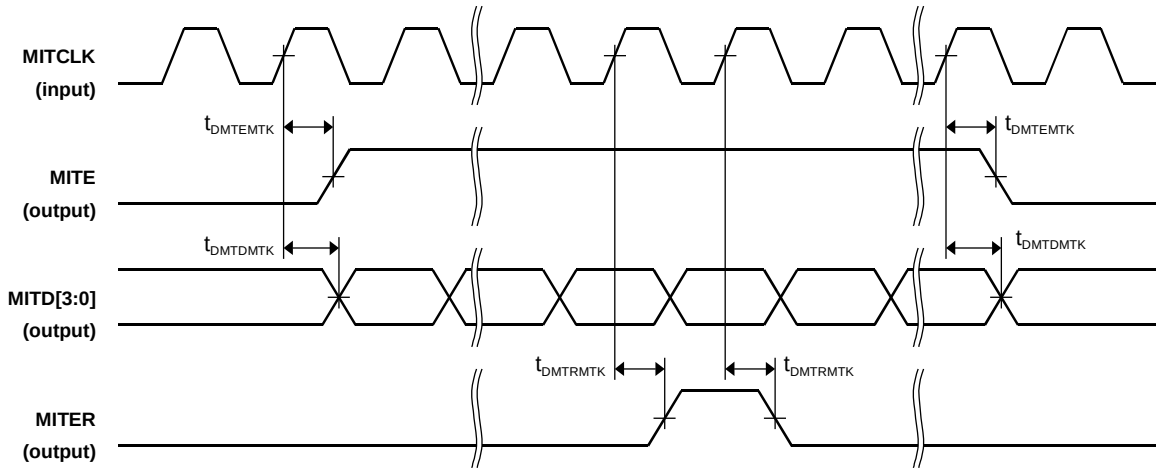
NOTE: i=0,1,2

NOTE: FAT is programmed in register RMATR according the following table

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

(9) Ethernet Interface Parameter

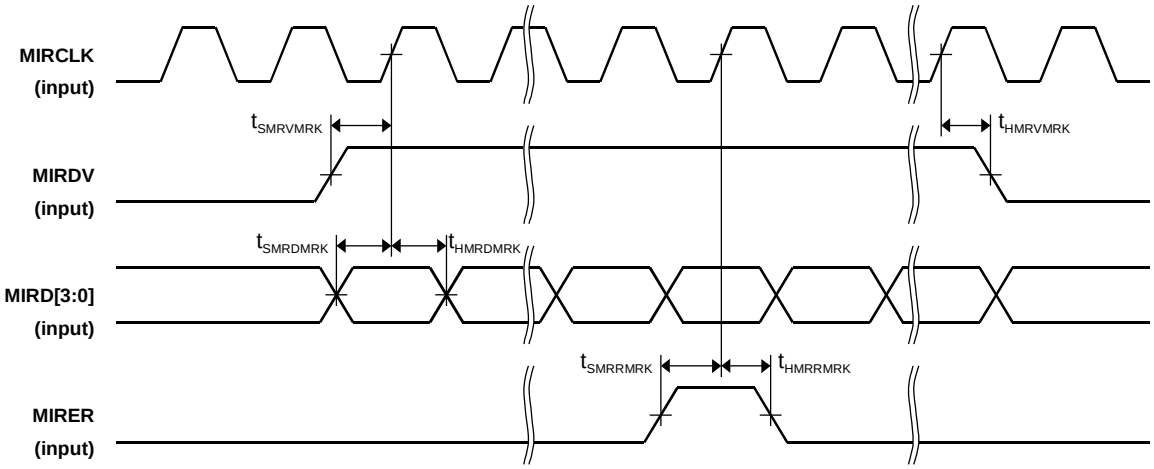
<MII Data Transmission>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MITE Output Delay	$t_{DMTEMTK}$	Load 50 pF	0	20 Note	ns
MITD[3:0] Output Delay	$t_{DMTDMTK}$	Load 50 pF	0	20 Note	ns
MITER Output Delay	$t_{DMTRMTK}$	Load 50 pF	0	20 Note	ns

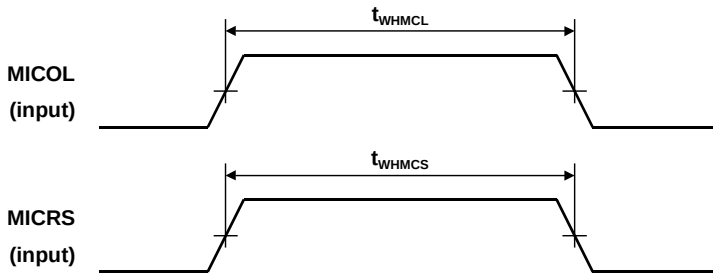
Note In MII Spec., Maximum output delay is specified as 25 ns

<MII Data Reception>



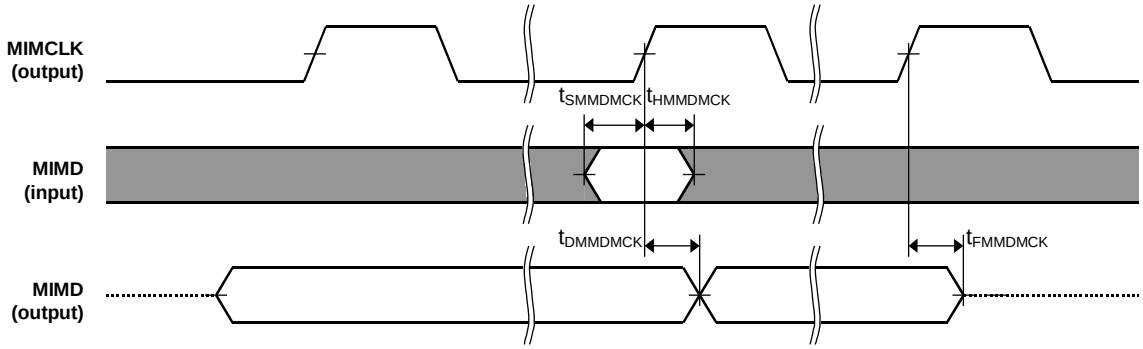
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MIRDV Setup Time	$t_{SMRVMRK}$		10		ns
MIRDV Hold Time	$t_{HMRVMRK}$		10		ns
MIRD[3:0] Setup Time	$t_{SMRDMRK}$		10		ns
MIRD[3:0] Hold Time	$t_{HMRDMRK}$		10		ns
MIRER Setup Time	$t_{SMRRMRK}$		10		ns
MIRER Hold Time	$t_{HMRRMRK}$		10		ns

<MII Interface Signals>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MICOL High Pulse Width	t_{WHMCL}		$2 \times t_{CYMTK}$		ns
MICRS High Pulse Width	t_{WHMCS}		$2 \times t_{CYMTK}$		ns

<MII Management Interface>

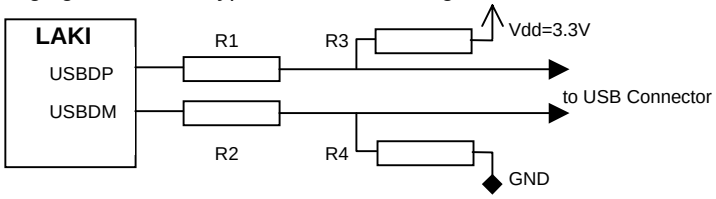


Parameter	Symbol	Condition	MIN.	MAX.	Unit
MIMD Setup to MIMCLK	$t_{SMMDMCK}$		30		ns
MIMD Hold from MIMCLK	$t_{HMMDMCK}$		0		ns
MIMD Output Delay from MIMCLK	$t_{DMMDMCK}$	Load 50 pF	10	20	ns
MIMD Floating Delay from MIMCLK	$t_{FMMDMCK}$	Load 50 pF	10	20	ns

(10) USB Interface Parameter

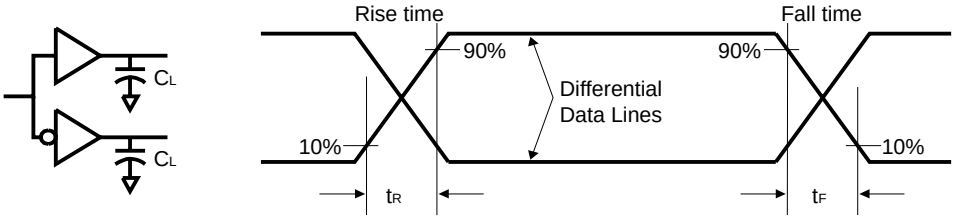
External Circuitry

The USB line output signals (refer to chapter 1.8) need 4 external resistors to adjust the output impedance (R1 and R2; 22 Ohm each), to code the full speed USB mode (R3 = 1.5 kOhm) and to protect the output driver of the USBDM pin (R4=51kOhm). The following figure shows a typical connection diagram.

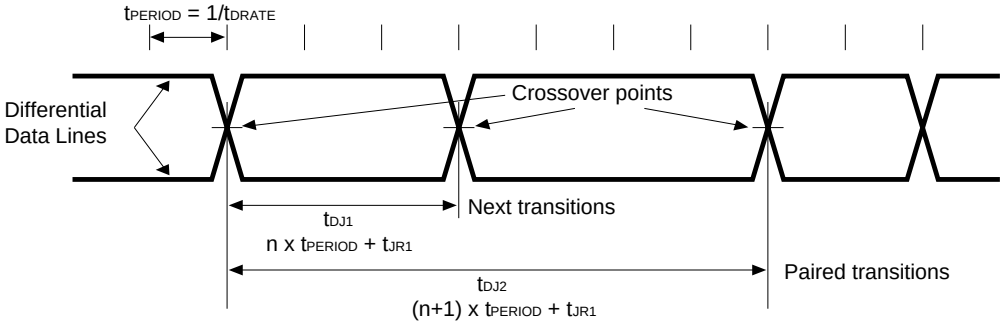


Parameter: USBDM, USBDP

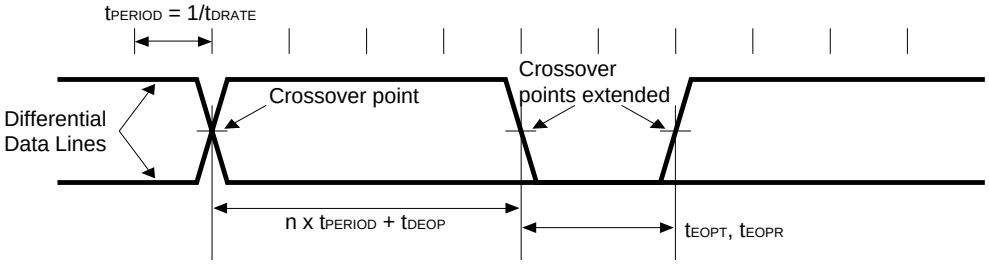
<Data Signal Rise and Fall>



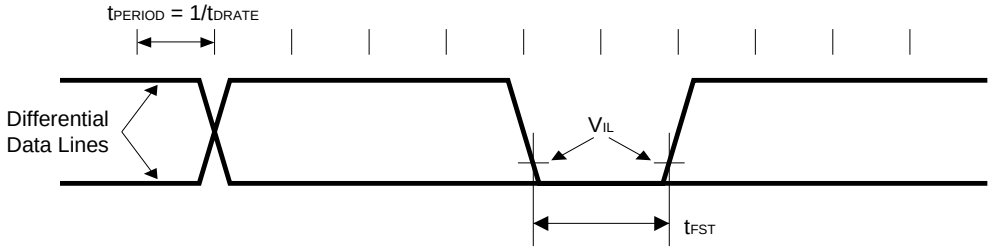
<Differential Data Jitter>



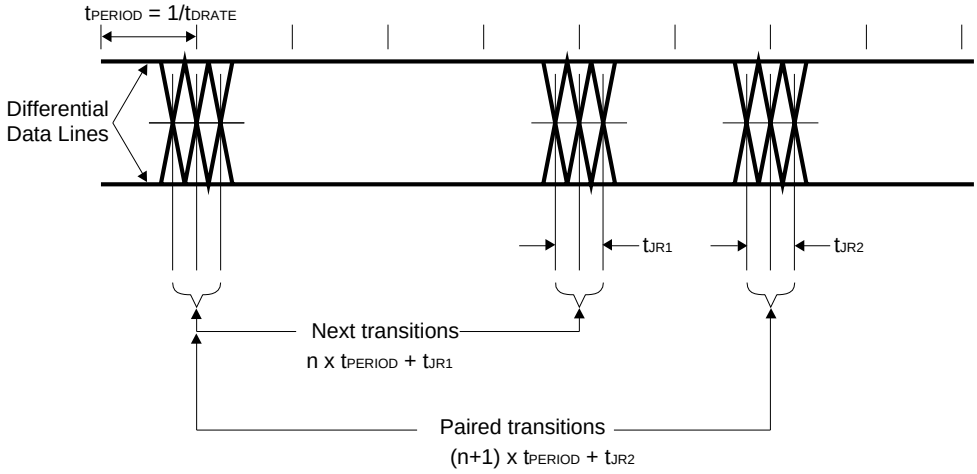
<Differential-to-EOP Transition Skew and EOP Width>



<Differential Transition Interval Width>

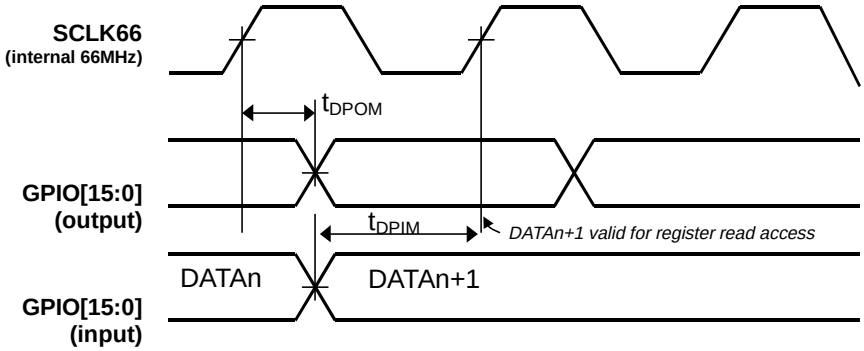


<Receiver Jitter Tolerance>



Parameter	Symbol	Condition	MIN.	MAX.	Unit
Rise Time	t_R		4	20	ns
Fall Time	t_F		4	20	ns
Differential Rise and Fall Time Matching	t_{FRFM}	t_R/t_F	90	111.11	%
Full-speed Data Rate	t_{DRATE}		11.9700	12.0300	Mbps
Source Jitter Total (including frequency tolerance):					ns
To Next Transition	t_{DJ1}		–3.5	+3.5	
For Paired Transitions	t_{DJ2}		–4	+4	
Source Jitter for Differential Transition to SE0 Transition	t_{DEOP}		–2	+5	ns
Receiver Jitter:					ns
To Next Transition	t_{JR1}		–18.5	+18.5	
For Paired Transitions	t_{JR2}		–9	+9	
Source SE0 interval of EOP	t_{EOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{EOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

(11) Parallel Port Interface Parameter

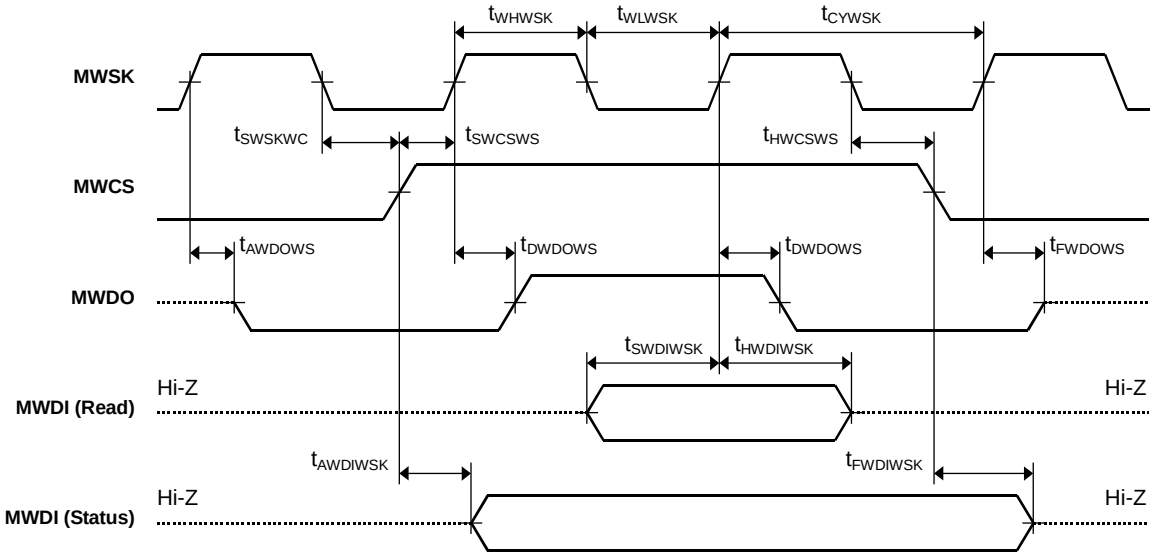


Parameter	Symbol	Conditions	MIN.	MAX.	Unit
GPIO[15:0] Output Delay	None				
GPIO[15:0] Input Delay	None				

(12) UART Interface Parameter

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
URCLK	None				
URSDI	None				
URDCD_B	None				
URDSR_B	None				
URCTS_B	None				
URSDO	None				
URDTR_B	None				
URRTS_B	None				

(13) Micro Wire Interface Parameter



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MWSK Clock Frequency	t_{CYWSK}	Load 50 pF	400 × t_{CYSK0}		ns
MWSK High Time	t_{WHWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK Low Time	t_{WLWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK Setup to MWSK	$t_{SWSKWCS}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS Setup to MWSK	$t_{SWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS Hold from MWSK	$t_{HWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWDO Output Active to Floating Delay from MWSK	$t_{AWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO Output Delay from MWSK	$t_{DWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO Output Floating to Active Delay from MWSK	$t_{FWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDI Setup to MWSK	$t_{SWDIWSK}$		10 × t_{CYSK0}		ns
MWDI Hold from MWSK	$t_{HWDIWSK}$		10 × t_{CYSK0}		ns
MWCS to Status Time from MWSK	$t_{AWDIWSK}$			100 × t_{CYSK0}	ns
MWCS to MWDO in 3-State	$t_{FWDIWSK}$			40 × t_{CYSK0}	ns

(14) PLL

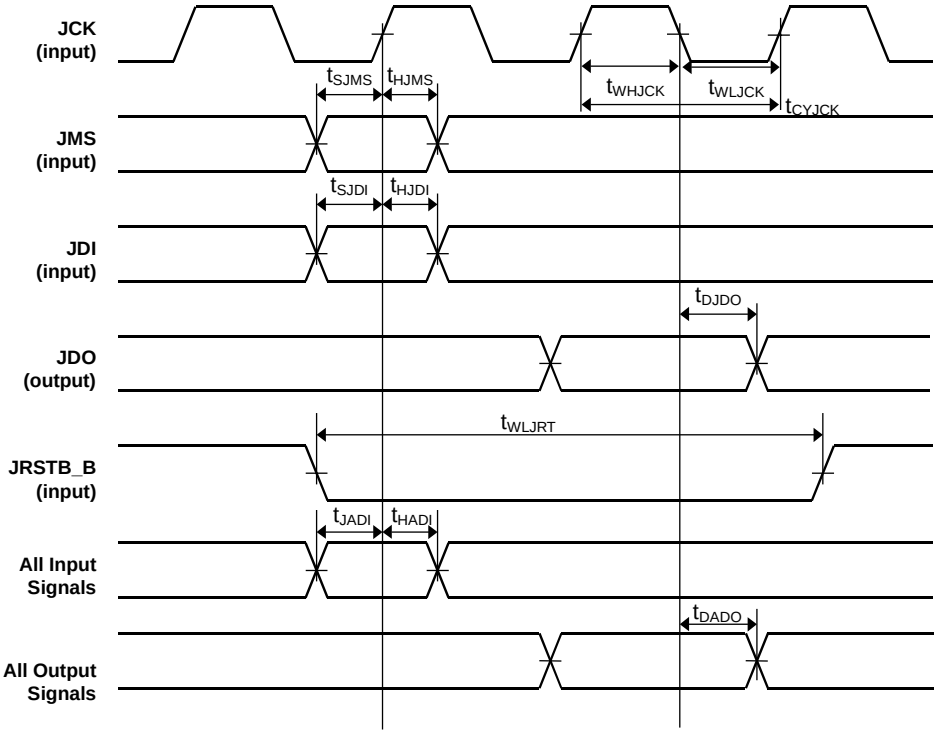
(14)-1 Analog PLL2 for System Clock Multiplying

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
PSTBY	T.B.D.				
PSMD	T.B.D.				

(14)-2 Analog PLL2 for USB Clock Multiplying

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
PUSTBY	T.B.D.				
PUMD	T.B.D.				

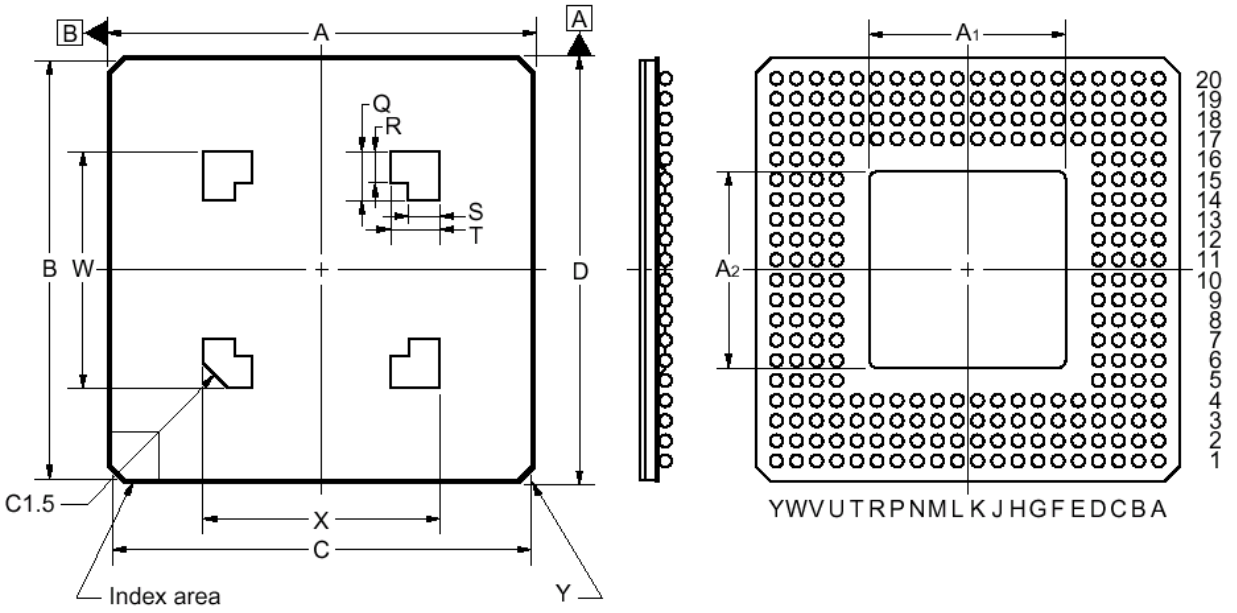
(15) JTAG Boundary-Scan

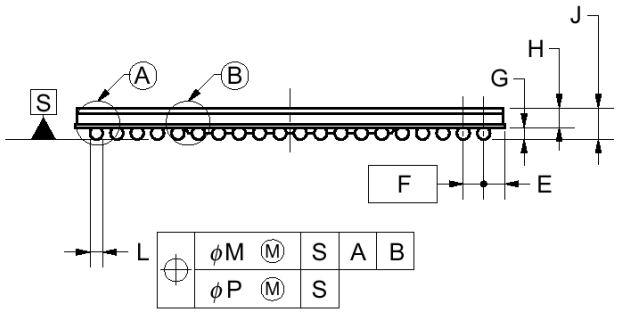


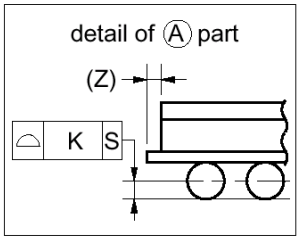
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
JCK Input Cycle	t_{CYJCK}		100	1000	ns
JCK Input High Width	t_{WHJCK}		0.4 x t_{CYJCK}	0.6 x t_{CYJCK}	ns
JCK Input Low Width	t_{WLJCK}		0.4 x t_{CYJCK}	0.6 x t_{CYJCK}	ns
JMS Setup Time	t_{SJMS}		10		ns
JMS Hold Time	t_{HJMS}		10.		ns
JDI Setup Time	t_{SJDI}		10		ns
JDI Hold Time	t_{HJDI}		10		ns
JDO Output Delay	t_{DJDO}	Load 50 pF		20	ns
JRSTB_B Low Pulse Width	t_{WLJRT}		5 × t_{CYJCK}		ns
All Input signal Setup Time	t_{SADI}		10		ns
All Input signal Hold Time	t_{HADI}		15		ns
All Output signal Output Delay	t_{DADO}	Load 50 pF		20	ns

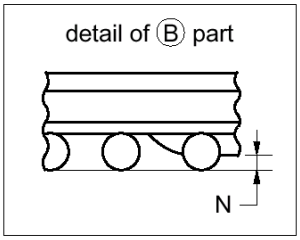
3. PACKAGE DRAWING

- **256-pin Tape-BGA (Heat Spreader Type) (27x27)**









ITEM	MILLIMETERS
A	27.00±0.20
A_1	15.50 MAX.
A_2	15.50 MAX.
B	26.60±0.15
C	26.60±0.15
D	27.00±0.20
E	1.435
F	1.27 (T.P.)
G	0.60±0.10
H	0.80
J	$1.40^{+0.30}_{-0.20}$
K	0.15
L	φ0.75±0.15
M	0.30
N	0.25MIN.
P	0.10
Q	3.0
R	2.0
S	2.0
T	3.0
W	15.11
X	15.11
Y	C 0.4
Z	0.20

P256N7-127-B6

4. RECOMMENDED SOLDERING CONDITIONS

LAKI should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-3
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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