PL 3120®/PL 3150®/PL 3170

Power Line Smart Transceiver Data Book

005-0193-01C

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Chapter 1

Introduction

Overview

This data book provides detailed technical specifications on the electrical interfaces, mechanical interfaces, and operating environment characteristics for the PL 3120®, PL 3150® and PL 3170 Power Line Smart Transceivers. This data book also provides guidelines for migrating applications to the PL Smart Transceiver using the NodeBuilder® Development Tool, the Mini EVK Evaluation Kit, or the ShortStack® Developer's Kit.

In some cases, vendor sources are included in this data book to simplify the task of integrating the PL Smart Transceivers with application electronics. A list of related documentation is provided in section 1.5, Related Documentation, at the end of this chapter. The documents listed in this section can be found on the Echelon Web site at www.echelon.com unless otherwise noted.

Product Overview

The PL Smart Transceivers provide a simple, cost-effective method of adding LONWORKS® power line signaling and networking to everyday devices. Compliant with the open ANSI/EIA standards, the smart transceivers are ideal for networked appliance, audio/video, lighting, heating/cooling, security, metering, and irrigation applications.

Representing a breakthrough in price, performance and packaging size, the PL Smart Transceivers integrate a Neuron® processor core with a power line transceiver that is fully compatible with the LONMARK® PL-20 channel type. Essentially a system-on-a-chip, the smart transceivers feature a highly reliable ANSI/EIA-709.2 compliant, narrow-band power line transceiver, an ANSI/EIA-709.1 compliant Neuron processor core for running applications and managing network communications, a choice of on-board or external memory, and an extremely small form factor. A wide variety of pre-designed, low-cost coupling circuit designs enable the PL Smart Transceivers to communicate over virtually any AC or DC power mains, as well as over an unpowered twisted pair.

LONWORKS Networks

In almost every industry today, there is a trend away from proprietary control schemes and centralized systems. The migration towards open, distributed, peer-to-peer LONWORKS networks is being driven by the interoperability, robust technology, faster development time, and scale economies afforded by LONWORKS based solutions. All of the everyday devices in a LONWORKS network communicate using the ANSI/EIA-709.1 protocol standard. This seven-layer OSI protocol provides a set of services that allow the application program in a device to send and receive messages from other devices in the network without needing to know the topology of the network or the functions of the other devices.

LONWORKS networks provide a complete suite of messaging services, including end-to-end acknowledgement, authentication, and priority message delivery. Network management services allow network tools to interact with devices over the network, including local or remote reconfiguration of network addresses and parameters, downloading of application programs, reporting of network problems, and start/stop/reset of device application programs.

Neuron Chips, a family of microprocessors originally designed by Echelon and licensed to third party semiconductor manufacturers, combine an ANSI/EIA-709.1 compliant processor core for running applications and managing the network communications, with a media-independent communication port, memory, I/O, and a 48-bit identification number (Neuron ID) that is unique to every device. The communication port permits short distance Neuron Chip-to-Neuron Chip communications, and can also be used with external line drivers and transceivers of almost any type.

The Neuron 3120 Chip family includes self-contained application program memory (no external memory bus) and the real-time operating system (RTOS) and application libraries pre-programmed in ROM. The Neuron 3150 Chip family includes both internal memory and an external memory bus.

The PL Smart Transceivers integrate a Neuron processor core with an ANSI/EIA-709.2 compliant power line transceiver within a single IC, eliminating the need for an external transceiver. Three variants of PL Smart Transceivers are available:

- The **PL 3120** chip includes self-contained application program memory, RTOS, and application library pre-programmed in ROM.
- The **PL 3150** chip includes both internal memory and an external memory bus.
- The **PL 3170** chip includes self-contained application program memory, Interoperable Self Installation (ISI) protocol, RTOS, and application library pre-programmed in ROM. With the ISI protocol, LONWORKS devices can interoperate automatically or at the push of a button, without requiring the use of an installation tool.

Three Product Families

The following table describes the three PL Smart Transceivers.

Product Name	Model Number	Maximum Input Clock	EEPROM	RAM	ROM	External Memory Interface	IC Package
PL 3120- E4T10	15311R-1000	10 MHz	4 Kbytes	2 Kbytes	24 Kbytes	No	38 TSSOP
PL 3170- E4T10	15331R-1000	10 MHz	4 Kbytes	2 Kbytes	24 Kbytes	No	38 TSSOP
PL 3150-L10	15321R-960	10 MHz	0.5 Kbytes	2 Kbytes	N/A	Yes	64 LQFP

The PL 3120 Smart Transceivers are targeted at small form factor designs that require up to 4KB of application code. The PL 3120 operates at either 6.5536MHz (A-band) or 10.0MHz (C-band), and includes 4KB of EEPROM and 2KB of RAM. Neuron system firmware (RTOS) along with application libraries is contained in on-chip ROM. The PL 3170 Smart Transceiver is targeted for the home control and automation market. The PL 3170 operates at 10.0MHz (C-band) only because this is the only band available for this market.

For applications that require more memory, the PL 3150 Smart Transceivers operate at either 6.5536MHz (A-band) or 10.0MHz (C-band), provide 0.5KB of EEPROM and 2KB of RAM, and use a 64 LQFP package. Through an external memory bus, the PL 3150 Smart Transceiver can address up to 58KB of external memory, of which 16KB is dedicated to Neuron system firmware.

The embedded EEPROM in both the PL Smart Transceivers can be written up to 10,000 times with no data loss. Data stored in the EEPROM will be retained for at least 10 years.

All three PL Smart Transceivers have 12 I/O pins which can be configured to operate in one or more of 38 predefined standard input/output modes. Combining a wide range of I/O models with two on-board timer/counters and hardware SCI/SPI UART enables the PL Smart Transceivers to interface to application circuits with minimal external logic or software development.

Power Line Signaling

The underlying signaling technology used in the PL Smart Transceivers was developed and optimized through more than ten years of field-testing. Over 30 million of the Echelon narrow-band transceivers have been deployed in a wide range of consumer, utility, building, industrial, and transportation applications worldwide. Features such as narrow-band BPSK signaling, dual-carrier frequency operation, adaptive carrier and data correlation, impulse noise cancellation, tone rejection and low-overhead error correction provide superior reliability in the face of interfering noise sources.

Dual-Carrier Frequency Operation

The PL Smart Transceivers utilize a dual-carrier frequency signaling technology to provide superior communication reliability in the face of interfering noise sources. In the case of acknowledged messaging, packets are initially transmitted on the primary frequency and if an acknowledgement is not received the packet is retransmitted on the secondary frequency. In the case of repeated messaging, packets are alternately transmitted on the primary and secondary frequencies. In utility applications the primary and secondary communication frequencies lie within the A-band shown in Figure 1.1. In non-utility applications, the primary communication frequency lies in the C-band shown in Figure 1.1 while the secondary frequency actually lies in what is called the B-band in CENELEC nomenclature. Figure 1.2 illustrates how the primary and secondary communications fit into the various frequency bands.

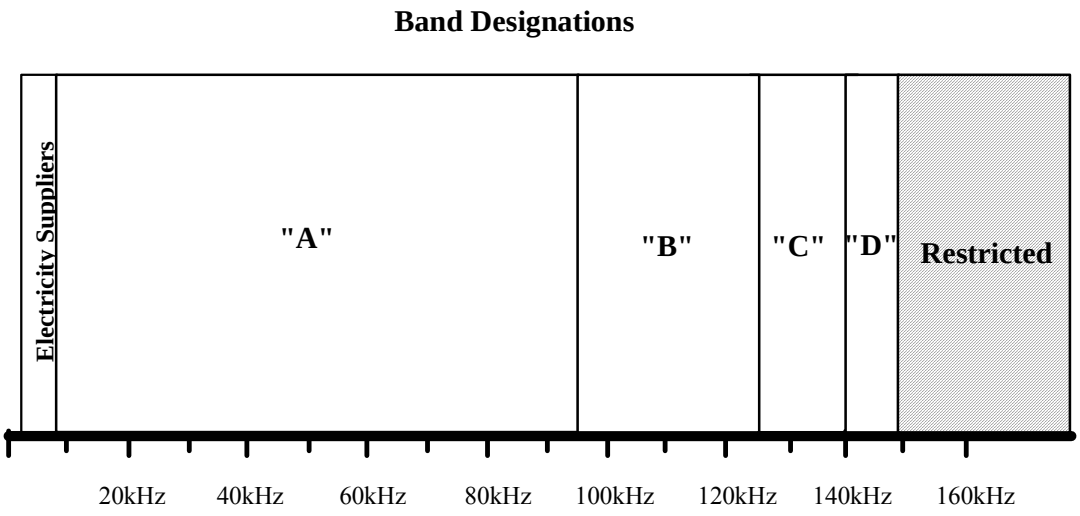


Figure 1.1 CENELEC Frequency Band Designations

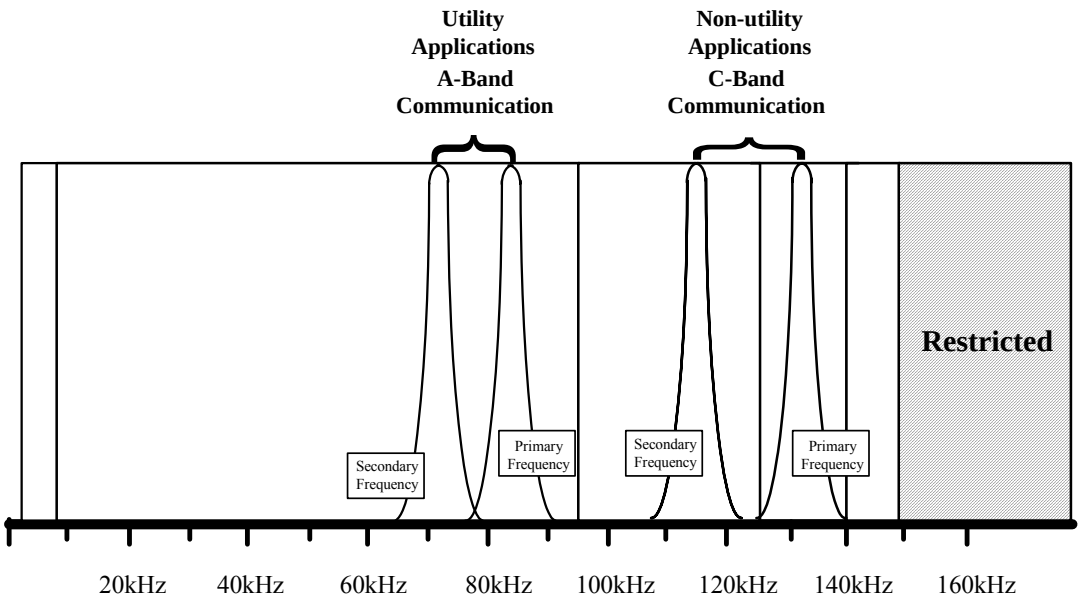


Figure 1.2 Dual-Carrier Frequency Operation

Forward Error Correction

Many noise sources interfere with power line signaling by corrupting data packets. The PL Smart Transceivers use a highly efficient, low-overhead forward error correction (FEC) algorithm in addition to a cyclical redundancy check (CRC) to overcome packet errors.

Powerful Output Amplifier

The external, high performance amplifier design developed for use with the PL Smart Transceivers provides a 1 ohm output impedance and 1Ap-p current capability to drive high output levels into low impedance circuits, while maintaining the extremely low signal distortion levels necessary to meet stringent international EMC regulations. For applications requiring even more output power an optional higher power design is available that provides up to 2Ap-p of output current.

Wide Dynamic Range

Dynamic range relates to the sensitivity of the receiver. The PL Smart Transceivers have a dynamic range of > 80dB. On a quiet line the Power Line Smart Transceivers can receive signals that have been attenuated by a factor of more than 10,000.

Low Current Consumption

The PL Smart Transceivers and their associated power amplifier circuitry are powered by user-supplied +8.5 to +18VDC (V_A) and +5VDC (V_{DD5}) power supplies. Built-in power management features, combined with a wide supply range, are key benefits when designing inexpensive power supplies. Power management is especially useful for high volume, low cost consumer products such as electrical switches, outlets, and incandescent light dimmers.

Very low receive mode current consumption of just 350µA typical from the V_A supply and 9mA typical from the V_{DD5} supply reduces power supply size and cost.

The PL Smart Transceivers communicate at a raw bit rate of 5.4kbps (C-band) or 3.6kbps (A-band), corresponding to the following maximum packet rates.

Band	**Packets Per Second**	**Collisions**	**Minimum Input Clock**	**Priority Slots**	**Oscillator Accuracy**	**Average Packet Size**	**Minimum Backlog**
C-band	15	None	10MHz	4	200 PPM	15 bytes	1
A-band	10	None	6.5536MHz	4	200 PPM	15 bytes	1

This high throughput makes the transceivers well suited for residential, commercial, and industrial automation applications.

Compliant with Regulations Worldwide

The PL Smart Transceivers are designed to comply with FCC [1], Industry Canada, Japan MPT, China, and European CENELEC EN50065-1 regulations [2], allowing them to be used in applications worldwide. The CENELEC communications protocol is fully implemented by the PL Smart Transceivers, eliminating the need for users to develop the complex timing and access algorithms mandated under CENELEC EN50065-1. Additionally, the PL 3120 and 3150 Smart Transceivers can operate in either the CENELEC utility (A-band) or consumer (C-band) bands.

Figure 1.1 shows the CENELEC frequency restrictions that are mandatory in EU countries and are observed in many non-EU countries as well. FCC, Industry Canada and the Japan MPT regulations are less strict than the CENELEC requirements. The frequency allocations for these countries are summarized in Figure 1.3.

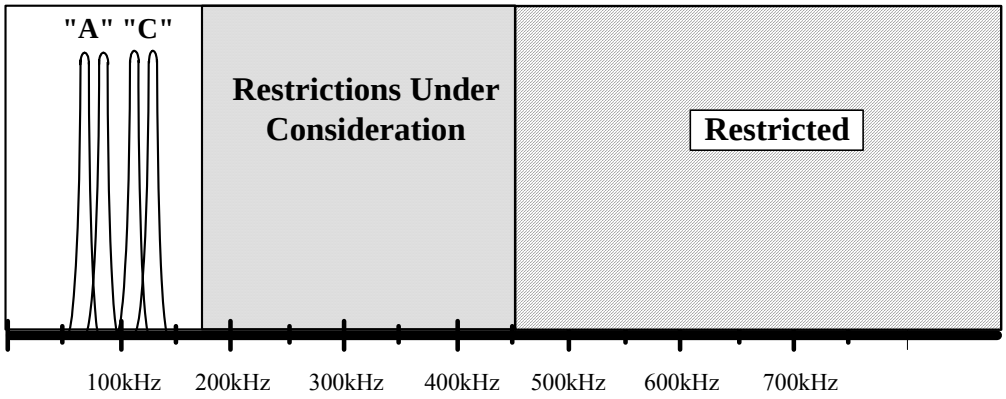


Figure 1.3 FCC, Industry Canada, Japan MPT Power-line Signaling

Integrated, Low-Cost and Small Form Factor Design

A small number of inexpensive external components are required to create a complete PL Smart Transceiver-based device. Figure 1.4 illustrates the block diagram of a PL Smart Transceiver based device. Acomprehensive Development Support Kit (DSK) is available from Echelon that includes sample PL Smart Transceivers, schematics, printed circuit board (PCB) layouts, bills of materials, and technology evaluation hardware with sample application code that customers can use to implement this interface circuitry.

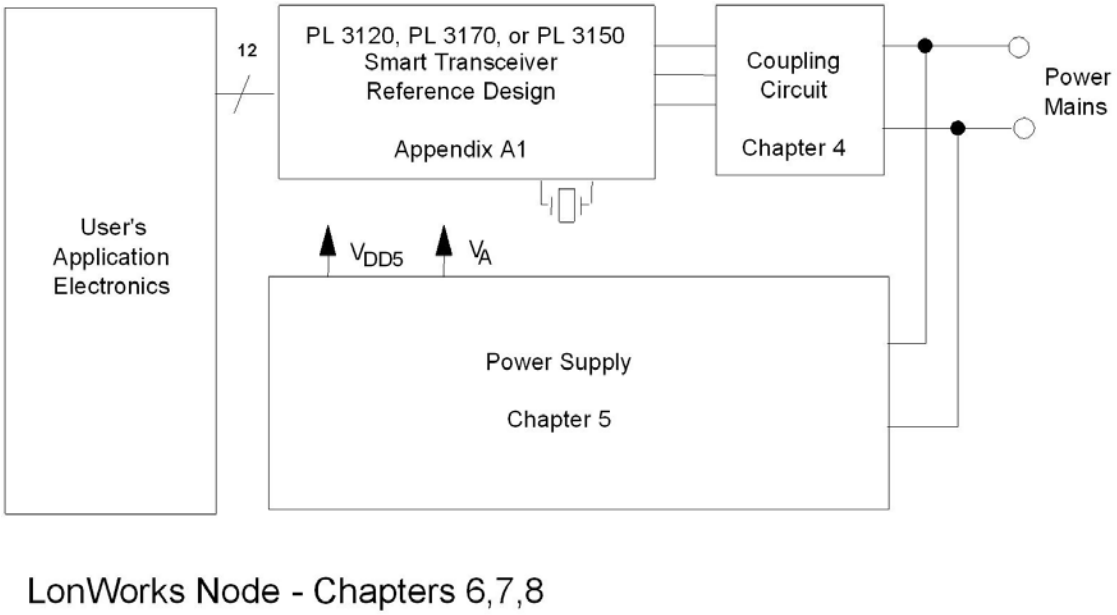


Figure 1.4 LONWORKS Device Block Diagram

Electric Utility vs. Home/Commercial/Industrial Applications

The PL 3120 and PL 3150 Smart Transceivers are designed to operate in one of two frequency ranges depending on the end application. However, the PL 3170 Smart Transceiver is designed to operate in one frequency range for the home control and automation market. When configured for use in electric utility applications, the Smart Transceivers communicate in the A-band frequency range. In home/commercial/industrial applications, they communicate in the C-band frequency range. The use of separate operating frequency bands for utility and non-utility applications originated in Europe and has because become a de facto standard because of the numerous benefits it provides in terms of bandwidth management, security, and privacy.

Extensive Development Resources

A wide assortment of technical documentation, diagnostic tools, support programs, and training courses are available to assist customers with their projects. Additionally, Echelon offers fee-based pre-production design reviews of customer's products, schematics, PCB layouts, and bills of material to verify that they comply with published guidelines. Communication performance-verification testing is provided to customers who submit working devices.

Audience

The *PL 3120/PL 3150/ PL 3170 Power Line Smart Transceiver Data Book* provides specifications and user instructions for PL Smart Transceiver customers.

Content

This data book describes the use of the PL Smart Transceivers in both utility (A-band) and home/commercial/industrial (C-band) applications.

Related Documentation

The following documents are suggested reading and are available at Echelon's Web site:

PL 3120/ PL 3150 Power Line Smart Transceiver Data Sheet (003-0378-01)

PL 3170 Power Line Smart Transceiver Data Sheet (003-0431-01)

Neuron C Programmer's Guide (078-0002-02)

Neuron C Reference Guide (078-0140-02)

Neuron 3150 Chip External Memory Interface Engineering Bulletin (005-0013-01)

ShortStack User's Guide (078-0189-01)

ShortStack 2 Nios II Example Port User's Guide (078-0354-01)

LONWORKS Microprocessor Interface Program User's Guide (078-0017-01)

NodeBuilder User's Guide (078-0141-01)

Mini EVK User's Guide (078-0302-01)

Parallel I/O Interface to the Neuron Chip Engineering Bulletin (005-0021-01)

PLCA-22 Power Line Communication Analyzer User's Guide (078-0147-01)

LONWORKS PCLTA-20 PCI Interface User's Guide (078-0179-01)

LONWORKS USB Network Interface User's Guide (078-0296-01)

Neuron Chip Quadrature Input Function Interface Engineering Bulletin (005-0003-01)

Chapter 2

Hardware Resources

Overview

The PL 3120 Smart Transceiver is a complete SoC (system-on-a-chip) for designs that require up to 4KB of memory. The PL 3170 Smart Transceiver includes self-contained application program memory, Interoperable Self-Installation (ISI) library and engine, RTOS, and an application library pre-programmed in ROM. The PL 3150 Smart Transceiver supports external memory for more complex applications. The major hardware blocks of the processors are the same, except where noted; see Table 2.1 and Figure 2.1.

Table 2.1 Comparison of PL Smart Transceivers

Characteristic	PL 3150 Smart Transceiver	PL 3120 Smart Transceiver	PL 3170 Smart Transceiver
RAM Bytes	2,048	2,048	2,048
ROM Bytes	—	24,576	24,576
ROM Version	N/A	V 14	V 17
EEPROM Bytes	512	4,096	4,096
General purpose I/O pins	12	12	12
16-Bit Timer/Counters	2	2	2
External Memory Interface	Yes	No	No
Package	64 pin LQFP	38 pin TSSOP	38 pin TSSOP

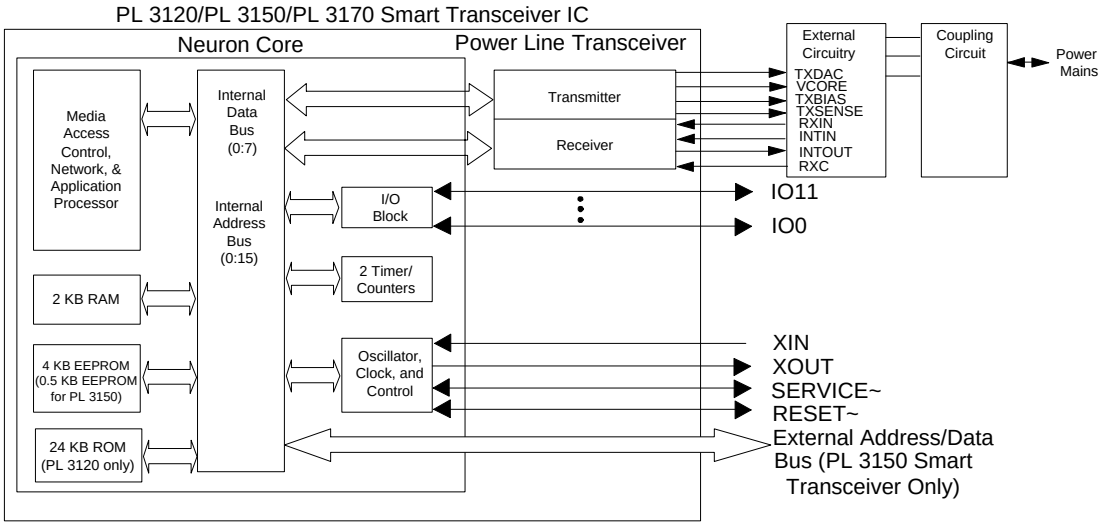


Figure 2.1 PL Smart Transceiver Block Diagram

Neuron Processor Architecture

The Neuron core is composed of three processors. These processors are assigned to the following functions by the Neuron firmware.

Processor 1 is the MAC layer processor that handles layers 1 and 2 of the 7-layer LonTalk® protocol stack. This includes driving the communications subsystem hardware and executing the media access control algorithm. Processor 1 communicates with Processor 2 using network buffers located in shared RAM memory.

Processor 2 is the network processor that implements layers 3 through 6 of the LonTalk protocol stack. It handles network variable processing, addressing, transaction processing, authentication, background diagnostics, software timers, network management, and routing functions. Processor 2 uses network buffers in shared memory to communicate with Processor 1, and application buffers to communicate with Processor 3. These buffers are also located in shared RAM memory. Access to them is mediated with hardware semaphores to resolve contention when updating shared data.

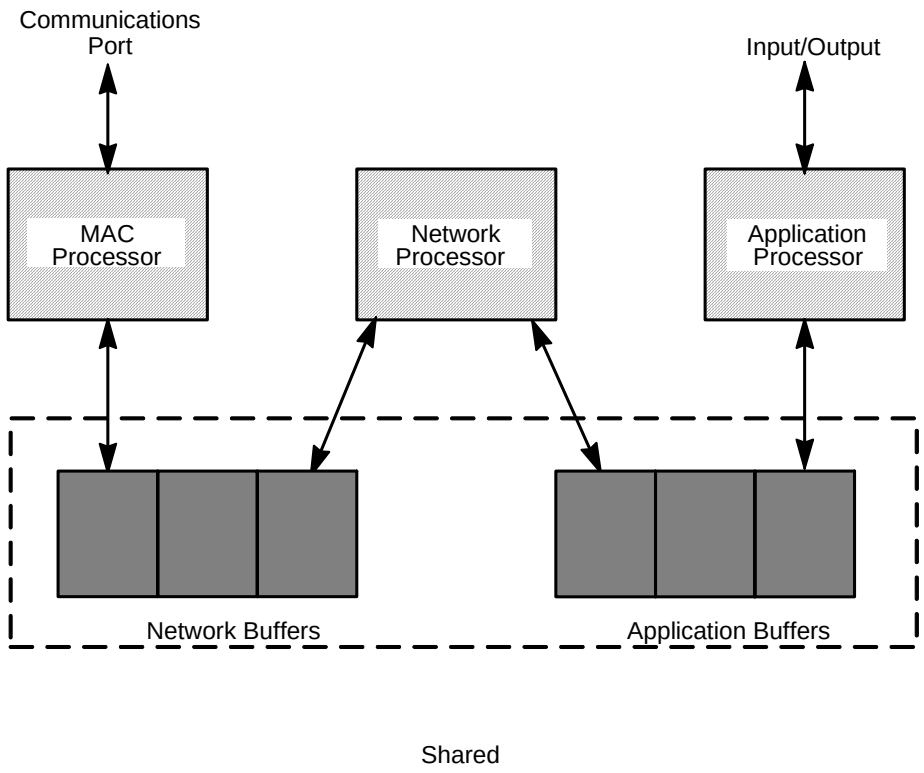


Figure 2.2 Processor Shared Memory Allocation

Processor 3 is the application processor. It executes the code written by the user, together with the operating system services called by user code. The primary programming language used by applications is Neuron C, a derivative of the ANSI C language optimized and enhanced for LONWORKS distributed control applications. The major enhancements are the following (see the *Neuron C Programmer's Guide* for details):

- A network communication model, based on *functional blocks* and *network variables*, that simplifies and promotes data sharing between like and disparate devices.
- A network configuration model, *based on functional blocks and configuration properties*, that facilitates interoperable network configuration tools.
- A type model based on standard and user *resource files* that expands the market for interoperable devices by simplifying the integration of devices from multiple manufacturers.
- An extensive set of I/O drivers that support the I/O capabilities of the Neuron core.
- Powerful event driven programming extensions that provide easy handling of network, I/O, and timer events.

The support for all these capabilities is part of the Neuron firmware, and does not need to be written by the programmer.

Each of the three identical processors has its own register set (Table 2.2), but all three processors share data, ALUs (arithmetic logic units) and memory access circuitry (Figure 2.3). On the PL 3150 Smart Transceiver, the internal address, data, and R/W~ signals are reflected on the corresponding external lines when utilized by any of the internal processors. Each CPU *minor* cycle consists of *three system clock* cycles, or phases; each system clock cycle is two input clock cycles. The minor cycles of the three processors are offset from one another by one system clock cycle, so that each processor can access memory and ALUs once during each instruction cycle. Figure 2.3 shows the active elements for each processor during one of the three phases of a minor cycle. Therefore, the system pipelines the three processors, reducing hardware requirements without affecting performance. This allows the execution of three processes in parallel without time-consuming interrupts and context switching.

Table 2.2 Register Set

Mnemonic	Bits	Contents
FLAGS	8	CPU Number, Fast I/O Select, and Carry Bit
IP	16	Next Instruction Pointer
BP	8	Address of 256-byte Base Page
DSP	8	Data Stack Pointer within Base Page
RSP	8	Return Stack Pointer within Base Page
TOS	8	Top of Data Stack, ALU Input

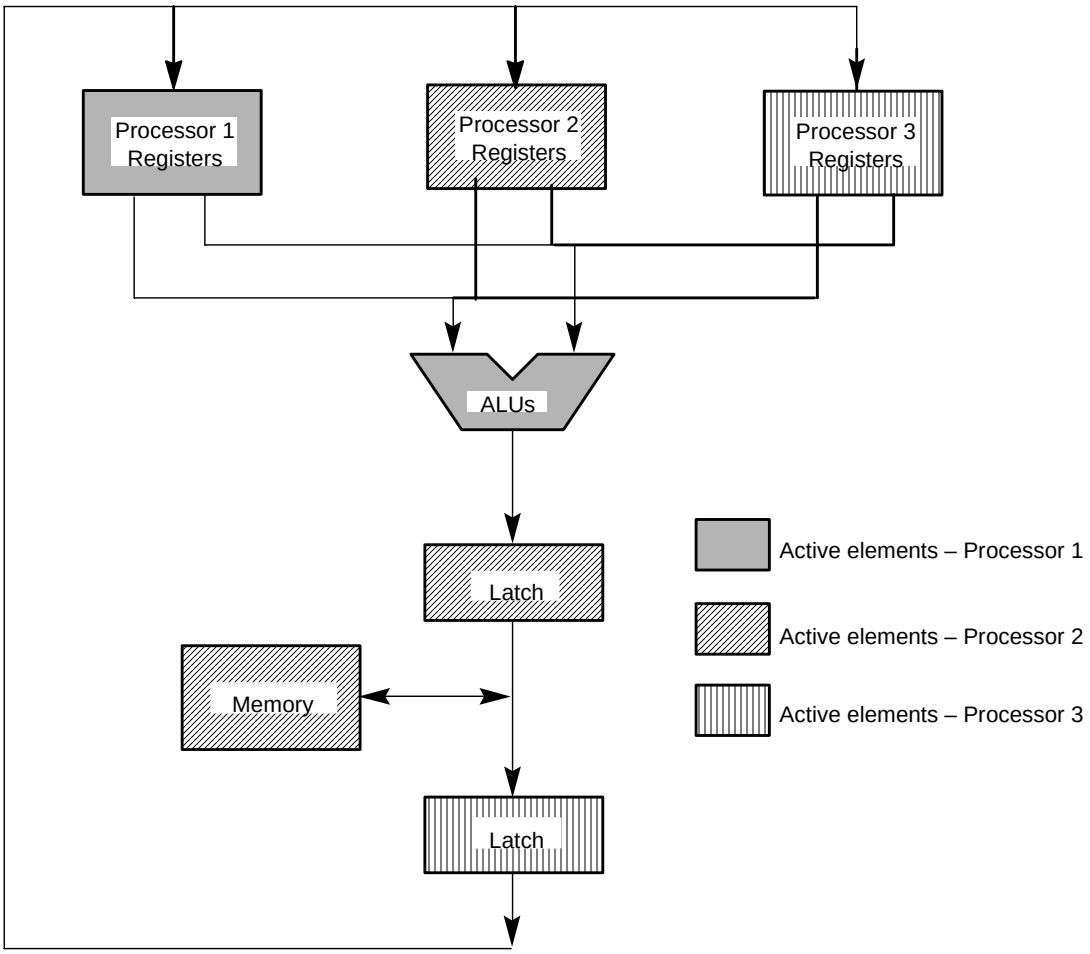


Figure 2.3 Processor/Memory Activity During One of the Three System Clock Cycles of a Minor Cycle

The architecture is stack-oriented; one 8-bit wide stack is used for data references, and the ALU operates on the TOS (Top of Stack) register and the next entry in the data stack which is in RAM. A second stack stores the return addresses for CALL instructions, and can also be used for temporary data storage. This stack architecture leads to very compact code. Tables 2.3, 2.4, and 2.5 outline the instruction set.

Figure 2.4 shows the layout of a base page, which can be up to 256 bytes long. Each of the three processors uses a different base page, whose address is given by the contents of the BP register of that processor. The top of the data stack is in the 8-bit TOS register, and the next element in the data stack is at the location within the base page at the offset given by the contents of the DSP register. The data stack grows from low memory towards high memory. The assembler shorthand symbol NEXT refers to the contents of the location (BP+DSP) in memory, which is not an actual processor register.

Pushing a byte of data onto the data stack involves the following steps: incrementing the DSP register, storing the current contents of TOS at the address (BP+DSP) in memory, and moving the byte of data to TOS.

Popping a byte of data from the data stack involves the following steps: moving TOS to the destination, moving the contents of the address (BP+DSP) in memory to TOS, and decrementing the DSP register.

The return stack grows from high memory towards low memory. Executing a subroutine call involves the following steps: storing the high byte of the instruction pointer register IP at the address (BP+RSP) in memory, decrementing RSP, storing the low byte of IP at the address (BP+RSP) in memory, decrementing RSP, and moving the destination address to the IP register.

Similarly, returning from a subroutine involves the following steps: incrementing RSP, moving the contents of (BP+RSP) to the low byte of the IP register, incrementing RSP, and moving the contents of (BP+RSP) to the high byte of IP.

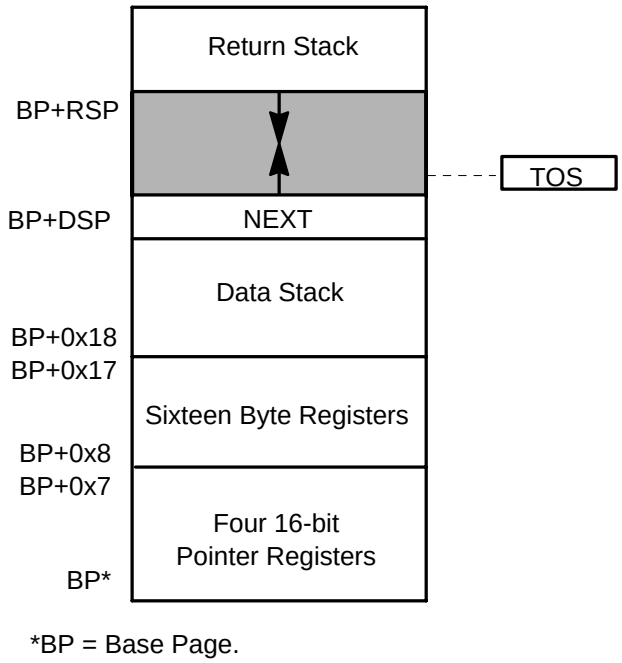


Figure 2.4 Base Page Memory Layout

A processor instruction cycle is three system clock cycles, or six input clock (XIN) cycles. Most instructions take between one and seven processor instruction cycles. At an input clock rate of 10MHz, instruction times vary between 0.6 µs and 4.2 µs. Execution time scales inversely with the input clock rate. The formula for instruction time is:

```
(Instruction Time) = (# Cycles) x 6 / (Input Clock)
```

Tables 2.3, 2.4, and 2.5 list the processor instructions, their timings (in cycles) and sizes (in bytes). This is provided for purposes of calculating the execution time and size of code sequences. All programming of the PL Smart Transceiver is typically done with Neuron C using the NodeBuilder development tool or the Mini EVK Evaluation Kit. The Neuron C compiler can optionally produce an assembly listing, and examining this listing can help the programmer to optimize the Neuron C source code.

Table 2.3 Program Control Instructions

Mnemonic	Cycles	Size (bytes)	Description	Comments
NOP	1	1	No operation	
SBR	1	1	Short unconditional branch	Offset 0 to 15
BR/BRC/BRNC	2	2	Branch, branch on (not) carry	Offset -128 to +127
SBRZ/SBRNZ	3	1	Short branch on TOS (not) zero	Offset 0 to 15. Drops TOS
BRF	4	3	Unconditional branch far	Absolute address
BRZ/BRNZ	4	2	Branch on TOS (not) zero	Offset -128 to +127. Drops TOS
RET	4	1	Return from subroutine	Drops two bytes from return stack
BRNEQ	4/6	3	Branch if TOS not equal (taken/not taken)	Offset -128 to +127. Drops TOS if equal
DBRNZ	5	2	Decrement [RSP] and branch if not zero	Offset -128 to +127. If not taken, drops one byte from return stack
CALLR	5	2	Call subroutine relative	Offset -128 to +127. Pushes two bytes to return stack
CALL	6	2	Call subroutine	Address in low 8KB. Pushes two bytes to return stack
CALLF	7	3	Call subroutine far	Absolute address. Pushes two bytes to return stack

Table 2.4 Memory/Stack Instructions

Mnemonic	Cycles	Size (bytes)	Comments / Effective Address (EA)
PUSH TOS	3	1	Increment DSP, duplicate TOS into NEXT
DROP TOS	3	1	Move NEXT to TOS, decrement DSP
DROP_R TOS	6	1	Move NEXT to TOS, decrement DSP, return from call
PUSH (NEXT, DSP, RSP, FLAGS)	4	1	Push processor register
POP (DSP, RSP, FLAGS)	4	1	Pop processor register
DROP NEXT	2	1	Decrement DSP
DROP_R NEXT	5	1	Decrement DSP and return from call

PUSH/POP !D	4	1	Byte register [8 to 23]
PUSH !TOS	4	1	EA = BP + TOS, push byte to NEXT
POP !TOS	4	1	EA = BP + TOS, pop byte from NEXT
PUSH [RSP]	4	1	Push from return stack to data stack, RSP unchanged
DROP [RSP]	2	1	Increment RSP
PUSHS #literal	4	1	Push short literal value [0 to 7]
PUSH #literal	4	2	Push 8-bit literal value [0 to 255]
PUSHPOP	5	1	Pop from return stack, push to data stack
POPPUSH	5	1	Pop from data stack, push to return stack
LDBP address	5	3	Load base page pointer with 16-bit value
PUSH/POP [DSP][-D]	5	1	EA = BP + DSP - displacement [1 to 8]
PUSHD #literal	6	3	16-bit literal value (high byte first)
PUSHD [PTR]	6	1	Push from 16-bit pointer [0 to 3], high byte first
POPD [PTR]	6	1	Pop to 16-bit pointer [0 to 3], low byte first
PUSH/POP [PTR][TOS]	6	1	EA = (16-bit pointer) + TOS
PUSH/POP [PTR][D]	7	2	EA = (16-bit pointer) + displacement [0 to 255]
PUSH/POP absolute	7	3	Absolute memory address
IN/OUT	7 + 4n	1	Fast I/O instruction, transfer *n* bytes

Table 2.5 ALU Instructions

Mnemonic	**Cycles**	**Size (bytes)**	**Operation**
INC/DEC/NOT	2	1	Increment/decrement/negate TOS
ROLC/RORC	2	1	Rotate left/right TOS through carry
SHL/SHR	2	1	Unsigned left/right shift TOS, clear carry
SHLA/SHRA	2	1	Signed left/right shift TOS into carry
ADD/AND/OR/XOR/ADC	4	1	Operate with NEXT on TOS, drop NEXT
ADD/AND/OR/XOR #literal	3	2	Operate with literal on TOS
(ADD/AND/OR/XOR)_R	7	1	Operate with NEXT on TOS, drop NEXT and return
ALLOC #literal	3	1	Add [1 to 8] to data stack pointer
DEALLOC_R #literal	6	1	Subtract [1 to 8] from data stack pointer and return
SUB NEXT,TOS	4	1	TOS = NEXT - TOS, drop NEXT
SBC NEXT, TOS	4	1	TOS = NEXT - TOS - carry, drop NEXT
SUB TOS,NEXT	4	1	TOS = TOS - NEXT, drop NEXT
XCH	4	1	Exchange TOS and NEXT
INC [PTR]	6	1	Increment 16-bit pointer [0 to 3]

Memory

Memory Allocation Overview

PL 3150 Smart Transceiver Memory Allocation

See Figure 2.5 for a memory map of the PL 3150 Smart Transceiver.

- 512 bytes of in-circuit programmable EEPROM that store the following:
  - — Network configuration and addressing information.
  - — Unique 48-bit Neuron ID — written at the factory.
  - — User-written application code and read-mostly data. See Table 2.6 for available EEPROM space.
- 2,048 bytes of static RAM that store the following:
  - — Stack segment, application, and system data.
  - — Network and application buffers.
- The processor can access 59,392 bytes of the available 65,536 bytes of memory address space via the external memory interface. The remaining 6,144 bytes of the memory address space are mapped internally.
- 16,384 bytes of the external memory (59,392 bytes total) are required to store the following:
  - — The Neuron firmware, including the system firmware executed by the MAC and Network processors, and the executive supporting the application program.
- The rest of the external memory (43,008 bytes) is available for:
  - — User-written application code.
  - — Additional application read/write and non-volatile data.
  - — Additional network buffers and application buffers.

PL 3120/PL 3170 Smart Transceiver Memory Allocation

See Figure 2.6 for a memory map of the PL 3120 and PL 3170 Smart Transceivers.

- 4,096 bytes of in-circuit programmable EEPROM that store:
  - — Network configuration and addressing information.
  - — Unique 48-bit Neuron ID — written at the factory.
  - — User-written application code and read-mostly data.
- 2,048 bytes of static RAM that store the following:
  - — Stack segment, application, and system data.
  - — Network buffers and application buffers.
- 24,576 bytes of ROM that store the following:
  - — The Neuron firmware, including the system firmware executed by the MAC and network processors, the executive supporting the application program, ISI library (PL 3170 only), and application libraries.

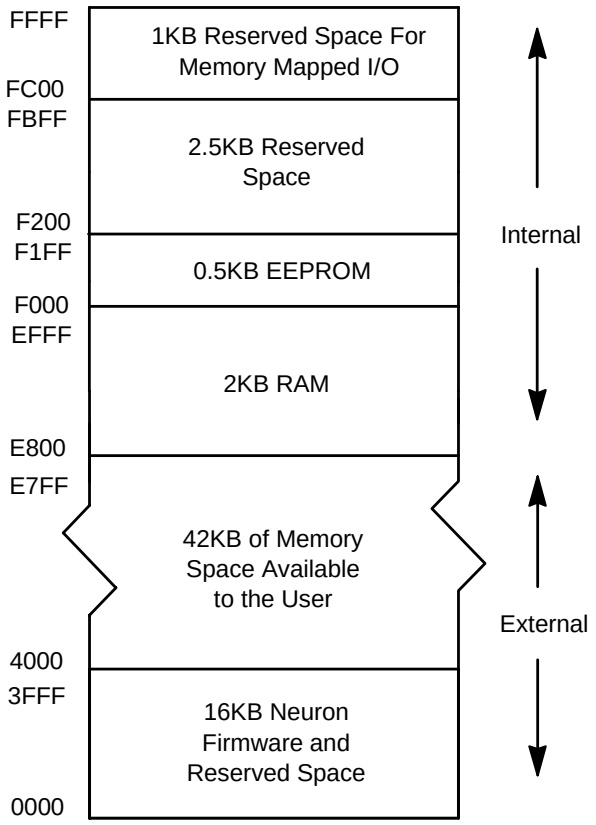


Figure 2.5 PL 3150 Smart Transceiver Memory Map

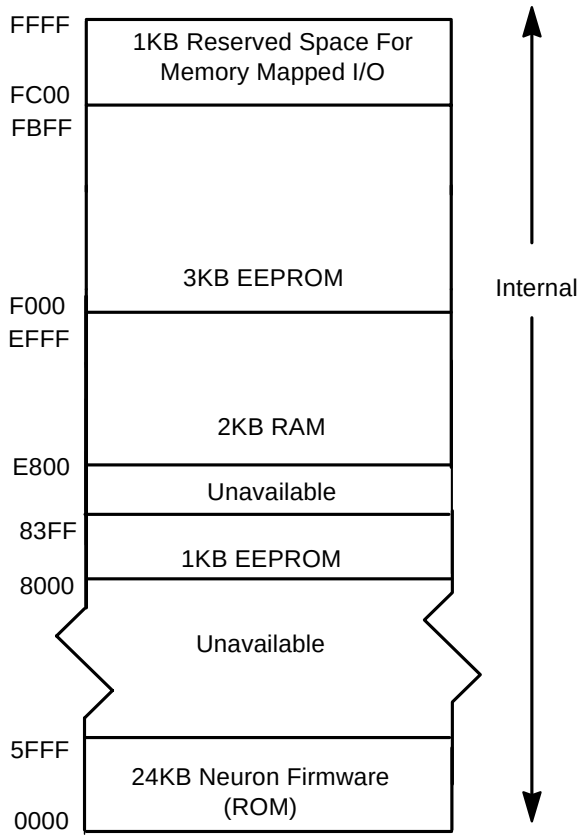


Figure 2.6 PL 3120/PL 3170 Smart Transceiver Memory Map

EEPROM

All three versions of the PL Smart Transceiver have internal EEPROM containing:

- Network configuration and addressing information.
- Unique 48-bit Neuron ID.
- Optional user-written application code and data tables.

All but 8 bytes of the EEPROM can be written under program control using an on-chip charge pump to generate the required programming voltage. The charge pump operation is transparent to the user. The remaining 8 bytes are written during manufacture, and contain a unique 48-bit identifier for each part called the *Neuron ID*, plus 16 bits for the chip manufacturer's device code. Each byte in the EEPROM region can be written up to 10,000 times. For all PL Smart Transceivers, the EEPROM stores the installation-specific information such as network addresses and communications parameters. For the PL 3120 and PL 3170 Smart Transceivers, the EEPROM also stores the application program generated by the NodeBuilder or Mini EVK tool. The application code for the PL 3150 Smart Transceiver can be stored either on-chip in the EEPROM memory or off-chip in external memory depending on the size of the application code. See Table 2.6 for available EEPROM space.

For all write operations to the internal EEPROM, the Neuron firmware automatically compares the value in the EEPROM location with the value to be written. If the two are the same, the write operation is not performed. This prevents unnecessary write cycles to the EEPROM, and reduces the average EEPROM write cycle latency.

When the PL Smart Transceiver is not within the specified power supply voltage range, a pending or on-going EEPROM write is not guaranteed. The PL Smart Transceiver contains a built-in low-voltage interruption (LVI) circuit that holds the chip in reset when V_{DD5} is below a certain voltage. See the *PL 3120/ PL 3150 or PL 3170 Smart Transceiver Datasheets* for LVI trip points. This reduces the risk of EEPROM data corruption. For PL 3150 Smart Transceiver devices with external flash memory an external pulse stretching LVI is required. See *RESET Pin* for more information on LVI circuitry.

In the event of a fault, the on-chip EEPROM of the PL 3150 Smart Transceiver can be reset to its factory default state by executing the EEBLANK program. To do so, program the appropriate EEBLANK file into an external memory device, temporarily replace the application's external ROM or flash with the chip that has EEBLANK loaded, and power up the device. The EEBLANK files are named eeb<n>.nri where <n> is the Neuron input clock rate in kHz and is one of the following: 20000, 10000, 05000, 02500, 01250, or 00625. If you are using an input clock between two of these speeds, select the next slower version of EEBLANK.

After around 20 seconds (or less depending on clock speed), the device's service LED should come on solid, indicating that the EEPROM has been blanked. Then replace the original application ROM or flash. The EEBLANK files are distributed with NodeBuilder 3.1 and Mini EVK Evaluation Kit software. Versions of EEBLANK distributed with prior releases of the LonBuilder® and NodeBuilder tools should not be used with the PL 3150 Smart Transceiver.

The `set_eeprom_lock()` function can also be used for additional protection against accidental EEPROM data corruption. This function allows the application program to set the state of the lock on the checksummed portion of the EEPROM. Refer to the *Neuron C Reference Guide* for more information.

The internal EEPROM of a PL Smart Transceiver will contain a fixed amount of overhead and a network image (configuration), in addition to user code and user data. The following table shows the maximum amount of EEPROM space available for user code and user data assuming a minimally-sized network image. Also shown is the minimum segment size for user data. Constant data is assumed to be part of the code space.

Table 2.6 Memory Usage

Device	Firmware Version	EEPROM Space (Bytes)	Segment Size (Bytes)
PL 3120 Smart Transceiver	14	3969	8
PL 3170 Smart Transceiver	17	3964	8
PL 3150 Smart Transceiver	14 or newer	384	2

EEPROM must be allocated in increments of the device's segment size, the smallest unit of EEPROM that can be allocated for variable space. For example, if there are three 3-byte variables used, there must be 9 bytes of variable space. For a PL 3120 or PL 3170 Smart Transceivers, this would result in the allocation of 16 bytes for variable space, as 16 bytes is the lowest increment of the device segment size (8 bytes) that can store the three 3-byte variables. For a PL 3150 Smart Transceiver, this would result in the allocation of 10 bytes for variable space, as 10 bytes is the lowest increment of the device segment size (2 bytes) that can store the three 3-byte variables.

Static RAM

The PL Smart Transceivers contain 2048 bytes of static RAM.

The RAM is used to store the following:

- Stack segment, application, and system data
- Network buffers and application buffers

The RAM state is retained as long as power is applied to the device. After reset, releasing the PL Smart Transceiver initialization sequence will clear the RAM (see the section *Reset Processes and Timing* for more information).

Pre-programmed ROM

The PL 3120 and PL 3170 Smart Transceivers contain 24,576 bytes of pre-programmed ROM. This memory contains the Neuron firmware, including the LonTalk protocol stack, real time task scheduler, and system function libraries. The Neuron firmware for the PL 3150 Smart Transceiver is stored in external memory. The Neuron firmware is supplied with the NodeBuilder and Mini EVK tools.

PL 3150 Smart Transceiver External Memory Interface

The external memory interface of the PL 3150 Smart Transceiver (the PL 3120 and PL 3170 Smart Transceivers have no external memory interface) supports up to 42K Bytes of external memory for additional user program and data. The total address space is 64K Bytes. However, the upper 6k of address space is reserved for internal RAM, EEPROM, and memory-mapped I/O (see Figures 2.5 and 2.6), leaving 58K Bytes of external address space. Of this space, 16K Bytes is used by the Neuron firmware. The external memory space can be populated with RAM, ROM, PROM, EPROM, EEPROM, or flash memory in increments of 256 bytes. The memory map for the PL 3150 Smart Transceiver is shown in Figure 2.5. The bus has 8 bidirectional data lines and 16 address lines driven by the processor. Two interface lines (R/W~ and E~) are used for external memory access. Refer to the *PL 3150 Smart Transceiver Datasheet* for the required access times for the external memory used. The input clock rates supported by the PL 3150 Smart Transceiver are 10MHz and 6.5536MHz. The Enable Clock (E~) runs at the system clock rate, which is one-half the input clock rate. All memory, both internal and external, can be accessed by any of the three processors at the appropriate phase of the instruction cycle. Because the instruction cycles of the three processors are offset by one-third of a cycle with respect to each other, the memory bus is used by only one processor at a time.

The *Neuron 3150 Chip External Memory Interface* engineering bulletin provides guidelines for interfacing the PL 3150 Smart Transceiver to different types of memory. A minimum hardware configuration would use one external ROM (PROM or EPROM), containing both the Neuron firmware and user application code. This configuration would **not** allow the system engineer to change the *application code* over the network after installation. The *network image* (*network address* and *connection* information) however, could be altered because this information resides in internal EE-PROM. If application downloads over the network are a requirement for maintenance or upgrade and the application code will not fit into the internal EEPROM, then external EEPROM or flash will be necessary. Refer to the *Neuron C Programmer's Guide* for guidelines to reduce code size.

The pins used to interface with external memory are listed in Table 2.7. The E~ clock signal is used to generate read (or write) signals to external memory. The A15 (address line 15) or a programmable array logic (PAL) decoded signal gated with R/W~ can be used to generate read signals to external memory.

Table 2.7 External Memory Interface Pins

Pin Designation	Direction	Function
A0 - A15	Output	Address Pins
D0 - D7	Input/Output	Data Pins
E	Output	Enable Clock
R/W	output	Read/Write Select Low

The PL Smart Transceiver can be interfaced to another MPU through the 12 I/O pins using a serial or parallel connection, or through a dual-ported RAM device such as the Cypress CY7C144, CY7C138, or CY7C1342. There are pre-defined serial and parallel I/O models for this purpose which are easily implemented. Use the Neuron C programming language, ShortStack firmware, or MIP firmware to simplify the interface. For more details of dual-ported RAM interfacing, see Appendix B of the *LONWORKS Microprocessor Interface Program User's Guide* (Echelon 078-0017-01).

Input/Output

Twelve Bidirectional I/O Pins

These pins are usable in several different configurations to provide flexible interfacing to external hardware and access to the internal timer/counters. The logic level of the output pins can be read back by the application processor.

Pins IO4 – IO7 and IO11 have programmable pull-up current sources. They are enabled or disabled with a compiler directive (see the *Neuron C Reference Guide*). Pins IO0 – IO3 have high current sink capability (20 mA @ 0.8 V). The others have sink capability of 1.4 mA @ 0.5 V. All pins (IO0 – IO11) have TTL level inputs with hysteresis. Pins IO0 – IO7 also have low level detect latches.

Two 16-Bit Timer/Counters

The timer/counters are implemented as a load register writable by the processor, a 16-bit counter, and a latch readable by the processor. The 16-bit registers are accessed 1 byte at a time. The PL Smart Transceivers have one timer/counter whose input is selectable among pins IO4 – IO7, and whose output is pin IO0, and a second timer/counter with input from pin IO4 and output to pin IO1 (Figure 2.7). No I/O pins are dedicated to timer/counter functions. If, for example, Timer/Counter 1 is used for input signals only, then IO0 is available for other input or output functions. Timer/counter clock and enable inputs can be from external pins, or from scaled clocks derived from the system clock; the clock rates of the two timer/counters are independent of each other. External clock actions occur optionally on the rising edge, the falling edge, or both rising and falling edges of the input.

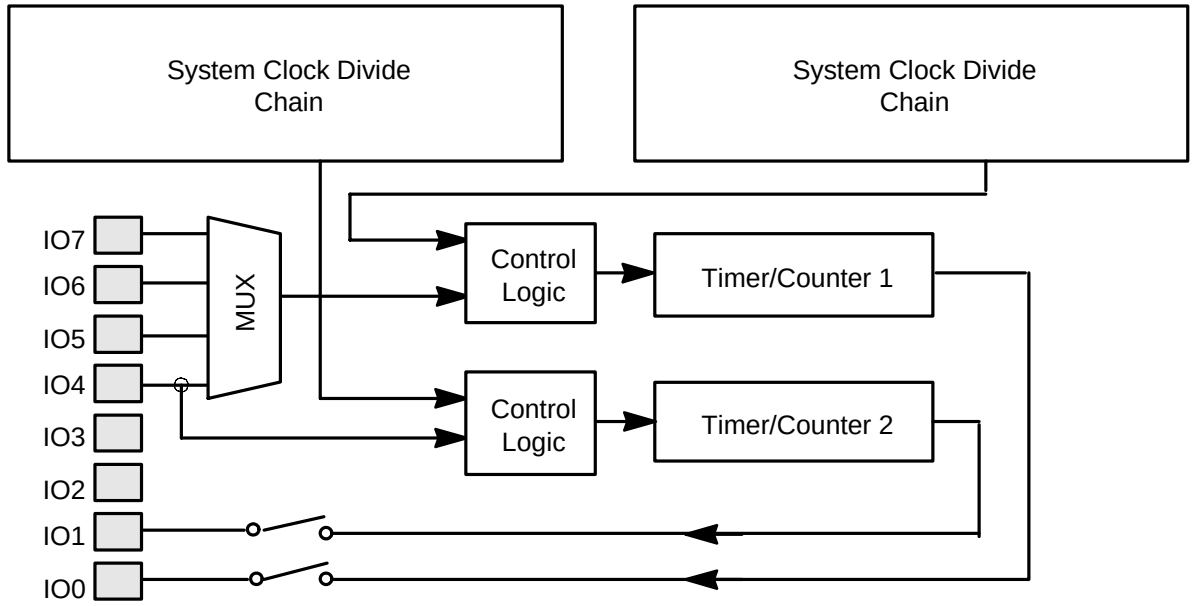


Figure 2.7 Timer/Counter Circuits

Clock Input

The PL Smart Transceiver requires a 10.0000MHz clock signal for C-band operation and a 6.5536MHz signal for A-band operation. This clock can be provided by connecting an appropriate parallel resonant crystal to the XIN and XOUT pins of the PL Smart Transceiver as shown in Figure 2.8.

The Smart Transceiver IC includes on-chip crystal load capacitors. If a crystal is chosen with a load capacitance rating that matches the capacitance provided by the combination of the PL Smart Transceiver IC and the XIN and XOUT circuit traces, then off-chip load capacitors are not needed. If the developer prefers to use a crystal with a different load capacitance rating, then each reference layout for the PL smart Transceiver includes provision for optional off-chip capacitors to tune the design to match different crystals (see Appendix A for a list of reference designs). The schematic for each reference design includes a table listing crystal and load capacitance options. These tables cover crystal load capacitance values ranging from 15 to 20pF.

Crystals with load capacitance ratings greater than 20pF should not be used with PL Smart Transceiver chips. Even though the optional off-chip capacitors would allow centering the frequency of oscillation, using more than 20pF of load capacitance could prevent the oscillator from starting under worst-case conditions. To further ensure proper oscillator startup, the ESR specification for the crystal should be ≤60Ω for C-band operation and ≤100Ω for A-band use.

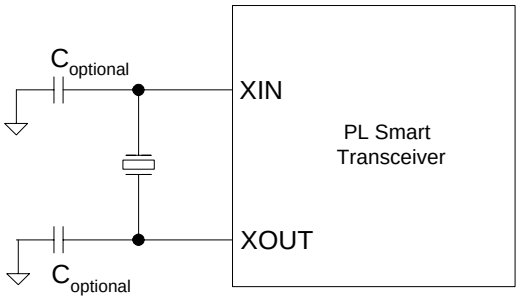


Figure 2.8 PL 3120, PL 3150, PL 3170 Smart Transceiver crystal clock connections

The PL Smart Transceiver requires a clock frequency accuracy of ±200ppm over the full range of component tolerances and operating conditions. Variation within the PL Smart Transceiver IC uses a portion of the overall ±200ppm budget. The remaining portion of the error budget allocated for *total crystal uncertainty* is ±85ppm (assuming that the selected crystal has a load capacitance specification which matches the circuit loading as described above). *Total crystal uncertainty* is the combination of the crystal's initial frequency tolerance plus its temperature and aging tolerances. Note that a typical crystal aging specification is 5ppm/yr but, since the aging effect tends to follow a logarithmic curve, aging over a 10 year span is commonly in the range of 10 to 15ppm (contact individual crystal vendors for detailed specifications regarding their particular products).

If the load capacitance specification of the crystal is not matched to the circuit design then the nominal frequency will not match the design center and the error budget for the crystal will be reduced. For example, using a 20pF crystal in a circuit designed to provide 18pF of loading results in about a 40ppm upward shift in the nominal frequency of oscillation. Thus a 2pF mismatch consumes nearly half of one side of the error budget. The resulting error budget for the crystal in this particular example would be +45/-125ppm. This example points out the importance of directly copying the selected reference layout so that differences in trace capacitance do not pull the nominal frequency away from the design center.

If a 10.0000MHz clock signal is already available elsewhere on a C-band circuit board (6.5536MHz for an A-band board) then it can be used as a clock source for the PL Smart Transceiver as long as the clock signal meets several requirements. First the clock must have an accuracy of ±200ppm over all operating conditions. Its duty cycle symmetry must be no worse than 60/40% when connected to a 33pF load and measured using a 0.9V threshold. In addition the voltage swing of the clock signal must be within the GND and V_{DD5} supply rails of the PL Smart Transceiver. To use this clock option, the appropriate clock signal should be connected to the XIN pin of the PL Smart Transceiver and the XOUT pin of the PL Smart Transceiver should be left open. Note also that appropriate high frequency clock distribution techniques must be used to ensure that a clean clock signal is present at the XIN pin of the PL Smart Transceiver.

The accuracy of any clock oscillator should be checked during the design verification phase of every PL Smart Transceiver based product. This measurement must be made without adding any capacitance to either the XIN or XOUT pins of the PL Smart Transceiver. Holding a probe near but not touching the clock lines and then connecting this probe to a spectrum analyzer with an accurate time-base provides one way to make this measurement without affecting the frequency of oscillation.

Band-In-Use (BIU) and Packet Detect (PKD) LED Connections

The PL Smart Transceiver supplies two output signals, PKD and BIU, that are intended to drive low-current light-emitting diodes (LEDs). Both signals are active-high and must be connected to separate LEDs, with series current-limiting resistors added between the LEDs and ground. The PKD and BIU pins are rated to source up to 12mA.

A Band-In-Use detector, as defined under CENELEC EN 50065-1, must be active whenever a signal that exceeds 86dBμV_{RMS} anywhere in the frequency range 131.5kHz to 133.5kHz is present for at least 4ms. The Band-In-Use detector is defined by CENELEC EN 50065-1 as part of the CENELEC access protocol. The Smart Transceiver incorporates the CENELEC access protocol, and the PL Smart Transceiver can be programmed to enable or disable its operation (See the *CENELEC Access Protocol* section in Chapter 8). When the PL Smart Transceiver is programmed to enable the CENELEC access protocol the state of the Band-in-Use signal regulates the flow of packet transmissions in accordance with CENECLEC-defined conditions. When the CENELEC access protocol is disabled, an active BIU signal has no affect on PL Smart Transceiver transmissions

The Band-In-Use function is defined for use in the CENELEC C-band and is not required for A-band operation. When the PL Smart Transceiver is programmed with proper A-band transceiver parameters, as described in Chapter 8, an active BIU signal does not prevent the PL Smart Transceiver from transmitting.

The PKD signal is active whenever a LonTalk packet addressed to any device is being received by the PL Smart Transceiver. The receive sensitivity of the transceiver is considerably greater than that of the BIU indicator. The PKD signal will go active when the PL Smart Transceiver receives packets whose signal level is as small as 36dBμV_{RMS}. Thus it is not uncommon for the PKD indicator to signal that a packet is present without the BIU indicator turning on; this occurs in cases where the signal strength of a received packet is less than the BIU threshold.

ESD protection diodes should be connected to the BIU and PKD lines in applications where BIU and PKD drive LEDs that could be subject to ESD exceeding 2kV. Refer to the *Design for Electrostatic Discharge Compliance* section of Chapter 6 for recommendations regarding ESD protection.

TXON Output Signal

TXON is a buffered version of the internal signal used to control the transceiver's transmit amplifier. The TXON output pin is active high while the PL Smart Transceiver is transmitting packets. This pin is rated to source up to 12mA. TXON can be used to drive a low-current LED to indicate transmit activity. A series current-limiting resistor is required between the LED and ground. ESD protection diodes should be connected to this pin in applications where the TXON signal line could be subjected to ESD exceeding 2kV.

Additional Functions

Reset Function

The reset function is a critical operation in any embedded microcontroller. In the case of the PL Smart Transceiver, the reset function plays a key role in the following conditions:

- Initial V_{DD5} power up (reset ensures proper initialization of the PL Smart Transceiver during power up).
- V_{DD5} power down (reset ensures proper shut down of the PL Smart Transceiver).
- Fluctuations in the V_{DD5} supply voltage (reset manages proper recovery of PL Smart Transceiver state after V_{DD5} stabilizes).
- Program recovery (if an application gets lost due to corruption of address or data the Smart Transceiver's watchdog timer initiates a watchdog reset event).
- Protecting the internal EEPROM of a PL 3120 or PL 3170 Smart Transceiver from corruption (an internal LVI insures that the transceiver is held in reset when the V_{DD5} supply is below a level that is safe for the EE activity).

The PL Smart Transceivers have four mechanisms to initiate a reset:

- RESET~ pin pulled low and then returned high.
- Software command either from the application program or from the network.
- Low-Voltage Indicator (LVI) detects a drop in the power supply below a set level.
- Watchdog timeout occurs during application execution (the timeout period is 840ms at 10MHz; this figure scales inversely with clock frequency).

When in reset, the pins of the PL Smart Transceiver go to the states described in the list below. Figure 2.10 shows the state of the pins during reset and the initialization sequence just after reset.

- Oscillator continues to run
- All processor functions stop
- SERVICE~ pin goes to high impedance (except for pull-up current source)
- I/O pins go to high impedance
- Address pins go to 0xFFFF (PL 3150 Smart Transceiver only)
- All data pins become outputs with low states (PL 3150 Smart Transceiver only)
- E~ clock goes high (PL 3150 Smart Transceiver only)
- R/W~ goes low (PL 3150 Smart Transceiver only)

When the RESET~ pin is released back to a high state, the PL Smart Transceiver begins its initialization procedure starting at address 0x0001. The time it takes the PL Smart Transceiver to complete its initialization differs between PL Smart Transceivers, the different firmware versions that are being run, and the memory space used by the application (code and data). This will be discussed later in this section.

RESET~ Pin

The RESET~ pin is both an input and an output. The RESET~ pin includes an internal current source that acts as a pull-up resistor. The RESET~ pin acts an output when any of the following events occur:

- The Smart Transceiver's internal low-voltage indicator (LVI) detects a low voltage condition
- The Smart Transceiver's software program initiates a reset event
- The Smart Transceiver's Watchdog Timer times out

In some cases it is desirable to use the input capability of RESET~ pin to allow other devices to reset the Smart Transceiver. Examples of external devices that may be used for this purpose include push button switches, microcontrollers, and external low-voltage detectors.

WARNING: If the proper external reset circuitry is not used, the PL Smart Transceiver can go "applicationless" or unconfigured. The applicationless or unconfigured state occurs when the checksum error verification routine detects corruption in memory which could have falsely been detected due to an improper reset sequence.

The following guidelines must be followed in order for the transceiver's reset functions to operate reliably:

- Any device connected to the RESET~ pin must have an open-drain (or equivalent) output. If an external device were to actively drive the RESET~ pin high, contention between that device and the Smart Transceiver's internal circuitry could result in anomalous behavior ranging from "applicationless" errors to device failure.
- If any external devices are connected to the RESET~ pin of the Smart Transceiver then a capacitor should be connected between RESET~ and ground in order to provide noise immunity. The value of this capacitor should be at least 100pF and must not exceed 1000pF. For even greater noise immunity, two capacitors (totaling ≤1000pF) can be used with one connected from the RESET~ pin to ground and the other from RESET~ to V_{DD5}. These capacitors should be located within 15mm of the Smart Transceiver's RESET~ pin.
- During board level in-circuit testing (ICT) the RESET~ pin should be hard wired to ground via a "pogo pin". The PL Smart Transceiver is sensitive to disruptions in on the RESET~ pin during the time it is performing its initial (one time) boot initialization sequence. For in-circuit test purposes a single test point with a trace of ≤2cm to the RESET~ pin is recommended.
- When using an external oscillator to drive the XIN pin of the PL Smart Transceiver, a power-on-pulse-stretching LVI with a delay ≥10ms is recommended in order to ensure that the external oscillator has stabilized before the PL Smart Transceiver is released from reset.
- A PL 3150 Smart Transceiver-based device must use an external pulse stretching LVI. This device must not just stretch reset events caused by low-voltage conditions but other reset events must also be stretched to a minimum of 10ms. The thresholds for this external LVI must be a minimum of 4.5V and maximum of 4.75V. Echelon recommends the use of the DS1813-5 LVI from Maxim Integrated Products (www.maxim-ic.com). Figure 2.9 shows a typical external reset circuit for a PL 3150 Smart Transceiver.
- A PL 3120 or PL 3170 Smart Transceiver-based device with no external devices attached to the RESET~ pin does not require an external LVI or any additional capacitance on the RESET~ line.

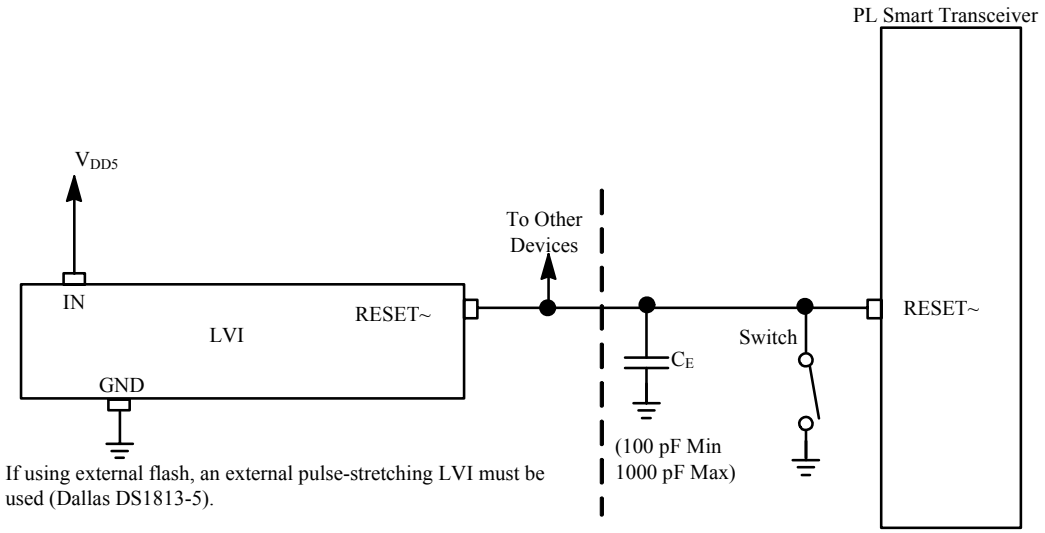


Figure 2.9 Example Reset Circuit For PL 3150 Smart Transceiver-based Devices

Power Up Sequence

During power up sequences, the RESET~ pin will be held low by the internal LVI until the power supply is stable. Likewise, when powering down, the PL Smart Transceiver RESET~ pin is driven low when the power supply goes below the Smart Transceiver's minimum operating voltage. Refer to the *PL 3120/PL 3150 or PL 3170 Smart Transceiver Datasheets* for LVI trip points.

Software Controlled Reset

When the CPU watchdog timer expires, or a software command to reset occurs, the RESET~ pin is pulled low for 256 XIN clock cycles.

Watchdog Timer

The PL Smart Transceivers are protected against malfunctioning software or memory faults by three watchdog timers, one for each processor that makes up the Neuron core. If application or system software fails to reset these timers periodically, the entire PL Smart Transceiver is automatically reset. The watchdog period is approximately 840 ms at a 10MHz input clock rate and scales inversely with the input clock rate. The Watchdog Timer circuit is always active and cannot be disabled.

ICTMode pin

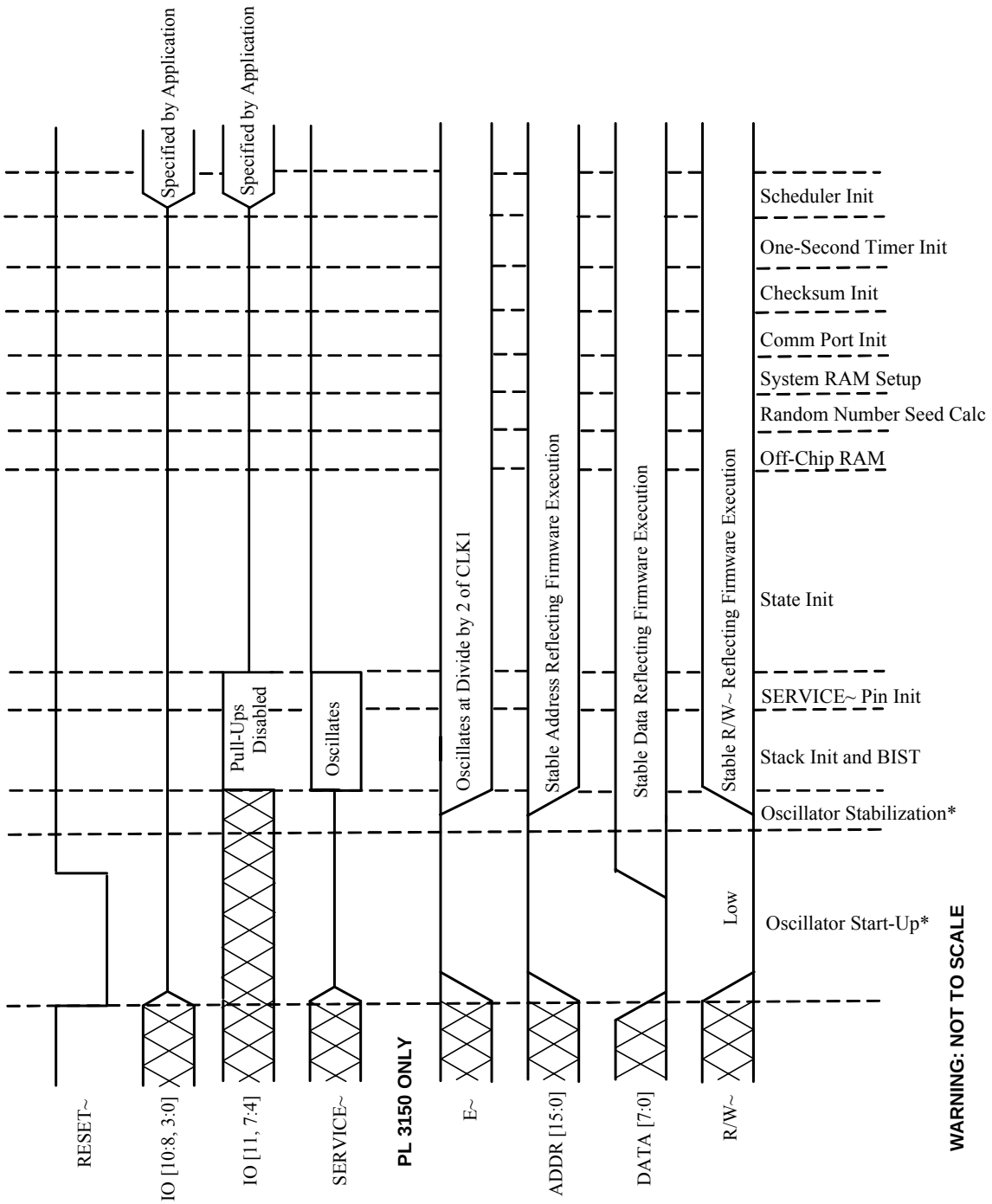
During normal operation of the PL Smart Transceiver the ICTMode pin should be in a logic low state. This pin can be used during the production test of a PL 3150 Smart Transceiver-based device to tri-state the memory interface lines for in-circuit testing (ICT). Driving the ICTMode pin high and the RESET~ pin low places all Smart Transceiver outputs in tri-state mode. Each PL 3150 reference design from Appendix A includes a pull-down resistor on the ICTMode pin so that this pin can be driven high by an in-circuit tester. Note that ICT can be performed on PL 3120 and PL 3170 Smart Transceiver I/O pins by driving the RESET~ pin low – without driving the ICTMode pin. For this reason the ICTMode pin on all PL 3120/PL 3170 reference designs from Appendix A have their ICTmode pin tied directly to ground.

Reset Processes and Timing

During the reset period, the I/O pins are in a high-impedance state. The PL 3150 Smart Transceiver address lines A15 – A0 are forced to 0xFFFF, R/W~ is forced to 0, and E is forced to 1. The data lines are driven low, so they will not float and draw excess current. The SERVICE~ pin is high impedance during reset and the internal pull-up is disabled. Reset overrides the effect of E~ clock on data lines in that, in normal operations the data bus is only driven in a write cycle during the E clock low portion of the bus cycle, while reset forces the data bus to be driven. The steps followed in preparing the PL Smart Transceiver to execute the application code are discussed below. These steps are summarized in Figure 2.10.

After the RESET~ pin is released, the PL Smart Transceiver performs hardware and firmware initialization before executing application programs. These tasks are:

- Oscillator start-up
- Oscillator stabilization
- Stack initialization and built-in self-test (BIST)
- SERVICE~ pin initialization
- State initialization
- Off-chip RAM initialization
- Random number seed calculation
- System RAM setup
- Communication port initialization
- Checksum initialization
- One-second timer initialization
- Scheduler initialization



*NOTE: On power up, the oscillator will start running before RESET~ is released.

Figure 2.10 RESET Timeline for PL Smart Transcievers

During internal oscillator start up (after power up), the PL Smart Transceiver waits for the oscillator signal amplitude to grow before using the oscillator waveform as the system clock. This period depends on the type of oscillator used and its frequency, and begins as soon as power is applied to the oscillator and is independent of the RESET~ pin.

After the oscillator has started up, the PL Smart Transceiver counts additional transitions on XIN to allow the oscillator's frequency to stabilize. From the time RESET~ is asserted until the end of the oscillator stabilization period, the I/O pins are in a high-impedance state. The E~ signal goes inactive (high) immediately after reset goes low, and the address bus becomes high (0xFFFF) to deselect external devices.

The stack initialization and BIST task tests the on-chip RAM, the timer/counter logic, and the counter logic. For the test to pass, all three processors and the ROM must be functioning. A flag is set to indicate whether the PL Smart Transceiver passed or failed the BIST. The RAM is cleared to all 0s by the end of this step. The SERVICE~ pin oscillates between a solid low and a weak high. The memory interface signals reflect execution of these tasks.

If the RAM self-test fails, the device goes offline, the service LED comes on solid, and an error is logged in the device's status structure.

Self-test results are available in the first byte of RAM (0xE800) as follows:

Value	**Description**
0	No Failure
1	RAM failure
2	Timer/counter failure
3	Counter failure
4	Configured input clock rate exceeds the chip maximum

The SERVICE~ pin initialization task turns off the SERVICE~ pin (high state).

The state initialization task determines if a PL Smart Transceiver boot is required (PL 3150 Smart Transceiver only), and performs the boot if it is required. The PL Smart Transceiver decides to perform a boot if it is blank, or if the boot ID does not match the boot ID in ROM.

The off-chip RAM initialization task checks the memory map to determine if any off-chip RAM is present and then either tests and clears all of the off-chip RAM or, optionally, clears the application RAM area only. This choice is controlled by the application program via a Neuron C compiler directive. This task applies only to the PL 3150 Smart Transceiver.

The random number seed calculation task creates a seed for the random number generator.

The system RAM setup task sets up internal system pointers as well as the linked lists of system buffers.

The checksum initialization task generates or checks the checksums of the nonvolatile writable memories. If the boot process was executed for the configured or unconfigured states, in the state initialization task, then the checksums are generated; otherwise, they are checked. This process includes on-chip EEPROM, off-chip EEPROM, flash, and off-chip nonvolatile RAM. There are two checksums, one for the configuration image and one for the application image. In each case, the checksum is a negated two's complement sum of the values in the image.

The one-second timer initialization task initializes the one-second timer. At this point, the network processor is available to accept incoming packets.

The scheduler initialization task allows the application processor to perform application-related initialization as follows:

- **State wait** — Wait for the device to leave the applicationless state.
- **Pointer initialization** — Perform a global pointer initialization.
- **Initialization step** — Execute initialization task, which is created by the compiler/linker to handle initialization of static variables and the timer/counters.

- **I/O pin initialization step** — Initialize I/O pins based on application definition. Prior to this point, I/O pins are high impedance.
- **State wait II** — Wait for the device to leave the unconfigured or hard-offline state. If waiting was required, a flag is set to indicate that the device should come up offline.
- **Parallel I/O synchronization** — Devices using parallel I/O attempt to execute the master/slave synchronization protocol at this point.
- **Reset task** — Execute the application reset task (`when (reset){ }`).
- If the offline flag was set, go offline and execute the offline task (`when(offline){}`). If the BIST flag indicated a failure, then the SERVICE~ pin is turned on and the offline task is executed. Otherwise, the scheduler starts its normal task scheduling loop.

The amount of time required to perform these steps depends on many factors, including: PL Smart Transceiver model; input clock rate; whether or not the device performs a boot process; whether the device is applicationless, configured, or unconfigured; amount of off-chip RAM; whether the off-chip RAM is tested or simply cleared; the number of buffers allocated; and application initialization. Tables 2.8 and 2.9 summarize the number of input clock cycles (XIN) required for each of these steps for the PL 3120 and the PL 3150 Smart Transceivers. The times are approximate and are given as functions of the most significant application variables.

Table 2.8 PL 3120 Smart Transceiver Reset Sequence Time

Step	Number of XIN Cycles	Notes
Stack Initialization and BIST	386,000	
SERVICE~ Pin Initialization	1000	
State Initialization	250 (for no boot) 2,275,000 (for boot)	
Off-Chip RAM Initialization	0	
Random Number Seed Calculation	0	1
System RAM Set-up	21,000 + 600*B	2
Communication Port Initialization	0	1
Checksum Initialization	3400 + 175*M	3
One-Second Timer Initialization	6100	
Scheduler Initialization	≥ 7400	4

Notes:

1) These tasks run in parallel with other tasks.

2) B is the number of application and/or network buffers allocated.

3) M is the number of bytes to be checksummed.

4) Assumes a trivial initialization task, no reset task and the configured state.

For example, the timing of each of these steps is shown for a PL 3120 Smart Transceiver application with the following parameters:

- 10MHz input clock
- Crystal oscillator
- No boot required, at least 10 application and/or network buffers
- 500 bytes of EEPROM checksummed.

Stack Initialization and BIST	38.6000 ms
SERVICE~ Pin Initialization	0.1000 ms
State Initialization	0.0250 ms
Off-Chip RAM Initialization	0 ms
Random Number Seed Calculation	0 ms
System RAM Setup	2.7000 ms
Communication Port Initialization	0.0000 ms
Checksum Initialization	10.8000 ms
One-Second Timer Initialization	0.6100 ms
Scheduler Initialization	0.7400 ms
Total	53.5757 ms

Table 2.9 PL 3150 Smart Transceiver Reset Sequence Time

Step	Number of XIN Cycles	Notes
Stack Initialization and BIST	425,000	
SERVICE~ Pin Initialization	1000	
State Initialization	1300 (for no boot) 70,000 + 25 ms*E (for boot)	1
Off-Chip RAM Initialization	24,000 + 214*R (for test and clear) 24,000 + 152*R_a (for clear only)	2 3
Random Number Seed Calculation	50,000 max	
System RAM Setup	27,000 + 1500*B	4
Communication Port Initialization	0	5
Checksum Initialization	7200 + 175*M (for no boot) 82,000 + 100 ms + 175*M (for boot)	6, 7
One-Second Timer Initialization	6100	
Scheduler Initialization	≥ 7400	8

***Notes*:**

1) E is the number of non-zero bytes being written (ranges from 10 to 504).

2) R is the number of off-chip RAM bytes.

3) R_a is the number of non-system off-chip RAM bytes.

4) B is the number of application and/or network buffers allocated.

5) These tasks run in parallel with other tasks.

6) M is the number of bytes to be checksummed.

7) Only if booting to the configured or unconfigured state; if booting to the applicationless state, use the “no boot” equation.

8) Assumes a trivial initialization task, no reset task, and the configured state.

For example, the timing of each of these steps is shown for a PL 3150 Smart Transceiver application with the following parameters: 10MHz input clock, crystal oscillator, no boot required, 16K bytes external RAM, test and clear external RAM, at least 10 application and/or network buffers, and 500 bytes of EEPROM checksummed.

Stack Initialization and BIST	42.50 ms
SERVICE~ Pin Initialization	0.10 ms
State Initialization	0.13 ms
Off-Chip RAM Initialization	353.00 ms
Random Number Seed Calculation	5.00 ms
System RAM Setup	4.20 ms
Communication Port Initialization	0 ms
Checksum Initialization	12.50 ms
One-Second Timer Initialization	0.61 ms
Scheduler Initialization	0.74 ms
Total	418.78 ms

Use the following compiler directive to disable testing of off-chip RAM:

```
# pragma ram_test_off
```

SERVICE~ Pin

The SERVICE~ pin alternates between input and open-drain output at a 76 Hz rate with a 50% duty cycle with a 10MHz input clock. At 6.5536MHz, the SERVICE~ pin alternates at a 50 Hz rate. When it is an output, it can sink 20 mA for use in driving a LED. When it is used exclusively as an input, it has an optional on-chip pull-up to bring the input to an inactive-high state for use when the LED and pull-up resistor are not connected. Under control of the Neuron firmware, this pin is used during configuration, installation, and maintenance of the device containing the PL Smart Transceiver. The firmware flashes the LED at a 1/2 Hz rate when the PL Smart Transceiver has not been configured with network address information. Grounding the SERVICE~ pin causes the PL Smart Transceiver to transmit a network management message containing its unique 48-bit Neuron ID and the application's program ID on the network. This information can then be used by a network tool to install and configure the device. A typical circuit for the SERVICE~ pin LED and push-button is shown in Figure 2.11. During reset the SERVICE~ pin state is indeterminate. The default state of the SERVICE~ pin pull-up is enabled.

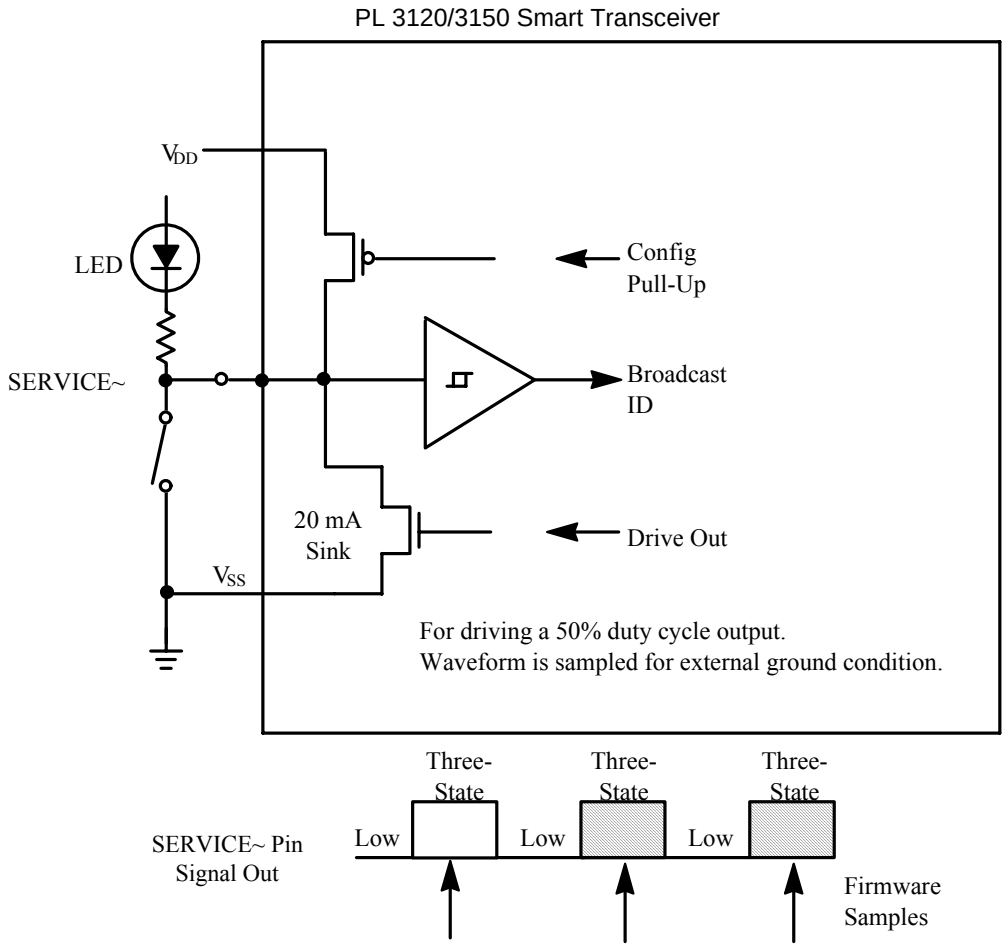


Figure 2.11 PL Smart Transceiver SERVICE~ Circuit

Table 2.10 Service LED Behavior During Different States

Device State	**0xF015 State Code**	**Service LED**
Applicationless and Unconfigured	3	On
Unconfigured (but with an Application)	2	Flashing
Configured, Hard Offline	6	Off
Configured	4	Off
PL 3150 Defective External Memory	—	On

The SERVICE~ pin is active low and the service pin message is sent at most once per SERVICE~ pin transition. The service pin message goes into the next available priority or non-priority output network buffer. Devices in the applicationless state that do not have an external pullup will transmit the SERVICE~ pin message after every reset.

Integrity Mechanisms

Memory Integrity Using Checksums

To ensure the integrity of the memory of the PL Smart Transceiver, the Neuron firmware maintains a number of checksums. Each checksum is a single byte and is the two's complement of the sum of all bytes it covers. These checksums are verified during reset processing and also on a continual basis via a background diagnostic process. There are three main checksums used to verify the integrity of the PL Smart Transceiver's memory:

- Configuration image checksum
- Application image checksum
- System image checksum (off-chip system image only)

The configuration image checksum covers the network configuration information and communication parameters residing in the on-chip EEPROM. The default behavior is that a configuration checksum error causes the device to go to the unconfigured state. Refer to Table 2.12 for other options.

The application image checksum covers the application code in both on-chip EEPROM and any application code in off-chip EEPROM, NVRAM, or flash memory. This checksum can optionally be extended to cover any application code in off-chip ROM as well. The default behavior is that an application checksum error causes the device to go to the applicationless state. Application read/write data residing in EEPROM, NVRAM, or flash is not checksummed. Refer to Table 2.12 for other options.

Table 2.11 Checksum Coverage of PL Smart Transceiver Memory Areas

Memory Area	Checksum
System image (optionally covered by application checksum on the PL 3150)	System
Any off-chip ROM code (optionally covered by Application checksum on the PL 3150)	Application
Any off-chip flash, EEPROM, or NVRAM code	Application
Any off-chip RAM code	Application
Configuration image	Configuration
All on-chip EEPROM code	Application

In the PL 3150 Smart Transceiver, all memory areas listed in Table 2.11 except for on-chip EEPROM code have their own checksum so that checksum errors can be further isolated. An unconfigured or configured device continually checks its application checksum in the background at the rate of 1 byte per iteration through the network processor's main loop (3 bytes per millisecond when running at 10MHz with no network activity).

The system image checksum covers the system image. It is only available when the system image resides in off-chip memory and its use is optional. A system image checksum error always forces the device to the applicationless state.

No checksum is computed if the device is in the applicationless state.

The checksums are all verified during reset processing by the network processor and as part of the background diagnostic process. The background diagnostic process causes the device to reset when an error is detected; no state change occurs. It is assumed that any persistent error will be found by the reset processing.

Upon detecting a checksum error, the reset process will force the appropriate state and log an error in the error log. For the PL 3150 Smart Transceiver, a checksum must fail twice during reset processing in order for it to be deemed bad.

Reboot and Integrity Options Word

A PL 3150 Smart Transceiver has a number of options for actions taken following a checksum error or other memory related fatal errors. The 16-bit word that controls these options resides in the system image and is defined as part of the device's export options in the NodeBuilder or Mini EVK tools.

The recovery process relies on the fact that the initial on-chip EEPROM image for the application, configuration, and communication parameter data reside in the off-chip system image. During initial power up, the system image data is copied (booted) to on-chip EEPROM. The recovery process recopies or reboots the suspect areas as dictated by the error and the recovery options. **Any changes made to the on-chip EEPROM (e.g., a network application load or network tool initiated reconfiguration) after the initial boot are lost in the recovery process.** The recovery action is defined by setting a combination of bits as defined by the following bit masks (Table 2.12).

Table 2.12 Recovery Action Bit Masks

Recovery Word	Description
0x0001	Reboot application if application fatal error.
0x0002	Always reboot application on reset (see note).
0x0004	Reboot configuration if configuration checksum fails.
0x0008	Reboot configuration on an application fatal error.
0x0010	Always reboot configuration on reset.
0x0020	Reboot communication parameters if configuration checksum fails.
0x0040	Reboot communication parameters if type or rate mismatch.
0x0080	Always reboot communication parameters on reset.
0x0100	Reboot EEPROM variables when rebooting application.
0x0200	Applicationless state is considered to be an application fatal error. If option 0x0001 or 0x0008 is set, applicationless state will result in a reboot. Application fatal errors are defined below (see note).
0x0400	Checksum all code, including system image.

Note: Applications exported with these options cannot be loaded over the network.

In the above options, "configuration" does not include the communication parameters because their recovery is governed separately. Also, fatal application errors refer to application image checksum errors, memory allocation failures, and memory map failures. Refer to *Loading an Application Image* in the *NodeBuilder User's Guide* (Release 3 Revision 2 or later) for more information.

The configuration will be rebooted independently of the application only if all the configuration table sizes match between EEPROM and ROM. This avoids a situation where a new application with different table sizes is loaded over the network, and a reboot of the configuration corrupts the program.

When an EEPROM recovery occurs due to a checksum failure or other error, the event will be logged in the error table of the Smart Transceiver. A test command will show **EEPROM recovery occurred** as the last error logged.

Reset Processing

During reset processing, the configuration checksum is checked first. If bad, and no configuration recovery options are set, then a configuration checksum error is logged, the checksum repaired, and the device state is changed to unconfigured. If the configuration recovery option is set, the configuration is recovered.

Next, the application checksum is checked. If bad, and the checksum error is in the system image, then a system image checksum error is logged and the device state is changed to applicationless.

If the application checksum is bad, and no application recovery options are set, an application checksum error is logged and the device state is changed to applicationless.

If the application checksum is bad and an application recovery option is set and the boot application does not contain references to any off-chip ROM, flash, EEPROM, NVRAM, or RAM code, or there are no checksum errors in any of these regions, then the application is recovered. Otherwise, an application checksum error is logged and the device goes applicationless.

Signatures

All off-chip code areas have a 2-byte cyclic redundancy check (CRC) called the **signature**, immediately following the area checksum. Signatures are stored in the code area and in the memory map. Mismatches between the area signature and memory map copy of the signature result in the device going applicationless. This mechanism prevents a partial application load over the network which is incompatible with any unloaded code (such as code in ROM).

Chapter 3

Input/Output Interfaces

Introduction

The PL 3120, PL 3150, and PL 3170 Power Line Smart Transceivers connect to application-specific external hardware via 12 pins, named IO0-IO11. These pins can be configured in numerous ways to provide flexible input and output functions with minimal external circuitry. The programming model (Neuron C language) allows the programmer to declare one or more pins as I/O objects. An I/O object provides programmable access to an I/O driver for a specified on-chip I/O hardware configuration and a specified input or output waveform definition. With the exception of the SCI (UART) model, the user's program can then refer to these objects in `io_in` and `io_out()` system calls to perform the actual input/output function during execution of the program. Certain events are associated with changes in input values. The task scheduler can thus execute associated application code when these changes occur.

There are many different I/O objects available for use with the PL Smart Transceivers. Most I/O Objects are available in the PL 3150, PL 3120, and PL 3170 Smart Transceiver system images by default. If an object that is not included in the default system image is required by an application, the development tool will link the appropriate object(s) into available memory space. For PL 3120 and PL 3170 Smart Transceiver designs, this means that internal EEPROM space must be used for the additional object. For PL 3150 Smart Transceiver designs, the object will be added to an external flash or ROM region beyond the 16KB space reserved for the system image.

PL Smart Transceivers have two 16-bit timer/counters on-chip (see Figure 2.7 and 3.1). The input to timer/counter 1, also called the *multiplexed timer/counter,* is selectable among pins IO4 – IO7, via a programmable multiplexer (MUX) and its output can be connected to pin IO0. The input to timer/counter 2, also called the *dedicated timer/counter,* can be connected to pin IO4 and its output to pin IO1. The timer/counters are implemented as a 16-bit load register writable by the CPU, a 16-bit counter, and a 16-bit latch readable by the CPU. The load register and latch are accessed a byte at a time. No I/O pins are dedicated to timer/counter functions. If, for example, timer/counter 1 is used for input signals only, then IO0 is available for other input or output functions. Timer/counter clock and enable inputs can be from external pins, or from scaled clocks derived from the system clock; the clock rates of the two timer/counters are independent of each other. External clock actions occur optionally on the rising edge, the falling edge, or both rising and falling edges of the input.

Multiple timer/counter input objects can be declared on different pins within a single application. By calling the `io_select()` function, the application can use the first timer/counter to implement up to four different input objects. If a timer/counter is configured to implement one of the output objects, or is configured as a quadrature input object, then it can not be reassigned to another timer/counter object in the same application program.

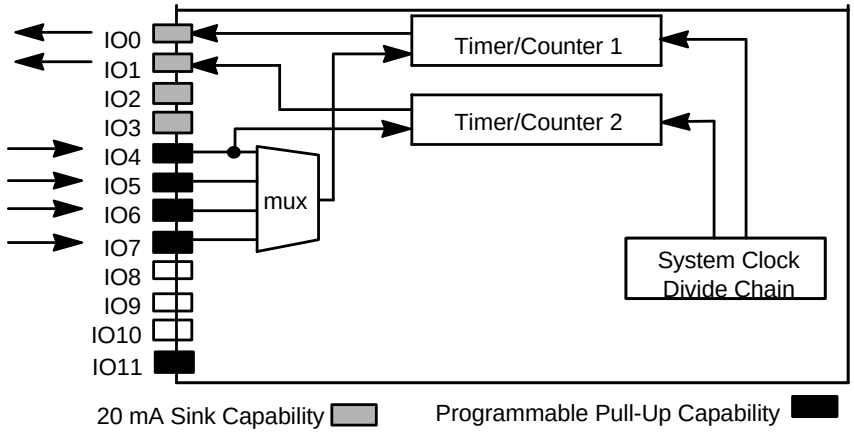


Figure 3.1 PL Smart Transceiver Timer/Counter External Connections

Hardware Considerations

Tables 3.1 through 3.5 list the available I/O objects. Various I/O objects of different types can be used simultaneously. Figure 3.3 summarizes the pin configuration for each of the I/O objects. For the electrical characteristics of these pins, refer to the *PL 3120/PL 3150 or PL 3170 Smart Transceiver Datasheets*. The following sections contain detailed descriptions of all the I/O objects. The application program can optionally specify the initial values of digital outputs. Pins configured as outputs can also be read as inputs, returning the value "at the I/O pin". Pins IO4 – IO7 and IO11 have optional pull-up current sources that act like pull-up resistors (see Figure 3.1). These are enabled with a Neuron C compiler directive (`#pragma enable_io_pullups`). Pins IO0 – IO3 have high sink capability. The others have standard sink capability. Pins IO0 – IO7 have low-level detect latches. **The latency and timing values described later in this section are typical at 10MHz.** The accuracy of these values is ± 10%. Most latency values scale inversely with clock rate.

The I/O pull-ups are not enabled during the stack initialization and BIST task. I/O pull-ups are only enabled if `#pragma enable_io_pullups` is specified in the Neuron C application. If an I/O pin is not used by the application, it must either be tied high or low on the PC board or left unconnected and configured as a bit output by the application in order to prevent unnecessary power consumption. This is particularly important for devices with energy storage power supplies (See Chapter 5 for more information).

Table 3.1 Summary of Direct I/O Objects

I/O Object	Applicable I/O Pins	Input/Output Value	Page
Bit Input	IO0 – IO11	0, 1 binary data	46
Bit Output	IO0 – IO11	0, 1 binary data	46
Byte Input	IO0 – IO7	0 – 255 binary data	48
Byte Output	IO0 – IO7	0 – 255 binary data	48
Leveldetect Input	IO0 – IO7	Logic 0 level detected	49
Nibble Input	Any adjacent 4 in IO0 – IO7	0 – 15 binary data	50
Nibble Output	Any adjacent 4 in IO0 – IO7	0 – 15 binary data	50

Table 3.2 Summary of Parallel I/O Objects

I/O Object	Applicable I/O Pins	Input/Output Value	Page
Muxbus I/O	IO0 – IO10	Parallel bidirectional port using multiplexed addressing	51
Parallel I/O	IO0 – IO10	Parallel bidirectional handshaking port	51

Table 3.3 Summary of Serial I/O Objects

I/O Object	Applicable I/O Pins	Input/Output Value	Page
Bitshift Input	Any adjacent pair (except IO7 + IO8 & IO10 + IO11)	Up to 16 bits of clocked data	59
Bitshift Output	Any adjacent pair (except IO7 + IO8 & IO10 + IO11)	Up to 16 bits of clocked data	59
I^2C	IO8 + IO9 or IO0 + IO1	Up to 255 bytes of bidirectional serial data	61
Magcard Input	IO8 + IO9 + (one of IO0 – IO7)	Encoded ISO7811 track 2 data stream from a magnetic card reader	63
Magtrack1	IO8 + IO9 + (one of IO0 – IO7)	Encoded ISO3554 track 1 data stream from a magnetic card reader	65
Magcard Bitstream	IO8 + IO9 + (one of IO0 – IO7)	Unprocessed serial data stream from a magnetic card reader	66
Neurowire I/O	IO8 + IO9 + IO10 + (one of IO0 – IO7)	Up to 256 bits of bidirectional serial data	66
Serial Input	IO8	8-bit characters	70
Serial Output	IO10	8-bit characters	70
Touch I/O	IO0 – IO7	Up to 2048 bits of input or output bits	72
Wiegand Input	Any adjacent pair in IO0 – IO7	Encoded data stream from Wiegand card reader	74
SCI (UART)	IO8 + IO10	Up to 255 bytes input and 255 bytes output	75
SPI	IO8 + IO9 + IO10 + (IO7)	Up to 255 byes of bidirectional data	76

Table 3.4 Summary of Timer/Counter Input Objects

I/O Object	Applicable I/O Pins	Input Signal	Page
Dualslope Input	IO0, IO1 + (one of IO4 – IO7)	Comparator output of the dualslope converter logic	83
Edgelog Input	IO4	A stream of input transitions	84
Infrared Input	IO4 – IO7	Encoded data stream from an infrared demodulator	86
Ontime Input	IO4 – IO7	Pulse width of 0.2 µs – 1.678 s	87
Period Input	IO4 – IO7	Signal period of 0.2 µs – 1.678 s	87
Pulsecount Input	IO4 – IO7	0 – 65,535 input edges during 0.839 s	89
Quadrature Input	IO4 + IO5, IO6 + IO7	± 16,383 binary Gray code transitions	90
Totalcount Input	IO4 – IO7	0 – 65,535 input edges	92

Table 3.5 Summary of Timer/Counter Output Objects

I/O Object	Applicable I/O Pins	Output Signal	Page
Edgedivide Output	IO0, IO1 + (one of IO4 – IO7)	Output frequency is the input frequency divided by a user-specified number	93
Infrared Pattern Output	IO0, IO1	Series of timed repeating square wave output signals	96
Frequency Output	IO0, IO1	Square wave of 0.3 Hz to 2.5MHz	95
Oneshot Output	IO0, IO1	Pulse of duration 0.2 µs to 1.678 s	97
Pulsecount Output	IO0, IO1	0 – 65,535 pulses	98
Pulsewidth Output	IO0, IO1	0 – 100% duty cycle pulse train	99
Triac Output	IO0, IO1 + (one of IO4 – IO7)	Delay of output pulse with respect to input edge	100
Triggered-Count Output	IO0, IO1 + (one of IO4 – IO7)	Output pulse controlled by counting input edges	102

To maintain and provide consistent behavior for external events and to prevent metastability, all 12 I/O pins of the PL Smart Transceiver, when configured as inputs, are passed through a hardware synchronization block sampled by the internal system clock. This is always the input clock divided by two (e.g. 10MHz ÷ 2 = 5MHz). For any signal to be reliably synchronized with a 10MHz input clock, it must be at least 220ns in duration (see Figure 3.2).

All inputs are software sampled during `when` statement processing. The latency in sampling is dependent on the I/O object which is being executed (see I/O timing specification and the *Neuron C Programmer's Guide* for more information). These latency values scale inversely with the input clock. Thus, any event that lasts longer than 220ns will be synchronized by hardware, but there will be latency in software sampling resulting in a delay detecting the event. If the state changes at a faster rate than software sampling can occur, then the interim changes will go undetected.

There are three exceptions to the synchronization block. First, the chip select (CS~) input used in the slave B mode of the parallel I/O object; this input will recognize rising edges asynchronously. Second, the **leveldetect** input is latched by a flip-flop with a 200ns clock. The level detect transition event will be latched, but there will be a delay in software detection. Third, the SCI (UART) and SPI objects are buffered on byte boundaries by the hardware and are transferred to memory using an interrupt mechanism. The input timer/counter functions are also different, in that events on the I/O pins will be accurately measured and a value returned to a register, regardless of the state of the application processor. However, the application processor can be delayed in reading the register. Consult the *Neuron C Programmer's Guide* for detailed programming information.

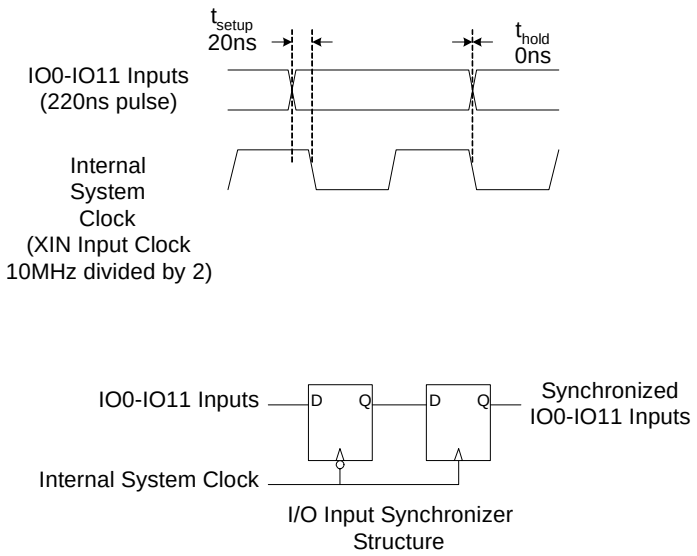


Figure 3.2 Synchronization of External Signals

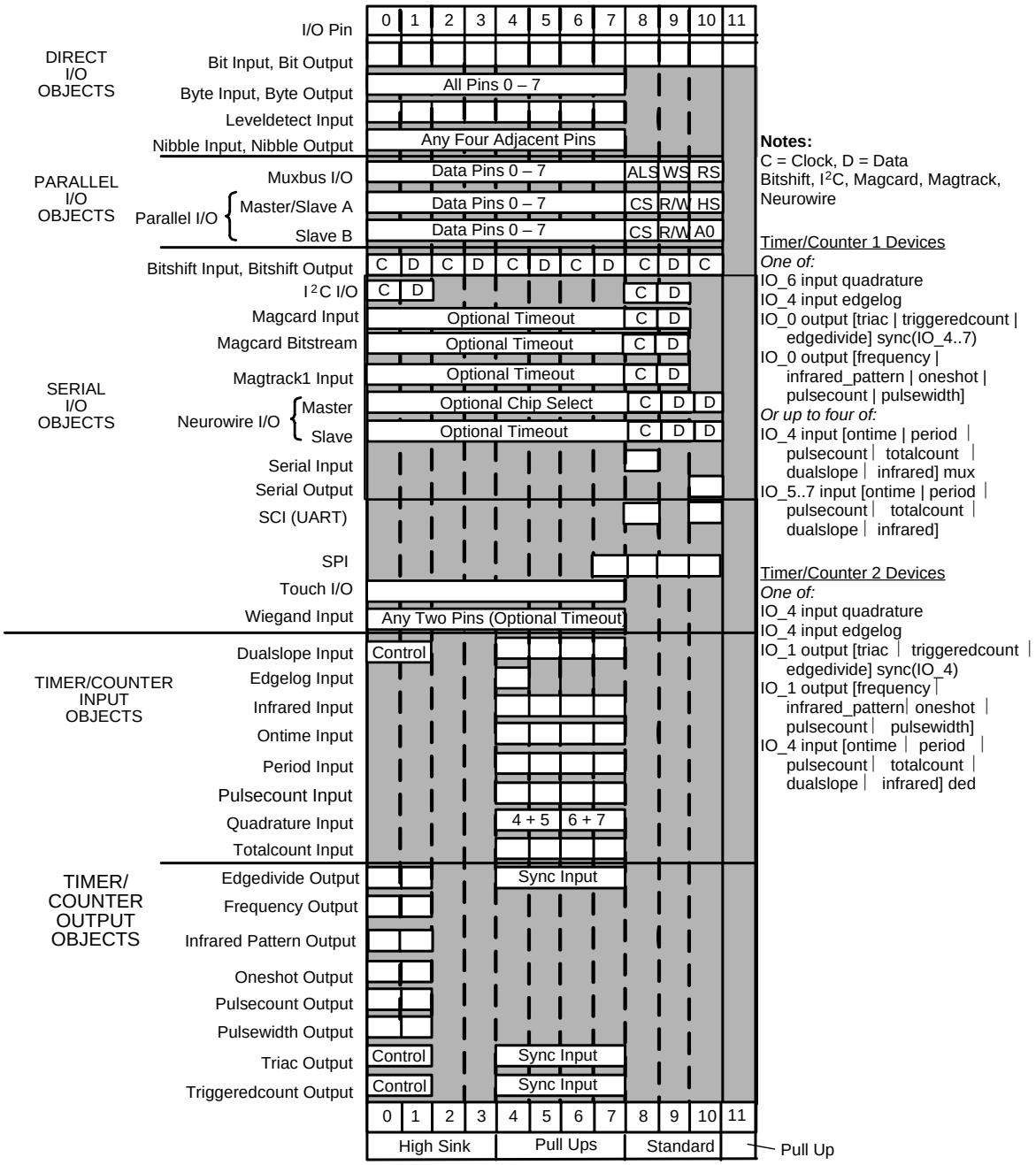


Figure 3.3 Summary of I/O Objects

I/O Timing Issues

The PL Smart Transceiver I/O timing is influenced by four separate, yet overlapping areas of the overall chip architecture:

- The scheduler
- The I/O object's firmware
- The PL Smart Transceiver hardware
- Interrupts

The contribution of the scheduler to the overall timing characteristic is approximately uniform across all I/O function blocks because its contribution to the overall I/O timing is at a relatively high functional level.

The contribution of firmware and hardware varies from one I/O object to another (for example, Bit I/O versus Neurowire I/O).

The contribution of interrupts varies with the nature of the data interrupting the processor. See the SCI (UART) and SPI section for details.

Scheduler-Related I/O Timing Information

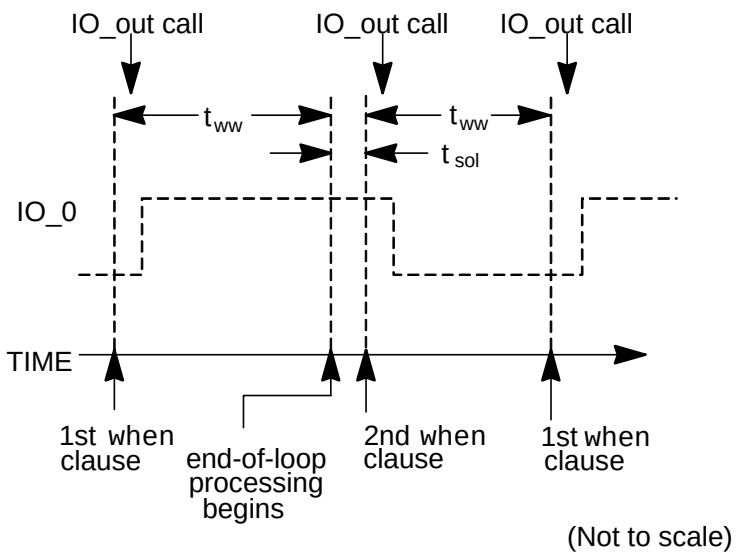
As part of the PL Smart Transceiver firmware, the scheduler provides an orderly and predictable means to facilitate the evaluation of user-defined events. The **`when`** clause, provided by the Neuron C language, is used to specify such events. For more information on the operation of the scheduler, refer to the *Neuron C Programmer's Guide.*

There is a finite latency associated with the operation of the scheduler. The time required for the scheduler to evaluate the same `when` clause in a particular user application code is, to a large extent, a function of the size of the user code, the total number of `when` clauses, and the state of the events associated with those `when` clauses. Therefore, it is impossible to specify a nominal value for this latency, as each application will have its own distinct behavior under different circumstances.

The best case latency can be viewed in several ways, each exposing a different aspect of the scheduler operation. A simple example consists of having an application program consisting of two `when` clauses, both of which always evaluate to TRUE, as shown below.

```
IO_0 output bit testbit;
when (TRUE) {
   io_out(testbit, 1);
}
when (TRUE) {
   io_out (testbit, 0);
}
```

Processing of `when` clauses is done in a round-robin fashion; therefore, the Neuron C code above performs alternating activation of the IO0 pin in order to isolate and extract the timing parameters associated with the scheduler. The waveform seen on pin IO0 of the PL Smart Transceiver, as a result of the above code, is shown in Figure 3.4.



Symbol	Description	Typ @ 10MHz
t_{ww}	`when`-clause to `when`-clause latency	940 µs
t_{sol}	Scheduler overhead latency (see text)	54 µs

Figure 3.4 `when`-Clause to `when`-Clause and Scheduler Overhead Latency

The `when`-clause to `when`-clause latency, t_{ww}, in this case includes the execution time of one `io_out()` function (65 µs latency at 10MHz) and is for an event that always evaluates to TRUE. The actual t_{ww} for a given application is driven by the actual task within the `when` statement as well as the `when` event which is evaluated.

The above example not only measures the best-case minimum latency between consecutive `when` clauses (whose events evaluate to TRUE), t_{ww}, but also reveals the scheduler's end-of-loop overhead latency, t_{sol}. As shown in Figure 3.4, t_{ww} is the off-time period of the output waveform and t_{sol} is the on-time of the output waveform, minus t_{ww}. This shows that the scheduler overhead latency, or the scheduler end-of-loop latency, occurs just before the execution of the last `when` clause in the program.

The latency associated with the return from the `io_out()` function is small, relative to that of the execution of the function call itself.

Note: Some I/O objects suspend application processing until the task is complete. This is because they are firmware-driven. These are bitshift, Neurowire, parallel, software serial I/O objects, I^2C, magcard, magtrack, Touch I/O, and Wiegand. They do not suspend network communication as this is handled by the network processor and the media access processor.

Firmware and Hardware Related I/O Timing Information

All I/O updates in the PL Smart Transceiver are performed by the Neuron firmware using system image function calls.

The total latency for a given function call, from start to end, can be broken down into two separate parts. The first is due to the processing time required before the actual hardware I/O update (read or write) occurs. The second delay is associated with the time required to finish the current function call and return to the application program.

Overall accuracy is always related to the accuracy of the XIN input of the PL Smart Transceiver. Timing diagrams are provided for all non-trivial cases to clarify the parameters given.

For more information on the operation of each of the I/O objects, refer to the *Neuron C Reference Guide.*

Direct I/O Objects

The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a **`when`** clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Bit Input/Output

Pins IO0 – IO11 can be individually configured as single-bit input or output ports. Inputs can be used to sense TTL-level compatible logic signals from external logic, contact closures, and the like. Outputs can be used to drive external CMOS and TTL level compatible logic, switch transistors and very low current relays to actuate higher-current external devices such as stepper motors and lights. The high (20mA) current sink capability of pins IO0 – IO3 allows these pins to drive many I/O devices directly (refer to Figure 3.5). Figures 3.6 and 3.7 show the bit input and bit output latency times, respectively. These are the times from which `io_in()` or `io_out()` is called, until a value is returned. The direction of bit ports can be changed between input and output dynamically under application control. (`io_set_direction()`)

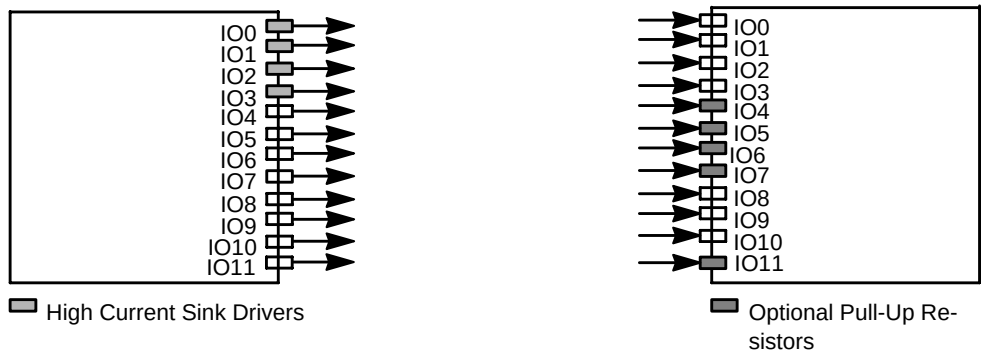
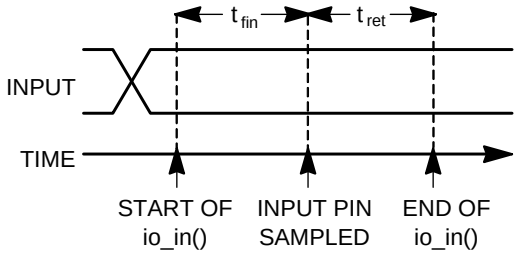


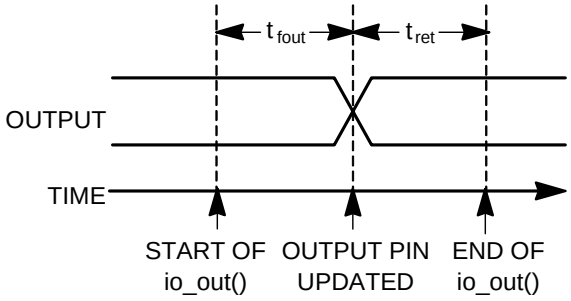
Figure 3.5 Bit I/O

***Note*:** After a reset, the PL Smart Transceiver disables the IO4-IO7 and IO11 pull-up resistors. The pull-up resistors are not turned on until application initialization. Pull-ups are only enabled when specified in the application configuration using a Neuron C directive (`#pragma enable_io_pullups`).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to sample IO0 – IO10 IO11	 41 µs 8.4µs
t_{ret}	Return from function IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7 IO8 IO9 IO10 IO11	 19 µs 23.4 µs 27.9 µs 32.3 µs 36.7 µs 41.2 µs 45.6 µs 50 µs 19 µs 23.4 µs 27.9 µs 7.8 µs

Figure 3.6 Bit Input Latency Values



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to update IO3 – IO5, IO11 All others	 69 µs 60 µs
t_{ret}	Return from function IO0 – IO11	 5 µs

Figure 3.7 Bit Output Latency Values

Byte Input/Output

Pins IO0 – IO7 can be configured as a byte-wide input or output port, which can be read or written using integers in the range 0 to 255. This is useful for driving devices that require ASCII data, or other data, eight bits at a time. For example, an alphanumeric display panel can use byte function for data, and use pins IO8 – IO11 in bit function for control and addressing. See Figures 3.8, 3.9, and 3.10. IO0 represents the LSB of data. The direction of a byte port can be changed between input and output dynamically under application control. (`io_set_direction()`)

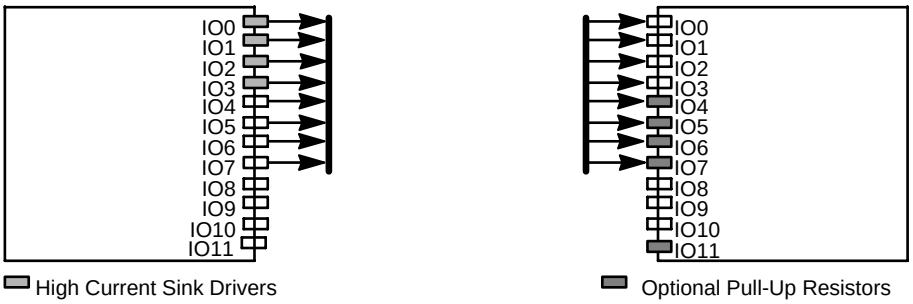
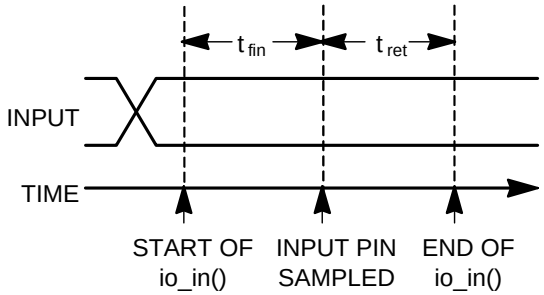
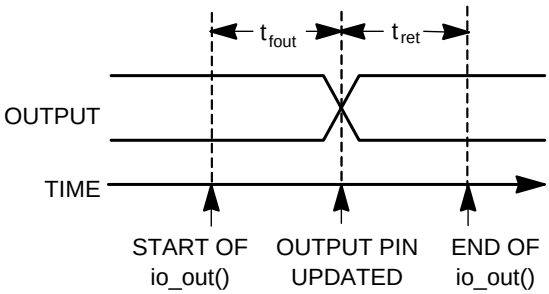


Figure 3.8 Byte I/O



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	24 µs
t_{ret}	Return from function	4 µs

Figure 3.9 Byte Input Latency Values

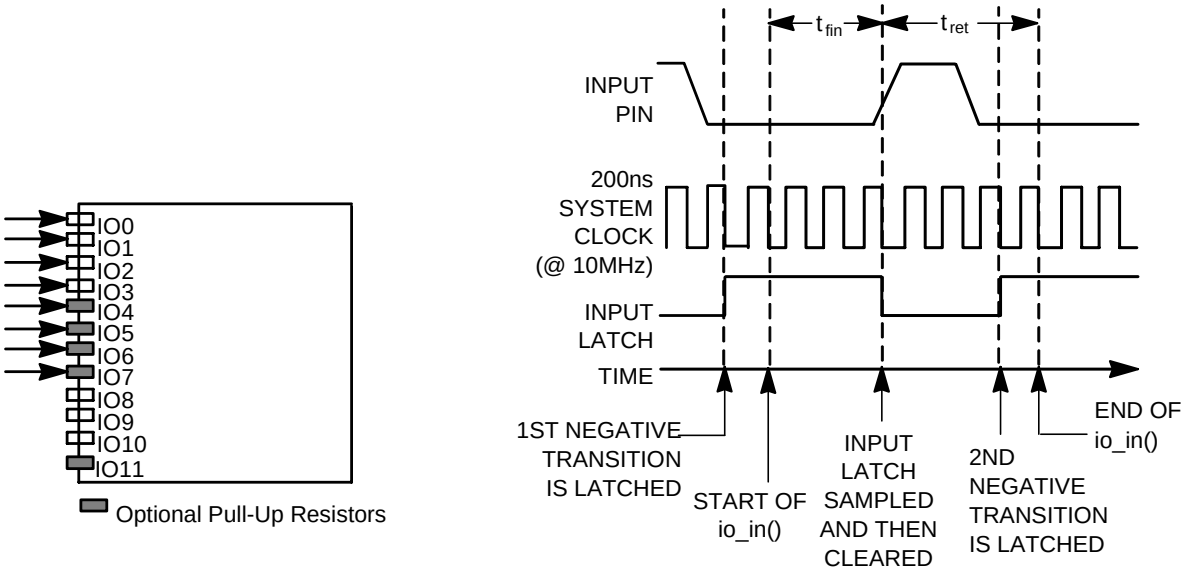


Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to update	57 µs
t_{ret}	Return from function	5 µs

Figure 3.10 Byte Output Latency Values

Leveldetect Input

Pins IO0 – IO7 can be individually configured as leveldetect input pins, which latch a negative-going transition of the input level with a minimal low pulse width of 200ns, with a PL Smart Transceiver clocked at 10MHz. The application can therefore detect short pulses on the input which might be missed by software polling. This is useful for reading devices, such as proximity sensors. **This is the only direct I/O object which is latched before it is sampled.** The latch is cleared during the `when` statement sampling and can be set again immediately after, if another transition should occur (see Figure 3.11).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to sample	
	IO0	35 µs
	IO1	39.4 µs
	IO2	43.9 µs
	IO3	48.3 µs
	IO4	52.7 µs
	IO5	57.2 µs
	IO6	61.6 µs
	IO7	66 µs
t_{ret}	Return from function	32 µs

Figure 3.11 Leveldetect Input Latency Values

Nibble Input/Output

Groups of four consecutive pins between IO0 – IO7 can be configured as nibble-wide input or output ports, which can be read or written to using integers in the range 0 to 15. This is useful for driving devices that require BCD data, or other data four bits at a time. For example, a 4x4 key switch matrix can be scanned by using one nibble to generate an output (row select — one of four rows), and one nibble to read the input from the columns of the switch matrix. See Figures 3.12, 3.13, and 3.14.

The direction of nibble ports can be changed between input and output dynamically under application control (see the *Neuron C Programmer's Guide*). The LSB of the input data is determined by the object declaration and can be any of the IO0 – IO4 pins.

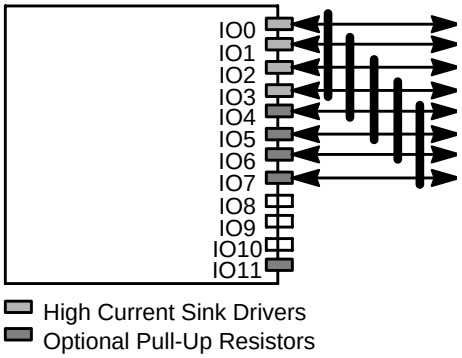
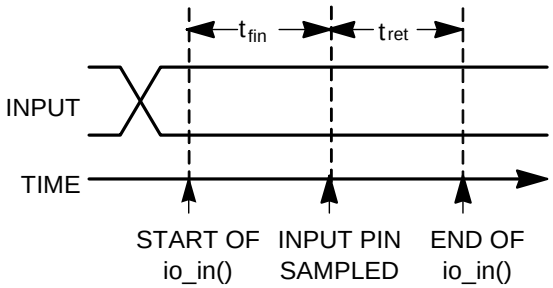
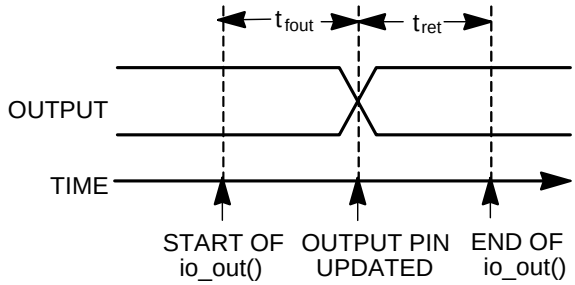


Figure 3.12 Nibble I/O



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to sample IO0 – IO4	41 µs
t_{ret}	Return from function	
	IO0	18 µs
	IO1	22.8 µs
	IO2	27.5 µs
	IO3	32.3 µs
	IO4	37 µs

Figure 3.13 Nibble Input Latency Values



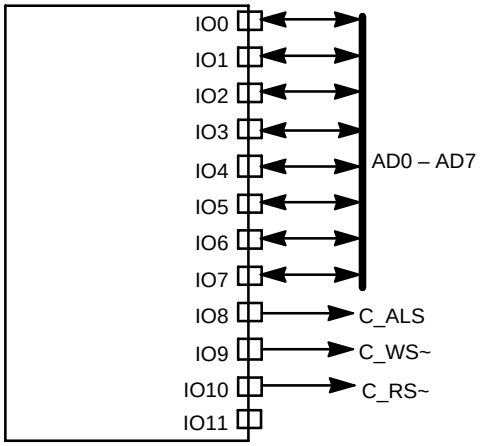
Symbol	Description	Typ @ 10MHz
t_{fout}	Function to update IO0 IO1 IO2 IO3 IO4	 78 µs 89.8 µs 101.5 µs 113.3 µs 125 µs
t_{ret}	Return from function IO0 – IO4	 5 µs

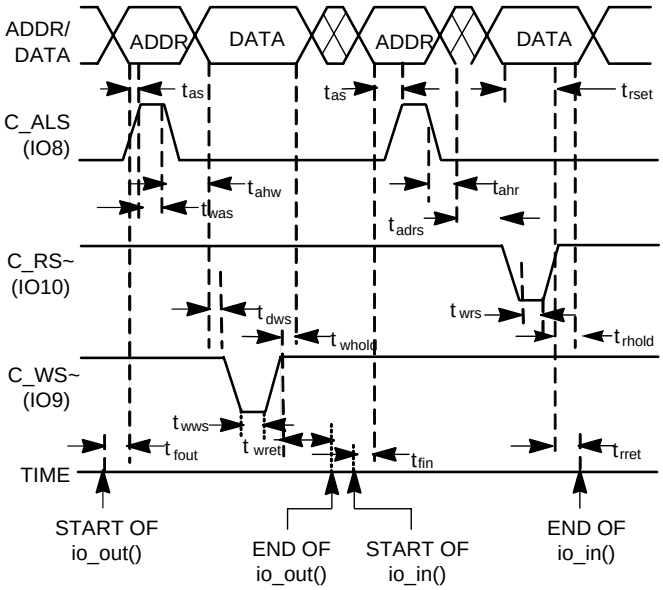
Figure 3.14 Nibble Output Latency Values

Parallel I/O Objects

Muxbus Input/Output

This I/O object provides a means of performing parallel I/O data transfers between the PL Smart Transceiver and an attached peripheral device or processor (see Figure 3.15). Unlike the parallel input/output object, which makes use of a token-passing scheme for ensuring synchronization, the muxbus input/output enables the PL Smart Transceiver to essentially be in control of all read and write operations at all times. This relieves the burden of protocol handling from the attached device and results in an easier-to-use interface at the expense of data throughput capacity. The data bus remains in the last state used.





NOTE: Data is latched 4.8 µs after the falling edge of C_RS~.

Symbol	Description	Min	Typ	Max
t_{fout}	`io_out()` to valid address	—	26.4 µs	—
t_{as}	Address valid to address strobe	—	10.8 µs	—
t_{ahw}	Address hold for write	—	4.8 µs	—
t_{ahr}	Address hold for read	—	6.6 µs	—
t_{was}	Address strobe width	—	6.6 µs	—
t_{wrs}	Read strobe width	—	10.8 µs	—
t_{wws}	Write strobe width	—	10.8 µs	—
t_{dws}	Data valid to write strobe	—	6.6 µs	—
t_{rset}	Read setup time	10.8 µs	—	—
t_{whold}	Write hold time	4.2 µs	—	—
t_{rhold}	Read hold time	0 µs	—	—
t_{adrs}	Address disable to read strobe	—	7.2 µs	—
t_{fin}	`io_in()` to valid address	—	26.4 µs	—
t_{rret}	Function return from read	—	4.2 µs	—
t_{wret}	Function return from write	—	4.2 µs	—

Figure 3.15 Muxbus I/O Object

Parallel Input/Output

Pins IO0 – IO10 can be configured as a bidirectional 8-bit data and 3-bit control port for connecting to an external processor. The other processor can be a computer, microcontroller, or another PL Smart Transceiver (for gateway applications). The parallel interface can be configured in master, slave A, or slave B mode. Typically, two PL Smart Transceivers interface in master/slave A mode and a PL Smart Transceiver interfaces with another microprocessor in the slave B configuration, with the other microprocessor as the master. Handshaking is used in both modes to control the instruction execution, and application processing is suspended for the duration of the transfer (up to 255 bytes/transfer). Consult the *Neuron C Reference Guide* for detailed programming instructions.

Upon a reset condition, the master processor monitors the low transition of the handshake (HS) line from the slave, then passes a CMD_RESYNC (0x5A) for synchronization purposes. This must be done within 0.84 seconds after reset goes high with a PL Smart Transceiver slave running at 10MHz, to avoid a watchdog reset error condition (see the *Neuron C Programmer's Guide*). The CMD_RESYNC is followed by the slave acknowledging with a CMD_ACKSYNC (0x07). This synchronization ensures that both processors are properly reset before data transfer occurs. When interfacing two PL Smart Transceivers, these characters are passed automatically (refer to the flow table illustrated later in this section). However, when using parallel I/O to interface the PL Smart Transceiver to another microprocessor, that microprocessor must duplicate the interface signals and characters that are automatically generated by the parallel I/O function of the PL Smart Transceiver.

For additional information, see the *Parallel I/O Interface to the Neuron Chip* engineering bulletin.

The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a `when` clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Master/Slave A Mode

This mode is recommended when interfacing two PL Smart Transceivers. In a master/slave A configuration, the master drives IO8 as a chip select and IO9 to specify a read or write cycle, and the slave drives IO10 as a handshake (HS) acknowledgment (see Figure 3.16). The maximum data transfer rate is 1 byte per 4 processor instruction cycles, or 2.4 µs per byte at a 10MHz input clock rate. The data transfer rate scales proportionally to the input clock rate (a master write is a slave read). Timing for the case where the PL Smart Transceiver is the master (Figure 3.17), refers to measured output timing at 10MHz. After every byte write or byte read, the HS line is monitored by the master, to verify the slave has completed processing (when HS = 0) and the slave is ready for the next byte transfer. This is done automatically in PL Smart Transceiver-to-PL Smart Transceiver (master/slave A mode) data transfers. **The HS line should be pulled up (inactive) with a 10kΩ resistor to ensure proper resynch behavior after the slave resets.** Slave A timing is shown in Figure 3.18.

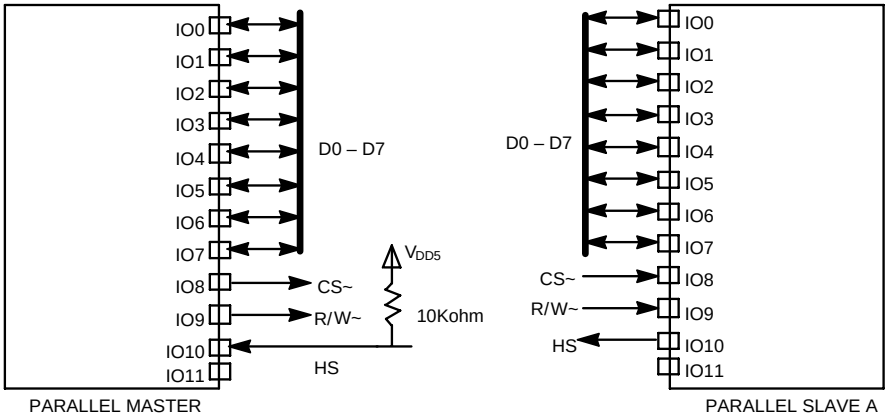
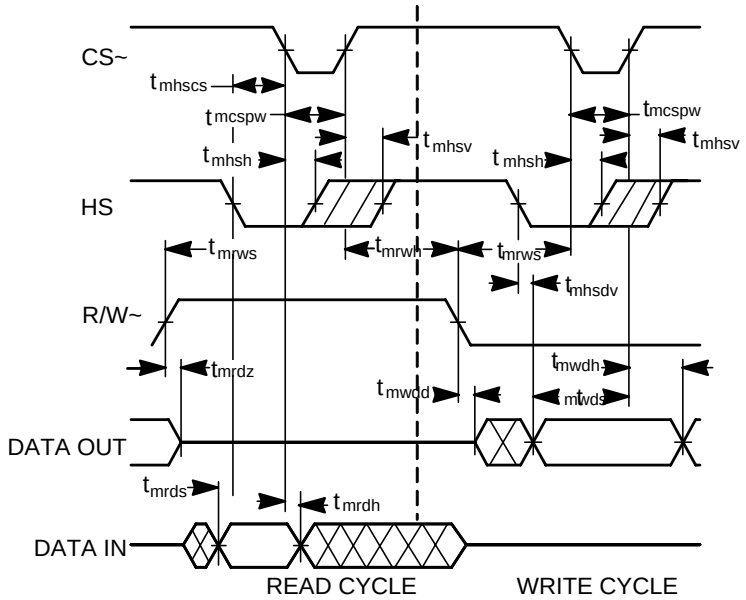


Figure 3.16 Parallel I/O — Master and Slave A

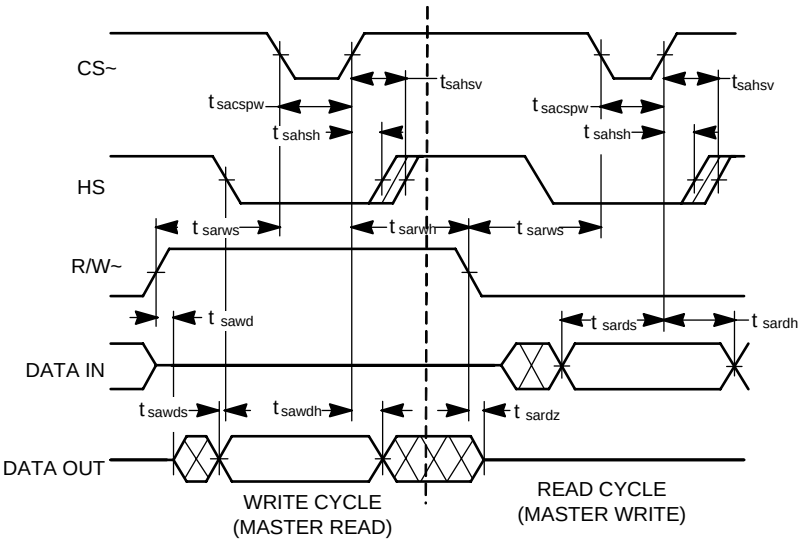


Symbol	Description	Min	Typ	Max
t_{mrws}	R/W~ setup before falling edge of CS~ (Note 6)	150 ns	3 XIN	—
t_{mrwh}	R/W~ hold after rising edge of CS~	100 ns	—	—
t_{mcspw}	CS~ pulse width (Note 6)	150 ns	2 XIN	—
t_{mhsh}	HS hold after falling edge of CS~	0 ns	—	—
t_{mhsv}	HS checked by firmware after rising edge of CS~ (Note 6)	150 ns	10 XIN	—
t_{mrdz}	Master three-state DATA after rising edge of R/W~ (Notes 1, 2)	—	0	25 ns
t_{mrds}	Read data setup before falling edge of HS (Note 3)	0 ns	—	—
t_{mhscs}	HS low to falling edge of CS~ (Notes 4,6)	2 XIN	6 XIN	—
t_{mrdh}	Read data hold after falling edge of CS~	0 ns	—	—
t_{mwdd}	Master drive of DATA after falling edge of R/W~ (Notes 1,6)	150 ns	2 XIN	—
t_{mhsdv}	HS low to data valid (Note 4)	—	50 ns	—
t_{mwds}	Write data setup before rising edge of CS~ (Note 6)	150 ns	2 XIN	—
t_{mwdh}	Write data hold after rising edge of CS~ (Note 5)	Note 5	—	—

Figure 3.17 Master Mode Timing

Notes:

1. Refer to the *PL 3120/PL 3150 or PL 3170 Smart Transceiver Datasheets* for detailed measurement information.
2. For PL Smart Transceiver-to-PL Smart Transceiver operation, bus contention (t_{mrdz}, t_{sawdd}) is eliminated by firmware, ensuring that a zero state is present when the token is passed between the master and slave. See *Parallel I/O Interface to the Neuron Chip* engineering bulletin for further information.
3. HS high is used as a slave busy flag. If HS is held low, the maximum data transfer rate is 24 XIN (2.4µs @ 10MHz) per byte. If HS is not used for a flag, caution should be taken to ensure the master does not initiate a data transfer before the slave is ready.
4. Parameters were added in order to aid interface design with the PL Smart Transceiver.
5. Master will hold output data valid during a write until the Slave device pulls HS high.
6. XIN represents the period of the PL Smart Transceiver input clock (100ns at 10MHz).
7. In a master read, CS~ pulsing low acts like a handshake to flag the slave that data has been latched in.



Symbol	Description	Min	Typ	Max
t_{sarws}	R/W~ setup before falling edge of CS~	25 ns	—	—
t_{sarwh}	R/W~ hold after rising edge of CS~	0 ns	—	—
t_{sacspw}	CS~ pulse width	45 ns	—	—
t_{sahsh}	HS hold after rising edge of CS~	0 ns	—	—
t_{sahsv}	HS valid after rising edge of CS~	—	—	50 ns
t_{sawdd}	Slave A drive of DATA after rising edge of R/W~ (Notes 1, 2)	0 ns	5 ns	—
t_{sawds}	Write data valid before falling edge of HS (Note 4)	150 ns	2 XIN	—
t_{sawdh}	Write data valid after rising edge of CS~ (Note 4)	150 ns (Note 3)	2 XIN	—
t_{sardz}	Slave A three-state DATA after falling edge of R/W~ (Note 1)	—	—	50 ns
t_{sards}	Read data setup before rising edge of CS~	25 ns	—	—
t_{sardh}	Read data hold after rising edge of CS~	10 ns	—	—

Figure 3.18 Slave A Mode Timing

Notes:
1. Refer to the *PL 3120/PL 3150 or PL 3170 Smart Transceiver Datasheets* for detailed measurement information.
2. For PL Smart Transceiver-to-PL Smart Transceiver operation, bus contention (t_{mrdz}, t_{sawdd}) is eliminated by firmware, ensuring that a zero state is present when the token is passed between the master and slave. See *Parallel I/O Interface to the Neuron Chip* engineering bulletin for further information.
3. If $t_{sarwh} < 150$ns, then $t_{sawdh} = t_{sarwh}$.
4. XIN represents the period of the PL Smart Transceiver input clock (100ns at 10MHz).
5. In slave A mode, the HS signal is high a minimum of 4 XIN periods. The typical time HS is high during consecutive data reads or consecutive data writes is also 4 XIN periods.

Slave B Mode

The slave B mode is recommended for interfacing a PL Smart Transceiver acting as the slave to another microprocessor acting as the master. When configured in slave B mode, the PL Smart Transceiver accepts IO8 as a chip select and IO9 to specify whether the master will read or write, and accepts IO10 as a register select input. When CS~ is asserted and either IO10 is low or IO10 is high and R/W~ is low, pins IO0 – IO7 form the bidirectional data bus. When IO10 is high, R/W~ is high, and CS~ is asserted, IO0 is driven as the HS acknowledgment signal to the master.

The PL Smart Transceiver can appear as two registers in the master's address space; one of the registers being the read/write data register, and the other being the read-only status register. Therefore, reads by the master to an odd address access the status register for handshaking acknowledgments and all other reads or writes access the data register for I/O transfers. The LSB of the control register, which is read through pin IO0, is the HS bit. The master reads the HS bit after every master read or write. **The D0/HS line should be pulled up (inactive) with a 10kΩ resistor to ensure proper resynch behavior after resets.**

When acting as a slave to a different microprocessor, the PL Smart Transceiver slave B mode handles all handshaking and token passing automatically. However, the master microprocessor must read the HS bit after each transaction and must also internally track the token passing. This mode is designed for use with a master processor that uses memory-mapped I/O, as the LSB of the master's address bus is typically connected to the IO10 pin of the PL Smart Transceiver. This is illustrated in Figures 3.19 and 3.20.

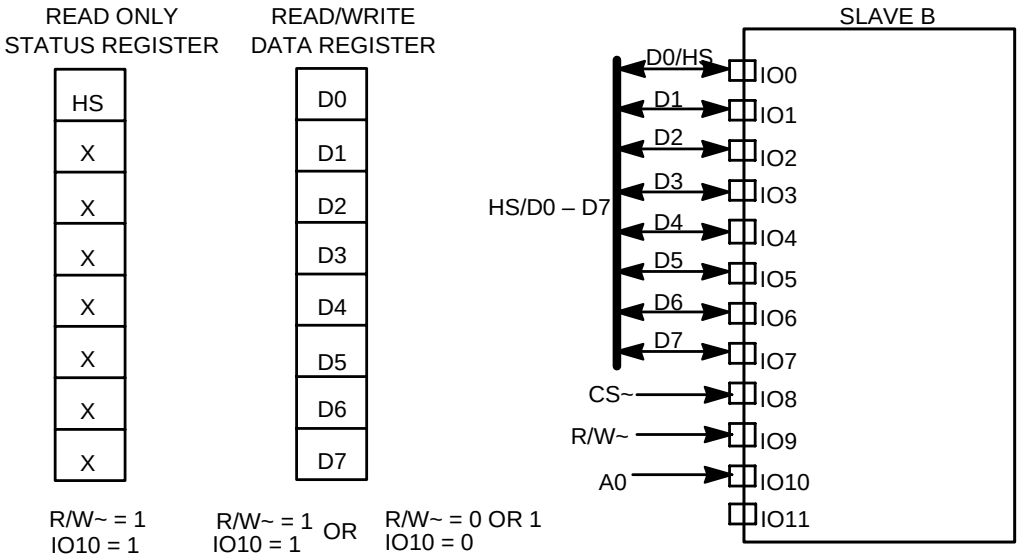
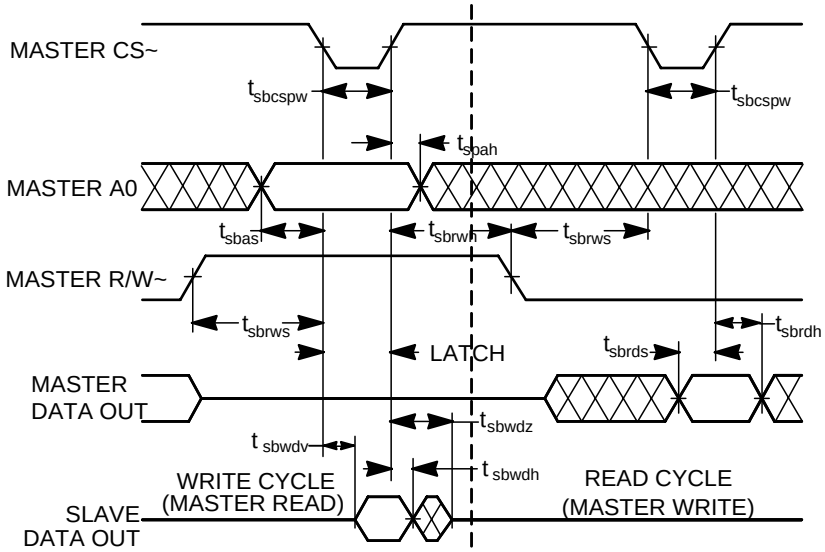


Figure 3.19 Parallel I/O Master/Slave B (PL Smart Transceiver as Memory-Mapped I/O Device)



Symbol	Description	Min	Typ	Max
t_{sbrws}	R/W~ setup before falling edge of CS~ PL 3120, PL 3150, and PL 3170 Smart Transceivers	0 ns	—	—
t_{sbrwh}	R/W~ hold after rising edge of CS~	0 ns	—	—
t_{sbcspw}	CS~ pulse width	Note 1	—	—
t_{sbas}	A0 setup to falling edge of CS~	10 ns	—	—
t_{sbah}	A0 hold after rising edge of CS~	0 ns	—	—
t_{sbwdv}	CS~ to write data valid	—	—	50 ns
t_{sbwdh}	Write data hold after rising edge of CS~ (Notes 2, 3)	0 ns	30 ns	—
t_{sbwdz}	CS~ rising edge to Slave B release data bus (Note 2)	—	—	50 ns
t_{sbrds}	Read data setup before rising edge of CS~	25 ns	—	—
t_{sbrdh}	Read data hold after rising edge of CS~	10 ns	—	—

Figure 3.20 Slave B Mode Timing

Notes:
1. The slave B write cycle (master read) CS~ pulse width is directly related to the slave B write data valid parameter and master read setup parameter. To calculate the write cycle CS~ duration needed for a special application use:
   $t_{sbcspw} = t_{sbwdv}$ + master's read data setup before rising edge of CS~. Refer to the master's specification data book for the master read setup parameter. The slave read cycle minimum CS~ pulse width = 50 ns.
2. Refer to the *PL 3120/PL 3150 or PL 3170 Smart Transceiver Datasheets* for detailed measurement information.
3. The data hold parameter, t_{sbwdh}, is measured to the disable levels shown in the *PL 3120/PL 3150 or PL 3170 Smart Transceiver Datasheets*, rather than to the traditional data invalid levels.
4. In a slave B write cycle, the timing parameters are the same for a control register (HS) write as for a data write.
5. Special applications: Both the state of CS~ and R/W~ determine a slave B write cycle. If CS~ cannot be used for a data transfer, then toggling the R/W~ line can be used with no changes to the hardware. In other words, if CS~ is held low during a slave B write cycle, a positive pulse (low to high to low) on R/W~ can execute a data transfer. The low to high transition on R/W~ causes slave B to drive data with the same timing parameters as t_{sbwdv} (redefined R/W~ to write data valid). Likewise, the falling edge of R/W~ causes slave B to release the data bus with the same timing limits as the CS~ rising edge in t_{sbwdz}. This scenario is only true for a slave B write cycle and is not applicable to a slave B read cycle or any slave A data transitions. This application can be helpful if the master has separate read and write signals but no CS~ signal. Caution must be taken to ensure the bus is free before transfers to avoid bus contention.

Serial I/O Objects

The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a **when** clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Bitshift Input/Output

Pairs of adjacent pins can be configured as serial input or output lines. The first pin of the pair can be IO0-IO6, IO8, or IO9, and is used for the clock (driven by the PL Smart Transceiver). The adjacent higher-numbered I/O pin is then used for up to 16 bits of serial data. The bit rate can be configured as 1kbps, 10kbps, or 15kbps at a 10MHz input clock rate. The bit rate scales proportionally to the input clock rate. The active clock edge can be specified as either rising or falling. This object is useful for transferring data to external logic employing shift registers. This function suspends application processing until the operation is complete (see Figures 3.21, 3.22, and 3.23).

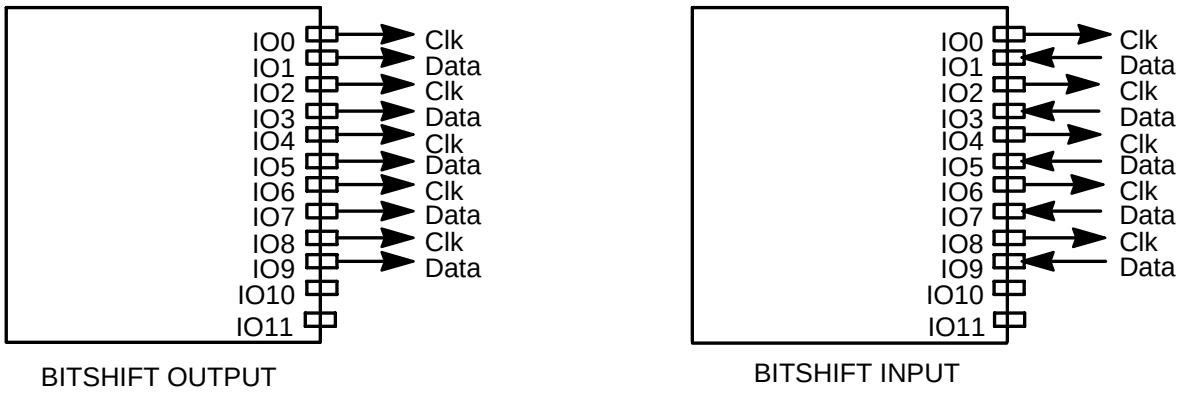
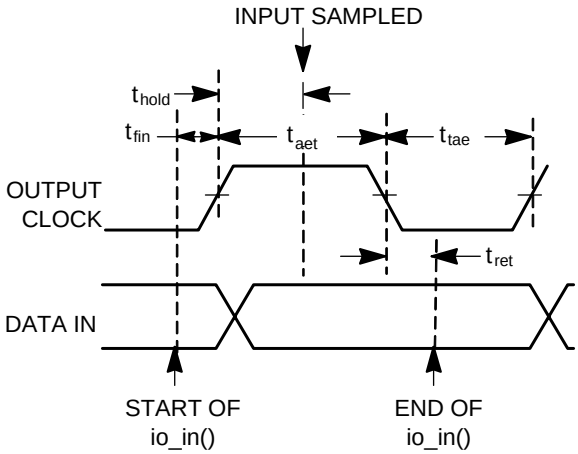


Figure 3.21 Bitshift I/O Examples

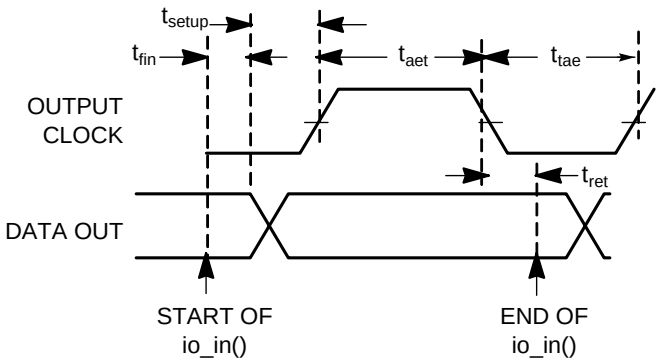
For bitshift input, the clock output is deasserted (to the inactive level) at the same time as the start of the first bit of data. For bitshift output, the clock output is initially inactive prior to the first bit of data (unless overridden by a bit output overlay).



Active clock edge assumed to be positive in the above diagram.

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to first edge	156.6 µs
t_{ret}	Return from function	5.4 µs
t_{hold}	Active clock edge to sampling of input data 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 9 µs 40.8 µs 938.2 µs
t_{aet}	Active clock edge to next clock transition 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 31.8 µs 63.6 µs 961 µs
t_{tae}	Clock transition to next active clock edge 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 14.4 µs 14.4 µs 14.4 µs
f	Clock frequency = $1/(t_{aet} + t_{tae})$ 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 21.6 kHz 12.8 kHz 1.03 kHz

Figure 3.22 Bitshift Input Latency Values



Active clock edge assumed to be positive in the above diagram.

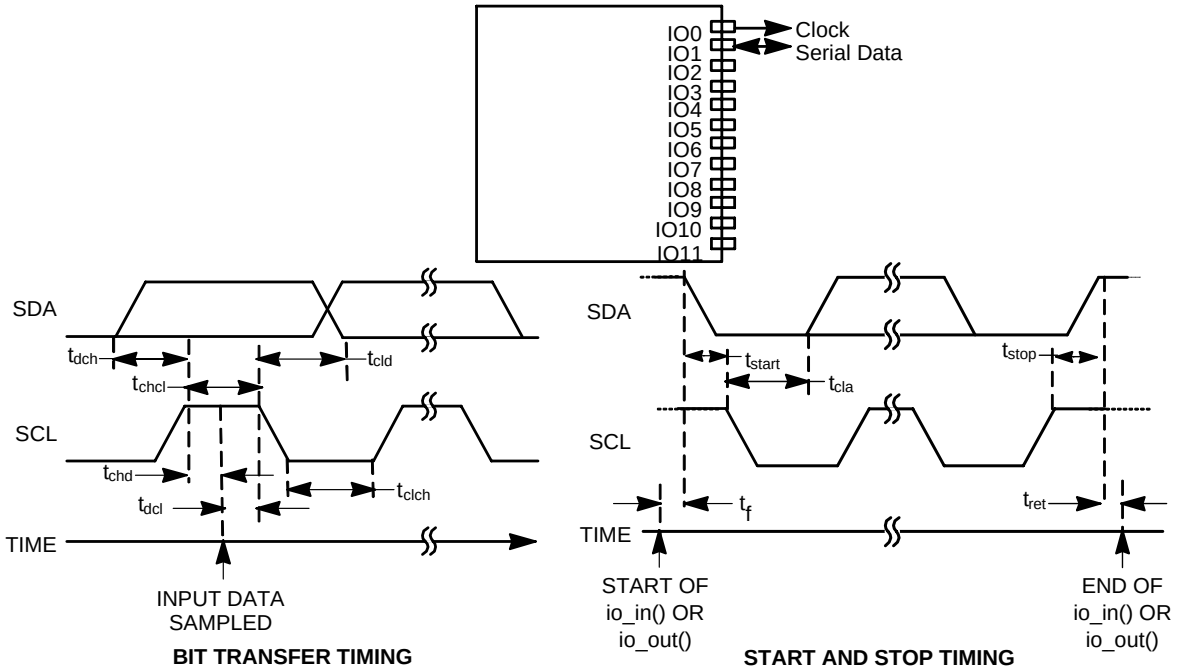
Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to first data out stable 16-bit shift count 1-bit shift count	 185.3 µs 337.6 µs
t_{ret}	Return from function	10.8 µs
t_{setup}	Data out stable to active clock edge 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 10.8 µs 10.8 µs 10.8 µs
t_{aet}	Active clock edge to next clock transition 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 10.2 µs 42 µs 939.5 µs
t_{tae}	Clock transition to next active clock edge 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 34.8 µs 34.8 µs 34.8 µs
f	Clock frequency = $1/(t_{aet} + t_{tae})$ 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 22 kHz 13 kHz 1.02 kHz

Figure 3.23 Bitshift Output Latency Values

I²C Input/Output

This I/O object is used to interface the PL Smart Transceiver to any device which adheres to Philips Semiconductor's Inter-Integrated Circuit (I^2C) bus protocol. The PL Smart Transceiver is always the master, with IO8 being the serial clock (SCL) and IO9 the serial data (SDA). Alternatively, IO0 can be used as the serial clock (SCL) and IO1 as the serial data (SDA). These I/O lines are operated in the open-drain mode in order to accommodate the special requirements of the I^2C protocol. With the exception of two pull-up resistors, no additional external components are necessary for interfacing the PL Smart Transceiver to an I^2C device. Up to 255 bytes of data can be transferred at a time.

At the start of all transfers, a right-justified 7-bit I²C address argument is sent out on the bus immediately after the I²C "start condition." For more information on this protocol, refer to Philips Semiconductor's I²C documentation.



Parameter	Description	Min	Typ	Max

t_f	I/O call to start condition
	`io_in()`
	`io_out()`
		
		—
		—
			
			54.6 µs
			43.4 µs
				
				—
				—

t_{start}	End of start condition
	`io_in()`
	`io_out()`
		
		5.4 µs
		5.4 µs
			
			—
			—
				
				—
				—

t_{cla}	End of start to start of address
	`io_in()`
	`io_out()`
		
		24.0 µs
		24.0 µs
			
			—
			—
				
				—
				—

t_{cld}	SCL low to data for `io_out()`	24.6 µs	—	—
t_{dch}	Data to SCL high for `io_out()`	7.2 µs	—	—
t_{chcl}	Clock high to clock low for `io_out()`	12.6 µs	—	—
t_{chd}	SCL high to data sampling for `io_in()`	13.2 µs	—	—
t_{dcl}	Data sample to SCL low for `io_in()`	7.2 µs	—	—
t_{clch}	Clock low to clock high for `io_in()`	24.0 µs	—	—

t_{stop}	Clock high to data
	`io_in()`
	`io_out()`
		
		12.6 µs
		12.6 µs
			
			—
			—
				
				—
				—

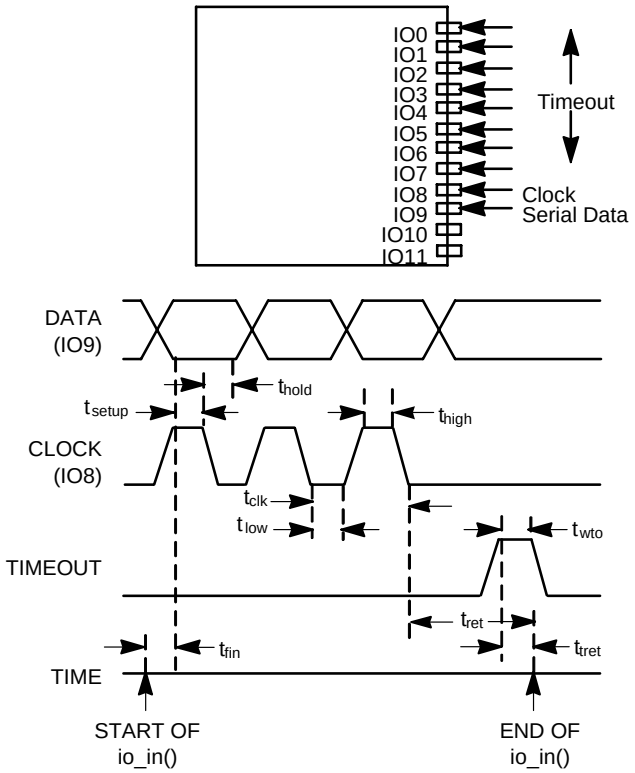
T_{ret}	SDA high to return from function
	`io_in()`
	`io_out()`
		
		—
		—
			
			—
			—
				
				4.2 µs
				4.2 µs

Figure 3.24 I²C I/O Object

Magcard Input

This I/O object is used to transfer synchronous serial data from an ISO 7811 Track 2 magnetic stripe card reader in real time. The data is presented as a data signal input on pin IO9, and a clock, or a data strobe, signal input on pin IO8. The data on pin IO9 is clocked on or just following the falling (negative) edge of the clock signal on IO8, with the LSB first. In addition, any one of the pins IO0 – IO7 can be used as a timeout pin to prevent lockup in case of abnormal abort of the input bit stream during the input process.

Up to 40 characters can be read at one time. Both the parity and the Longitudinal Redundancy Check (LRC) are checked by the PL Smart Transceiver.



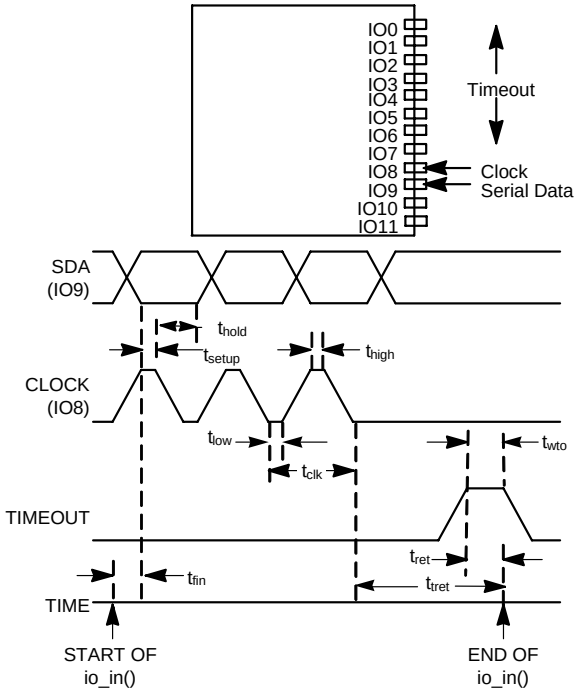
Symbol	Description	Min	Typ	Max
t_{fin}	Function call to first clock input	—	45.0 µs	—
t_{hold}	Data hold	0 µs	—	—
t_{setup}	Data setup	0 µs	—	—
t_{low}	Clock low width	60 µs	—	—
t_{high}	Clock high width	60 µs	—	—
t_{wto}	Width of timeout pulse	60 µs	—	—
t_{clk}	Clock period	120 µs	—	—
t_{tret}	Return from timeout	21.6 µs	—	81.6 µs
t_{ret}	Return from function	—	—	301.8 µs

Figure 3.25 Magcard Input Object

A PL Smart Transceiver operating at 10MHz can process a bit rate at up to 8334 bits/second (of a bit density of 75 bits/inch). This equates to a card velocity of 111 inches/second. Most magnetic card stripes contain a 15-bit sequence of zero data at the start of the card, allowing time for the application to start the card reading function. At 8334 bits/second, this period is about 1.8ms. If the scheduler latency is greater than the 1.8ms value, the `io_in( )` function will miss the front end of the data stream. The bit rate processing capability scales with input clock rate.

Magtrack1 Input

This input object type is used to read synchronous serial data from an ISO3554 magnetic stripe card reader. The data input is on pin IO9, and the clock, or data strobe, is presented as input on pin IO8. The data on pin IO9 is clocked in just following the falling edge of the clock signal on IO7, with the LSB first.



Symbol	Description	Min	Typ	Max
t_{fin}	Function call to first clock input	—	45.0 µs	—
t_{hold}	Data hold	t_{low}	—	t_{clk}
t_{setup}	Data setup	0 µs	—	—
t_{low}	Clock low width	31 µs	—	—
t_{high}	Clock high width	31 µs	—	—
t_{wto}	Width of timeout pulse	60 µs	—	—
t_{clk}	Clock period	138 µs	—	—
t_{tret}	Return from timeout	21.6 µs	—	81.6 µs
t_{ret}	Return from function	—	—	301.8 µs

Figure 3.26 Magtrack1 Input Object

The minimum period for the entire bit cycle (t_{clk}) is greater than the sum of t_{low} and t_{high}. The t_{setup} and t_{hold} times should be such that the data is stable for the duration of t_{low}.

Data are recognized in the IATA format as a series of 6-bit characters plus an even parity bit per character. The process begins when the start sentinel (hex 05) is recognized, and continues until the end sentinel (0x0F) is recognized. No more than 79 characters, including the 2 sentinels and the LRC character, will be read. The data is stored as right-justified bytes in the buffer space pointed to by the buffer pointer argument in the `io_in()` function with the parity stripped, and includes the start and end sentinels. This buffer should be 78 bytes long.

The magtrack1 input object optionally uses one of the I/O pins IO0 – IO7 as a timeout/abort pin. Use of this feature is suggested because the `io_in()` function will update the watchdog timer during clock wait states, and could result in a lockup if the card were to stop moving in the middle of the transfer process. If a logic 1 level is detected on the I/O timeout pin, the `io_in()` function will abort. This input can be a oneshot timer counter output, an R/C circuit, or a DATA_VALID~ signal from the card reader.

A PL Smart Transceiver with a clock rate of 10MHz can process an incoming bit rate of up to 7246 bits/second when the strobe signal has a 1/3 duty cycle (t_{high} = 46µs, t_{low} = 92µs). At a bit density of 210 bits/inch, this translates to a card speed of 34.5 inches/second. The bit rate processing capability scales with PL Smart Transceiver input clock rate.

Magcard Bitstream Input

A **magcard_bitstream** I/O object provides the ability to read unprocessed serial data streams from most magnetic stripe card readers in real time. This function can be used to read magnetic card data in either direction, forward or reverse, because the data does not need to follow any specific format.

This I/O object can read up to 65,535 bits of data, stored in 8192 bytes of data, from a magnetic stripe card reader.

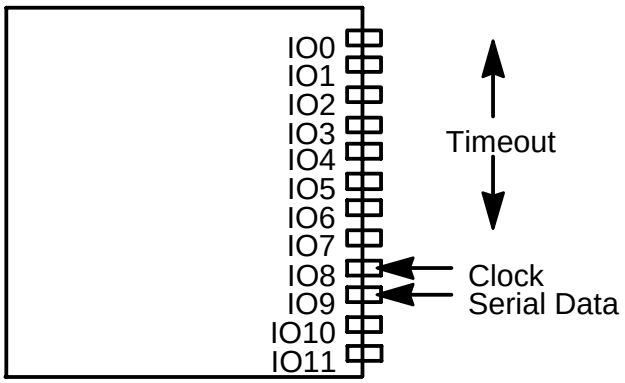


Figure 3.27 Magcard Bitstream Input

Neurowire Input/Output Object

The Neurowire object implements a full-duplex synchronous transfer of data to some peripheral device. It can operate as the master (drive a clock out) or as the slave (accept a clock in). In both master and slave modes, up to 255 bits of data can be transferred at a time. The Neurowire I/O suspends application processing until the operation is completed. The Neurowire object is useful for external devices, such as A/D, D/A converters, and display drivers incorporating serial interfaces that conform with Motorola's SPI or National Semiconductor MICROWIRE™ interface.

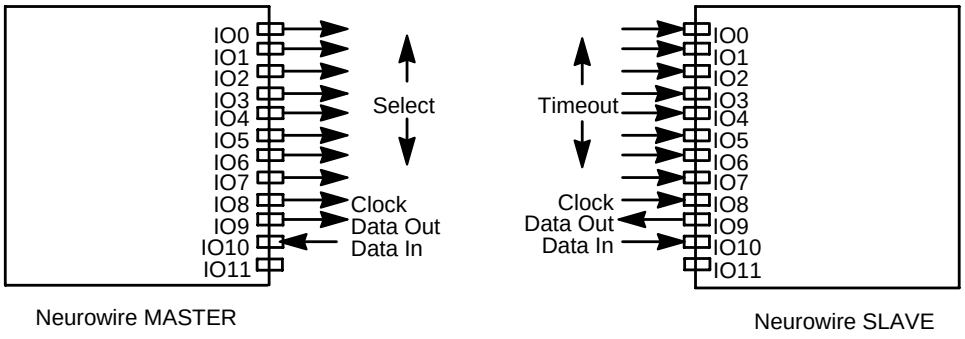
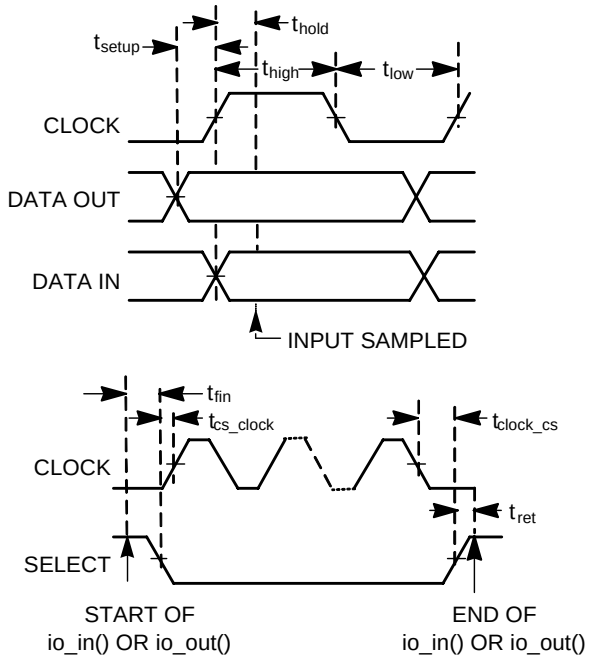


Figure 3.28 Neurowire Input/Output

Neurowire Master Mode

The Neurowire master mode I/O object is still provided for legacy support. Echelon recommends using the hardware SPI instead of the legacy software I/O object (See the *SPI Input/Output* section later in this manual). The hardware SPI provides much higher performance with lower software overhead.

In Neurowire master mode, pin IO8 is the clock (driven by the PL Smart Transceiver), IO9 is the serial data output, and IO10 is the serial data input. Serial data is clocked out on pin IO9 at the same time as data is clocked in from pin IO10. Data is clocked by the rising edge of the clock signal by default. The *clockedge* keyword changes the active edge of the clock to negative. In addition, one or more of the IO0 – IO7 pins can be used as a chip select, allowing multiple Neurowire devices to be connected on a three-wire bus. The clock rate can be specified as 1kbps, 10kbps, or 20kbps at an input clock rate of 10MHz; these scale proportionally with input clock (see Figure 3.29).



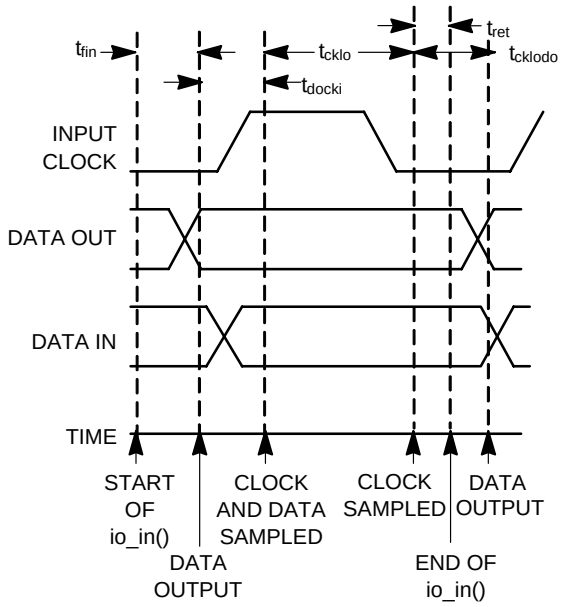
Parameter	Description	Typ
t_{fin}	Function call to CS~ active	69.9 µs
t_{ret}	Return from function	7.2 µs
t_{hold}	Active clock edge to sampling of input data 20 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 11.4 µs 53.4 µs 960.6 µs
t_{high}	Period, clock high (active clock edge = 1) 20 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 25.8 µs 67.8 µs 975.0 µs
t_{low}	Period, clock low (active clock edge = 1)	33.0 µs
t_{setup}	Data output stable to active clock edge	5.4 µs
t_{cs_clock}	Select active to first active clock edge	91.2 µs
t_{clock_cs}	Last clock transition to select inactive	81.6 µs
f	Clock frequency = $1/(t_{high} + t_{low})$ 20 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 17.0 kHz 9.92 kHz 992 Hz

Figure 3.29 Neurowire Master Timing

Neurowire Slave Mode

The Neurowire slave mode I/O object is still provided for legacy support. Echelon recommends using the hardware SPI instead of the legacy software I/O object (See SPI Input/Output section). The hardware SPI provides much higher performance with lower software overhead.

In Neurowire slave mode, pin IO8 is the clock (driven by the external master), IO9 is the serial data output, and IO10 is the serial data input. Serial data is clocked out on pin IO9 at the same time as data is clocked in from pin IO10. Data is clocked by the rising edge of the clock signal (default), which can be up to 18kbps at 10MHz. This data rate scales with PL Smart Transceiver input clock rate. The **`invert`** keyword changes the active clock edge to negative. One of the IO0 – IO7 pins can be designated as a timeout pin. A logic 1 level on the timeout pin causes the Neurowire slave I/O operation to be terminated before the specified number of bits has been transferred. This prevents the PL Smart Transceiver watchdog timer from resetting the chip in the event that fewer than the requested number of bits are transferred by the external clock (see Figure 3.30).



Parameter	Description	Typ
t_{fin}	Function call to data bit out	41.4 µs
t_{ret}	Return from function	19.2 µs
t_{docki}	Data out to input clock and data sampled	4.8 µs
t_{cklo}	Data sampled to clock low sampled	24.0 µs
t_{cklodo}	Clock low sampled to data output	25.8 µs
f	Clock frequency (max)	18.31 kHz

Figure 3.30 Neurowire Slave Timing

The algorithm for each bit of output/input for the Neurowire slave objects is described below. In this description, the default active clock edge (positive) is assumed; if the `invert` keyword is used, all clock levels stated should be reversed.

1. Set IO9 to the next output bit value.
2. Test pin IO8, the clock input, for a high level. This is the test for the rising edge of the input clock. If the input clock is still low, sample the timeout event pin and abort if high.
3. When the input clock is high, store the next data input bit as sampled on pin IO10.

4. Test the input clock for a low input level. This is the test for the falling edge of the input clock. If the input clock is still high, sample the timeout event pin and abort if high.
5. When the input clock is low, return to step 1 if there are more bits to be processed.
6. Else return the number of bits processed.

When either clock input test fails (that is, the clock is sampled *before* the next transition), there is an additional timeout check time of 19.8µs (wait for clock high) or 19.2µs (wait for clock low) added to that stage of the algorithm.

The chip select logic for the Neurowire slave can be handled by the user through a separate bit input object, along with an appropriate handshaking algorithm implemented by the user application program. In order to prevent unnecessary timeouts, the setup and hold times of the chip select line, relative to the start and end of the external clock, must be satisfied.

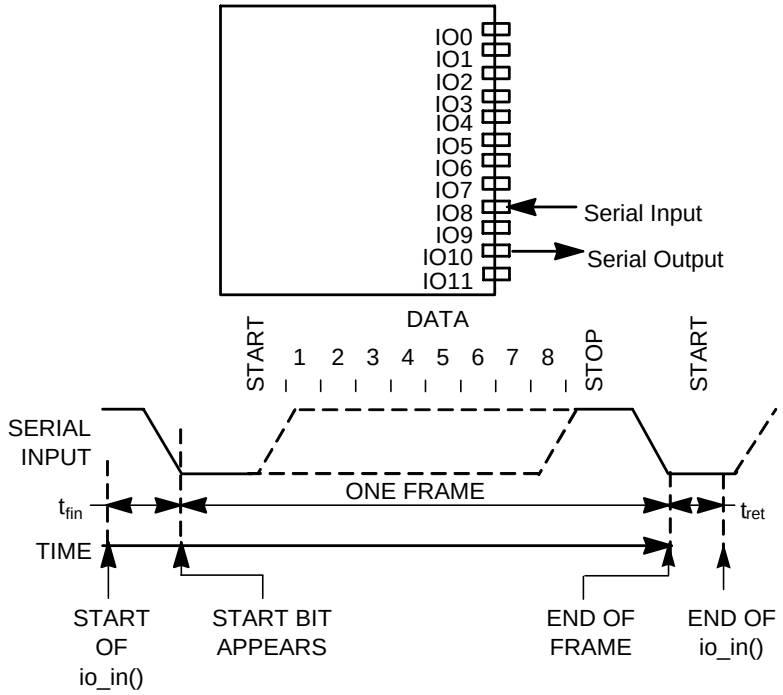
The timeout input pin can either be connected to an external timer or to an output pin of the PL Smart Transceiver that is declared as a oneshot object.

Serial Input/Output

The Serial I/O object is still provided for legacy support. Echelon recommends using the SCI (UART) instead of the legacy software I/O object (See SCI (UART) Input/Output section). The hardware UART provides much higher performance with lower software overhead.

Pin IO8 can be configured as an asynchronous serial input line, and pin IO10 can be configured as an asynchronous serial output line. The bit rates for input and for output can be independently specified to be 600, 1200, 2400, or 4800 bits/second at a 10MHz input clock rate. The data rate scales proportionally to the input clock rate.

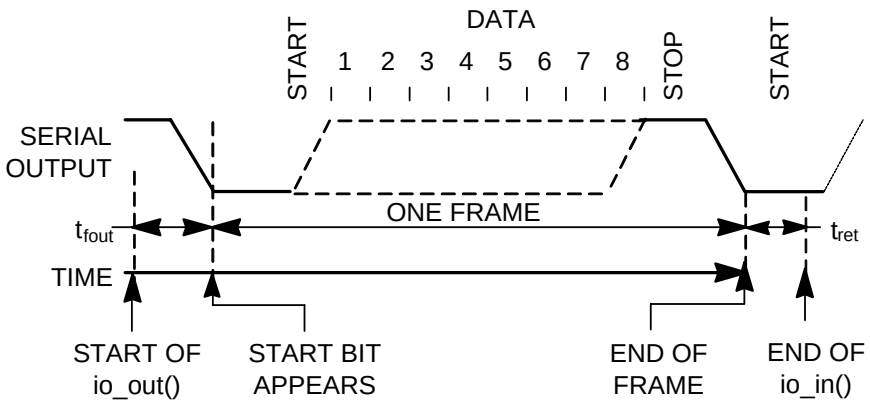
The frame format is fixed at 1 start bit, 8 data bits, and 1 stop bit; and up to 255 bytes can be transferred at a time. Either a serial input or a serial output operation (but not both) can be in effect at any one time. The interface is half-duplex only. This function suspends application processing until the operation is completed. On input, the `io_in()` request will time out after 20 character times if no start bit is received. If the stop bit has the wrong polarity (it should be a 1), the input operation is terminated with an error. The application code can use bit I/O pins for flow control handshaking if required. This function is useful for legacy applications that transfer data to serial devices such as terminals, modems, and computer serial interfaces (see Figures 3.31 and 3.32).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample Min (first sample) Max (timeout)	 67 µs 20 byte frame
t_{ret}	Return from function	10 µs

Figure 3.31 Serial Input Object

The duration of this function call is a function of the number of data bits transferred and the transmission bit rate. t_{fin} (max) refers to the maximum amount of time this function will wait for a start bit to appear at the input. After this time, the function will return a 0 as data. t_{fin} (min) is the time to the first sampling of the input pin. As an example, the timeout period at 2400 bits/second is (20 x 10 x 1/2400) + t_{fin} (min).



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to start bit	79 µs
t_{ret}	Return from function	10 µs

Figure 3.32 Serial Output

The duration of this function call is a function of the number of data bits transferred and the transmission bit rate. As an example, to output 100 bytes at 300 bits/second would require a time duration of (100 x 10 x 1/300) + t_{fout} + t_{ret}.

Touch Input/Output

The Touch I/O object enables easy interface to any slave device which adheres to Dallas Semiconductor's 1-Wire® Memory standard. This interface is a one-wire, open-drain, bidirectional connection.

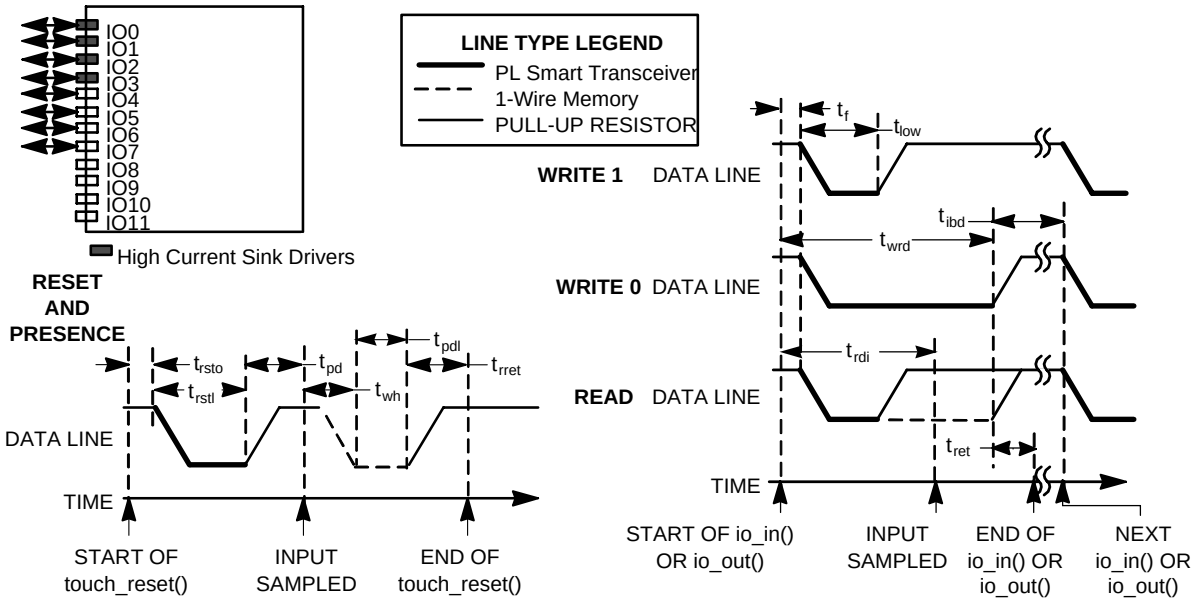
Up to eight 1-Wire Memory busses can be connected to a PL Smart Transceiver through the use of the first eight I/O pins, IO0 – IO7. The only additional component required for this is a pull-up resistor on the data line (refer to the 1-Wire Memory specification below on how to select the value of the pull-up resistor). The high current sink capabilities of IO0 – IO3 pins of the PL Smart Transceiver can be used in applications where long wire lengths are required between the 1-Wire Memory device and the PL Smart Transceiver.

The slave acquires all necessary power for its operation from the data line. Upon physical connection of a 1-Wire Memory device to a master (in this case the PL Smart Transceiver), the 1-Wire Memory generates a low presence pulse to inform the master that it is awaiting a command. The PL Smart Transceiver can also request a presence pulse by sending a reset pulse to the 1-Wire Memory device.

Commands and data are sent bit by bit to make bytes, starting with the LSB. The synchronization between the PL Smart Transceiver and the 1-Wire Memory devices is accomplished through a negative-going pulse generated by the PL Smart Transceiver.

Figure 3.33 shows the details of the reset pulse in addition to the read/write bit slots.

Note: NodeBuilder 3.1., Mini EVK 1, or later, features the ability to adjust the t_{low}, t_{wrd}, and t_{rdi} timing values.



Symbol	Description	Min	Typ	Max
t_{rsto}	Reset call to data line low	—	60.0 µs	—
t_{rstl}	Reset pulse width	—	500 µs	—
t_{pdh}	Reset pulse release to data line high 10MHz	4.8 µs	—	275 µs
t_{pdl}	Presence pulse width	—	120.0 µs	—
t_{wh}	Data line high detect to presence pulse	—	80 µs	—
t_{rret}	Return from reset function	—	12.6 µs	—
t_f	I/O call to data line low (start of bit slot)	—	125.4 µs	—
t_{low}	Start pulse width 10MHz	—	4.2 µs	—
t_{rdi}	Start pulse edge to sampling of input (read operation) 10MHz	—	15.0 µs	—
t_{wrd}	Start pulse edge to PL Smart Transceiver releasing the data line 10MHz	—	66.6 µs	—
t_{ibd}	Inter-bit delay 10MHz	—	61.2 µs	—
t_{ret}	Return from I/O call	—	42.6 µs	—

Figure 3.33 Touch Input/Output Object

The leveldetect input object can be used for detection of asynchronous attachments of 1-Wire Memory devices to the PL Smart Transceiver. In such a case, the leveldetect input object is overlaid on top of the Touch I/O object. Refer to the *Neuron C Programmer's Guide* for information on I/O object overlays.

For more specific information on the mechanical, electrical, and protocol specifications, refer to the 1-Wire device information available from Dallas Semiconductor Corporation.

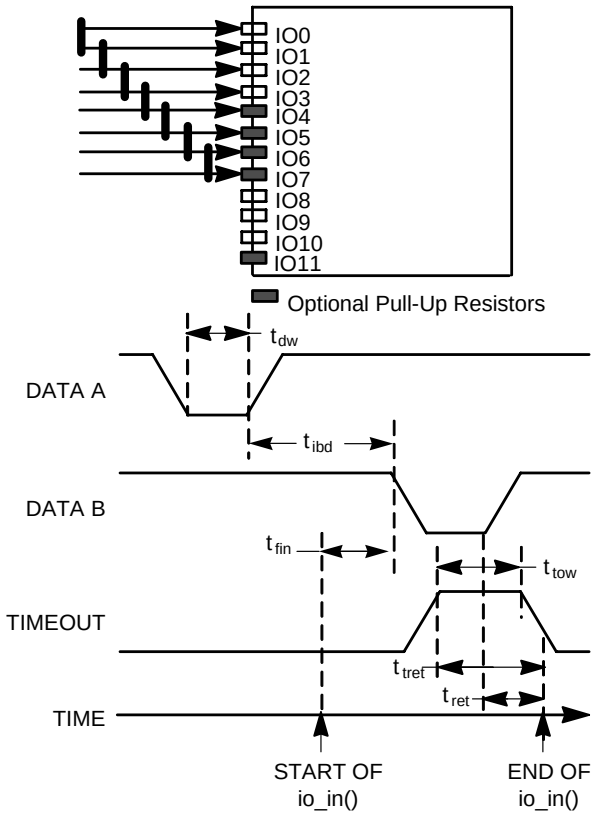
Wiegand Input

This input object provides an easy interface to any card reader supporting the Wiegand standard. Data from the reader is presented to the PL Smart Transceiver through the use of two of its first eight I/O pins, IO0 – IO7. Up to four Wiegand devices can be connected to the PL Smart Transceiver. Data is read MSB first.

Wiegand data starts as a negative-going pulse on one of the two pins selected. One input represents a logical 0 bit and the other pin a logical 1, as selected through the I/O declaration. The bit data on the two lines are mutually exclusive and are spaced at least 150µs apart. Figure 3.34 shows the timing relationship of the two data lines with respect to each other and the PL Smart Transceiver.

Any unused I/O pin from IO0 to IO7 can be optionally selected as the timeout pin. When the timeout pin goes high, the function aborts and returns. The application processor's watchdog timer is automatically updated during the operation of this input object.

Incoming data on any of the Wiegand input pins is sampled by the PL Smart Transceiver every 200ns at a 10MHz clock (scales inversely with the clock frequency). because the Wiegand data is usually asynchronous, care must be taken in the application program to ensure that this function is called in a timely manner in order that no incoming data is lost.



Symbol	Description	Min	Typ	Max
t_{fin}	Function call to start of second data edge	—	75.6 µs	—
t_{dw}	Input data width (at 10MHz)	200 ns	100 µs	880 ms
t_{ibd}	Inter-bit delay	150 µs	—	900 µs
t_{tow}	Timeout pulse width	—	39 µs	—
t_{tret}	Timeout to function return	—	18.0 µs	—
t_{ret}	Last data bit to function return	—	74.4 µs	—

Figure 3.34 Wiegand Input Object

SCI (UART) Input/Output

Pins IO8 and IO10 can be configured as asynchronous SCI (serial communications interface) input and output lines, respectively. The SCI object model supports the following bit rates for half-duplex transfers when operating at 10MHz: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, and 115200 bits per second. The effective transmitted data rate for half-duplex transfers corresponds to the bit rate at all speeds. There are no inter-byte idle periods and the bit rate of the input and output can not be independently specified.

For full-duplex transfers, when data is being received and transmitted at the same time, the effective bit rate will be 60% at 57600 bits per second, and 30% at 115200 bits per second. All other bit rates specified above for half-duplex transfers

are also supported for full-duplex transfers. No errors are introduced (other than inter-byte spacing of transmitted data) under these conditions.

For 6.5536MHz operation, the bit rates are limited to a maximum of 19200 bits per second for both half and full-duplex transfers.

The frame format is one start bit, eight data bits and one or two stop bits. Up to 255 output bytes and 255 input bytes can be transferred at a time. If an input stop bit has the wrong polarity, the interface will attempt to recover and re-synchronize. However, a framing error will be flagged in the status register. If necessary, the application code can use other bit I/O pins for flow-control handshaking.

This I/O model depends on interrupts to receive data at high speed. Once reception has be set up, control will be returned to the application immediately and the application will need to poll the I/O model for reception completion. Reception can be suspended and resumed by disabling and enabling interrupts. Turning off interrupts might be required when going off-line, or for ensuring that other time-critical application execution is not disturbed by background interrupts. Additionally, SCI reception can also be aborted. Note that sustained reception at 115,200bps can starve the application processor. Care must be given to allow the PL Smart Transceiver to process received bytes in a timely manner and update the watchdog timer.

However, data transmission is NOT handled by interrupts; control will be returned to the application only after the last byte has been placed in the transmission shift register. It is important to note that if previously set up, reception interrupts will work even while transmission is taking place. This provides a **full duplex interface**.

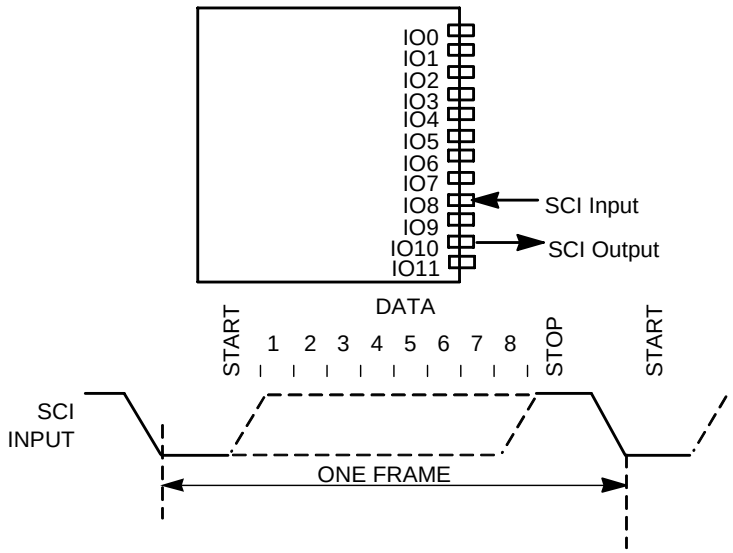


Figure 3.35 SCI Input/Output

SPI Input/Output

Pins IO8, IO9 and IO10 can be configured as a serial peripheral interface (SPI) port. The directions of the pins vary with the configuration. In master mode, pin IO8 is the clock (driven by the PL Smart Transceiver), IO9 is serial data input (Master In Slave Out or MISO) and IO10 is serial data output (Master Out Slave In or MOSI). In slave mode, pin IO8 is the clock input, IO9 is serial data output (MISO) and IO10 is serial data input (MOSI). If the **`Neurowire`** keyword is used, the pins assume a Neurowire compatible direction in which IO9 is always output and IO10 is always input. Serial data is clocked out on the output pin at the same time as it is clocked in on the input pin. In SPI master mode, no other masters are allowed on the bus. IO7 can be used as a select pin in slave mode, allowing the PL Smart Transceiver to

coexist with other slave mode devices on a 3 wire bus. A logic one level on the select line disables the output drivers of the output pins and puts them in a high impedance state.

If the PL Smart Transceiver is the only slave device on the SPI bus and the master device does not drive the **Slave Select** (SS~) signal, then either

Pin IO7 should be declared as an input pin and externally grounded.

OR

Pin IO7 must be declared in the following order:

```
IO_7 output bit io_p7_out = 1;     // initialize to '1'
IO_7 input bit io_p7_in;
```

As long as the IO7 output bit is initialized to a 1 and the SS~ is disabled, IO7 can be used as an input. Note that SS~ should be used whenever possible to ensure proper synchronization and recovery in the event of framing errors from the master device.

The bit rates supported by the SPI port are summarized in Tables 3.6 and 3.7

Table 3.6 Master mode

Clock	10MHz	6.5536MHz	
7	19.531kbps	12.8kbps	
6	39.063kbps	25.6kbps	
5	78.125kbps	51.2kbps	See *Note*
4	156.250kbps	102.4kbps	See *Note*
3	312.500kbps	204.8kbps	See *Note*
2	625.000kbps	409.6kbps	See *Note*
1	1250.000kbps	819.2kbps	See *Note*
0	2500.000kbps	1638.4kbps	See *Note*

Note: For Clock 5 and higher bit rates, the bit rate shown is the peak rate. The data is burst out in pairs of bytes and the overall average data rate is limited to approximately 40kbps and 25kbps for 10MHz and 6.5536MHz input clocks, respectfully.

Table 3.7 Slave mode

	10MHz	6.5536MHz	
Max burst rate	1250kbps	819.2kbps	
Max burst size	2 bytes	2 bytes	
Min burst spacing	400us	640us	From start of one burst to next.
Max sustained data rate	40kbps	25kbps	

Sustained reception in slave mode at maximum bit rate can starve the application processor and cause overruns and presents a possible risk of watchdog timeout. Care must be given to allow the PL Smart Transceiver to process received bytes in a timely manner. Master mode has no such restriction because the PL Smart Transceiver regulates the data transfer.

The **`clockedge`** and **`invert`** keywords are used to determine the point at which data is sampled and the idle level of the clock signal. The clock signal is idle at the logic 1 level. The `invert` keyword could be used to change the idle state to correspond to a logic 0 level. Common SPI implementations use the terms clock phase (**CPHA**) and clock

polarity (**CPOL**) to determine the behavior of the clock signal during SPI transmissions. These terms relate directly to the `clockedge` and `invert` keywords used in this data book as follows:

CPHA

```
1 = clockedge(+)
0 = clockedge(-)
```

CPOL

```
1 = [default]
0 = invert
```

The active edge of the clock is determined by the `clockedge` and `invert` keywords. If the clock signal is idle at logic 1 (default), then `clockedge(-)` indicates that the falling edge of the clock signal is active. If the `invert` keyword is used, the rising edge of the clock signal would be active (see Figures 3.36 and 3.37).

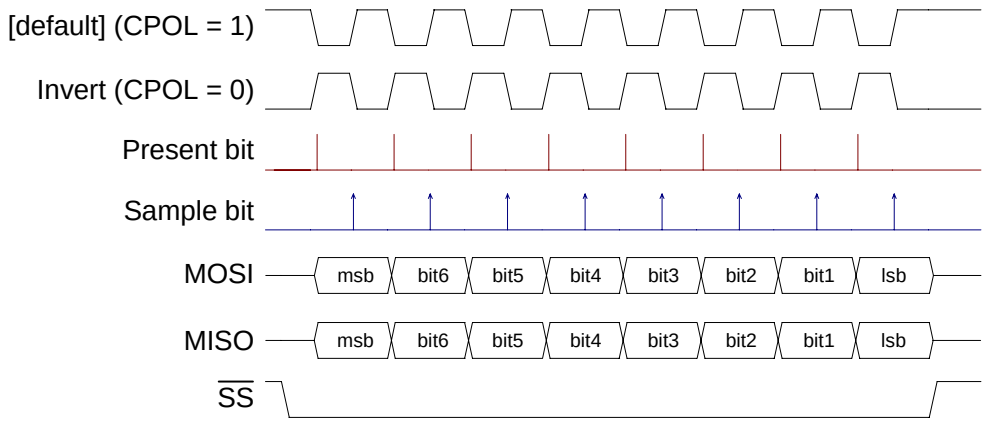


Figure 3.36 Transmission Timing for Clockedge(-) (CPHA : 0)

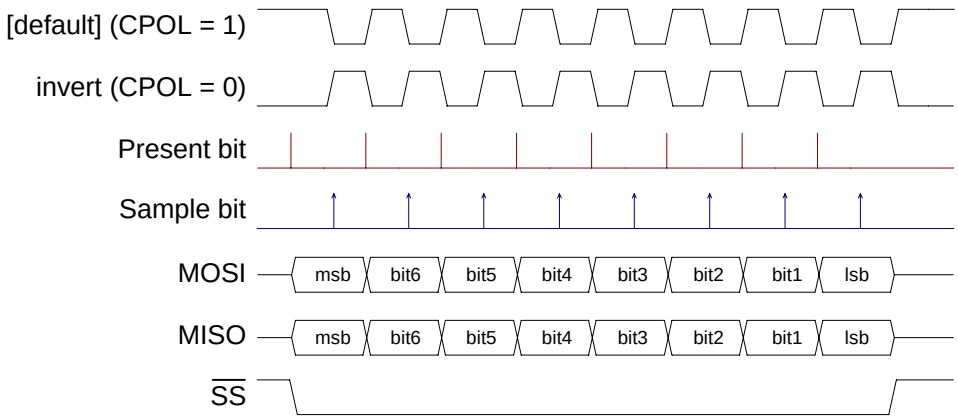
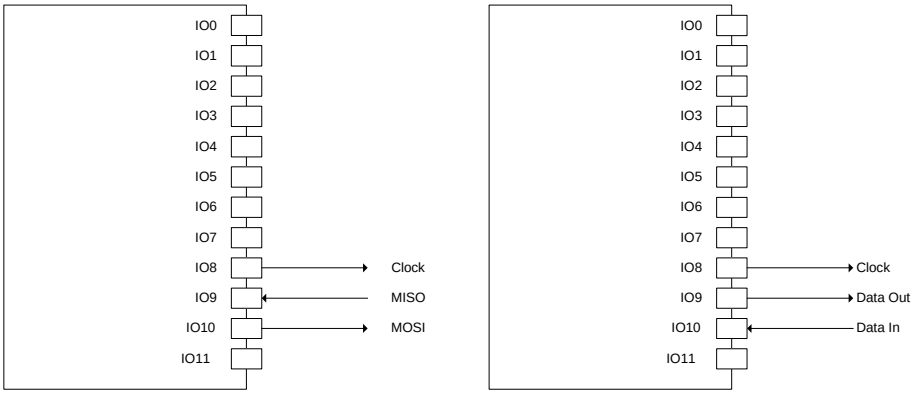


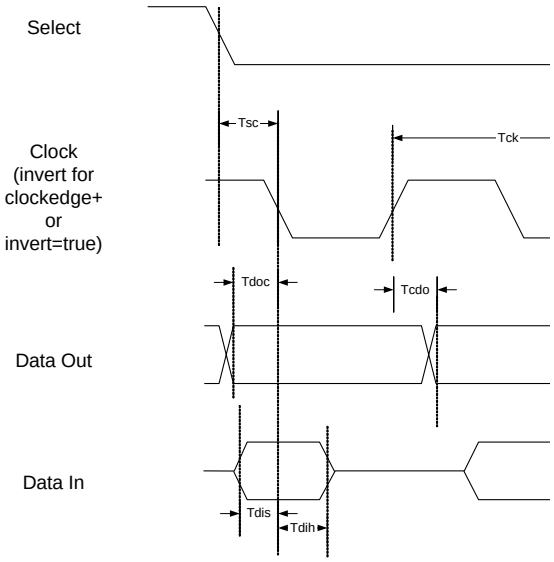
Figure 3.37 Transmission Timing for Clockedge(+) (CPHA : 1)

Up to 255 bytes can be bi-directionally transferred at a time. This I/O model depends on interrupts to process data at high speed and does not use the `io_in()` and `io_out()` function calls. Once transfer is initiated, control will be returned to the application immediately and the application will need to poll the I/O model for completion. Transfers can be suspended and resumed by disabling and enabling interrupts. Turning off interrupts might be required when going off-line, or for assuring that other time-critical application execution is not disturbed by background interrupts. Additionally, transfers can also be aborted.



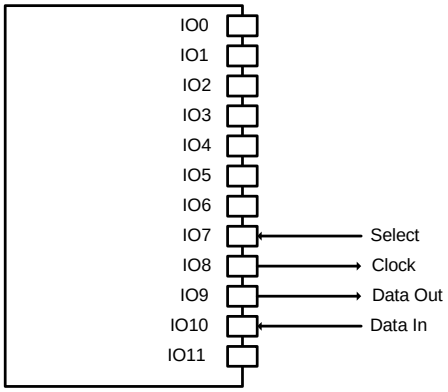
SPI Master

SPI Master (Neurowire pin mode)

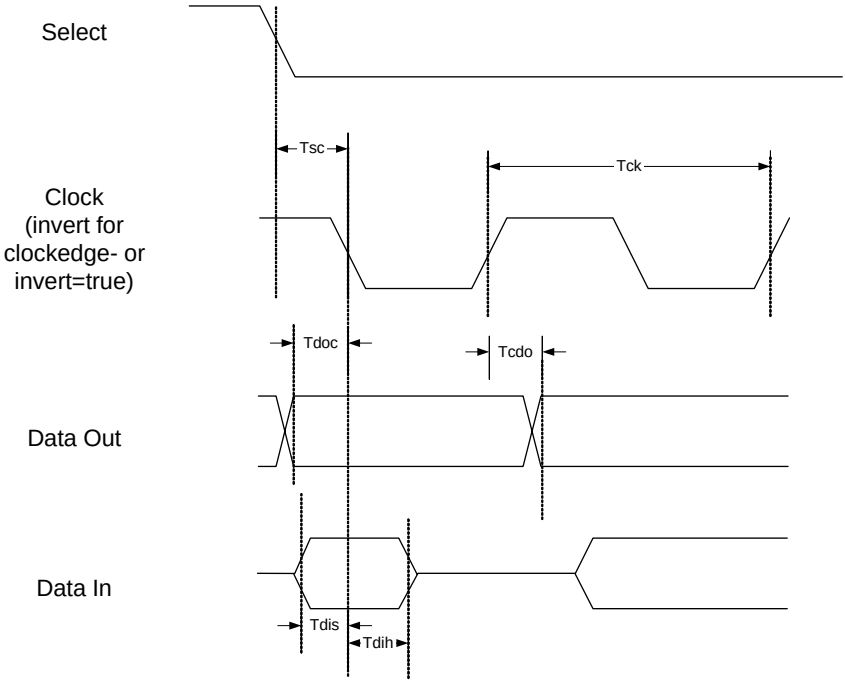


Param	Description	Min	Typ	Max	Units
Tck	Clock cycle (user specified)				
Tsc	Select low to Clock transition	4.8			µs
Tdoc	Data out to Clock (1st bit of invert mode)	0.5*Tck			ns
Tcdo	Clock to data out			5	ns
Tdis	Data in setup	10			ns
Tdih	Data in hold	10			ns

Figure 3.38 SPI Master Mode Timing



SPI Slave



Param	Description	Min	Typ	Max	Units
Tck	Clock cycle (user specified)			1.25	
Tsc	Select low to Clock transition	220			µs
Tdoc	Data out to Clock (1st bit of invert mode)	440			ns
Tcdo	Clock to data out			45	ns
Tdis	Data in setup	10			ns
Tdih	Data in hold	10			ns
Tsdz	Select high to data in high impedance			220	ns

Figure 3.39 SPI Slave Mode Timing

Timer/Counter Input Objects

The PL Smart Transceivers have two 16-bit timer/counters. For the first timer/counter, IO0 is used as the output, and a multiplexer selects one of pins IO4 – IO7 as the input. The second timer/counter uses IO1 as the output and IO4 as the input (see Figure 2.7). Multiple timer/counter input objects can be declared on different pins within a single application. By calling the `io_select()` function, the application can use the first timer/counter in up to four different input functions. If a timer/counter is configured in one of the output functions, or as a quadrature input, then it can not be reassigned to another timer/counter object in the same application program.

The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a **`when`** clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Input timer/counter objects have the advantage (over non-timer/counter objects) in that input events will be captured even if the application processor is occupied doing something else when the event occurs. A true `when` statement condition for an event being measured by a timer/counter is the completion of the measurement and a value being returned to an event register. If the processor is delayed due to software processing and cannot read the register before another event occurs, then the value in the register will reflect the status of the last event. The timer/counters are automatically reset upon completion of a measurement. **The first measured value of a timer/counter is always discarded to eliminate the possibility of a bad measurement after the chip comes out of a reset condition.** Single events can not be measured with the timer/counters. Figure 3.40 shows an example of how the timer/counter objects are processed with a Neuron C `when` statement.

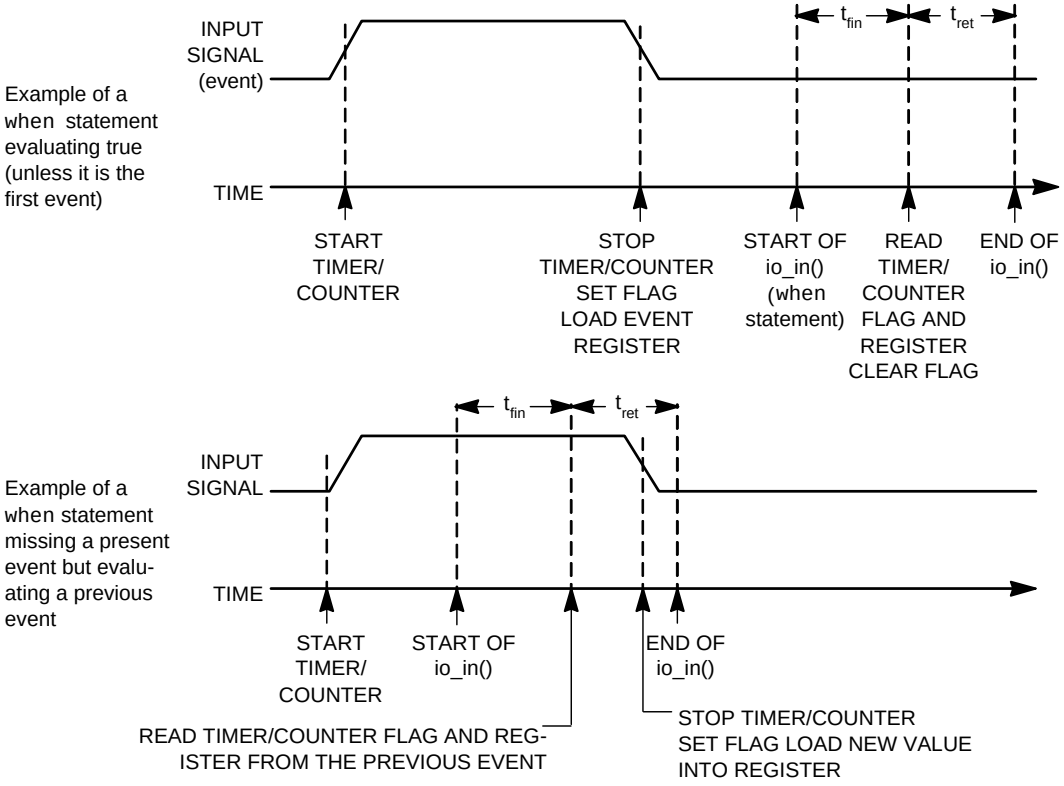
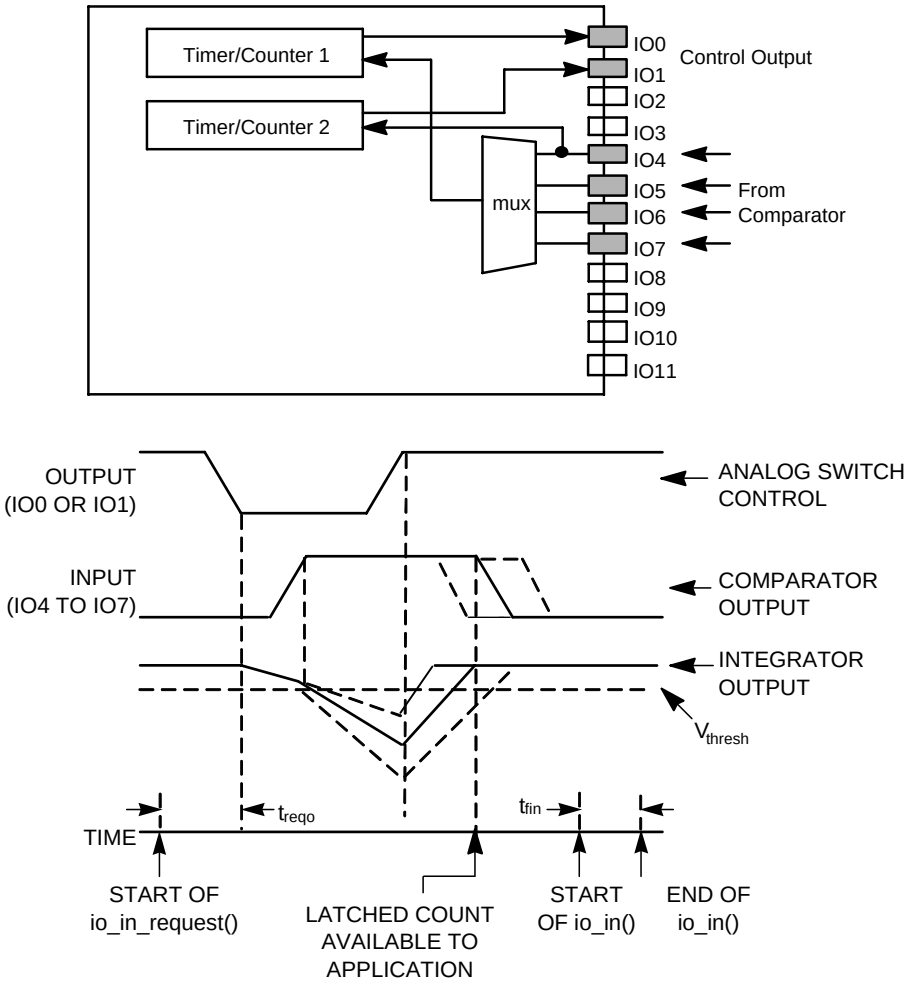


Figure 3.40 Example of `when` Statement Processing Using the Ontime Input Function

Dualslope Input

This input object uses a timer/counter to control and measure the integration periods of a dualslope integrating analog to digital converter (see Figure 3.41). The timer/counter provides the control output signal and senses a comparator output signal. The control output signal controls an external analog multiplexer which switches between the unknown input voltage and a voltage reference. The timer/counter's input pin is driven by an external comparator which compares the integrator's output with a voltage reference. At the end of conversion, the external comparator will drive a low level to one of pins IO4 – IO7. If external circuitry indicates "end of conversion" with a high level, use the **`invert`** keyword in the I/O declaration.

The resolution and range of the timer/counter period options is shown in Table 3.8 in the *Notes* section of this chapter.



Symbol	Description	Min	Typ	Max
t_{reqo}	`io_in_request()` to output toggle	—	75.6 µs	—
t_{fin}	Input function call and return	—	82.8 µs	—

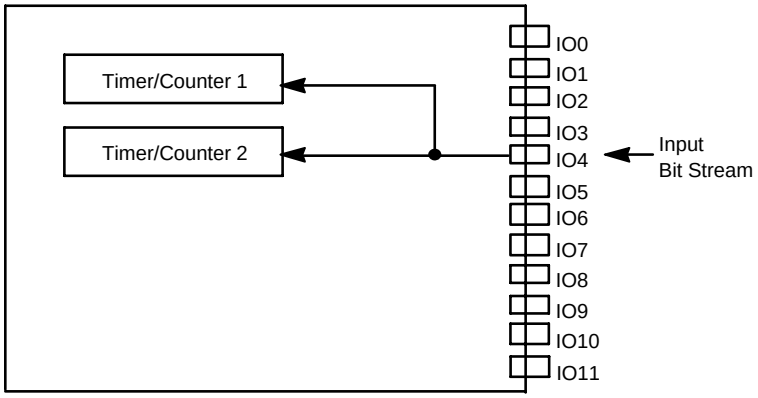
Figure 3.41 Dualslope Input Object

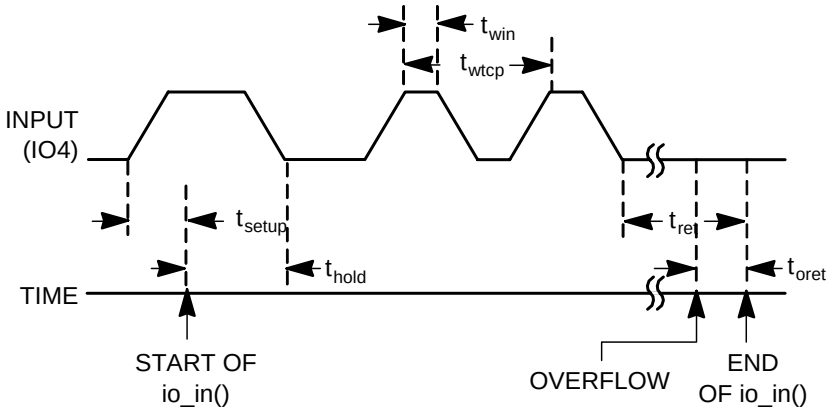
Edgelog Input

The edgelog input object can record a stream of input pulses measuring the consecutive low and high periods at the input and storing them in user-defined storage (see Figure 3.42). The values stored represent the units of clock period between rising and falling input signal edges.

The measurement series starts on the first rising (positive) edge, unless the **`invert`** keyword is used in the I/O object declaration. The measurement process stops whenever an overflow condition is sensed on either timer/counter.

The resolution and range of the timer/counter period options are shown in Table 3.8 in the *Notes* section at the end of this chapter. This object is useful for analyzing an arbitrarily-spaced stream of input edges (or pulses), such as the output of a UPC bar-code reader or infrared receiver.





Symbol	Description	Min	Typ	Max
t_{setup}	Input data setup	0	—	—
t_{win}	Input pulse width	1 T/C clk	—	65,534 T/C clks
t_{hold}	`io_in()` call to data input edge for inclusion of that pulse	26.4 µs	—	—
t_{wtcp}	Two consecutive pulse widths	104 µs	—	—
t_{oret}	Return on overflow	—	42.6 µs	—
t_{ret}	Return on count termination	—	49.6 µs	—

Figure 3.42 Edgelog Input Object

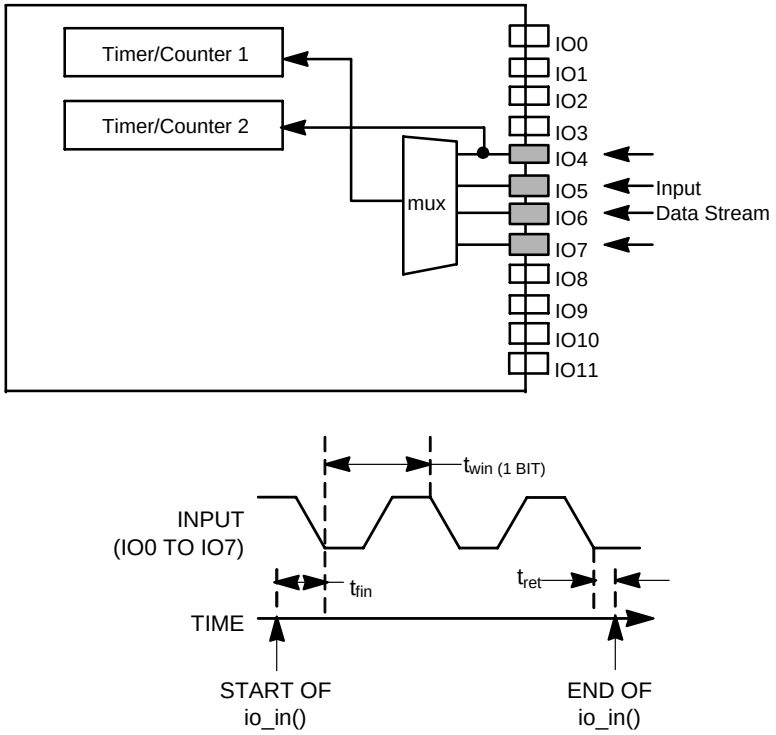
***Note*:** T/C clk represents the period of the clock used during the declaration of the I/O object.

Infrared Input

The infrared input object is used to capture a stream of data generated by a class of infrared remote control devices (see Figure 3.43). The input to the object is the demodulated series of bits from infrared receiver circuitry. The period of the on/off cycle determines the data bit value, a shorter cycle indicating a one, and a longer cycle indicating a zero. The actual threshold for the on/off determination is set at the time of the call of the function. The measurements are made between the negative edges of the input bits unless the **`invert`** keyword is used in the I/O declaration.

The infrared input object, based on the input data stream, generates a buffer containing the values of the bits received. The resolution and range of the timer/counter period options is shown in Table 3.8 in the *Notes* section at the end of this chapter.

This function can be used with an off-the-shelf IR demodulator such as an NEC µPD1913 or Sharp GP1U50X to quickly develop an infrared interface to the PL Smart Transceiver. The edgelog input object can also be used for this purpose. However, this requires more code.



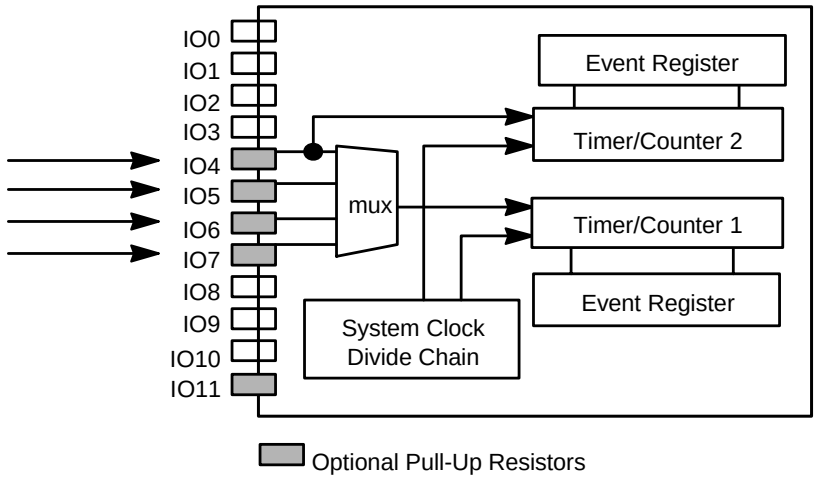
Symbol	Description	Min	Typ	Max
t_{fin}	Function call to start of input sampling	—	82.2 µs	—
t_{ret}	End of last valid bit to function return	max-period	max-period	—
t_{win}	Minimum input period width	—	93 µs	—

Note: max-period is the timeout period passed to the function at the time of the call.

Figure 3.43 Infrared Input Object

Ontime Input

A timer/counter can be configured to measure the time for which its input is asserted. Table 3.8 shows the resolution and maximum times for different I/O clock selections. Assertion can be defined as either logic high or logic low. This object can be used as a simple analog-to-digital converter with a voltage-to-time circuit, or for measuring velocity by timing motion past a position sensor (see Figures 3.40 and 3.44).



Reference Figure 3.40

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	86 µs
t_{ret}	Return from function	52/22 µs*

*If the measurement is new, t_{ret} = 52µs. If a new time is not being returned, t_{ret} = 22µs.

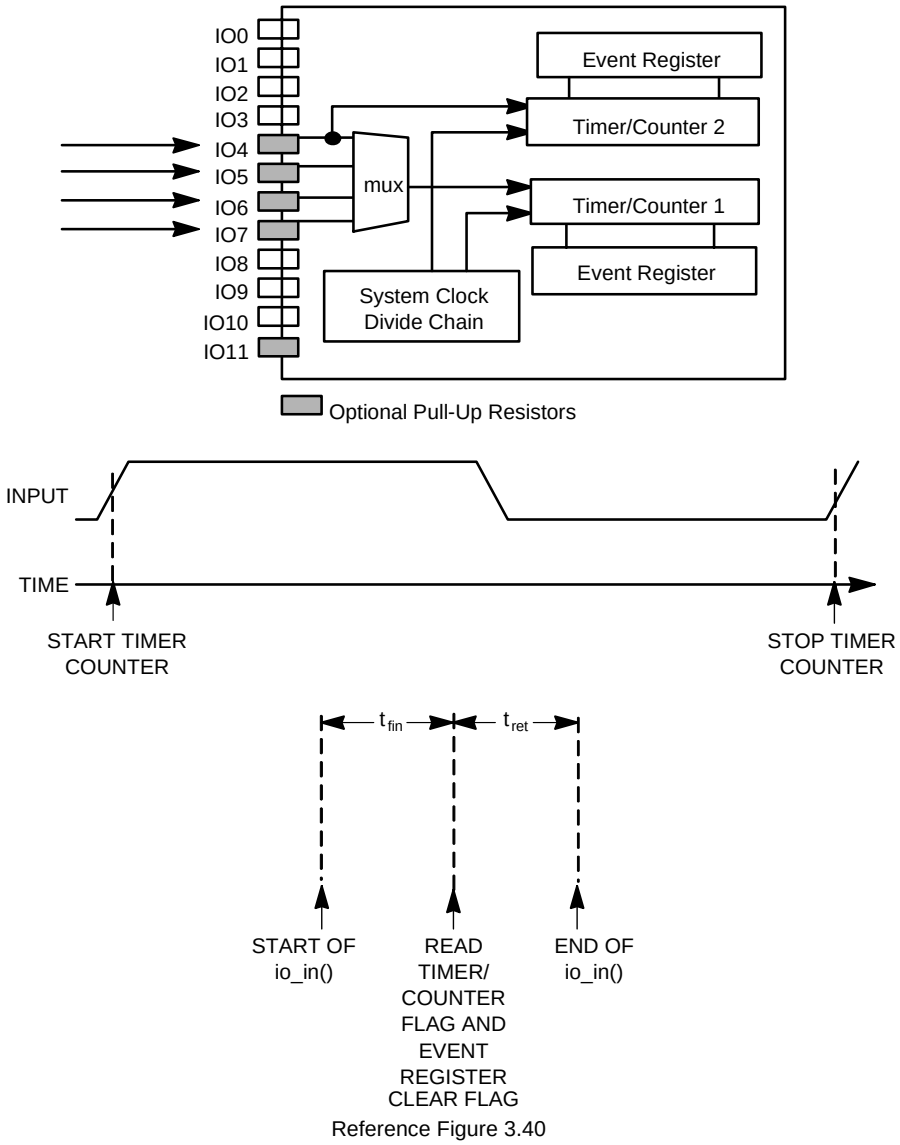
Figure 3.44 Ontime Latency Values

This is a level-sensitive function. The active level of the input signal gates the clock driving the internal counter in the PL Smart Transceiver.

The actual active level of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the high level.

Period Input

A timer/counter can be configured to measure the period from one rising or falling edge to the next corresponding edge on the input. Table 3.8 shows the resolution and maximum time measured for various clock selections. This object is useful for instantaneous frequency or tachometer applications. Analog-to-digital conversion can be implemented using a voltage-to-frequency converter with this object (see Figure 3.45).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	86 µs
t_{ret}	Return from function	52/22 µs*

*If the measurement is new, t_{ret} = 52µs. If a new time is not being returned, t_{ret} = 22µs.

Figure 3.45 Period Input Latency Values

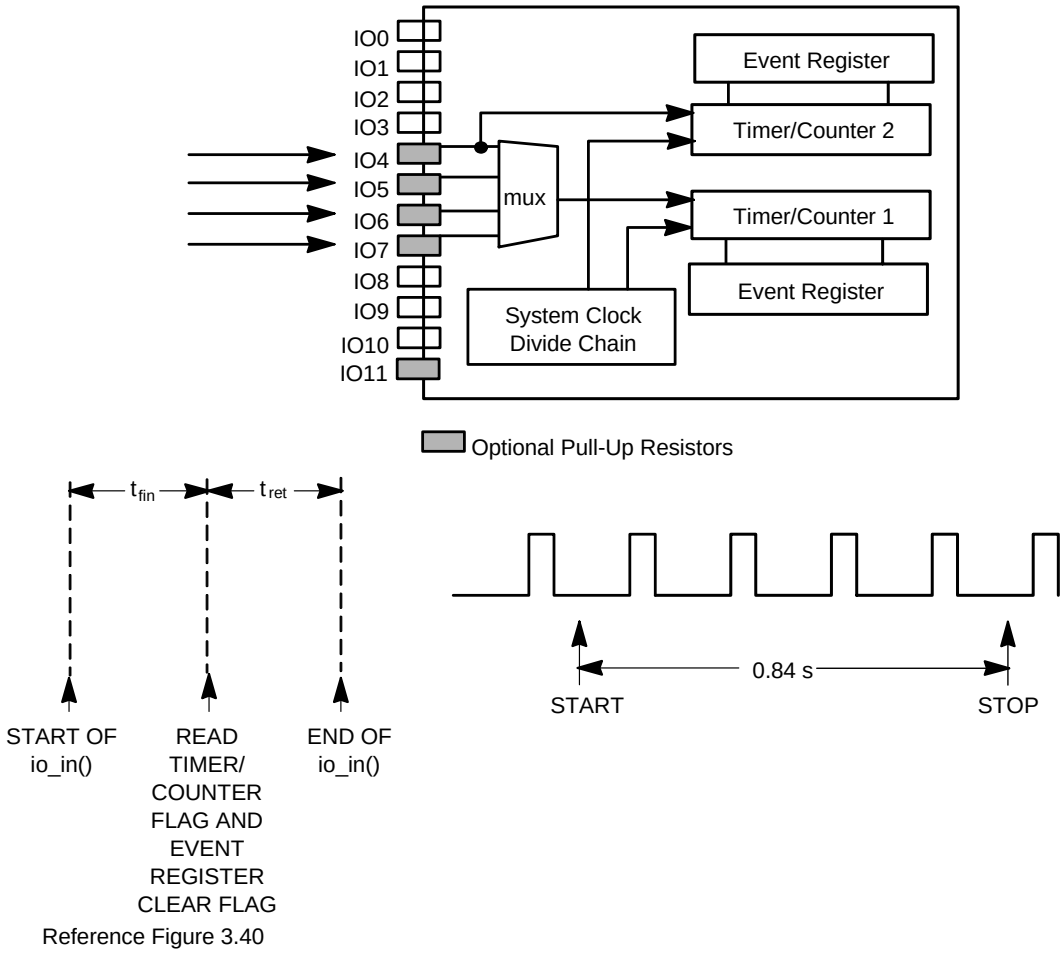
This is an edge-sensitive function. The clock driving the internal counter in the PL Smart Transceiver is free running. The detection of active input edges stops and resets the counter each time.

The actual active edge of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the negative edge.

Because the period function measures the delay between two consecutive active edges, the `invert` option has no effect on the returned value of the function for a repeating input waveform.

Pulsecount Input

A timer/counter can be configured to count the number of input edges (up to 65,535) in a fixed time (0.8388608 second) at all allowed input clock rates. Edges can be defined as rising or falling. This object is useful for average frequency measurements, or tachometer applications (see Figure 3.46).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	86 µs
t_{ret}	Return from function	52/22 µs*

*If the measurement is new, t_{ret} = 52µs. If a new time is not being returned, t_{ret} = 22µs.

Figure 3.46 Pulse Count Input Latency Values

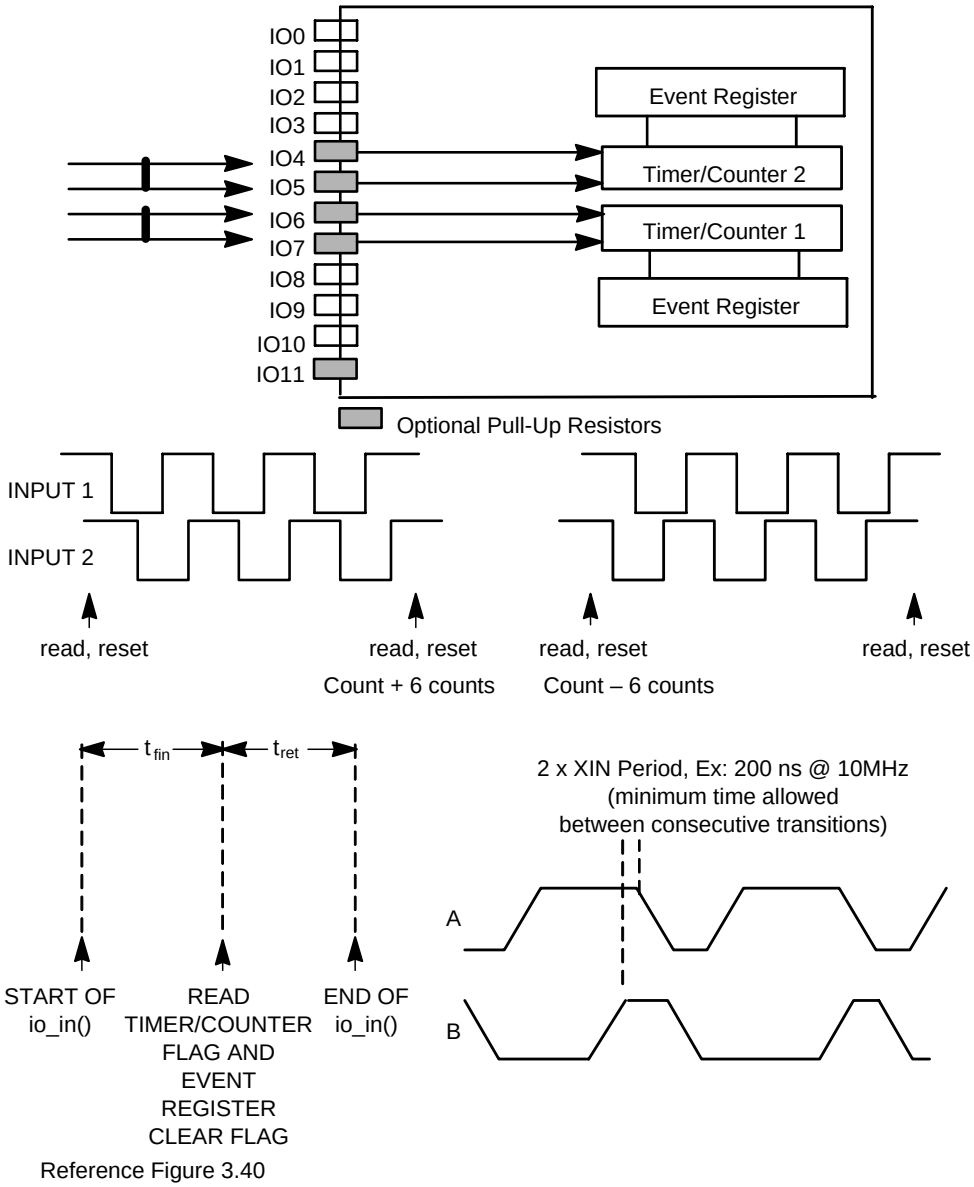
This is an edge-sensitive function. The clock driving the internal counter in the PL Smart Transceiver is the actual input signal. The counter is reset automatically every 0.839 second.

The internal counter increments with every occurrence of an active input edge. Every 0.839 second, the content of the counter is saved and the counter is then reset to 0. This sequence is repeated indefinitely.

The actual active edge of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the negative edge.

Quadrature Input

A timer/counter can be configured to count transitions of a binary Gray code input on two adjacent input pins. The Gray code is generated by devices such as shaft encoders and optical position sensors which generate the bit pattern (00,01,11,10,00, …) for one direction of motion and the bit pattern (00,10,11,01,00, …) for the opposite direction. Reading the value of a quadrature object gives the arithmetic net sum of the number of transitions because the last time it was read (-16,384 to 16,383). The maximum frequency of the input is one-quarter of the input clock rate, for example 2.5MHz with a 10MHz PL Smart Transceiver input clock. Quadrature devices can be connected to timer/counter 1 via pins IO6 and IO7, and timer/counter 2 via pins IO4 and IO5 (see Figure 3.47). If the second input transitions low while the first input is low and high while the first input is high, the counter counts up. Otherwise, the count is down.



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	90 µs
t_{ret}	Return from function	88 µs

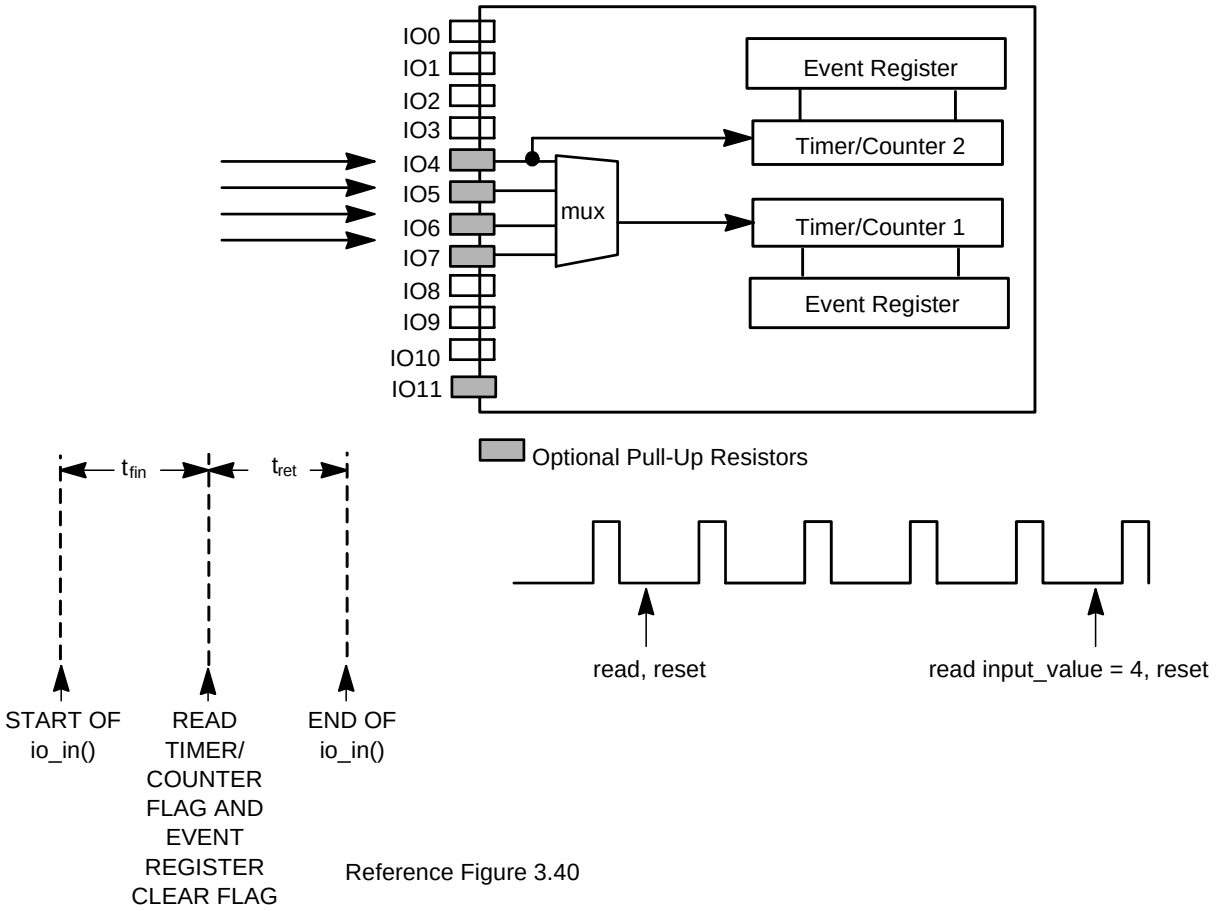
Figure 3.47 Quadrature Input Latency Values

A call to this function returns the current value of the quadrature count because the last read operation. The counter is then reset and ready for the next series of input transitions. The count returned is a 16-bit signed binary number, capped at ±16K.

The number shown in the diagram above is the minimum time allowed between consecutive transitions at either input of the quadrature function block. For more information, see the, *Neuron Chip Quadrature Input Function Interface* engineering bulletin.

Totalcount Input

A timer/counter can be configured to count either rising or falling input edges, but not both. Reading the value of a totalcount object gives the number of transitions because the last time it was read (0 to 65,535). Maximum frequency of the input is one-quarter of the input clock rate, for example 2.5MHz at a maximum of 10MHz PL Smart Transceiver input clock. This object is useful for counting external events such as contact closures, where it is important to keep an accurate running total (see Figure 3.48).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	92 µs
t_{ret}	Return from function	61 µs

Figure 3.48 Totalcount Input Latency Values

A call to this function returns the current value of the totalcount value corresponding to the total number of active clock edges because the last call. The counter is then reset, and ready for the next series of input transitions.

The actual active edge of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the negative edge.

Timer/Counter Output Objects

Edgedivide Output

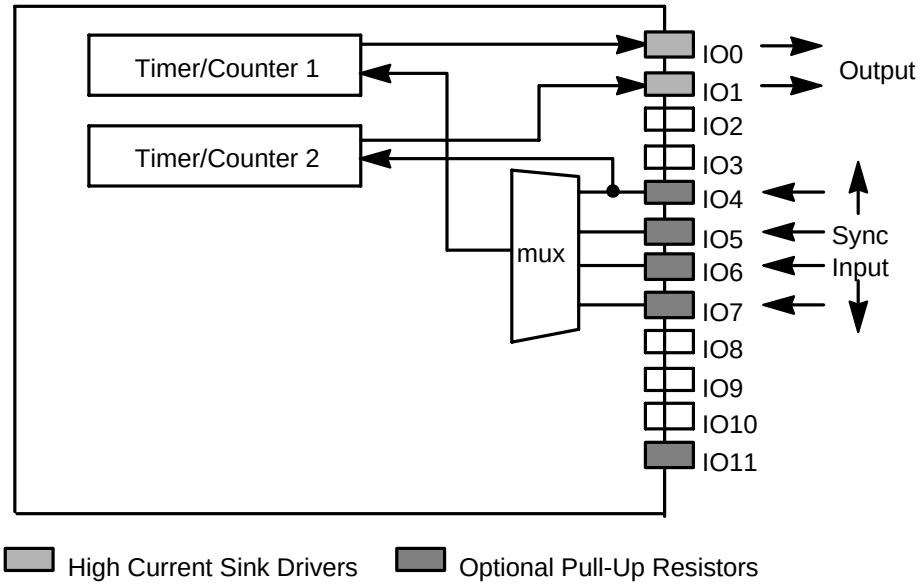
This output object acts as a frequency divider by providing an output frequency on either pin IO0 or IO1. The output frequency is a divided-down version of the input frequency applied on pins IO4 – IO7. The object is useful for any divide-by-n operation, where *n* is passed to the timer/counter object through the application program and can be from 1 to 65,535. The value of 0 forces the output to the off level and halts the timer/counter.

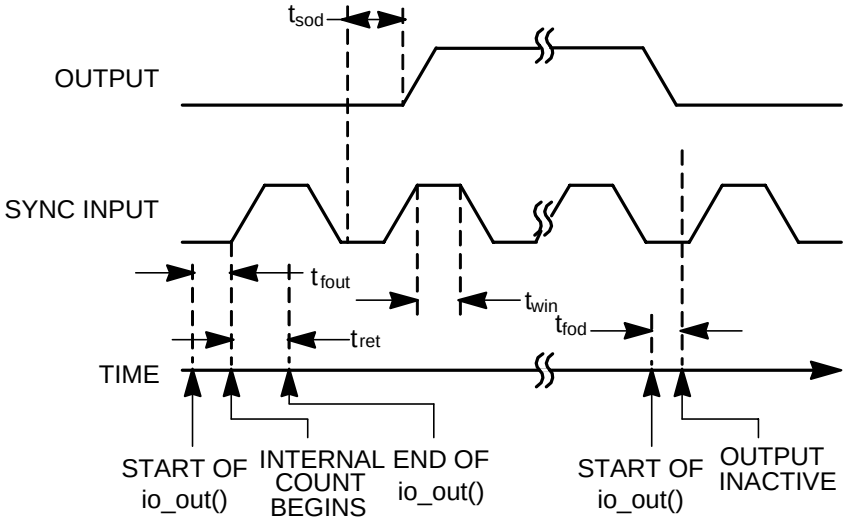
A new divide value will not take effect until after the output toggles, with two exceptions: if the output is initially disabled, the new (non-zero) output will start immediately after t_{fout}; or, for a new divide value of 0, the output is disabled immediately.

Normally the negative edges of the input sync pulses are the active edge. Using the **`invert`** keyword in the object declaration makes the positive edge active.

The initial state of the output pin is logic 0 by default. This can also be changed to logic 1 through the object declaration.

Figure 3.49 shows the pinout and timing information for this output object.



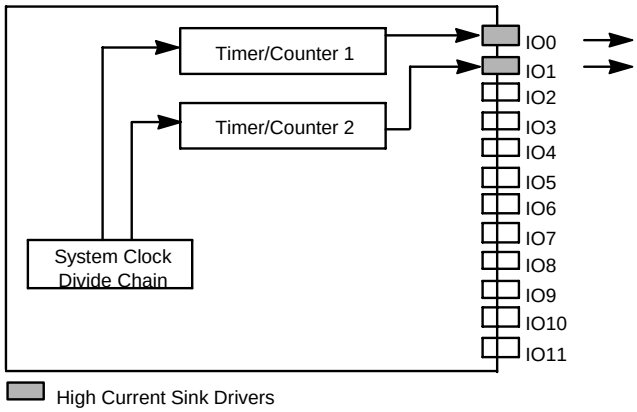


Symbol	Description	Min	Typ	Max
t_{fout}	Function call to start of timer	—	96 µs	—
t_{fod}	Function to output disable	—	82.2 µs	—
t_{sod}	Active sync edge to output toggle	550 ns	—	750 ns
t_{win}	Sync input pulse width (10MHz)	200 ns	—	—
t_{ret}	Return from function	—	13 µs	—

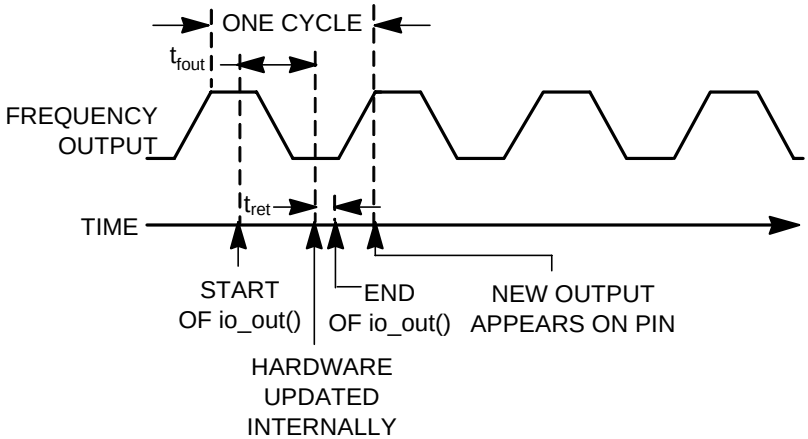
Figure 3.49 Edgedivide Output Object

Frequency Output

A timer/counter can be configured to generate a continuous square wave of 50% duty cycle. Writing a new frequency value to the device takes effect at the end of the current cycle. This object is useful for frequency synthesis to drive an audio transducer, or to drive a frequency to voltage converter to generate an analog output (see Figure 3.50).



Frequency Resolution and Maximum Range at 10MHz



CLK	Resolution	Range	Unit
0	0.4	26.21	µs
1	0.8	52.42	µs
2	1.6	104.86	µs
3	3.2	209.71	µs
4	6.4	419.42	µs
5	12.8	838.85	µs
6	25.6	1677	µs
7	51.2	3355	µs

Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to output update	96 µs
t_{ret}	Return from function	13 µs

Figure 3.50 Frequency Output Latency Values

A new frequency output value will not take effect until the end of the current cycle. There are two exceptions to this rule. If the output is disabled, the new (non-zero) output will start immediately after t_{fout}. Also, for a new output value of zero, the output is disabled immediately and not at the end of the current cycle.

A disabled output is a logic zero by default unless the **invert** keyword is used in the I/O object declaration. The resolution and range for this object scale with PL Smart Transceiver input clock rate.

Infrared Pattern Output

An **`infrared_pattern`** I/O object produces a series of timed repeating square wave output signals. The frequency of the square wave output is controlled by the application. Normally, this frequency is the modulation frequency used for infrared transmission.

The pattern of this modulation frequency is controlled by an array of unsigned long timing values. The first value in this array controls the length of the first burst of modulation frequency signal output. The output is active for this period. The second value in this array controls the length of an absence of the modulation frequency signal. The output is idle for this period. This pattern is then repeated by subsequent values in the array in order to produce a sequence of frequency output bursts separated by idle periods. This array is similar to the array generated by the **edgelog** input object.

This I/O object is useful for driving an infrared LED to provide infrared control of devices that support infrared remote control.

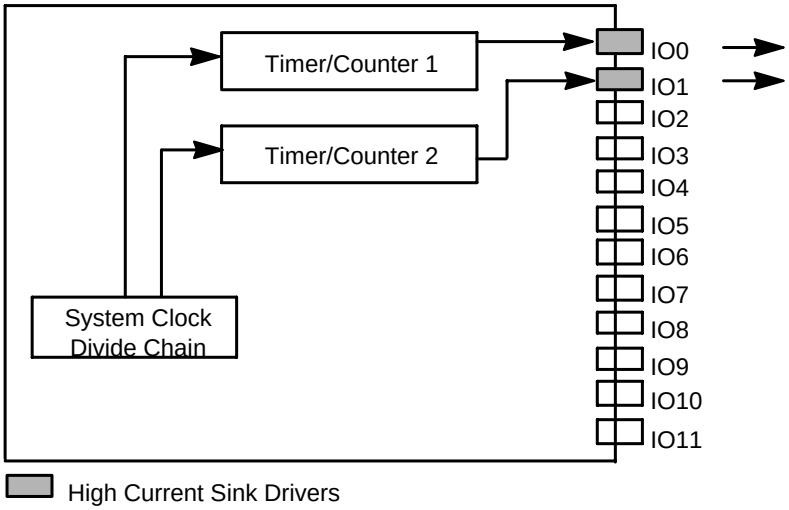
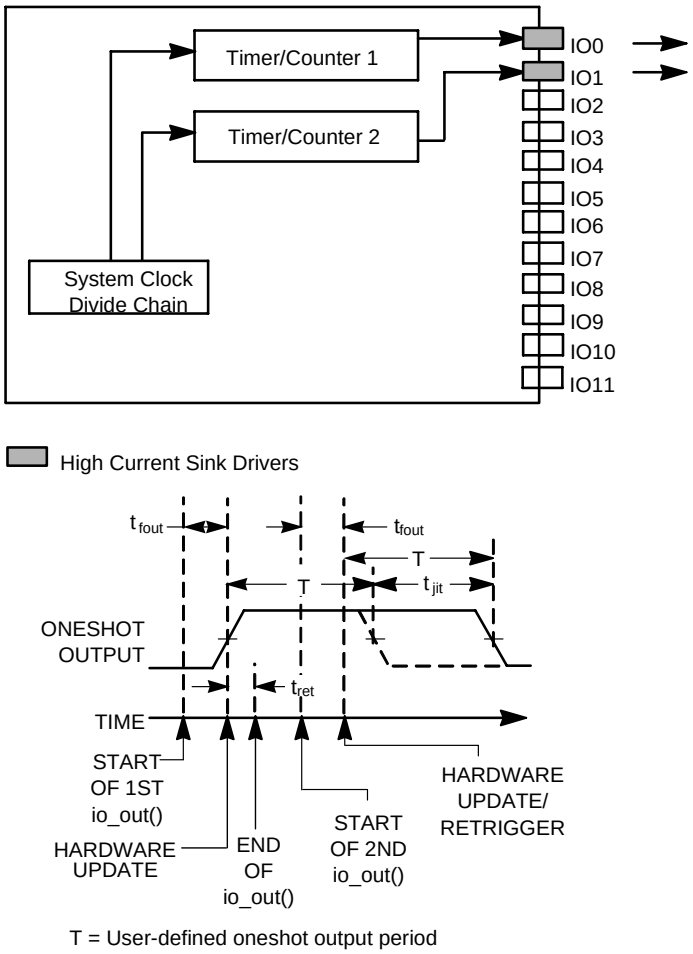


Figure 3.51 Infrared Pattern I/O

Oneshot Output

A timer/counter can be configured to generate a single pulse of programmable duration. The asserted state can be either logic high or logic low. Retriggering the oneshot before the end of the pulse causes it to continue for the new duration. Table 3.8 in the *Notes* section at the end of this chapter gives the resolution and maximum time of the pulse for various clock selections. This object is useful for generating a time delay without intervention of the application processor (see Figure 3.52).



Symbol	Description	Typ @ 10MHz	Max
t_{fout}	Function call to output update	96 µs	—
t_{ret}	Return from function	13 µs	—
t_{jit}	Output duration jitter	—	1 timer/counter clock period*

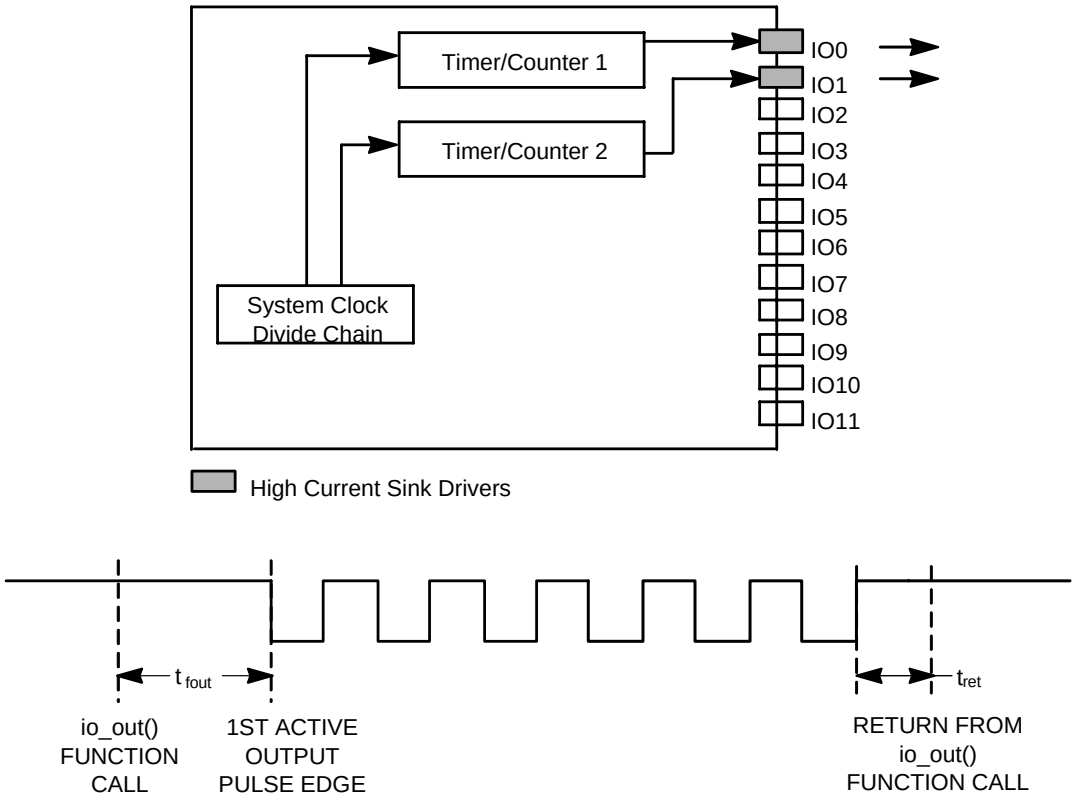
Figure 3.52 Oneshot Output Latency Values

*Timer/counter clock period = (2000ns * 2^(clock))/(input clock in MHz).

While the output is still active, a subsequent call to this function will cause the update to take effect immediately, extending the current cycle. This is, therefore, a retriggerable oneshot function.

Pulsecount Output

A timer/counter can be configured to generate a series of pulses. The number of pulses output is in the range 0 to 65,535, and the output waveform is a square wave of 50% duty cycle. This function suspends application processing until the pulse train is complete. The frequency of the waveform can be one of eight values given by Table 3.9 in the *Notes* section at the end of this chapter with clock select values of 0 through 7. This object is useful for external counting devices that can accumulate pulse trains, such as stepper motors (see Figure 3.53).



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to first active output pulse edge	115 µs
t_{ret}	Return from function	5 µs

Figure 3.53 Pulsecount Output

The return from this function does not occur until all output pulses have been produced.

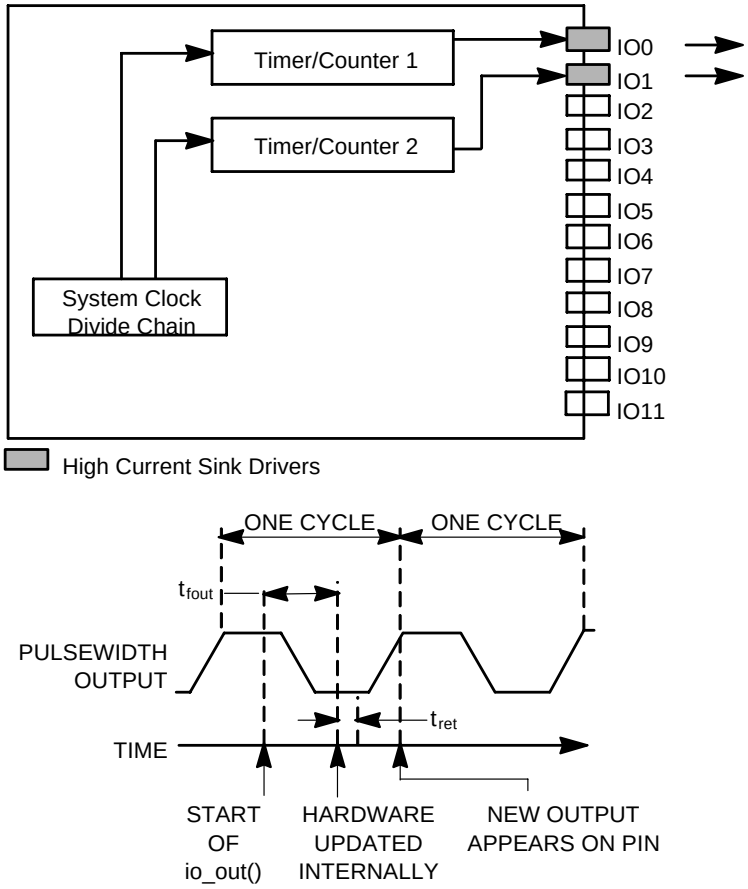
t_{fout} is the time from function call to first output pulse. Therefore, the calling of this function ties up the application processor for a period of N x (pulse period) + t_{fout} + t_{ret}, where N is the number of specified output pulses.

The polarity of the output depends on whether or not the **`invert`** option was used in the declaration of the function block. The default is low with high pulses.

Pulsewidth Output

A timer/counter can be configured to generate a pulsewidth modulated repeating waveform. In pulsewidth short function, the duty cycle ranges from 0% to 100% (0/256 to 255/256) of a cycle in steps of about 0.4% (1/256). The frequency of the waveform can be one of eight values given by Table 3.9.

In pulsewidth long function, the duty cycle ranges from 0% to almost 100% (0/65,536 to 65,535/65,536) of a cycle in steps of 15.25 ppm (1/65,536). The frequency of the waveform can be one of eight values given by Table 3.10 in the *Notes* section at the end of this chapter. The asserted state of the waveform can be either logic high or logic low. Writing a new pulsewidth value to the device takes effect at the end of the current cycle. A pulsewidth modulated signal provides a simple means of digital-to-analog conversion (see Figure 3.54).



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to output update	101 µs
t_{ret}	Return from function	13 µs

Figure 3.54 Pulsewidth Output Latency Values

The new output value will not take effect until the end of the current cycle. There are two exceptions to this rule. If the output is disabled, the new (non-zero) output will start immediately after t_{fout}. Also, for a new output value of zero, the output is disabled immediately and not at the end of the current cycle.

A disabled output is a logic 0 by default unless the **`invert`** keyword is used in the I/O object declaration.

Triac Output

On the PL Smart Transceiver, a timer/counter can be configured to control the delay of an output signal with respect to a synchronization input. This synchronization can occur on the rising edge, the falling edge, or both the rising and falling edges of the input signal. For control of AC circuits using a triac device, the sync input is typically a zero-crossing signal, and the pulse output is the triac trigger signal. Table 3.8 shows the resolution and maximum range of the delay (see Figure 3.55).

The output gate pulse is gated by an internal clock with a constant period of 25.6µs at 10MHz (39.062µs at 6.5536MHz). because the input trigger signal (zero crossing) is asynchronous relative to this internal clock, there is a jitter, t_{jit}, associated with the output gate pulse.

The actual active edge of the sync input and the triac gate output can be set by using the **`clockedge`** or **`invert`** parameters, respectively.

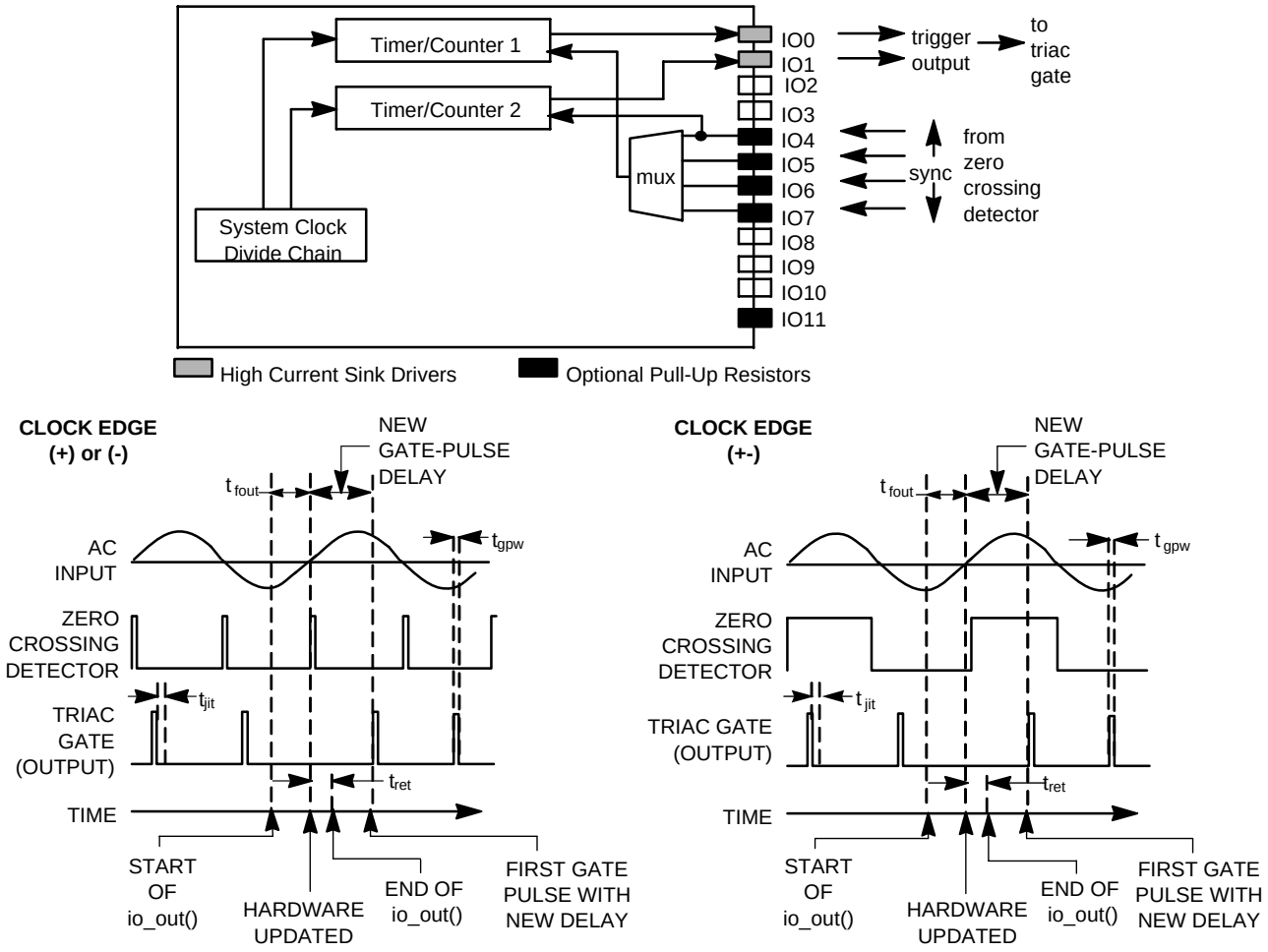


Figure 3.55 Triac Output Latency Values

The hardware update does not happen until the occurrence of an external active sync clock edge. The internal timer is then enabled and a triac gate pulse is generated after the user-defined period has elapsed. This sequence is repeated indefinitely until another update is made to the triac gate pulse delay value.

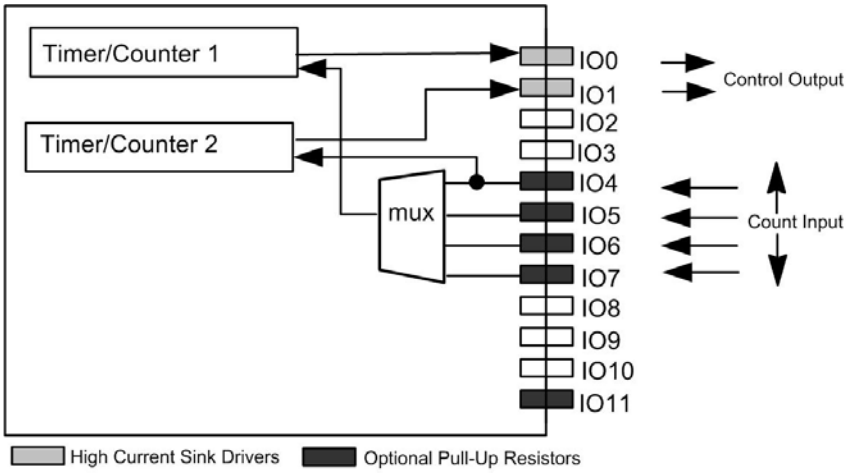
t_{fout} (min) refers to the delay from the initiation of the function call to the first sampling of the sync input. In the absence of an active sync clock edge, the input is repeatedly sampled for 10ms (1/2 wave of a 50Hz line cycle time), t_{fout} (max), during which the application processor is suspended.

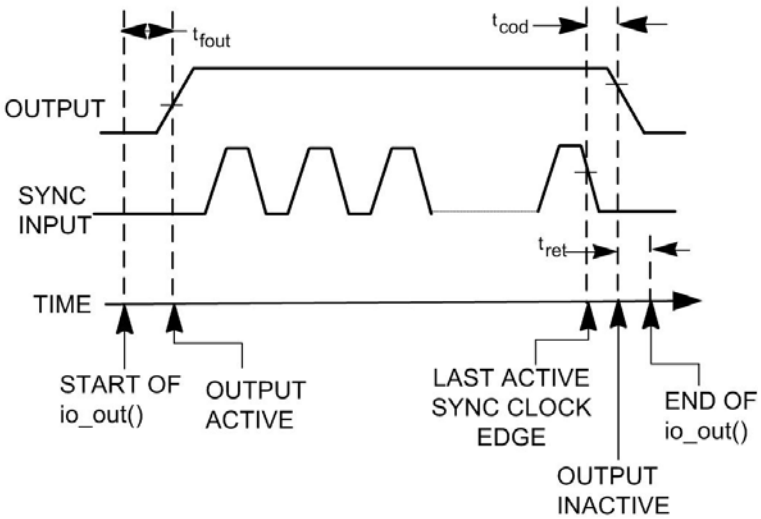
The output gate pulse is gated by an internal clock with a constant period of 25.6µs at 10MHz (39.062µs at 6.5536MHz). because the input trigger signal (zero crossing) is asynchronous relative to this internal clock, there is a jitter, t_{jit}, associated with the output gate pulse.

The actual active edge of the sync input and the triac gate output can be set by using the `clockedge` or `invert` parameters, respectively.

Triggered Count Output

A timer/counter can be configured to generate an output pulse that is asserted under program control, and de-asserted when a programmable number of input edges (up to 65,535) has been counted on an input pin (IO4 – IO7). Assertion can be either logic high or logic low. This object is useful for controlling stepper motors or positioning actuators which provide position feedback in the form of a pulse train. The drive to the external device is enabled until it has moved the required distance, and then the device is disabled (see Figure 3.56).





Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to output pulse	109 µs
t_{cod}	Last negative sync Clock edge to output inactive	min 550 ns max 750 ns
t_{ret}	Return from function	7 µs

Figure 3.56 Triggered Count Output Latency Values

The active output level depends on whether or not the **`invert`** option was used in the declaration of the function block. The default is high.

Notes

Various combinations of I/O pins can be configured as basic inputs or outputs. The application program can optionally specify the initial values of basic outputs. Pins configured as outputs can also be read as inputs, returning the value last written.

The gradient behavior of the timing numbers for different PL Smart Transceiver pins for some of the I/O objects is due to the shift-and-mask operation performed by the Neuron firmware.

For dualslope input, edgelog input, ontime input, and period input, the timer/counter returns a value (or a table of values, in the case of edgelog input) in the range 0 to 65,535, representing elapsed times from 0 up to the maximum range given in Table 3.8.

For ontime input, period input, dualslope, edgelog, and infrared; the timer/counter returns a number in the range 0 to 65,535, representing elapsed times from 0 up to the maximum range given in Table 3.8.

For oneshot output, frequency output, and triac output; the timer/counter can be programmed with a number in the range 0 to 65,535. This number represents the waveform ontime for oneshot output, the waveform period for frequency output, and the control period from sync input to pulse/level output for the triac output. Table 3.8 gives the range and resolution for these timer/counter objects at 10MHz. The clock select value is specified in the declaration of the I/O object in the Neuron C application program, and can be modified at runtime.

Table 3.8 Timer/Counter Resolution and Maximum Range

	Oneshot and Triac Outputs; Dualslope, Edgelog, Ontime, and Period Inputs		**Frequency Output**	
Clock Select	**Resolution (µs)**	**Maximum Range (ms)**	**Resolution (µs)**	**Maximum Range (ms)**
0	0.2	13.1	0.4	26.2
1	0.4	26.2	0.8	52.4
2	0.8	52.4	1.6	105
3	1.6	105	3.2	210
4	3.2	210	6.4	419
5	6.4	419	12.8	838
6	12.8	839	25.6	1,678
7	25.6	1,678	51.2	3,355

Note: This table is for a 10MHz input clock. Scale appropriately for other clock rates:
Resolution (µs) = $2^{(\text{Clock Select} + n)}$/(Input Clock in MHz)
Maximum Range (µs) = 65535 x Resolution (µs) x n
n = 1 for oneshot and triac output, and dualslope, edgelog, ontime, and period input
n = 2 for frequency output.

For pulsewidth short output and pulsecount output, Table 3.9 gives the possible choices for pulsetrain repetition frequencies. Pulsecount can not be used with clock select 0.

Table 3.9 Timer/Counter Square Wave Output

Clock Select (System Clock ÷)	Repetition Rate (Hz)	Repetition Period (µs)	Resolution of Pulse (µs)
0 (÷1) (5MHz)	19,531	51.2	0.2
1 (÷ 2) (2.5MHz)	9,766	102.4	0.4
2 (÷ 4) (1.25MHz)	4,883	204.8	0.8
3 (÷ 8) (625 kHz)	2,441	409.6	1.6
4 (÷ 16) (312.5 kHz)	1,221	819.2	3.2
5 (÷ 32) (156.25 kHz)	610	1,638.4	6.4
6 (÷ 64) (78.125 kHz)	305	3,276.8	12.8
7 (÷ 128) (39.06 kHz)	153	6,553.6	25.6

This table is for 10MHz input clock. Scale appropriately for other clock rates:
Period (µs) = 512 x $2^{\text{Clock Select}}$ / (Input Clock in MHz)
Frequency (Hz) = 1,000,000 / Period (µs).

For pulsewidth long output, the table below gives the possible choices for pulsetrain repetition frequencies.

Table 3.10 Timer/Counter Pulsetrain Output

Clock Select	Frequency (Hz)	Period (ms)
0	76.3	13.1
1	38.1	26.2
2	19.1	52.4
3	9.54	105
4	4.77	210
5	2.38	419
6	1.19	839
7	0.60	1,678

This table is for 10MHz input clock. Scale appropriately for other clock rates:
Period (ms) = 131.072 x $2^{\text{Clock Select}}$ / (Input Clock in MHz)
Frequency (Hz) = 1,000 / Period (ms)

As with all CMOS devices, floating I/O pins can cause excessive current consumption. To avoid this, declare all unused I/O pins as bit output. Alternatively, unused I/O pins can be connected to + V_{DD5} or GND.

Chapter 4

Coupling Circuits

Introduction

This chapter includes example coupling circuits that address most application requirements. For those who wish to understand the background behind coupling circuit design, a tutorial covering the design principles follows the detailed example circuits.

Recommended Coupling Circuits

This section provides schematics and component information for coupling the PL Smart Transceiver to the power mains. The schematics are divided into classes based on coupling type, isolation and application. Table 4.1 provides a summary which can be used as a guide to determine the appropriate coupling circuit for a given application.

For each schematic the required component specifications and example suppliers/part numbers are provided. Vendor part number information is provided as a way to reduce component selection times - because the data sheets for the suggested parts have already been checked to confirm that the published specifications for these parts meet all of the required specifications. Alternate component suppliers can be used provided that ***all*** of the required specifications listed for each component are met. While line surge testing must be performed for every new product design, using the first vendor/part number listed for each component in the tables has the additional advantage that they were the parts used by Echelon for surge verification.

Table 4.1 Coupling Circuit Selection Guide

Example	Connection Type	Line Voltage	Isolated/ Non-Isolated	Freq. Band	Typical Application(s)	Page
1	1-Phase L-N	≤240VAC/DC	Non-Isolated	C	Consumer, residential devices world-wide, Commercial devices in CENELEC countries	108
				A	Electric utility meters world-wide	
2	1-Phase L-N	≤240VAC/DC	Isolated	C	Consumer residential devices world-wide, Commercial devices in CENELEC countries	110
				A	Utility devices world-wide	
3	1-Phase L-E	100-277VAC	Non-Isolated	C	Commercial devices in North America	112
4	1-Phase L-E	100-277VAC	Isolated	C	Commercial devices in North America	114
5	3-Phase	100-277VAC	Non-Isolated	C	Commercial panel devices world-wide	116
				A	3-Phase utility devices world-wide	
6	3-Phase	100-277VAC	Isolated	C	Commercial panel devices world-wide	118
				A	3-Phase utility devices world-wide	
7	1-Phase L-N Floating	≤240VAC/DC	Non-Isolated	C	Consumer, residential devices world-wide, Commercial devices in CENELEC countries	120
				A	Utility devices world-wide	
8	Power Supply Plus Coupler	90-240VAC	Isolated	C	Consumer, residential devices world-wide, Commercial devices in CENELEC countries	122
9	Low-Volt AC	≤48Vpk	Non-Isolated	C	HVAC and irrigation devices world-wide	124
10	Low-Volt AC	≤48Vpk	Isolated	C	HVAC and irrigation devices world-wide	126
11	Low-Volt DC	≤48Vpk	Non-Isolated	C	Automotive wiring world-wide	128
12	Retired				N/A	
13	Long-Haul	≤240VAC/DC	Isolated	C	300m-20km dedicated lines world-wide	See *Note*
14	Current-loop	N/A	Isolated	C	Airport lighting devices world-wide	See *Note*
15	1 or 2 of 3-Phase L-E	100–240VAC	Isolated	C	Commercial devices in North America	See *Note*
16	UL 197 L-E	100–240VAC	Isolated	C	Commercial cooking equipment in North America	See *Note*

Note: Contact the Echelon LonSupport™ group for additional information on this coupling circuit.

Example 1. Line-to-Neutral, Non-Isolated Coupling Circuit

Figure 4.1 presents a schematic for a line-to-neutral (L-N), non-isolated mains coupling circuit. Table 4.2 lists component values and example suppliers/part numbers for coupling to the AC mains with a nominal line voltage of ≤240VAC. This schematic can also be used for coupling to wiring other than AC mains with AC or DC voltages of $250V_{RMS}$ or less.

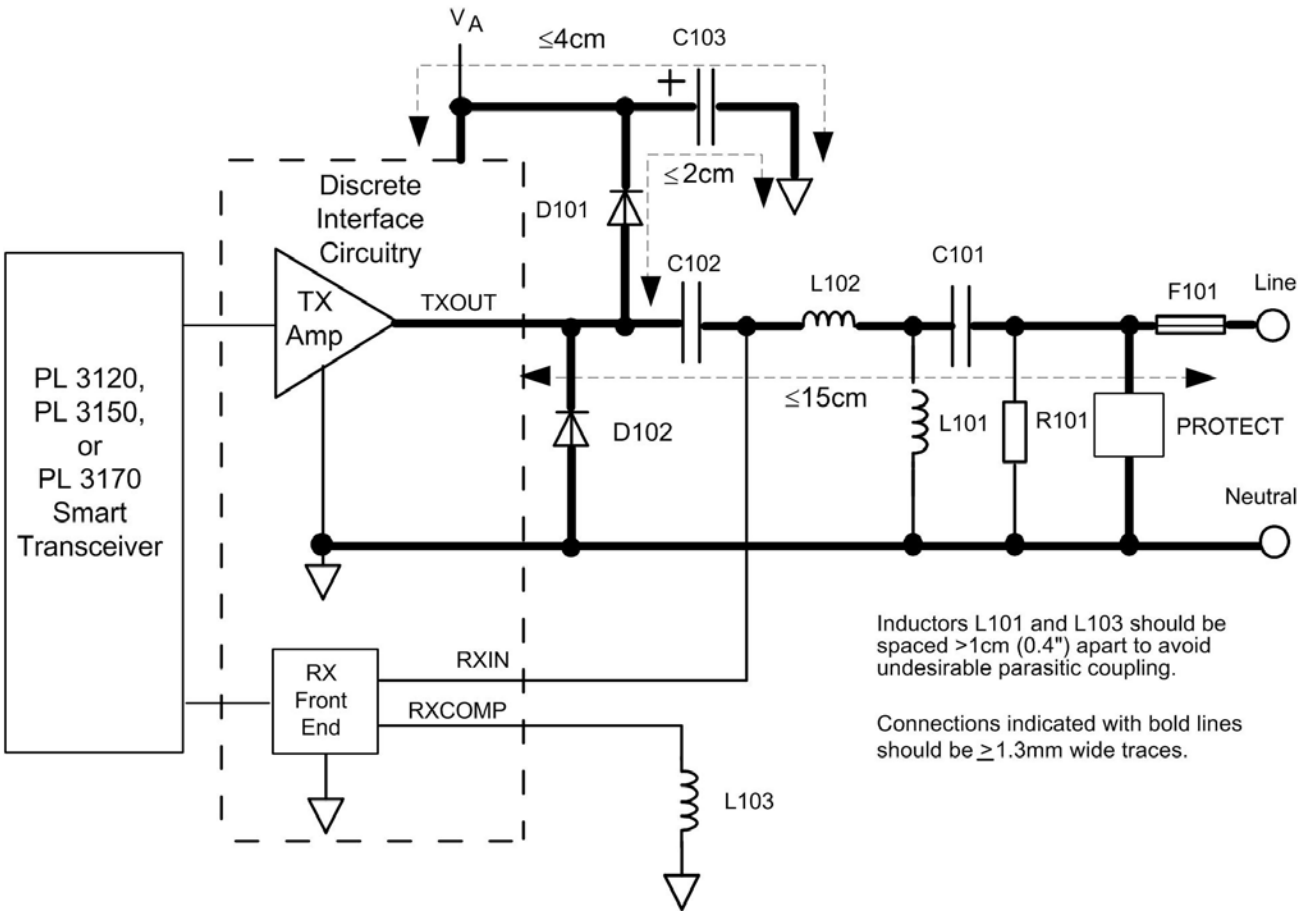


Figure 4.1 Line-to-Neutral, Non-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Joyin** www.joyin.com.tw
ACT www.act1.com	**Nichicon** www.nichicon-us.com
AID Electronics www.aid.com.tw	**ON Semiconductor** www.onsemi.com
Arcotronics www.arcotronics.us	**Panasonic** www.panasonic.com/industrial/components
Fairchild Semiconductor www.fairchildsemi.com	**Shinhom** www.shinhom.com
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Taiyo Yuden** www.ty-top.com
Hollyfuse www.hollyfuse.com	**Vishay** www.vishay.com
Illinois Capacitor www.illinoiscapacitor.com	**Wickmannn** www.littlefuse.com/cgibin/r.cgi/en/brand_Wickmannn.html

Table 4.2 ≤240VAC Line-to-Neutral, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C101	0.15µF	0.10µF	±10%, ≥250VAC, X2 type (1)	IllinoisCap/154MKP275KB AID Electronics/ MEX154K275AC	IllinoisCap/104MKP275K AID Electronics/ MEX104K275AC
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
F101	6A or 6.3A	6A or 6.3A	For indoor branch circuit or power entry use, 250VAC, time-lag (1), (2)	Wickmann/3741630041 Hollyfuse/5RT-063H	Wickmann/3741630041 Hollyfuse/5RT-063H
	10A	10A	For outdoor use, 250VAC, time-lag (2)	Wickmann/3742100041	Wickmann/3742100041
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K
L102	27µH	12µH	±10%, Imax ≥700mA, R_{DC} ≤0.25Ω	Taiyo Yuden/ LHL08TB270K Abracon/AIAP-01-270K Shinhom/LGA0512-270K	Taiyo Yuden/ LHL08TB120K Abracon/AIAP-01-120K Shinhom/LGA0512-120K
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
R101	1MΩ	1MΩ	±5%, ≥1/4W, max working voltage ≥360VDC (1), (3)		
PROTECT	300VAC (470VDC)	300VAC (470VDC)	For indoor branch circuits, ≥1250A surge current, 8x20µs, 2 times	Panasonic/ERZ-V07D471 Joyin/JVR07S471K65	Panasonic/ERZ-V07D471 Joyin/JVR07S471K65
	300VAC (470VDC)	300VAC (470VDC)	For power entry, ≥4500A surge current, 8x20µs, 2 times	Panasonic/ERZ-V14D471 Joyin/JVR14S471K87	Panasonic/ERZ-V14D471 Joyin/JVR14S471K87
	300VAC (470VDC)	300VAC (470VDC)	For outdoor use, ≥6500A surge current, 8x20µs, 2 times	Panasonic/ERZ-V20D471 Joyin/JVR20S471K11	Panasonic/ERZ-V20D471 Joyin/JVR20S471K11

NOTES:

1. For nominal line voltages of 120VAC or less, the voltage rating on these parts can be lowered to reduce cost and space.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 510kΩ resistors in series, each with a working voltage rating of at least half of the value listed above.

Example 2. Line-to-Neutral, Transformer-Isolated Coupling Circuit

Figure 4.2 presents a schematic for a line-to-neutral (L-N), transformer-isolated coupling circuit. Table 4.3 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage of ≤240VAC. This schematic can also be used for coupling to wiring other than AC mains with AC or DC voltages of $250V_{RMS}$ or less or for coupling to an un-powered wire pair.

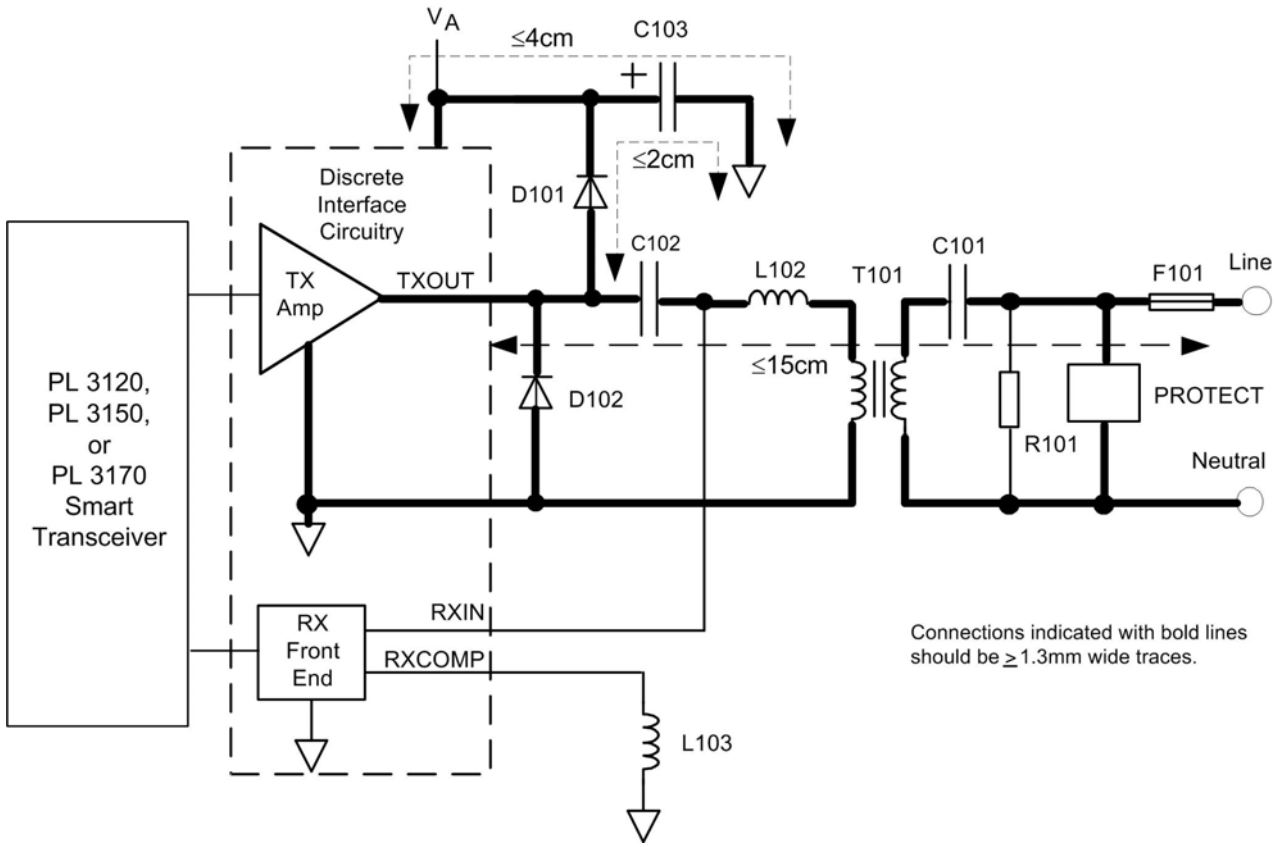


Figure 4.2 Line-to-Neutral, Transformer-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Joyin** www.joyin.com.tw
ACT www.act1.com	**Nichicon** www.nichicon-us.com
AID Electronics www.aid.com.tw	**ON Semiconductor** www.onsemi.com
Arcotronics www.arcotronics.us	**Panasonic** www.panasonic.com/industrial/components
Fairchild Semiconductor www.fairchildsemi.com	**Shinhom** www.shinhom.com
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Taiyo Yuden** www.ty-top.com
Hollyfuse www.hollyfuse.com	**Vishay** www.vishay.com
Illinois Capacitor www.illinoiscapacitor.com	**Wickmannn** www.littlefuse.com/cgibin/r.cgi/en/brand_Wickmannn.html

Table 4.3 Line-to Neutral, Transformer-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C101	0.15µF	0.10µF	±10%, ≥250VAC, X2 type (1)	IllinoisCap/154MKP275KB AID Electronics/ MEX154K275AC	IllinoisCap/104MKP275K AID Electronics/ MEX104K275AC
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
F101	6A or 6.3A	6A or 6.3A	For indoor branch circuit or power entry use, 250VAC, time-lag (1), (2)	Wickmann/3741630041 Hollyfuse/5RT-063H	Wickmann/3741630041 Hollyfuse/5RT-063H
	10A	10A	For outdoor use, 250VAC, time-lag (2)	Wickmann/3742100041	Wickmann/3742100041
L102	15µH	None	±10%, Imax ≥700mA, R_{DC} ≤0.20Ω	Taiyo Yuden/ LHL08TB150K Abracon/AIAP-01-150K Shinhom/LGA0512-150K	N/A
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
R101	1MΩ	1MΩ	±5%, ≥1/4W, max working voltage ≥360VDC (1), (3)		
PROTECT	300VAC (470VDC)	300VAC (470VDC)	For indoor branch circuits, ≥1250A surge current, 8x20µs, 2 times	Panasonic/ERZ-V07D471 Joyin/JVR07S471K65	Panasonic/ERZ-V07D471 Joyin/JVR07S471K65
	300VAC (470VDC)	300VAC (470VDC)	For power entry, ≥4500A surge current, 8x20µs, 2 times	Panasonic/ERZ-V14D471 Joyin/JVR14S471K87	Panasonic/ERZ-V14D471 Joyin/JVR14S471K87
	300VAC (470VDC)	300VAC (470VDC)	For outdoor use, ≥6500A surge current, 8x20µs, 2 times	Panasonic/ERZ-V20D471 Joyin/JVR20S471K11	Panasonic/ERZ-V20D471 Joyin/JVR20S471K11
T101	12uH-leakage transformer		See Appendix C	See Appendix C	See Appendix C

NOTES:

1. For nominal line voltages of 120VAC or less, the voltage rating on these parts can be lowered to reduce cost and space.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 510kΩ resistors in series, each with a working voltage rating of at least half of the value listed above.

Example 3. Line-to-Earth, Non-Isolated Coupling Circuit

Figure 4.3 presents a schematic for a line-to-earth, non-isolated mains coupling circuit. Table 4.4 lists component values and example suppliers/part numbers for coupling to the AC mains with a nominal line voltage in the range 100-277VAC.

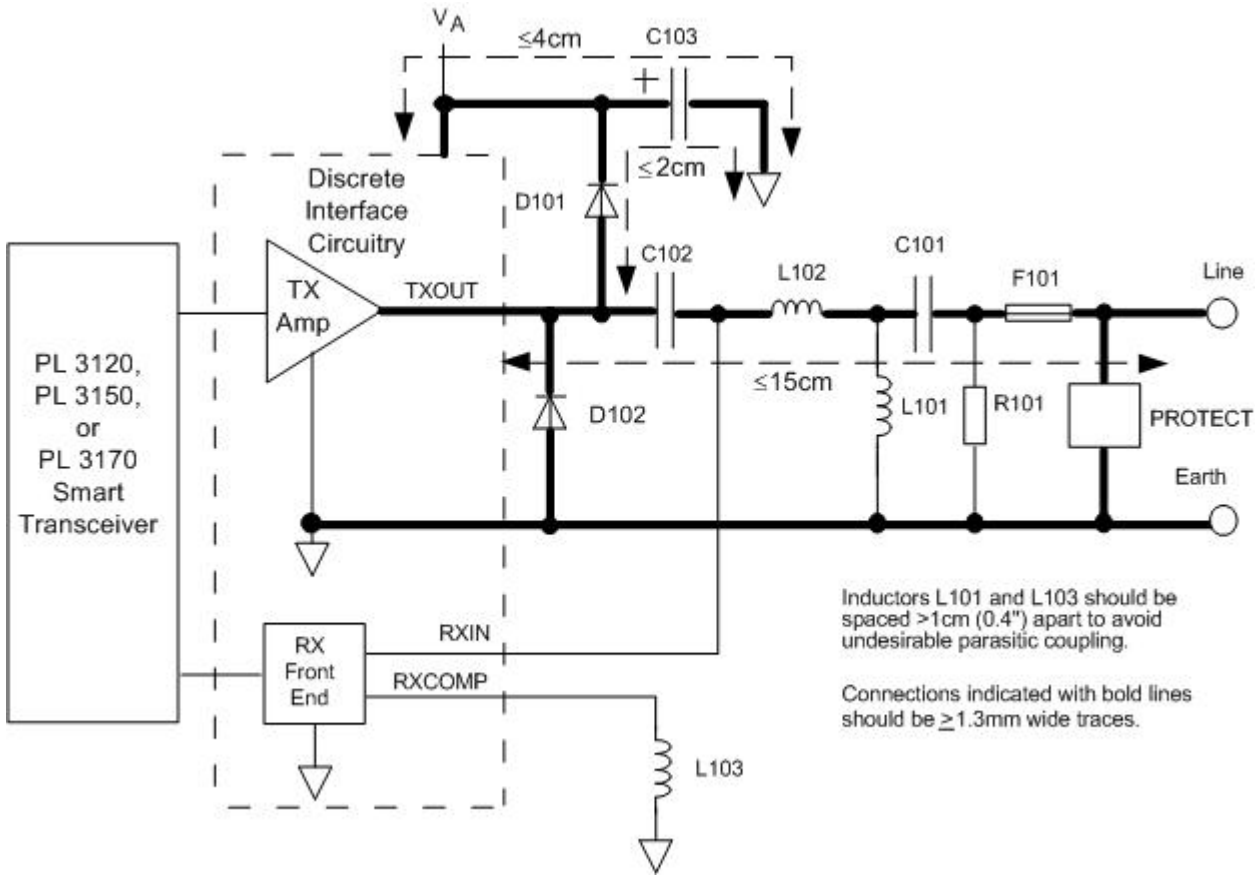


Figure 4.3 Line-to-Earth, Non-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Littlefuse** www.littlefuse.com
AID Electronics www.aid.com.tw	**Nichicon** www.nichicon-us.com
Arcotronics www.arcotronics.us	**ON Semiconductor** www.onsemi.com
Bel www.belfuse.com	**Panasonic** www.panasonic.com/industrial/components
Evox Rifa www.evox-rifa.com	**Shinhom** www.shinhom.com
Fairchild Semiconductor www.fairchildsemi.com	**Surge Components** www.surgecomponents.com
Fastron www.fastrongroup.com	**Taiyo Yuden** www.ty-top.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Vishay** www.vishay.com
Hollyfuse www.hollyfuse.com	**Wickmannn** www.littlefuse.com/cgibin/r.cgi/en/brand_Wickmannn.html
Illinois Capacitor www.illinoiscapacitor.com	

Table 4.4 Line-to-Earth Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	C-band 100-120VAC	C-band 200-277VAC		C-band 100-120VAC	C-band 200-277VAC
C101	0.068µF ≥120VAC	0.033µF ≥300VAC	±10%, X2 type (1)	IllinoisCap/683MKP275KB AID Electronics/ MEX683K275AC	Evox-Rifa/ PHE840EA5330KA02
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
F101	6A or 6.3A ≥120VAC	6A or 6.3A ≥277VAC	Time-lag, (2)	Wickmann/3741630041 Hollyfuse/5RT-063H	Bel/MRT6.3
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K
L102	18µH	39µH	±10%, Imax ≥700mA, R_{DC} ≤0.30Ω	Taiyo Yuden/ LHL08TB180K Abracon/AIAP-01-180K Shinhom/LGA0512-180K	Taiyo Yuden/ LHL08TB390K Abracon/AIAP-01-390K Shinhom/LGA0512-390K
L103	820µH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
R101	10MΩ ≥200VDC	10MΩ ≥450VDC	±5%, ≥1/4W, (3)		
PROTECT	N/A	N/A	For indoor branch circuits no component is required	N/A	N/A
	120VAC	300VAC	Power entry - use AC gas discharge tube (4)	Littlefuse/AC240L	
	120VAC	300VAC	Outdoor - use AC gas discharge tube (4)	Littlefuse/AC240L	

NOTES:

1. An X2 capacitor is required for adequate surge immunity in branch circuit applications.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 5.1MΩ resistors in series, each with a working voltage rating of at least 1/2 of the value listed above. Also, peak power and voltage ratings of R101 must be chosen to meet the high-pot testing requirements of the application.
4. High-pot manufacturing tests must be performed prior to installation of this gas discharge tube. High-pot testing between line and earth is usually performed at voltages above the gas tube arc-over voltage, and the test will fail if the gas tube arcs during testing. In addition, a DC high-pot tester must be used to avoid excess current flow through C101.

Example 4. Line-to-Earth, Transformer-Isolated Coupling Circuit

Figure 4.4 presents a schematic for a line-to-earth, transformer-isolated coupling circuit. Table 4.5 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-277VAC.

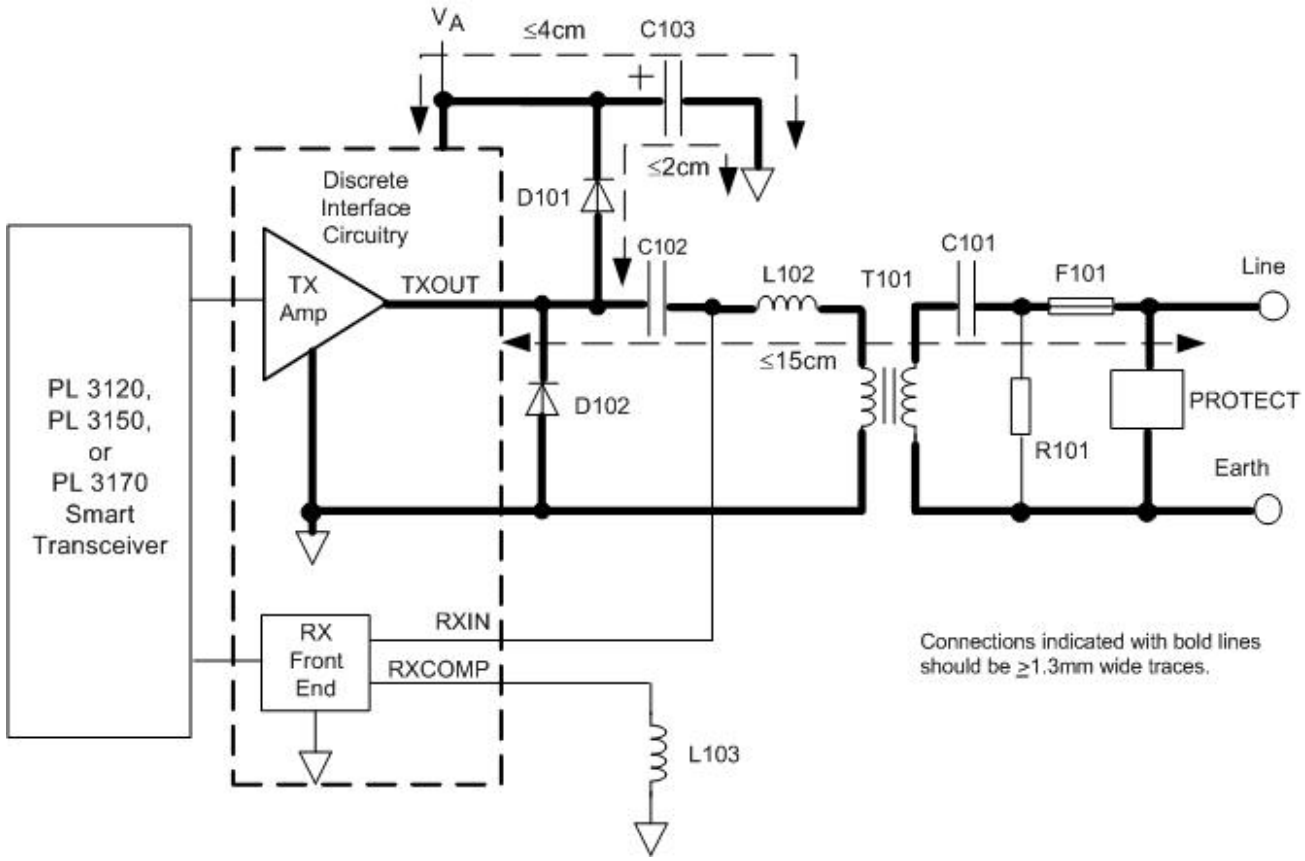


Figure 4.4 Line-to-Earth, Transformer-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Illinois Capacitor** www.illinoiscapacitor.com
AID Electronics www.aid.com.tw	**Littlefuse** www.littlefuse.com
Arcotronics www.arcotronics.us	**Nichicon** www.nichicon-us.com
Bel www.belfuse.com	**ON Semiconductor** www.onsemi.com
CTC Coils www.ctccoils.com/eng/index.htm	**Panasonic** www.panasonic.com/industrial/components
Evox Rifa www.evox-rifa.com	**Shinhom** www.shinhom.com
Fairchild Semiconductor www.fairchildsemi.com	**Surge Components** www.surgecomponents.com
Fastron www.fastrongroup.com	**Taiyo Yuden** www.ty-top.com

Table 4.5 Line-to-Earth, Transformer-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	C-band 100-120VAC	C-band 200-277VAC		C-band 100-120VAC	C-band 200-277VAC
C101	0.068µF ≥120VAC	0.033µF ≥300VAC	±10%, X2 type (1)	IllinoisCap/683MKP275KB AID Electronics/ MEX683K275AC	Evox-Rifa/ PHE840EA5330KA02
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
F101	6A or 6.3A ≥120VAC	6A or 6.3A ≥277VAC	Time-lag, (2)	Wickmann/3741630041 Hollyfuse/5RT-063H	Bel/MRT6.3
L102	5.6µH	27µH	±10%, Imax ≥700mA, R_{DC} ≤0.25Ω	Abracon/AIAP-01-5R6K Shinhom/LGA0512-5R6K CTC Coils/ EC385R6K-506409-T	Taiyo Yuden/ LHL08TB270K Abracon/AIAP-01-270K Shinhom/LGA0512-270K
L103	820µH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
R101	10MΩ ≥200VDC	10MΩ ≥450VDC	±5%, ≥1/4W, (3)		
PROTECT	N/A	N/A	For indoor branch circuits no component is required	N/A	N/A
	120VAC	300VAC	Power entry - use AC gas discharge tube (4)	Littlefuse/AC240L	
	120VAC	300VAC	Outdoor - use AC gas discharge tube (4)	Littlefuse/AC240L	
T101	12uH-leakage transformer		See Appendix C	See Appendix C	See Appendix C

NOTES:

1. An X2 capacitor is required for adequate surge immunity in branch circuit applications.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 5.1MΩ resistors in series, each with a working voltage rating of at least 1/2 of the value listed above. Also peak power and voltage ratings of R101 must be chosen to meet the high-pot testing requirements of the application.
4. High-pot manufacturing tests must be performed prior to installation of this gas discharge tube. High-pot testing between line and earth is usually performed at voltages above the gas tube arc-over voltage, and the test will fail if the gas tube arcs during testing. In addition, a DC high-pot tester must be used to avoid excess current flow through C101.

Example 5. 3-Phase, Non-Isolated Coupling Circuit

Figure 4.5 presents a schematic for a non-isolated 3-phase coupling circuit. Table 4.6 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-277VAC.

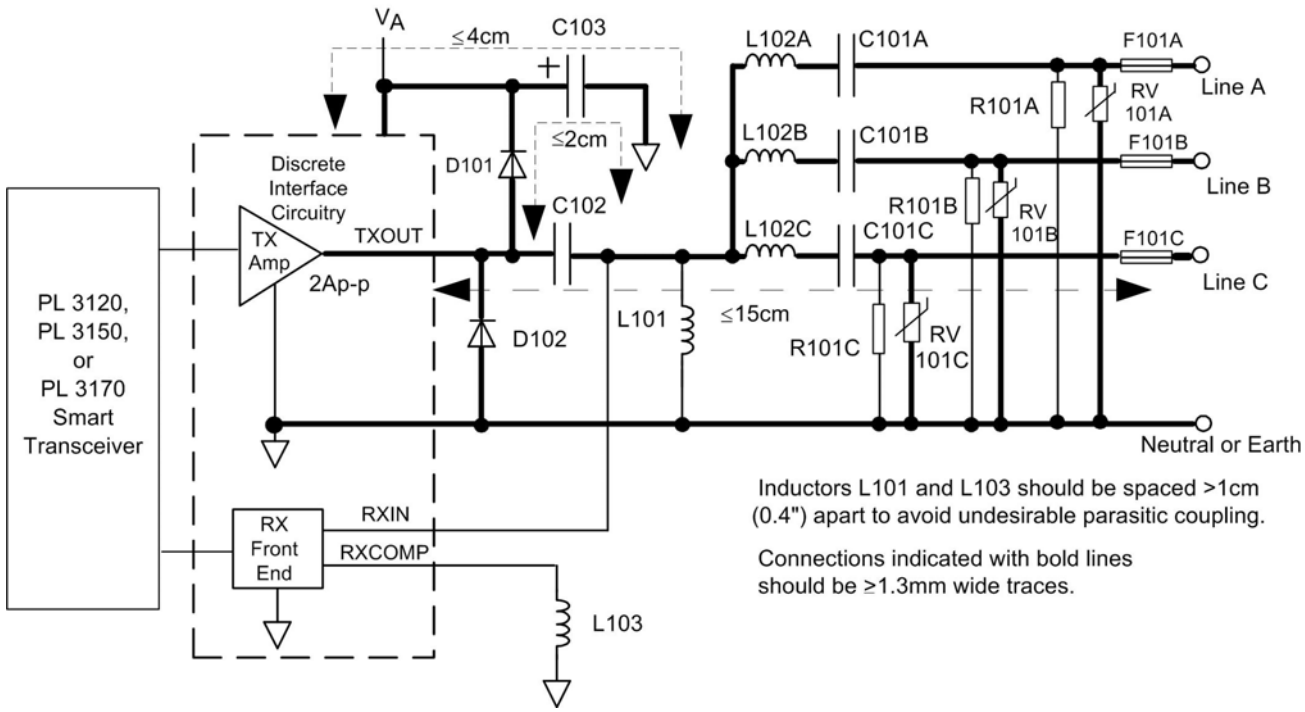


Figure 4.5 3-Phase, Non-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Joyin** www.joyin.com.tw
ACT www.act1.com	**Nichicon** www.nichicon-us.com
AID Electronics www.aid.com.tw	**ON Semiconductor** www.onsemi.com
CTC Coils www.ctccoils.com/eng/index.htm	**Panasonic** www.panasonic.com/industrial/components
Fairchild Semiconductor www.fairchildsemi.com	**Shinhom** www.shinhom.com
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Taiyo Yuden** www.ty-top.com
Hollyfuse www.hollyfuse.com	**Vishay** www.vishay.com
Illinois Capacitor www.illinoiscapacitor.com	**Wickmannn** www.littlefuse.com/cgibin/r.cgi/en/brand_Wickmannn.html

Table 4.6 100-277 VAC, 3-Phase, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C101A-C	0.15µF	0.10µF	±10%, ≥250VAC, X2 type (1)	IllinoisCap/154MKP275KB AID Electronics/ MEX154K275AC	IllinoisCap/104MKP275K AID Electronics/ MEX104K275AC
C102	1.0µF	1.0µF	±10%, ≥250VDC, metallized film	Panasonic/ECQ-E2105KB Surge Components/ SRMA250V105K	Panasonic/ECQ-E2105KB Surge Components/ SRMA250V105K
C103	≥220µF	≥220µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.16Ω ESR @100kHz/20C, ≥550mA$_{RMS}$ ripple current @105C	Nichicon/UHE1E221MPD Fenghua/ 8221LDM0812LY	Nichicon/UHE1E221MPD Fenghua/ 8221LDM0812LY
D101, D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
F101A-C	6A or 6.3A	6A or 6.3A	For indoor use, 250VAC, time-lag (1), (2)	Wickmann/3741630041 Hollyfuse/5RT-063H	Wickmann/3741630041 Hollyfuse/5RT-063H
	10A	10A	For outdoor use, 250VAC, time-lag (1)	Wickmann/3742100041	Wickmann/3742100041
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K
L102A-C	27µH	18µH	±10%, Imax ≥1.5A, R_{DC} ≤0.15Ω	Taiyo Yuden/ LHL08TB270K Shinhom/LCHB0810270K CTC Coils/ CH6080270K-542318-B	Taiyo Yuden/ LHL08TB180K Shinhom/LCHB0810180K CTC Coils/ CH6080180K-542316-B
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
R101A-C	1MΩ	1MΩ	±5%, ≥1/4W, max working voltage ≥600VDC (1), (3)		
RV101A-C	510VAC (820VDC)	510VAC (820VDC)	For indoor use, ≥4500A surge current, 8x20µs, 2 times (4)	Panasonic/ERZ-V14D821 Joyin/JVR14S821K87	Panasonic/ERZ-V14D821 Joyin/JVR14S821K87
	510VAC (820VDC)	510VAC (820VDC)	For outdoor use, ≥6500A surge current, 8x20µs, 2 times (4)	Panasonic/ERZ-V20D821 Joyin/JVR20S821K11	Panasonic/ERZ-V20D821 Joyin/JVR20S821K11

NOTES:

1. For 277VAC nominal line voltage operation, the voltage rating of these components must be increased.
2. In some applications, fuses might not be required. Consult applicable safety standards.
3. The voltage rating of R101A-C can be achieved by using two 510kΩ resistors in series, each with a working voltage rating of at least half of the value listed above. For earth-return coupling, the peak power and peak voltage ratings of R101A-C must be chosen to meet high-pot testing requirements of the application.
4. The voltage rating indicated is necessary to prevent damage to the varistor should the neutral (or earth) connection be lost while all three phases are connected and live. For earth-return coupling, high-pot testing must be performed prior to installation of these varistors. High-pot testing between line and earth is usually performed at voltages above the varistor clamp voltage, and the test will fail if the varistors clamp during testing. In addition, a DC high-pot tester must be used to avoid excess current flow through C101.

Example 6. 3-Phase, Transformer-Isolated Coupling Circuit

Figure 4.6 presents a schematic for a transformer-isolated 3-phase coupling circuit. Table 4.7 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-277VAC.

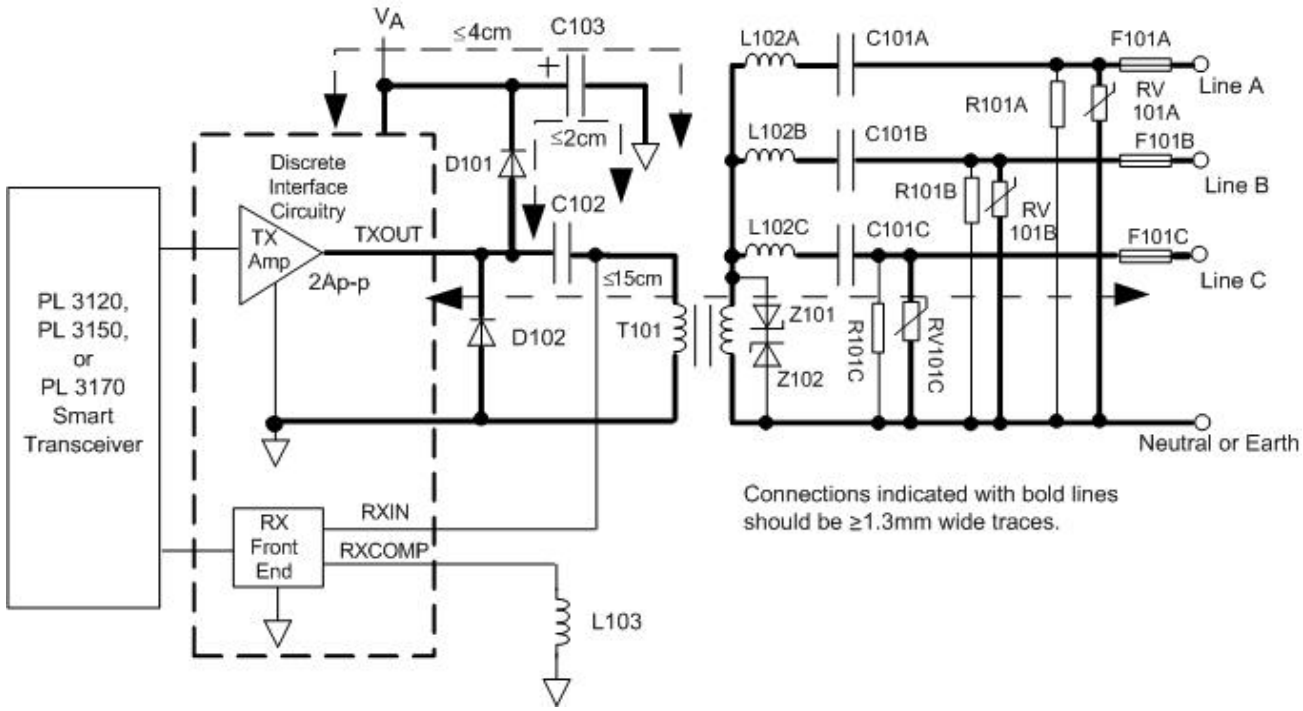


Figure 4.6 3-Phase, Transformer-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Joyin** www.joyin.com.tw
ACT www.act1.com	**MCC** www.mccsemi.com
AID Electronics www.aid.com.tw	**Nichicon** www.nichicon-us.com
Arcotronics www.arcotronics.us	**ON Semiconductor** www.onsemi.com
CTC Coils www.ctccoils.com/eng/index.htm	**Panasonic** www.panasonic.com/industrial/components
Fairchild Semiconductor www.fairchildsemi.com	**Shinhom** www.shinhom.com
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Taiyo Yuden** www.ty-top.com
Hollyfuse www.hollyfuse.com	**Vishay** www.vishay.com
Illinois Capacitor www.illinoiscapacitor.com	**Wickmannn** www.littlefuse.com/cgibin/r.cgi/en/brand_Wickmannn.html

Table 4.7 3-Phase, Transformer-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C101A-C	0.15µF	0.10µF	±10%, ≥250VAC, X2 type (1)	IllinoisCap/154MKP275KB AID Electronics/ MEX154K275AC	IllinoisCap/104MKP275K AID Electronics/ MEX104K275AC
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥220µF	≥220µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.16Ω ESR @100kHz/20C, ≥550mA$_{RMS}$ ripple current @105C	Nichicon/UHE1E221MPD Fenghua/ 8221LDM0812LY	Nichicon/UHE1E221MPD Fenghua/ 8221LDM0812LY
D101, D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
F101A-C	6A or 6.3A	6A or 6.3A	For indoor use, 250VAC, time-lag (1), (2)	Wickmann/3741630041 Hollyfuse/5RT-063H	Wickmann/3741630041 Hollyfuse/5RT-063H
	10A	10A	For outdoor use, 250VAC, time-lag (1)	Wickmann/3742100041	Wickmann/3742100041
L102A-C	27µH	18µH	±10%, Imax ≥1.5A, R_{DC} ≤0.10Ω	Taiyo Yuden/ LHL08TB270K Shinhom/LCHB0810270K CTC Coils/ CH6080270K-542318-B	Taiyo Yuden/ LHL08TB180K Shinhom/LCHB0810180K CTC Coils/ CH6080180K-542316-B
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
Z101, Z102	7.5V	7.5V	±5%,, 5W, Zener	OnSemi/1N53443BRLG MCC/1N5343B	OnSemi/1N53443BRLG MCC/1N5343B
R101A-C	1MΩ	1MΩ	±5%, ≥1/4W, max working voltage ≥600VDC (1), (3)		
RV101A-C	510VAC (820VDC)	510VAC (820VDC)	For indoor use, ≥4500A surge current, 8x20µs, 2 times (4)	Panasonic/ERZ-V14D821 Joyin/JVR14S821K87	Panasonic/ERZ-V14D821 Joyin/JVR14S821K87
	510VAC (820VDC)	510VAC (820VDC)	For outdoor use, ≥6500A surge current, 8x20µs, 2 times (4)	Panasonic/ERZ-V20D821 Joyin/JVR20S821K11	Panasonic/ERZ-V20D821 Joyin/JVR20S821K11
T101	Low-leakage transformer		See Appendix C	See Appendix C	See Appendix C

NOTES:

1. For 277VAC nominal line voltage operation, the voltage rating of these components must be increased.
2. In some applications, fuses might not be required. Consult applicable safety standards.
3. The working voltage rating of R101A-C can be achieved by using two 510kΩ resistors in series, each with a working voltage rating of at least half of the value listed above. For earth return coupling, the peak power and peak voltage ratings of R101A-C must be chosen to meet high-pot testing requirements of the application.
4. The voltage rating indicated is necessary to prevent damage to the varistor should the neutral (or earth) connection be lost while all three phases are connected and live. For earth-return coupling, high-pot testing must be performed prior to installation of these varistors. High-pot testing between line and earth is usually performed at voltages above the varistor clamp voltage, and the test will fail if the varistors clamp during testing. In addition, a DC high-pot tester must be used to avoid excess current flow through C101.

Example 7. Line-to-Neutral, Non-Isolated Floating Coupling Circuit

Figure 4.7 presents a schematic for a line-to-neutral (L-N), non-isolated mains coupling circuit that can be used in con conjunction with full-wave rectified non-isolated power supply based devices. Refer to the section later in this chapter titled *Non-isolated Floating Coupling Circuits* for more detailed application information. Table 4.8 lists component values and example suppliers/part numbers for coupling to the AC mains with a nominal line voltage of ≤240VAC.

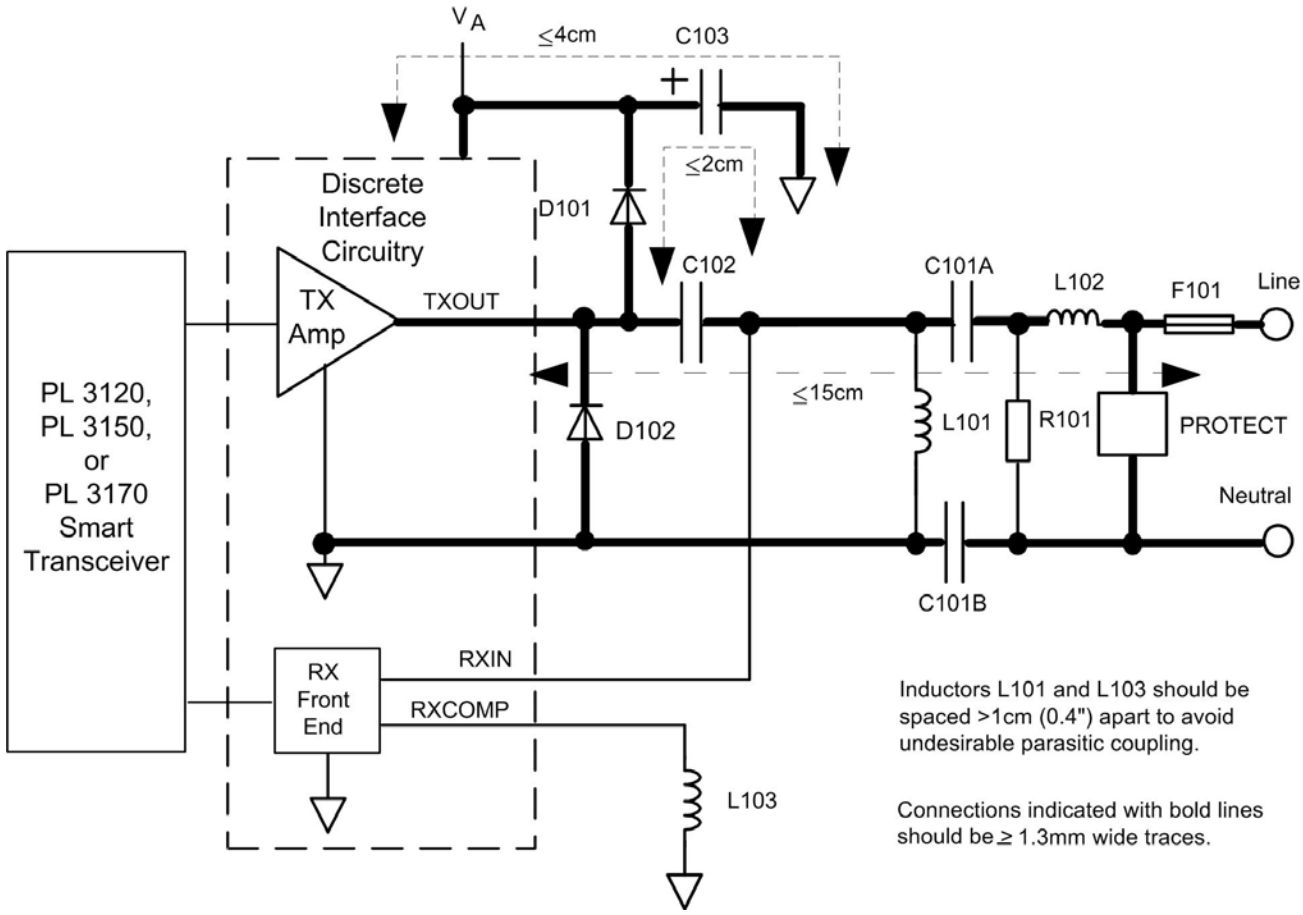


Figure 4.7 Line-to-Neutral, Non-Isolated Floating Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Joyin** www.joyin.com.tw
ACT www.act1.com	**Nichicon** www.nichicon-us.com
AID Electronics www.aid.com.tw	**ON Semiconductor** www.onsemi.com
Arcotronics www.arcotronics.us	**Panasonic** www.panasonic.com/industrial/components
Fairchild Semiconductor www.fairchildsemi.com	**Shinhom** www.shinhom.com
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Taiyo Yuden** www.ty-top.com
Hollyfuse www.hollyfuse.com	**Vishay** www.vishay.com
Illinois Capacitor www.illinoiscapacitor.com	**Wickmannn** www.littlefuse.com/cgibin/r.cgi/en/brand_Wickmannn.html

Table 4.8 Line-to-Neutral, Non-Isolated Floating Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C101A,B	0.22µF	0.15µF	±10%, ≥250VAC, X2 type (1)	IllinoisCap/224MKP275KB AID Electronics/ MEX224K275AC	IllinoisCap/154MKP275K AID Electronics/ MEX154K275AC
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
F101	6A or 6.3A	6A or 6.3A	250VAC, time-lag (1), (2)	Wickmann/3741630041 Hollyfuse/5RT-063H	Wickmann/3741630041 Hollyfuse/5RT-063H
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K
L102	39µH	15µH	±10%, Imax ≥700mA, R_{DC} ≤0.30Ω	Taiyo Yuden/ LHL08TB390K Abracon/AIAP-01-390K Shinhom/LGA0512-390K	Taiyo Yuden/ LHL08TB150K Abracon/AIAP-01-150K Shinhom/LGA0512-150K
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
R101	1MΩ	1MΩ	±5%, ≥1/4W, max working voltage ≥360VDC (1), (3)		
PROTECT	300VAC (470VDC)	300VAC (470VDC)	For indoor branch circuits, ≥1250A surge current, 8x20µs, 2 times	Panasonic/ERZ-V07D471 Joyin/JVR07S471K65	Panasonic/ERZ-V07D471 Joyin/JVR07S471K65

NOTES:

1. For nominal line voltages of 120VAC or less, the voltage rating on these parts can be lowered to reduce cost and space.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 510kΩ resistors in series, each with a working voltage rating of at least half of the value listed above.

Example 8. Line-to-Neutral, Power Line Power Supply Plus Coupler

Figure 4.8 presents a schematic for using a communication coupler combined with a power supply. Both 5W and 10W versions of this combined power supply/coupler are available from Echelon Corporation. These Power Supply/Couplers incorporate line-to-neutral coupling. Table 4.9 lists component values and recommended suppliers/part numbers for this design.

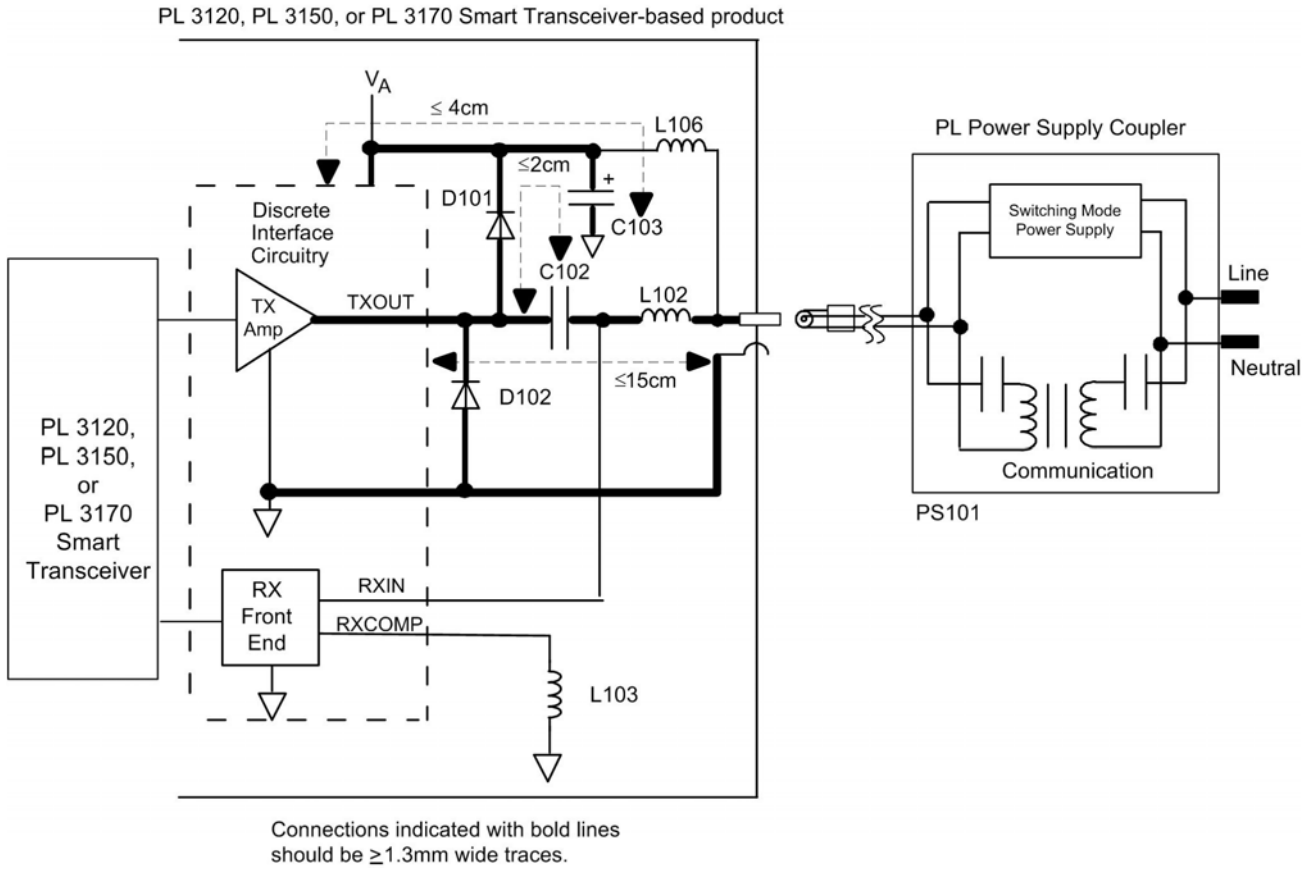


Figure 4.8 Line-to-Neutral, Isolated Power Line Power Supply Plus Coupler

Example Vendor Websites

Abracon Corporation www.abracon.com	**Nichicon** www.nichicon-us.com
Arcotronics www.arcotronics.us	**ON Semiconductor** www.onsemi.com
CTC Coils www.ctccoils.com/eng/index.htm	**Panasonic** www.panasonic.com/industrial/components
Echelon corporation www.echelon.com	**Shinhom** www.shinhom.com
Fairchild Semiconductor www.fairchildsemi.com	**Steward** www.steward.com/default.asp
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Vishay** www.vishay.com
Illinois Capacitor www.illinoiscapacitor.com	

Table 4.9 Line-to-Neutral, Power Line Power Supply Plus Coupler Component Values

Comp	Value C-band	Required Specifications	Example Vendors / Part# C-band
C102	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥820µF	±20%, ≥25VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1E821MPD Fenghua/8821LDM1020LY
D101	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
L102	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-10
L103	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ test frequency≤400kHz	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
L106	220µH	±10%, Imax ≥850mA, R_{DC} ≤0.5Ω	Shinhom/LCHB0912221K CTC Coils/ CH8010221K-542417-B
PS101	12V/5W	See Echelon model 78100R, 78101R data sheet	Echelon/78100R or 78101R
	12V/10W	See Echelon model 78112R, 78113R data sheet	Echelon/78112R or 78113R

Example 9. Low-Voltage AC, Non-Isolated Coupling Circuit

Figure 4.9 presents a schematic for a low-voltage AC, non-isolated coupling circuit. Table 4.10 lists component values and example suppliers/part numbers for coupling to AC circuits with voltages of ≤48Vpk.

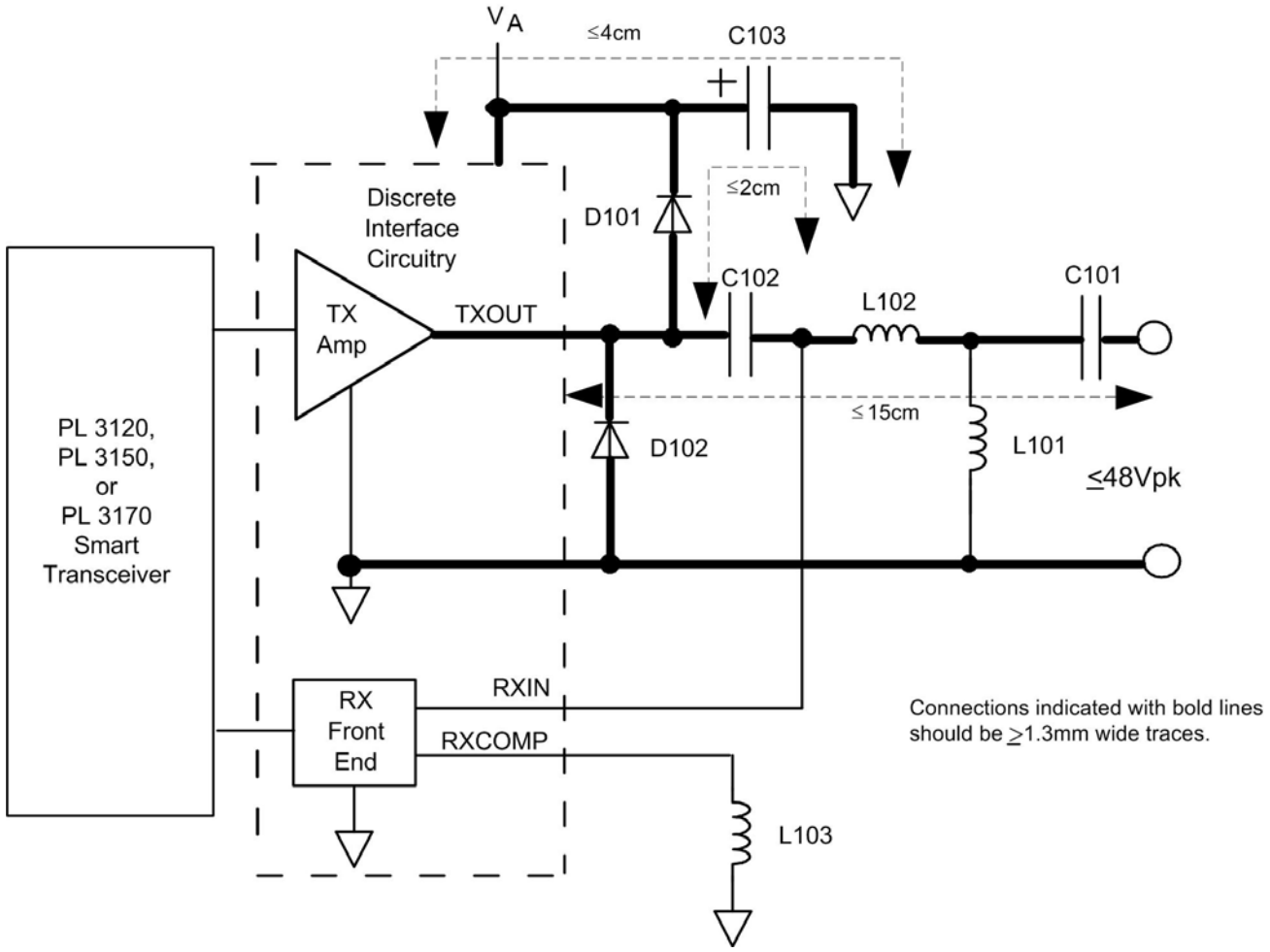


Figure 4.9 Low-Voltage AC, Non-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**ON Semiconductor** www.onsemi.com
ACT www.act1.com	**Panasonic** www.panasonic.com/industrial/components
Arcotronics www.arcotronics.us	**Shinhom** www.shinhom.com
Fairchild Semiconductor www.fairchildsemi.com	**Steward** www.steward.com/default.asp
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Taiyo Yuden** www.ty-top.com
Nichicon www.nichicon-us.com	**Vishay** www.vishay.com

Table 4.10 Low-Voltage AC, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C101	0.47µF	0.47µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC3470AA60J Surge /SRMA100V474K	Arcotronics/ R82DC3470AA60J Surge /SRMA100V474K
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K	Fastron/SMCC/N-102K Shinhom/LGA0410-102K TaiyoYuden/ LAL04TB102K
L102	Bead	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-10	Steward/ HI1206P121R-10
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF

Example 10. Low-Voltage AC, Transformer-Isolated Coupling Circuit

Figure 4.10 presents a schematic for a low-voltage AC, transformer-isolated coupling circuit. Table 4.11 lists component values and example suppliers/part numbers for coupling to AC circuits with voltages of ≤48Vpk.

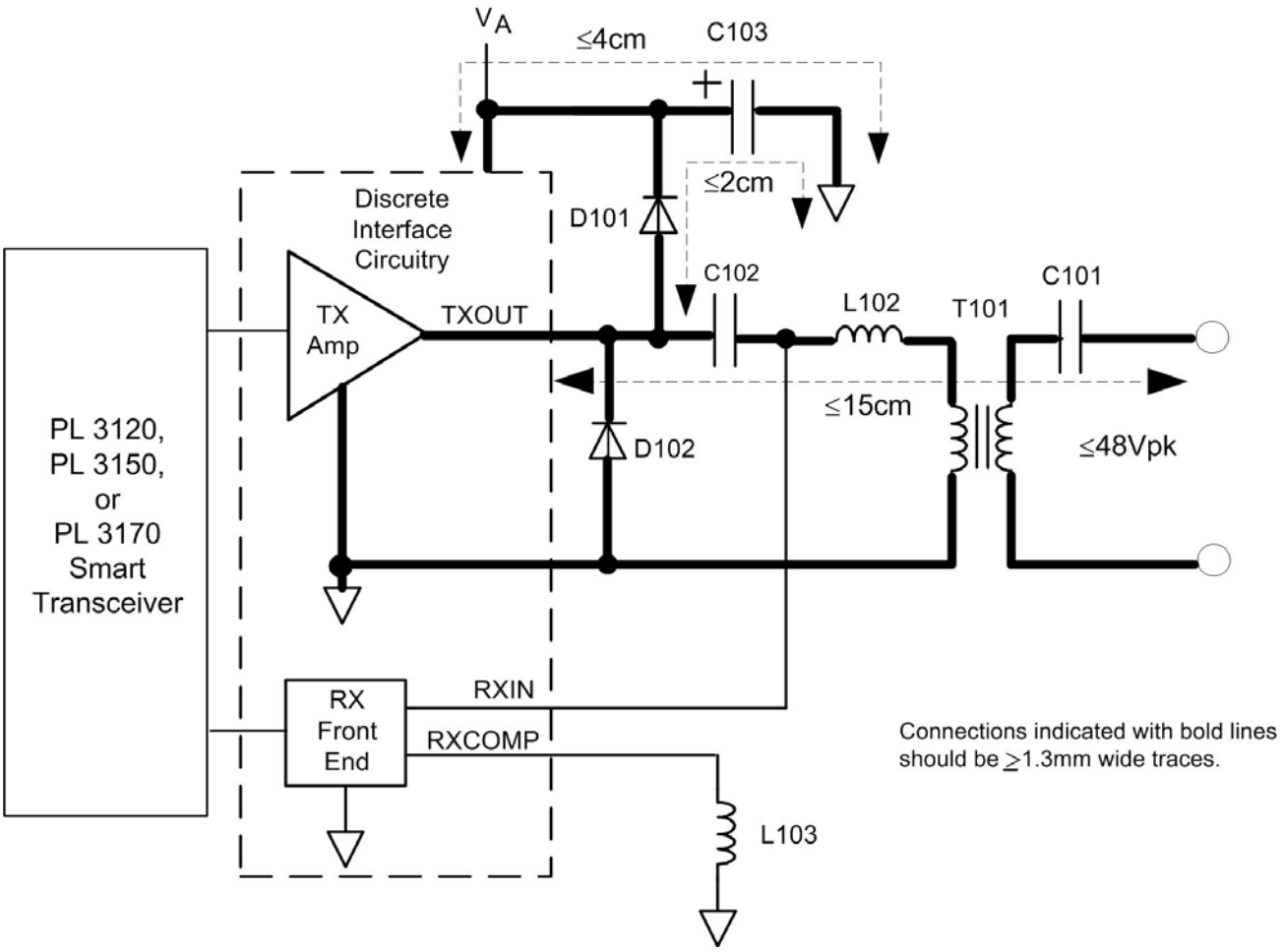


Figure 4.10 Low-Voltage AC, Transformer-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**ON Semiconductor** www.onsemi.com
ACT www.act1.com	**Panasonic** www.panasonic.com/industrial/components
Arcotronics www.arcotronics.us	**Shinhom** www.shinhom.com
Fairchild Semiconductor www.fairchildsemi.com	**Steward** www.steward.com/default.asp
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Vishay** www.vishay.com
Nichicon www.nichicon-us.com	

Table 4.11 Low-Voltage AC, Transformer -Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C101	0.47µF	0.47µF	±10%, ≥63VAC, metallized film	Arcotronics/ R82DC3470AA60J Surge /SRMA100V474K	Arcotronics/ R82DC3470AA60J Surge /SRMA100V474K
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G
L102	Bead	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-10	Steward/ HI1206P121R-10
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF
T101	Low-leakage transformer		See Appendix C	See Appendix C	See Appendix C

Example 11. Low-Voltage DC, Non-Isolated Coupling Circuit

Figure 4.11 presents a schematic for a low-voltage DC, non-isolated coupling circuit. Table 4.12 lists component values and example suppliers/part numbers for coupling to DC circuits with voltages of ≤48Vpk.

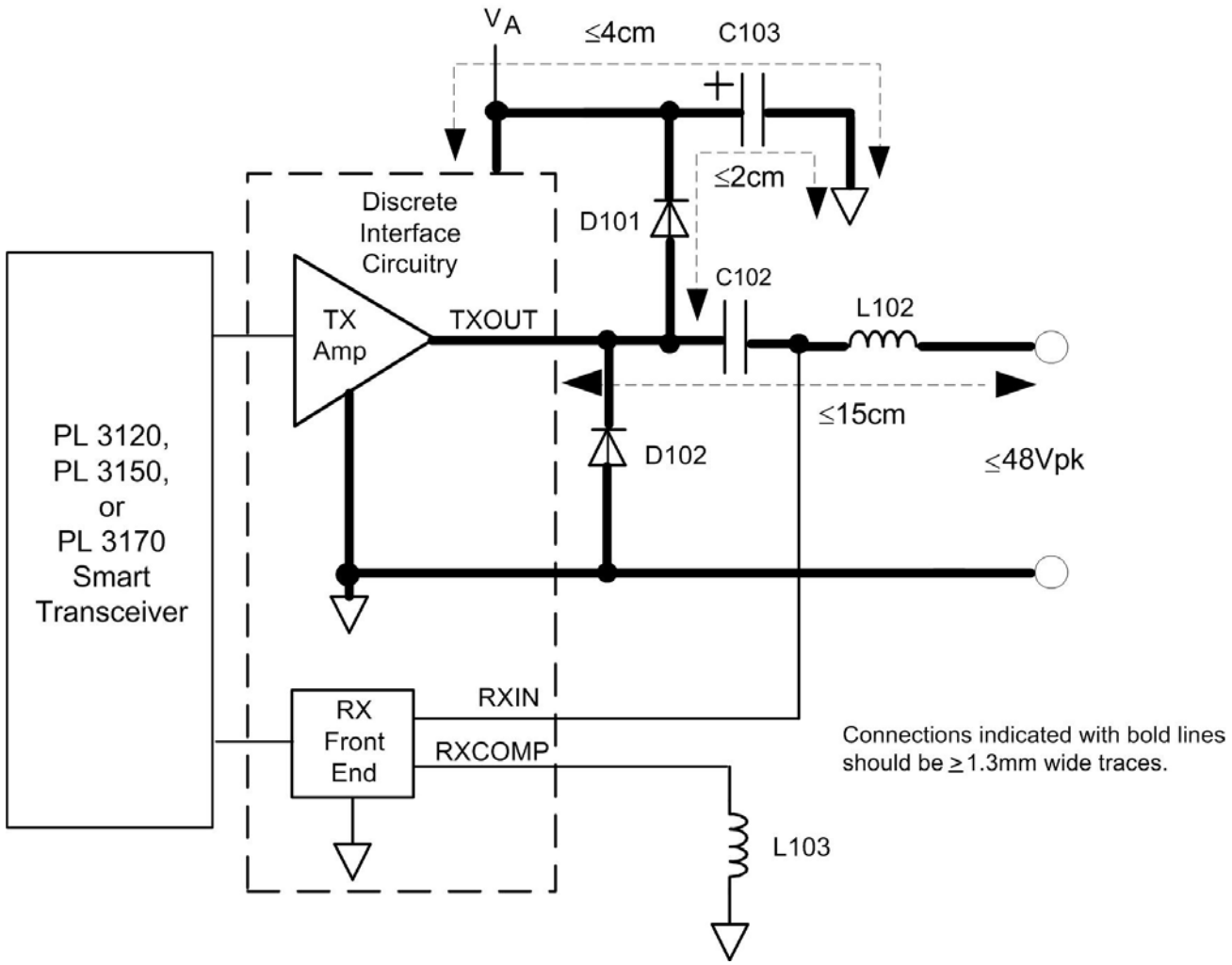


Figure 4.11 Low-Voltage DC, Non-Isolated Coupling Circuit Schematic

Example Vendor Websites

Abracon Corporation www.abracon.com	**Nichicon** www.nichicon-us.com
ACT www.act1.com	**ON Semiconductor** www.onsemi.com
Arcotronics www.arcotronics.us	**Panasonic** www.panasonic.com/industrial/components
Fairchild Semiconductor www.fairchildsemi.com	**Steward** www.steward.com/default.asp
Fastron www.fastrongroup.com	**Surge Components** www.surgecomponents.com
Fenghua Advanced Technology www.fenghua-advanced.com	**Vishay** www.vishay.com

Table 4.12 Low-Voltage DC, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendors / Part numbers	
	A-band	C-band		A-band	C-band
C102	1.0µF	1.0µF	±10%, ≥63VDC, metallized film	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K	Arcotronics/ R82DC4100AA60J Surge /SRMA100V105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY	Nichicon/UHE1C121MED Fenghua/ 8121LCMAA11LY
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D	Fairchild/1N4937 Vishay/1N4935-E3 Fairchild/RS1D
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ES1B Vishay/ES1D-E3 OnSemi/MUR120G	Fairchild/ES1B Vishay/ES1D–E3 OnSemi/MUR120G
L102	Bead	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-10	Steward/ HI1206P121R-10
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	Fastron/SMCC-152K Abracon/AIAP-01-152K ACT/DD152K-R	Fastron/SMCC-821K Abracon/AIAP-01-821K Panasonic/ELJ-FB821JF

Coupling Circuit Tutorial

Power Line Communications Background

The PL Smart Transceivers employ sophisticated digital signal processing techniques, a transmit power amplifier with a very low output impedance, and a very wide (>80dB) dynamic range receiver to overcome the signal attenuation and noise inherent in power mains communication. Maintaining the full communication capability of the PL Smart Transceivers requires careful selection and implementation of the mains coupling circuitry associated with those transceivers. This section gives an overview of the sources of signal attenuation as a basis for understanding choices in selecting and implementing mains coupling circuits.

Attenuation is the difference between the signal level at the output of the power line transmitter and the level of that same signal at the input of the intended receiver. While attenuation is often defined as the ratio of power levels, it is referred to in this document as the ratio of the transmitted signal voltage (unloaded) to the voltage of that same signal at the receiver input. A voltage ratio is more convenient to measure because power measurements require knowledge of the circuit impedance which, in the case of the power mains, varies with both location and time.

In power mains communications the attenuation of transmitted signals spans a wide range and is most conveniently denoted in decibels (dB), where voltage attenuation is defined in dB as $20\log_{10}(V_{transmit}/V_{receive})$. Thus 20dB of attenuation means that the signal was reduced by a factor of 10 by the time it arrived at the receiver, 40dB of attenuation corresponds to a factor of 100, 60dB a factor of 1000, and so on. A PL Smart Transceiver is capable of reliably communicating on a low-noise line, such as a dedicated twisted wire pair, when the transmit signal is attenuated by 80dB (a factor of 10,000). Thus a signal transmitted at 7Vp-p ($2.5V_{RMS}$) can be received when reduced to less than 700µVp-p ($250\mu V_{RMS}$).

To better understand the sources of attenuation in a network of power mains, it is helpful to look at a simplified model of a power distribution network. This example is based on an installation having one power distribution panel and two phases of mains power. While many applications for power line communication employ different numbers of phases, different topologies, voltages, and wire types, this example illustrates some of the key issues affecting the successful application of the PL Smart Transceiver.

Figure 4.12 depicts the path that a power line communication signal might traverse, starting from a wall socket and passing through the building's electrical wiring and circuit breaker panel, across power phases, and ultimately to another wall socket. Each socket in the power network can power a device that generates noise and loads the communications signal. For clarity, neutral and earth wires have not been shown.

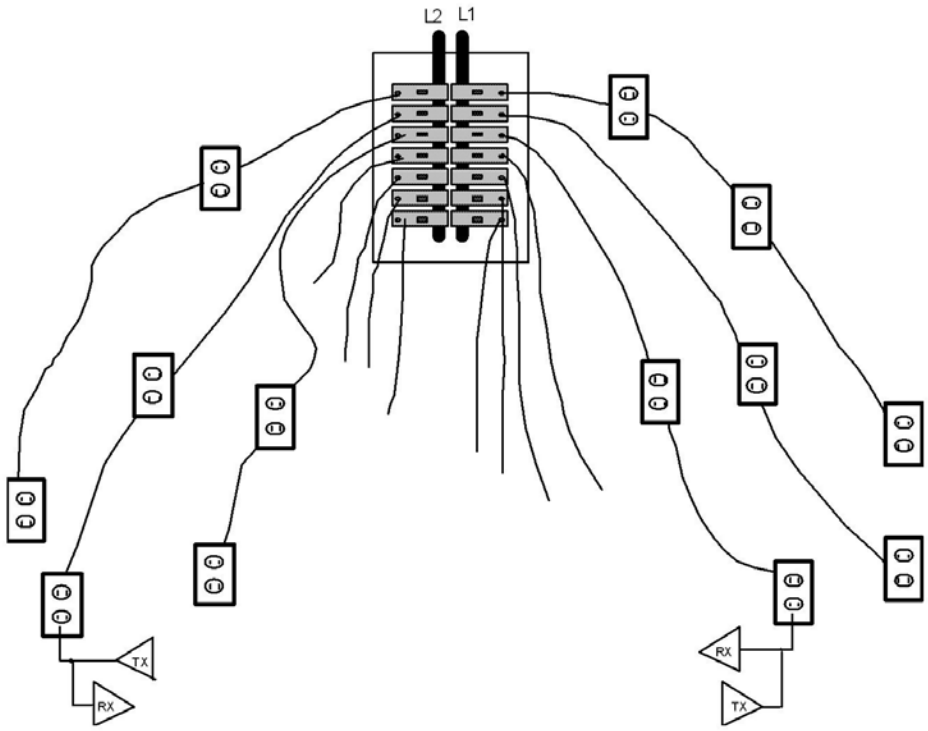


Figure 4.12 Power Distribution Model

Attenuation is most easily understood in terms of a voltage-divider circuit formed by the output impedance of the transmitter, the impedance of the various mains circuit branches, and any loads present on the mains branch circuits. At the communication frequencies of the PL Smart Transceiver (70kHz to 138kHz), the significant impedances are due to the series inductance of the mains wiring itself, capacitive loads between line and neutral, resistive loads between line and neutral, and the coupling between L101 and L102 which occurs due to mutual inductance and parasitic capacitance between phases. If these distributed impedances are lumped together and treated as if a single frequency is being transmitted, a simple attenuation model results as shown in Figure 4.13.

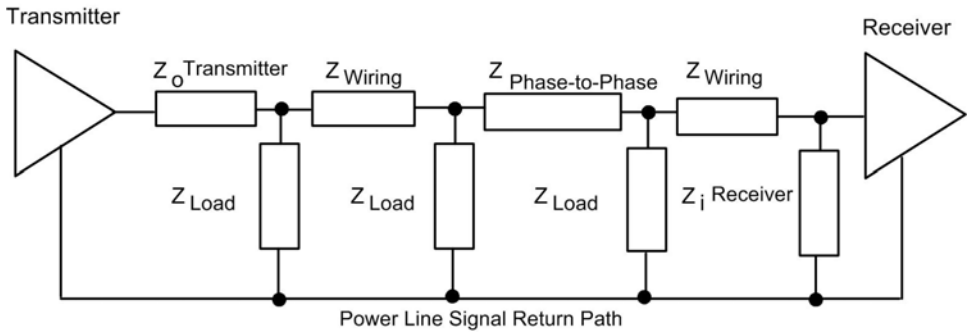


Figure 4.13 Power Mains Attenuation Model

This model illustrates that minimizing the series impedances and maximizing the line-to-return path impedances reduces the attenuation of the transmitted signal.

Power Line Coupling Basics

Injecting a communication signal into a power mains circuit is normally accomplished by capacitively coupling the output of a transceiver to the power mains. In addition to the coupling capacitor, an inductor or transformer is generally present. The coupling capacitor and the inductor or transformer together act as a high-pass filter when receiving the communications signal. The high-pass filter attenuates the large AC mains signal (at either 50Hz or 60Hz), while passing the communication signal of the transceiver. Figure 4.14 shows a basic mains coupling circuit. The value of the capacitor is chosen to be large enough so that its impedance at the communication frequencies is low, yet small enough that its impedance at the mains power frequency (50Hz or 60Hz) is high. The impedance of the capacitor can be considered as part of the transmitter's output impedance (Z_0 Transmitter) shown in Figure 4.13. Keeping the impedance of the coupling capacitor low minimizes the **signal injection loss** caused by the voltage divider formed between the output impedance of the amplifier and the mains loading (Z_{Load}).

The value of the inductor is chosen to provide a relatively high impedance at the communication frequencies of the PL Smart Transceiver. The inductor impedance can be considered part of the receiver input impedance ($Z_{i\ Receiver}$) shown in Figure 4.13. Keeping the inductor impedance high helps minimize any signal loss at the receiver due to the voltage divider formed by the wiring impedance and the receiver input impedance.

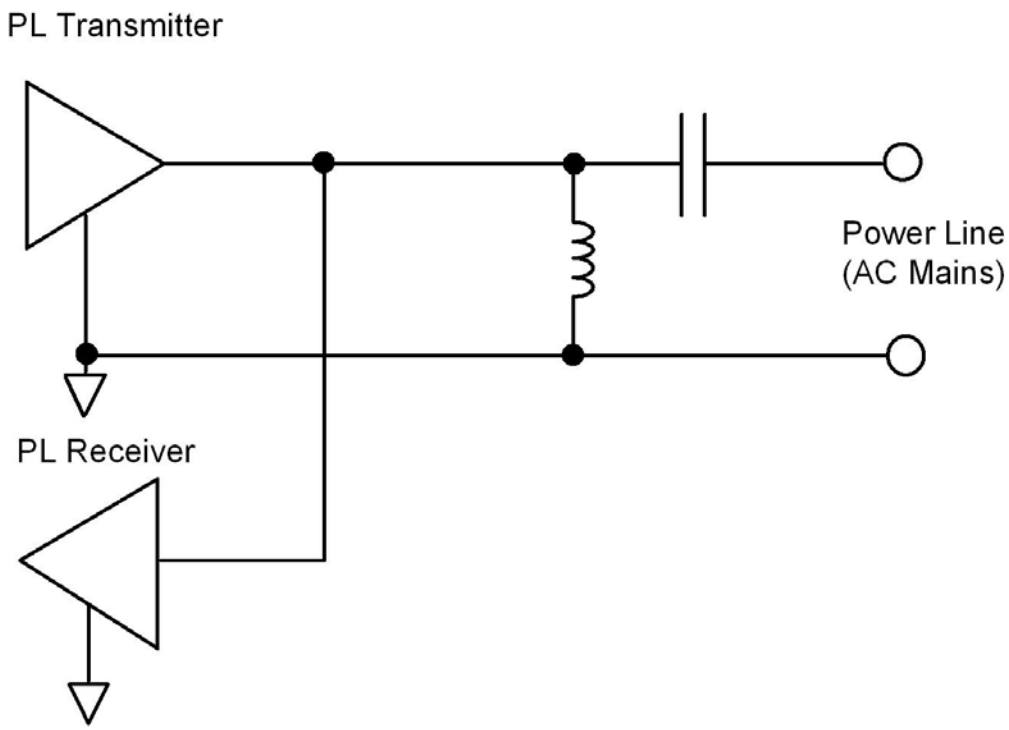


Figure 4.14 Basic Mains Coupling Circuit

A key factor affecting the type of coupling circuit to be used is the wiring style of the power distribution system to which the coupling circuit will be connected. Wiring topologies vary from application to application, e.g., homes versus commercial buildings, as well as from country to country. Wiring styles can be divided into two major categories: wiring

systems where a separate earth conductor is present and accessible (i.e., safety ground, which is not the same as a neutral wire with an earth bond), and wiring systems where there is no earth conductor.

When an earth conductor is always present, a coupling method known as **line-to-earth** coupling provides the best communications performance. With line-to-earth coupling, the communications signal is coupled to the line wire relative to earth, and earth is used as the return path for the communications signal. This coupling technique is also referred to as **earth-return** coupling. Local restrictions might apply to the use of line-to-earth coupling (see *Ground Leakage Currents* in the *Safety Issues* section of this chapter for more information). As a general rule, line-to-earth coupling is only used in commercial applications in North America and non-EU countries where local electrical codes require the presence of an earth safety ground and permit the associated 50/60Hz leakage current. Figure 4.15 illustrates a simple example of a line-to-earth coupling circuit.

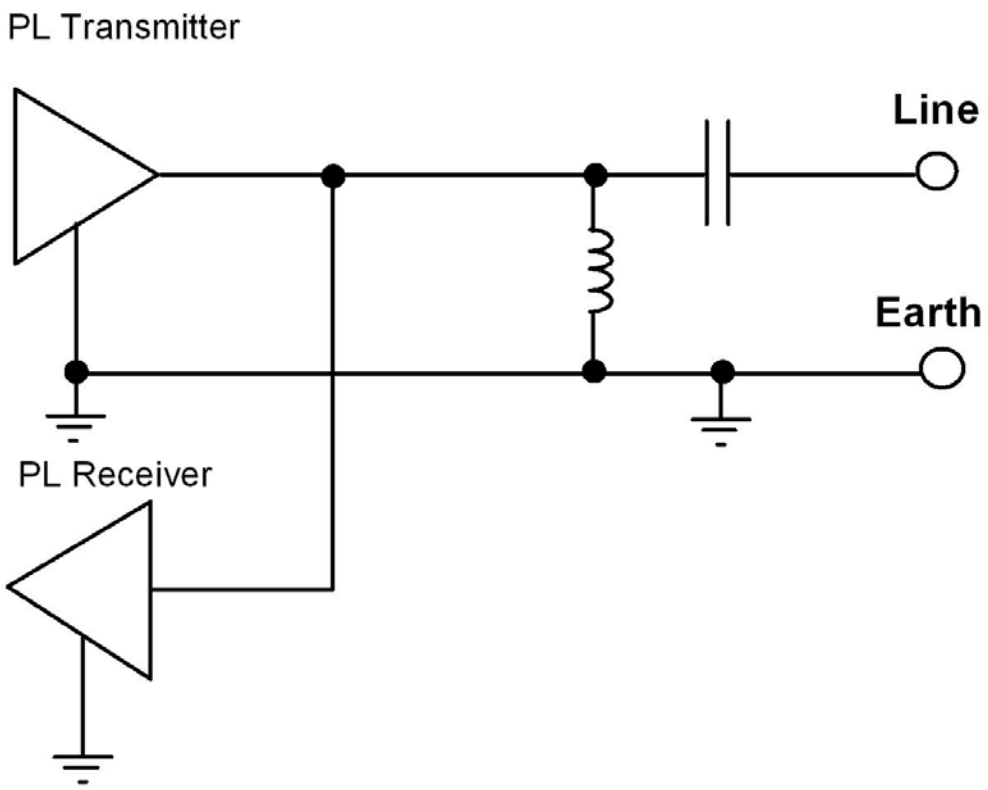


Figure 4.15 Line-to-Earth Coupling Method

To understand the advantage of line-to-earth coupling, recall that a major component of signal attenuation is due to the loads presented by devices that are connected to the power mains between the line and neutral wires. These loads have only minimal affect on signal attenuation when line-to-earth coupling is used. Field measurements have shown consistent improvements in received signal-to-noise ratios of more than 15dB for transceivers using line-to-earth coupling, relative

to transceivers using non-earth-return coupling. For this reason, when a safety ground connection is known to be available throughout the wiring system, a line-to-earth coupling scheme is preferred.

In applications where a safety ground connection is not always available, or where line-to-earth coupling is precluded by local regulations, the coupling circuit must be connected between the line and neutral wires. This style of coupling is known as either **line-to-neutral** or **neutral-return** coupling. Line-to-neutral coupling is recommended for in-home applications world wide, and is illustrated in Figure 4.16.

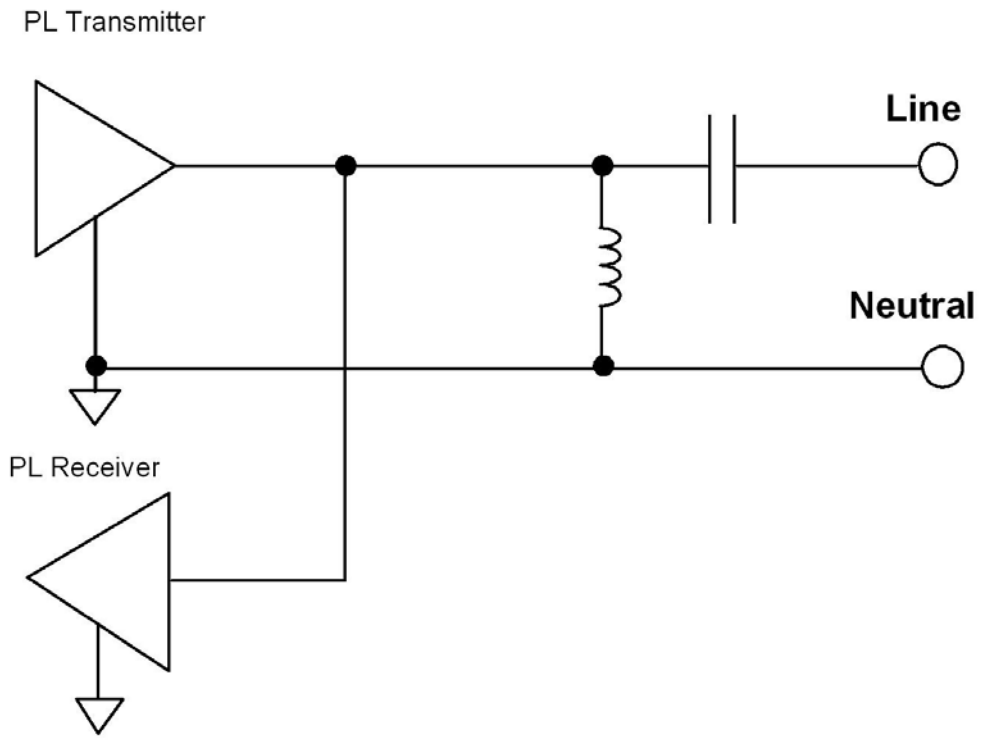


Figure 4.16 Line-to-Neutral Coupling Style

In the following section the simple circuits shown in Figures 4.15 and 4.16 are expanded to make them practical in real applications. The following discussion applies to both line-to-neutral coupling and line-to-earth coupling, as the coupling circuit topology for each is the same.

Power Line Coupling Details

The coupling circuits shown in Figures 4.15 and 16 require the addition of a small number of components to make them practical. Figure 4.17 shows the addition of an AC coupling capacitor (C102) to prevent the inductor from shorting the DC bias voltage of the transmit amplifier.

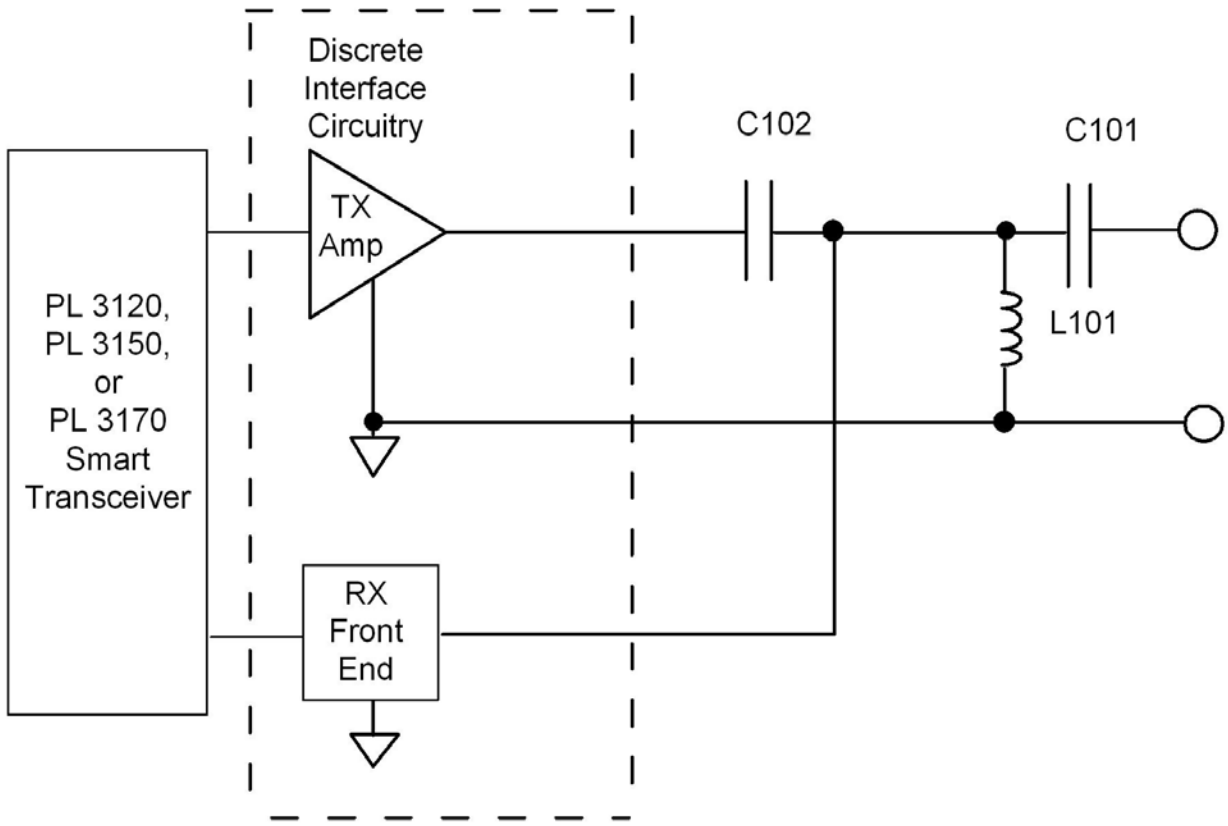


Figure 4.17 Simplified Coupling Circuit with DC Blocking Capacitor

Given the attenuation model presented earlier in Figure 4.13, one critical design constraint is that the impedance of the series combination of C101 and C102 must be very low at the communication frequencies of the PL Smart Transceiver. The impedance of these capacitors, along with the PL Smart Transceiver transmit amplifier's output impedance, corresponds to "Z_0 Transmitter" in Figure 4.13. Because the equivalent load impedance of the power line can in some cases be on the order of 1 ohm, and because the output impedance of the PL Smart Transceiver transmit amplifier is less than 1 ohm, the impedance of these capacitors at communication frequencies should be less than 1 ohm so that they do not add significantly to "Z_0 Transmitter". While the values of C101 and C102 could be set high enough to meet this goal, doing so would significantly increase the cost of the high-voltage capacitor C101. Because C102 is connected only to low voltage, and thus is lower cost for a given value, its value can be set higher relative to the value of the high-voltage capacitor C101.

A simple and cost-effective way to achieve low transmit impedance with modest size capacitors is to add inductor L102, as shown in Figure 4.18. This inductor forms a series-resonant circuit with C101 and C102, and its value can therefore be chosen to optimize coupling at the communication frequencies of the PL Smart Transceiver while minimizing the cost of C101 and C102. Different values of C101 and L102 are needed for A-band and C-band operation to optimize the performance of a coupler in its respective band. The component values listed with the example coupling circuits documented in this chapter include values optimized for each application and band of operation.

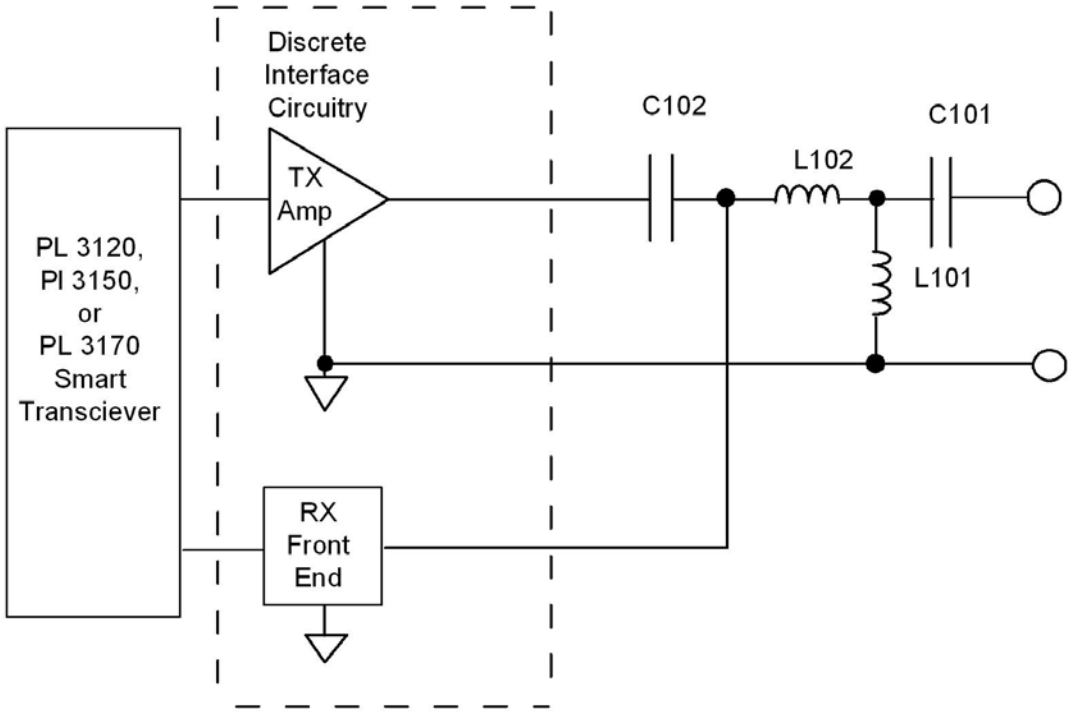


Figure 4.18 Simplified Coupling Circuit with Resonant Inductor

An important design constraint on L102 is that its DC resistance must be a small fraction of an ohm because it is in the transmit signal path and effectively part of the transmitter's output impedance. Fortunately low-cost inductors with DC resistance of 0.3 ohms or less are widely available.

Capacitors C101 and C102 should be of metalized film construction in order to minimize their equivalent series resistance and provide adequate surge immunity.

It is critical that no additional series impedance be added in the signal path between the PL Smart Transceiver transmit amplifier and the power mains (or in the return path from the power mains to the ground pins of the PL Smart Transceiver) unless verified to be less than 0.5 ohms between 70kHz and 138kHz.

To illustrate the importance of maintaining a low impedance signal path, consider the example of a ferrite bead with an impedance of 9 ohms at 100kHz added in series with the line. In this case the signal injected into a 1 ohm power line would be reduced *by a factor of 10*. Under typical conditions, the end product would still function, however, communication margin and reliability over a full range of power line environments would be severely compromised. Ferrite beads, unless carefully selected to be low impedance at 100kHz, offer too much series impedance. Most devices built with the PL Smart Transceiver do no need ferrite beads in order to pass EMC regulations. If, due to other noise generating circuitry ferrite beads are required, then refer to the end of Chapter 6 for a discussion of acceptable topologies.

The impedance of series circuit protection elements must also be kept very low. Low current fuses (<2A) and protection devices that can be reset generally add unacceptable series impedance to the signal path.

Figure 4.19 shows additions to the coupling circuit which are required to make it fully functional. The first is an inductor, L103, connected to the PL Smart Transceiver receive filtering circuitry. The DC resistance of L103 can be up to 55 ohms. The second consists of diodes, D101 and D102, connected from the transmitter to the amplifier supply rails to protect the inputs of the PL Smart Transceiver from large (>18V) transients. The characteristics of these diodes are very important for them to perform their intended function without impairing the operation of the transmit amplifier. All of the necessary specifications are listed in the "*Required Specifications*" column of the component tables for each example coupling circuit included in this chapter. Bypass capacitor C103 also has been added to emphasize the fact that it is an integral part of the coupling circuit. One of the functions of this capacitor is to protect the V_A supply line from excessive overshoot when positive going line surges discharge through diode D101. If the output capacitor of the V_A power supply meets all of the required specifications for C103 (and it can be located close to the transmit amplifier and D101) then no additional capacitor is needed as part of the coupling circuit. Alternately a separate C103 capacitor can be included close to the transmit amplifier and D101, if the V_A power supply capacitor does not meet these requirements.

To maintain a low impedance signal path, all of the circuit board traces between the output of the transmit amplifier and the AC mains wiring should be at least 1.3mm (50 mils) wide and less than 15cm (6 inches) long. The corresponding signal return path should either be a copper plane or a trace that is at least 1.3mm wide and less than 15cm long. Because positive polarity surge events cause high currents to flow through D101 and C103 back to ground, the circuit traces from the point where D101 taps into the signal path to the point where C103 connects back to ground are also critical. They should be at least 1.3mm wide and no more than 2cm (0.8 inches) long. To properly control ripple on the V_A supply of the transmit amplifier, the traces between the V_A input of the transmit amplifier and the point where C103 connects back to ground should also be at least 1.3mm wide and no more than 4cm (1.6 inches) long. The solid bold lines in Figure 4.20 indicate circuit traces that should be greater than or equal to 1.3mm wide. The dotted-line arrows in the figure indicate the maximum trace lengths.

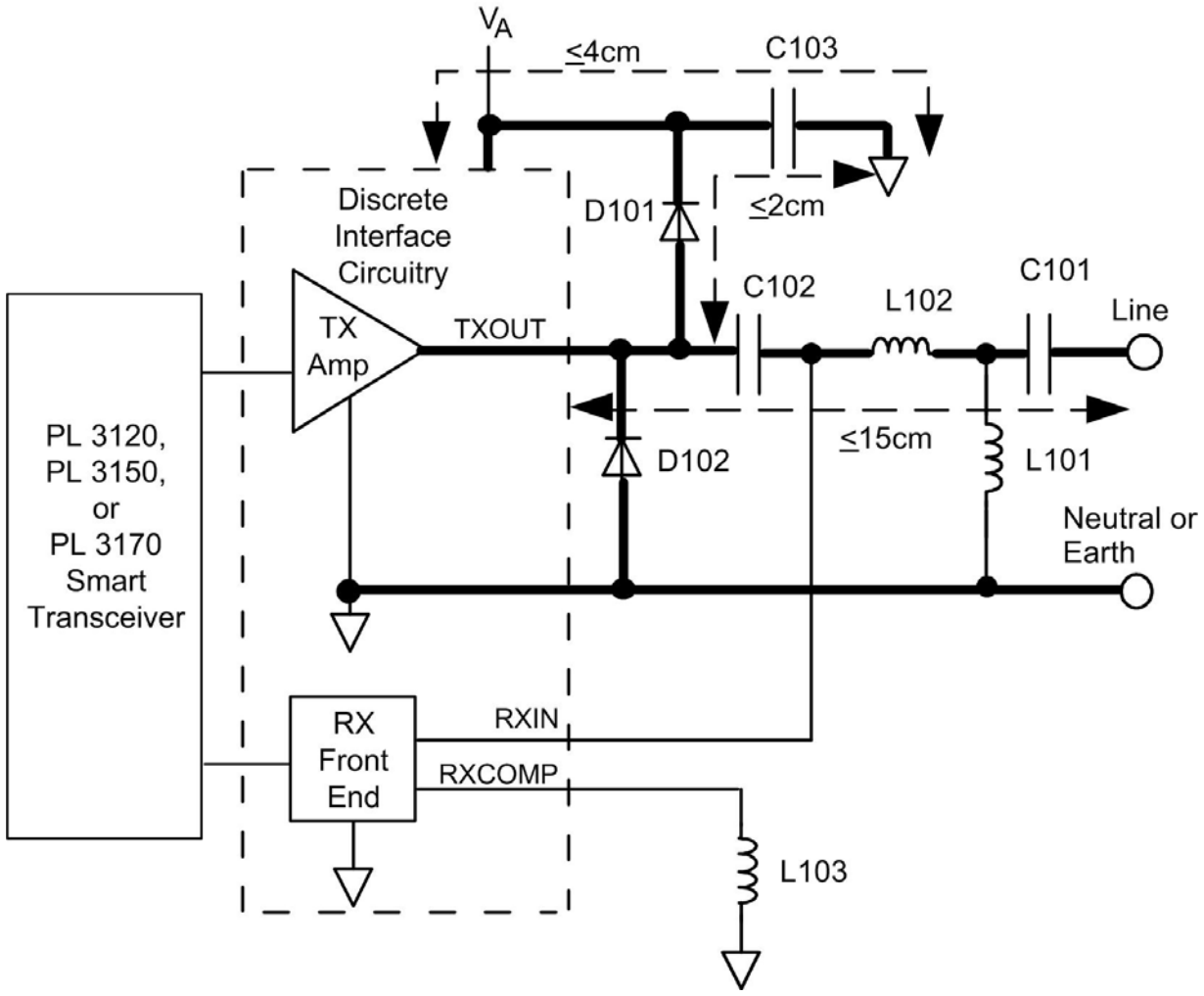


Figure 4.19 Functional Line-to-Neutral or Line-to-Earth Coupling Circuit

In instances where large ambient magnetic fields might be present (such as from switched mode power supply open frame magnetic elements), it is possible that one or more of the PL Smart Transceiver coupling circuit inductors might pick up these stray fields and conduct them onto the power mains. Depending on the frequency and amplitude of these fields they could result in failure to meet conducted emission regulations.

If noise from parasitic coupling is suspected, it can be confirmed by inserting a 10cm (4 inch) twisted wire pair in series with one of the inductors in question. If the conducted noise spectrum varies by more than a few dB when this inductor is moved closer to, and farther from, other components, then parasitic coupling might be the source of the problem.

If stray coupling is a problem, regulations can usually be met by adjusting the location or orientation of the radiating device relative to the coupling circuit inductors. Alternately, shielded or toroidal inductors can be used to reduce coupling as long as all electrical parameters specified in the example coupling circuit tables given later in this chapter are met. If, however, a toroidal or shielded inductor is used in place of L102, then the selected part must handle the maximum output current of the PL Smart Transceiver transmit amplifier without approaching saturation. If L102 even approaches saturation it can add harmonics of the PL Smart Transceiver transmit signal which might result in failure to meet conducted emission regulations (in this instance, due to inductor distortion instead of a stray pickup). For this reason, a shielded or toroidal inductor used for L102 should have DC current rating two or three times higher than listed in the example circuits given later in this chapter. The recommended open frame axial inductors do not need this extra operating margin due to the linearity provided by a magnetic path that is partly in air.

Coupling Circuit Receive Impedance

To avoid attenuating receive signals, the transmit amplifier of the PL Smart Transceiver is switched to a high impedance state (approximately 500 ohms) when it is not transmitting. The receive-mode impedance of the PL Smart Transceiver circuitry, in conjunction with the coupling circuits recommended in this chapter, is greater than 250 ohms in the communication frequency range (70kHz to 90kHz for A-band and 110kHz to 138kHz for C-band).

Regulations in some countries might set a limit on how low the receive-mode impedance can be outside the communication frequency range. The receive-mode impedance of most coupling circuits dips near 10kHz due to a series resonant effect between the line coupling capacitor (C101) and the coupling inductor (L101). This dip in receive-mode impedance near 10kHz does not have any adverse effect on the communication performance of the PL Smart Transceivers. If local regulations require a minimum out of band receive impedance of 5 ohms, then this can be accomplished by selecting an inductor, L1, which has more than 5 ohms of DC resistance. In order to meet conducted emission regulations, the DC resistance of this inductor should not exceed 14 ohms, as specified in the example coupling circuits shown in this chapter.

Safety Issues

This guide is intended only as an introduction to some of the safety issues associated with designing circuits using the PL Smart Transceiver. This document is not a primer on electrical safety or electrical codes, and it is the responsibility of the user to become familiar with any applicable safety rules or regulations. A review of all designs by competent safety consultants and the pertinent regulatory or safety agencies is strongly recommended.

Safety Isolation Considerations

Many products include an isolation barrier in the form of an insulated enclosure between a user and any hazardous conductors. A typical product of this type is a light switch in which the PL Smart Transceiver and all of the associated electrical components are contained inside the switch enclosure. The type of coupling circuit that can be used in these applications is called a *non-isolated coupling circuit*. A non-isolated coupling circuit generally requires lower cost components, making it especially desirable for use in price-sensitive consumer products and wiring devices. All of the coupling circuit examples that have been shown so far are of the non-isolated type.

Some products cannot rely on their enclosure as a safety isolation barrier and an alternate method of safety isolation must then be provided. For example, a circuit board that used a non-isolated line-to-neutral coupling circuit in conjunction with a PL Smart Transceiver whose I/O pins are user-accessible would present a potential electrical shock hazard. Because the mains neutral lead is connected directly to the circuit board common, the user could be exposed to a hazardous voltage at the I/O connector, especially if the line and neutral connections are accidentally reversed. Additional circuitry is needed in such a product to provide a safety isolation barrier between the user-accessible I/O connector and the mains line and neutral conductors.

The most common solution is to provide isolation in the coupling circuit by modifying the simple coupling circuit described earlier. This style of coupling circuit is referred to as an **isolated coupling circuit**. The preferred isolated coupling circuit uses **transformer-isolation**. Transformer-isolation requires substituting a safety agency-recognized transformer having the appropriate communication characteristics in place of L101 (see Appendix C). Transformer-isolation can be used for both line-to-neutral and line-to-earth coupling. Transformer-isolated coupling has the advantage that the resonant inductor L102 can be incorporated into the isolation transformer by designing the leakage inductance of the transformer to match the value of L102. A transformer-isolated coupling circuit is shown in Figure 4.20, where it can be seen that the transformer isolates the PL Smart Transceiver from the line conductor and the neutral or earth conductor.

It is important to note that mains powered products that require circuit isolation must incorporate both an isolated coupling circuit and an isolated power supply. An isolated coupling circuit can be used with a non-isolated power supply (or visa-versa) but a mixed combination will not provide circuit isolation.

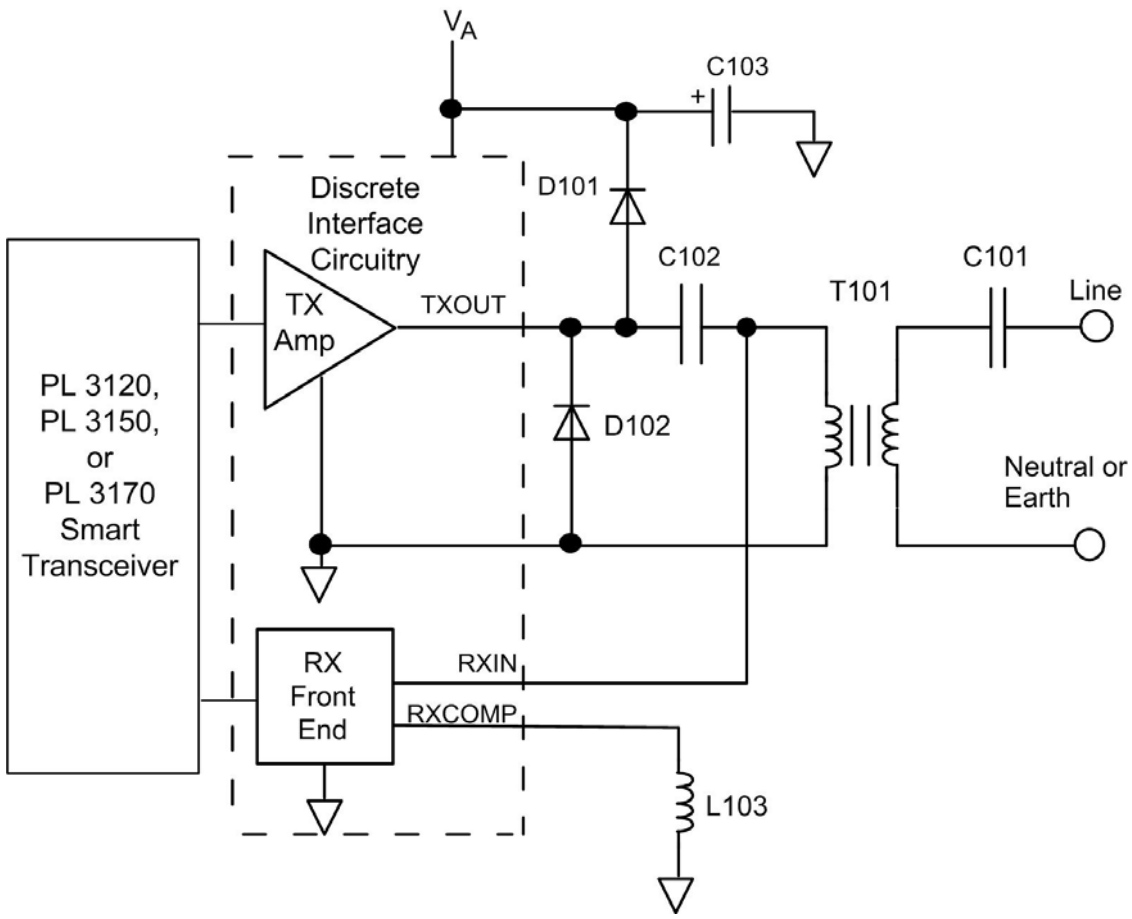


Figure 4.20 Functional Transformer-Isolated Coupling Circuit

The receive-mode impedance of the transformer isolated coupling circuit dips near 10kHz due to the series resonant effect between C101 and T101. This dip in out-of-band impedance does not have any adverse effect on communication performance. If local regulations require a receive impedance at this resonant frequency of greater than 5 ohms, then an optional series RLC circuit can be added as shown in Figure 4.21.

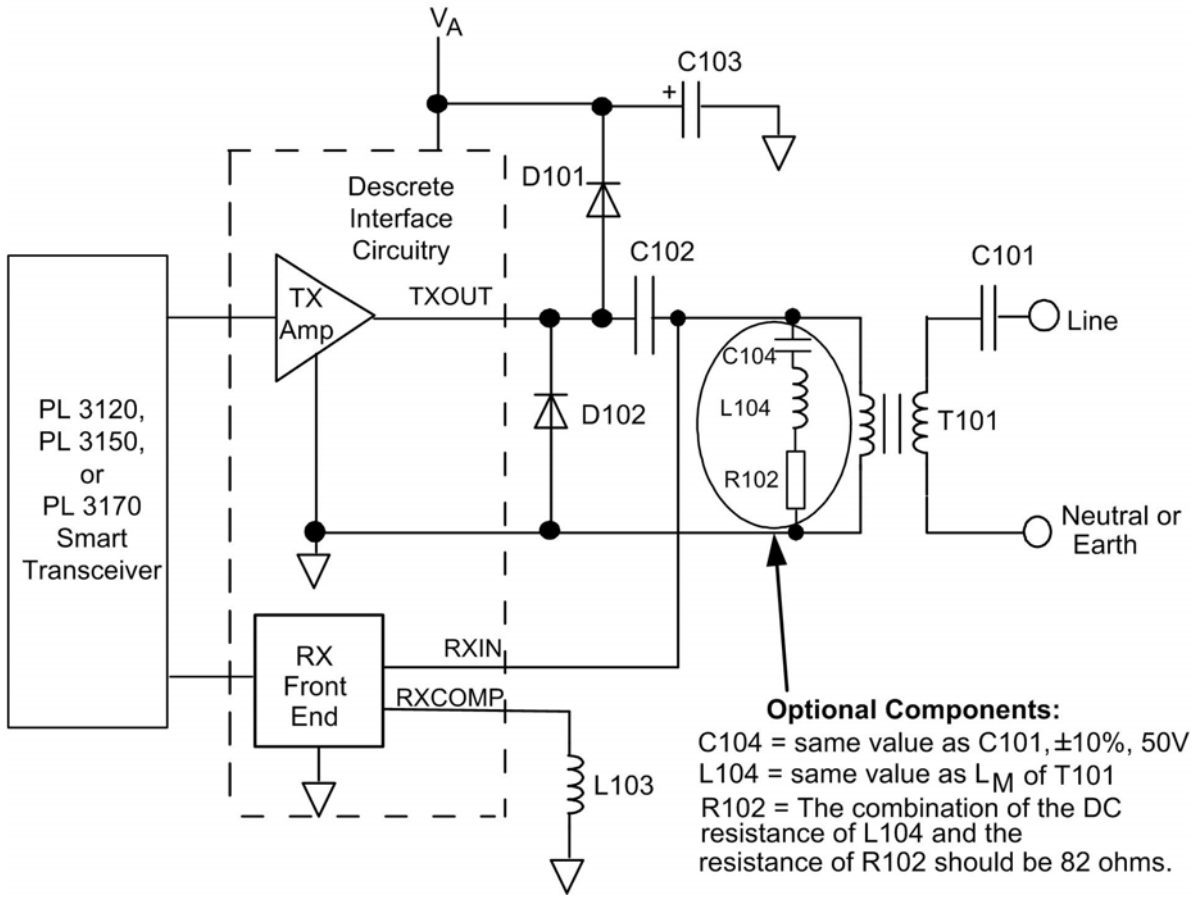


Figure 4.21 Transformer-Isolated Coupling Circuit with Optional RLC Circuit

Ground Leakage Currents

In power line systems that use line-to-earth coupling, there are both safety and practical limits on the level of ground leakage currents that are permitted. In the case of products intended for use in commercial buildings and homes, many safety agency standards set a ground leakage current limit of 3.5mA. This leakage limit determines the maximum value of C101 (in Figures 4.19 and 4.20) for line-to-earth coupling circuits. In the line-to-earth coupling circuits documented at the beginning of this chapter the value of C101 has been chosen to limit the ground leakage current to less than 3.5mA.

A practical limit on the use of line-to-earth coupling also exists. Many single circuit ground fault interrupters (GFIs), also known as residual current devices (RCDs), can be triggered with ground currents as low as 4mA. If each PL Smart Transceiver employing line-to-earth coupling generates about 3mA of ground current, then only one such transceiver can be installed on each GFI-protected circuit. For this reason line-to-earth coupling might not be suitable for some applications with low-current GFIs, and line-to-neutral coupling should be used instead. Local regulations also might prohibit the use of earth as the return path for a signaling system.

Capacitor Charge Storage

The coupling capacitors depicted in the earlier figures can retain substantial charge even after a PL Smart Transceiver-based device has been disconnected from the power mains. This can be of significant concern in applications where a line cord could be touched by a user after being disconnected from the power mains. To minimize potential shock hazard, coupling circuits should include a large value bleeder resistor to discharge the coupling capacitors following disconnection from the mains. Even in applications where the connection to the mains is permanently wired, it is good practice to include the resistor to protect service personnel. The example coupling circuits shown at the beginning of this chapter include appropriate bleeder resistors. If an alternate path to discharge this capacitor exists (such as the primary winding of a linear power supply transformer) then this bleeder resistor can be eliminated.

Fuse Selection

Safety considerations might require a fuse in series with the mains connection. For an end product to continue to function (without user intervention) it is necessary that the selected fuse not open following a specified line surge. A minimum 6A time-lag ("slow blow") rating has been shown to be necessary to avoid unintentional fusing action for surge events in branch circuit and power entry applications. For outdoor applications a 10A time-lag part is needed to avoid unintentional fusing.

If a coupling circuit that incorporates varistor protection is selected, the recommendations of the varistor manufacturer for maximum fuse current rating should be followed. Several varistor manufactures recommend a maximum fuse rating of 6A to 6.3A for use with 1250A surge-rated varistors and a maximum rating of 18A for use with 4500A surge-rated varistors.

If a current rating greater than 6.3A is required by the application then a varistor with a surge current rating of >2000A is recommended.

For the purposes of communication signaling it is also important that the fuse add very little resistance (<0.1 ohms) to the transmit signal path. Use of fuses in the 6A to 10A range satisfy this requirement.

3-Phase Coupling Circuits

When power line communication devices are located on different AC power phases, a significant portion of the overall attenuation between these devices is caused by loss in crossing phases (typically 10-20dB). Most of this loss can be avoided if one of two communicating devices connects to all power phases as illustrated in Figure 4.22. If all communications are to (and from) a device located at a central distribution panel, then the use of a 3-phase coupling circuit in that device is recommended to maximize communication distance. Due to the fact that this central device must drive the parallel combined impedance of all three phases, a higher current transmit amplifier is recommended for use in these locations.

The standard transmit amplifier recommended for use in most PL Smart Transceiver-based products includes circuitry to limit output current to 1Ap-p (so that the amplifier will not be damaged when driving very low impedance lines). An alternate transmit amplifier, which can provide 2Ap-p of output is recommended for use with 3-phase couplers. The appropriate transmit amplifier can be implemented using an optional discrete interface circuit with the PL Smart Transceiver. Reference design implementations for both the 1Ap-p and 2Ap-p interface circuitry are available, and are summarized in Appendix A.

Note that the return path for a 3-phase coupling circuit can be either neutral or earth, whichever is appropriate for the application. Note also that a 3-phase earth-return coupling circuit does not result in the same ground leakage current as a single-phase line-to-earth coupling circuit. The ground leakage current of a 3-phase earth-return coupling circuit is nominally zero. This is due to the canceling effect of the three leakage currents through C101A, C101B, and C101C, which are 120 degrees out of phase with each other.

Detailed schematics and component values for both non-isolated and isolated 3-phase coupling circuits are given in example coupling circuit numbers 5 and 6, respectively.

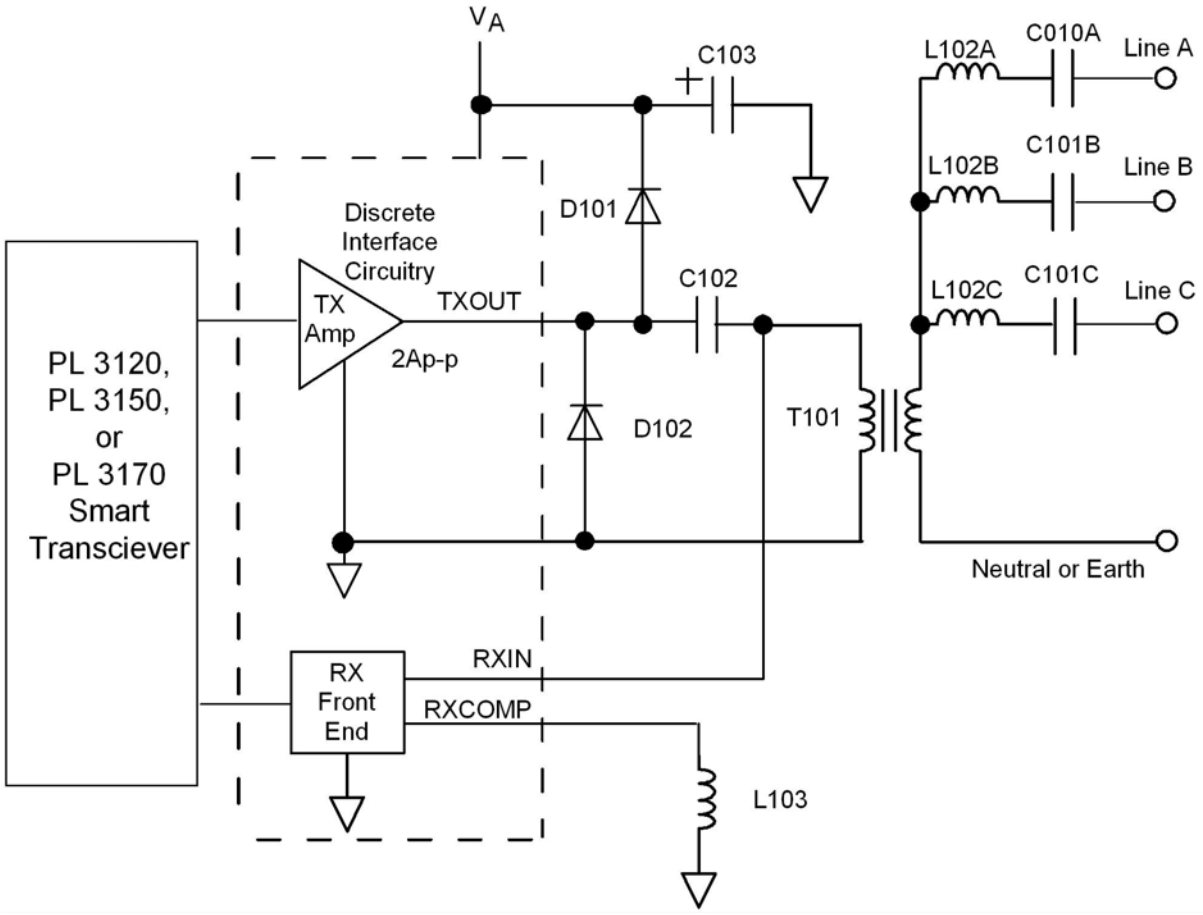


Figure 4.22 Transformer Isolated 3-Phase Coupling Circuit

Non-isolated Floating Coupling Circuits

The non-isolated coupling circuits discussed so far are suitable for use with devices incorporating power supplies where the output common terminal can be connected directly to the mains wiring. A non-isolated power supply with half-wave rectification is an example of such a supply (Figure 4.23). A non-isolated power supply which incorporates a full-wave bridge rectifier is not compatible with the non-isolated coupling circuits discussed earlier since the presence of the coupling circuit will effectively short out part of the rectifier (see Figure 4.24). While this problem can be avoided by using an isolated coupling circuit, a lower cost option for use with full-wave rectified power supplies is illustrated in Figure 4.25. This type of coupling circuit is referred to as a *Non-isolated Floating Coupling Circuit.* The detailed component values for this coupling circuit are given in coupling circuit example 7 earlier in this chapter.

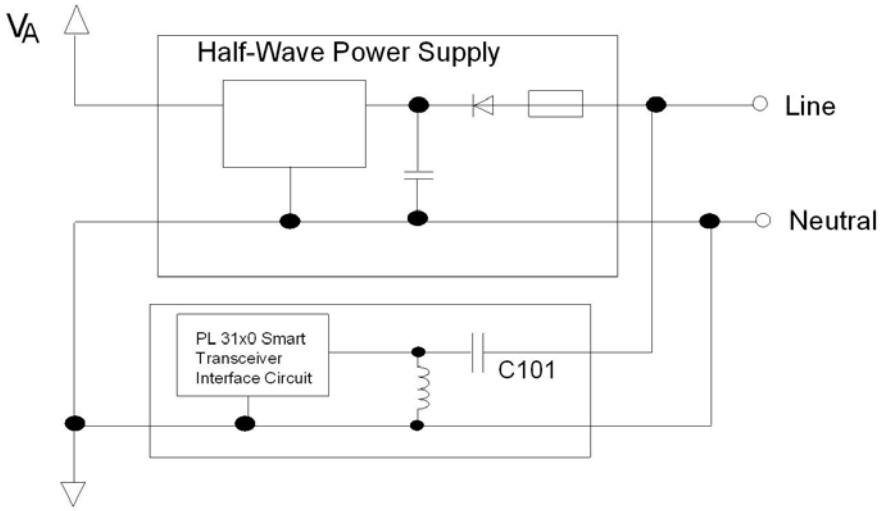


Figure 4.23 Half-Wave Rectified Power Supply and Non-Isolated Coupling

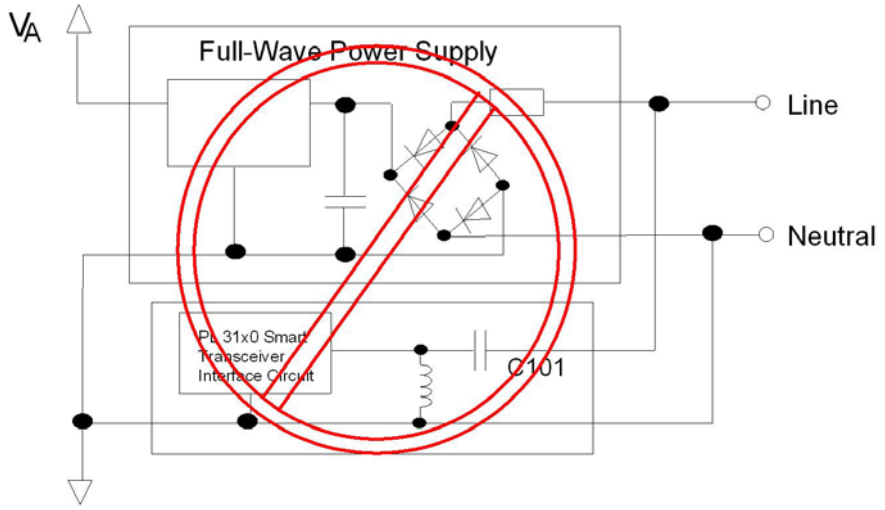


Figure 4.24 Full-Wave Rectified Power Supply and Non-Isolated Coupling Circuit

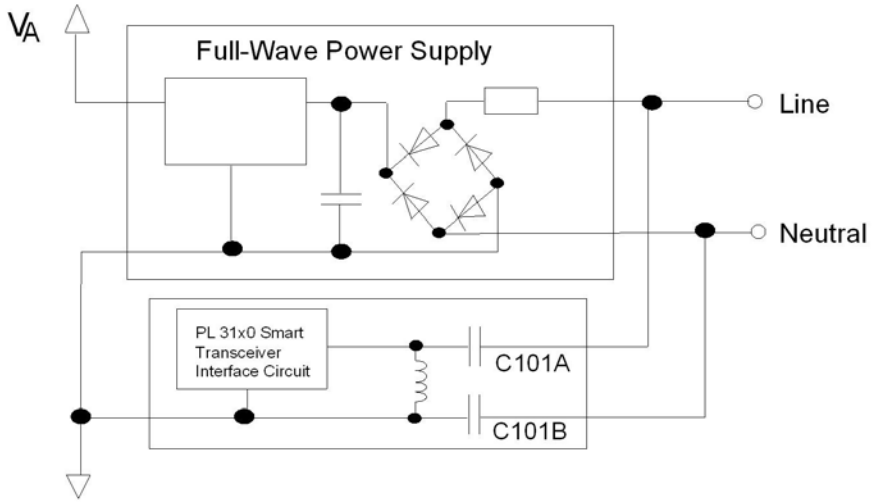


Figure 4.25 Full-Wave Rectified Power Supply and Non-Isolated Floating Coupling Circuit

Power Line Power Supply Plus Coupler

One very convenient coupling circuit implementation combines an isolated universal-input power supply and a line-to-neutral coupling circuit. Figure 4.26 illustrates how such a device is connected to a PL Smart Transceiver-based product. The switch mode power supply inside the combined power supply/coupler provides power for the PL Smart Transceiver-based product while the communication transformer couples the communication signal to the product over a common pair of low-voltage wires. Inside the PL Smart Transceiver-based product the power and communication signals are separated to perform their respective functions. Inductor L106 is used to prevent the low impedance of C103 from shorting out the communication signal. Ferrite bead L102 has been added to ensure stability of the transmit amplifier with the coupling transformer being remotely located from the PL Smart Transceiver. The particular ferrite bead that is specified has been selected to have less or equal to 0.5 ohms of impedance at 100kHz so that a low value of transmit-mode impedance is maintained at communication frequencies. Echelon Corporation sells both 5W and 10W versions of this combined power supply plus coupler. Component values and part numbers for the circuitry to interface with this power supply/coupler are given in example coupling circuit number 8 earlier in this chapter.

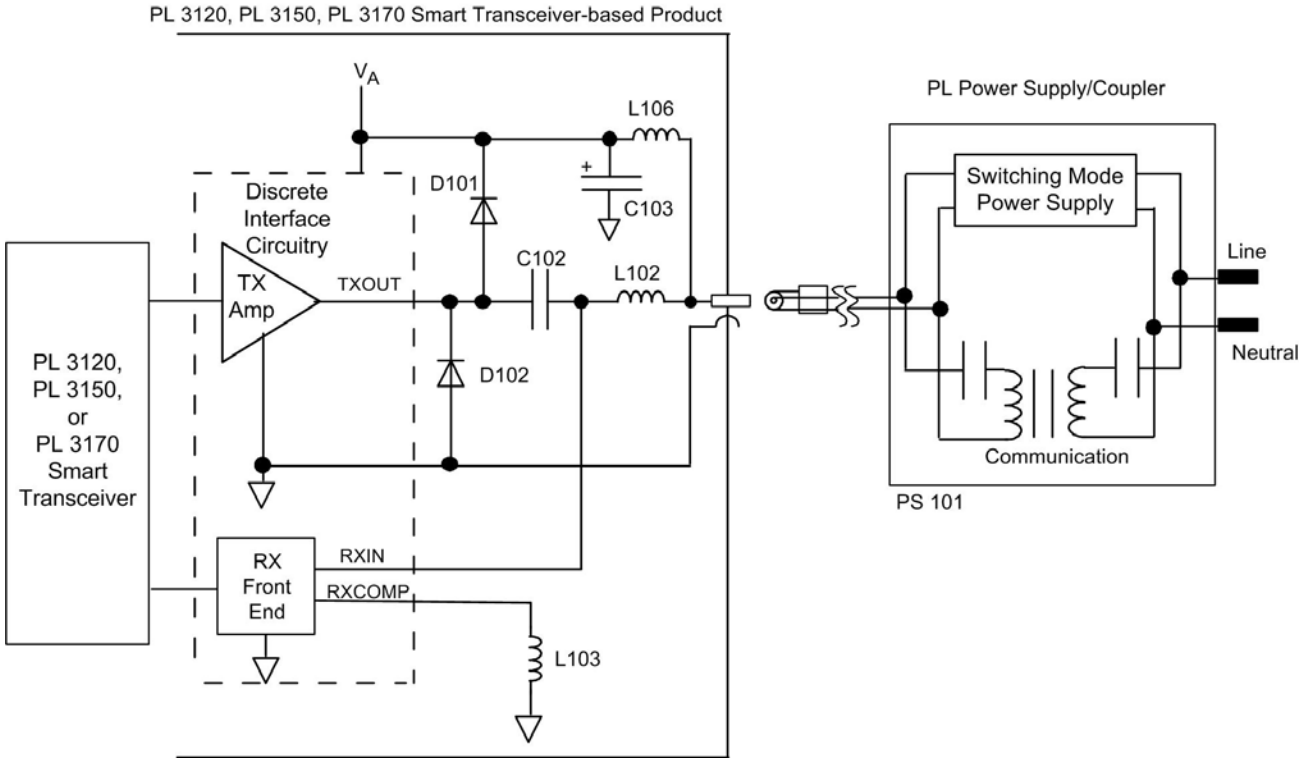


Figure 4.26 Power Line Power Supply Plus Coupler

Low-Voltage Coupling Circuits

While the same coupling circuits that are used to couple to the AC mains can also be used to couple to lower voltage AC or DC lines, simplified and lower cost options are possible for these lower voltage applications. This section discusses the simplifications that are possible when coupling to AC and DC lines with peak voltages below 48V.

For applications where power line communication on power lines with ≤48Vpk voltage is desired, coupling capacitor C101 does not need to have as high a voltage rating as required when coupling to the AC mains. Lower voltages also eliminate the need for a resistor to bleed stored charge from the coupling capacitor. While the user needs to determine the appropriate surge requirements for their particular low-voltage environment (and then perform surge testing applicable to that environment) varistor type protection is not needed in most instances. Fuses are generally not required for these lower voltage coupling circuits.

Low-Voltage AC Coupling Circuits

The simplifications described above are applied to both non-isolated and isolated low-voltage AC coupling circuits given in Examples 9 and 10 in this chapter, respectively.

Low-Voltage DC Coupling Circuits

For applications where power line communication on ≤48V low-voltage DC power lines is required (for example, 12V automotive systems) the coupling circuit can be simplified by removing the high-pass filter components L101 and C101 as shown in Figure 4.27. Component values and part numbers for this circuit are shown in Example 11 in this chapter.

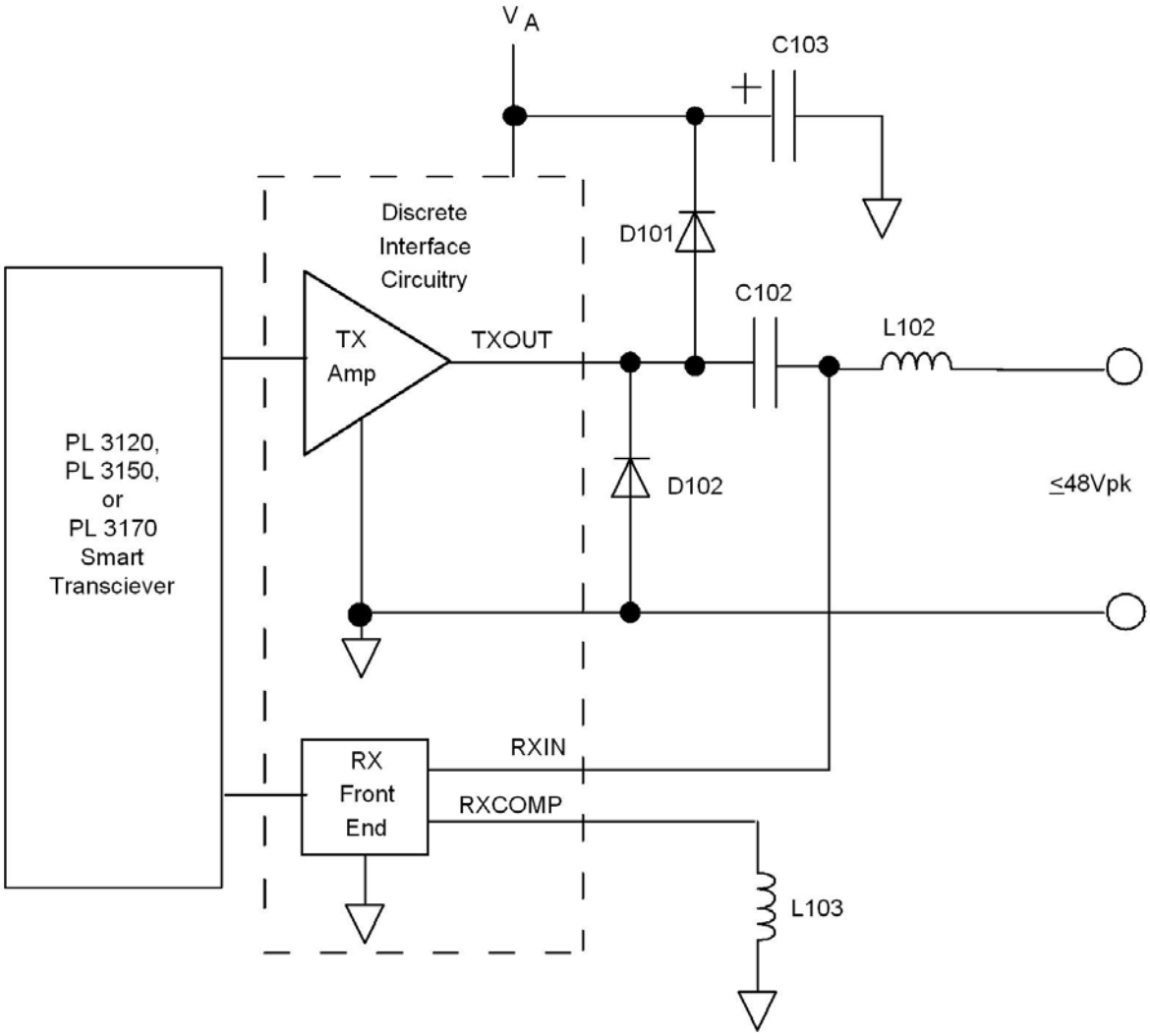


Figure 4.27 Low-Voltage DC Coupling Circuit

Line Surge Protection

Coupling circuits that connect the PL Smart Transceiver to the power mains require the addition of one or more components to provide protection for the PL Smart Transceiver from the high-voltage surges that occur on power distribution systems. Primarily lightning induced, these surges can present voltages of up to 6kV at very high current levels, for brief periods, to the coupling circuits inside buildings and homes. Even higher voltages can be seen on mains wiring outside of buildings.

The level of surge protection required for a given product often depends on the installed location of the product to be protected. Devices connected to branch circuits within a building or home are typically subject to the lowest level of surge stress. Devices connected at, or close to, the power entry point of a building or home (for example, electrical meters and main breaker panels) are subject to higher levels of surge stress. Devices connected to outdoor wiring are subjected to the highest levels of surge stress.

Standard tests for surge immunity are defined in what is commonly called the IEEE surge "Trilogy" (IEEE C62.41.1[8], C62.41.2[9] and C62.45[10], and CEI/IEC 61000-4-4[7]. Both documents classify levels of surge stress by the type of surge waveform (either Ring wave or Combination wave), surge voltage, and surge current. In addition to describing standard test methods, both documents also suggest surge immunity levels based on the application environments described above.

The recommended test procedures described in the two sets of standards are the same, but the suggested immunity levels called out in the IEEE Trilogy substantially exceed the suggested immunity levels of CEI/IEC 61000-4-5. The more severe (and thus more conservative) immunity levels called out in the IEEE Trilogy were used in characterizing the recommended surge protection circuitry shown in the PL Smart Transceiver coupling circuit examples of this chapter (up to the limits of available test equipment).

Metal oxide varistors provide a low-cost, yet effective, way to absorb and divert most transient surge energy away from sensitive circuitry. It is important to select a varistor with a high enough voltage rating so that the varistor will not clamp on occasional long duration line voltage swells - which could otherwise destroy a varistor due to excessive heat. Specifying an appropriate varistor is complicated by the fact that some manufacturers use part numbers that correspond to the DC voltage that results in 1mA of current flow, while other manufacturers number their parts according to the maximum allowable AC voltage. To allow for line voltage swells without damaging the varistor, a part with a DC rating at least 35% above the peak AC line voltage is recommended (e.g., a 470VDC varistor for a 240VAC mains). For AC rated varistors a 25% allowance above the nominal line voltage is recommended (e.g., a 300VAC varistor for a mains voltage of 240VAC). When selecting varistors for use in 3-phase coupling circuits it is wise to also allow for the possibility that the neutral and phase connections might inadvertently be reversed, resulting in 1.7 times the nominal phase-to-neutral voltage across 2 of the 3 varistors. The varistors specified in the coupling circuits shown in this chapter are all selected in accordance with the above guidelines.

Surge protection with earth-return coupling is often constrained by the need to maintain low leakage current. A varistor connected between line and earth adds leakage current that might result in violation of applicable safety standards. For this reason the use of a varistor for surge protection in single-phase line-to-earth coupling circuits is often prohibited. Adequate surge immunity in single-phase branch circuit applications can be achieved without varistors by the use of an X2-type capacitor in the C101 location. Surge immunity of single-phase line-to-earth coupling circuits can be increased to provide protection for power entry and outside wiring applications by the use of a gas tube surge arrester between line and earth. Varistors can be used in 3-phase earth-return applications because the leakage current from each of the phases cancels.

If a gas tube surge arrestor or varistor is used between line and earth, it will have to be loaded on the PCB after hi-pot testing. Hi-pot testing between line and earth is usually performed at voltages above the break-down voltage of gas tube surge arrestors (or the clamp voltage of varistors). The hi-pot test will fail if a gas tube surge arrestor fires (or the varistor clamps) during the testing. Note that the use of gas tube surge arrestors is not recommended in applications where equipment will be powered from an electronic AC power source (as opposed to utility power distribution).

Surge Immunity of Example Circuits

The recommendations for the surge protection components that are included in the example circuits documented in this chapter are based on testing performed on particular PCB layouts. The efficacy of the surge protection implemented in each product containing the PL Smart Transceiver must always be verified empirically using the final product design because factors such as PCB layout and packaging can influence the results as much as the choice of protection components.

Table 4.13 lists the surge levels that the coupling circuits in this chapter can withstand without any damage to the coupling circuit, the PL Smart Transceiver chip, or the PL Smart Transceiver interface circuitry. This criterion of "no damage" is the one most commonly applied for surge testing. A simple and practical way to determine if a device has been damaged after surge testing is to use the production test method described in Appendix D of this data book. Checking the capacitance of C101 and C102 before and after a surge test is also recommended.

Each of the AC mains coupling circuits documented in this chapter was subjected to a sequence of surge events followed by an Appendix D production test and capacitor test to verify that neither the coupling circuit, the Smart Transceiver chip nor the associated discrete interface circuitry were damaged.

The surge waveform type and levels used to test each circuit are listed in Table 4.13. Tests in columns indicating "30 Surge Events" were tested with 5 events of positive polarity and 5 events of negative polarity at each phase angle of 0, 90 and 270 degrees (phase measured relative to the AC mains zero-cross rising edge). Tests in columns indicating "4 Surge Events" were tested with 2 events of negative polarity at 90 degrees and 2 events of positive polarity at 270 degrees. These phase and polarity settings were previously determined to provide the greatest level of stress to the most sensitive components. Multi-phase coupling circuits were tested both with a single phase connected to the surge generator and then again with all phases connected to the generator in parallel.

If the surge requirements for the product under test are different from those described in this section, then it is up to the developer to perform testing in accordance with their own particular requirements. As mentioned above, the efficacy of any surge protection plan must always be verified using samples of the final product because the results can vary with circuit layouts.

Table 4.13 Surge Levels of the Example Coupling Circuits

Example	Coupling Type	Location Type	Ring Wave (0.5µs-100kHz)	Combination Wave (1.2/50µs-8/20µs)	
			Level Tested with 30 Surge Events	Level Tested with 4 Surge Events	Level Tested with 30 Surge Events
1	1-phase, L-N, non-isolated	Branch circuit	6kV/200A	6kV/500A	2kV/1000A
		Power entry	6kV/500A	6kV/3000A	2kV/1000A
		Outdoor	7.8kV/650A	7.4kV/3700A	4kV/2000A
2	1-phase, L-N, isolated	Branch circuit	6kV/200A	6kV/500A	2kV/1000A
		Power entry	6kV/500A	6kV/3000A	2kV/1000A
		Outdoor	7.8kV/650A	7.4kV/3700A	4kV/2000A
3	1-phase, L-E, non-isolated	Branch circuit	4kV/130A	4kV/333A	2kV/1000A
		Power entry	6kV/500A	6kV/3000A	2kV/1000A
		Outdoor	7.8kV/650A	7.4kV/3700A	4kV/2000A
4	1-phase, L-E, isolated	Branch circuit	4kV/130A	4kV/333A	2kV/1000A
		Power entry	6kV/500A	6kV/3000A	2kV/1000A
		Outdoor	7.8kV/650A	7.4kV/3700A	4kV/2000A
5	3-phase, non-isolated	Indoor	6kV/500A	6kV/3000A	2kV/1000A
		Outdoor	7.8kV/650A	7.4kV/3700A	4kV/2000A
6	3-phase, isolated	Indoor	6kV/500A	6kV/3000A	2kV/1000A
		Outdoor	7.8kV/650A	7.4kV/3700A	4kV/2000A
8	Power Supply Plus Coupler	Branch circuit	4kV/130A	4kV/333A	2kV/1000A

It is important to be aware that the PL Smart Transceiver used in conjunction with some of the coupling circuits listed in this chapter might experience a reset event when subjected to higher surge levels. The system designer must determine if their application can tolerate a reset event under high surge conditions.

The level of immunity to reset events under surge conditions varies from one coupling circuit to another – as well as with specific layout. Samples of the example coupling circuits in this chapter have been demonstrated to operate without reset when subjected to surge levels of 2kV. The greatest immunity levels can generally be achieved by locating D101 and C103 such that positive surge currents return to ground without passing close to the PL Smart Transceiver.

If a non-isolated coupling application requires greater reset immunity then the optional components shown in Figure 4.28 can be added. The corresponding optional components to increase reset immunity with isolated coupling circuits are shown in Figure 4.29. Samples of coupling circuits that include these optional components have been demonstrated to not reset when subjected to 6kV surge events.

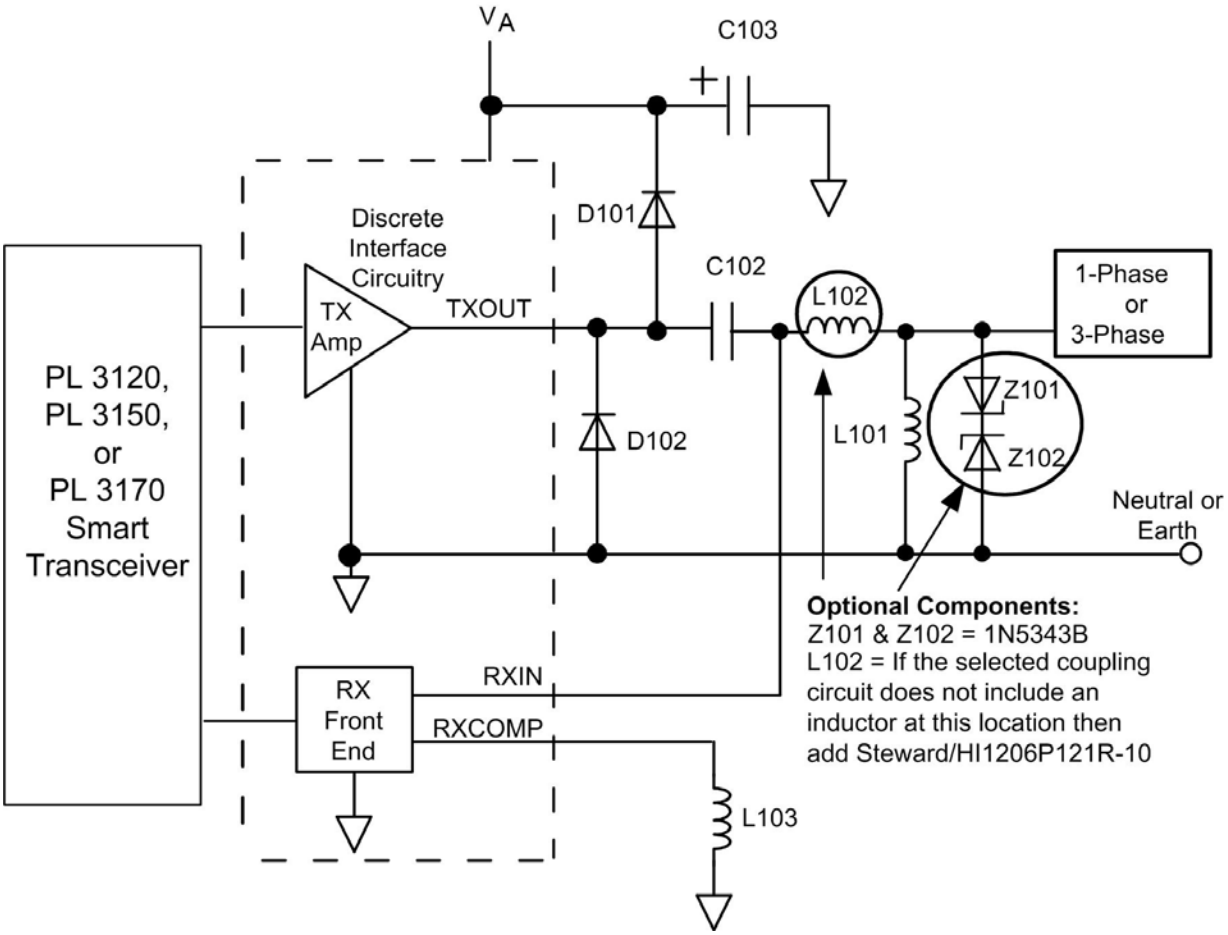


Figure 4.28 Optional Components for Non-Isolated Coupling Circuits

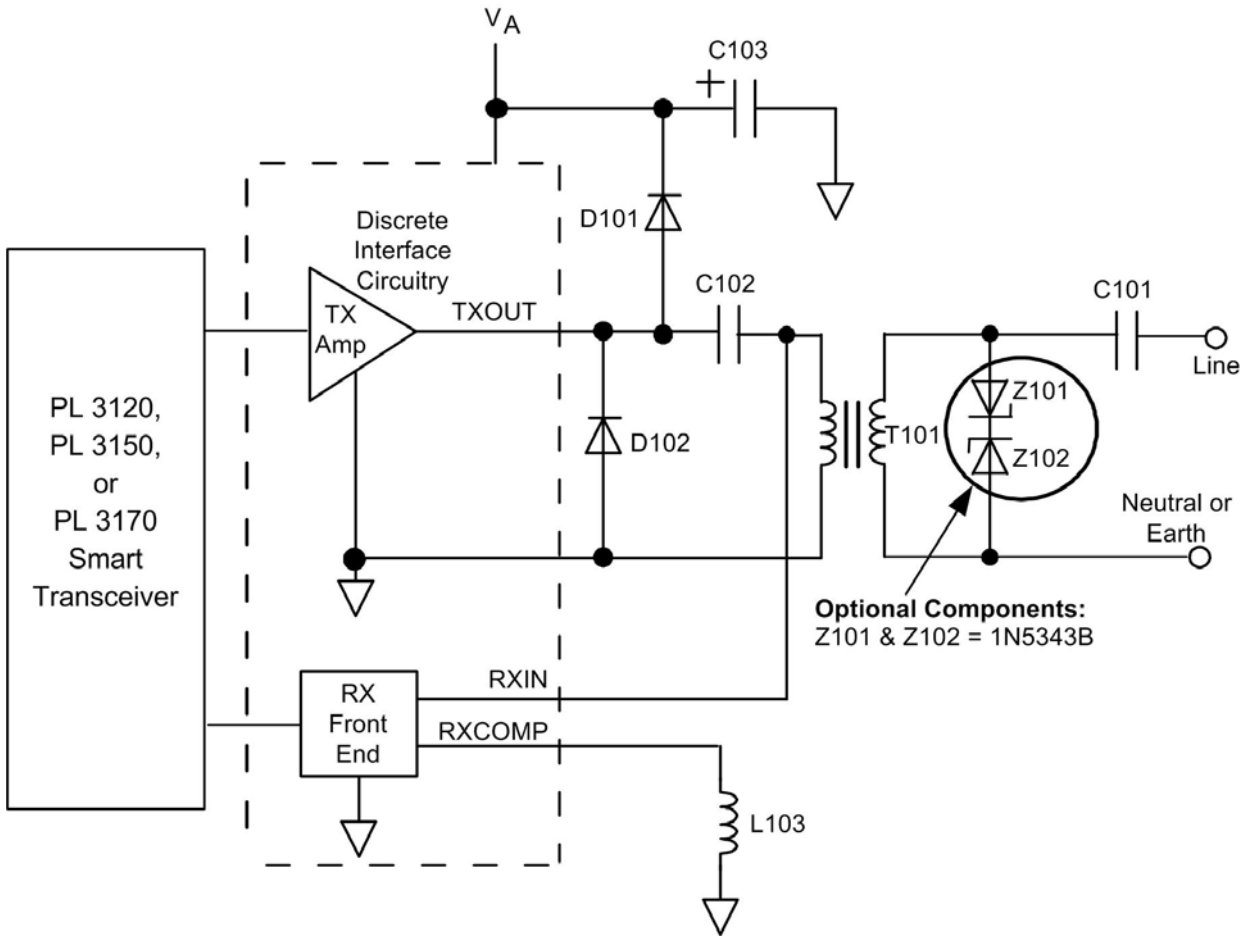


Figure 4.29 Optional Components for Isolated Coupling Circuits

Chapter 5

Power Supplies for PL Smart Transceivers

Introduction

In order to preserve the full communications capability of the PL Smart Transceiver, it is important to ensure that the power supply does not impair communication performance. If not properly designed, a power supply could attenuate the communication signal and couple noise into the transceiver - since the input of the supply is connected directly to the communication channel. Likewise, without proper design, the power supply outputs, V_{DD5} and V_A, have the potential to degrade performance by coupling noise into the PL Smart Transceiver through its supply terminals.

In order to minimize time required to implement a successful product design, several "pre-verified" power supply options (where an instance of the supply has been verified to meet all the PL Smart Transceiver noise and impedance requirements) are documented in this chapter. While testing a product incorporating one of these designs is still necessary, due to differences in layout, use of a pre-verified supply can significantly reduce development time. For those who wish to design their own unique supply, or embed a PL Smart transceiver into a product with an existing supply, the information necessary to accomplish this without impairing communications is also provided in this chapter.

The pre-verified power supplies listed in this chapter support the transceiver reference designs from Appendix A that incorporate the standard PL transmit amplifier with a 1Ap-p current limit. While the voltage and current requirements for the optional 2Ap-p reference amplifier differ, the noise and impedance requirements from this chapter are also applicable to design of a supply that supports this optional high power amplifier. The voltage and current requirements for the PL Smart Transceiver and Reference circuitry are listed in Tables 5.1 through 5.3 below.

Table 5.1 Power Supply Requirements for PL 3120, PL 3150 and PL 3170 Smart Transceivers ICs

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD5}	V_{DD5} 5V PL IC Digital Power Supply	4.75	5.00	5.25	V
V_{DD5A}	V_{DD5A} 5V PL IC Analog Power Supply	4.60	5.00	5.25	V
I_{DD}	PL 3120/PL 3170 Smart Transceiver V_{DD5}+V_{DD5A} Supply Current (not including I/O or internal pull-up current)		9	13	mA
I_{DD}	PL 3150 Smart Transceiver V_{DD5}+V_{DD5A} Supply Current (not including I/O or internal pull-up current)		12	16	mA

Table 5.2 Power Supply Requirements for Standard 1Ap-p Transmit Amplifier Reference Circuit

Symbol	Parameter	Min	Typ	Max	Unit
V_{ARX}	V_A Supply Voltage - Receive mode	8.5	12.0	18.0	V
V_{ATX}	V_A Supply Voltage - Transmit mode (1), (2)	10.8	12.0	18.0	V
I_{ARX}	V_A Supply Current - Receive mode		350	500	µA
I_{ATX}	V_A Supply Current - Transmit mode		120	250	mA

Table 5.3 Power Supply Requirements for Optional 2Ap-p Transmit Amplifier Reference Circuit

Symbol	Parameter		Min	Typ	Max	Unit
V_{ARX}	V_A Supply Voltage - Receive mode		12.0	15.0	18.0	V
V_{ATX}	V_A Supply Voltage - Transmit mode (2)	C-band A-band	14.25 12.0	15.0 15.0	18.0 18.0	V V
I_{ARX}	V_A Supply Current - Receive mode			350	500	µA
I_{ATX}	V_A Supply Current - Transmit mode			160	500	mA

Note 1: When using the 1Ap-p transmit amplifier, V_A must be ≥10.8V under typical line voltage and current draw conditions (including typical V_A transmit current of 120mA). The minimum transmit V_A voltage can be relaxed to 8.5V when worst case line voltage, component tolerance and transmit power supply loading are present (including a maximum V_A transmit current of 250mA).

Note 2: When using a supply voltage above 12.6V the following formula must be satisfied. The table below the formula illustrates the formula results for common input values.

$$V_{ATXAVE} < (150-T_{AMAX})/(K*D_{MAX});$$

Where: V_{ATXAVE} = Average V_A supply voltage while transmitting
T_{AMAX} = Maximum ambient temperature inside the product enclosure (degrees C)
D_{MAX} = Maximum transmit duty cycle of the device (expressed as a decimal number where 0.64 is the practical max)
K = 8.0 for most 1Ap-p TX amplifier designs and 5.6 for the 2Ap-p TX amplifier designs (See Appendix A)

T_{AMAX}	D_{MAX}	V_{ATXAVE} w/1Ap-p Amp	V_{ATXAVE} w/2Ap-p Amp
85C	64%	12.7V	18V (V_A max limit)
70C	64%	15.6V	18V (V_A max limit)
85C	45%	18V (V_A max limit)	18V (V_A max limit)
70C	55%	18V (V_A max limit)	18V (V_A max limit)

Power Supply Options

There are a number of power supply options available for use with the PL Smart Transceivers. These various options differ in key characteristics such as size and cost. The following table is designed to aid in power supply selection.

Table 5.4 Power Supply Options

Power Supply Type	**Application Current**	**Safety-Isolated**	**Universal Input** (see Note 1)	**Relative Cost** (see Note 2)	**Relative Size** (see Note 2)	**Pre-Verified Version Available**	**Page**
Energy Storage Capacitor Input	≤25mA	No	No	1	1	Yes	158
Energy Storage Linear	≤10mA	Yes	No	2	2	Yes	161
Traditional Linear	Any	Yes	No	3	≥3	No	162
Energy Storage Switcher	≤10mA	Yes	Yes	4	1	Yes	162
Pre-verified Isolated Switcher	≤100mA	Yes	Yes	3	3	Yes	164
5W Echelon Power Supply Plus Coupler	≤140mA	Yes	Yes	8	5	Yes	168
10W Echelon Power Supply Plus Coupler	≤640mA	Yes	Yes	10	7	Yes	168
Off-the-shelf Switcher	Any	Yes	Yes	≥5	≥5	No	169
Full Custom Switcher	Any	Optional	Optional	≥3	≥3	No	169

Notes: 1. Multi-country line voltage support without switches 2. Relative rank of 1 = low and 10 = high.

Energy Storage Power Supplies

PL Smart Transceivers incorporate a power management feature that supports the design of low cost power supplies in cost sensitive consumer applications such as networked light dimmers, switches, and household appliances. This class of application typically requires only occasional low-duty cycle transmission from the device. Power supplies for these devices can take advantage of the very low receive current and wide V_A supply range of the PL Smart Transceiver to charge a capacitor during receive mode, and then use the energy stored on the capacitor for transmission. By using an energy storage system, the device can use a smaller, less expensive, power supply than a device with an equivalent "full power" supply. In this way, a low-current supply can be used which only has to supply the required receive mode current, plus an incremental current to recharge a capacitor between transmissions.

An energy storage power supply is generally designed so that its V_A supply voltage, while in receive mode, is above the 12V nominal specification (e.g., 15V). During packet transmission the voltage on the V_A supply is then allowed to drop as energy from the capacitor is used for transmission. The value of the energy storage capacitor must be large enough so that the V_A supply voltage is still sufficient for proper operation after transmitting a single maximum-length packet. Proper device operation is then maintained when the energy storage capacitor is selected such that the V_A power supply meets both of the following conditions:

- $V_A \geq 10.8$V after the typical I_A transmit load of 120mA has been active for 92.2ms for a C-band device (140.7ms for an A-band device). This condition only needs to be met at room temperature with nominal AC line voltage (see footnote below regarding derivation of transmission times).
- $V_A \geq 8.5$V after the worst case I_A transmit load of 250mA has been active for 92.2ms for a C-band device (140.7ms for an A-band device). For proper node operation this condition must be met over the full range of worst-case component tolerances (including I_{DD5} drain), AC line voltage, and temperature (see footnote below regarding derivation of transmission times).

Having chosen a storage capacitor to provide adequate voltage after transmitting a single packet, the power management feature of the PL Smart Transceiver must also be enabled to ensure adequate supply voltage over the span of multiple packet transmissions. The power management feature prevents excessive power supply droop from transmission of multiple back-to-back packets under worst case conditions by monitoring the voltage on the energy storage capacitor and then, if required, regulating the time between transmissions so that the capacitor has time to recharge.

The power management feature is enabled by first connecting an appropriate resistive voltage divider between the V_A supply and the OOGAS pin of PL Smart Transceiver IC, as shown in reference schematic diagrams described in Appendix A. In addition, use of a standard transceiver type with a "-LOW" suffix is required to enable the power management feature, as described in Chapter 8, *PL Smart Transceiver Programming*.

Note: For the primary carrier frequency, a 32 byte packet (without preamble but including CRC) corresponds to a maximum transmission duration of 74.6ms for a C-band device and 113.8ms for an A-band device. Calculating the maximum transmission duration for a packet at the secondary carrier frequency is somewhat more complicated due to the combination of error correction and data compression used with that carrier frequency. If we consider a case where message traffic satisfies the 32 byte packet length condition plus three further common conditions, then the maximum transmission duration can be calculated to be 92.2ms for a C-band device (140.7ms for an A-band device). This maximum duration is applicable for applications where: 1) there are no priority packet transmissions from the energy storage device; 2) subnet and node numbers are in the range 0 through 15; and 3) if a six byte domain is used, it is assigned to be equal to a Neuron core ID number. For applications which do not meet the conditions listed in this note, contact Echelon Lon Support for maximum packet length calculations.

Once enabled, the power management system detects any instance where the V_A supply drops below the Smart Transceiver's lower power management threshold (nominally 7.9V). The PL Smart Transceiver then delays transmission until the energy storage capacitor has been recharged, to allow transmission of a complete packet. The PL Smart Transceiver then transmits any waiting packets once the capacitor has fully charged.

If a high packet transmission duty cycle causes V_A to drop too low during packet transmission, then the packet is aborted prior to completion. The PL Smart Transceiver will re-transmit that packet independent of the LonTalk protocol service in use. Even when unacknowledged service is employed, a packet that is interrupted by low supply voltage will be re-transmitted once the power management system determines that the supply is fully recharged.

The power management circuitry of the PL Smart Transceiver adjusts the amount of time that it inhibits transmission based on the actual recharge characteristics of the device. A properly designed energy storage device will typically transmit without intervention by the power management circuitry. When a device powered by an energy storage supply has worst case component tolerances and is exposed to worst case AC line conditions, such that a packet must be aborted and retransmitted, the power management circuitry of the Smart Transceiver calculates a suitable transmit hold-off time by measuring the supply recharge rate. The formula used to make this calculation is three times the time required for the supply to charge from its lower power management threshold (nominally 7.9V) to its upper power management threshold (nominally 12.1V). Figure 5.1 illustrates examples of an energy storage node operating under both typical and worst case conditions.

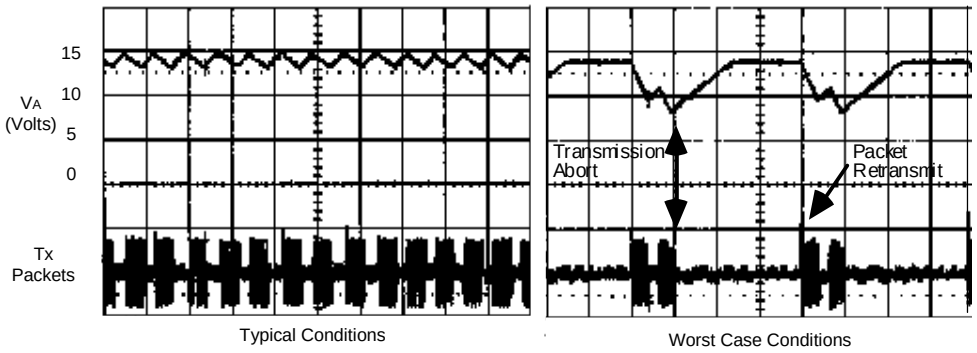


Figure 5.1 Supply Voltage vs. Packet Transmission

Energy Storage Capacitor-Input Power Supplies

A particularly cost-effective example of an energy storage power supply is the *capacitor-input power supply.* The most attractive feature of this supply is that both the V_A and V_{DD5} supplies can be built with just a few components for approximately US$1.00.

Figure 5.2 illustrates the operation of a capacitor-input power supply. As shown in the figure, a capacitor in series with the AC mains causes AC current to flow through a zener diode, which acts as a shunt regulator. This regulator is selected to limit the V_A supply voltage to ≤16V. An energy storage capacitor is connected across the shunt regulator to provide current capacity required for transmission. Note that unused source current flows through the shunt regulator. This maximizes the zener diode temperature when the supply load is at a minimum. Because the regulation voltage of a >10V zener diode has a strong positive temperature coefficient, a pair of forward-biased silicon diodes, which have negative temperature coefficients, have been added in series with a slightly lower-voltage zener diode. Note that this type of capacitor-input power supply would inherently attenuate communication signals, due to its low impedance, if not for the addition of a series inductor, as shown in Figure 5.2

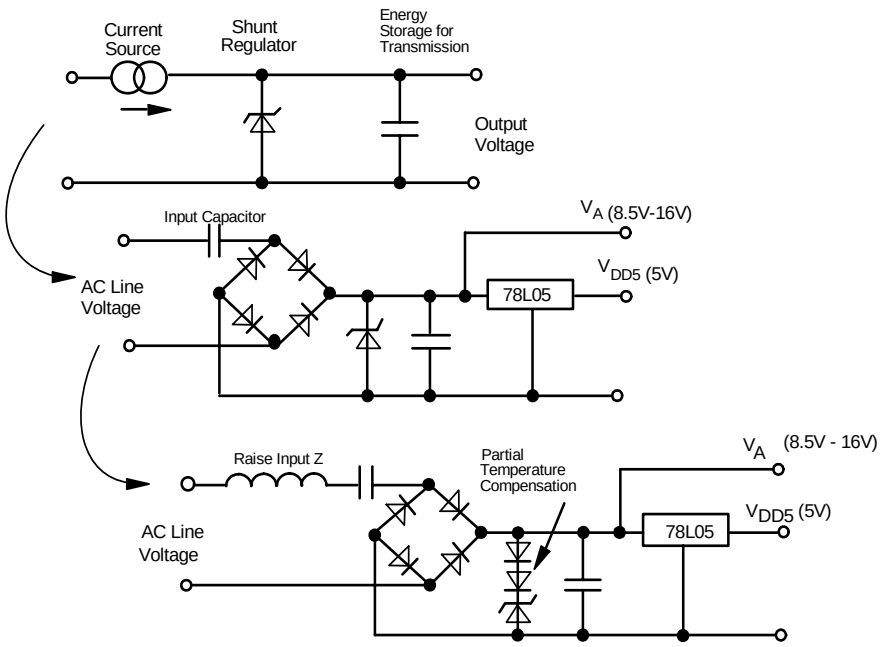
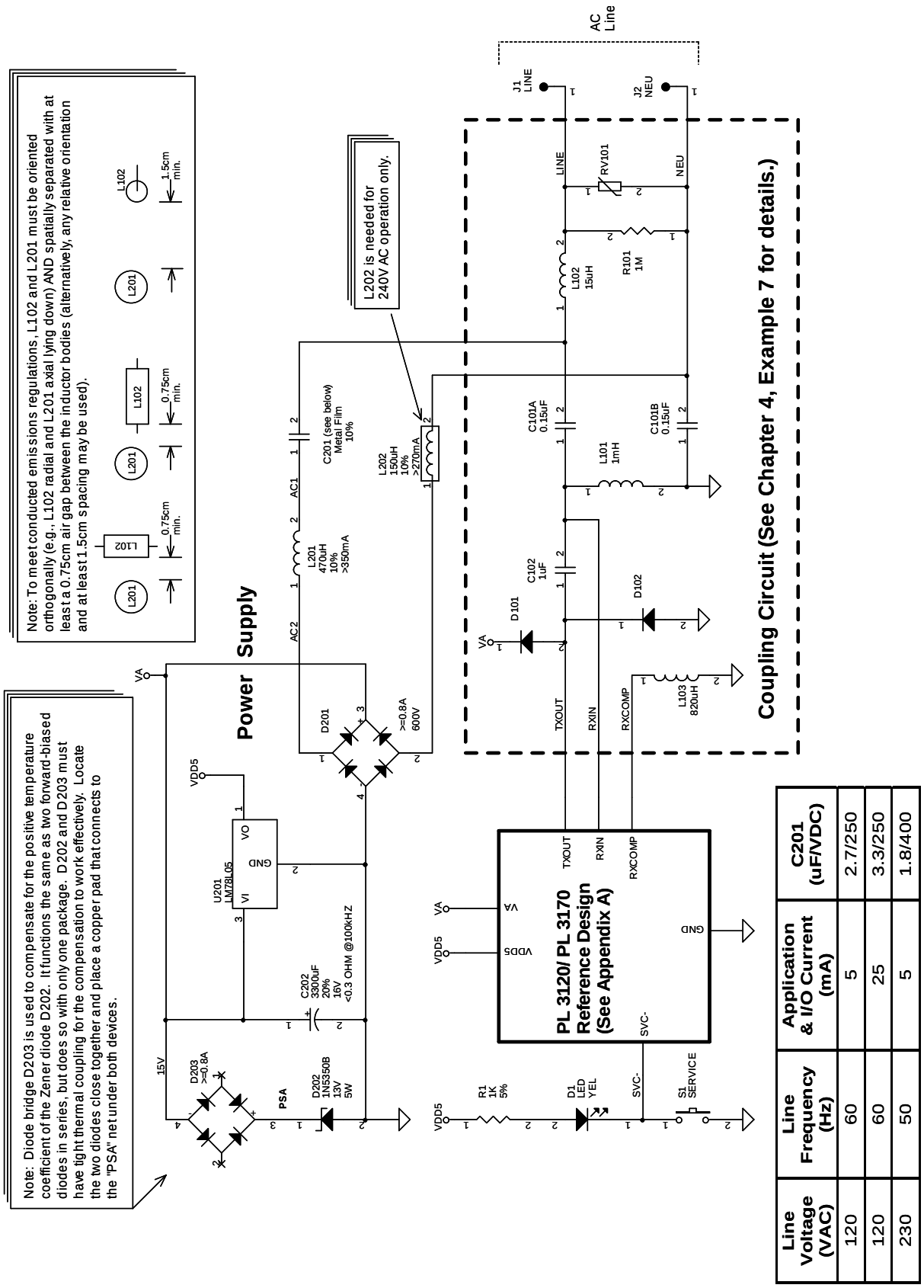


Figure 5.2 Capacitor-Input Power Supply Theory of Operation

Due to the low available current, the use of capacitor-input power supplies is generally limited to PL 3120 and PL 3170 based devices which require minimal I/O and application current (e.g., latching relays, SCR triggers, low-power LEDs). Figure 5.3 presents a schematic for a C-band device based on a PL 3120 or PL 3170 Smart Transceiver IC powered by a capacitor-input power supply. Figure 5.4 shows the A-band version. These devices are designed to operate with an enclosure internal air temperature range of 0-70°C.

The C-band versions provide enough stored energy to transmit a 92.2ms packet under worst-case conditions prior to recharging. The A-band option provides sufficient stored energy to transmit one complete 140.7ms packet under worst-case conditions prior to recharging. Under typical conditions, the C-band and A-band versions support a maximum transmit duty cycle of ≥65%. Under worst-case conditions, they each support maximum transmit duty cycles of ≥10%. Note that the use of any of these capacitor-input power supply options requires that the configuration data of the device be programmed to enable power management, as described in Chapter 8.



Line Voltage (VAC)	Line Frequency (Hz)	Application & I/O Current (mA)	C201 (uF/VDC)
120	60	5	2.7/250
120	60	25	3.3/250
230	50	5	1.8/400

Figure 5.3 C-band Capacitor-Input Power Supply Schematic

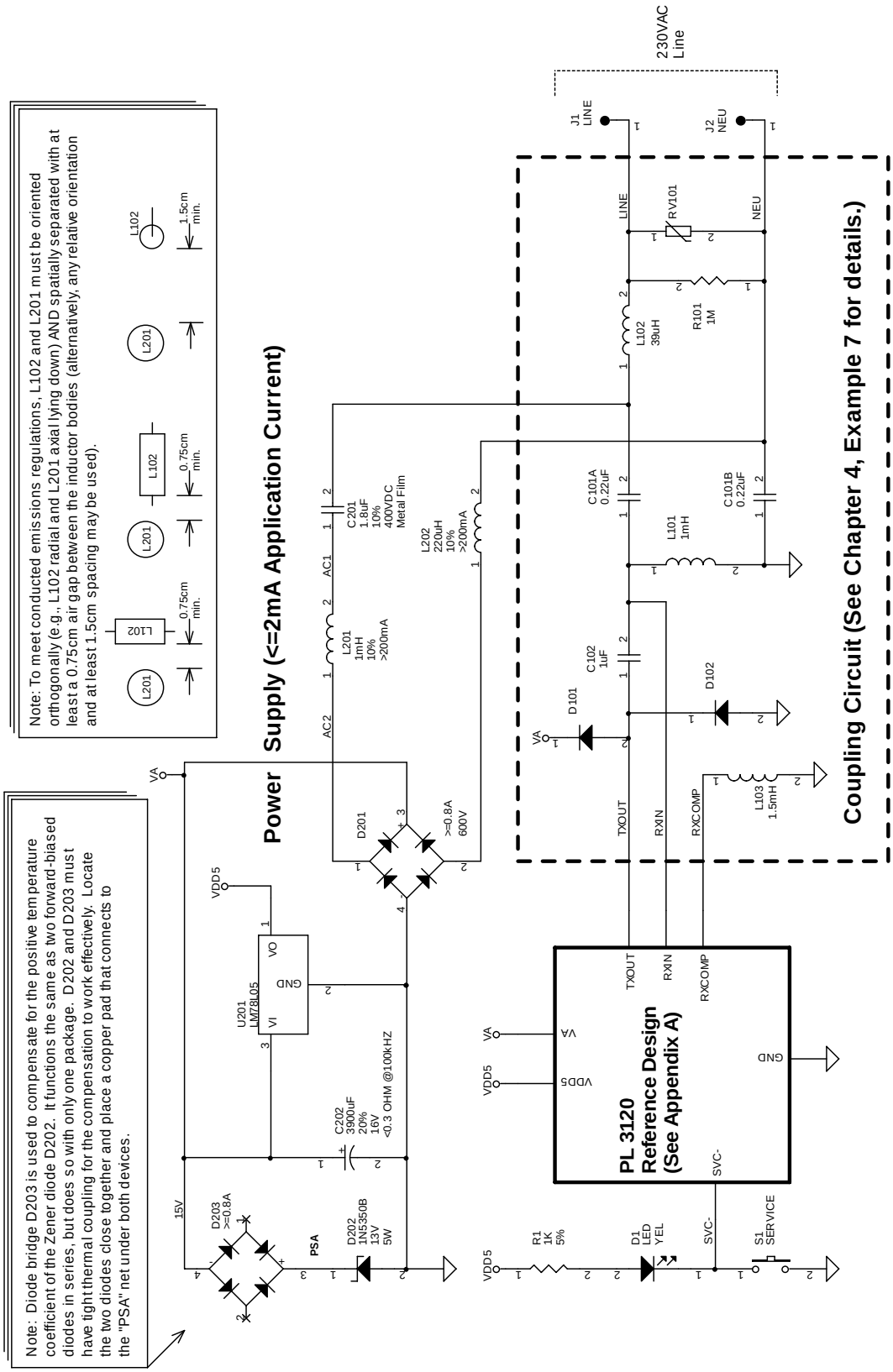


Figure 5.4 A-band Capacitor-Input Power Supply Schematic

Energy Storage Linear Supplies

For products requiring minimal application current and safety isolation, an energy storage linear supply is a small cost effective option. Consider a device based on a PL 3120 or PL 3170 Smart Transceiver consuming 10mA of application and I/O current. Using a linear V_A power supply and a linear regulator for the V_{DD5} supply, the worst case current requirements are presented in the table below.

Table 5.5 Worst-Case Device Current Consumption Example

	Transmit	**Receive**
V_A Current	250mA	0.5mA
PL 3120/PL 3170 Smart Transceiver V_{DD5} Current	13mA	13mA
Application & I/O Current	10mA	10mA
78L05 Regulator Current	5mA	5mA
Total	278mA	29mA

A traditional linear supply would require a transformer with an output current rating of ≥300mA. By taking advantage of the PL Smart Transceiver's power management feature, an energy storage linear supply can be built with a 100mA transformer.

Figure 5.5 shows an example of an energy storage linear supply. This example supply meets the criteria listed in the energy storage section of this chapter, for both C-band and A-band operation. With a transient load of 120mA for 140.7ms added to a constant 29mA receive load, this supply does not drop below 10.8V. This supply also maintains ≥9.0V after a 250mA load is added to the constant 29mA load for 140.7ms. Both of these criteria hold true even with an AC line voltage that is 10% low and an output capacitance value that is 20% below nominal. In addition, this example supply supports transmit duty cycles of ≥65% under typical conditions and ≥10% with worst case line voltage and component tolerances.

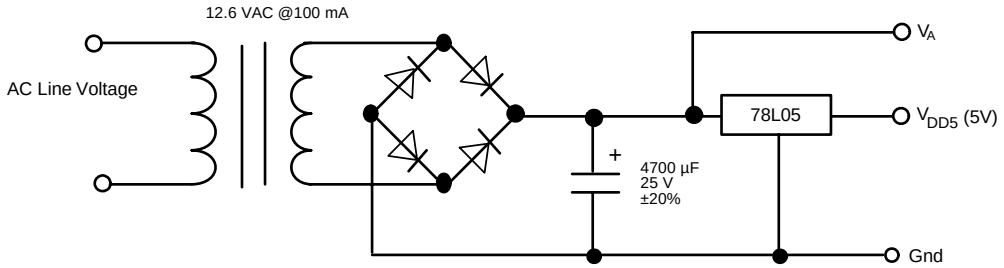


Figure 5.5 Energy Storage Linear Power Supply

In summary, an energy storage linear supply differs from a traditional linear supply in the following ways:

- Allows the use of a smaller transformer
- Requires more output capacitance for energy storage
- Requires that the device be programmed to enable power management, as described in Chapter 8.
- Under typical conditions, exhibits transmit duty cycles which are not limited. Over the full range of line voltage and component tolerance, the power management circuitry of the PL Smart Transceiver may act to regulate transmit duty cycle of the device (to ≥10% in the above example).

Traditional Linear Power Supplies

This option is usually suitable if the physical size of the power supply is not constrained by the application, since linear supplies tend to be physically larger than switching power supplies. Linear power supplies do not load the power line in the range of the PL Smart Transceiver communication frequencies, nor do they generate significant noise. For these reasons, a linear power supply can be used without concern that communication performance will be adversely affected by the supply.

Pre-Verified Switching Power Supplies

Switch mode power supplies provide a number of desirable features such as multi-country support and optional circuit isolation. While generally smaller than linear power supplies, switching power supplies can be a significant source of noise and power line signal attenuation unless they are specifically designed to avoid these effects. To minimize development effort, three types of switching power supplies have been pre-verified to preserve the high performance communication capabilities of the PL Smart Transceiver. These three types are listed below and described in detail in the sections that follow.

- Pre-Verified Energy Storage Switching Supply
- Pre-Verified Switching Supply
- 5W and 10W Echelon Power Supply Plus Couplers

Pre-Verified Energy Storage Switching Supply

Bias Power LLC has developed a small (2.6 x 2.3cm), switching power supply module that has been tested for compatibility with the PL 3120 and PL 3170 Smart Transceivers. This power supply option is a good choice when the benefits of a switching supply (small size, universal input, safety isolation, and good efficiency) are needed but simplicity of design is also a priority.

The Bias Power LLC BPS 1-14-00 power supply module provides approximately 1 watt of output power at 14VDC. It must be operated as an energy storage supply by the addition of an energy storage output capacitor. Figure 5.6 illustrates the required application schematic for use of the BPS 1-14-00 module with the PL 3120 or PL 3170 Smart Transceivers. Note that a simple RC circuit has also been added to the input of the Bias Power module in order to avoid any degradation of power line communication signals due to excessive noise or loading. Note also that because this is an energy storage design the power management feature of the PL Smart Transceiver must be enabled as described in Chapter 8.

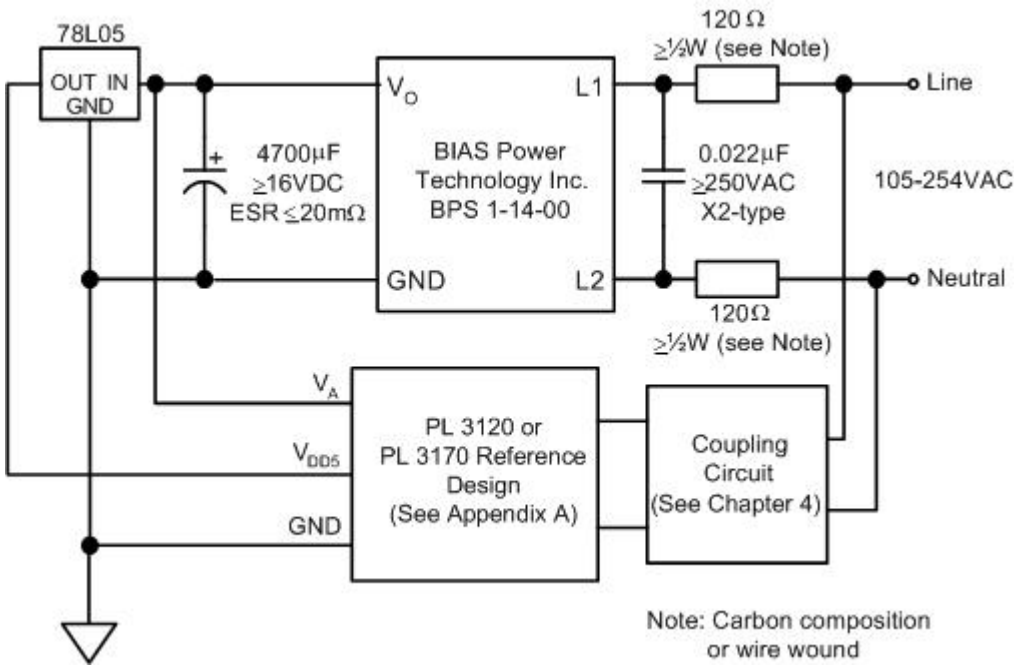


Figure 5.6 Pre-verified Energy Storage Switching Supply Schematic

The circuit in Figure 5.6 supports the power requirements of the PL 3120 and PL 3170 Smart Transceiver in conjunction with 10mA of application current. The design has been verified to meet the energy storage power supply requirements described earlier in this chapter. Specifically, it provides ≥10.8V after a transient load of 120mA for 140.7ms has been added to a 19mA static load (9mA PL Smart Transceiver typical I_{DD5} + 10mA application current) under conditions of nominal AC line voltage and room temperature. In addition it has been verified to provide ≥8.5V after a 250mA load has been added for 140.7ms to a 23mA static load (13mA PL Smart Transceiver maximum I_{DD5} + 10mA application current) with 105VAC line voltage, -20% output capacitor tolerance and either 0C or 70C ambient temperatures. It supports typical transmit duty cycles of >65% and worst case transmit duty cycles of ≥30%.

This combination of Bias Power BPS 1-14-00 module and Echelon PL 3120 or PL 3170 Smart Transceiver has been verified to pass all of the communication performance tests described in Chapter 7. In addition, a sample of the BPS 1-14-00 used with the application schematic of Figure 5.6 has been verified to pass EN50065-1 and FCC regulations for conducted emissions. The user of this circuit must perform regulatory qualification of their own particular product, but this design has been found to be relatively insensitive to layout variations.

Further information regarding the Bias Power BPS 1-14-00 module contact:

Bias Power LLC www.biaspower.com

A Pre-Verified Isolated Switching Supply

When significant application current is required and small size, universal input, safety isolation and/or good efficiency are also desired, the power supply described in this section is an excellent choice. This design is based on the STMicroelectronics VIPer®20A off-line switch-mode power supply IC.

This pre-verified power supply provides a total output current of 363mA at 12V. It thus supports 100mA of application and I/O current after allowing for 250mA of the worst case V_A current and 13mA of worst case V_{DD5} current of a PL 3120 or PL 3170 Smart Transceiver IC. The specifications for this supply are listed in Table 5.6, the application schematic is provided in Figure 5.7, the bill of material (BOM) is provided in Table 5.7 and a recommended PCB layout is provided in Figure 5.8.

Table 5.6 Pre-Verified Isolated Switching Supply Specifications

Parameter	Min	Typ	Max	Units
Input voltage	90	230	254	VAC
V_A output voltage	10.8	12.4	14.0	VDC
V_{DD5} output voltage	4.75	5.0	5.25	VDC
Output load current (V_A+V_{DD5})	10	150	363	mA
Switching frequency	46	51	55	kHz
Ambient operating temperature	-40	25	85	C

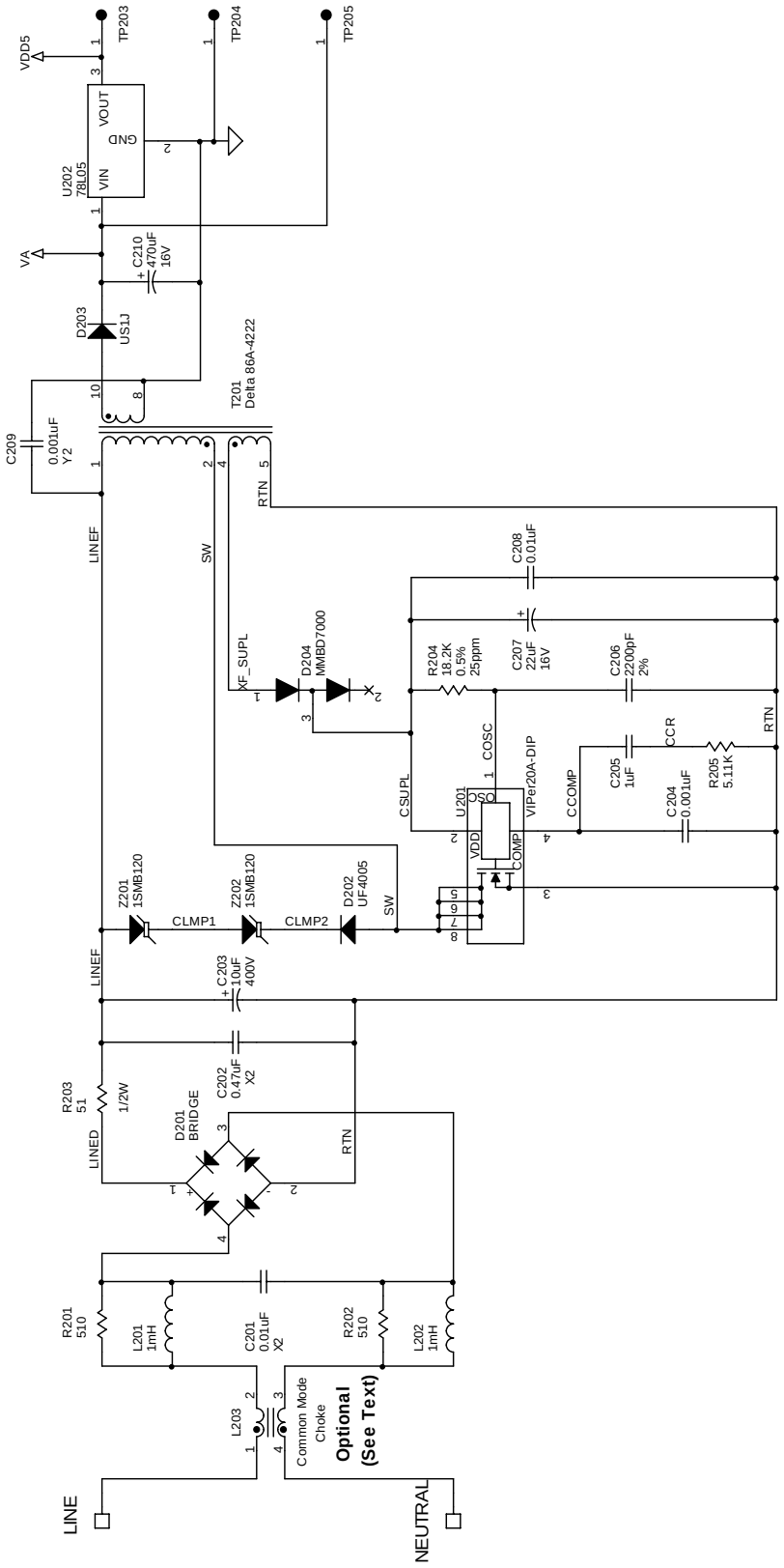


Figure 5.7 Pre-Verified Isolated Switching Supply Schematic

Table 5.7 Pre-Verified Isolated Switching Supply Bill of Materials (BOM)

Component	Value	Required Specifications	Example Vendor / Part #
R201, R202	510Ω	±5%, ≥1/4W, overload voltage ≥500V	Generic
R203	51Ω	±5%, ≥1/2W, carbon composition or wire-wound	KOA/RC1/2TT52A510J
R204	18.2kΩ	±0.5%, ≥1/16W, ≤25ppm/C, 0603	Susumu/RR0816P-1822-D
R205	5.11kΩ	±1%, ≥1/16W, 0603	Generic
C201	0.01µF	±20%, ≥250VAC, X2 type	Panasonic/ECQ-U2A103ML
C202	0.47µF	±20%, ≥250VAC, X2 type	Panasonic/ECQ-U2A474ML
C203	10µF	±20%, ≥400VDC, aluminum electrolytic	Nichicon/UPW2G100MHD
C204	0.001µF	±10%, ≥25VDC, X7R, 0603	Generic
C205	1.0µF	±10%, ≥10VDC, X7R, 0805	Kemet/C0805C105K8RAC
C206	2200pF	±2%, ≥25VDC, NPO, 0603	Generic
C207	22µF	±20%, ≥16VDC, tantalum, EIA size B	Kemet/T491B226M016AT
C208	0.01µF	±10%, ≥25VDC, X7R, 0603	Generic
C209	0.001µF	±20%, ≥250VAC, Y2 type	Vishay/WYO102MCMBF0K
C210	470µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.1Ω ESR @100kHz/20C, 500≥mA$_{RMS}$ ripple current @105C	Nichicon/UHE1C471MPD
D201	0.8A	V_R ≥600VDC, bridge rectifier	Shindengen/S1ZB60
D202	1A	V_R ≥600VDC, V_F ≤1.7V@1A/25C, reverse recovery ≤75ns	Generic/UF4005
D203	1A	V_R ≥50VDC, V_{Fmax}@1.7V@1A/25C, reverse recovery ≤75ns, SMA	Generic/US1J
D204	Dual Diode	I_F≥100mA, 550≤V_F≤700mV@1mA, V_R≥75V, SOT-23	Generic/MMBD7000
Z201, Z202	120V	600 watt peak power, transient voltage suppressor, SMB	ON Semi/1SMB120AT3G
L201, L202	1.0mH	±10%, Imax ≥250mA	Taiyo Yuden//LHL08TB102J
L203	3.9mH	Optional common-mode choke, ≥300mA	Sumida/UU9LFHNP-HB392
T201	Transformer	Delta 86A-4222A isolation transformer	Delta/86A-4222A
U201	VIPer20A-E	VIPer20A switch-mode power supply IC, DIP-8	STMicroelectronics/VIPer20A-E
U202	5V regulator	LM78L05 or equivalent, SOT-89	Generic/LM78L05

Example Vendor Websites

Delta Electronics www.delta.com.tw	**Shindengen** www.shindengen.com
Kemet Corporation www.kemet.com	**STMicroelectronics** www.st.com
KOA www.koaspeer.com	**Sumida Corporation** www.sumida.com/en/products
Nichicon www.nichicon-us.com	**Susumu** www.susumu.co.jp
ON Semiconductor www.onsemi.com	**Taiyo Yuden** www.ty-top.com
Panasonic www.panasonic.com/industrial/components	**Vishay** www.vishay.com

The performance of this power supply is somewhat sensitive to layout. Minimizing the length of the net from the Drain of the VIPer20A IC is of particular importance in controlling conducted emissions. In order to reduce the time required to successfully implement this supply, a recommended layout is provided below.

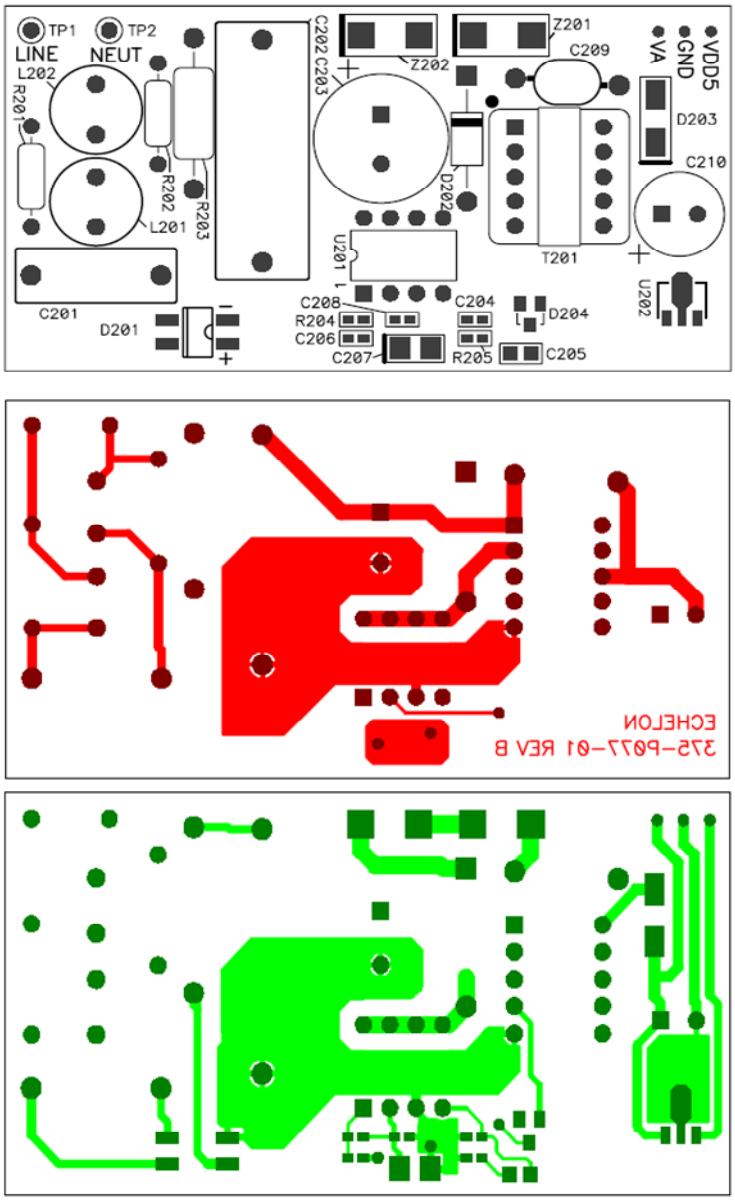


Figure 5.8 Recommended Layout of the Pre-Verified Isolated Switching Supply

While each new product must be verified for regulatory compliance and communication performance, using this supply simplifies the development task since an instance of this design has been pre-verified. This supply was tested in combination with PL 3120 Smart Transceiver reference design #1217 from Appendix A and the isolated Line-to-Neutral coupling circuit Example 2 from Chapter 4. This combination passed EN50065-1 and FCC regulations for conducted emissions with 8dB of margin when the output of the supply was floating (not connected to earth ground). In applications requiring a grounded output, adding the optional common mode choke provides a passing result. This supply and PL reference design was also verified to pass all of the communication performance tests of Chapter 7. In addition, this supply and coupling circuit combination passed the surge tests documented for the Example 2 coupling circuit in Table 4.14 in Chapter 4.

5W and 10W Echelon Power Supply Plus Couplers

One very convenient power supply implementation combines an isolated universal-input power supply and a C-band line-to-neutral coupling circuit into a single package. The power supply inside the combined unit provides power for a PL Smart Transceiver-based product while a communication transformer couples the communication signal to the product over a common pair of low-voltage wires. A simple interface circuit is then used inside the PL Smart Transceiver-based product to separate the DC power and communication signals. Details of this interface circuit are provided in coupling circuit Example 8 in Chapter 4. Detailed specifications for these units are given in the data sheet for Echelon model 78101R and 78113R power supplies (5watt and 10 watt versions respectively).

Figure 5.9 Echelon Power Supply Plus Coupler

Off-the-Shelf and Custom Switching Power Supplies

As mentioned earlier, switching power supplies can be a significant source of noise and signal attenuation unless specifically designed to avoid these effects. As a result, the input impedance of a switching power supply that has not been pre-verified must be evaluated and an inductor will most likely need to be added to its input as described later in the section titled *Power Supply-Induced Attenuation*. In addition, a switching power supply that has not been pre-verified to meet the input and output noise requirements presented later in this chapter may need additional filtering components.

Selection of an appropriate operating frequency for a switching power supply will minimize the effect of switching noise on communication performance. By choosing an operating frequency such that the fundamental and harmonics of that switching supply avoid the transceiver's communication frequencies, the amount and cost of additional filter components will be minimized. Table 5.8 lists the recommended switching frequency ranges. The switching supply should be designed such that the fundamental switching frequency falls within the stated ranges under all line, load, environmental, and production conditions. Supplies with other fundamental operating frequencies may be able to meet the required noise masks with greater effort and/or cost; however, meeting the noise requirements with a power supply fundamental frequency (or second or third harmonic) in the 70kHz to 90kHz or 110kHz to 138kHz range is **very challenging and not recommended**.

Table 5.8 Recommended Switching Power Supply Fundamental Operating Frequencies

Recommended Frequency Ranges
46kHz - 55kHz
90kHz - 110kHz
>155kHz

Off-the-Shelf Switching Supplies

Most commercially available switching power supplies have been designed with some level of input noise filtering. Frequently this level of filtering is adequate if the supply's fundamental switching frequency falls within the recommended ranges of Table 5.8 under all conditions.

Most off-the-shelf switching power supplies have a very low input impedance and require the addition of an input inductor as described on the following page in the section titled *Power supply-Induced Attenuation*.

Full Custom Switching Supplies

Developing a custom switching supply, even one which employs a commercially available controller chip, is very challenging and is only recommended if none of the other options outlined in this chapter are suitable. If this option is chosen, it is recommended that it only be pursued by experienced switching supply and electromagnetic compatibility experts. Even if such personnel are available, extra time must be allowed for design iterations during development. If this approach is chosen, it is absolutely essential that the supply is verified to meet the input and output noise masks provided later in this chapter.

Many of the off-line switching regulators available from Power Integrations Inc. (for example, LinkSwitch®and TinySwitch® regulators) operate at frequencies which are not within the recommended range for use with PL Smart Transceivers and thus they are not recommended for use with PL Smart Transceivers. The TopSwitch® family of off-line switching regulators from Power Integrations operate within the recommended range of frequencies at room temperature but they do not stay within the recommended range over temperature. TopSwitch®regulators are therefore no longer recommended for powering PL Smart Transceiver-based devices.

Most 1st and 2nd generation SIMPLE SWITCHER® regulators from National Semiconductor Corporation operate at frequencies which are not within the recommended range for use with the PL Smart Transceivers (that is, most LM25xx parts). Use of any SIMPLE SWITCHER regulator with a nominal operating frequency of 52kHz, 100kHz or 150kHz is not recommended because these devices have a very wide frequency tolerance which could result in operation outside the recommend range.

Newer SIMPLE SWITCHER regulators, for example LM26xx parts, with operating frequencies of ≥200kHz can be used, however, a supply designed with one of these parts must still be verified to meet the noise mask requirements of this chapter over all operating conditions.

Power Supply Impedance and Noise Requirements

Power Supply-Induced Attenuation

The input stage of a switching power supply typically contains an EMC filter that includes one or more capacitors connected directly from line to neutral and, in many cases, additional capacitors from line and neutral to ground. When the AC line terminals of the switching power supply are connected to the AC mains (in parallel with the coupling circuit), additional signal attenuation occurs. This loss can be avoided by inserting a series inductor between the power supply input and the power line communication channel as shown in Figure 5.10.

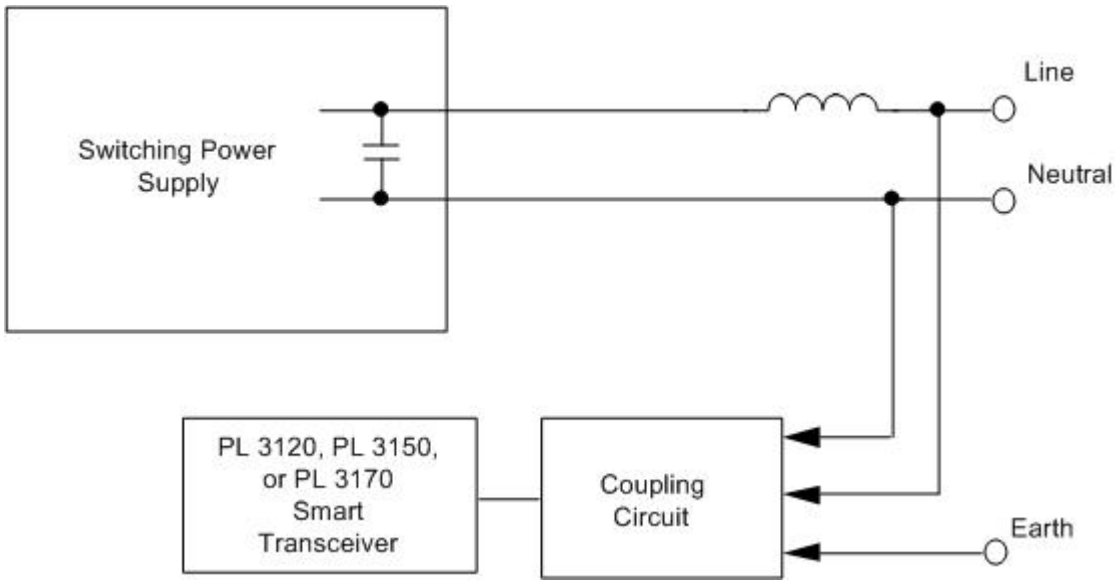


Figure 5.10 Reducing Attenuation Caused by a Switching Power Supply

This inductor is necessary because the increase in attenuation for a given load is much worse when the load, in this case the switching power supply, is connected directly to the transceiver. In contrast, the loading caused by other switching power supplies on the AC mains that are separated from the receiver is reduced by the series inductance of power line wiring.

The value of the inductor should be chosen such that the power supply does not impose a low impedance onto the power line in the communication frequency range. The appropriate value of inductance is a trade-off between required impedance, which is a function of system topology, and node cost. The selected inductor must have a current rating which is greater than the peak current drawn by the power supply in order to avoid impedance reduction due to inductor saturation. Higher impedances require larger inductance values which are more expensive for a given power supply input current.

For most AC mains distribution systems, where the line impedance at the communication frequencies of the PL Smart Transceiver is typically in the range of 1 to 20 ohms, a power supply input impedance of 100 ohms is sufficient to avoid added signal attenuation. To maximize communication distance on mains distribution systems between buildings where the system impedance can be as high as 50 ohms, a minimum power supply input impedance of 250 ohms is recommended.

An example of a system that would benefit from an even greater input impedance would be one in which 100 or more PL Smart Transceiver-based devices were connected to a long twisted pair cable. In this case the input impedance of the power supply could limit either the maximum transmission distance and/or the maximum number of devices that could be connected to the cable. To maximize communication distance on dedicated twisted pair wiring where the system impedance is approximately 100 ohms, a minimum power supply input impedance of 500 ohms is recommended. For extreme cases with >100 nodes on dedicated lines longer than 1000m, a power supply input impedance of 2000 ohms might be needed to maximize communication distance. Table 5.9 shows the appropriate inductor value by application.

Table 5.9 Recommended Inductor Value vs. Application

Application	Network Impedance at Communication Frequencies	Inductor Impedance at Primary Communication Frequencies	C-band Inductor Value	A-band Inductor Value
Single building AC mains	1-20 ohms	≥100 ohms	≥150µH	≥220µH
Inter-building mains distribution	1-50 ohms	≥250 ohms	≥330µH	≥470µH
Dedicated cable ≤100 nodes ≤100m	50-100 ohms	≥500 ohms	≥680µH	≥1mH
Dedicated cable >100 nodes >100m	50-100 ohms	≥2000 ohms	≥2.4mH	≥3.9mH

There is one further constraint on the value of the inductor. When the inductor is combined with the input capacitance of the switching supply, the LC resonant frequency should be at least one octave away from the communication frequency range (110kHz-138kHz for C-band and 70kHz-90kHz for A-band). The unintentional series resonance between the inductor's reactance and the power supply's capacitive reactance can produce a low impedance at communication frequencies if this frequency range is not avoided.

One way to reduce the size and cost of an inductor used to raise a power supply's input impedance is to purposefully parallel resonate it at the communication frequency with a capacitor, as shown in Figure 5.11. If this option is chosen, resistive damping must be included so that impulse noise from the power line does not excite excessive filter ringing, which could degrade the reception of weak signals. The parallel resistor has been selected to optimize receive impedance and impulse noise damping. Note that even though only a 100µH inductor is shown in Figure 5.11, this circuit built with C-band values provides a series impedance of ≥200 ohms from 125kHz to 138kHz due to the parallel resonant effect. When built with A-band values the series impedance is ≥150 ohms from 70kHz to 90kHz. Also, note that the inductor must be rated for the peak AC current drawn by the power supply.

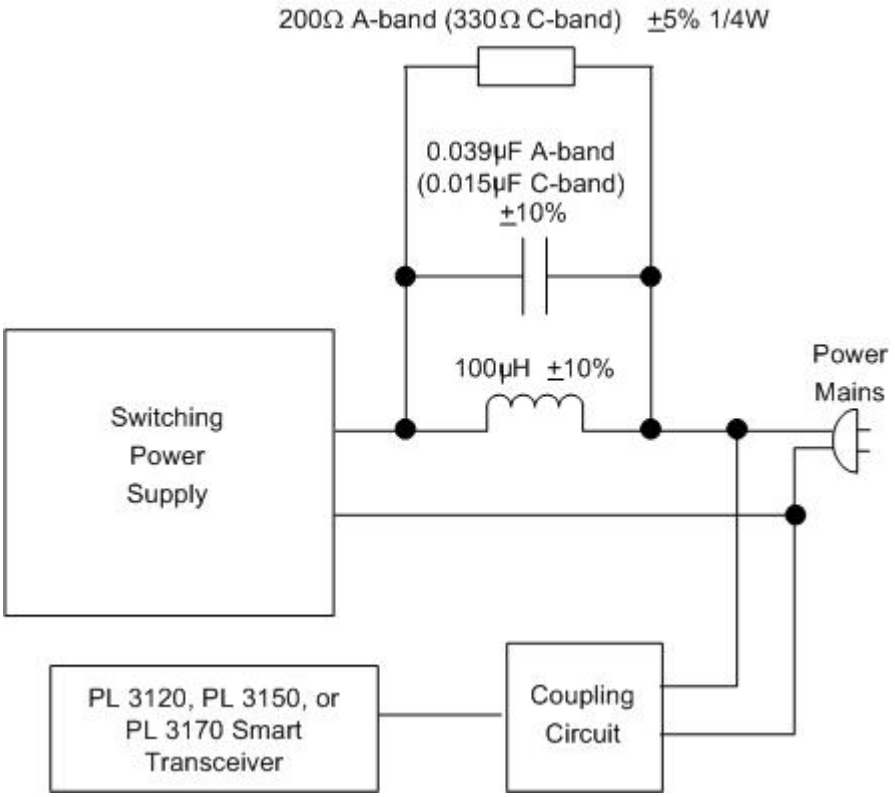


Figure 5.11 Reducing Attenuation Caused by a Switching Power Supply with a Resonant Circuit

Noise at the Power Supply Input

In order to achieve maximum communication performance and to comply with the conducted emissions regulations such as CENELEC EN 50065-1 and FCC Part 15, a switching power supply input must not conduct excessive noise onto the power mains. A switching power supply contains an oscillator that operates at a frequency between 10kHz and several MHz. Depending on the power supply design, significant energy at the switching frequency fundamental and/or its harmonics can appear at the input (mains side) of the power supply. If the amplitude of the signal is large enough in sensitive frequency ranges the performance of the PL Smart Transceiver may be degraded.

While the PL Smart Transceiver is designed to operate reliably with a combination of attenuation and significant switching supply noise, noise from the switching power supply closest to the receiver will have the most deleterious effect on communication performance. Noise from more distant sources will be attenuated before reaching a receiver, minimizing its effect on reception. For this reason it is important that noise at the input of a switching supply of a PL Smart Transceiver-based device be controlled to meet the noise masks provided in the following section.

Switching Power Supply Input Noise Masks

The noise “masks” presented in Figures 5.12 through 5.15 show the maximum noise allowable at the input of a switching power supply such that optimum performance of the PL Smart Transceiver is achieved and the appropriate conducted emissions regulation satisfied. Figure 5.12 defines the noise mask for C-band CENELEC EN 50065-1 [2] conducted emissions compliance. Figure 5.13 defines the noise mask for C-band FCC [1] conducted emissions compliance. Likewise Figure 5.14 defines the noise mask for A-band CENELEC EN 50065-1 conducted emissions compliance and Figure 5.15 defines the noise mask for A-band FCC conducted emissions compliance.

Measurements of a particular power supply should be made by connecting the supply to the artificial mains network as specified in sub clause 8.2.1 of CISPR Publication 16 [3]. Measurements should be made over the full range of anticipated loads on the supply because many switching supplies vary their switching frequency with load. Two different limits are shown for the CENELEC measurements. One limit is measured using a quasi-peak detector, the other using an average detector. Note that these limits are the same as required for any other CENELEC compliant product, except in the communication range of 110kHz to 138kHz for C-band devices (70kHz to 90kHz for A-band devices), where lower noise levels are specified.

For FCC applications, the limits of Figures 5.13 and 5.15 correspond to FCC Class B limits for frequencies above 450kHz. Below 450kHz, the limits are set such that the communication performance of the PL Smart Transceiver is maintained. A quasi-peak detector should be used when verifying power supply noise against the limit lines of Figures 5.13 and 5.15.

For both CENELEC and FCC measurements, the measurement bandwidths are 200Hz for frequencies below 150kHz, and 9kHz for frequencies above 150kHz, as described in CISPR 16.

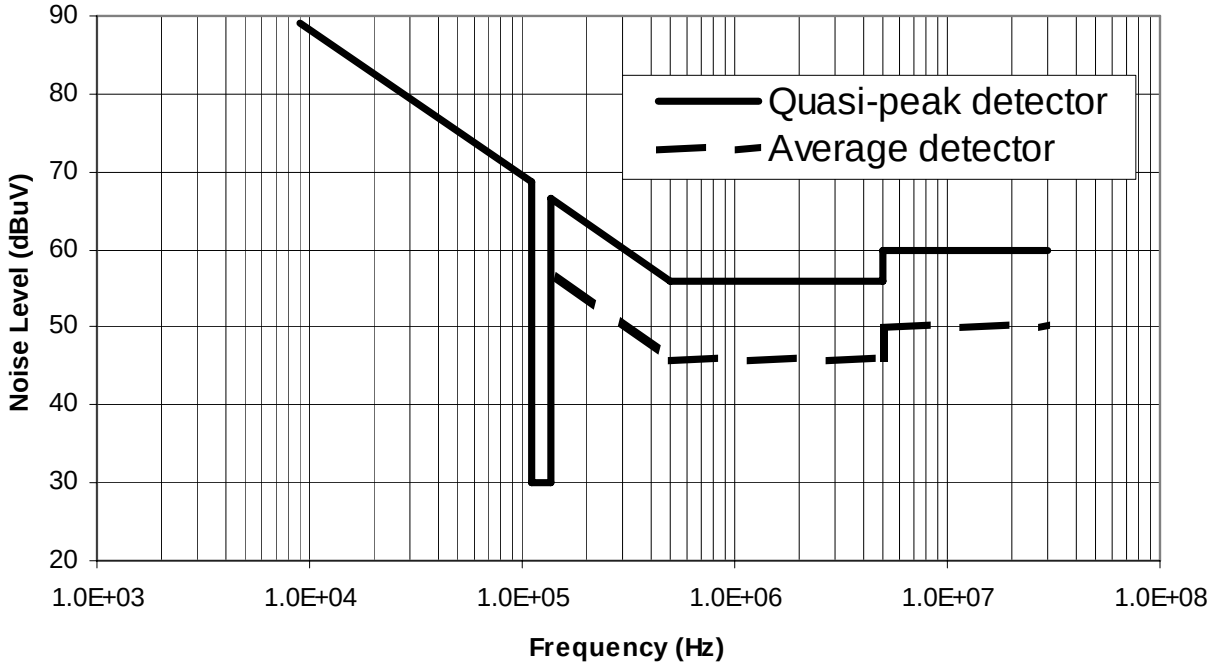


Figure 5.12 Switching Power Supply Input Noise Limits for C-band CENELEC Compliance

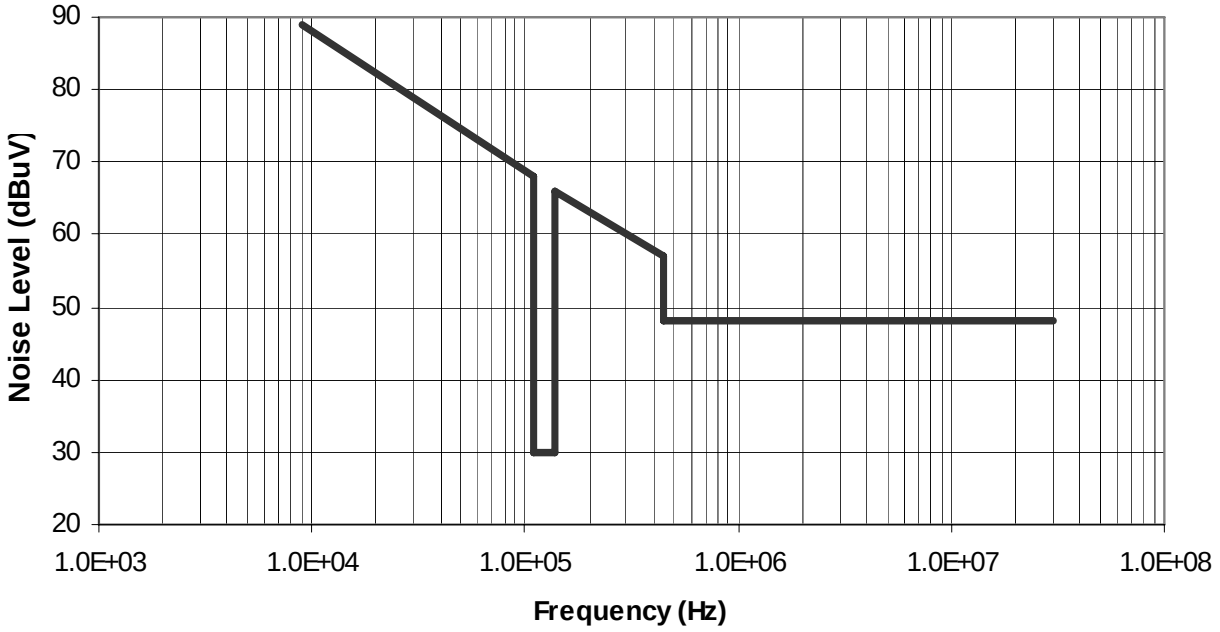


Figure 5.13 Switching Power Supply Input Noise Limits for C-band FCC Compliance

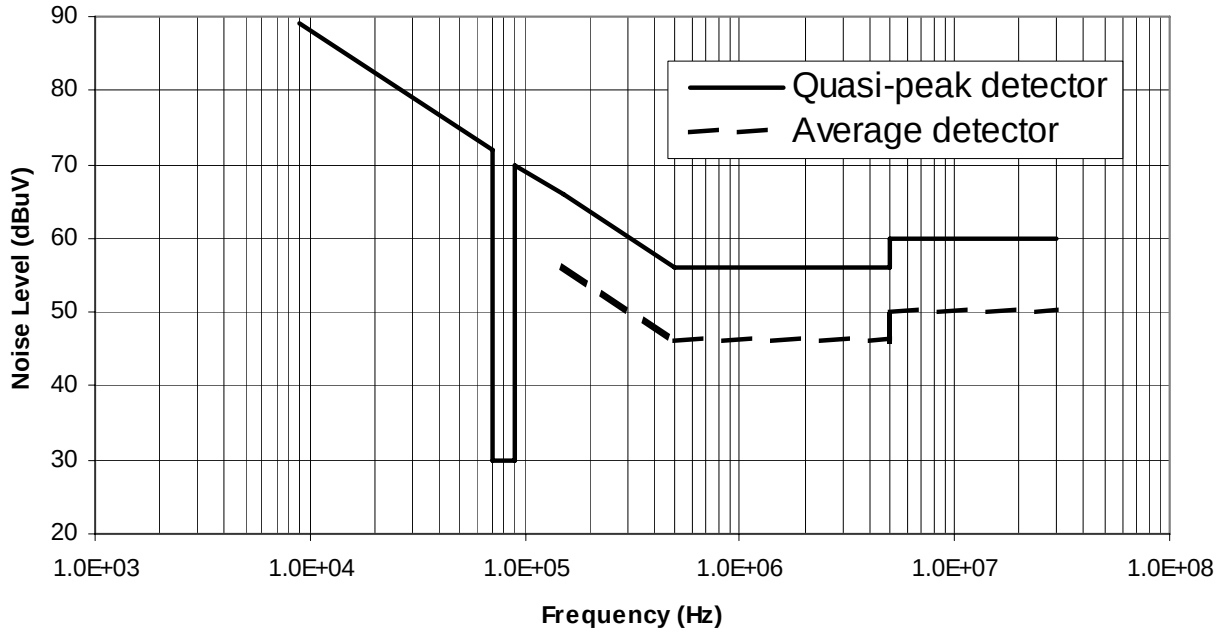


Figure 5.14 Switching Power Supply Input Noise Limits for A-band CENELEC Compliance

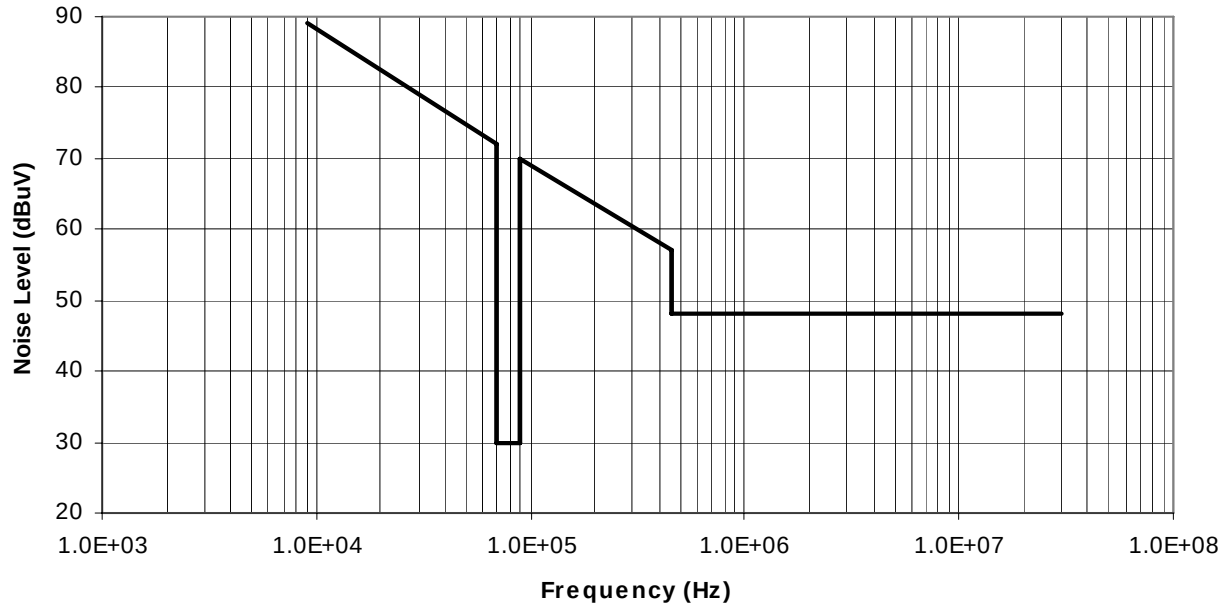


Figure 5.15 Switching Power Supply Input Noise Limits for A-band FCC Compliance

Table 5.10 lists the endpoints of the straight lines shown in Figure 5.12, and Table 5.11 lists those shown in Figure 5.13. Table 5.12 lists the end points of the straight lines shown in Figure 5.14. Table 5.13 lists the levels shown in Figure 5.15.

Table 5.10 Switching Power Supply Input Noise Limits for C-band CENELEC EN 50065-1 Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector	Noise Level (dBμV): Average Detector
9	89	N/A
110	68	N/A
110+	30	N/A
138	30	N/A
138+	66	56
500	56	46
500+	56	46
5000	56	46
5000+	60	50
30000	60	50

Table 5.11 Switching Power Supply Input Noise Limits for C-band FCC Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector
9	89
110	68
110+	30
138	30
138+	66
450	57
450+	48
30000	48

Table 5.12 Switching Power Supply Input Noise Limits for A-band CENELEC Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector	Noise Level (dBμV): Average Detector
9	89	N/A
70	72	N/A
70+	30	N/A
90	30	N/A
90+	70	N/A
150	66	56
500	56	46
5000	56	46
5000+	60	50
30000	60	50

Table 5.13 Switching Power Supply Input Noise Limits for A-band FCC Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector
9	89
70	72
70+	30
90	30
90+	70
450	57
450+	48
30000	48

A PL Smart Transceiver-based device with a power supply that does not meet the appropriate power supply input noise mask will require a filter between supply and the power mains.

An example of a filter which both attenuates switching supply noise and provides >200 ohm input impedance in the C-band is shown in Figure 5.16. Note that both inductors must be rated for the peak AC current drawn by the power supply.

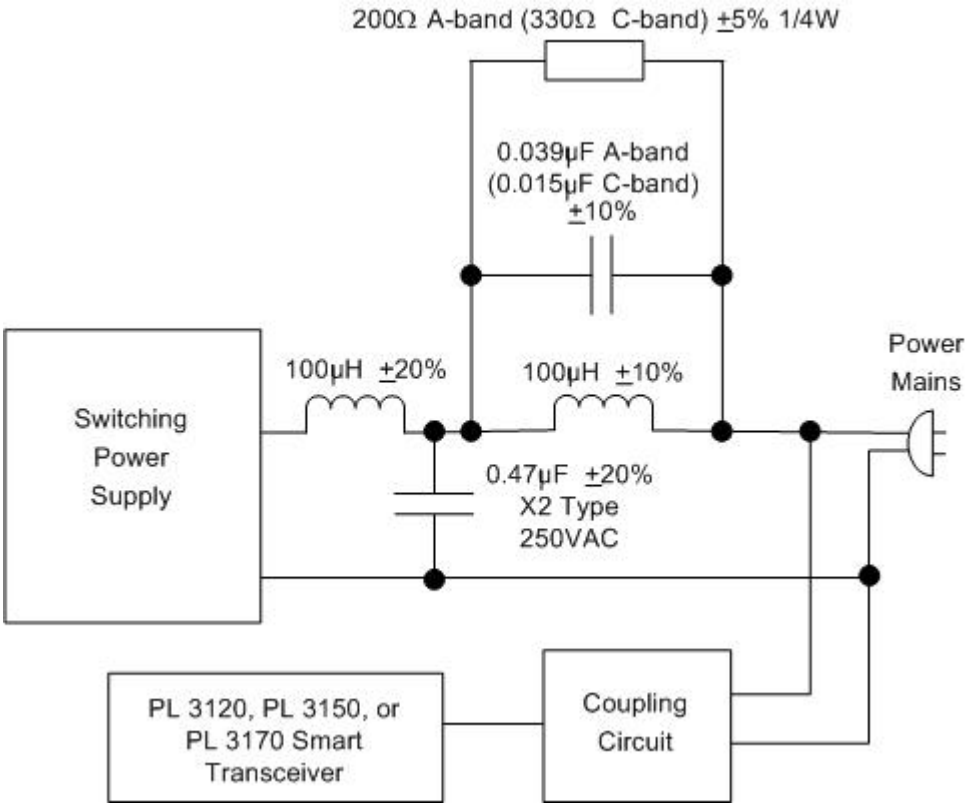


Figure 5.16 Optional Switching Power Supply Filter

The C-band version of this filter has the attenuation characteristics shown in Figure 5.17, when connected to a 50Ω mains network. The characteristics of the A-band version of the filter into a 50Ω network are shown in Figure 5.18.

If the power supply noise drops by less than the values indicated in the graph when the filter is added, it is likely due to parasitic coupling between the two inductors. If this occurs, filtering of the level shown in Figures 5.17 or 5.18 can usually be accomplished by adjusting the relative location and orientation of the inductors (orthogonal orientation typically reduces inductor coupling). Alternately, shielded or toroidal inductors can be used to reduce coupling.

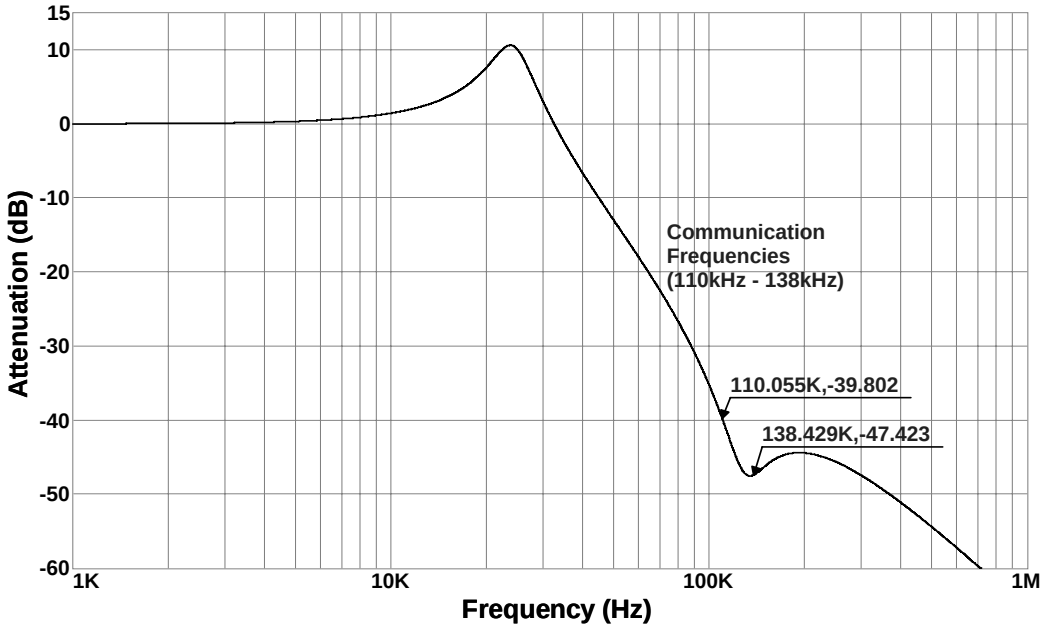


Figure 5.17 C-band Filter Frequency Response

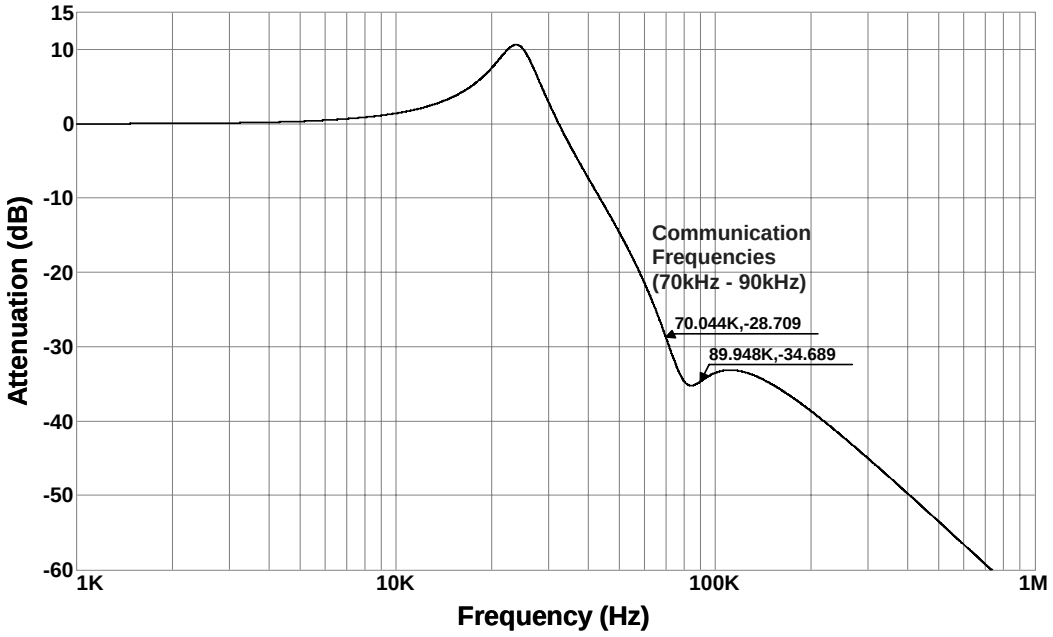


Figure 5.18 A-band Filter Frequency Response

In some instances it is possible that noise radiated from either the power supply or the supply filter can couple into the inductors of the coupling circuit of the PL Smart Transceiver. The coupling circuit can then couple this noise onto the power mains. This problem can be diagnosed by disconnecting the transceiver's coupling circuit and then analyzing the conducted line noise.

If noise from parasitic coupling is suspected, it can be confirmed by inserting a 10cm (4 inch) twisted wire pair in series with one of the inductors in question. If the conducted noise spectrum varies by more than a few dB when this inductor is moved closer to, and farther from, other components, then parasitic coupling might be the source of the problem.

There is a second, although less likely, potential cause for reduced filter effectiveness. It is possible for the inductive reactance of the filter components to be canceled by capacitive reactance from the input of the power supply. This problem is generally seen as narrow band noise which appears to pass through the filter unattenuated. This problem can be remedied by either damping the unintended resonance, or by adjusting the values of the filter inductor and capacitor to move the resonance to a non-interfering frequency. Damping can be accomplished by adding resistance in the range of 200 ohms to 5k ohms in parallel with any undamped power supply filter inductor(s).

Power Supply Output Noise Masks

Products incorporating a PL Smart Transceiver require a 5V (V_{DD5}) supply and a second nominally 12V (V_A) supply. The amplitude of the noise and ripple on these power supply outputs must be controlled in order to comply with CENELEC EN 50065-1 or FCC-conducted emission limits, as well as to maintain maximum communication performance. Noise requirements to accomplish these goals are provided in Figures 5.20 and 5.21. Figure 5.20 shows the noise limits on the V_A and V_{DD5} supplies for C-band while Figure 5.21 illustrates the A-band limits. In each band the same limit lines are used to comply with both CENELEC EN50065-1 and FCC conducted emissions. Satisfying these noise masks ensures that full performance of both operating frequencies is available to overcome unexpected power line noise in either of the two frequency ranges.

Measurements should be made over the full range of anticipated loads on the supply, because many switching supplies vary their switching frequency with load. For all CENELEC EN 50065-1 and FCC power supply measurements a peak detector should be used. The measurement bandwidth for V_A should be 3kHz. For V_{DD5} the two separate measurements must be made each a using different measurement bandwidth and each having a separate noise mask. The measurements made using the 3kHz filter should be performed at all frequencies shown in the graph, while the measurements made using the ≤300Hz filter only need to be performed at frequencies in the communication frequency range of the PL Smart Transceiver (110kHz-138kHz for C-band and 70kHz-90kHz for A-band). The video (post detection) bandwidth for all power supply output noise measurements should be 10Hz.

Note that these output noise masks should generally be checked even if the V_A and V_{DD5} power supplies are not generated by a switching regulator since it is possible for switching loads to introduce noise onto an otherwise quiet linear supply. An example of one type of device that can inject noise back onto a supply is an IC that includes an on-chip switching regulator to generate additional internal supply voltages.

Figure 5.19 shows a probe that can be used to measure the noise on the power supply. The twisted wires must be connected directly to the PL Smart Transceiver power and ground pins, and the coaxial cable must be connected to the 50Ω measuring equipment. Note that the 1/10 gain of the probe must be taken into account.

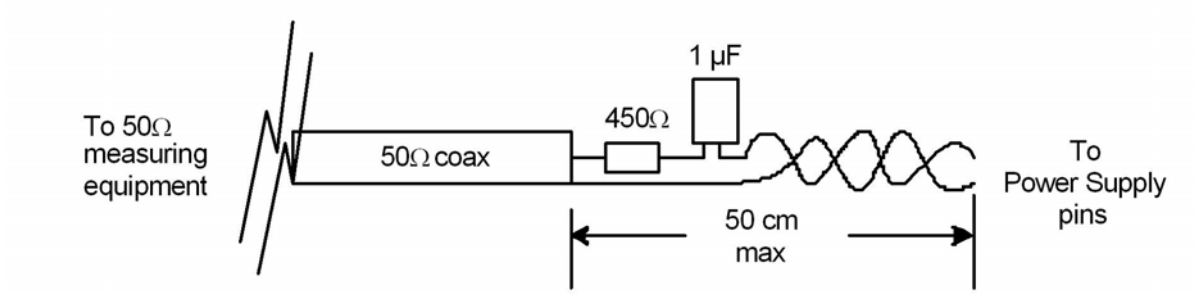


Figure 5.19 10X Power Supply Noise Probe

If the noise masks for either the V_A or V_{DD5} power supplies are not met, then additional filtering must be added to the offending supply in order to bring it into compliance. In the event that extra filtering is needed an inductor of about 10µH can be added in series with the supply line. When combined with a bulk bypass capacitor of >10µF (on the PL Smart Transceiver side of the inductor) the LC combination will provide >20dB of attenuation at communication frequencies. An alternate way to provide a low noise V_{DD5} supply is to use a dedicated 5V linear regulator to feed the PL Smart Transceiver circuitry. In this way noise from other devices on the PCB will be isolated from the V_{DD5} supply line of the PL Smart Transceiver. If a switching power supply is used which meets the recommended operating frequencies of Table 5.8 then additional V_A and V_{DD5} filtering is generally not required.

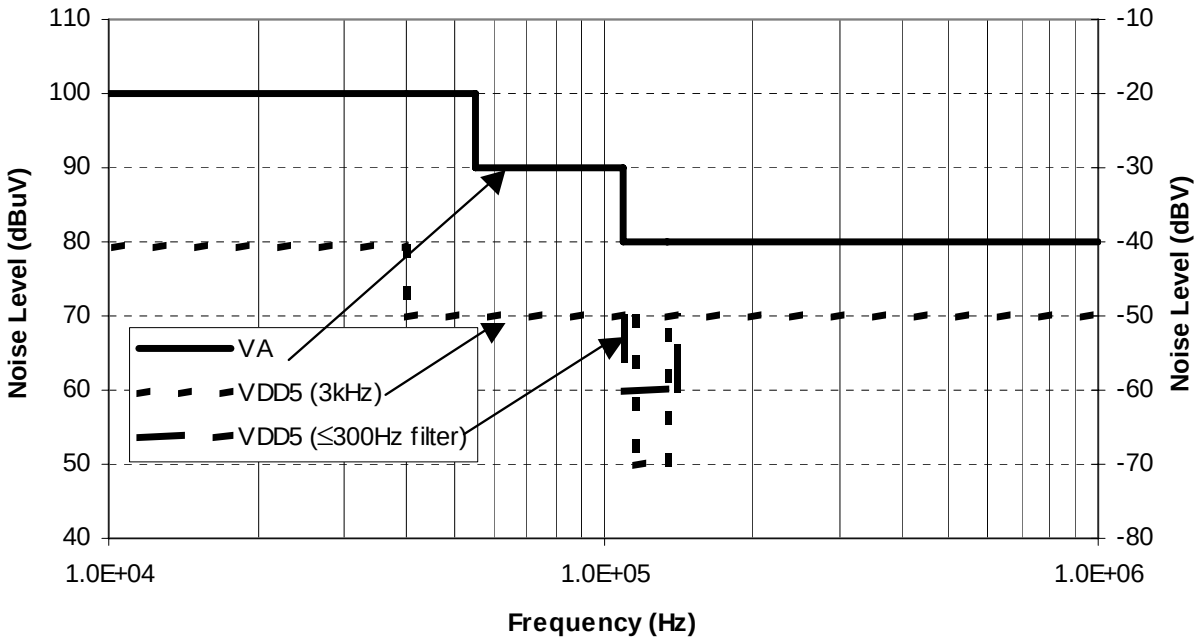


Figure 5.20 V_A and V_{DD5} Power Supply Output Noise Limits for C-band

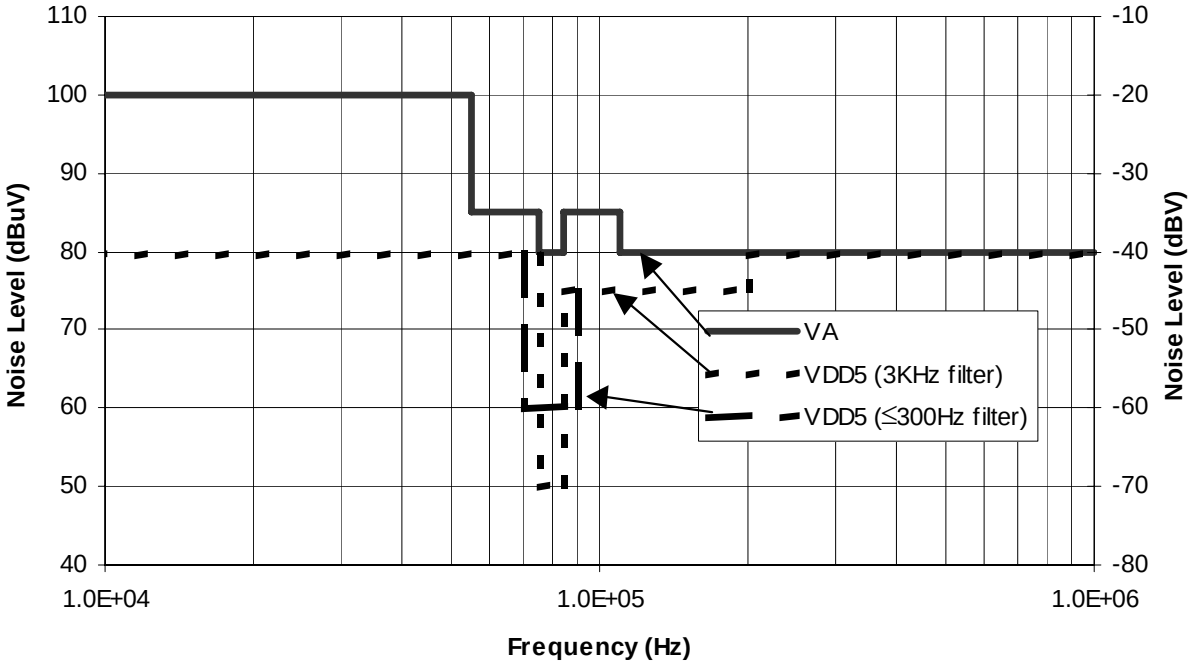


Figure 5.21 V_A and V_{DD5} Power Supply Output Noise Limits for A-band

Tables 5.14 and 5.15 list the levels shown in Figures 5.20 and 5.21 respectively.

Table 5.14 V_A and V_{DD5} Power Supply Output Noise Limits for C-band

Frequency (kHz)	V_A Noise Level w/3kHz filter (dBV)	V_{DD5} Noise Level w/3kHz filter (dBV)	Frequency (kHz)	V_{DD5} Noise Level w/300Hz filter (dBμV)
10-40	-20	-40		
40-55	-20	-50		
55-110	-30	-50		
110-115	-40	-50		
115-135	-40	-70	110-138	-60
135-1000	-40	-50		

Table 5.15 V_A and V_{DD5} Power Supply Output Noise Limits for A-band

Frequency (kHz)	V_A Noise Level w/3kHz filter (dBV)	V_{DD5} Noise Level w/3kHz filter (dBV)	Frequency (kHz)	V_{DD5} Noise Level w/300Hz filter (dBμV)
10-55	-20	-40		
55-75	-35	-40		
75-85	-40	-70	70-90	-60
85-110	-35	-45		
110-200	-40	-45		
200-1000	-40	-40		

Chapter 6

Design and Test for Electromagnetic Compatibility

Introduction

Products that communicate using public ac mains wiring generally need to demonstrate compliance with electromagnetic compatibility (EMC) standards from various regulatory agencies. This chapter provides information regarding the most effective ways to satisfy electromagnetic interference (EMI) and electrostatic discharge (ESD) requirements with Smart Transceiver-based products. For information regarding surge immunity refer to the discussion at the end of Chapter 4.

Electromagnetic Interference (EMI) Compliance

In the USA, the FCC[1] requires that unintentional radiators comply with Part 15 level "B" for consumer and household products and level "A" for industrial products. European countries generally require compliance to CENELEC EN 50065-1[2]. Similar regulations are imposed in most countries throughout the world.

While it is the responsibility of each product developer to demonstrate compliance of their own product, the task is greatly simplified by the availability of multiple Smart Transceiver reference layouts that have all been carefully designed to pass the required regulations. Directly copying one of the eight PL Smart Transceiver layouts referenced in Appendix A allows the product developer to proceed with the confidence that this same circuit layout has been verified to meet the required regulations. Using one of the pre-verified power supply designs from Chapter 5 adds confidence that an instance of this portion of the product has also been verified to satisfy regulatory requirements.

Most EMI sensitive circuitry is encapsulated in the PL Smart Transceiver reference layouts. Directly copying these reference layouts greatly reduces the risk of EMI related issues. There are, however, a couple of sensitive circuit traces that in some instances are either near the edge of a reference layout, or connect between the reference layout and the coupling circuit. These traces need to be kept away from any high speed digital signals in order to preserve the proven electromagnetic compatibility of the design. In no case should any circuit traces not associated with a reference layout be run through the reference layout area. Digital or clock signals that operate at rates any higher than about 1kHz should be placed >2mm from the edge of the reference layout if there is an intervening ground to act as a guard (or >10mm if there is no intervening guard ground). The following is a list of reference circuit nets that should be isolated from potential interference generating lines as described above:

TXOUT
RXIN
RXCOMP
TX2
TX3
XIN
XOUT

In addition to the specific recommendations above, good design practice dictates the use of a low inductance return path for all signals (e.g., a ground plane) and the use of one or more power supply decoupling capacitors located next to each integrated circuit.

If there are other aspects of product design for EMI compliance not associated with the PL Smart Transceiver that require attention, the developer is encouraged to refer to the book, *Noise Reduction Techniques in Electronic Systems* [11].

Conducted Emissions Testing

Each PL Smart Transceiver reference design has been demonstrated to comply with both FCC Section 15.107 “Limits for carrier current systems” [1] and CENELEC EN 50065-1 “Signaling on low-voltage electrical installations in the frequency range 3kHz to 148.5kHz” Part 1 “General requirements, frequency bands and electromagnetic disturbances” [2].

Measuring the conducted emissions of a power line transceiver places extreme demands on the dynamic range of the test equipment and even many of the most expensive EMI receivers on the market do not have sufficient dynamic range to make the measurement without producing measurement artifacts that can lead to false conclusions. The traditional technique of adding input attenuation to prevent instrument overload, is often insufficient since the required level of attenuation often results in a measurement noise floor that is above or very close to the regulation limits. Note that this problem is compounded by the fact that the overload indicator on many of these instruments fails to properly indicate an overload condition when faced with burst like PL transmissions.

Both Rohde & Schwarz and Agilent (formerly Hewlett Packard) have acknowledged this problem and they each recommend the use of a 150kHz high-pass filter at the instrument input to solve the problem. Rohde & Schwarz makes a filter suitable for use with any measuring receiver “for conducted emission measurements in the presence of high long-wave mains disturbance signals.” Use of this Rohde & Schwarz R&S EZ-25 150kHz high-pass filter (or equivalent) is thus recommended.

Proper measurement of conducted emissions to verify compliance with FCC[1] and CENELEC EN 50065-1[2] requires strict adherence to all of the following guidelines.

- Connect the product under test to the correct 50Ω//(50μH+5Ω) Line Impedance Stabilization Network (LISN) as specified in CISPR Publication 16 [3]. Using a LISN that does not include the specified 5 ohm series resistor may yield erroneous results.
- Connect a Rohde and Schwarz R&S EZ-25 150kHz high-pass filter (or equivalent) between the LISN and the measuring receiver. Account for the filter’s 10dB pass-band loss when determining the measured result.
- Set the input attenuator of the measuring receiver to avoid instrument overload. This is accomplished by measuring the emissions, then adding attenuation in the measurement path and re-measuring emissions. For instruments that have a built-in input attenuator (and built-in compensation for that attenuator) the reported levels should not change when the attenuation is changed. If there is an overload problem the indicated level will change.
- Verify that the residual noise floor of the entire measurement setup remains at least 10dB below the regulation limit once the appropriate attenuator is installed. Thus the corrected noise floor with all attenuators in place should be < 38dBμV for FCC measurements, and < 36dBμV for CENELEC EN 50065-1 measurements.
- Use proper quasi-peak and average detector settings as specified in CISPR Publication 16. Although a measurement scan with a peak detector is common, because it can be performed quickly, the limits specified by FCC Section 15.107 and by CENELEC EN 50065-1 are for quasi-peak and average detectors only (for power line transceivers, peak measurements are frequently higher than the required quasi-peak limits).
- Perform the measurements with the proper specified measurement bandwidths of 200Hz for frequencies below 150kHz and 9kHz for frequencies above 150kHz.

While most EMI receivers and spectrum analyzers do not have sufficient dynamic range to measure the emissions of a power line transceiver without the addition of a highpass filter, two samples of the older Rohde & Schwarz ESHS30 EMI Receiver have been found to have sufficient internal dynamic range and filtering to make the measurement without adding an external filter. Note however that the algorithms for “automatic” input attenuation on this instrument are confused by burst like power line transmissions. The proper attenuation must be selected using manual mode. A set-up program to accurately run scans for CENELEC EN 50065-1 compliance using the Rohde & Schwarz ESHS30 is available from Echelon's Downloads page at www.echelon.com/downloads in the **Transceivers** category.

EMI Remedies

If a device does not pass conducted emission regulatory limits it is helpful to know whether the failing frequencies are from a switching power supply (fundamental or harmonics), communication harmonics, or other frequencies from other digital circuitry. If a failing frequency is related to the power supply, refer to the sections of Chapter 5 that cover power supply noise and mitigation techniques.

If the device under test fails at a harmonic of the communication frequency (i.e., an integer multiple of 131.6kHz for C-band or 86.2kHz for A-band) then the most common reason for failure is overload of the measuring instrument as described in the previous section. The second most common cause of a failure at a communication harmonic is the use of a switch mode power supply with an impedance raising inductor (described in Chapter 5) that saturates and thus does not provide the proper impedance. Another source of failure at communication harmonics is the use of coupling circuit components that do not meet the specifications listed as “Required Specifications” for each example coupling circuit of Chapter 4.

If the unit under test is found to exceed the applicable conducted noise limit at frequencies other than those related to power line communication or a switching power supply, it is likely the result of unintentional coupling of noise from various other digital circuits. If this occurs, improvements in grounding and printed circuit layout are often required. It is also possible for the coupling circuit components to pick up stray fields from nearby circuitry and then conduct it onto the power mains. Refer to Chapter 4 for a discussion of how to avoid stray field pickup in coupling circuits.

In some instances conducted emissions above 500kHz can be adequately reduced by the addition of a **small** value capacitor (e.g., 470pF) either across the AC mains or from the line conductor to ground. While devices using the PL Smart Transceiver have been demonstrated to pass CENELEC and FCC limits without an additional capacitor, variations in node design and layout might require the addition of this small value capacitor. If a capacitor is added across the line it should be an X2 safety-rated type for maximum surge reliability. If capacitors are added from either line or neutral to earth, they should be Y safety rated. Alternately, this capacitor can be added across coupling circuit inductor L101 (see Figure 4.2) or across the line-side winding of transformer T101 (see Figure 4.1). If this option is chosen, either a metallized film capacitor of ≥250VDC, a ceramic 1000VDC capacitor, or a Y-type capacitor should be used for surge reliability. Note that this extra capacitance should only be added to the line side of the coupling transformer and not to the transceiver side of the transformer.

Adding capacitance in the above locations reduces the input impedance of the device and could therefore cause an increase in communication signal attenuation. The maximum value of capacitance which can be added without significantly affecting attenuation depends on the application. Table 6.1 shows the maximum value of added capacitance by application.

Table 6.1 EMC Suppression Capacitor Value vs. Application

Application	Network Impedance at Communication Frequencies	Capacitor Impedance at Primary Communication Frequencies	A-band Capacitor Value	C-band Capacitor Value
Single building AC mains	1-20 ohms	≥250 ohms	≤4700pF	≤4700pF
Inter-building mains distribution	1 - 50 ohms	≥500 ohms	≤3600pF	≤2200pF
Dedicated cable ≥100 devices ≥100m	50 - 100 ohms	≥1000 ohms	≤1800pF	≤1200pF
Dedicated cable >100 devices >100m	50 - 100 ohms	≥2500 ohms	≤680pF	≤470pF

Under no circumstances should a capacitor >4700pF be used directly between line and neutral because it will result in excessive signal attenuation.

Another common method of EMC suppression, the addition of ferrite beads, is unacceptable if high impedance beads are placed anywhere in the transmit signal path. Most ferrite beads have an impedance of several ohms at 100kHz. The impedance of any element placed in series with the transmit signal or return path must be less than 0.5 ohms at communication frequencies, as described in chapter 4.

There is, however, one means whereby a higher impedance ferrite bead can be used to reduce common mode high frequency emissions without affecting the transmit signal. If both the communication signal and its return conductor (i.e., Line and Neutral for L-to-N coupling or Line and Earth for L-to-E coupling) pass through the same bead in a common-mode fashion, the bead will not add any series impedance to the transmitter. This is true because the signal currents in the two conductors produce opposite polarity (canceling) flux in the ferrite bead's core. Common mode noise of equal polarity on both conductors will produce additive flux in the ferrite bead's core and will thus be attenuated. Figure 6.1 illustrates both acceptable and unacceptable topologies for high-impedance ferrite beads.

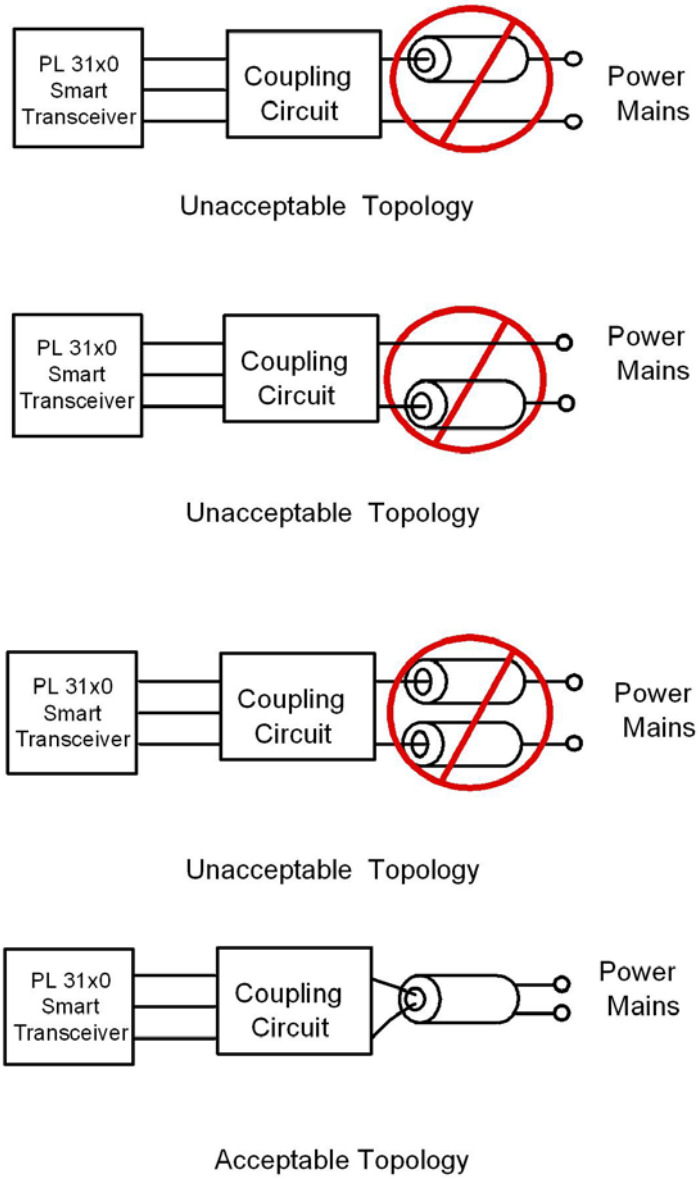


Figure 6.1 Topologies for High Impedance Ferrite Beads

Design for Electrostatic Discharge (ESD) Compliance

Reliable system design must consider the effects of ESD and steps must be taken to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. Keyboards, connectors, and enclosures themselves can provide paths for static discharges to reach ESD sensitive components such as the PL Smart Transceiver.

ESD requirements for products sold throughout Europe are provided in *IEC 61000-4-2 Electromagnetic Compatibility (EMC), Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test* [4]. Conforming to this standard in other parts of the world is good practice and highly recommended.

There are two general methods that are used to protect products from ESD. The first is to seal the product in order to prevent static discharges from reaching sensitive circuits inside the package. The second method is to provide a path for ESD currents to be shunted around sensitive circuitry on the way back to ground. If the first method is selected care must be taken to ensure that the creapage path from all points of entry to any internal conductive elements is >1cm. Note that many LEDs and switches will not satisfy this requirement – unless they are positioned away from the enclosure boundary and their reach is increased by means of an insulated extender (e.g., a light pipe for an LED).

If the developer chooses the second method of ESD protection (providing a safe path back to ground) particular attention must be given to device ground paths. ESD currents should not be allowed to pass near to the PL Smart Transceiver or other sensitive circuits. Note that if the device is floating with respect to earth ground then the ESD current will return by capacitive coupling to earth via the power supply wires and/or the PCB ground plane.

User accessible circuitry requires explicit diode clamping to shunt ESD currents from that circuitry to earth ground using a path that will not disturb sensitive circuitry. For example, if a PL Smart Transceiver scans a keypad using I/O lines, then the I/O lines to that keypad will need to be diode-clamped as shown in Figure 6.2. If a negative ESD hit discharges into the keypad, the grounded diodes shunt the ESD current to the ground plane. If a positive ESD hit discharges into the keypad, the V_{DD5} diodes shunt the current to the ground plane via a 0.1µF decoupling capacitor that is placed directly adjacent to the clamp diodes. The keypad connector, diodes, and decoupling capacitor should all be located so that ESD current does not pass through sensitive circuitry as it exits the PCB.

In addition to the above considerations, the product's package should be designed to minimize the possibility of ESD hits arcing into the device's circuit board. If the product's package is plastic, then the PCB should be supported in the package so that unprotected circuitry on the PCB is not adjacent to any seams in the package. The PCB should not touch the plastic of an enclosure near a seam, because a static discharge can "creep" along the surface of the plastic through the seam and arc onto the PCB.

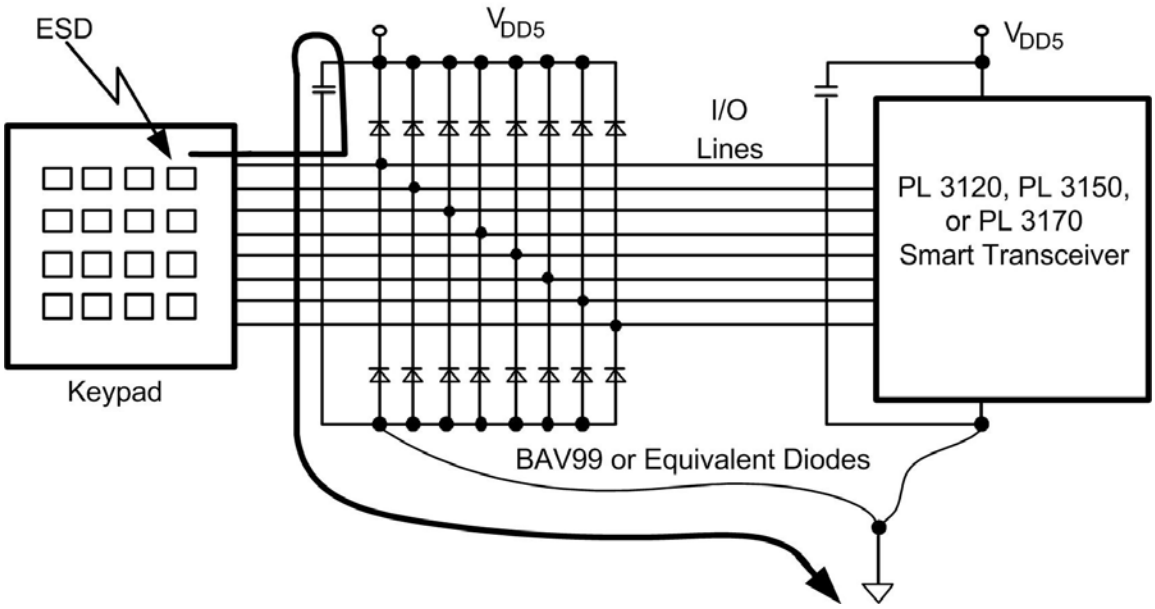


Figure 6.2 Illustration of I/O Line ESD Clamping

Chapter 7

Communication Performance Verification

Introduction

This chapter describes a simple “black box” testing methodology for determining whether or not the basic communication performance of a PL Smart Transceiver-based product has been significantly compromised. This procedure works equally well for products employing L-N or L-E coupling.

The verification procedure described in this chapter is designed to identify gross errors in the implementation of the support circuitry surrounding the PL Smart Transceiver. Before starting this verification, compliance with all items of the checklist in Appendix B must first be confirmed. The Appendix B checklist and the performance test described in this chapter are designed to be complementary. Achieving a passing result for both is essential in order to ensure a properly functioning device (a performance test that could verify all important parameters independent of the Appendix B check list would be many times more complicated than the simple tests described in this chapter). Thus any items of non-conformance with Appendix B must be corrected even if a device passes this Chapter 7 test.

Reasons for Verifying Communication Performance

While each PL Smart Transceiver is thoroughly tested prior to shipment, circuitry external to the transceiver could compromise the communication performance of the device in which the transceiver is used. Ways in which communication performance could be compromised include mis-loaded components, inadequately filtered switching power supplies, circuitry improperly added between the coupling circuit of the transceiver and the power mains, and deviations from recommended part specifications. Due to the robust communication capability of the PL Smart Transceivers, it might not be obvious that communication performance has been compromised when testing in a nominal environment.

Because compromised performance is generally observable only under “corner-case” conditions, failure to verify performance prior to deployment could result in many marginal units in the field before a problem is detected. It is therefore essential that the communication performance of every PL Smart Transceiver design be verified prior to field deployment. This can be accomplished either by self verification, using the procedures given in this chapter, or by contacting your Echelon sales representative to make arrangements to send the device to Echelon for confidential evaluation.

Verification Procedure

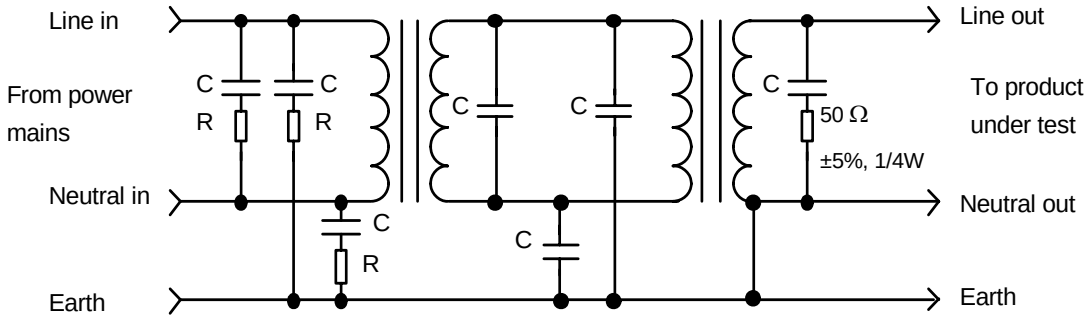
A summary of the recommended verification procedure is as follows:

1. Create a controlled power line environment that is isolated from typical power mains noise and loading.
2. Provide known load impedances at the communication frequencies of the PL Smart Transceiver.
3. Use the PLCA-22 Power Line Communications Analyzer (model 58022) as a calibrated reference transmitter and receiver.
4. Test the performance independent of the product's application by making use of the service pin of the Smart Transceiver and internal statistics features. If the product under test does not have a service pin switch then it will need to be added to the product for testing purposes.
5. Test for unintentional noise injection and excessive loading by the product under test. This is to ensure that the device can behave as a “good citizen” on a power line network.
6. Verify that the product's transmit signal level is within acceptable limits. This is done by deliberately loading the isolated power mains on which the product under test is operating and comparing the output transmission level under load against a reference level.
7. Verify that the receive sensitivity of the product is within acceptable limits. This is performed using a pair of PLCA-22 analyzers. The communication signal level of the transmitting PLCA-22 analyzer is gradually decreased and the receive performance of the product under test is monitored and compared against reference performance levels.
8. All test results can be documented using Table 7.1 at the end of this chapter.

Power Line Test Isolator

The circuit shown in Figure 7.1 is used to create a power mains environment that is isolated from the noise and loading present on typical power mains. When properly constructed, the circuit provides 60 to 80dB of isolation between the power mains and the product under test at the communication frequencies of the PL Smart Transceiver. The effectiveness of the circuit should be verified by using a pair of PLCA-22 analyzers communicating between the power mains input and the output. To perform this verification, set the PLCA-22 analyzer that is connected to the input side of the isolator to send packets at 3.5Vpp in **UnackPri** mode in the **C-band**. The green bar graph meter on the receiving analyzer (connected to the "product under test" output) should indicate a signal strength no higher than –60dB (0dB on the PLCA-22 bar graph meter =3.5Vpp). Without any packet transmission, no LEDs above the –78dB primary and secondary signal strength LEDs should be illuminated or flashing. Note that Neon power indicators should not be used on the isolated output, because they frequently produce noise in the –72dB range.

Because the isolator does not completely block communications from other PL 3120, PL 3150, or PL 3170 Smart Transceivers (or older PLT-2X transceivers) communicating on the power mains, receive testing must only be performed when there is no other packet activity on the power mains.



All capacitors 0.47µF 250VAC (X2 type)
All resistors 20Ω 1 Watt ±5%, unless otherwise indicated
Isolation transformer rating based on load requirements

Figure 7.1 Power Mains Isolation Circuit

The transformers shown in the circuit are 50/60 Hz, 1:1 isolation transformers. The load (VA) rating of each transformer should be chosen based on the load requirements of the devices under test. Care should be taken when wiring the isolator to avoid inadvertent signal coupling between the input and output wiring by spacing the input and output wires at least 15cm (6 inches) apart.

Test Equipment

In addition to the power mains isolator described in the previous section, the following "off-the-shelf" equipment will be needed for testing:

- One pair of PLCA-22 Power Line Communications Analyzers (Model 58022). The older PLCA-21 is not suitable.
- Two PL-20 Line-to-Neutral power line couplers, Echelon model 78200-221.
- Two 50Ω coax cables approximately 30cm long with male BNC connectors on both ends (AMP 1-221128-x or equivalent).

- A four (or more) outlet power strip which does not include surge protection, neon lights, or noise filtering circuitry.
- One personal computer configured with a PL-20 network interface (such as PCLTA-20/SMX network interface with PLM-22 SMX transceiver, or U20 USB network interface).

Test Equipment to be Constructed

The following additional equipment will need to be constructed for testing:

"5Ω Load" Circuit

This circuit, as shown in Figure 7.2, should be built in a suitable enclosure and provided with an appropriate male AC mains plug. Note that the maximum working voltage of the 1MΩ resistor should be greater than or equal to the peak line voltage.

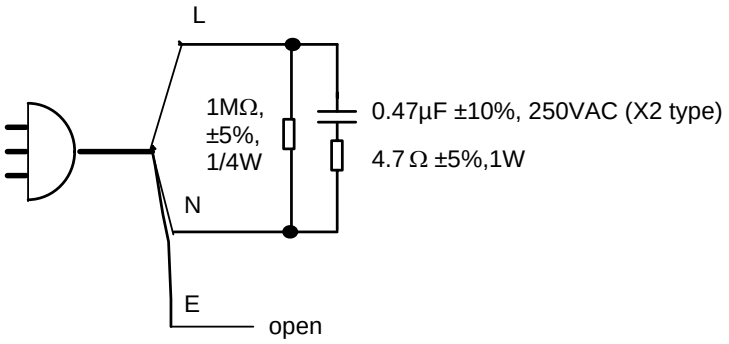


Figure 7.2 "5Ω Load" Circuit

"7Ω Load" Circuit

This circuit, as shown in Figure 7.3, should be built in a suitable enclosure and provided with an appropriate male AC mains plug. Note that the maximum working voltage of the 1MΩ resistor should be greater than or equal to the peak line voltage.

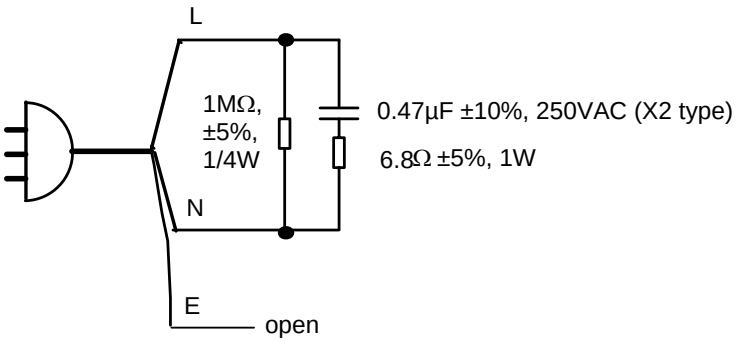


Figure 7.3 "7Ω Load" Circuit

Impedance Circuit

This circuit, as shown in Figure 7.4, should be built in a suitable enclosure with bulkhead BNC jacks (AMP 227755-x or equivalent). This impedance circuit, placed in series with the output path of a PLCA-22 analyzer, effectively increases its output impedance. This will allow for a more sensitive measurement of the receive mode impedance of the product under test.

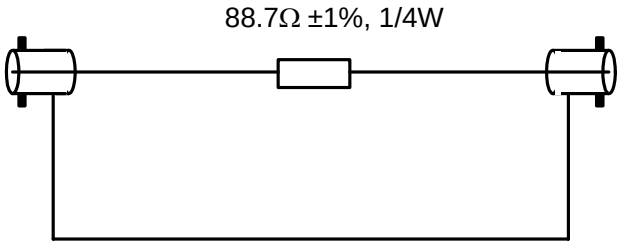


Figure 7.4 Impedance Circuit Used For Excessive Loading Verification

Attenuation Circuit

This circuit, as shown in Figure 7.5, should be built in a suitable enclosure with bulkhead BNC jacks (AMP 227755-x or equivalent). This attenuation circuit, or "pad", will provide approximately 60dB of attenuation when connected into the receive performance verification set-up of Figure 7.9.

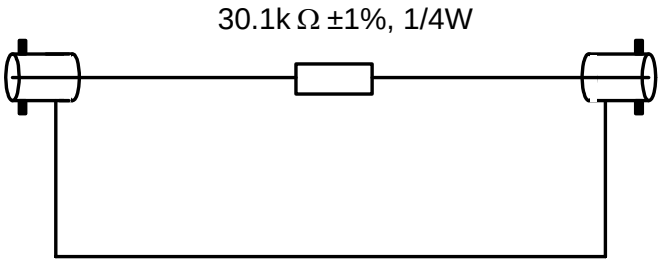


Figure 7.5 Attenuation Circuit Used For Receive Performance Verification

For the receive performance verification, a computer running **NodeUtil Node Utility** (`nodetuil.exe`) is required. This utility is available on the Echelon Web site at www.echelon.com/downloads under **Development Tools**. The **`Node Status`** command is used to obtain a record of the number of uncorrupted packets received by the Unit Under Test (UUT). This set-up is described in detail in the *Packet Error Measurement with NodeUtil* section later in this chapter.

Good Citizen Verification

The following steps are used to verify that the Unit Under Test (UUT) does not inject unwanted noise onto the power mains or excessively load the power mains.

Unintentional Output Noise Verification

The following procedure determines if the UUT is generating unwanted noise which might hinder its communication performance or that of other devices on the power mains.

1. Connect a single PLCA-22 analyzer, the UUT, and the Isolator as shown in Figure 7.6 below. Verify that the analyzer is set for the same band of operation as the UUT (A-band or C-band) by observing the selected band in the upper right-hand corner of the LCD display (if its band setting does not match, then it must be changed using the Setup screen of the analyzer). Leave the PLCA-22 analyzer in idle mode (no packets being transmitted) and set it for Internal and Line-to-Neutral coupling (coupling mode switch to the right).
2. Verify that the UUT application program is not sending messages.
3. Observe the signal strength bar graph LEDs. The -72dB LED should not be on solid and the -66dB LED should not be flashing on either the primary or secondary bar graph meters. In addition, the Packet Detect (PKD) LEDs should not flash any more than once per minute.
4. Record the results from Step 3 in Table 7.1 at the end of this chapter.

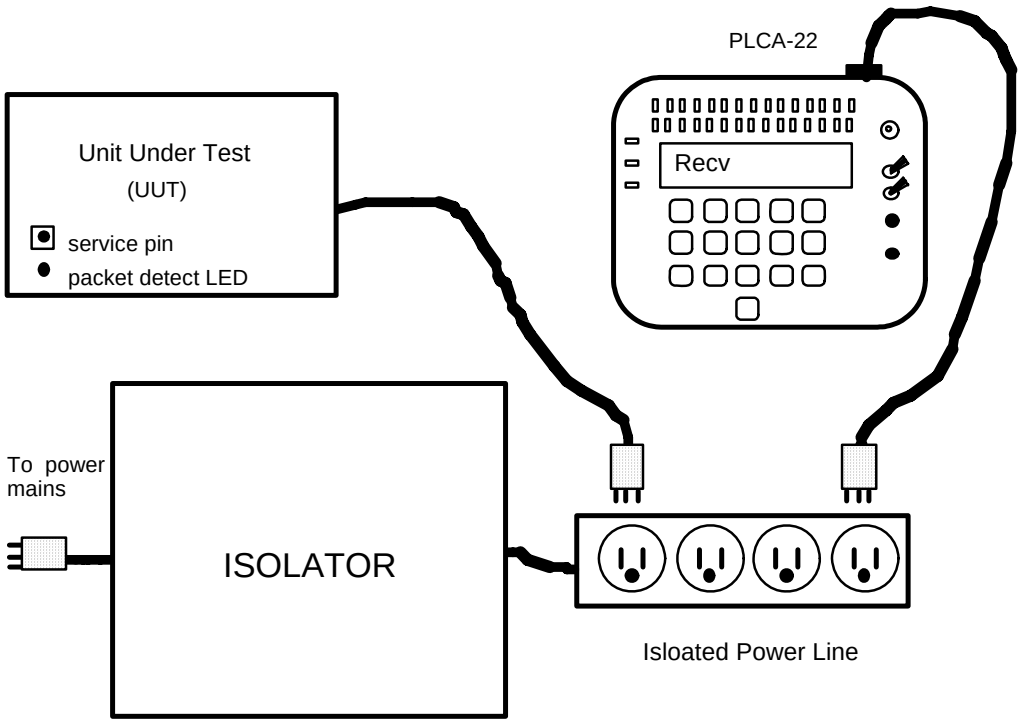


Figure 7.6 Unintentional Output Noise Verification

If either of the -72dB LEDs is on solid or if either of the -66dB LEDs flash or if the PKD LED flashes more than once per minute, then excessive noise or interference is present. This could be caused by one or more of the following sources:

- The UUT is generating unwanted noise internally. This is most often associated with on-board switching power supplies. If the UUT includes a switching power supply, verify that the power supply noise masks of Chapter 5 have been met.
- Power line communications signals present on the power input side of the isolator are not sufficiently attenuated. Ensure that no other power line signaling equipment is operating on the power mains when performing this test.
- The isolator is not completely isolating the test set-up from noise on the power mains. Verify the effectiveness of the isolator as described earlier.

The source of this noise or interference must be identified and eliminated before proceeding with verification testing.

Excessive Loading Verification

The procedure described in this section is used to determine if the receive mode impedance of the UUT is greater than approximately 100Ω at its primary communication frequency (as it should be). A receive mode impedance of less than 100Ω could cause excessive signal attenuation resulting in impaired reception by both the UUT and its neighboring nodes. For applications which require an even higher receive impedance, refer to discussions in Chapters 5 and 6.

The 10Vp-p output capability of the PLCA-22 analyzer is used to increase the sensitivity of the test. The higher output signal allows the 0dB, -3dB, and -6dB LEDs of the PLCA-22 analyzer signal strength meter to be used for observing signal strength. These LEDs, unlike the other LEDs in the signal strength meter, are only 3dB apart allowing for better measurement resolution.

A series impedance circuit (Figure 7.4) in the output path of the transmitting PLCA-22 analyzer is used to increase its effective output impedance, thereby preventing its normally low transmit output impedance from overshadowing the receive mode impedance of the product under test.

The recommended verification procedure is as follows:

1. Set a first PLCA-22 analyzer (referred to as the Recv PLCA-22 analyzer) to use the same band of operation as the UUT. Set it for `Recv` and `UnackPri` modes of operation and configure it for Internal and Line-to-Neutral coupling as shown in Figure 7.7.
2. Set a second PLCA-22 analyzer (referred to as the Send PLCA-22 analyzer) for the same band of operation as the UUT. Set it for `Send` and `UnackPri` modes of operation and configure it for External coupling. Connect the impedance circuit (88.7Ω resistor of Figure 7.4) and the coupling circuit as shown in Figure 7.7. This test is best conducted with the CENELEC protocol (an option for C-band operation) turned off in order to provide uninterrupted LED illumination (select this option on the send unit's setup screen if testing in C-band).
3. Verify that `Attn` on the Send PLCA-22 analyzer is set to 0. Set the number of packets to be transmitted to 9999k on that unit and set the packet length to 13 bytes. Set `TxVpp`: `10`.
4. Without the UUT connected, press START on the Send PLCA-22 analyzer. A test should begin and the receive packet count on the Recv PLCA-22 analyzer should increment with a packet error rate very close to 0%. The signal strength meter on the Recv PLCA-22 analyzer should have the LEDs up to and including the -3dB primary signal strength LED illuminated. The 0dB primary LED may or may not be flashing.
5. Next, connect the UUT as shown in Figure 7.7. The -3dB primary signal strength LED on the Recv PLCA-22 analyzer either should be flashing or illuminated continuously. If the -3dB primary LED is extinguished, then the input impedance of the UUT is excessively low (<100Ω). The impedance of the UUT must be corrected before proceeding; refer to the node checklist of Appendix B for assistance.
6. Record the results of Step 5 in Table 7.1 at the end of this chapter.

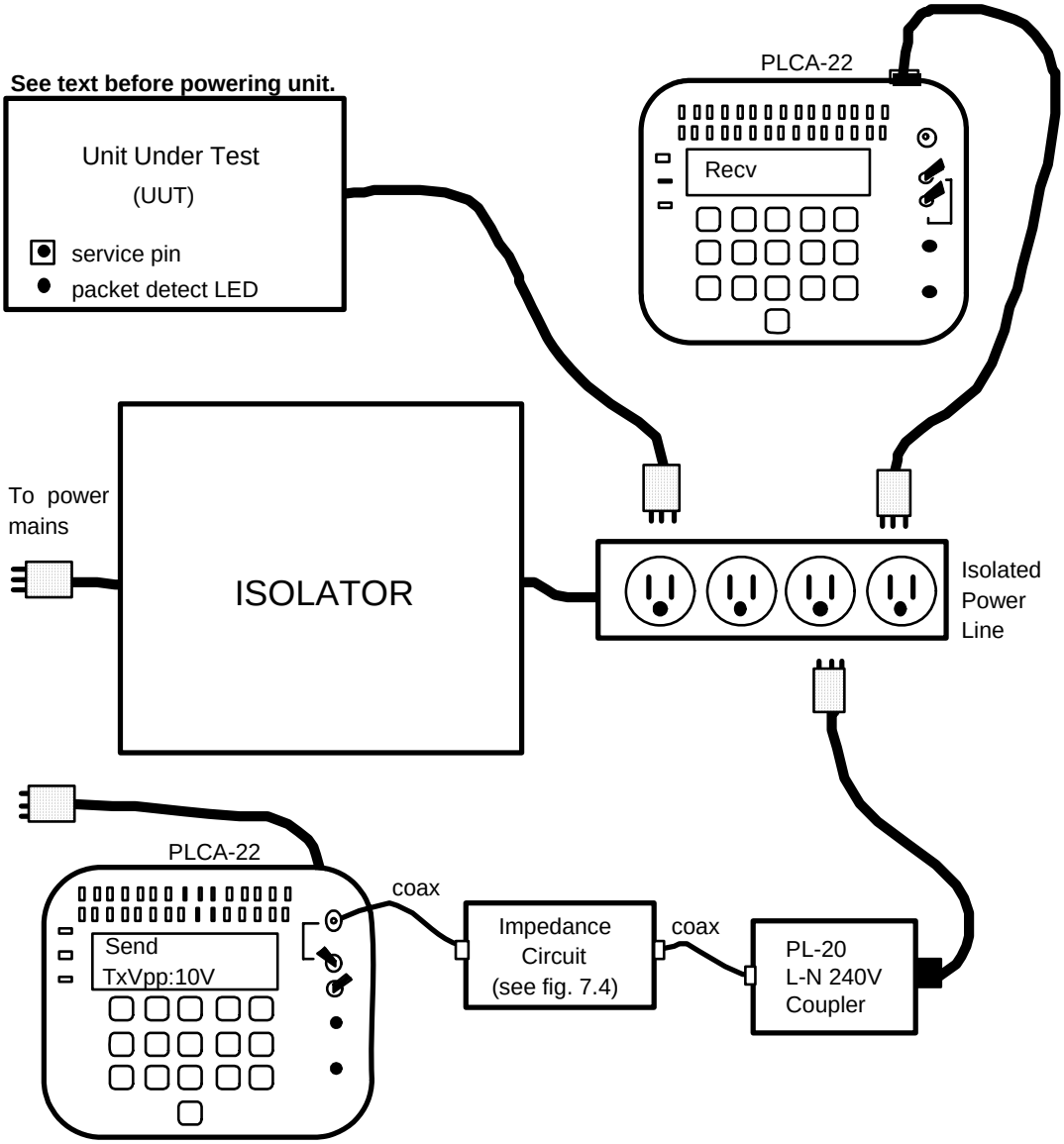


Figure 7.7 Excessive Loading Verification

Transmit Performance Verification

Use the following procedure to verify that the transmit output impedance of the UUT is low enough to adequately drive low impedance loads.

1. With a single PLCA-22 analyzer in idle mode (no packets being transmitted) and set for the same band of operation as the UUT, Internal and Line-to-Neutral coupling, connect the analyzer, the UUT, the "5Ω load", and the Isolator as shown in Figure 7.8 (if the UUT uses Line-to-Earth coupling to a single power phase then the "7Ω load" should be used instead).
2. Verify that the UUT application program is not sending messages. (depending on the application it may be necessary to set the device status to "applicationless" to accomplish this).
3. Press the service switch on the UUT.
4. Observe the primary signal strength LEDs on the PLCA-22 analyzer and check which of the primary LEDs illuminate. All primary LEDs up to, and including, the 0dB LED should flash for at least 6 out of 10 service pin messages from the UUT.
5. Record the result of Step 4 in Table 7.1 at the end of this chapter.

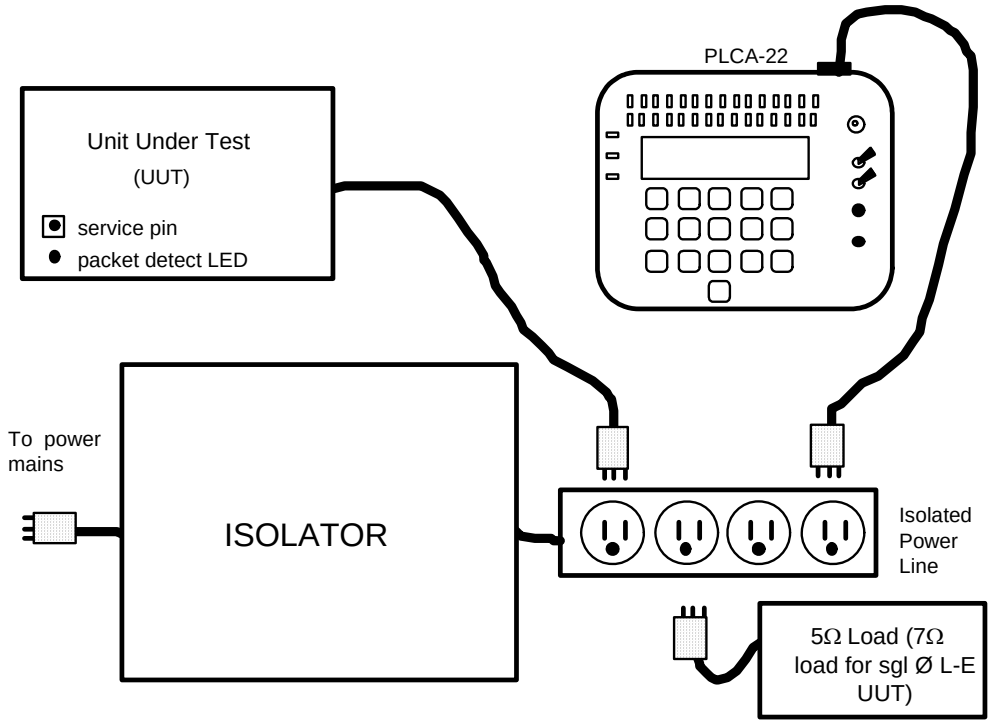


Figure 7.8 Transmit Performance Verification

If the correct LEDs do not illuminate, there might be a problem in the transmit path of the power mains coupling circuit of the UUT. Possible causes of a reduced transmit signal level include:

- Additional series impedance that has been inadvertently added between the transmit amplifier of the PL Smart Transceiver and the mains connection.
- The DC resistance of the series resonant inductor in the coupling circuit (L102 in Chapter 4 coupling circuit figures) is too high.
- The UUT contains a low-current line fuse that has high series resistance.
- A component of the wrong value has been inadvertently used in the UUT.
- Inadequate analog power supply (V_A) voltage under conditions of full transmit current loading.

Refer to the node checklist in Appendix B for more information about verifying the design of the UUT.

Receive Performance Verification

The receive performance verification procedure requires a software tool to measure the number of uncorrupted packets received by the UUT. Packet error rate is then calculated based on the number of packets sent and the number correctly received.

Packet Error Measurement with NodeUtil

A utility called **NodeUtil** (`nodeutil.exe`) is used to measure packets correctly received by the UUT. The NodeUtil software allows a computer to remotely query the UUT and extract its status, including the number of uncorrupted packets received by the device. NodeUtil is available free of charge from the Echelon Web (go to `www.echelon.com/downloads`, select the **Development Tools** category and then select the **NodeUtil Node Utility**).

Figure 7.9 illustrates the setup for the computer running the NodeUtil utility. The computer should contain an Echelon PCLTA-20/SMX card equipped with a PLM-22 SMX transceiver (alternately a U-20 USB network interface can be used for C-band testing). The PCLTA-20/PLM-22 is connected to the isolated power line via a PL-20 power line coupler. Ensure that the proper drivers for the PCLTA-20 and computer operating system are installed. Refer to the *LONWORKS PCLTA-20 PCI Interface User's Guide* for detailed driver setup and operation information.

The verification procedure below describes how to use NodeUtil to access the UUT over the power line.

The startup screen for NodeUtil is shown below. Refer to the "ReadMe Node Util" file for additional setup information.

```
Echelon Node Utility Release 2.04

Successfully installed network interface.

Welcome to the Echelon Node Utility application.

Activate the service pin on remote device to access it.

Enter one of the following commands by typing the indicated letter:
=============================
The main command menu for NODEUTIL is as follows:
F1-- Show Banner.
A -- (A)dd device to list.
D -- Set the (D)omain of the network interface.
E -- (E)xit this application.
F -- (F)ind devices in the current domain.
1 -- Find devices in all (1)-byte domains.
G -- (G)o to device menu....
H -- (H)elp with commands.
I -- Redirect (I)nput from a file.
L -- Display device (L)ist.
M -- Change device (M)ode or state.
O -- Redirect (O)utput to a file.
P -- Send a service (P)in message.
R -- (R)eboot 3150 device.
S -- Report device (S)tatus and statistics.
T -- (T)ransceiver parameters.
V -- Control (V)erbose modes.
W -- (W)ink a device.
Z -- Shell out to command prompt.
NodeUtil>
```

Receive Performance Verification Procedure

The following procedure is used to verify that the receive sensitivity of the UUT is correct. Determination of receive sensitivity is made by monitoring the physical layer error rate while increasing the level of signal attenuation between a reference transmitter and the UUT.

1. Insure that the UUT application program is not sending messages (depending on the application it may be necessary to set the device status to "applicationless" to accomplish this).
2. Set a first PLCA-22 analyzer (referred to as the Recv PLCA-22 analyzer) to the same band of operation as the UUT. Set it for `Recv` and `UnackPri` modes and configure it for Internal, Line-to-Neutral coupling as shown in Figure 7.9.
3. Set a second PLCA-22 analyzer (referred to as the send PLCA-22 analyzer) for the same band of operation as the UUT. Set it for `Send` and `UnackPri` modes of operation and configure it for External coupling. Connect the PLCA-22 analyzer using the attenuation circuit (30.1kΩ resistor of Figure 7.5) and the PL-20 Line-to-Neutral coupler as shown in Figure 7.9. Note that the line cord of the Send PLCA-22 analyzer is connected to the power mains on the input side of the isolator to prevent communications between the two PLCA-22 analyzers via parasitic line cord coupling.
4. Set the following parameters on the Send PLCA-22 analyzer:

Number of Packets	1000 (1k)
Packet Length	13 bytes
TxVpp	3.5V
Attn	0 dB

   Note that 3.5Vp-p TxVpp is used for the Send PLCA-22 even though PL Smart Transceiver-based UUT's transmit using 7Vpp. Setting the Send PLCA-22 analyzer to 3.5Vp-p (6dB lower than the 7Vp-p transmit level of the UUT) provides the opportunity to test for 6dB more receive sensitivity when the analyzer's `Attn` is varied in later steps of this procedure.

5. Connect the UUT test setup as shown in Figure 7.9. Once NodeUtil is running correctly and the start-up screen shown above is displayed, press the service switch on the UUT. This will cause NodeUtil to register the service pin message received from the device. Select the "S" command to obtain the status from the UUT (the entry in the results screen named "Packets received by node" is the number of uncorrupted packets received by the UUT since the last time the statistics were cleared). Type "Y" at the prompt to clear the status of the UUT. The S command will be used in the next few steps to obtain the received packet count from the UUT. Be sure to clear the status of the UUT after each reading.
6. Press START on the Send PLCA-22 analyzer. The test will begin and the receive packet count on the Recv PLCA-22 analyzer should increment with a packet error rate very close to 0% (<1%). The -60dB LED on the primary frequency signal strength meter on the Recv PLCA-22 analyzer should illuminate, indicating that the received signal is approximately -60dB relative to the 3.5Vp-p transmit level (-66dB relative to a 7Vp-p transmit level). This level serves as a starting point; additional attenuation will be added via the `Attn` function of the Send PLCA-22 analyzer in Steps 8 and 9.
7. Once the Send PLCA-22 analyzer has sent 1000 packets and all packet transmission has stopped, obtain the received packet count from the UUT using the NodeUtil **`S`** command. Record that value and the packet error rate of the Recv PLCA-22's analyzer in columns 4 and 5 primary frequency section of Table 7.1 at the end of this chapter. Calculate the error value as a percentage by subtracting the number of packets received by the node from 1011 and then dividing by 10 (divide by 1000 then multiply by 100) and record the result in the right most column of Table 7.1. Refer to the notes at the end of these steps for details of this calculation. If more than 1011 packets are reported as having been received, this likely indicates that the UUT was not cleared immediately before the test was started. In this case clear the UUT statistics and repeat the test.

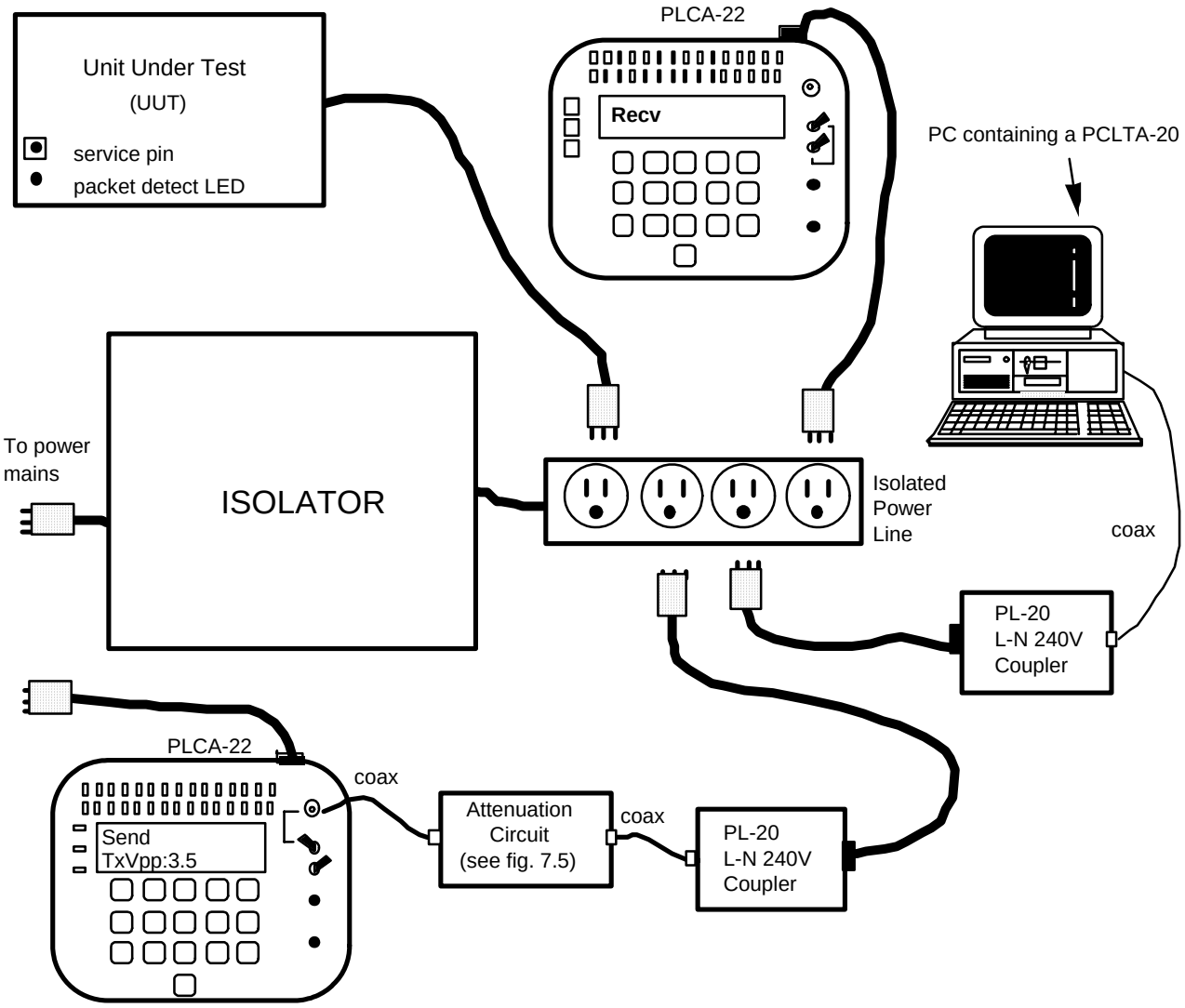


Figure 7.9 Receive Performance Verification

8. After moving the cursor to the `Attn` field, press the CHANGE and ENTER keys on the Send PLCA-22 analyzer to increment the `Attn` level by 6dB. Then clear the status on the UUT by responding with a "Y" to the NodeUtil prompt and then press START on the Send PLCA-22 analyzer.
9. Repeat Steps 7 through 8 above for all **Send Attn** levels up to, and including **24dB**, recording the results each time in Table 7.1 at the end of this chapter.
10. To test the secondary operating frequency of the UUT, change the PLCA-22 analyzers from **UnackPri** to **UnackSec** mode. Repeat Steps 6 through 9, above, but record the results in the secondary frequency section of Table 7.1.

The overall signal attenuation between the Send PLCA-22 analyzer and Recv PLCA-22 analyzer shown in Table 7.1 is the sum of the attenuation level of the attenuator circuit and the `Attn` level of the Send PLCA-22 analyzer plus 6dB resulting from the use of a 3.5Vp-p transmit level on the Send PLCA-22 analyzer. A properly performing PL Smart Transceiver-based product will show a low packet error rate (<3%) up to an overall attenuation of 78dB r.e. 7Vpp (72dB for secondary frequency). Above these attenuations the error rate for the UUT can increase.

If the Recv PLCA analyzer and UUT error rates are not greater than 5% with 90dB of overall attenuation, then there is a problem with the test setup. Check that everything is setup as shown in Figure 7.9. Note that it is common for the UUT to work to approximately 6dB more overall attenuation than the Recv PLCA-22 analyzer due to enhancements in the PL Smart Transceivers.

If the results of this test are worse than expected, it is helpful to know if the problem affects only the performance of the UUT or if adjacent receivers are also impaired by the presence of UUT. If the receive performance of the Recv PLCA-22 analyzer was worse than expected, disconnect the UUT and recheck the PLCA-22 analyzer error rate versus attenuation. If it is determined that the presence of the UUT impairs the performance of the PLCA-22 analyzers then the UUT might be injecting noise back onto the power line. Note that the same symptoms would also be observed if no corrections were made to a UUT which previously failed the Excessive Loading Verification test.

If it is determined through a comparison of the UUT's expected and observed error rates that the UUT cannot reliably receive packets with an overall attenuation of at least 78dB r.e. 7Vp-p, then check the following:

- If the UUT includes a switching power supply, ensure that the power supply noise masks of Chapter 5 have been met.
- Compare the values of the coupling circuit components with those recommended in Chapter 4. It is possible that the wrong value component was inserted and partial, though compromised, receive performance was still possible.
- Examine the PCB to check for solder bridges, broken traces or miss-loaded components.
- Re-verify the Unintentional Output Noise Verification test earlier in this chapter.
- Re-verify the receive mode impedance of the UUT by repeating the Excessive Loading Verification Test earlier in this chapter.

Refer to the node checklist in Appendix B for more information about verifying the design of the UUT.

Notes:

The calculation of packet error rate used in the above verification procedure avoids inaccuracies which would result from the use of CRC error count to compute packet error rate. The material in this note is provided to explain how an accurate measure of packet error rate is determined.

Packet error rate actually includes both packets received with an incorrect CRC plus any packets which were so weak or corrupted they were not detected at all. These “missed packets” are, by definition, not included in the CRC error count of a node. For a physical layer packet error rate of 10%, the percentage of missed packets is generally negligible. Under conditions where the packet error rate is greater than 10%, a significant portion of the error rate might be due to missed packets.

The “Packets received by node” field in NodeUtil software yields the actual number of packets correctly received by the node. Subtracting this number from the total number of packets sent gives the exact packet error count, including missed packets.

In addition to the number of test packets selected on the PLCA-22 analyzers, the total number of packets sent on the power line actually includes several control packets sent between the PLCA-22 analyzers. These control packets are used by the PLCA-22 analyzers to synchronize their settings before the test, and to exchange data related to the test immediately after the test. Additionally, querying the status of the UUT causes a few packets to be logged. The total overhead is generally 11 packets.

Given the above, a more accurate formula for calculating the physical layer packet error rate with 1000 test packets is then:

PER% = (1011 - # “Packets received by node”) x 100 / 1011

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Table 7.1 PL 3120/PL 3150/PL 3170 Smart Transceiver Performance Verification

Manufacturer		Test spec	Echelon 005-00193-01 Ch 7
Product		Line voltage	_____VAC
Neuron Core ID	_____ _____ _____ _____ _____ _____	Line frequency	_____50Hz _____60Hz
Band	_____A-band _____ C-band	Date tested	_____/_____/_____
Coupling type	_____1-Phase _____ 2-Phase _____ 3-Phase	Tested by	

Preliminary Checks

		Fail	Pass
V_A power supply voltage	10.8V to 18.0V _____V		
V_{DD5} power supply voltage	4.75V to 5.25V _____V		
Oscillator frequency	(6.5523 to 6.5549 or 9.9980 to 10.0020MHz)_____MHz		

Good Citizen Verification

Unintentional Output Noise Verification-UUT and RX analyzer with no packet transmission		Fail	Pass
Primary signal LEDs	-72dB not "on" solid and -66dB not flashing _____dB_____		
Secondary signal LEDs	-72dB not "on" solid and -66dB not flashing _____dB_____		
Packet Detect LED	must not flash more than once per minute _____/min		

Excessive Loading Verification - Send 10Vpp through 88.7Ω and external coupler		Fail	Pass
RX analyzer primary LEDs	-3dB LED must be "on" or flashing ____dB____on____Flash		

Transmit Performance Verification - RX analyzer reading UUT svc pin msg. 5/7Ω load		Fail	Pass
RX analyzer primary LEDs	0dB LED must flash ≥6/10 tries ____dB____/10 tries		

Receive Performance Verification - Send 1kpkts at 3.5Vpp through 30.1kΩ attenuator	Fail	Pass

Primary Frequency

Send PLCA Transmit Attenuation (Attn)	Overall Attenuation (Attn + 66)	Recv PLCA UnackPri Error% (expected)	Recv PLCA UnackPri Error% (observed)	UUT #Pkts Received (observed)	UUT Pri Error% (expected)	UUT Pri Error% (1011-#Rcvd)/10
0 dB	66 dB	<1%	%		<1%	%
6 dB	72 dB	<3%	%		<2%	%
12 dB	78 dB	any	%		<3%	%
18 dB	84 dB	any	%		any	%
24 dB	90 dB	≥5%	%		≥5%	%

Secondary Frequency

Send PLCA Transmit Attenuation (Attn)	Overall Attenuation (Attn + 66)	Recv PLCA UnackSec Error% (expected)	Recv PLCA UnackSec Error% (observed)	UUT #Pkts Received (observed)	UUT Sec Error% (expected)	UUT Sec Error% (1011-#Rcvd)/10
0 dB	66 dB	<1%	%		<1%	%
6 dB	72 dB	any	%		<3%	%
12 dB	78 dB	any	%		any	%
18 dB	84 dB	any	%		any	%
24 dB	90 dB	≥5%	%		≥5%	%

Chapter 8

PL Smart Transceiver Programming

Introduction

Certain parameters of PL Smart Transceivers are programmed by the developer. This chapter provides an explanation of the various choices and how they are programmed by way of the NodeBuilder® Development Tool, Mini EVK Evaluation Kit, or ShortStack® Developer's Kit.

The factory preprogrammed settings for the PL 3120 and PL 3170 Smart Transceivers are in accordance with the PL-20N "standard transceiver type" described in this chapter. This allows programming these chips in a system through the power line network without having to pre-program the parts using a programmer.

Dual Carrier Frequency Mode

Each PL Smart Transceiver incorporates dual carrier frequency capability which allows it to communicate with other PL Smart Transceiver and PLT-22-based devices, even if noise is blocking its primary communication frequency range. If impairments prevent communication in this range, a PL Smart Transceiver based device can automatically switch to a secondary carrier frequency to complete a transaction with other PL Smart Transceiver or PLT-22-based devices.

With the dual carrier frequency feature the last two retries of acknowledged service messages are sent using the secondary carrier frequency. Thus, in C-band and when acknowledged service is used with three retries (four total tries), the first two tries are sent using the 132kHz primary carrier frequency. If the last two tries are needed to complete the transaction, they are sent (and acknowledged) using the 115kHz secondary carrier frequency. Similarly, for A-band operation the primary and secondary frequencies are 86kHz and 75kHz respectively. A minimum of two retries must be used if the PL Smart Transceiver is to be able to use both carrier frequency choices. For optimum reliability and efficiency, Echelon recommends the use of three retries when using acknowledged service messaging with the PL Smart Transceiver when heartbeats are not used.

When the repeated message service is used, the PL Smart Transceiver leverages the reliability of both carrier frequencies by alternating between them. In this case, a repeated message with three repeats results in the first and third packets being sent using the primary carrier frequency, while the second and fourth packets are sent using the secondary carrier frequency. A minimum of one repeat must be used with the repeated service for the PL Smart Transceiver to use both carrier frequency choices.

In the C-band mode of operation, every PL Smart Transceiver transmission at the secondary carrier frequency is accompanied by a simultaneous 132kHz "pilot" signal which older PLT-20 and PLT-21-based devices can use to recognize that the channel is busy. This pilot signal prevents PLT-20- or PLT-21-based devices (which cannot detect the 115kHz secondary carrier frequency) from transmitting at the same time that a PL Smart Transceiver is transmitting on its 115kHz secondary carrier frequency.

CENELEC Access Protocol

To allow multiple power line signaling devices from different manufacturers to operate on a common AC-mains circuit, the CENELEC EN 50065-1 standard specifies an access protocol for the C-band (125kHz to 140kHz). The 132.5kHz frequency is designated as the primary band-in-use frequency that indicates when a transmission is in progress.

Every CENELEC compliant C-band device must both monitor the 132.5kHz band-in-use frequency and be able to detect the presence of a signal of at least 86dBμV_{RMS} anywhere in the range from 131.5kHz to 133.5kHz which has a duration greater than or equal to 4 milliseconds. A power line signaling device is permitted to transmit if the band-in-use detector shows that the band has been free for at least 85 milliseconds. Each device must randomly choose an interval for transmission, and at least seven evenly distributed intervals must be available for selection. A group of power line signaling devices is allowed to transmit continually for a period less than or equal to one second, after which it must cease transmitting for at least 125 milliseconds.

The PL Smart Transceivers incorporate the CENELEC access protocol and the user can enable or disable the CENELEC access protocol at the time of channel definition. When enabled, the PL Smart Transceiver enforces the CENELEC

access protocol while still maintaining the benefits of the LonTalk protocol. When the CENELEC access protocol is enabled, overall network throughput is reduced by 11%.

The CENELEC access protocol must be enabled to meet regulatory requirements in countries that follow CENELEC regulations (i.e., most European countries). It is recommended that the CENELEC access protocol be disabled on products that will be used in any country that does not follow CENELEC regulations, in order to maximize throughput. Note that devices that have the CENELEC protocol enabled should not be installed on the same network with devices that have the CENELEC protocol disabled. In this instance the devices with the CENELEC protocol enabled would be prevented from transmitting whenever there was heavy traffic from the CENELEC protocol disabled devices. Thus all of the devices on a single channel should either have their CENELEC protocol enabled or they should all have it disabled. A CENELEC Configuration Library is available at www.echelon.com/downloads. This library can be used with the NodeBuilder or Mini EVK tools to control support for the CENELEC protocol at runtime. The PL 3170 Smart Transceiver includes the CENELEC Configuration Library function in ROM.

CENELEC regulations do not specify an access protocol for use in the CENELEC A-band. When programmed with the A-band transceiver parameters described later in this chapter, the internal CENELEC access protocol for the PL Smart Transceiver is disabled. With this selection, an active Band-In-Use signal will not prevent a PL Smart Transceiver from transmitting.

Power Management

PL Smart Transceivers incorporate a power management feature that supports the design of low cost power supplies in very cost sensitive consumer applications such as networked light dimmers, switches, and household appliances. This class of application typically requires only occasional low-duty cycle, transmission from the device. Power supplies for these devices can take advantage of the very low receive current and wide V_A supply range of the PL Smart Transceiver to charge a capacitor during receive mode, and then use the energy stored on the capacitor for transmission. With this feature the continuous current rating of the power supply can actually be less than the current required for transmission since it only needs to support the receive mode current of the device—plus a modest amount to recharge the capacitor. Examples of these “Energy Storage Power Supplies”, and a detailed description of how they work, are provided in Chapter 5.

In order for a device incorporating an energy storage power supply to function properly it is essential that the device not be required to transmit more than about 10% of the time so that there is sufficient time for the supply to recharge the capacitor between transmissions under worst case conditions for the supply. The power management feature built into each PL Smart Transceiver monitors the V_A supply voltage and, when enabled, automatically regulates the flow of queued packets to maintain the V_A supply above its required minimum level. Should the device attempt to transmit too frequently, the power management feature enforces a limit on the transmit duty cycle by preventing the PL Smart Transceiver from transmitting until the power supply of the device recovers to the point that sufficient energy is available to transmit a packet. Details of this feature are provided in Chapter 5.

The user can enable or disable power management by selecting how the Out-Of-Gas (OOGAS) pin of the PL Smart Transceiver is connected ***and*** by the “standard transceiver type” that is selected at the time of channel definition. If the OOGAS pin of the PL Smart Transceiver is connected directly to its VCORE pin then power management is disabled independent of the standard transceiver type that is used. If the OOGAS pin of the PL Smart Transceiver is connected to the resistive voltage divider specified in the selected hardware reference design, then the user can enable power management at the time of channel definition by choosing a standard transceiver type with a “LOW” suffix. The only difference between a set of standard transceiver parameters with the “LOW” suffix and the corresponding set without the “LOW” suffix is whether the power management feature is selected or not. Enabling power management requires both, use of the specified OOGAS voltage divider and a standard transceiver type with a “LOW” suffix.

When power management is enabled, PL Smart Transceivers require a V_A supply voltage of 13.0V before they can be assured of transmitting a packet. A product with a fixed V_A power supply less than or equal to 13.0V should never have power management enabled because it might not be allowed to transmit. Likewise a device whose power supply relies on power management to operate correctly should never have the power management feature disabled. Table 8.1 summarizes these points.

Table 8.1 Power Management Requirements Vs. Type of Power Supply

Power Management	**Fixed V_A Power Supply ≤13.0V**	**Energy Storage V_A Power Supply >13.0V in Receive Mode**
Disabled	OK	Not allowed if the power supply design relies on power management for worst case duty cycle and supply conditions.
Enabled	Not allowed: device might not transmit	OK

Note that some legacy network tools load a device's communication parameters as part of the installation and replacement process and calculate those parameters based on the channel (rather than the particular device). Such tools cannot be used for systems that contain a mixture of devices with and without power management enabled on the same channel.

Tools based on the LNS® network operating system, such as the LonMaker® Integration Tool, correctly support all configurations of PL Smart Transceiver based devices with or without power management. For a tool not based on LNS, contact your tool vendor to determine if it can support a mixture of power management and non-power management devices on the same channel.

Standard Transceiver Types

Two standard transceiver types are defined for the PL Smart Transceivers operating in A-band and four are defined for C-band operation. These standard transceiver types specify communications parameters for a PL Smart Transceiver (or PLT-22, PLT-21, or PLT-20) based device.

In A-band, the two available communication parameters differ only with regard to selection of the power management feature.

In C-band, the communication parameters of the four standard types are identical except for the state of the CENELEC protocol and selection of the power management feature.

Table 8.2 shows how the various features of the PL Smart Transceiver are selected using the six standard transceiver types and OOGAS pin on the PL Smart Transceiver.

Table 8.2 Standard PL Smart Transceiver Types

Standard Transceiver Type	Band	Communications Parameters	CENELEC Protocol	Power Management	
				OOGAS Pin Connected to VCORE Pin	OOGAS Pin Connected to Specified Resistors
PL-20N (factory default)	C	0E 01 00 10 00 00 00	Disabled	Disabled	Disabled
PL-20C	C	4A 00 00 10 00 00 00	Enabled	Disabled	Disabled
PL-20N-LOW	C	0E 01 00 12 00 00 00	Disabled	Disabled	Enabled
PL-20C-LOW	C	4A 00 00 12 0000 00	Enabled	Disabled	Enabled
PL-20A	A	0E 01 00 10 00 01 00	Disabled	Disabled	Disabled
PL-20A-LOW	A	0E 01 00 12 00 01 00	Disabled	Disabled	Enabled

Development Tools Support

Applications for the PL Smart Transceivers can be developed using the Mini EVK Evaluation Kit, NodeBuilder Development Tool, or ShortStack Developer's Kit. These tools are described in the following sections. The LonBuilder Developer's Workbench cannot be used to develop applications for the PL Smart Transceivers.

Mini EVK Evaluation Kit

The Mini EVK Evaluation Kit can be used to evaluate the LONWORKS platform and PL Smart Transceivers, and can also be used to develop a prototype or production device based on the PL 3120 or 3150 Smart Transceiver. Any release of the Mini EVK can be used to develop applications for the PL 3120 or 3150 Smart Transceiver, though Release 1.02 or newer is recommended. A free update to Release 1.02 is available for Mini EVK Release 1.00 and 1.01 at www.echelon.com/downloads.

To develop an application for a PL Smart Transceiver using the Mini EVK, one of the following hardware templates must be selected under **Target Hardware** in the Mini Application:

- PL 3120 Evaluation Board (CENELEC off)
- PL 3120 Evaluation Board (CENELEC on)
- PL 3150 Evaluation Board (CENELEC off)
- PL 3150 Evaluation Board (CENELEC on)

Custom hardware can be developed with the Mini EVK,as long as the custom hardware has the same hardware properties—such as clock speed and memory map—as one of the four PL evaluation boards. Developers requiring other hardware configurations must use the NodeBuilder Development Tool.

NodeBuilder Development Tool

The NodeBuilder Development Tool can be used to develop a prototype or production device based on the PL 3120, 3150, or 3170 Smart Transceiver. Release 3.1 or newer of the NodeBuilder Development Tool is required to develop applications for the PL 3120 or 3150 Smart Transceiver. NodeBuilder 3.14 (NodeBuilder 3.1 with Service Pack 4) or newer is required to develop applications for the PL 3170 Smart Transceiver. NodeBuilder 3.1 Service Pack 4 is available for free download from www.echelon.com/downloads.

PL Smart Transceiver Channel Definitions

The appropriate standard transceiver type (PL-20N, PL-20C, PL-20N-LOW, PL-20C-LOW, PL-20A or PL-20A-LOW) is selected on the NodeBuilder Hardware Template Properties page, as shown in the figure below:

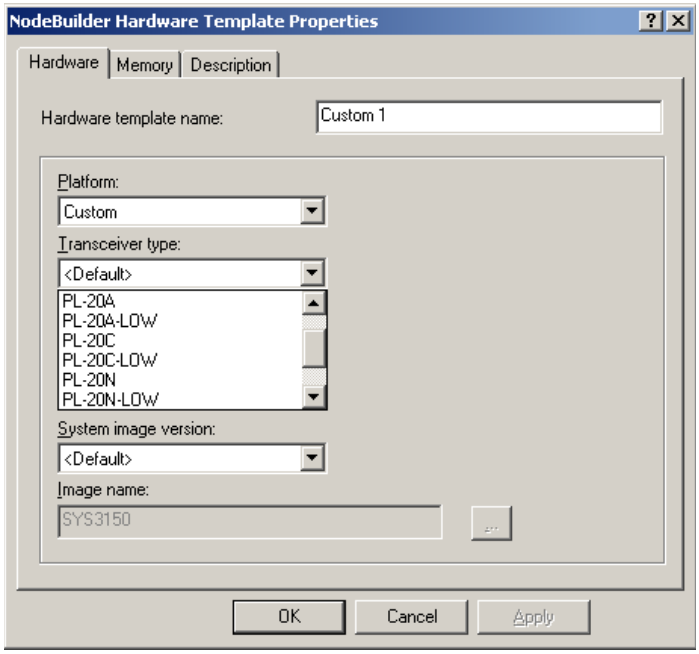


Figure 8.1 Choosing the Standard Transceiver Type in NodeBuilder Tool

PL Smart Transceiver Clock Speed Selection

When operating in A-band the PL Smart Transceiver uses a 6.5536MHz crystal and thus a clock speed of 6.5536MHz must be selected on the NodeBuilder Hardware Template Properties page as shown on the left of Figure 8.2. For C-band operation where a 10MHz crystal is used a clock speed of 10MHz must be selected as shown on the right of Figure 8.2.

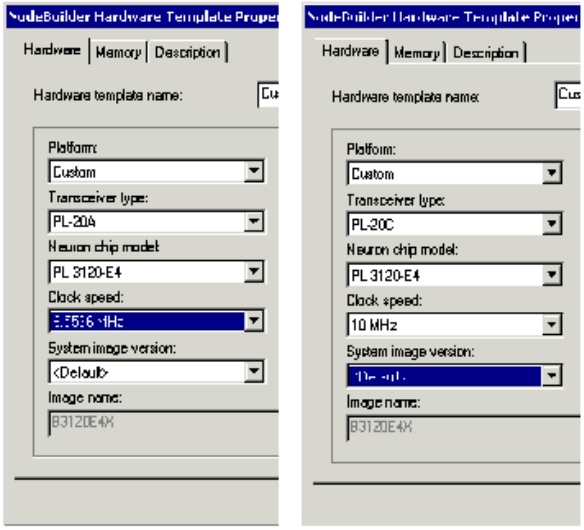


Figure 8.2 Choosing the Clock Speed in NodeBuilder

ShortStack Developer's Kit

The ShortStack Developer's can be used to develop a prototype or production device based on the PL 3120, 3150, or 3170 Smart Transceiver, with an application that runs on an attached microcontroller. Any release of the ShortStack Developer's Kit can be used to develop applications for the PL 3120 or 3150 Smart Transceiver. ShortStack 2.1 (or newer) is required to develop applications for the PL 3170 Smart Transceiver. ShortStack 2.1 can be used to develop applications with up to 254 network variables and can also be used to develop self-installed applications that use ISI. A PL 3150 Smart Transceiver must be used to support more than 62 network variables, or to support ISI applications developed using ShortStack 2.1.

The ShortStack 2.1 Developer's Kit includes three pre-built memory images that can be used to load ShortStack images on a PL Smart Transceiver. There is one image for a PL 3120 Smart Transceiver without ISI, and two images for a PL 3150 Smart Transceiver—one with and one without ISI support. Custom ShortStack images can be created using the NodeBuilder Development Tool or Mini EVK Evaluation Kit.

Downloading Application and Transceiver Type Parameters

A developer can solder the PL 3120 or PL 3170 Smart Transceiver into a device and load applications and different transceiver parameters using the NodeLoad utility. This utility is a command-line application available as a free download from the Echelon Web site (go to www.echelon.com/downloads, select the **Development Tools** category, and then select the **NodeLoad Utility**).

The PL 3120 and PL 3170 Smart Transceiver devices arrive from the factory with an initial set of transceiver parameters pre-loaded for programming purposes. To ensure optimal operation, you must re-program the transceiver parameters for all PL 3120 and PL 3170 chips.

For a PL 3120 Smart Transceiver-based device, you can use the NodeLoad utility with the –X option to change the transceiver parameters from the factory default parameters to any of the supported parameters. For a PL 3170 Smart Transceiver-based device, you can use the utility to change the parameters to any of the various C-band types (the PL 3170 Smart Transceiver does *not* support A-band operation). To load transceiver parameters using the NodeLoad utility, you must use the *.NDL or *.NEI image because the *.NXE image does not contain transceiver parameter values. You can also use a universal programmer, such as BP Microsystems' programmer or HiLo System's programmer, to change the parameters prior to soldering the chip onto your PCB board. Any valid transceiver parameters included in the image files generated by the NodeBuilder Development Tool or the Mini EVK Evaluation Kit are supported.

If you reboot a PL 3120 or PL 3170 Smart Transceiver, the smart transceiver will restore the factory default parameters and go back to the initial state. Rebooting in this case refers to any of the following operations:

Software	Action
LNS application	Invoking the Reboot() method for AppDevice or Router object
NodeUtil utility version older than 1.96	Sending the "Reboot" command for the device
network management command with the appl_reset option	Writing a value of zero to the second byte of the transceiver parameters on the Smart Transceiver and resetting the device with the Set Node Mode

If you simply power cycle or reset your device, it will maintain the programmed change and will NOT restore the factory default.

When building devices with energy storage power supplies, care must be taken to insure the power supply does not drop below 10 volts during programming or before the LOW transceiver parameters are loaded. This can in some cases be accomplished by using a higher voltage on the power line input or alternately by directly applying the V_A voltage using pogo pins into the device. The first step when using the NodeLoad utility should be to download the PL 3120/PL 3170 Smart Transceiver parameters. See the NodeLoad utility user's guide for how to download these parameters.

The NodeLoad utility supports the Echelon standard power line network interfaces. The maximum download time is about 30 seconds for an application that consumes all available EEPROM memory in the PL 3120 or PL 3170 Smart

Transceiver. If a production line is capable of producing one completed device every 10 seconds, then 3 NodeLoad stations will be required to keep up with the production volume. Isolators will be required at each NodeLoad station to prevent communication from occurring between stations. See the *Power Line Test Isolator* section in Chapter 7 for details on how to build your own isolator.

A

PL Smart Transceiver Reference Designs

Introduction

This appendix describes the implementation of the external, discrete interface circuitry for the PL 3120, PL 3150 and PL 3170 Smart Transceivers. The interface circuitry includes the front-end filter for the receiver and the power amplifier for the transmitter. The interface is comprised of roughly fifty components, primarily resistors and capacitors. Echelon provides a comprehensive **PL Development Support Kit** (DSK) for implementing the interface circuitry. The section that follows lists the contents of the DSK. Contact your Echelon salesperson to purchase the DSK.

A variety of **reference designs** are provided with the DSK to address applications requiring different numbers of printed circuit board (PCB) trace layers, single- or double-sided component assembly, various aspect ratios, and transmit current requirements. Each PL Smart Transceiver reference design package consists of a zip archive file that contains all of the relevant files for that design. The naming convention used for these zip files is shown in the figure below.

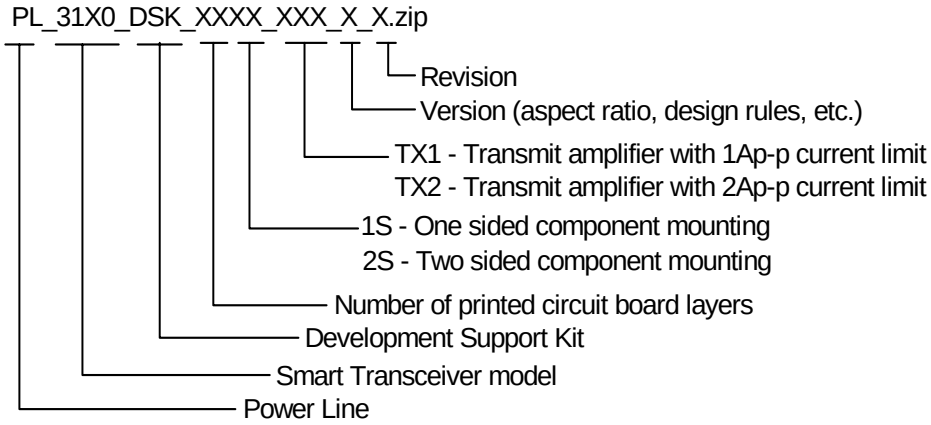


Figure A.1 Reference Design Naming Convention

Development Support Kit Contents

The PL Smart Transceiver DSK includes the following reference designs:

Reference Design Number	PL Smart Transceiver Model	Description	Zip File Name
1200F	PL3120-E4T10 or PL3170-E4T10	2 layer 23x63mm PCB layout with 1-sided component mounting and 1Ap-p transmit amplifier	Reference Designs\1200
1201F	PL3120-E4T10 or PL3170-E4T10	4 layer 20x38mm PCB layout with 2-sided component mounting and 1Ap-p transmit amplifier	Reference Designs\1201
1204E	PL3120-E4T10 or PL3170-E4T10	2 layer 33x38mm PCB layout with 1-sided component mounting and 1Ap-p transmit amplifier	Reference Designs\1204
1205E	PL3150-L10	4 layer 36x49mm PCB layout with 2-sided component mounting and 1Ap-p transmit amplifier	Reference Designs\1205
1209E	PL3120-E4T10 or PL3170-E4T10	4 layer 31x53mm PCB layout with 2-sided component mounting and 2Ap-p transmit amplifier	Reference Designs\1209
1217D	PL3120-E4T10 or PL3170-E4T10	4 layer 17x38mm PCB layout with 2-sided component mounting and 1Ap-p transmit amplifier (**SIP Design**)	Reference Designs\1217
1218E	PL3150-L10	4 layer 48x66mm PCB layout with 2-sided component mounting and 2Ap-p transmit amplifier	Reference Designs\1218
1255C	PL3120-E4T10 or PL3170-E4T10	4 layer 17x28mm PCB layout with 2-sided component mounting and 1Ap-p transmit amplifier **(SIP Design)**	Reference Designs\1255

Reference Design Files

For each reference design the following files are provided.

File Name	Description
`Circuit Description.pdf`	Document describing the operation of the reference circuitry
`Using the Reference Layouts.pdf`	Explains how to use the reference layout files
`Using the Viewer.pdf`	Description of how to obtain and use a free P-CAD® viewer
`012-xxxx-51_R_Schematic.dsn`	Schematic design file in OrCAD® format
`012-xxxx-51_R_Schematic.pdf`	Schematic design file in PDF format
`012-xxxx-51_R_BOM.doc`	Bill of materials in MS Word format
`012-xxxx-51_R_BOM.pdf`	Bill of materials in PDF format
`373-xxxx-51_R_Layout_PCAD.pcb`	Layout design file in P-CAD format
`373-xxxx-51_R_Layout_Altium.pcbdoc`	Layout design file in Altium® format (See note 2)
`373-xxxx-51_R_Layout_PADS.pcb`	Layout design file in PADS/PowerPCB format (See note 2)
`373-xxxx-51_R_Layout_OrCAD.max`	Layout design file in OrCAD format (See note 2)
`373-xxxx-51_R_Layout_ASCII.pcb`	Layout design in ASCII format
`373-xxxx-51_R_Layout_PDIF.zip`	Layout design in P-CAD Database Interchange (PDIF) format (zip file)
`373-xxxx-51_R_Layout_Gerbers.zip`	Layout layer plots in Gerber format (zip file)
`373-xxxx-51_R_Layout.pdf`	Layout layer plots in PDF format

Notes:

1. Since reference design numbers 1217 and 1255 document layouts that can be directly fabricated in the form of a SIP module, they also include an assembly package (zip file) which contains an assemble drawing, pick and place file, and paste stencils. In addition, the Gerber package (zip file) for these two reference designs includes drill files.

2. The 1217 reference design does not include layout files in Altium, PADS, or OrCAD formats.

Reference Design Specifications

Recommended Operating Conditions for Reference Designs with 1Ap-p Transmit Amplifier

Symbol	Parameter	Min	Typ	Max	Unit
V_{ARX}	V_A Supply Voltage - Receive Mode	8.5	12.0	18.0	V
V_{ATX}	V_A Supply Voltage - Transmit Mode (1)	10.8	12.0	18.0	V
T_A	Ambient Temperature (1)	-40	25	85	°C

Electrical characteristics of Reference Designs with 1Ap-p Transmit Amplifier
(over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Unit
I_{ARX}	V_A Supply Current - Receive Mode		350	500	µA
I_{ATX}	V_A Supply Current - Transmit Mode		120	250	mA
V_{OTX}	Transmit Output Voltage		7		Vp-p
I_{TXLIM}	Transmit Output Current Limit		1.0		Ap-p
Z_{INRX}	Input Impedance - Receive Mode (with recommended RXCOMP inductor)		500		Ω
Z_{OTX}	Output Impedance - Transmit Mode		0.9		Ω
V_{PMU}	Power Management - Upper V_A Threshold	11.2	12.1	13.0	V
V_{PML}	Power Management - Lower V_A Threshold	7.3	7.9	8.6	V

NOTE 1: Minimum value can be 8.5V under certain conditions (refer to Chapter 5 for details).
The following formula must also be satisfied:

$$V_{ATXAVE} < \frac{150 - T_{AMAX}}{k x D_{MAX}}$$

Where:
V_{ATXAVE} = Average V_A supply voltage while transmitting
T_{AMAX} = Maximum ambient temperature (degrees C)
D_{MAX} = Maximum transmit duty cycle of the device (expressed as a decimal number where 0.64 is the practical max)
k = 8.0 for reference design numbers 1200, 1201, 1204, 1205, and 1217
k = 9.3 for reference design number 1255

V_{ATXAVE} formula results for common input values:

T_{AMAX}	D_{MAX}	V_{ATXAVE} w/ most 1Ap-p Amps	V_{ATXAVE} w/ #1255 1Ap-p Amp
85C	64%	12.7V	10.9V
70C	64%	15.6V	13.4V
85C	45%	18V (V_A max limit)	15.5V
70C	55%	18V (V_A max limit)	15.6V
55C	64%	18V (V_A max limit)	15.9V

Recommended Operating Conditions for Reference Designs with 2Ap-p Transmit Amplifier

Symbol	Parameter	Min	Typ	Max	Unit
V_{ARX}	V_A Supply Voltage - Receive Mode	12.0	15.0	18.0	V
V_{ATX}	V_A Supply Voltage - Transmit Mode (1) C-band A-band	14.25 12.0	15.0 15.0	18.0 18.0	V V
T_A	Ambient Temperature (1)	-40	25	85	°C

Electrical characteristics of Reference Designs with 2Ap-p Transmit Amplifier
(over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Unit
I_{ARX}	V_A Supply Current - Receive Mode		350	500	µA
I_{ATX}	V_A Supply Current - Transmit Mode		160	500	mA
V_{OTX}	Transmit Output Voltage C-band A-band		10 8		Vp-p
I_{TXLIM}	Transmit Output Current Limit		2.0		Ap-p
Z_{INRX}	Input Impedance - Receive Mode (with recommended RXCOMP inductor)		500		Ω
Z_{OTX}	Output Impedance - Transmit Mode		0.7		Ω

NOTE 1: The following formula must also be satisfied:

$$V_{ATXAVE} < \frac{150 - T_{AMAX}}{5.6 \times D_{MAX}}$$

Where:
V_{ATXAVE} = Average V_A supply voltage while transmitting
T_{AMAX} = Maximum ambient temperature (degrees C)
D_{MAX} = Maximum transmit duty cycle of the device (expressed as a decimal number where 0.64 is the practical max)

The Importance of Using Development Support Kit (DSK) Reference Designs

Each DSK reference design implements a very wide dynamic range circuit that is sensitive to layout variations. In the same way that traces of radio PCB are part of the design, the traces, pads and copper pours of the Smart Transceiver reference layouts are part of the design and must not be altered,. With the proper layout, each Smart Transceiver is capable of receiving signals measured in hundreds of micro-volts (millionths of a volt). Even apparently minor changes to the layout can compromise performance and render the device unsuitable for many applications.

Every Power Line Smart Transceiver transmits signals on the order of several volts and is capable of driving 1 to 2 amperes of current into a low-impedance power line. Careful circuit layout is required to ensure that heat is properly dissipated and that the amplifier remains stable across the full range of operating conditions. Ordinary circuit layout practices are not suitable for driving high frequency modulated signals at high currents. The combination of voltage and current produced by the transmit amplifier results in significant heat which requires very careful component placement and design of the PCB copper areas to achieve proper dissipation.

Each DSK reference design has been subjected to thorough electrical and thermal analysis which addresses all of the above issues. The DSK reference designs have been thoroughly validated by Echelon using the following:

- A multi-hundred hour validation test at voltage and temperature extremes;
- Verification of compliance with a twenty-six point checklist, which was developed based on knowledge drawn from dozens of Smart Transceiver implementations; and
- Circuit simulation using Monte Carlo techniques covering thousands of circuit instantiations to ensure that all critical performance parameters are maintained over the full range of component tolerance and environmental conditions.

Any deviation from the DSK reference layouts will very likely result in degraded performance in one or more of the areas listed in the table below.

Critical Area	**Consequences of not following Guidelines**	**Causes for Consequence(s)**	**Solutions**
Electromagnetic Compliance (e.g., conducted emissions, surge, or ESD)	- Multiple PCB layout iterations - Field failures due to degraded surge immunity - Intermittent operation due to degraded ESD immunity	- Deviating from DSK reference lay-outs - Ignoring the coupling circuit and power supply recommendations in Chapters 4 and 5	- Use an approved DSK reference design without modification - Follow the recommendations in Chapters 4 and 5 - Submit the design for a design review by Echelon
Heat Management	- Premature field failure	- Changing the relative position of components on the reference layout - Reducing the quantity or location of copper on the reference layout - Adding “thermal reliefs” to the reference copper design	- Use an approved DSK reference design without modification - Submit the design for a design review by Echelon
Communication Performance	- Devices that function under typical laboratory conditions may not be able to communicate under worst case field conditions - Low production yield	- Changing the relative proximity or dimensions of certain PCB traces on the reference design - Ignoring the coupling circuit and power supply recommendations in Chapters 4 and 5	- Use an approved DSK reference design without modification - Follow recommendations in Chapters 4 and 5 - Verify that the frequency of the crystal oscillator is centered as described in Chapter 2 - Verify communication performance as described in Chapter 7 - Submit the design for a design review by Echelon

All of the above issues can be avoided by using DSK reference designs without modification, and by following the coupling circuit, power supply, and crystal oscillator recommendations in Chapters 2, 4, and 5 of this data book.

Echelon offers a comprehensive design review service to assist developers with respect to adherence to the DSK and Data Book requirements. Contact your local distributor or Echelon sales person to arrange for a design review.

B

PL Smart Transceiver-Based Device Checklist

Introduction

This appendix includes a checklist that can be used to verify critical design elements described in this user's guide. Verifying compliance with these items is an important step toward insuring that a Smart Transceiver-based product realizes the full communication performance of the PL Smart Transceiver. All of the items listed below should be carefully checked prior to releasing a design either for review by Echelon or for production.

Echelon offers a confidential design review process that provides an independent review of most items on this list. Contact your local Echelon sales representative to arrange for a review. Note that the following items must be provided with each design review submission to Echelon:

1) Schematic diagrams in PDF format
2) Gerber files of the PCB(s) including **all** layers
3) A detailed bill of material including all required component specifications, vendor names and part numbers
4) Answers to checklist question numbers 1, 25 and 45

If the product design is modular, then the above documentation should be provided for all relevant modules including the power supply, PL reference design, and coupling circuit.

Supplying the following additional documentation is also recommended in order to expedite the design review process:

1) Soft copy of data sheets for any components that are; only available locally, unique, or custom components. The specifications of individual components are checked as part of the design review process. Due to the number of components that must be reviewed, if documentation is not readily available on the Internet or provided in the review package, such components can not be reviewed.
2) Bill of Material with a column added listing the original reference designations if they differ from the designations in the DSK and data book.
3) Any additional notes that provide information relevant to the design. This may include explanations of parts of the design not included in the documentation, or aspects of the design that may be obscure.
4) Explanation of "compound designs" where different variations exist depending on component selection. Note that the BOM should indicate component selections for each variant.

Having reviewed dozens of products, Echelon has made note of the most common errors. These items are indicated below with and asterisk after the item number. Special care should be taken to ensure that these items are implemented correctly.

All pages of Appendix B can be copied.

Device Checklist

PL Smart Transceiver Development Support Kit (DSK) Reference Design (refer to the DSK and Chapter 2)

Item	OK?	Description
1		Reference design used:_____ Use the name of the ZIP archive file containing the reference design document (for example, `PL_3120_DSK_2L1S_TX1_1_R`).
2 *		Check that the reference design portion of the circuit is an accurate copy of the reference layout without any deviations. This check can be performed using a Gerber viewer to overlay the new design with the reference design. Describe any deviations from the reference layout (note that more than 30 critical layout features have been carefully designed into each reference layout and thus only very minor well justified deviations from the reference layout can be accepted):
3		Check that fabrication notes from the DSK layout files are correct and included in the fabrication documentation for the device (i.e., PCB material, layer thickness, plating and via clearance).
4 *		Verify that "thermal reliefs" have not been added to Q4, Q5, R21, R22 or R23 (note that some PCB layout tools automatically add thermal reliefs, but proper heat dissipation from these devices requires a solid copper connection without thermal reliefs).
5 *		Verify that the copper areas that provide thermal coupling between Q4 & Q2B and between Q5 & Q3A match the reference layout (note that some PCB layout tools automatically modify certain features of these areas but proper thermal management requires a direct match to the reference layout).
6		Verify that the in-circuit-test (ICT) points of the reference design have been preserved (note that some PCB layout tools may delete these test points yet ICT is required in order to insure proper component assembly).
7 *		Check that the layout of the traces to the crystal have not been modified, or if a crystal with a different pad pattern is chosen verify that the capacitance to ground (approximately proportional to copper area) of the XIN and XOUT lines still matches that of the reference layout within 25%.
8 *		The crystal has sufficient accuracy and does not exceed the ±85ppm error budget for the sum of the following: Frequency or Calibration Tolerance @ +25°C Frequency Stability over the full operating temperature range Aging Stability (accounting for the desired life of the product)
9		The specified crystal has an ESR of ≤60Ω for C-band operation and ≤100Ω for A-band operation.
10		The crystal load capacitors (C18, C19 or C26, C27 of the reference design) have been chosen to match the selected crystal load capacitance rating, as defined in the reference design documentation (schematic and BOM).
11		The PL Smart Transceiver operating clock frequency has been verified to be sufficiently close to 10.0000MHz for C-band operation (6.5536MHz for A-band) such that after accounting for crystal and temperature variation, the total frequency deviation from nominal will not exceed ±200ppm.
12		The OOGAS pin has been connected to appropriate V_A voltage divider and bypass capacitor (R24, R25 and C28). If the device power supply is not an energy storage type, then the OOGAS pin may optionally be connected directly to VCORE, eliminating R24, R25 and C28. If the selected reference design uses the 2Ap-p transmit amplifier then the OOGAS pin should be connected directly to the VCORE (an energy storage power supply is not practical for use with the 2Ap-p amplifier).
13		The component values for the reference design circuitry have been selected for the proper band of operation (C-band or A-band).
14		The proper part is specified for Q1 of the reference design; either OnSemi BC857BDW1T1G, Philips BC857BS or Infineon BC857S.

15		The proper parts are specified for Q2 and Q3 of the reference design; OnSemi BC847B**P**DW1T1G and OnSemi BC847BDW1T1G respectively.
16		The proper transistors are specified for Q4 and Q5 of the reference design; Zetex FCX690B or STM 2STF1360 for Q4 and Zetex FCX790A or STM 2STF2360 for Q5 for the 1Ap-p transmit amplifier (Zetex ZXT690B and ZXT790A respectively for the 2Ap-p amplifier).
17		If the BIU, PKD, or TXON signals are connected to LEDs, the appropriate current limiting resistor has been included to limit the current to ≤12mA.
18		If BIU, PKD, or TXON are connected to LEDs and there is a creepage path of ≤1cm from user accessible points to the signal lines, then ESD protection diodes are included on these signal lines (and V_{DD5} bypass capacitors are also included directly adjacent to the protection diodes).
19		The ICTMode pin is tied to ground for PL 3120 and PL 3170 Smart Transceiver-based devices and pulled low through a 3kΩ to 5kΩ resistor for PL 3150 Smart Transceiver-based devices (allowing tri-state control of memory interface lines during in-circuit-test).
20		The CLKSEL pin of the Smart Transceiver is tied high.
21		Any device connected to the RESET~ pin of the Smart Transceiver has an open-drain (or equivalent) output.
22		If external devices are connected to the RESET~ pin, then a bypass capacitor(s) of 100pF to 1000pF are included on the RESET~ line within 15mm of the Smart Transceiver pin.
23		For PL 3150 Smart Transceiver-based devices, an LVI that stretches reset events to ≥10ms and has a threshold range of 4.5V to 4.75V, or tighter, has been specified (e.g., Maxim DS1813-5).
24		If an external oscillator is fed to the XIN pin of the Smart Transceiver (instead of connecting a crystal between the XIN and XOUT pins) then a power-on-pulse stretching LVI with a delay of ≥10ms is used.

Coupling Circuits (refer to Chapter 4)

25		Coupling circuit used is Example number _____
26		Capacitor C101 – Line coupling capacitor Proper value 10% (or better) tolerance Proper voltage rating (AC or DC as applicable) Safety listing, if applicable
27		Capacitor C102 – DC blocking capacitor 1uF value 10% (or better) tolerance Proper voltage rating Metallized film construction (required for surge immunity)
28		Capacitor C103 – V_A filter capacitor Proper value 20% (or better) tolerance Proper voltage rating Proper ESR @100kHz/20C Proper ripple current rating at 105C
29		Diode D101 – V_A clamp diode Current Rating ≥1A Reverse breakdown ≥50V Proper forward voltage @1A/25C Surge current ≥30A for 8.3ms Proper reverse recovery Reverse current ≤100uA@100C Typical capacitance ≤40pF@4V

30		Diode D102 – Ground clamp diode Current Rating ≥1A Reverse breakdown ≥50V Forward voltage ≤1.0V@1A/25C Surge current ≥30A for 8.3ms Reverse recovery ≤25ns Reverse current ≤100uA@100C Typical capacitance ≤40pF@4V
31 *		Fuse F101 – Line fuse 6A or 6.3A rating (or higher if in accordance with varistor vendor recommendations) Proper voltage rating Time-lag (slow-blow type)
32		Inductor L101 – Shunt coupling inductor (for a non-transformer isolated coupling circuit) 1.0mH value 10% (or better) tolerance DC current rating ≥30mA DC resistance ≤14Ω
33		Inductor L102 – Series coupling inductor (if applicable) Proper value 10% (or better) tolerance Proper DC current rating Proper DC resistance If toroidal or shielded inductor is used a current rating 2 to 3 times higher than listed in the component table for this inductor is used.
34 *		Inductor L103 – RXCOMP inductor Proper value 10% (or better) tolerance DC current rating ≥30mA DC resistance ≤55Ω 1kHz≤ Test Frequency ≤400kHz
35		Resistor R101 – Safety discharge resistor Proper value Proper voltage rating Proper power rating for hi-pot test (if applicable)
36		PROTECT circuit If varistor used: Proper AC or DC voltage rating Proper surge current rating for 8x20µs for 2 times No varistor to earth unless hi-pot testing is performed prior to insertion of varistor and ground leakage current is not an issue. If gas-discharge tube used place on line side of fuse
37		Transformer T101 (for a transformer isolated coupling circuit) Transformer with correct specifications is selected (see Appendix C)
38		No filters or power supply transformers are in the coupling circuit path. If a ferrite bead is in the coupling circuit path it is either common mode connected (see Chapter 6) or has been verified to be <0.5Ω @100kHz.
39		L101 and L103 are spaced >1cm apart (for a non-transformer isolated coupling circuit)
40		Circuit board traces between the output of the transmit amplifier and the AC mains are ≥1.3mm wide and ≤15cm long.

41		The signal return traces from the AC mains connection to the transmit amplifier are a copper plane or ≥1.3mm wide and ≤15cm long (before becoming a ground plane).
42		Traces from the point where D101 taps into the signal path to the point where C103 connects back to ground are ≥1.3mm wide and ≤2cm long.
43		The traces between the V_A input of the transmit amplifier and the point where C103 connects back to ground are at least 1.3mm wide and no more than 4cm long.
44		Surge testing has been performed in accordance with applicable surge standards and the application requirements.

Power Supply (refer to Chapter 5)

45		Type of V_A power supply (from Table 5.4, or if some other type is used provide a text description): _____ Type of V_{DD5} power supply: _____ _____ If traditional linear supplies are used for both V_A and V_{DD5}, then skip check list items 46, 47, and 49 - 55. If either supply contains switching elements, then complete this section in its entirety.
46		If a the selected power supply is one of the "Pre-Verified" type from Table 5.4, then check that it matches the documentation for that supply in Chapter 5 - noting any deviations.
47		If the selected reference design uses a 1Ap-p transmit amplifier, verify that the V_A power supply operates in the range of 8.5V to 18.0V during receive mode and 10.8V to 18.0V during transmit mode (refer to Chapter 5).
48		If the selected reference design uses a 2Ap-p transmit amplifier, verify that the V_A power supply operates in the range of 12.0V to 18.0V during receive mode, 14.25V to 18.0V for C-band transmit mode and 12.0V to 18.0V for A-band transmit mode (refer to Chapter 5).
49 *		Switching supplies operate in the recommended frequency ranges of 46kHz - 55kHz, or 90kHz - 110kHz, or >155kHz under all line, load, environmental, and volume production variations.
50		A series inductor is used between the power supply input and the power mains to avoid attenuation due to the input stage of a switching power supply.
51		The value of the series inductor has been selected according to the application requirements of Table 5.9.
52		The series power supply inductor has a current rating adequate to support the peak currents drawn by the power supply without saturation.
53		The resonant frequency of the LC circuit created by the inductor and the input capacitance of the switching supply is at least 1 octave from the communication frequency range (70kHz-90kHz for A-band and 110kHz-138kHz for C-band).
54		The power supply complies with the input noise masks shown in Chapter 5. Measurement of the power supply was made by connecting the supply to the artificial mains network as specified in sub clause 8.2.1 of *CISPR Publication 16*. Measurements are made over the full range of anticipated loads on the supply and conducted in accordance with the CENELEC EN 50065-1 or FCC measurement standards with measurement bandwidths of 200Hz below 150kHz and 9kHz above 150kHz, as described in *CISPR Publication 16*.
55		If the power supply does not meet the appropriate noise mask, an appropriate filter is installed between the local switching power supply and the power line (refer to Chapter 5).

56		The output noise masks shown in Chapter 5 are satisfied using measurements taken over the full range of anticipated loads.

Design and Test for Electromagnetic Compatibility (refer to Chapter 6)

57		Product enclosure is made from the following material(s) _____ Method of ESD mitigation is _____ A) The product is sealed to prevent static discharges from reaching sensitive circuitry. B) A path is provided for ESD currents to be shunted around sensitive circuitry.
58		There are no traces running through the reference layout area that are not associated with the reference circuitry.
59		Digital or clock signals outside the reference layout area are >2mm from critical nets TXOUT, RXIN, RXCOMP, TX2, TX3, XIN and XOUT, assuming an intervening guard ground (>10mm if there is no intervening guard ground).
60		Conducted emissions testing was performed using a 50Ω//(50μH+5Ω) Line Impedance Stabilization Network (LISN) as specified in *CISPR Publication 16*.
61		For conducted emission measurements a Rohde and Schwarz R&S EZ-25 150kHz high-pass filter (or equivalent) was used between the LISN and the measuring receiver.
62		For conducted emissions testing the appropriate attenuator is used to ensure that the transceiver's transmit signal does not overload the measuring instrument.
63		The residual noise floor of the entire conducted emissions measurement setup has been verified to be at least 10dB below the specification limit (i.e., a noise floor less than 38dBμV for FCC measurements, and a noise floor less than 36dBμV for CENELEC EN 50065-1 measurements).
64		Proper quasi-peak and average detectors in compliance with *CISPR Publication 16* are used for conducted emissions testing (although measurements with a peak detector are common, the limits specified by FCC Section 15.107 and by CENELEC EN 50065-1 are for quasi-peak and average detectors only).
65		Testing of conducted emissions is preformed with the proper bandwidth filters of 200Hz for frequencies below 150kHz and 9kHz for frequencies above 150kHz.
66		Compliance with the appropriate conducted emissions regulation was verified in accordance with checklist items 60 through 65.
67		If capacitors are added from line to neutral for EMI suppression these capacitors meet the requirements of Table 6.1.
68		For products designed to prevent static discharges from reaching sensitive circuitry by means of a sealed enclosure, the creepage path from all points of entry to any internal conductive elements is ≥1cm.
69		User accessible circuitry with <1cm creepage path to conductive elements have explicit diode clamping to shunt ESD currents from that circuitry to earth ground using a path that does not pass through sensitive circuitry (including the PL Smart Transceiver Reference circuitry).
70		The circuit design includes dedicated 0.1μF V_{DD5} bypass capacitor(s) mounted directly adjacent to each group of ESD protection diodes.
71		Compliance with *IEC 61000-4-2 Electromagnetic Compatibility, Part4: Testing and measurement techniques – Section 2 Electrostatic discharge immunity test* has been verified.

Communication Performance Verification (refer to Chapter 7)

72		Compliance with the communication performance verification requirements of Chapter 7 has been verified.

PL Smart Transceiver Programming (refer to Chapter 8)

73		The correct standard transceiver type is defined for the transceiver by way of NodeBuilder 3.1, Mini EVK 1, or newer: 1. A-band Power management disabled: PL-20A Power management enabled: PL-20A-LOW 2. C-band Power management disabled: CENELEC disabled: PL-20N CENELEC enabled: PL-20C Power management enabled: CENELEC disabled: PL-20N-LOW CENELEC enabled: PL-20C-LOW

*** Items marked in bold with an asterisk (2, 4, 5, 7, 8, 31, 34, and 49) indicate the most frequently missed items.**

C

Isolation Transformer Specifications

12μH-Leakage Transformer Specifications

Schematic

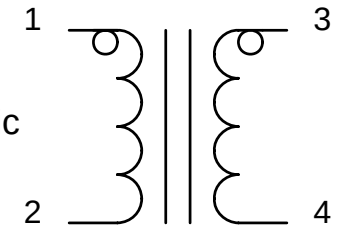


Table C.1 12μH-Leakage Transformer Electrical Specifications

Parameter	Min	Typ	Max	Units
Turns Ratio (1-2):(3-4)		1.0		
DC Resistance 1-2, 3-4			0.20	ohm
Magnetizing Inductance 1-2 Dry, @100kHz, $1V_{RMS}$	0.75	1.0	1.25	mH
Magnetizing Inductance 1-2, Wet, @100kHz, $1V_{RMS}$, plus 15mADC	0.75			mH
Leakage Inductance 1-2 (3-4 shorted) @100kHz, $1V_{RMS}$	10.8	12.0	13.2	μH
Winding Capacitance 1-2			30	pF
Winding-to-Winding Capacitance 1-2 shorted to 3-4 shorted			30	pF

Contact vendors for mechanical information, temperature ranges, safety agency compliance, and pricing information.

Table C.2 12μH-Leakage Transformer Vendors and Part Numbers

Vendor	Vendor website	Part Number(s)
EXCEL Electric Corporation	www.excelelectriccorp.com	EXL-324
Precision Components, Inc	www.pcitransformers.com	0505-0671, 0505-0671FG
Tamura Corporation	www.tamuracorp.com	PLP01UE
Transtek Magnetics	www.transtekmagnetics.com	TMS80079CT
Tyco Electronics	www.tycoelectronics.com	MGCD0-00008

Low-Leakage Transformer Specifications

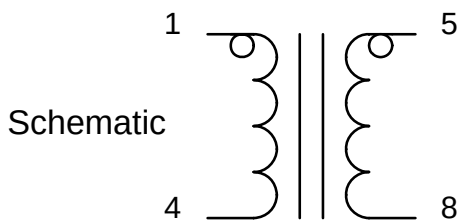


Table C.3 Low-Leakage Transformer Electrical Specifications

Parameter	Min	Typ	Max	Units
Turns Ratio (1-4):(5-8)		1.0		
DC Resistance 1-4, 5-8			0.35	ohm
Magnetizing Inductance 1-4 Dry, @100kHz, $1V_{RMS}$	0.75	1.45	1.8	mH
Magnetizing Inductance 1-4, Wet, @100kHz, $1V_{RMS}$, plus 30mADC	0.75			mH
Leakage Inductance 1-4 (3-4 shorted) @100kHz, $1V_{RMS}$			1.0	µH
Winding Capacitance 1-4			25	pF
Winding-to-Winding Capacitance 1-4 shorted to 5-8 shorted			50	pF

Contact vendors for mechanical information, temperature ranges, safety agency compliance, and pricing of their parts listed below.

Table C.4 Low-Leakage Transformer Vendors and Part Numbers

Vendor	Vendor website	Part Number
Precision Components, Inc.	www.pcitransformers.com	0505-0821G
Tyco Electronics	www.tycoelectronics.com	MGCD0-00011

D

Manufacturing Test and Handling Guidelines

Production Test Guidelines

This appendix describes recommended production test procedures that can be used to verify the communication functionality of each PL Smart Transceiver-based device. The production test procedure described below is applicable for PL Smart Transceiver-based devices operating in either the A or C bands.

Physical Layer Production Test

Production Test Strategy

The production test strategy described in this document is not intended as a design verification test. It is assumed that compliance with the device checklist of Appendix B and communication performance verification in accordance with Chapter 7 have been fully verified for the product design. Rather, the production test is designed to:

- Identify devices with manufacturing defects in components surrounding the PL Smart Transceivers.
- Identify component substitutions, made over the course of high volume manufacturing that inadvertently impair power line communication performance by a significant amount. Such detection is not meant to replace re-qualification of the product design after component substitution, which should be considered a mandatory process.

In-Circuit Test (ICT)

The basis for the physical layer performance verification test is the assumption of 100% ICT of the printed circuit board (PCB) for the Unit Under Test (UUT) prior to production functional test. All passive components are to be tested to the accuracy of the ICT equipment, all transistor diode junctions and betas should be tested, all ICs should have solder junctions verified via input diode tests, and all PCB traces should be verified for continuity and lack of short circuit conditions. The PCB reference layouts supplied with the PL Smart Transceiver Development Support Kit (DSK) all include test points to allow 100% ICT coverage.

Any deviation from 100% ICT coverage will require an extended physical layer test different from the one described in this document.

The RESET~ pin of the PL Smart Transceiver should be grounded during ICT. This will prevent the chip from performing an initial boot sequence. An initial boot should only be allowed when the integrity of the V_{DD5} supply and RESET~ signal can be assured for the entire boot sequence. See Chapter 2 for details of the boot process and timing.

Transmitter Performance Verification

Transmitter performance is verified by causing the unit under test to transmit a packet into a low impedance load (approximately 5 ohms), and then verifying that an acceptable amplitude signal is produced.

Initiating a Packet Transmission

A simple way of causing the PL Smart Transceiver-based device to transmit a packet is to communicate with it over the power mains connection using a standard network management command. For instance, if a Query ID message is sent to the UUT the PL Smart Transceiver will respond with an "ID Response" message over the mains connection. This approach always works if the PL Smart Transceiver is an un-configured state and authentication is not enabled. If the UUT is in a configured state and has authentication enabled an alternate method of initiating a packet must be used.

Measurement Time Window

The ID Response message consists of a preamble followed by the unique 48 bit Neuron ID (NID) that was programmed into the PL Smart Transceiver when it was manufactured. Because each NID is unique, the RMS voltage of the transmit signal from the PL Smart Transceiver will vary from unit to unit when averaged over the entire transmitted packet. In order to provide a reproducible test, the transmit signal amplitude (V_{RMS}) of the UUT should only be measured during the initial preamble of the ID Response message. The preamble spans the first 35 bit times of the ID Response message. The first 35 bit times of the packet will be identical for all UUTs, independent of their unique NID.

The duration of the first 35 bit times varies depending on whether the product is operating in C-band or A-band as follows:

C-band 35 bit times = 6.36ms
A-band 35 bit times = 9.70ms

Transmit Signal Amplitude

While transmitting into the ~5Ω load (described later in this chapter), the PL Smart Transceiver should produce an output signal of approximately $1V_{RMS}$ during the first 35 bit times of the service pin message (see Table D.1 for suggested test limits). The suggested test limits allow for normal production variability and should not have any further guard band added.

Receiver Performance Verification

Receiver performance is verified by sending a highly attenuated message to the UUT and verifying that the device responds to that message. The attenuated message is transmitted from an appropriate D/A card (such as the National Instruments PXI-6070E) using a waveform file supplied by Echelon. The response by the UUT to the attenuated message can be used for transmitter performance verification. It is not necessary to validate the contents of the response packet. The fact that the response packet was transmitted by the UUT indicates that the attenuated message was correctly received.

In order to have reasonable assurance that the UUT can receive packets with acceptable sensitivity, the receive test message is attenuated by approximately 70dB using the interface circuit described below (where attenuation = $20\log_{10}(Vin/Vout)$).

A/D, D/A- based Test System

This section describes a practical test system that can perform both transmit and receive performance verification.

Hardware Description

The test system should have the following components.

- Data acquisition hardware
- Test interface board

Data Acquisition Hardware

- A 12-bit A/D channel with a throughput of at least 1 Ms/s that is configured for single ended reference and ±10V range
- A 12-bit D/A channel with a throughput of at least 1Ms/s that is configured for ±10V range
- Data acquisition channels that have an external trigger capability

National Instruments multi-function cards, such as PXI-6070E or PCI-MIO-16E-1, are examples of data acquisition hardware that meet the requirements for the test system.

Test Interface Board

A custom interface board needs to be designed that provides 70dB attenuation, a ~5 ohm load, a coupling circuit, and a peak detector circuit that triggers on the UUT transmitted packets. Figure D.1 is a diagram of circuitry that provides the required interface functions.

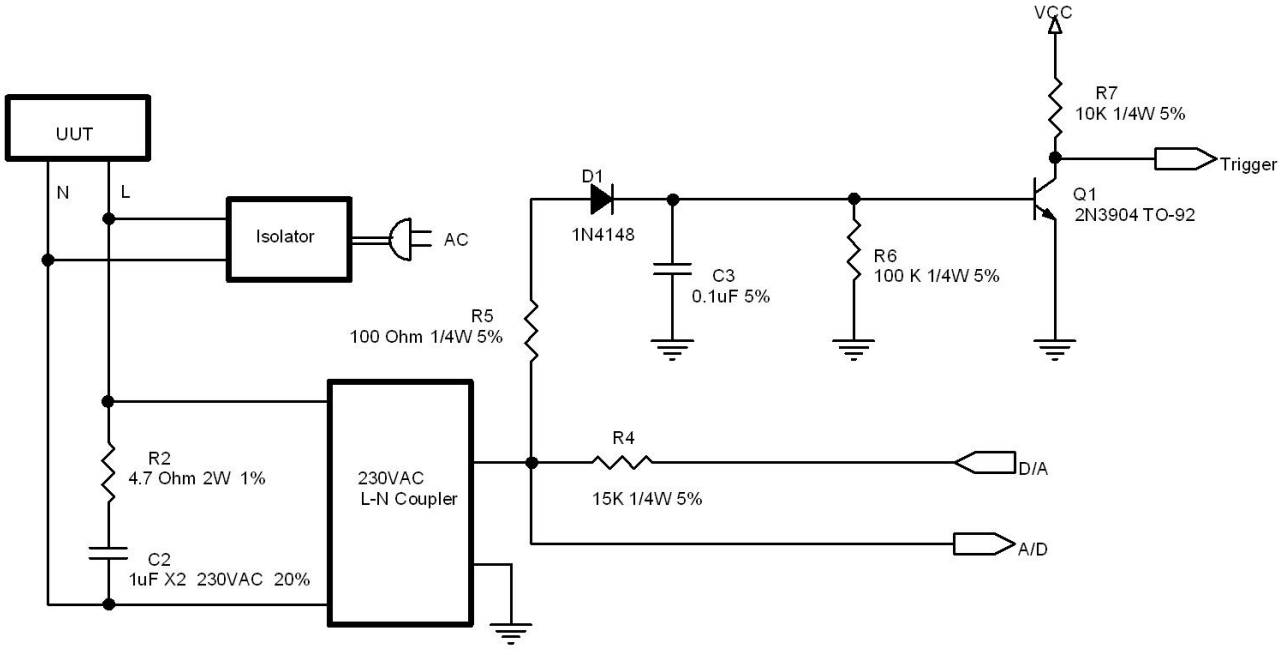


Figure D.1 Test Interface Board

The interface board performs three functions:

- The 4.7 ohm resistor in series with the 1uF X2 capacitor provides a low impedance load for the transmit level verification test.
- The 15k ohm resistor, in conjunction with the 4.7 ohm resistor and 1uF X2 capacitor, provide approximately 70dB of attenuation of the message generated by the D/A converter as part of the receive mode test.
- The 1N4148 diode, 0.1uF capacitor, 100k ohm resistor, 100 ohm resistor, and 2N3904 transistor provide a peak detect function to trigger the A/D converter when a packet is transmitted by the UUT in response to the message generated by the D/A converter.

A circuit, such as the one in Figure 7.1 of Chapter 7, should be used for the block in Figure D1 labeled "Isolation". A Line-to-Neutral coupler such as Echelon model number 78200-221 should be used for the block in the figure labeled "230VAC L-N Coupler".

Software Description

Input file

A file containing either the C-band or A-band waveform that represents the Query ID broadcast message should be used as an input to the software. The data file represents amplitude in volts while the interval between data points is 1µs. Any unconfigured device with a PL Smart Transceiver will respond to the appropriate waveform by transmitting its Neuron ID. The files are available as a free download from the Echelon Web site (go to www.echelon.com/downloads and select the **Transceivers** category).

Test process

1. Read the waveform data into a buffer called `waveform[]`.
2. Scale the waveform by applying proper gain and offset to produce a 7V p-p waveform prior to the attenuation circuit. The waveform should be centered on zero volts.
3. Prepare the A/D channel to be ready for capturing the response of the UUT upon receiving a trigger signal from the interface board.
4. Output the `waveform[]` signal to the UUT through the A/D channel.
5. When the UUT receives the signal, it will respond with a message that contains the Neuron ID. This will take place within a few hundred milliseconds.
6. Capture the response and calculate the RMS voltage over the first 35 bits. The measurement window should be 6.36ms for C-band and 9.7ms for A-band.

The test limit for the RMS voltage depends on the transceiver channel type and amplifier type of the UUT. The table below lists recommended limits.

Table D.1 Test Limits of Different Transceiver Types

UUT Transceiver and Amplifier Type	V_{RMS}
C-band 7V p-p/1A	0.8 (0.65 for 1-phase L-E coupling)
C-band 10V p-p/2A	1.3
A-band 7V p-p/1A	0.8
A-band 8V p-p/2A	1.2

Figure D.2 shows a complete test cycle with respect to transmit, receive, and trigger signals (the signal levels and timings in the figure are ***not to scale*** but are meant to illustrate the measurement concepts).

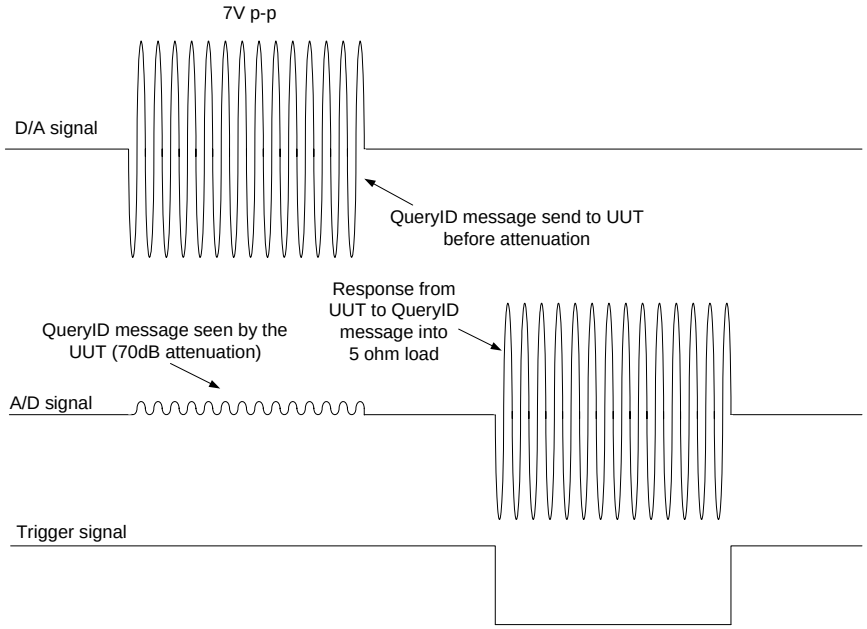


Figure D.2 Test Cycle Waveforms

Notes on Missed Messages

Due to the adaptive sensitivity algorithms inside the PL Smart Transceiver, it is statistically possible for a good transceiver to miss a single packet. Therefore the test should be repeated two more times if the initial test fails. If the test passes in two out of three tries then the UUT is good. If the UUT passes in only one out of three times then the UUT should be considered marginal and should be verified by way of the procedure in Chapter 7. A UUT that fails three or more tests is defective.

Test System Verification

This section is intended to describe a verification procedure that should be performed on the production test system in order to ensure repeatability of the power line physical layer test. The procedure includes:

- Verification of background noise in the test system
- Verification of Query ID message amplitude

Verification of Background Noise

One of the functions of the test system isolator is to prevent noise from the power mains from disturbing the test results. The test system is designed to transmit a Query ID message that has been attenuated by approximately 70dB. The amplitude of the 70dB-attenuated message should be about 2mVp-p. In order to consistently test that UUTs can receive this low level signal, the background noise of the test system must be at least 6-9 dB lower than the attenuated message. It is important to note that only noise at or near the PL Smart Transceiver's communication frequencies affect the reproducibility of the test. The power line isolator is designed to filter noise in the PL Smart Transceivers communication frequency range. The isolator does not, however, filter low frequency noise to a level that is 80dB below the PL Smart Transceiver's transmit level. In fact it is not uncommon to observe low frequency noise on the order of 1Vp-p passing through the isolator. A consequence of this fact is that the background noise level must be measured with a frequency-selective instrument.

The simplest method of verifying the test system background noise is to connect one PLCA-22 Power Line Communications Analyzer, Echelon Model 58022, to the UUT port of the test system. The PLCA-22 can be used to monitor the noise level via its signal strength bar graph LED. The signal strength meter displays the mains signal level after being filtered by the transceiver's internal digital signal processing. Thus the meter displays only the noise that will affect the PL Smart Transceiver. The background noise should read no higher than –78dB on the PLCA-22 bar-graph meter. That is, at most, only the –78dB LED on the signal strength meter should be illuminated. If additional LEDs are illuminated then the isolator should be tested as described in Chapter 7.

Verification of Query ID Message Amplitude

The amplitude of the attenuated Query ID message should be about 2mVp-p and as described in the *Verification of Background Noise* section, however, there will be low frequency noise present on the mains that will be much larger in amplitude. The consequence of this fact is that it is not practical to make a direct measurement of the attenuated message using a wide band instrument such as an oscilloscope. It will be very difficult to trigger on the packet given the noise present. The solution, once again, is to use a frequency-selective instrument.

The PLCA-22 can be used to verify the attenuation of the Query ID message using the unit's signal strength meter. The UUT must be disconnected from the test system so that only the Query ID message is observed and not the response to the Query ID message from the UUT. Simply run the production test with the UUT disconnected and monitor the signal strength LEDs on the PLCA-22. The LEDs up to and including the –72dB LED should illuminate when the Query ID is transmitted. If more LEDs illuminate (for example, if the –66dB LED illuminates) this indicates that the attenuation circuit is not operating properly. The key elements to verify are the 4.7 ohm resistor (R2) and the 15k ohm resistor (R4).

Manufacturing Handling Guidelines

The following section provides manufacturing guidelines regarding both soldering and handling of the PL Smart Transceivers.

Board Soldering Considerations

All PL Smart Transceiver chips have an IPC/JEDEC Standard J-STD-020C Level 3 Classification. This means that the parts have a 168-hour floor life once the parts have been removed from the moisture barrier bag (at ≤30ºC and ≤60% R.H.). To prevent *pop-corning* during reflow, parts removed from the moisture barrier protection must be reflow soldered within 168 hours. If they are not, then they must be drybaked. If drybaking is required, the parts should be baked for 24 hours at 125ºC, or as required per IPC/JEDEC J-STD-033A. The tubes and reels that the PL 3120 and PL 3170 Smart Transceivers are shipped in will not withstand the drybake. The trays that the PL 3150 Smart Transceiver is shipped in will withstand a drybake of up to 125ºC.

The PL 3120, PL 3150, and PL 3170 Smart Transceiver ICs comply with the European Union Restriction of Hazardous Substances (RoHS). The maximum peak temperature for PL Smart Transceivers is 260ºC. Consult the solder manufacturer's datasheet for recommendations on optimum reflow profile. The actual reflow profile chosen should consider the peak temperature limitation noted above.

The parts should, if possible, be handled only with properly calibrated mechanical pick and place equipment. Handling the parts manually increases the risk that the leads will become bent. Bent leads can result in open or short circuit connections during the board-level assembly process.

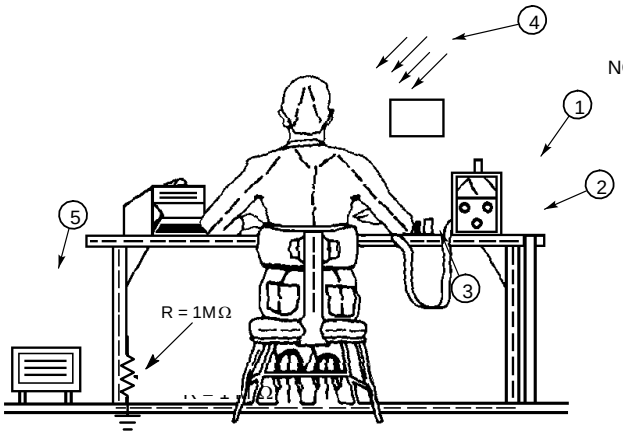
Handling Precautions and Electrostatic Discharge

All CMOS devices have an insulated gate that is subject to voltage breakdown. The gate oxide for the PL Smart Transceiver breaks down at a gate-source potential of about 10V. The high-impedance gates on the PL Smart Transceiver are protected by on-chip networks. However, these on-chip networks do not make the IC immune to ESD. Laboratory tests show that devices can fail after one very high voltage discharge. They can also fail due to the cumulative effect of several lower potential discharges.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is shorted to V_{DD5}, shorted to GND, or is open-circuit. As a result of this, the device will no longer function. Less severe cases are more difficult to detect because they can cause intermittent failures or degraded performance. Static damage often increases leakage currents.

All CMOS devices are susceptible to large static voltage discharges that can be generated while handling. Static voltages generated by a person walking across a waxed floor, for example, have been measured in the range of 4kV – 15kV (depending on humidity, surface conditions, etc.). Therefore the following general precautions should be followed when handling CMOS devices such as the PL Smart Transceiver.

- Do not exceed the maximum ratings specified in the data sheet.
- All unused digital device input pins should be connected to V_{DD5} or GND.
- All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
- A circuit board containing CMOS devices is merely an extension of the device and the same handling precautions apply to that board. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the value of the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and is brought into contact with static-generating materials.
- All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic “snow,” Styrofoam®, or plastic trays. Devices should be left in their original container until ready for use.
- All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure D.3.
- Nylon or other static-generating materials should not come in contact with CMOS circuits.
- If automatic handling equipment is being used, high levels of static electricity can be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
- Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material, or soldered onto a PCB.
- When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.



NOTES:

1. 1/16 inch conductive sheet stock covering bench-top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside a building to be less than outside humidity.

Figure D.3 Typical Manufacturing Work Station

Wave-solder Operations

The following steps should be observed during wave-solder operations.

- The solder pot and conductive conveyor system of the wave-soldering machine must be grounded to an earth ground.
- The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
- Operators must comply with precautions previously explained.
- Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

Board Cleaning Operations

The following steps should be observed during board cleaning operations.

- Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
- Brush or spray cleaning should not be used.
- Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
- Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
- High-velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
- The use of static-detection meters for line surveillance is highly recommended.
- Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
- Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing to be certain there are no voltage transients present.
- Double-check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.
- Do not reuse shipping rails. Continuous use causes deterioration of their antistatic coating.
- Wrist straps and equipment logs should be maintained and audited on a regular basis. Malfunctioning wrist straps can go unnoticed and as equipment is occasionally moved ground connections may inadvertently be forgotten.

E

References

This appendix provides a list of the reference material used in the preparation of this manual.

[1] 47CFR15, Subpart B (Unintentional Radiators), *U.S. Code of Federal Regulations.*

[2] *CENELEC EN 50065-1:2001 "Signaling on low-voltage electrical installations in the frequency range 3kHz to 148.5kHz" Part 1 "General requirements, frequency bands and electromagnetic disturbances".*

[3] *CISPR 16, All Parts, Specification for radio disturbance and immunity measuring apparatus and methods*, International Electrotechnical Commission.

[4] *IEC 61000-4-2 Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques-Electrostatic discharge immunity test*, International Electrotechnical Commission.

[5] *IEC 61000-4-3 Electromagnetic compatibility (EMC) – Part 4-3: Testing and measurement techniques -Radiated, radio-frequency, electromagnetic field immunity test*, International Electrotechnical Commission.

[6] *IEC 61000-4-4 Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test*, International Electrotechnical Commission.

[7] *IEC 61000-4-5 Electromagnetic compatibility (EMC) – Part 4-5: Testing and measurement techniques - Surge immunity test*, International Electrotechnical Commission.

[8] *IEEE Std C62.41.1™ – 2002, IEEE Guide on the Surge Environment in Low-Voltage (1000V and Less) AC Power Circuits.*

[9] *IEEE Std C62.41.2™ – 2002, IEEE Recommended Practice on Characterization of Surges in Low-Voltage (1000V and Less) AC Power Circuits.*

[10] *IEEE Std C62.45™ – 2002, IEEE Recommended Practice on Surge Testing for Equipment Connected to Low-Voltage (1000V and Less) AC Power Circuits.*

[11] *Noise Reduction Techniques in Electronic Systems*, 2nd ed., by Henry W. Ott, John Wiley & Sons, 1988.