

NP50P04SLG

-40V – -50A – P-channel Power MOS FET

R07DS0241EJ0101

Application : Automotive

Rev.1.01

May. 20, 2022

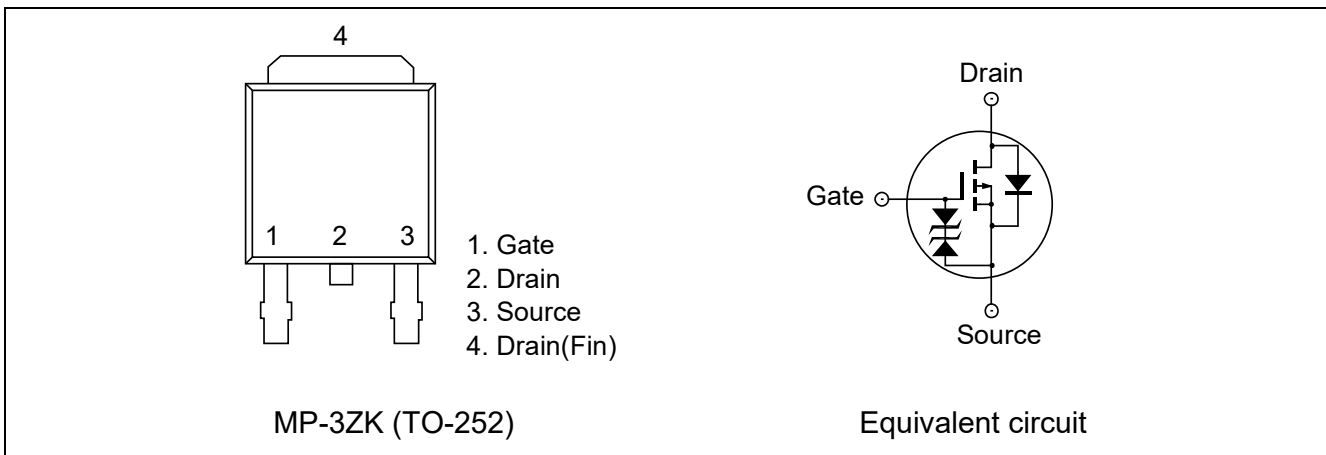
Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance : $R_{DS(on)} = 9.6 \text{ m}\Omega \text{ Max.}$ ($V_{GS} = -10 \text{ V}$, $I_D = -25 \text{ A}$)
 $R_{DS(on)} = 15 \text{ m}\Omega \text{ Max.}$ ($V_{GS} = -4.5 \text{ V}$, $I_D = -25 \text{ A}$)
- Low input capacitance : $C_{iss} = 3800 \text{ pF Typ.}$
- Built-in gate protection diode
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

Outline



Absolute Maximum Ratings

($T_a=25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC) ($T_c = 25^\circ\text{C}$)	$I_{D(DC)}$	∓ 50	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes1	∓ 150	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	84	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 175	$^\circ\text{C}$
Single Avalanche Current	I_{AS} Notes2	37	A
Single Avalanche Energy	E_{AS} Notes2	136	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch}=25^\circ\text{C}$, $V_{DD} = -20\text{V}$, $R_G = 25 \Omega$, $V_{GS} = -20 \rightarrow 0\text{V}$, $L = 100\mu\text{H}$

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-c)}$ ^{Notes3}	1.78	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ ^{Notes3}	125	°C/W

Electrical Characteristics

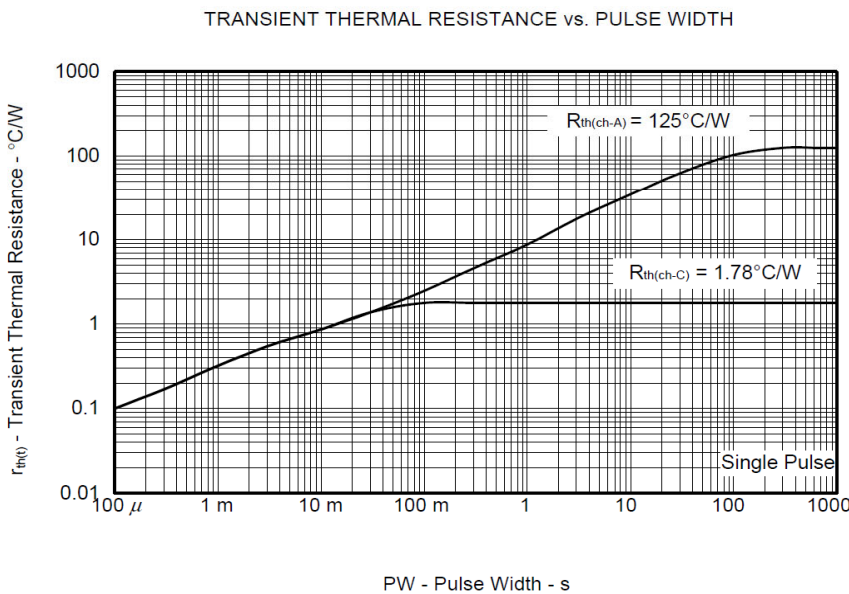
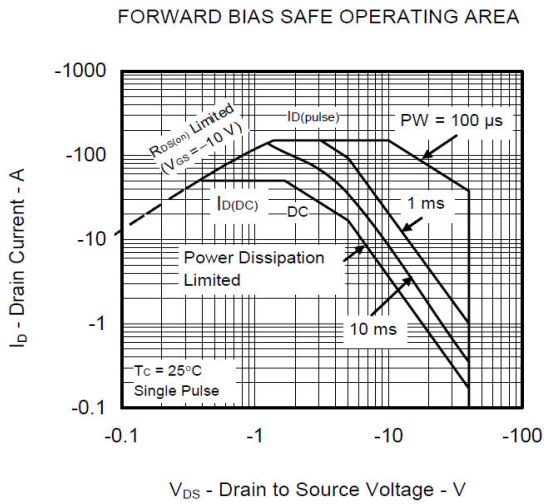
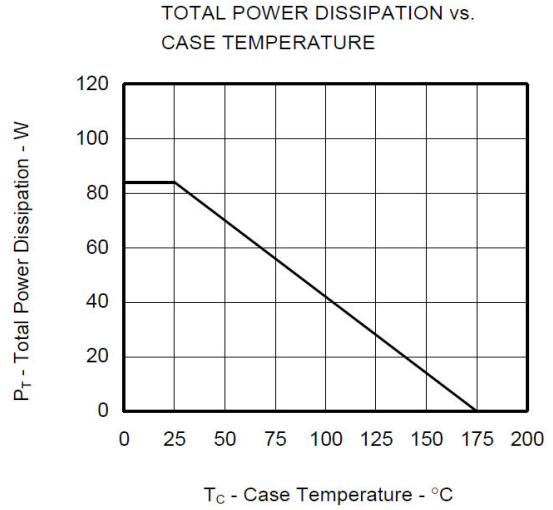
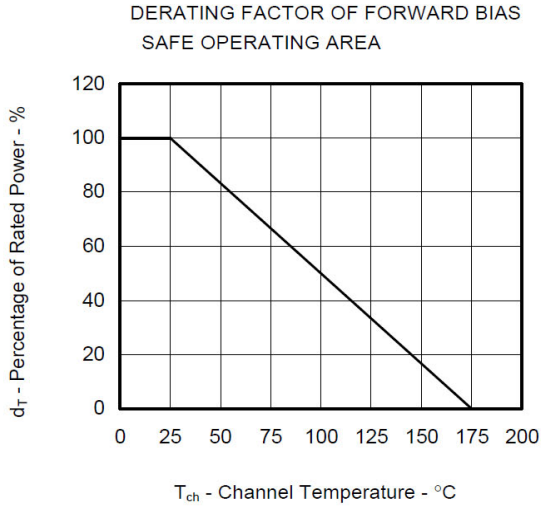
(T_a=25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V _{DS} = -40 V, V _{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±10	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	-1.0	-1.4	-2.5	V	V _{DS} = V _{GS} , I _D = -250 μA
Forward Transfer Admittance	y _{fs} ^{Notes4}	12	44	—	S	V _{DS} = -10 V, I _D = -25 A
Drain to Source On-state Resistance	$R_{DS(on)1}$ ^{Notes4}	—	8.2	9.6	mΩ	V _{GS} = -10 V, I _D = -25 A
	$R_{DS(on)2}$ ^{Notes4}	—	9.8	15	mΩ	V _{GS} = -4.5 V, I _D = -25 A
Input Capacitance	C _{iSS} ^{Notes3}	—	3800	5700	pF	V _{DS} = -10 V
Output Capacitance	C _{oss} ^{Notes3}	—	740	1120	pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rSS} ^{Notes3}	—	500	905	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)} ^{Notes3}	—	11	24	ns	V _{DD} = -20 V
Rise Time	t _r ^{Notes3}	—	15	39	ns	I _D = -25 A
Turn-off Delay Time	t _{d(off)} ^{Notes3}	—	250	505	ns	V _{GS} = -10 V
Fall Time	t _f ^{Notes3}	—	150	380	ns	R _G = 0 Ω
Total Gate Charge	Q _g ^{Notes3}	—	100	150	nC	V _{DD} = -32 V
Gate to Source Charge	Q _{gs}	—	13	—	nC	V _{GS} = -10 V
Gate to Drain Charge	Q _{gd}	—	30	—	nC	I _D = -50 A
Body Diode Forward Voltage	V _{F(S-D)} ^{Notes4}	—	0.96	1.5	V	I _F = -50 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	50	—	ns	I _F = -50 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	—	63	—	nC	di/dt = -100 A/μs

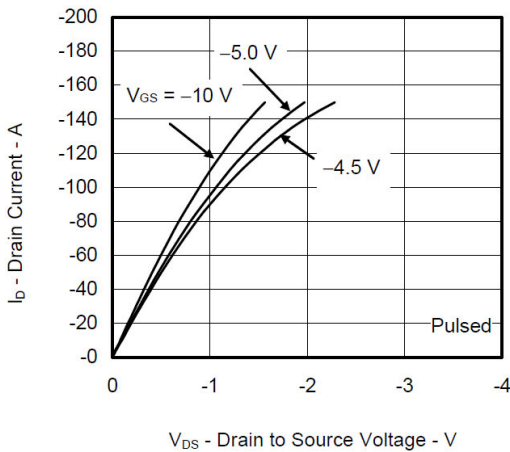
Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

4. Pulse test.

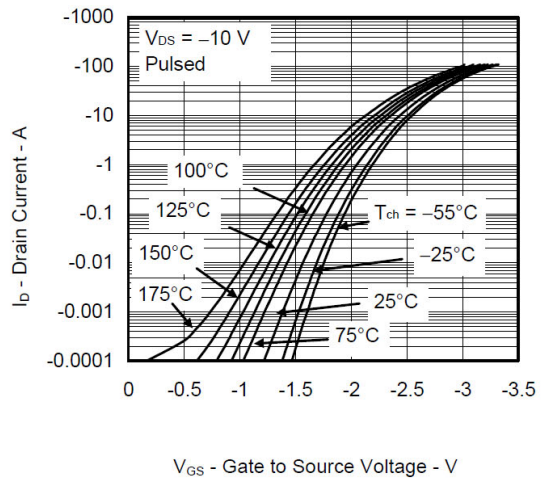
Typical Characteristics



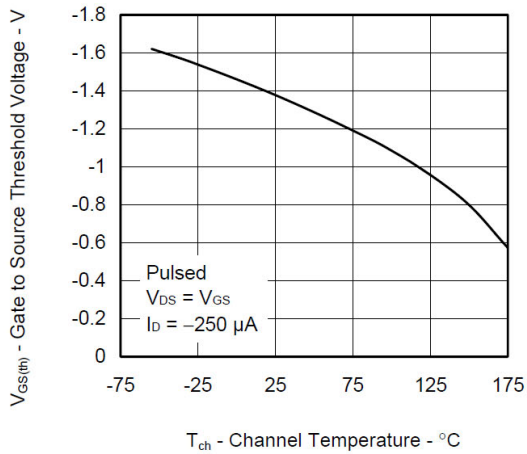
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



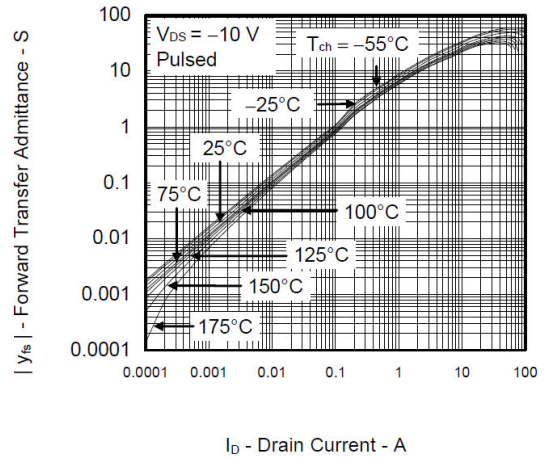
FORWARD TRANSFER CHARACTERISTICS



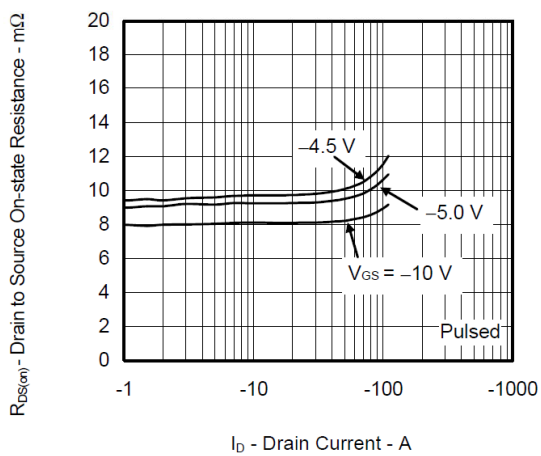
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



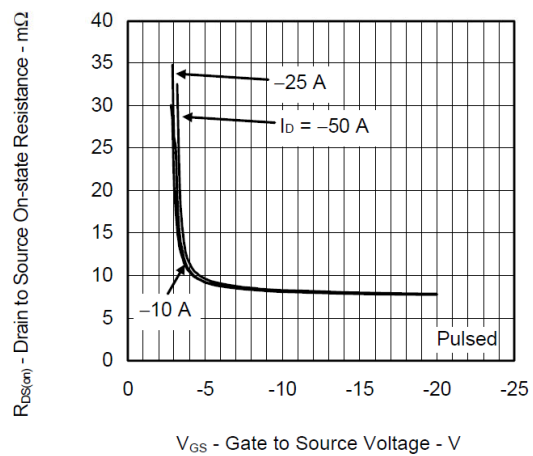
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



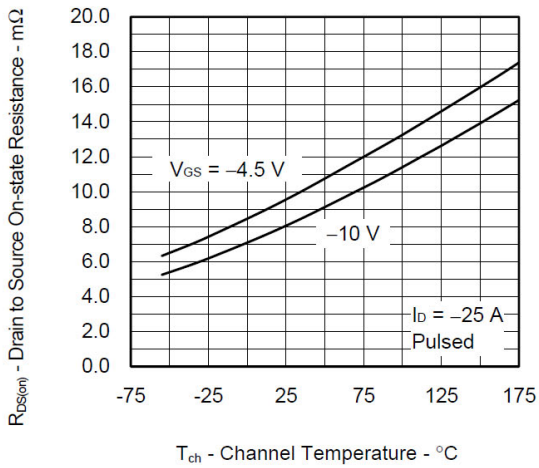
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



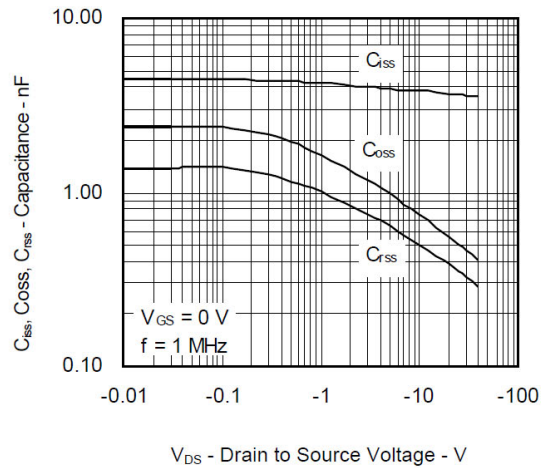
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



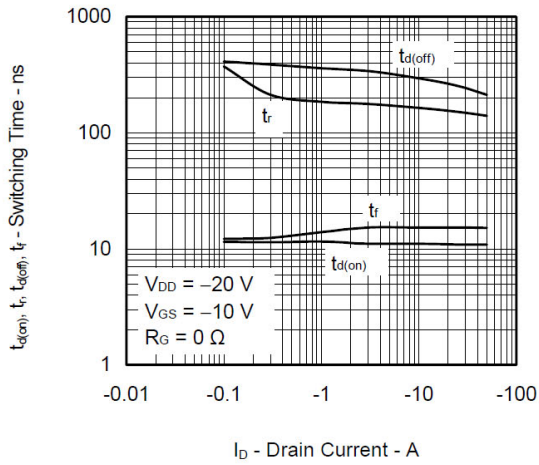
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



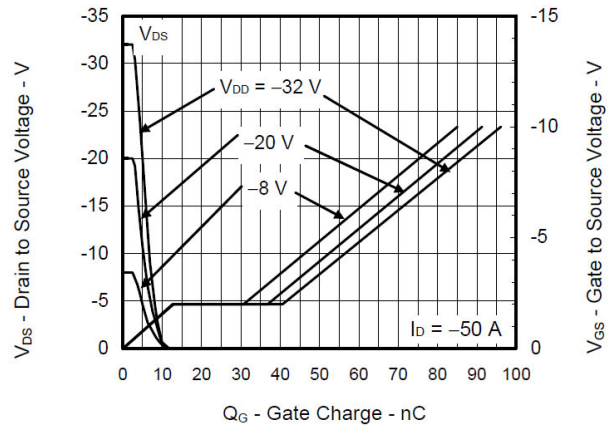
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



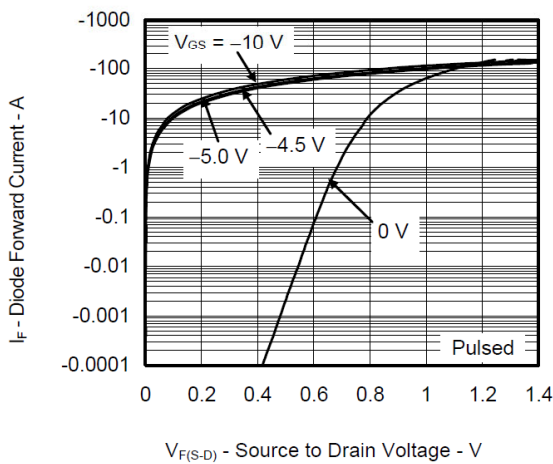
SWITCHING CHARACTERISTICS



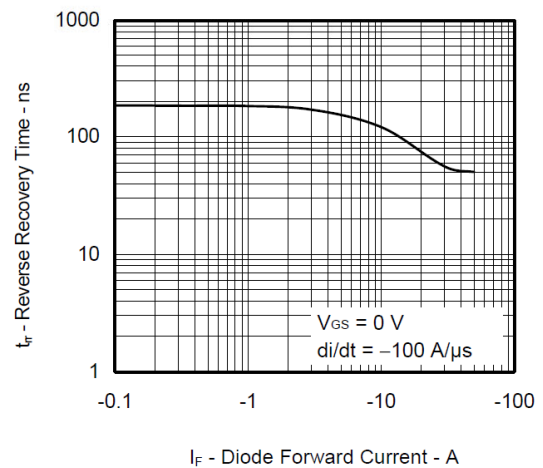
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



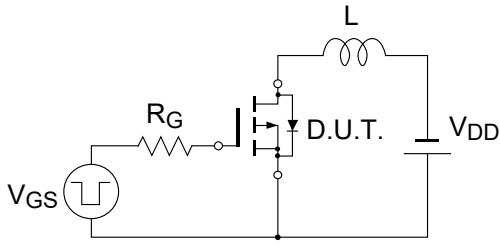
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



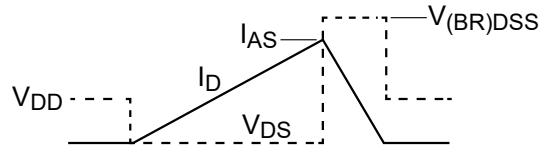
Test Circuit

Avalanche

Test Circuit



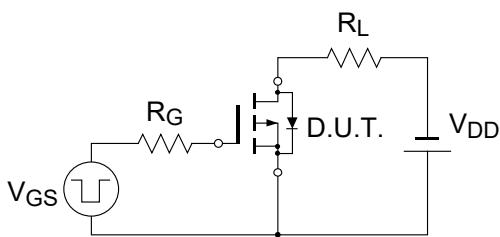
Waveform



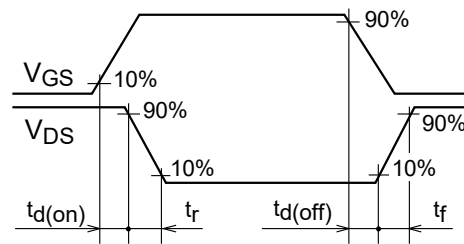
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

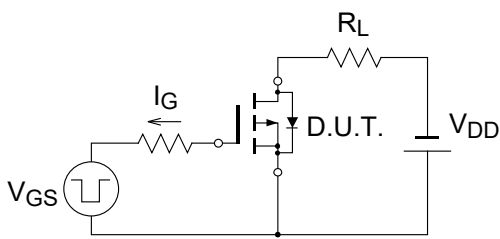


Waveform

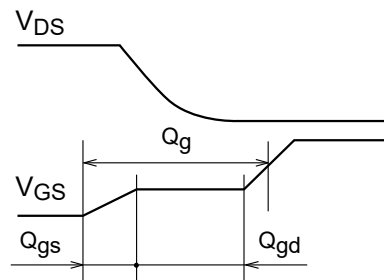


Gate Charge

Test Circuit

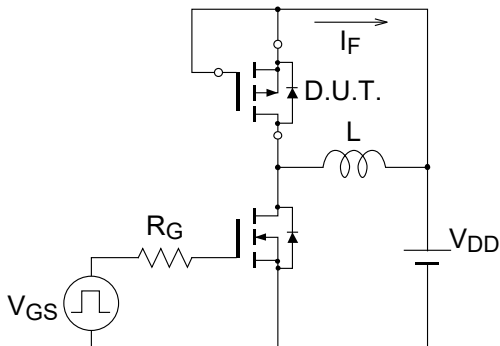


Waveform

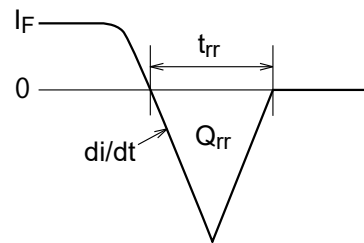


Reverse Recovery

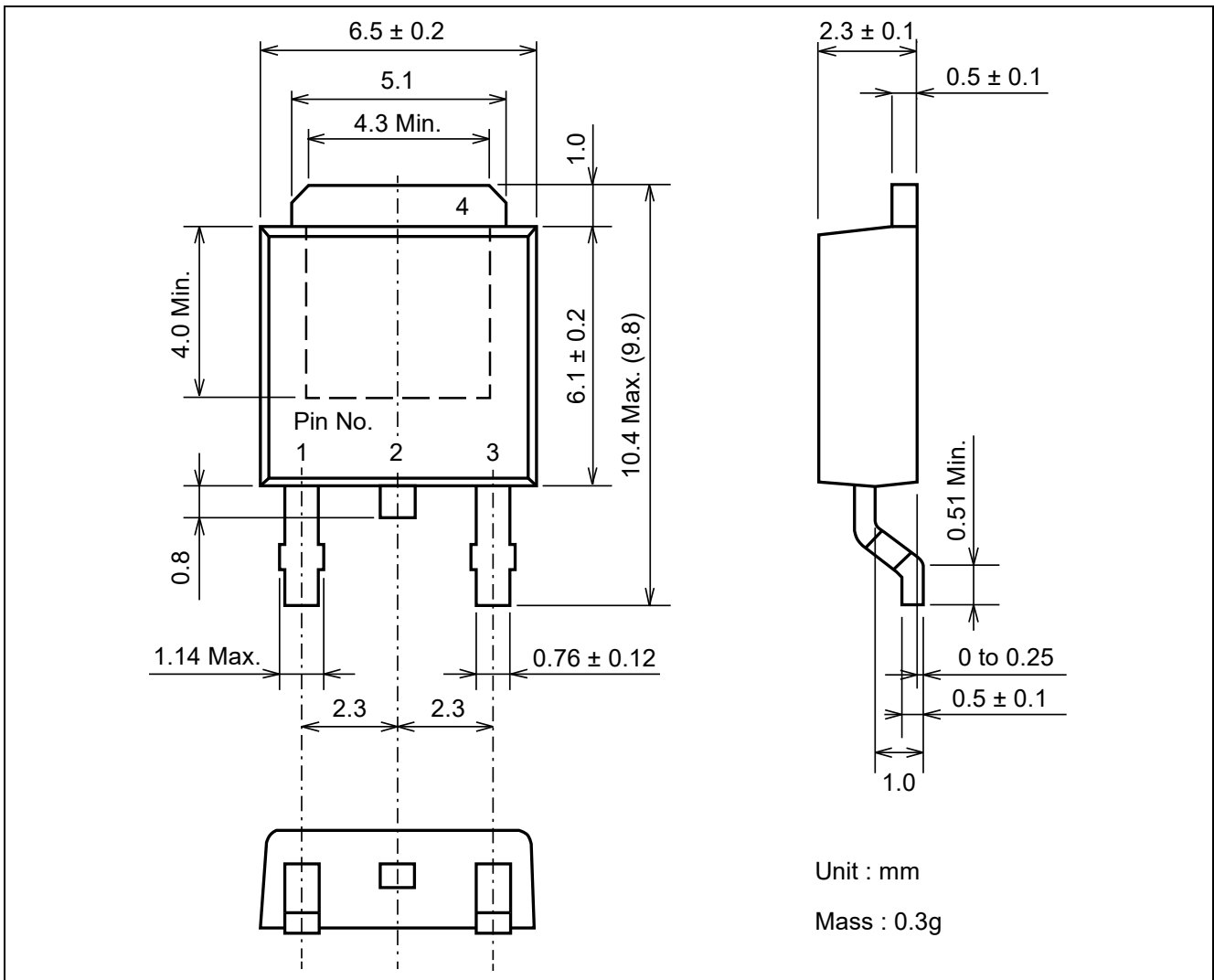
Test Circuit



Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping container
NP50P04SLG-E1-AY	2500pcs/reel	Taping

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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