

NP16N06YLL

60 V – 16 A – N-channel Power MOS FET
 Application: Automotive

R07DS1124EJ0100
 Rev.1.00
 Oct 30, 2013

Description

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Low on-state resistance
 — $R_{DS(on)} = 35 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$)
- Low C_{iss} : $C_{iss} = 400 \text{ pF TYP.}$ ($V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}$)
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

Outline

8-pin HSON

1, 2, 3 : Source
 4 : Gate
 5, 6, 7, 8: Drain

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Packing		Package
NP16N06YLL-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP16N06YLL-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0\text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0\text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 16	A
Drain Current (pulse) ^{*1}	$I_{D(pulse)}$	± 32	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	27.3	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{*2}	P_{T2}	1.25	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Single Avalanche Current ^{*3}	I_{AS}	10	A
Single Avalanche Energy ^{*3}	E_{AS}	10	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	5.49	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance ^{*2}	$R_{th(ch-A)}$	120.0	$^\circ\text{C/W}$

Notes: *1. $T_C = 25^\circ\text{C}$, $PW \leq 10\ \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of $40\text{ mm} \times 40\text{ mm} \times 1.6\text{ mm}$ with 4% copper area ($35\ \mu\text{m}$)

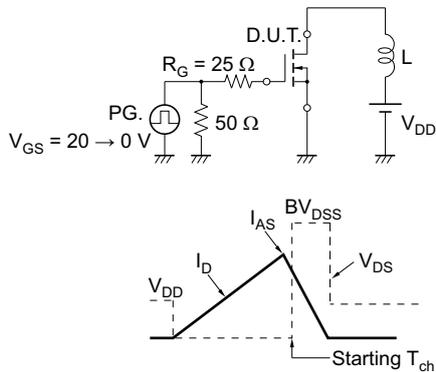
*3. $T_{ch(start)} = 25^\circ\text{C}$, $V_{DD} = 30\text{ V}$, $R_G = 25\ \Omega$, $L = 100\ \mu\text{H}$, $V_{GS} = 20\text{ V} \rightarrow 0\text{ V}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

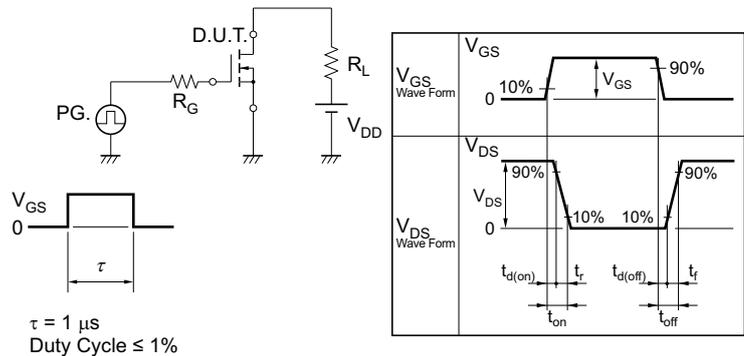
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$
Gate Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$
Gate Cut-off Voltage	$V_{GS(off)}$	1.0	1.5	2.0	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
Forward Transfer Admittance *1	$ y_{fs} $	5	12		S	$V_{DS} = 5.0\text{ V}, I_D = 8\text{ A}$
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		31	35	$\text{m}\Omega$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$
	$R_{DS(on)2}$		42	55	$\text{m}\Omega$	$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$
Input Capacitance	C_{iss}		400	600	pF	$V_{DS} = 25\text{ V},$ $V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		84	130	pF	
Reverse Transfer Capacitance	C_{rss}		54	100	pF	
Turn-on Delay Time	$t_{d(on)}$		8	16	ns	$V_{DD} = 30\text{ V}, I_D = 8\text{ A},$ $V_{GS} = 10\text{ V},$ $R_G = 0\ \Omega$
Rise Time	t_r		8	20	ns	
Turn-off Delay Time	$t_{d(off)}$		25	50	ns	
Fall Time	t_f		5	12.5	ns	
Total Gate Charge	Q_G		12	18	nC	
Gate to Source Charge	Q_{GS}		1.4		nC	$V_{DD} = 48\text{ V},$ $V_{GS} = 10\text{ V},$ $I_D = 16\text{ A}$
Gate to Drain Charge	Q_{GD}		4		nC	
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.95	1.24	V	$I_F = 16\text{ A}, V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}		27		ns	$I_F = 16\text{ A}, V_{GS} = 0\text{ V},$
Reverse Recovery Charge	Q_{rr}		28		nC	$di/dt = 100\text{ A}/\mu\text{s}$

Note: *1. Pulsed test

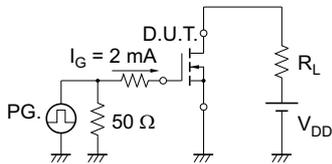
TEST CIRCUIT 1 AVALANCHE CAPABILITY



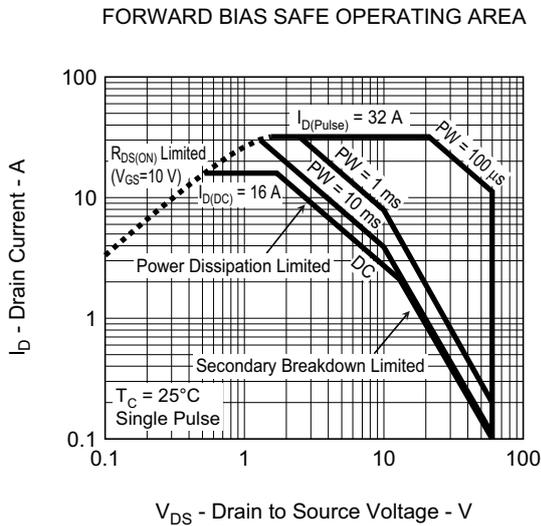
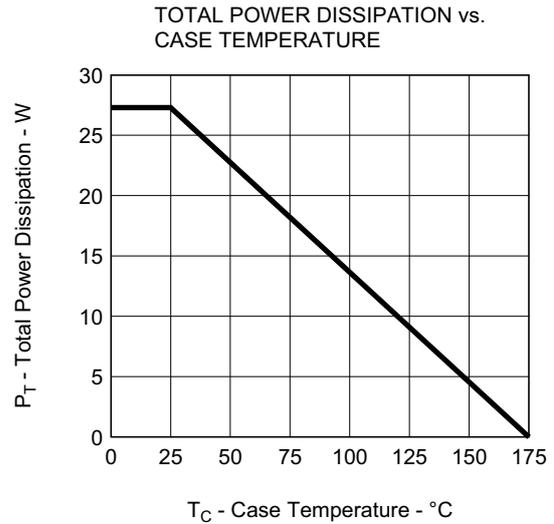
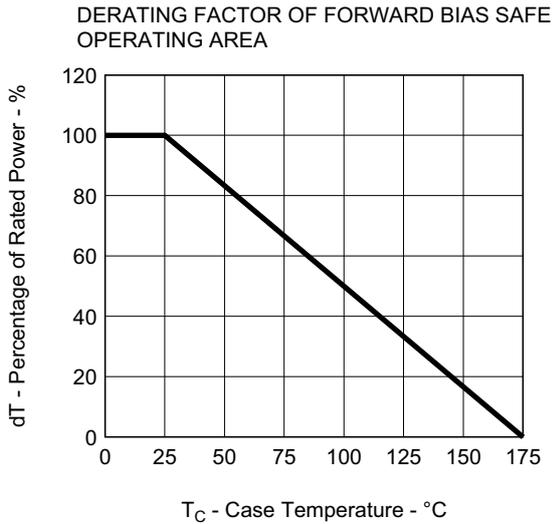
TEST CIRCUIT 2 SWITCHING TIME



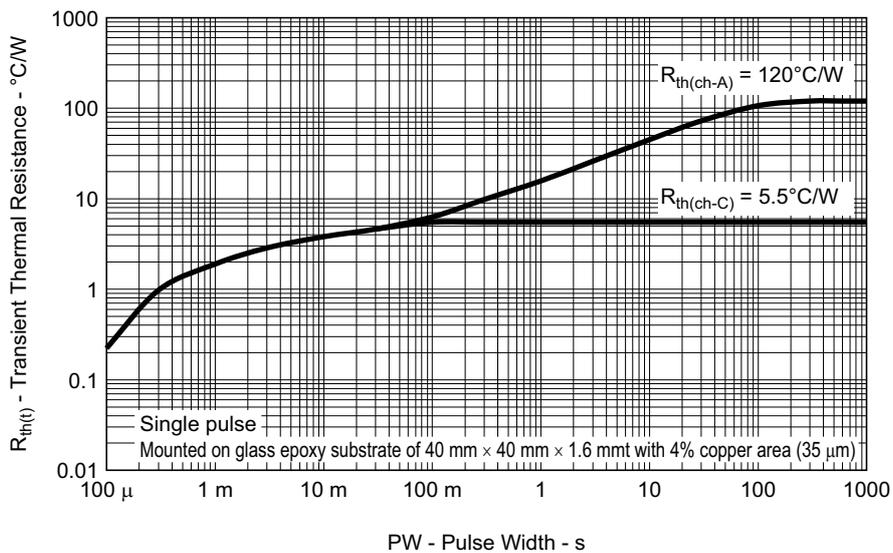
TEST CIRCUIT 3 GATE CHARGE



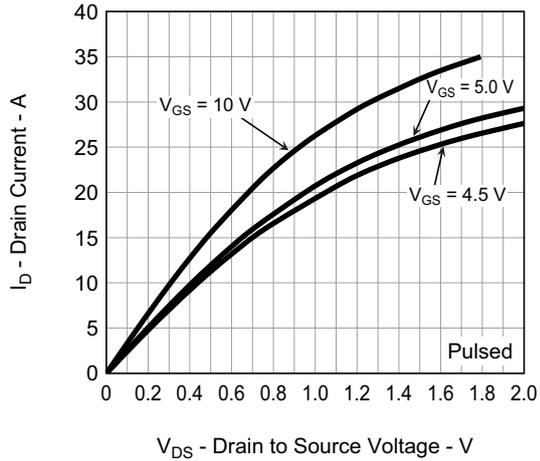
Typical Characteristics (T_A = 25°C)



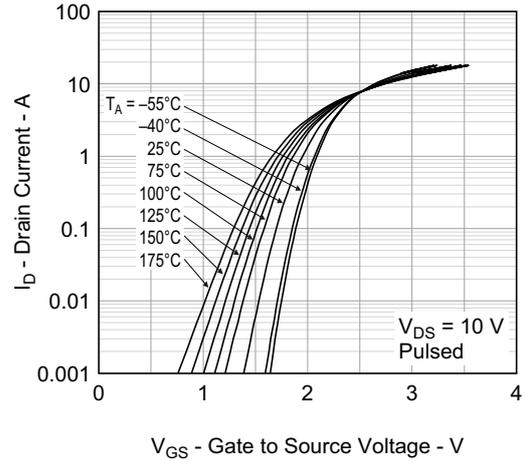
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



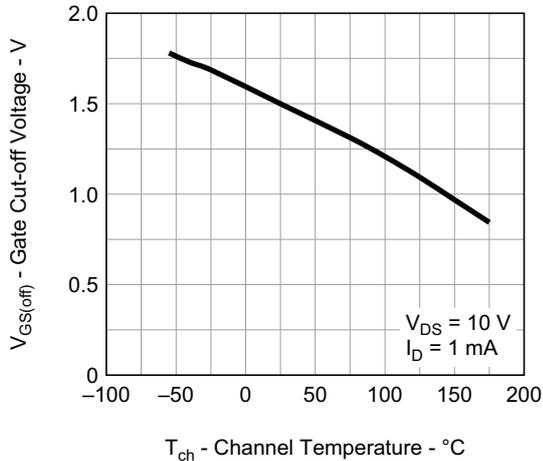
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



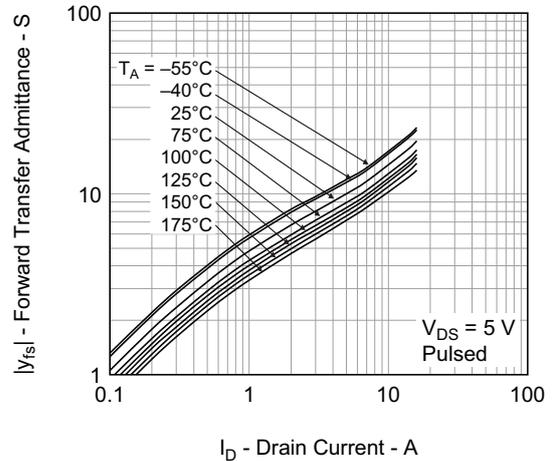
FORWARD TRANSFER CHARACTERISTICS



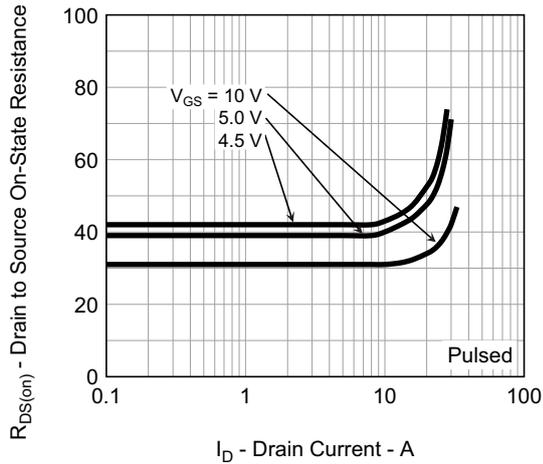
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



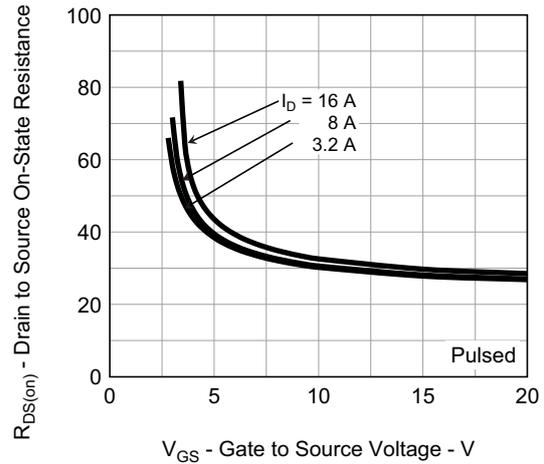
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



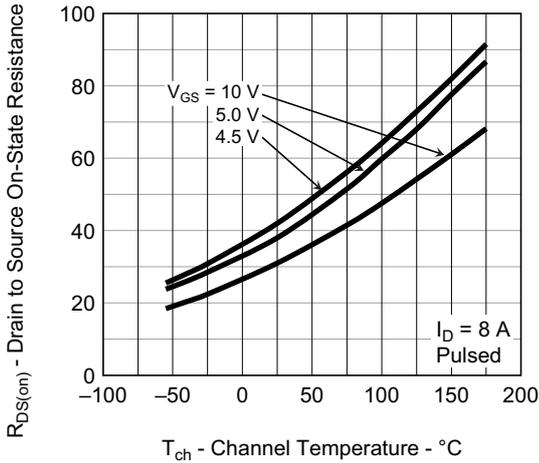
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



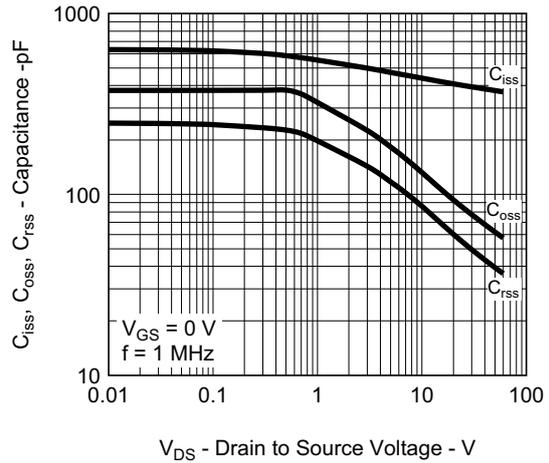
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



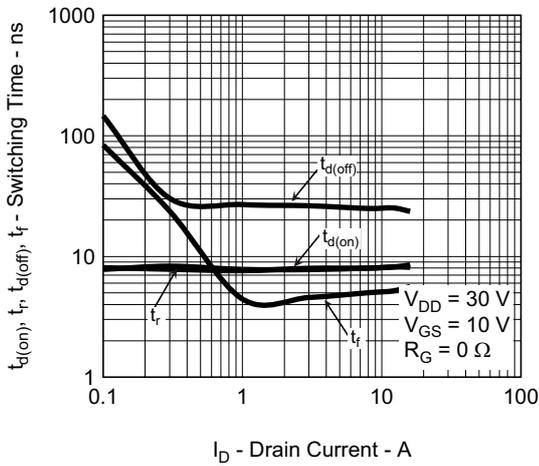
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



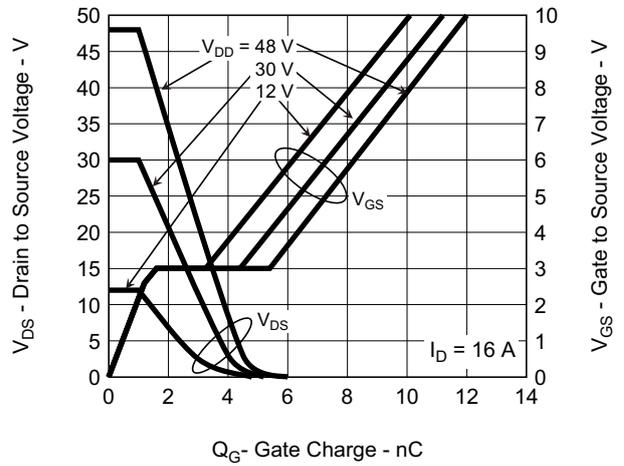
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



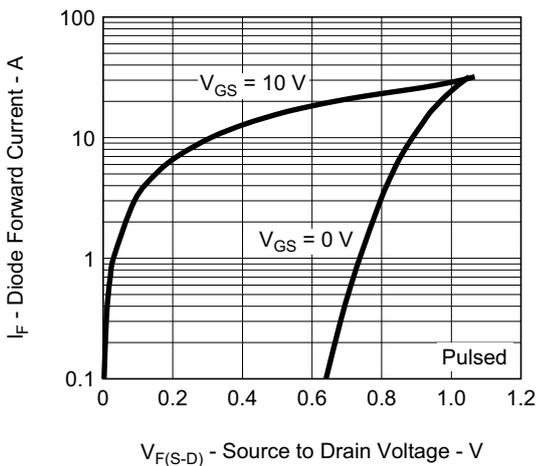
SWITCHING CHARACTERISTICS



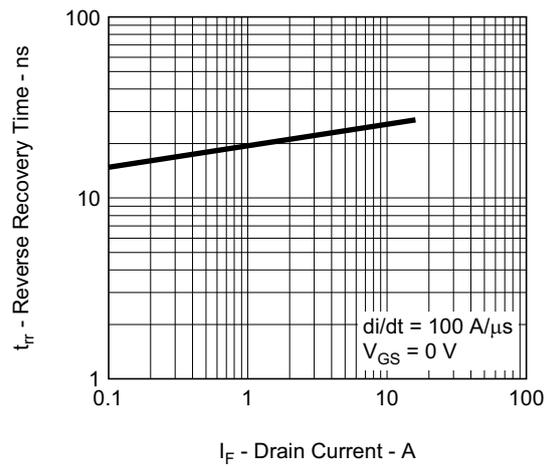
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



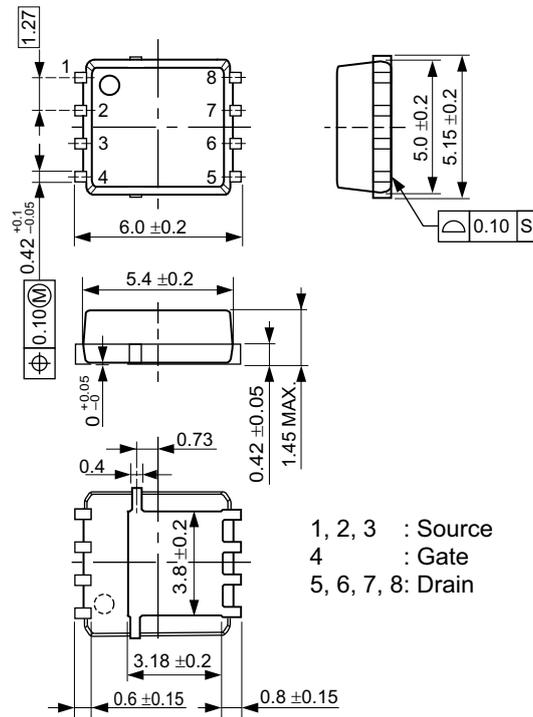
REVERSE RECOVERY TIME vs. DRAIN CURRENT



Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)

Renesas package code: PLSN0008KA-A



Revision History	NP16N06YLL Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Oct 30, 2013	—	First Edition Issued

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