

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued

GaAs FET

NES1823M-240

240 W L, S-BAND PUSH-PULL POWER GaAs FET

DESCRIPTION

The NES1823M-240 is a 240 W push-pull type GaAs FET designed for high power transmitter applications for IMT-2000 base station systems. It operates at 12 V and is capable of delivering 240 W of output power (CW) with high linear gain, high efficiency and low distortion. Its primary band is 1.8 to 2.3 GHz. The device employs 0.7 μm Tungsten Silicide gates, via holes, plated heat sink, and silicon dioxide passivation for superior performance, thermal characteristics, and reliability.

FEATURES

- Push-pull type GaAs FET
- $V_{DS} = 12.0$ V operation
- High output power: $P_{out} = 240$ W TYP.
- High linear gain: $G_L = 12.0$ dB TYP.
- High power added efficiency: $\eta_{add} = 45\%$ TYP. @ $V_{DS} = 12.0$ V, $I_{Dset} = 2.0$ A (total), $f = 2.17$ GHz
- Hollow plastic package

★ ORDERING INFORMATION

Part Number	Order Number	Package	Supplying Form
NES1823M-240	NES1823M-240-A	T-92M (Pb-Free)	ESD protective tray

Remark To order evaluation samples, contact your nearby sales office.

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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 Not all devices/types available in every country. Please check with local NEC Compound Semiconductor Devices representative for availability and additional information.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

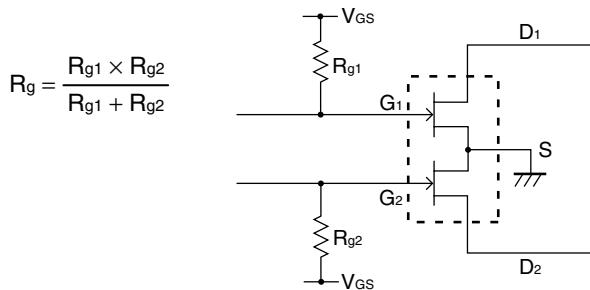
Operation in excess of any one of these parameters may result in permanent damage.

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DS}	19	V
Gate to Source Voltage	V _{GSO}	-7	V
Gate to Drain Voltage	V _{GDO}	-26	V
Gate Current	I _G	900	mA
Total Power Dissipation	P _{tot}	250	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-65 to +150	°C
Gain Compression(CW)	Gcomp	3.0	dB

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V _{DS}		-	12.0	12.0	V
Channel Temperature	T _{ch}		-	-	+150	°C
Set Drain Current	I _{Dset}	V _{DS} = 12.0 V, RF OFF	-	2.0	6.0	A
Gate Resistance	R _g ^{Note}		-	0.6	1.2	Ω

Note R_g is the series resistance between the gate supply and the FET gate.



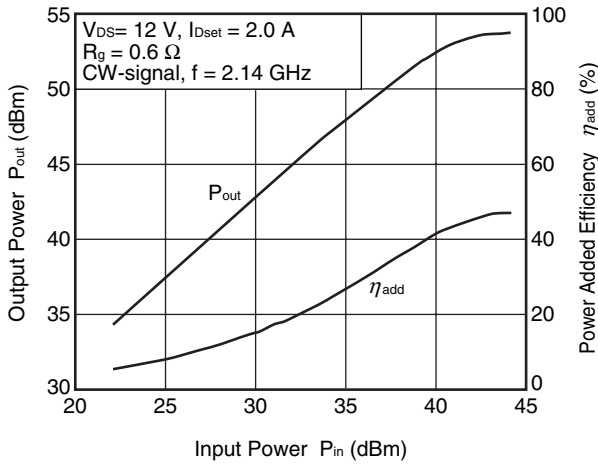
ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Pinch-off Voltage	V _p	V _{DS} = 2.5 V, I _D = 650 mA	-0.8	-0.5	-0.2	V
Thermal Resistance	R _{th}	Channel to Case	-	0.30	0.40	°C/W
Output Power	P _{out}	f = 2.17 GHz, V _{DS} = 12.0 V,	52.8	53.4	-	dBm
Drain Current	I _D	P _{in} = 44.0 dBm, R _g = 0.6 Ω,	-	38.5	-	A
Power Added Efficiency	η _{add}	I _{Dset} = 2.0 A Total (RF OFF) ^{Note1}	-	45	-	%
Linear Gain	G _L ^{Note2}		11.0	12.0	-	dB

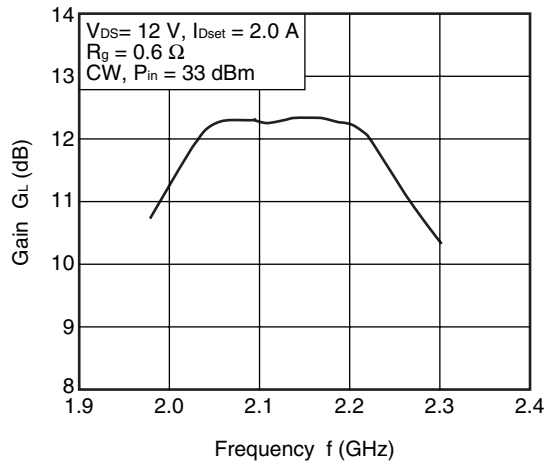
- Notes1.** I_{Dset} = 1.0 A each drain
- 2.** P_{in} = 33 dBm

TYPICAL CHARACTERISTICS (T_A = +25°C)

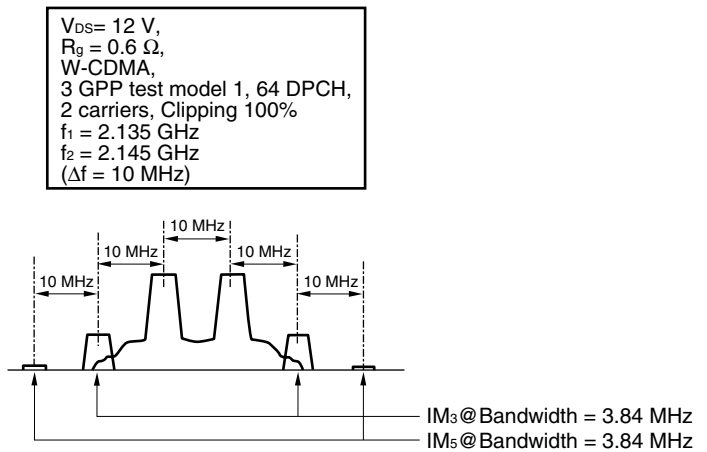
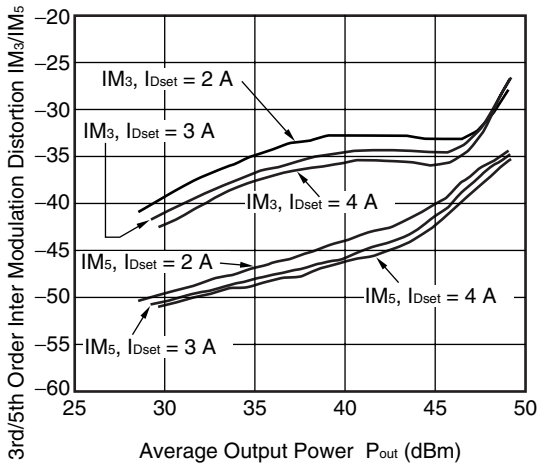
OUTPUT POWER, η_{add} vs. INPUT POWER



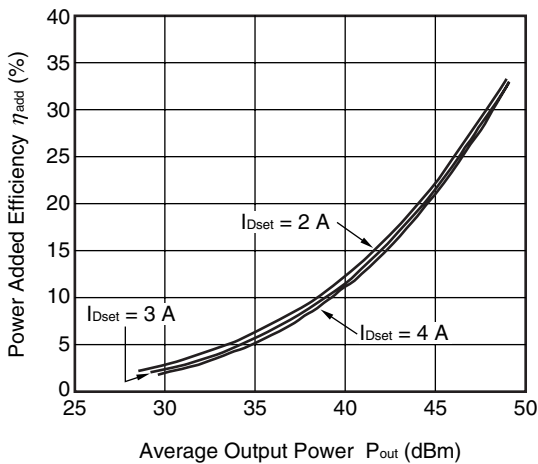
GAIN vs. FREQUENCY RESPONSE



IM₃/IM₅ vs. AVERAGE OUTPUT POWER (SET I_{DS} DEPENDENCE)

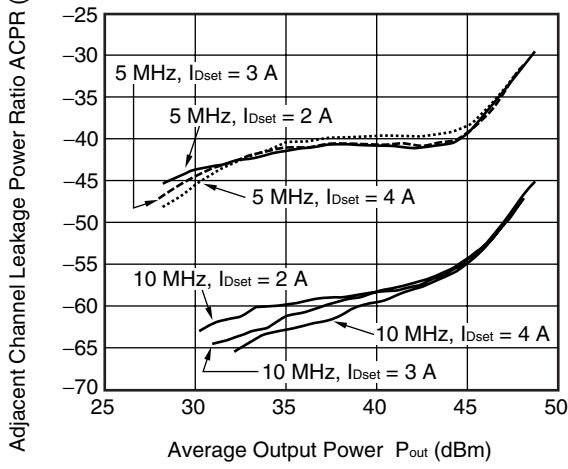


η_{add} vs. AVERAGE OUTPUT POWER (SET I_{DS} DEPENDENCE)

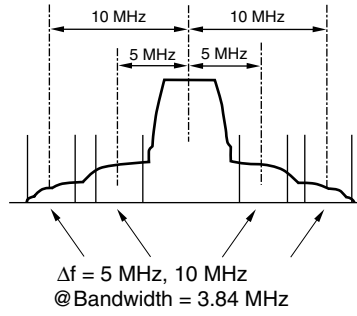


Remark The graphs indicate nominal characteristics.

ACPR vs. AVERAGE OUTPUT POWER
(SET I_{Dset} DEPENDENCE)

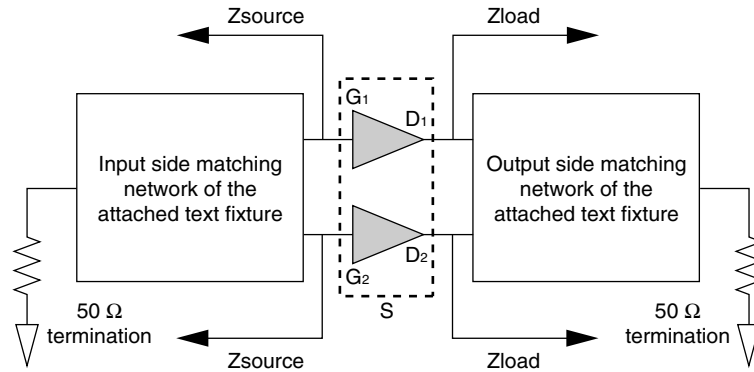


$V_{DS} = 12$ V,
 $R_g = 0.6 \Omega$,
 W-CDMA,
 3 GPP test model 1, 64 DPCH,
 1 carriers, Clipping 100%
 $f = 2.14$ GHz



Remark The graphs indicate nominal characteristics.

**LARGE SIGNAL IMPEDANCES
(HALF (EACH SIDE) DEVICE OPTIMAL INPUT AND OUTPUT IMPEDANCE)**



Test fixture tuning condition
 $V_{DS} = 12\text{ V}$, $I_{Dset} = 2.0\text{ A}$
 $R_g = 0.6\ \Omega$, $P_{IN} = 44\text{ dBm}$

- Remarks1.** $Z_{in} = R_{in} + jX_{in}$ (Conjugate of Z_{source} for single ended device)
 $Z_{out} = R_{out} + jX_{out}$ (Conjugate of Z_{load} for single ended device)
2. Z_{out} was chosen based on tradeoffs between gain, PAE and IM.

f (GHz)	$Z_{in} (\Omega)$	$Z_{out} (\Omega)$
2.10	1.063 – j7.204	3.862 – j5.151
2.11	1.060 – j6.685	3.994 – j4.854
2.12	1.111 – j6.233	4.114 – j4.653
2.13	1.129 – j5.839	4.218 – j4.519
2.14	1.135 – j5.403	4.296 – j4.400
2.15	1.173 – j5.161	4.368 – j4.304
2.16	1.176 – j4.735	4.402 – j4.083
2.17	1.188 – j4.384	1.382 – j3.948
2.18	1.184 – j4.013	4.442 – j3.780
2.19	1.201 – j3.694	4.457 – j3.726

f (GHz)	$Z_{in} (\Omega)$	$Z_{out} (\Omega)$
2.20	1.268 – j3.319	4.441 – j3.539
2.21	1.283 – j2.838	4.463 – j3.350
2.22	1.315 – j2.518	4.462 – j3.257
2.23	1.401 – j2.172	4.451 – j3.102
2.24	1.458 – j1.777	4.429 – j2.921
2.25	1.544 – j1.408	4.452 – j2.755
2.26	1.622 – j1.129	4.454 – j2.614
2.27	1.711 – j0.773	4.456 – j2.431
2.28	1.794 – j0.482	4.399 – j2.184
2.29	1.899 – j0.180	4.454 – j2.074
2.30	1.971 + j0.174	4.493 – j1.836

S-PARAMETERS

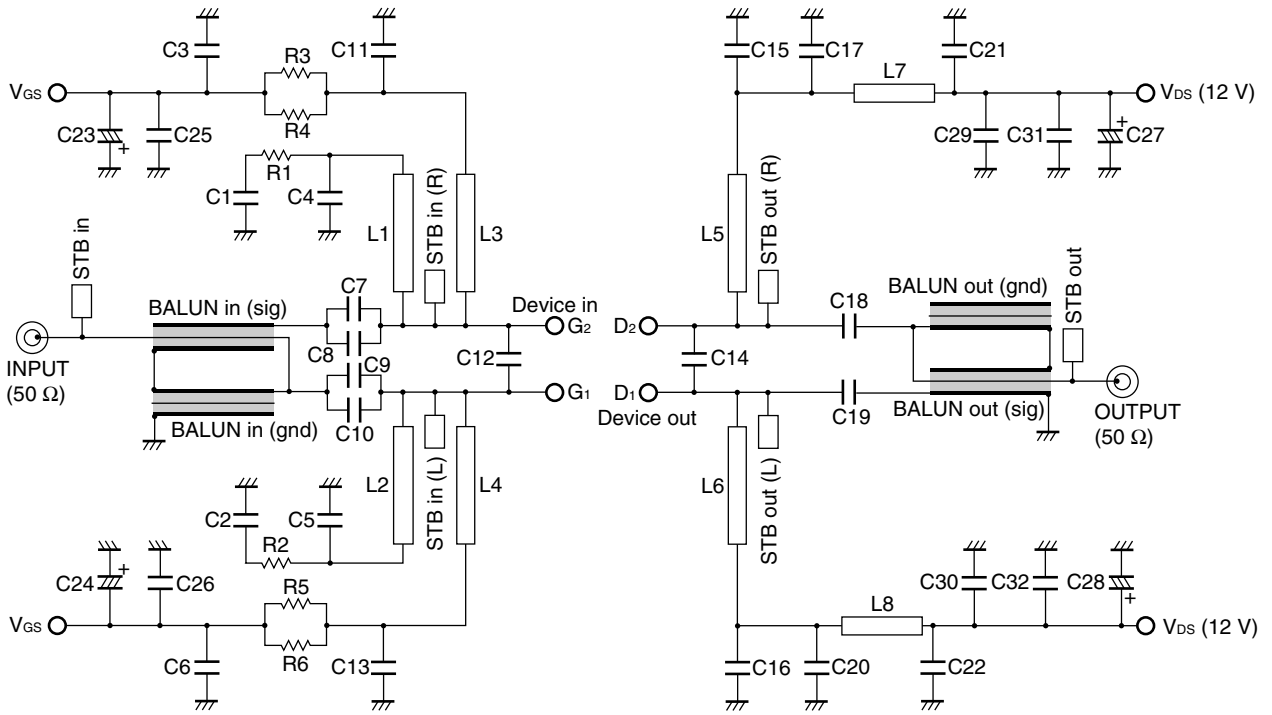
S-parameters/Noise parameters are provided on the NEC Compound Semiconductor Devices Web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

Click here to download S-parameters.

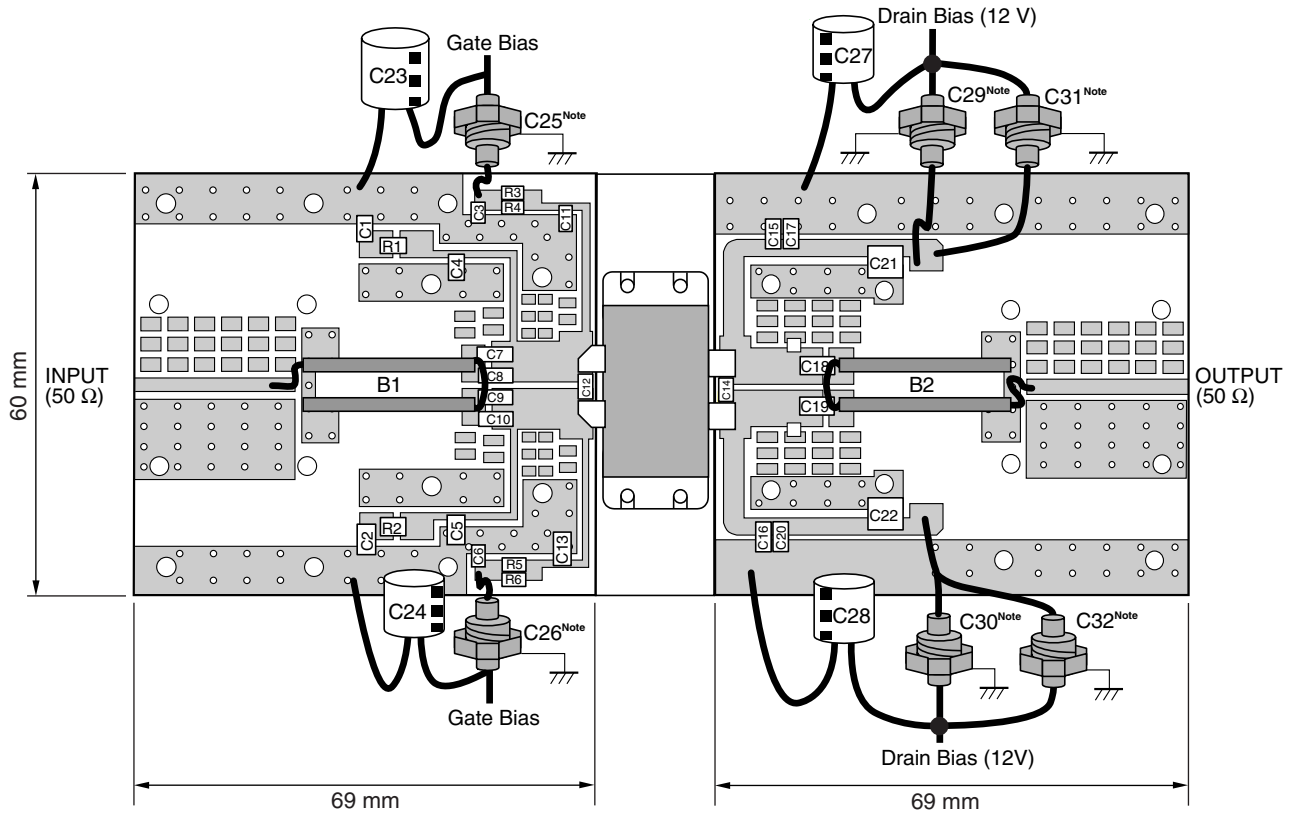
[RF and Microwave] → [Device Parameters]

URL <http://www.ncsd.necel.com/>

★ EVALUATION PWB CIRCUIT

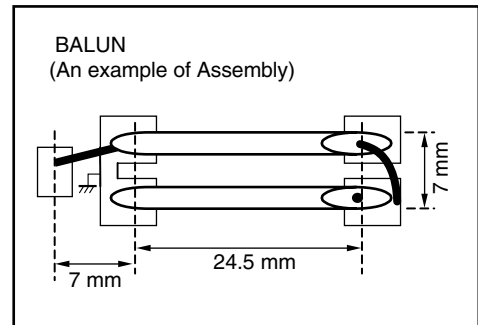


EVALUATION PWB PARTS LAYOUT



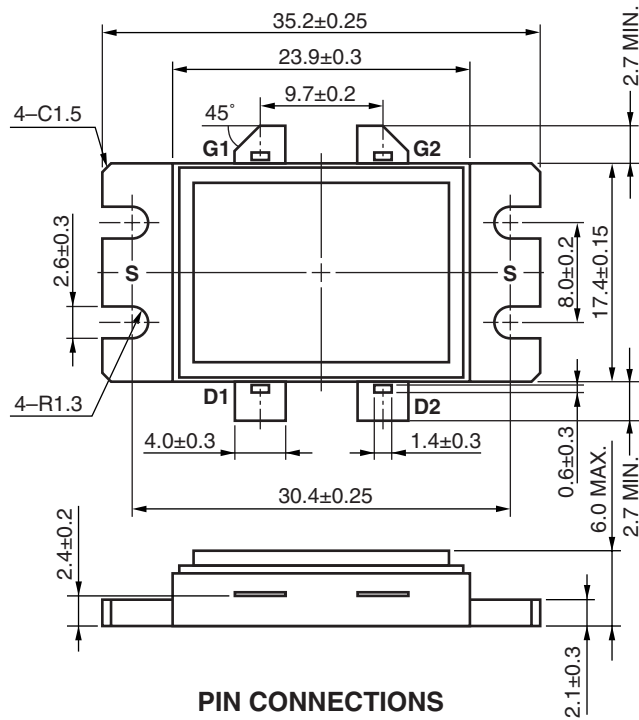
Note Feed-through capacitor

Parts Name	Parts Value
C12, C14	1 pF chip capacitor
C4, C5, C11, C13	4 pF chip capacitor
C18, C19	10 pF chip capacitor
C7, C8, C9, C10	12 pF chip capacitor
C15, C16	22 pF chip capacitor
C1, C2, C3, C6	1 000 pF chip capacitor
C25, C26, C29, C30, C31, C32	1 000 pF feed-through capacitor
C17, C20	0.1 μ F chip capacitor
C21, C22	10 μ F chip capacitor (25 V)
C23, C24, C27, C28	100 μ F Electrolytic capacitor (25 V)
R3, R4, R5, R6	2.2 Ω chip resistor (1/4 W)
R1, R2	10 Ω chip resistor (1/4 W)
B1, B2	BALUN
Circuit Board	Material ; Teflon, Er = 2.6, PWB Thickness : 0.8 mm, Cu-Pattern Thickness : 18 μ m



PACKAGE DIMENSIONS

T-92M (UNIT: mm)



PIN CONNECTIONS

- G1, G2 : Gate
- D1, D2 : Drain
- S : Source

RECOMMENDED MOUNTING CONDITIONS FOR CORRECT USE

- (1) Fix to a heat sink or mount surface completely with screws at the four holes of the flange.
- (2) The recommended torque strength of the screws is 29.4 N-cm typical using M2.3 type screws.
- (3) The recommended flatness of the mount surface is less than $\pm 10 \mu\text{m}$ (roughness of surface is $\nabla\nabla\nabla$).

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Partial Heating	Peak temperature (terminal temperature)	: 350°C or below
	Soldering time (per terminal of device)	: 3 seconds or less
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below

Caution Do not use different soldering methods together (except for partial heating).

DEFINIITON OF THERMAL RESISTANCE

This thermal resistance (R_{th} : channel to case) guaranteed in the electrical characteristics shows the value between chip surface and the backside surface of the package.

The thermal resistance between chip surface and mount surface is 0.2 (MAX.) °C/W larger than the thermal resistance value guaranteed in the electrical characteristics, when the package is under the above-mentioned recommendation mounting condition screwed down.

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M8E 00.4-0110

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► For further information, please contact

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