

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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for new design

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SILICON POWER MOS FET NE5510279A

4.8 V OPERATION SILICON RF POWER LDMOS FET FOR 1.8 GHz 2 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE5510279A is an N-channel silicon power MOS FET specially designed as the transmission power amplifier for 4.8 V GSM 1 800 handsets. Dies are manufactured using our NEWMOS technology (our 0.6 μm WSi gate laterally diffused MOS FET) and housed in a surface mount package. The device can deliver 33.0 dBm output power with 47% power added efficiency at 1.8 GHz under the 4.8 V supply voltage.

FEATURES

- High output power : $P_{\text{out}} = 35.5$ dBm TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 300$ mA, $f = 900$ MHz, $P_{\text{in}} = 25$ dBm)
: $P_{\text{out}} = 33.0$ dBm TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 300$ mA, $f = 1.8$ GHz, $P_{\text{in}} = 25$ dBm)
- High power added efficiency : $\eta_{\text{add}} = 65\%$ TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 300$ mA, $f = 900$ MHz, $P_{\text{in}} = 25$ dBm)
: $\eta_{\text{add}} = 47\%$ TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 300$ mA, $f = 1.8$ GHz, $P_{\text{in}} = 25$ dBm)
- High linear gain : $G_{\text{L}} = 16.0$ dB TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 300$ mA, $f = 900$ MHz, $P_{\text{in}} = 10$ dBm)
: $G_{\text{L}} = 10.0$ dB TYP. ($V_{\text{DS}} = 4.8$ V, $I_{\text{Dset}} = 300$ mA, $f = 1.8$ GHz, $P_{\text{in}} = 10$ dBm)
- Surface mount package : $5.7 \times 5.7 \times 1.1$ mm MAX.
- ★ • Single supply : $V_{\text{DS}} = 3.0$ to 8.0 V

APPLICATIONS

- Digital cellular phones : 4.8 V GSM 1 800 class 1 handsets
- Others : General purpose amplifiers for 1.6 to 2.0 GHz TDMA applications

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5510279A-T1	79A	W2	<ul style="list-style-type: none"> • 12 mm wide embossed taping • Gate pin face the perforation side of the tape • Qty 1 kpcs/reel

Remark To order evaluation samples, contact your nearby sales office.
Part number for sample order: NE5510279A

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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Not all devices/types available in every country. Please check with local NEC Compound Semiconductor Devices representative for availability and additional information.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DS}	20.0	V
Gate to Source Voltage	V _{GS}	5.0	V
Drain Current	I _D	1.0	A
Drain Current (Pulse Test)	I _D ^{Note}	2.0	A
Total Power Dissipation	P _{tot}	20	W
Channel Temperature	T _{ch}	125	°C
Storage Temperature	T _{stg}	-65 to +125	°C

Note Duty Cycle ≤ 50%, T_{on} ≤ 1 s

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
★ Drain to Source Voltage	V _{DS}		3.0	4.8	8.0	V
Gate to Source Voltage	V _{GS}		0	2.0	3.5	V
Drain Current (Pulse Test)	I _D	Duty Cycle ≤ 50%, T _{on} ≤ 1 s	–	1.0	1.5	A
Input Power	P _{in}	f = 1.8 GHz, V _{DS} = 4.8 V	25	–	27	dBm

Not recommended for new design

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	I _{GSS}	V _{GSS} = 5.0 V	–	–	100	nA
Drain to Source Leakage Current (Zero Gate Voltage Drain Current)	I _{DSS}	V _{DSS} = 8.5 V	–	–	100	nA
Gate Threshold Voltage	V _{th}	V _{DS} = 4.8 V, I _D = 1 mA	1.0	1.35	2.0	V
Transconductance	G _m	V _{DS} = 4.8 V, I _D = 600 mA	–	1.50	–	S
Drain to Source Breakdown Voltage	BV _{DSS}	I _{DSS} = 10 μA	20	24	–	V
Thermal Resistance	R _{th}	Channel to Case	–	5	–	°C/W
Linear Gain	G _L	f = 900 MHz, P _{in} = 10 dBm, V _{DS} = 4.8 V, I _{Dset} = 300 mA, Note 1, 2	–	16.0	–	dB
Output Power	P _{out}	f = 900 MHz, P _{in} = 25 dBm,	–	35.5	–	dBm
Operating Current	I _{op}	V _{DS} = 4.8 V, I _{Dset} = 300 mA, Note 1, 2	–	1 000	–	mA
Power Added Efficiency	η _{add}		–	65	–	%
Linear Gain	G _L	f = 1.8 GHz, P _{in} = 10 dBm, V _{DS} = 4.8 V, I _{Dset} = 300 mA, Note 1, 2	–	10.0	–	dB
Output Power	P _{out}	f = 1.8 GHz, P _{in} = 25 dBm,	32.0	33.0	–	dBm
Operating Current	I _{op}	V _{DS} = 4.8 V, I _{Dset} = 300 mA, Note 1, 2	–	750	–	mA
Power Added Efficiency	η _{add}		38	47	–	%

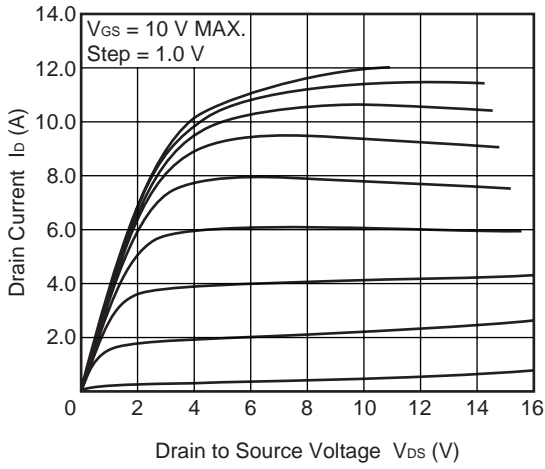
Notes 1. Peak measurement at Duty Cycle ≤ 50%, T_{on} ≤ 1 s.

2. DC performance is 100% testing. RF performance is testing several samples per wafer.

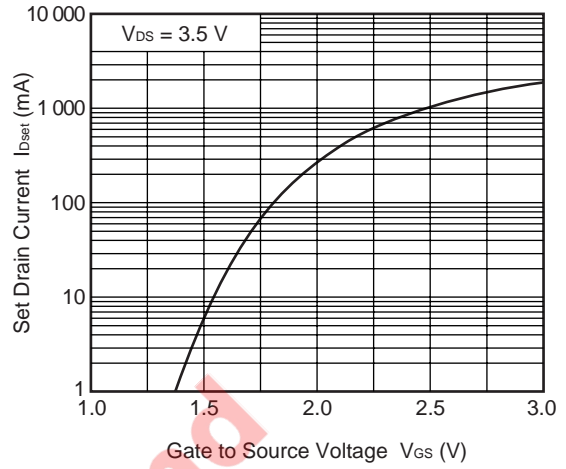
Wafer rejection criteria for standard devices is 1 reject for several samples.

TYPICAL CHARACTERISTICS (T_A = +25°C)

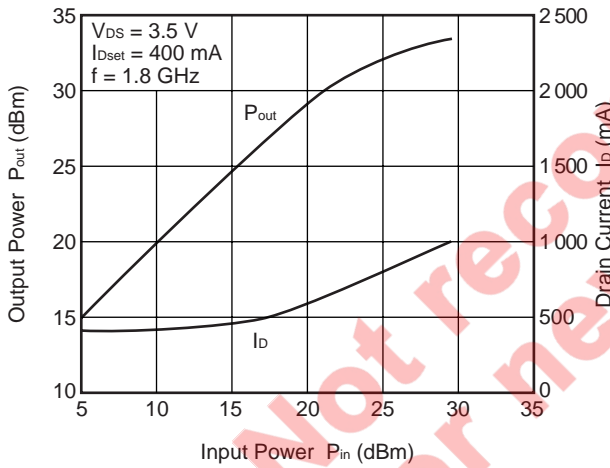
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



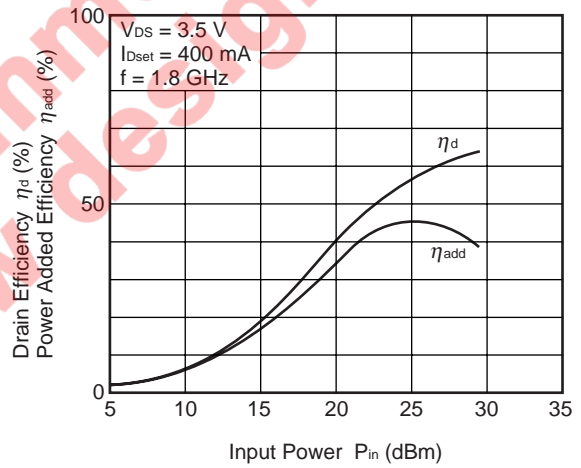
SET DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



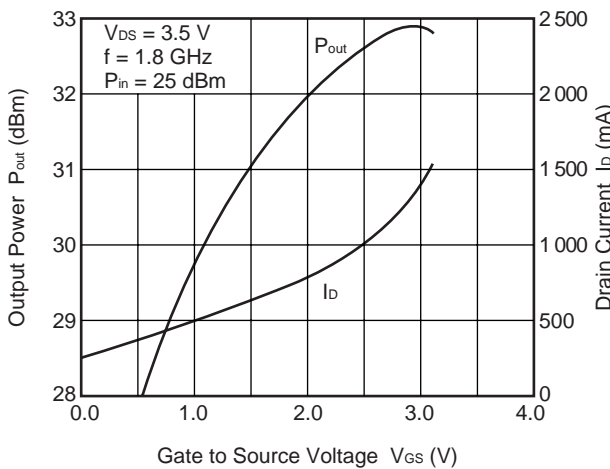
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



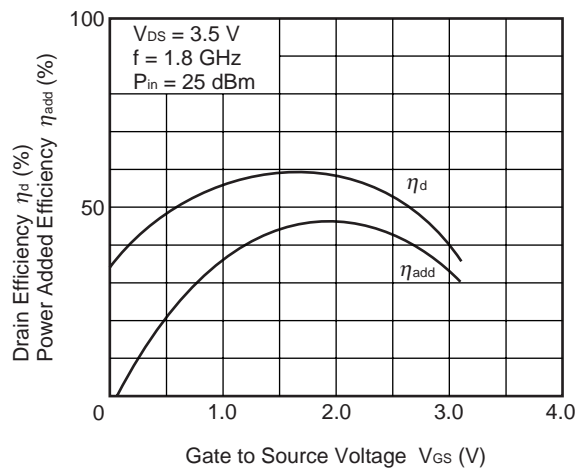
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



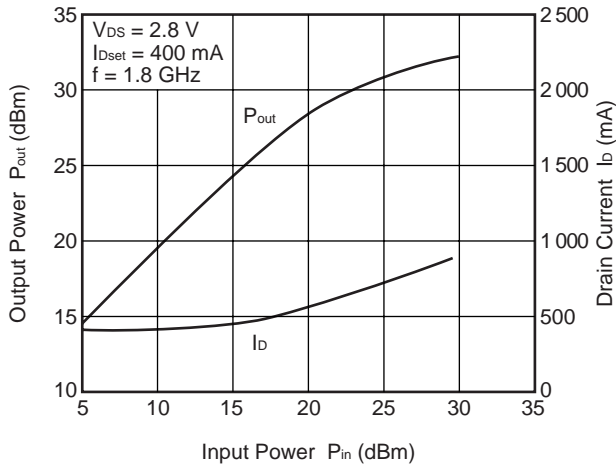
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



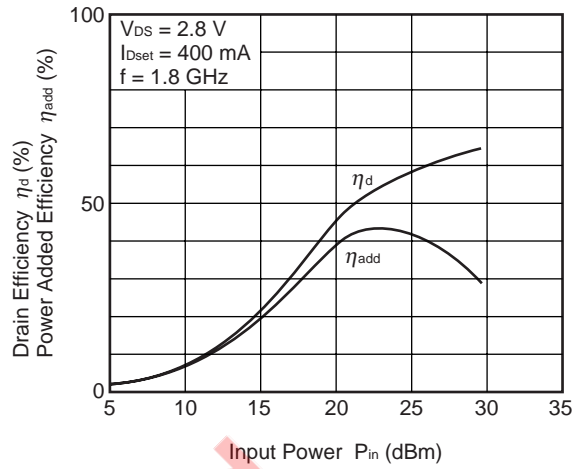
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



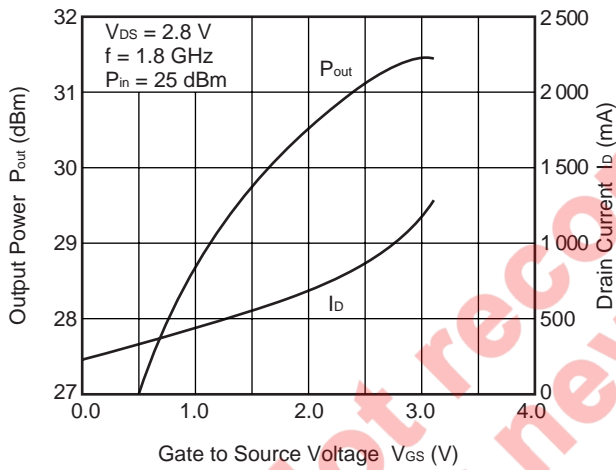
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



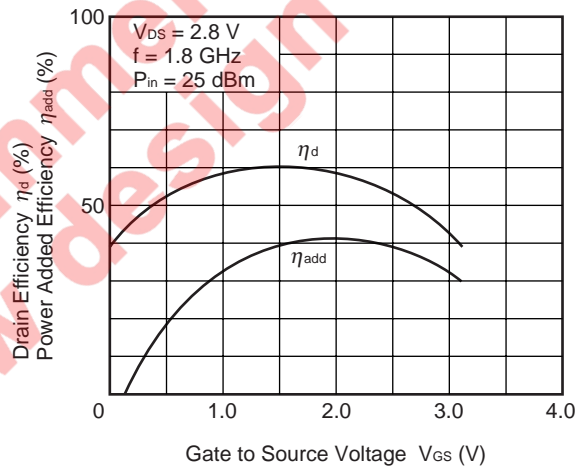
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



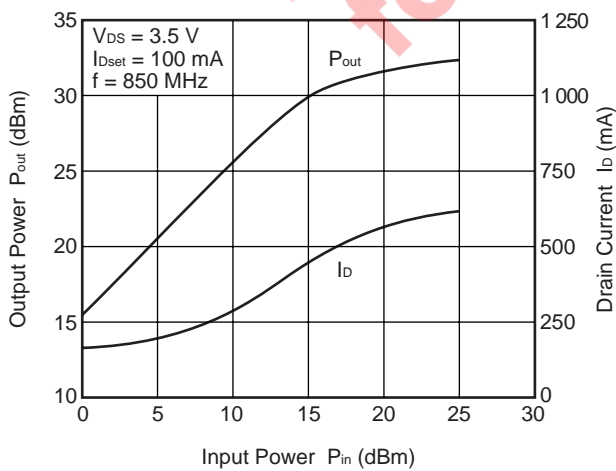
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



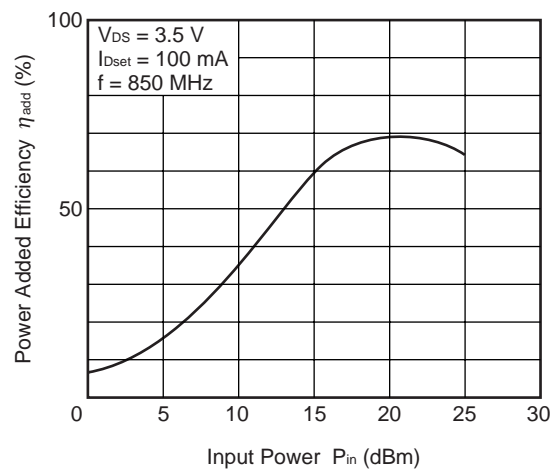
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



POWER ADDED EFFICIENCY vs. INPUT POWER



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

S-parameters/Noise parameters are provided on the NEC Compound Semiconductor Devices Web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

Click here to download S-parameters.

[RF and Microwave] → [Device Parameters]

URL <http://www.csd-nec.com/>

LARGE SIGNAL IMPEDANCE ($V_{ds} = 3.5\text{ V}$, $I_b = 400\text{ mA}$, $P_{in} = 25\text{ dBm}$)

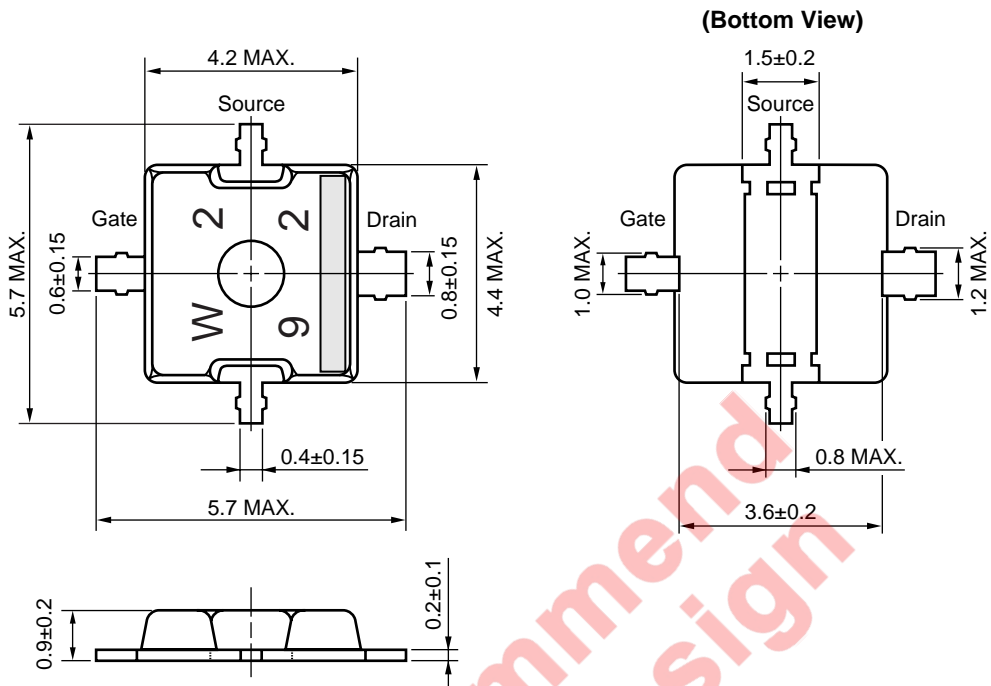
f (GHz)	Z_{in} (Ω)	Z_{OL} (Ω) ^{Note}
1.8	TBD	TBD

Note Z_{OL} is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

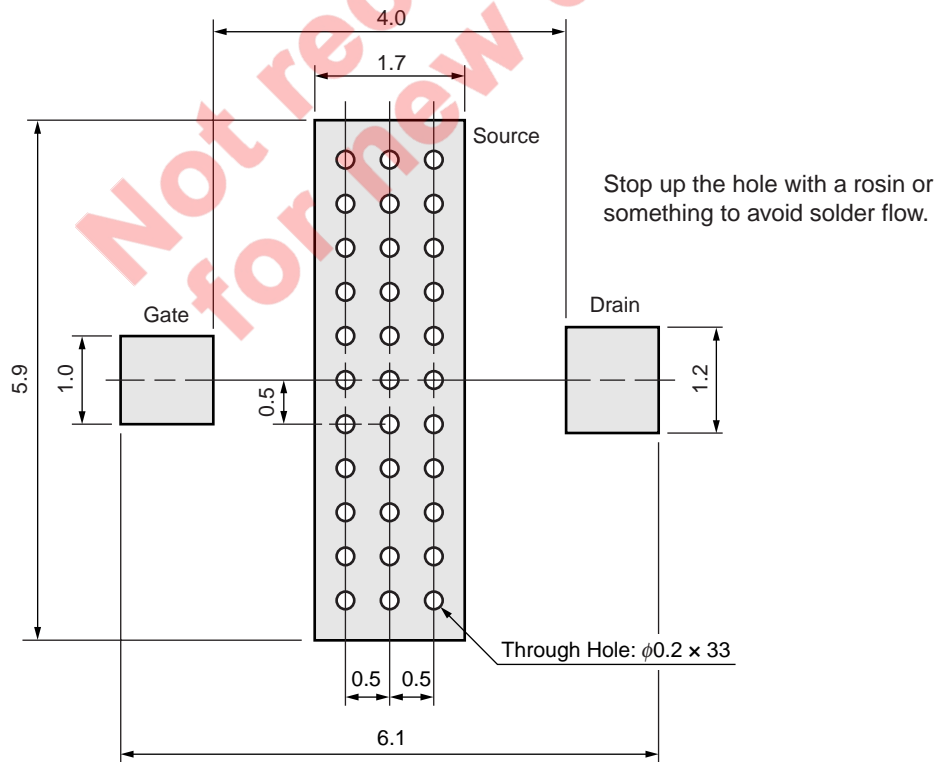
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★ PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)



RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) : 215°C or below Time at temperature of 200°C or higher : 25 to 40 seconds Preheating time at 120 to 150°C : 30 to 60 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) : 260°C or below Time at peak temperature : 10 seconds or less Preheating temperature (package surface temperature) : 120°C or below Maximum number of flow processes : 1 time Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) : 350°C or below Soldering time (per pin of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	HS350-P3

Caution Do not use different soldering methods together (except for partial heating).

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