To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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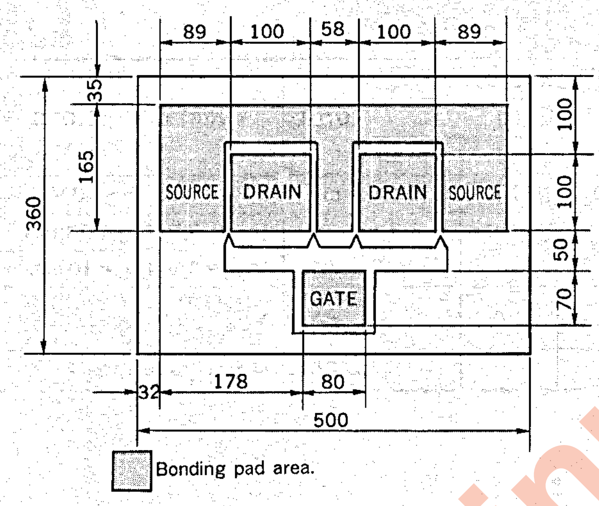
RENESAS

GaAs MES FET
NE218

LOW NOISE X-BAND GaAs FET
N-CHANNEL GaAs MES FET

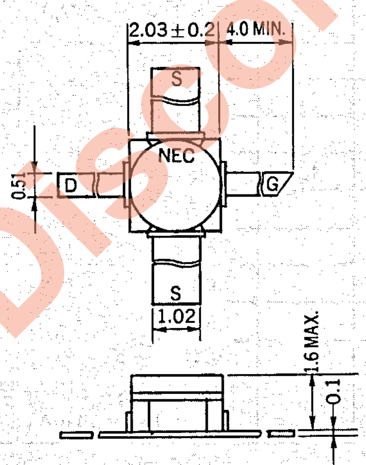
PHYSICAL DIMENSIONS

NE21800 (Chip) (Units in μm)



PACKAGE CODE - 89

(Units in mm)



DESCRIPTION

The NE218 is a n-channel GaAs FET employing a 1.0 μm recessed gate. Offering exceptionally low noise figure and high associated gain through 8 GHz, the NE218 is ideal for 3.7 to 4.2 GHz ground station LNA applications. The device is available as a chip (NE21800), and in a hermetically sealed package (NE21889). The chip's gate and channel are glassivated with a thin layer of SiO_2 for mechanical protection.

FEATURES

- Very high $f_{max.}$: 60 GHz
- Low noise figure :
  - NF 1.0 dB, G_a 12.0 dB @f = 4 GHz
  - NF 1.7 dB, G_a 10.5 dB @f = 8 GHz
  - NF 2.8 dB, G_a 7.0 dB @f = 12 GHz
- High maximum available gain
  - MAG 16.5 dB @f = 4 GHz
  - MAG 11.5 dB @f = 8 GHz
  - MAG 9.5 dB @f = 12 GHz
- Proven reliability and stability
- 1.0 μm recessed gate

ORDERING INFORMATION

PART NUMBER	PACKAGE CODE
NE21800	00 (CHIP)
NE21889	89

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DS}	5.0	V	
Gate to Source Voltage	V_{GS}	-6.0	V	
Drain Current	I_{DS}	120	mA	
Total Power Dissipation	P_T	500 *1, *3	mW	(NE21800)
		300 *2	mW	(NE21889)
RF Input Power	P_{in}	40	mW	
Channel Temperature	T_{ch}	175	°C	
Storage Temperature	T_{stg}	-65 to +175	°C	

*1 T_a = 90 °C
*2 T_a = 55 °C
*3 R_{th} (channel to case) for chips mounted on a copper heatsink.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

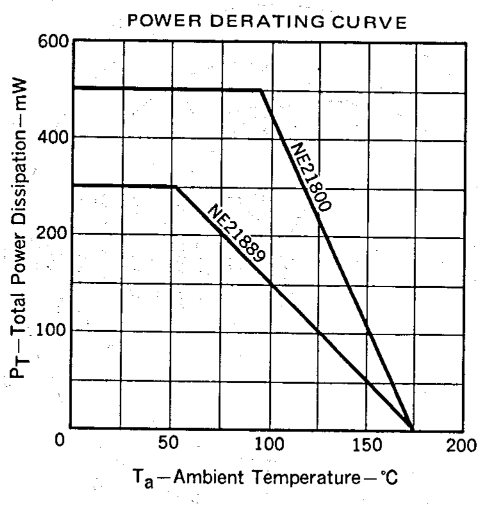
PART NUMBER		NE21800			NE21889			UNIT	TEST CONDITIONS
PACKAGE CODE		00 (CHIP)			89				
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Saturated Drain Current	I_{DSS}	30	70	120	30	70	120	mA	V_{DS} = 3 V, V_{GS} = 0 V
Pinch-off Voltage	V_P	-0.8	-2.0	-6.0	-0.8	-2.0	-6.0	V	V_{DS} = 3 V, I_{DS} = 0.1 mA
Transconductance	g_m	20	40	100	20	40	100	mS	V_{DS} = 3 V, I_{DS} = 10 mA
Gate to Source Leakage Current	I_{GS}		1.0	10		1.0	10	μA	V_{GS} = -5 V
Thermal Resistance	R_{th}			170*3			400	°C/W	channel to case

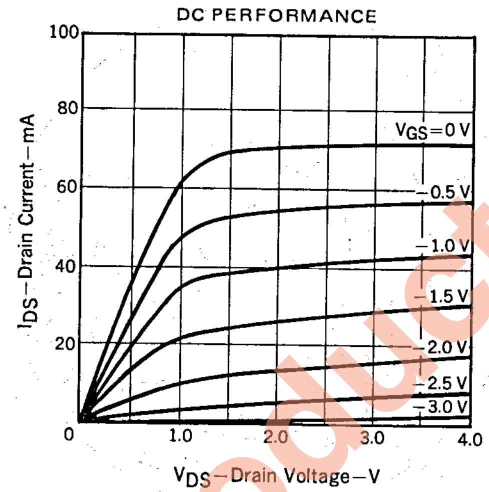
PERFORMANCE SPECIFICATIONS (T_a = 25 °C)

PART NUMBER		NE21800			NE21889			UNIT	TEST CONDITIONS	
PACKAGE CODE		00 (CHIP)			89					
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Maximum Frequency of Oscillation	$f_{max.}$		60			60		GHz	V_{DS} = 3 V, I_{DS} = 30 mA	
Maximum Available Gain *4	MAG		16.5			16.0		dB	V_{DS} = 4 V, I_{DS} = 30 mA	f = 4 GHz
			11.5			11.0		dB		f = 8 GHz
			9.5			9.0		dB		f = 12 GHz
Optimum Noise Figure	NF_{opt}		1.0	1.2		1.0	1.2	dB	V_{DS} = 3 V, I_{DS} = 10 mA	f = 4 GHz
			1.7			1.7		dB		f = 8 GHz
			2.8			2.8		dB		f = 12 GHz
Associated Gain at Optimum Noise Figure	G_a		13.0		12.0	13.0		dB	V_{DS} = 3 V, I_{DS} = 10 mA	f = 4 GHz
			10.5			12.0		dB		f = 8 GHz
			7.5			7.0		dB		f = 12 GHz
Output Power at 1 dB Gain Compression Point	$P_{O(1\,dB)}$		50			50		mW	V_{DS} = 4 V, I_{DS} = 30 mA	f = 4 GHz

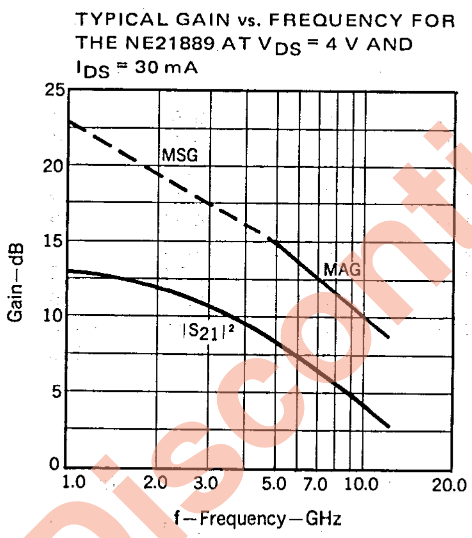
*4 Gain Calculations : $MAG = \frac{|S_{21}|}{|S_{12}|}(K \pm \sqrt{K^2 - 1})$, $K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{21}|}$, $\Delta = S_{11}S_{22} - S_{21}, S_{12}$; $MSG = \frac{|S_{21}|}{|S_{12}|}$

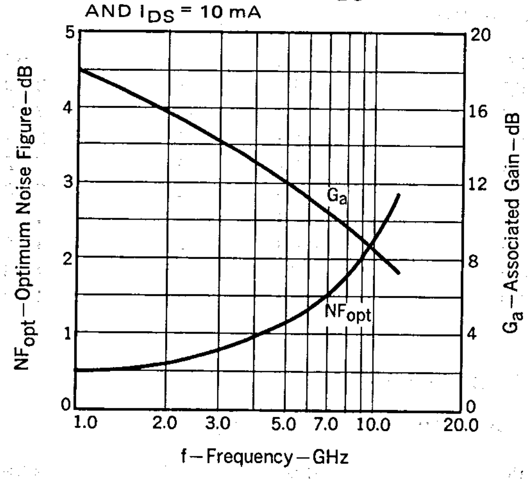
DEVICE CHARACTERISTICS



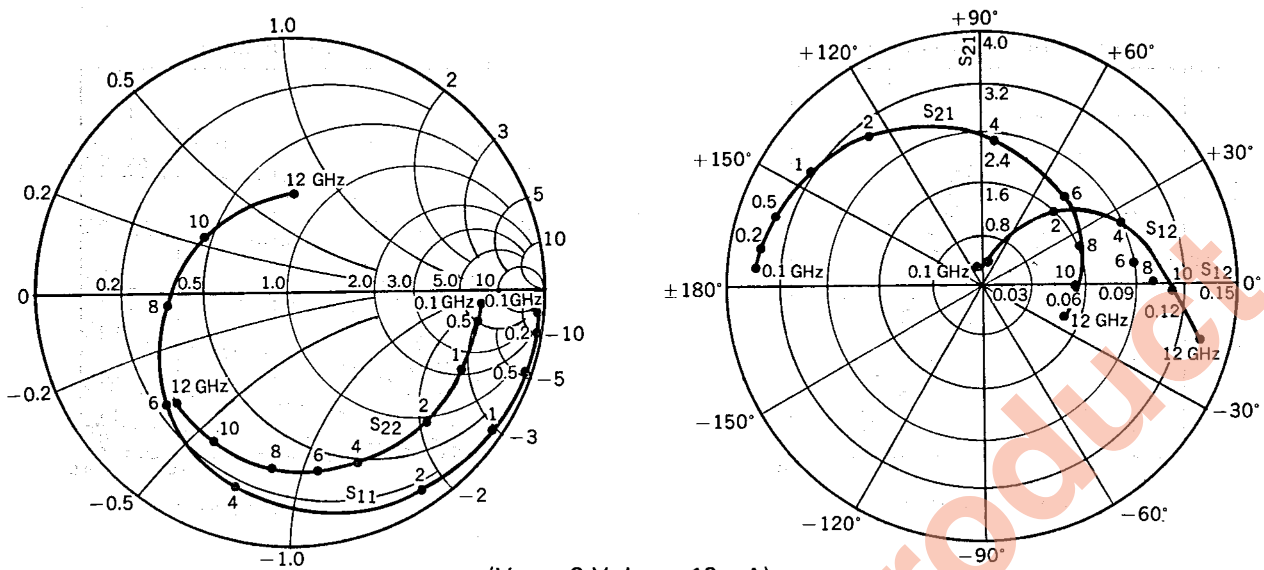


TYPICAL CHARACTERISTICS (T_a = 25 °C)





NE21889 S-PARAMETERS



(V$_{DS}$ = 3 V, I$_{DS}$ = 10 mA)

S-MAGN AND ANGLES

V_{DS} = 3 V, I_{DS} = 10 mA

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
100	0.98	−5	3.57	175	0.01	105	0.76	−3
200	0.98	−10	3.50	170	0.01	85	0.76	−6
500	0.98	−20	3.48	160	0.01	80	0.75	−12
1000	0.95	−35	3.23	145	0.03	65	0.75	−25
2000	0.92	−65	2.92	125	0.06	45	0.74	−40
4000	0.80	−105	2.32	85	0.09	25	0.72	−65
6000	0.66	−140	1.92	55	0.09	10	0.71	−80
8000	0.48	−176	1.64	20	0.10	1	0.70	−95
10000	0.42	145	1.38	0	0.11	−2	0.68	−115
12000	0.40	90	1.32	−25	0.13	−15	0.61	−135

V_{DS} = 4 V, I_{DS} = 30 mA

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
100	0.99	−7	4.89	175	0.01	75	0.71	−4
200	0.98	−10	4.79	170	0.01	75	0.71	−5
500	0.97	−20	4.73	160	0.01	75	0.70	−10
1000	0.94	−40	4.36	145	0.02	65	0.70	−25
2000	0.87	−70	3.81	120	0.03	60	0.69	−40
4000	0.74	−115	2.92	85	0.06	30	0.68	−60
6000	0.58	−150	2.30	50	0.07	25	0.67	−75
8000	0.42	170	1.89	20	0.08	20	0.66	−90
10000	0.40	125	1.56	−5	0.11	20	0.64	−110
12000	0.39	60	1.39	−35	0.14	−5	0.63	−130

CHIP HANDLING

DIE ATTACHMENT

Die attach can be accomplished with a Au-Sn (300±10 °C) preforms in a forming gas environment. Epoxy die attach is not recommended.

BONDING

Gate and drain bonding wires should be minimum length, semi-hard gold wire (3-8 % elongation) 20 microns or less in diameter.

Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Die attach and bonding time should be kept to a minimum. As a general rule, the bonding operation should be kept within a 280 °C – 5 minute curve. If longer periods are required, the temperature should be lowered.

PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

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