

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

Notice

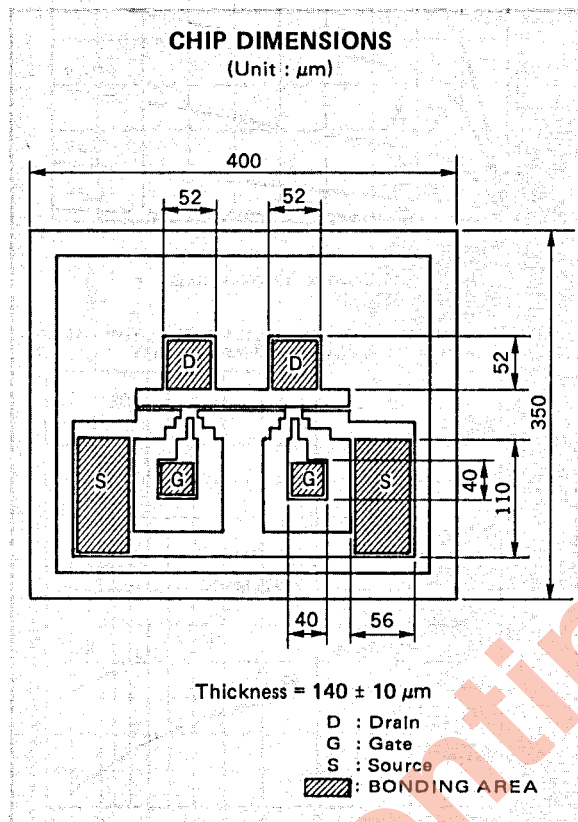
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HETERO JUNCTION FIELD EFFECT TRANSISTOR
NE21200

X to Ku BAND SUPER LOW NOISE FET
AlGaAs/GaAs HETERO JUNCTION FIELD EFFECT TRANSISTOR CHIP



FEATURES

- Super Low Noise Figure
NF = 1.0 dB TYP. at $f = 12 \text{ GHz}$
- High Associated Gain
 $G_a = 10.5 \text{ dB TYP. at } f = 12 \text{ GHz}$
- n^+ AlGaAs/Undoped GaAs Hetero Structure
- Gate Length: $L_g = 0.3 \mu\text{m}$
- Gate Width: $W_g = 200 \mu\text{m}$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DS}	4.0	V
Gate to Source Voltage	V_{GS}	-3.0	V
Drain Current	I_D	60	mA
Total Power Dissipation	P_{tot}^*	200	mW
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +175	$^\circ\text{C}$

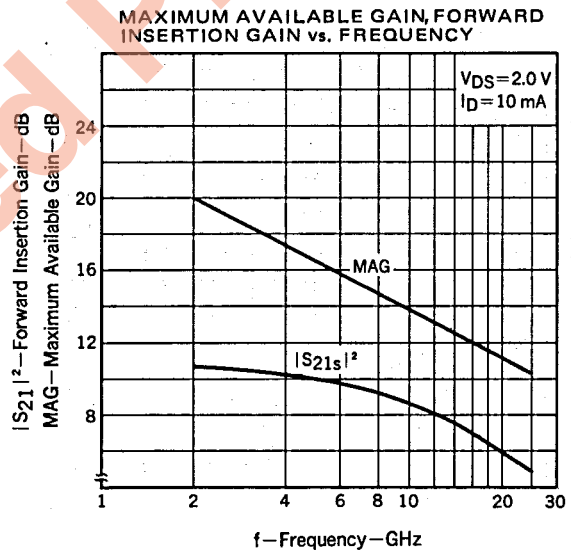
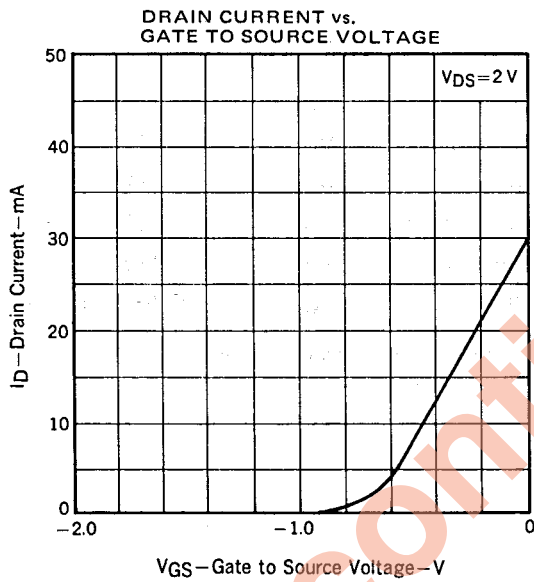
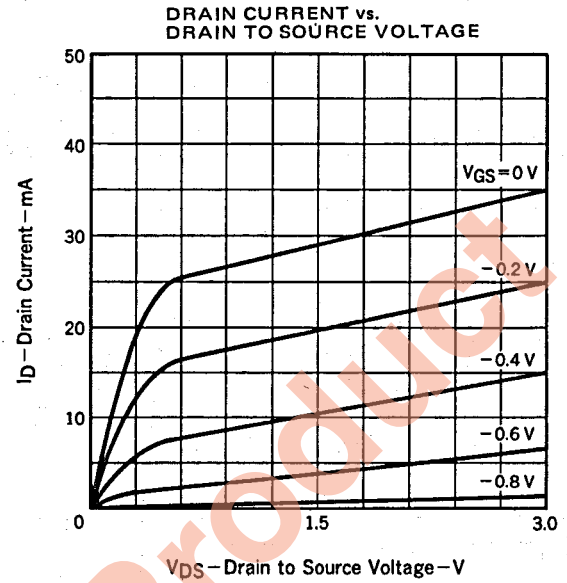
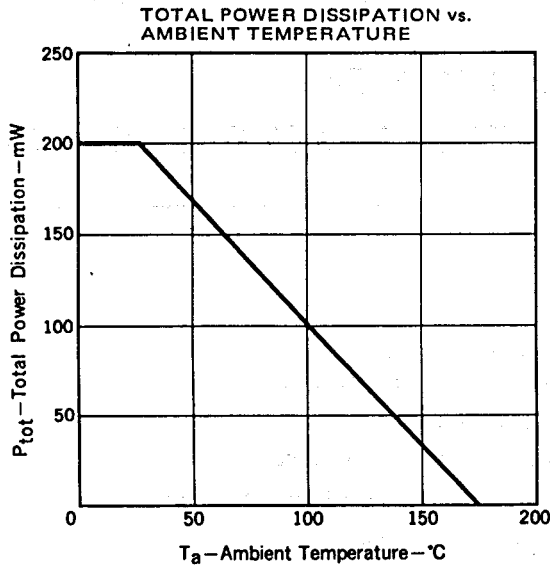
* : P_{tot} for chip mounted on a Alumina heatsink (size: $3 \times 3 \times 0.6^t \text{ mm}$)

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Gate to Source Leak Current	I_{GSO}		1	10	μA	$V_{GS} = -3 \text{ V}$
Saturated Drain Current	I_{DSS}	12	30	60	mA	$V_{DS} = 2 \text{ V}, V_{GS} = 0$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-0.2	-1.0	-2.0	V	$V_{DS} = 2 \text{ V}, I_D = 100 \mu\text{A}$
Transconductance	g_m	30	40		mS	$V_{DS} = 2 \text{ V}, I_D = 10 \text{ mA}$
Noise Figure	NF		1.0	1.2	dB	$V_{DS} = 2 \text{ V}, I_D = 10 \text{ mA}, f = 12 \text{ GHz}$
Associated Gain	G_a	10.0	10.5		dB	

Caution: Avoid high static voltage or electric fields, because this device is AlGaAs/GaAs Hetero junction field effect transistor with GaAs Schottky barrier gate.

TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

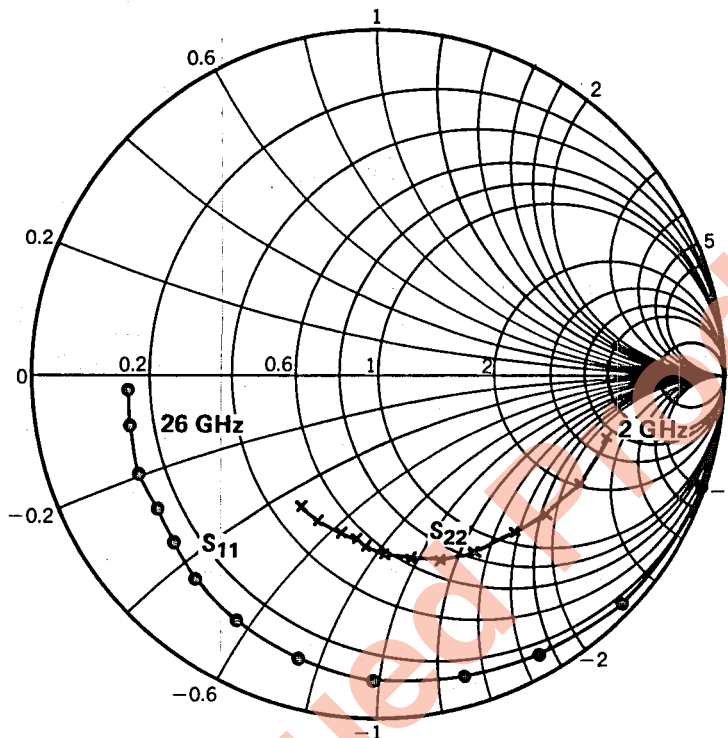


Discontinued Product

S-PARAMETERS

$V_{DS}=2\text{ V}$
 $I_D=10\text{ mA}$

START 2 GHz STOP 26 GHz STEP 2 GHz

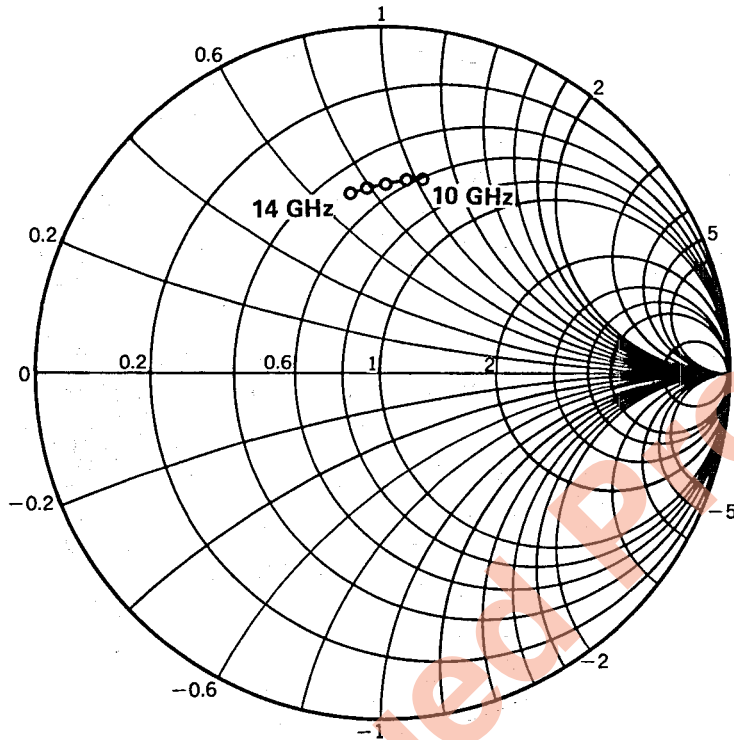


MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂		k	G _{max}
	MAG.	ANG. (deg.)	MAG.	ANG. (deg.)	MAG.	ANG. (deg.)	MAG.	ANG. (deg.)		
2000	0.986	-22	3.442	161	0.034	74	0.680	-15	0.09	20.0
4000	0.967	-43	3.270	144	0.063	61	0.654	-28	0.13	17.1
6000	0.938	-60	3.072	129	0.086	48	0.622	-40	0.22	15.5
8000	0.916	-74	2.867	116	0.100	39	0.603	-49	0.25	14.6
10000	0.894	-91	2.711	101	0.124	27	0.582	-62	0.27	13.4
12000	0.859	-106	2.546	88	0.138	20	0.565	-72	0.29	12.7
14000	0.824	-120	2.337	75	0.147	7	0.537	-81	0.40	12.0
16000	0.794	-132	2.206	63	0.152	0	0.523	-89	0.47	11.6
18000	0.762	-141	2.072	51	0.154	-10	0.502	-95	0.60	11.3
20000	0.748	-149	1.970	42	0.139	-14	0.483	-98	0.72	11.5
22000	0.753	-158	1.873	33	0.138	-16	0.472	-104	0.73	11.3
24000	0.740	-169	1.757	24	0.149	-18	0.460	-113	0.72	10.8
26000	0.730	-177	1.652	19	0.151	-22	0.449	-121	0.73	10.4

NOISE PARAMETERS

$V_{DS}=2.0\text{ V}$
 $I_D=10\text{ mA}$

START 10 GHz STOP 14 GHz STEP 1 GHz



Freq. (dB)	NF MIN. (dB)	Gain (dB)	Γ_{opt}		$R_n/50 (\Omega)$
			MAG.	ANG. (deg.)	
10.0	0.85	12.7	0.58	78	0.40
11.0	0.90	11.7	0.57	82	0.65
11.5	0.95	11.2	0.56	85	0.90
12.0	1.00	10.5	0.55	88	0.90
12.5	1.05	10.1	0.54	91	0.80
13.0	1.10	9.75	0.54	94	0.85
14.0	1.20	9.50	0.53	99	0.90

Γ_{opt} includes bond wired.

17.3 microns diameter gold wires used during testing.

Gate : 2 wires total, 1 per bond pad, 322 microns long each wire.

Drain : 2 wires total, 1 per bond pad, 398 microns long each wire.

Source : 6 wires total, 3 per side, 222 microns long each wire.

CHIP HANDLING**DIE ATTACHMENT**

Die attach operation can be accomplished with Au-Sn (within a 300 °C – 10 s) performs in a forming gas environment.

Epoxy die attach is not recommend.

BONDING

Bonding wires should be minimum length, semi hard gold wire (3–8 % elongation) 20 microns in diameter. Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Bonding time should be kept to a minimum.

As a general rule, the bonding operation should be kept within a 280 °C, 2 minutes for all bonding wires.

If longer periods are required, the temperature should be lowered.

PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Discontinued Product

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Discontinued Product

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