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April 1st, 2010
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RENESAS

MOS Integrated Circuit

V850ES/FJ2

32-bit single-chip micro controller

INTRODUCTION

The V850ES/FJ2 are 32-bit single-chip microcontrollers that include the V850ES CPU core and integrate peripheral functions such as timers/counters, serial interfaces, and an A/D converter. These microcontrollers also incorporate a CAN (Controller Area Network) as an automotive LAN.

In addition to highly real-time responsive, 1-clock-pitch basic instructions, these microcontrollers have instructions ideal for digital servo applications, such as multiplication instructions using a hardware multiplier, sum-of-products operation instructions, and bit manipulation instructions. These microcontrollers can also realize a real-time control system that is highly cost effective and can be used in automotive instrumentation fields.

FEATURES

- Number of instructions: 83
- Minimum instruction execution time: 50 ns (main clock (fxx) = 20 MHz)
- General-purpose registers: 32 bits × 32
- Power-on clear function
- Low-voltage detection function
- Ring-OSC: 200 kHz (TYP.)
- Internal memory:
    - RAM: 12/20 KB
    - Flash memory: 256/512KB
    - Mask ROM: 64/128KB
- Interrupts/exceptions :
    - Non-maskable interrupts : 1 source
    - Maskable interrupts : 72/82 sources
    - Software exceptions: 2 sources
    - Exception trap: 1 source
- I/O lines I/O ports: 128
- Timer/counters:
    - 16-bit interval timer M (TMM): 1 ch
    - 16-bit timer/event counter P (TMP): 4 ch
    - 16-bit timer/event counter Q (TMQ): 3 ch
- Watch timer: 1 ch
- Watchdog timer 2: 1 ch
- Serial interface (SIO):
    - Asynchronous serial interface A (UART): 3 ch
    - 3-wire variable-length serial interface B (CSIB): 3/4 ch
- CAN controller: 2/4 ch
- A/D converter 10-bit resolution: 24 ch
- Clock generator Main clock/subclock operation:
    - CPU clock in seven steps (fxx, fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxt)
    - Clock-through mode/PLL mode selectable
    - Internal oscillator: 200 kHz (TYP.)
- Power save function: HALT/IDLE1/IDLE2/software STOP/subclock/sub-IDLE modes
- Package: 144-pin plastic LQFP (fine pitch) (20 × 20)

Part Number	Internal ROM	Internal RAM	CAN I/F
uPD70F3237	256KB (Flash)	12KB	2 channel
UPD70F3238	376KB (Flash)	20KB	4 channel
uPD70F3239	512KB (Flash)	20KB	4 channel

Table of Contents

1. Electrical Specification 4
1.1 Electrical Specifications of (A)-Grade 4
1.1.1 Absolute maximum ratings 4
1.1.2 Capacitance 6
1.1.3 Operating conditions 6
1.1.4 Oscillator Characteristics 7
1.1.5 PLL Characteristics 9
1.1.6 Ring-OSC Characteristics 9
1.1.7 Voltage Regulator Characteristics 9
1.1.8 DC Characteristics 10
1.1.9 Data Retention Characteristics 16
1.1.10 AC Characteristics 17
1.2 Electrical Specifications of (A1)-Grade 33
1.2.1 Absolute maximum ratings 33
1.2.2 Capacitance 35
1.2.3 Operating conditions 35
1.2.4 Oscillator Characteristics 36
1.2.5 PLL Characteristics 38
1.2.6 Ring-OSC Characteristics 38
1.2.7 Voltage Regulator Characteristics 38
1.2.8 DC Characteristics 39
1.2.9 Data Retention Characteristics 44
1.2.10 AC Characteristics 45
1.3 Electrical Specifications of (A2)-Grade 61
1.3.1 Absolute maximum ratings 61
1.3.2 Capacitance 63
1.3.3 Operating conditions 63
1.3.4 Oscillator Characteristics 64
1.3.5 PLL Characteristics 66
1.3.6 Ring-OSC Characteristics 66
1.3.7 Voltage Regulator Characteristics 66
1.3.8 DC Characteristics 67
1.3.9 Data Retention Characteristics 72
1.3.10 AC Characteristics 73
2. Injected Current Specification 89
2.1 Injected Current Specification of (A)-Grade 89
2.1.1 Absolute Maximum Ratings 89
2.1.2 DC Characteristics for overload current 89
2.1.3 DC Characteristics for pins influenced by injected current on an adjacent pin 90
2.1.4 A/D converter influenced by injected current on an adjacent pin 91
2.2 Injected Current Specification of (A1)-Grade 92
2.2.1 Absolute Maximum Ratings 92
2.2.2 DC Characteristics for overload current 92
2.2.3 DC Characteristics for pins influenced by injected current on an adjacent pin 93
2.2.4 A/D converter influenced by injected current on an adjacent pin 94
2.3 Injected Current Specification of (A2)-Grade 95

2.3.1 Absolute Maximum Ratings 95
2.3.2 DC Characteristics for overload current 95
2.3.3 DC Characteristics for pins influenced by injected current on an adjacent pin 96
2.3.4 A/D converter influenced by injected current on an adjacent pin 97
3. Package Drawing 98
Figure 3-1: Package Drawing 98
4. Recommended Soldering Conditions 99
Table 4-1: Soldering Conditions 99

1. Electrical Specification

1.1 Electrical Specifications of (A)-Grade

1.1.1 Absolute maximum ratings

Absolute maximum ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	BV_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	EV_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	AV_{REF0}		−0.5 to +6.5	V
	V_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	BV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	EV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 Note	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6		
	V_{I2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	−0.5 to BV_{DD} + 0.5 Note	V
	V_{I3}	X1, X2, XT1, XT2	−0.5 to V_{RO} + 0.5 Note	V
Analog input voltage	V_{IAN}	P70 to P715, P120 to P127	−0.5 to AV_{REF0} + 0.5 Note	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	Per pin	4	mA
			Total of all pins	50	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6			
		P70 to P715, P120 to P127	Per pin	4	mA
			Total of all pins	20	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	Per pin	4	mA
			Total of all pins	50	mA
Output current, high	I_{OH}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	Per pin	−4	mA
			Total of all pins	−50	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6			
		P70 to P715, P120 to P127	Per pin	−4	mA
			Total of all pins	−20	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	Per pin	−4	mA
			Total of all pins	−50	mA
Operating ambient temperature	T_A	Normal operating mode		−40 to +85	°C
		Flash programming mode			
Storage temperature	T_{stg}			−40 to +125	°C

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.1.2 Capacitance

(T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	f_X = 1 MHz, Unmeasured pins returned to 0 V.			10	pF

1.1.3 Operating conditions

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

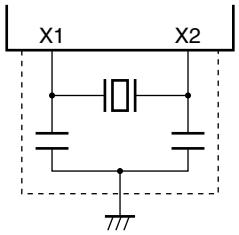
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC Capacity = 4.7 μF, at operation with main clock	4		20	MHz
		REGC Capacity = 4.7 μF, at operation with subclock (crystal resonator)	32		35	kHz
		REGC Capacity = 4.7 μF, at operation with subclock (RC resonator)	12.5 Note		27.5 Note	kHz

Note The internal system clock frequency is half the oscillation frequency.

1.1.4 Oscillator Characteristics

Main clock oscillator characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1		4		5	MHz
		Oscillation stabilization time Note 2	After reset release		$2^{16}/f_X$		s
			After STOP mode release	0.5 Note 3	Note 4		ms
			After IDLE2 mode release	0.35	Note 4		ms
Crystal resonator		Oscillation frequency (f_X) Note 1		4		5	MHz
		Oscillation stabilization time Note 2	After reset release		$2^{16}/f_X$		s
			After STOP mode release	0.5 Note 3	Note 4		ms
			After IDLE2 mode release	350	Note 4		μs

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the crystal resonator after reset or STOP mode is released.

3. Time required to stabilize access to the internal flash memory.

4. The value differs depending on the OSTS register settings.

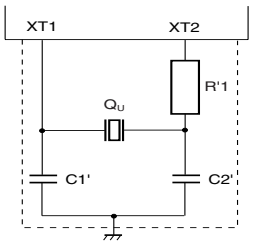
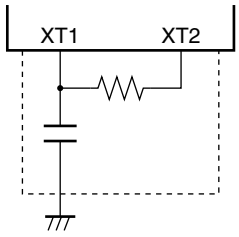
Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock oscillator characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator Note 5		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2				10	s
RC resonator		Oscillation frequency (f_{XT}) Notes 1, 4	R = 390 kΩ ±5% Note 3 C = 47 pF ±10% Note 3	25	40	55	kHz
		Oscillation stabilization time Note 2				100	μs

Notes 1. Indicates only oscillator characteristics. Refer to **28. 1. 10 AC Characteristics** for CPU operating clock.

2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).

5. The values of capacitors C1', C2' and resistors R'1 depend on the resonator used and must be specified in cooperation with the manufacturer.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.1.5 PLL Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		4		5	MHz
Output frequency	f_{xx}		16		20	MHz
Clock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			800	μs

1.1.6 Ring-OSC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

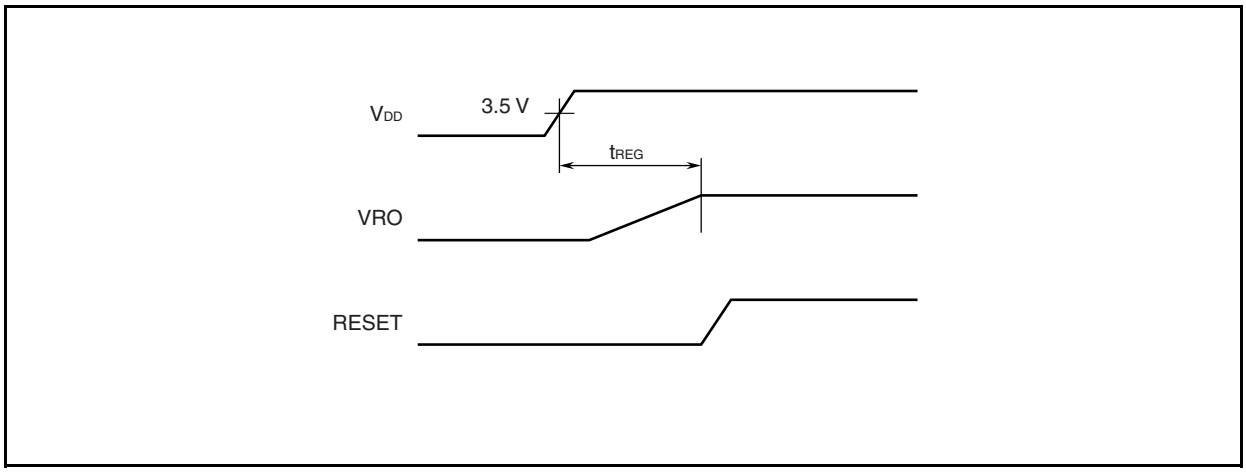
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_r		100	200	400	kHz

1.1.7 Voltage Regulator Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{DD}		3.5		5.5	V
Output voltage	V_{RO}			2.5		V
Lock time[Note 1]	t_{REG}	After V_{DD} reaches MIN.: 3.5 V Connect C = 4.7 μF ± 20% to REGC pin			1	ms

Note 1. The lock time does not have to be considered for devices that have POC.



1.1.8 DC Characteristics

(1) Input/Output level

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P30, P34, P36 to P38, P41, P63 to P69, P614, P615, P81, P98, P911 PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6	0.7EV_{DD}		EV_{DD}	V
	V_{IH2}	P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P60 to P62, P610 to P613, P80, P90 to P97, P99, P910, P912 to P915	0.8EV_{DD}		EV_{DD}	V
	V_{IH3}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	0.7BV_{DD}		BV_{DD}	V
	V_{IH4}	P70 to P715, P120 to P127	0.7AV_{REF0}		AV_{REF0}	V
	V_{IH5}	$\overline{RESET}$, FLMD0	0.8EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL1}	P30, P34, P36 to P38, P41, P63 to P69, P614, P615, P81, P98, P911 PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6	EV_{SS}		0.3EV_{DD}	V
	V_{IL2}	P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P60 to P62, P610 to P613, P80, P90 to P97, P99, P910, P912 to P915	EV_{SS}		0.2EV_{DD}	V
	V_{IL3}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	BV_{SS}		0.3BV_{DD}	V
	V_{IL4}	P70 to P715, P120 to P127	AV_{SS}		0.3AV_{REF0}	V
	V_{IL5}	$\overline{RESET}$, FLMD0	EV_{SS}		0.2EV_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high[Note 1]	V_{OH1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80 to P81, P90 to P915	I_{OH} = –1.0 mA	EV_{DD} – 1.0		EV_{DD}	V
			I_{OH} = –0.1 mA	EV_{DD} – 0.5		EV_{DD}	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6					
	V_{OH2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	I_{OH} = –1.0 mA	BV_{DD} – 1.0		BV_{DD}	V
			I_{OH} = –0.1 mA	BV_{DD} – 0.5		BV_{DD}	V
	V_{OH3}	P70 to P715, P120 to P127	I_{OH} = –1.0 mA	AV_{REF0} – 1.0		AV_{REF0}	V
			I_{OH} = –0.1 mA	AV_{REF0} – 0.5		AV_{REF0}	V
Output voltage, low[Note 1]	V_{OL1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	I_{OL} = 1.0 mA	0		0.4	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6					
	V_{OL2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	I_{OL} = 1.0 mA	0		0.4	V
	V_{OL3}	P70 to P715, P120 to P127	I_{OL} = 1.0 mA	0		0.4	V
Pull-up resistor	R_1	V_I = 0 V		10	30	100	kΩ
Pull-down resistor[Note 2]	R_2	V_I = V_{DD}		10	30	100	kΩ

Notes 1. Total IOH/IOL (Max.) is 20 mA/-20 mA each power supply terminal (EVDD, BVDD and AVREF0).

2. $\overline{\text{DRST}}$ pin only (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Analog pins			+0.2	μA
			Other pins Note 1			+0.5	
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Analog pins			–0.2	μA
			Other pins Note 1			–0.5	
Output leakage current, high	I_{LOH1}	V_O = V_{DD}	Analog pins			+0.2	μA
			Other pins			+0.5	
Output leakage current, low	I_{LOL1}	V_O = 0 V	Analog pins			–0.2	μA
			Other pins			–0.5	

Note 1. For flash memory product, specification of FLMD0 is as follows:

Input leakage current, high: 2 μA

Input leakage current, low: –2 μA

(3) Supply current

Supply current (V850ES/FJ2: μPD70F3239, μPD70F3238)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current Note 1	I_{DD1}	Normal operation	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		40	55	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		27		mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		25	35	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		14		mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.6	0.9	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.7	mA
	I_{DD5}	Subclock operation mode Notes 2, 3	Crystal resonator f_{XT} = 32.768 kHz		200	400	μA
			RC resonator f_{XT} = 40 kHz Note 4		200	400	μA
	I_{DD6}	Sub-IDLE mode Notes 2, 3	Crystal resonator f_{XT} = 32.768 kHz		20	120	μA
			RC resonator f_{XT} = 40 kHz Note 4		35	140	μA
	I_{DD7}	Stop mode Notes 2, 5	POC stopped, Ring-OSC stopped		7	50	μA
			POC operating, Ring-OSC stopped		10	55	μA
			POC stopped, Ring-OSC operating		15	65	μA
			POC operating, Ring-OSC operating		18	70	μA

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).
The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.

3. POC operating, Ring-OSC operating.

4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.

5. When the sub-OSC is not used.

Supply current (V850ES/FJ2: μPD70F3237)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current Note 1	I_{DD1}	Normal operation	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		30	45	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		22		mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		18	28	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		11		mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.6	0.9	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.7	mA
	I_{DD5}	Subclock operation mode Notes 2, 3	Crystal resonator f_{XT} = 32.768 kHz		200	400	μA
			RC resonator f_{XT} = 40 kHz Note 4		200	400	μA
	I_{DD6}	Sub-IDLE mode Notes 2, 3	Crystal resonator f_{XT} = 32.768 kHz		20	120	μA
			RC resonator f_{XT} = 40 kHz Note 4		35	140	μA
	I_{DD7}	Stop mode Notes 2, 5	POC stopped, Ring-OSC stopped		7	50	μA
			POC operating, Ring-OSC stopped		10	55	μA
			POC stopped, Ring-OSC operating		15	65	μA
			POC operating, Ring-OSC operating		18	70	μA

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).
The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.

3. POC operating, Ring-OSC operating.

4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.

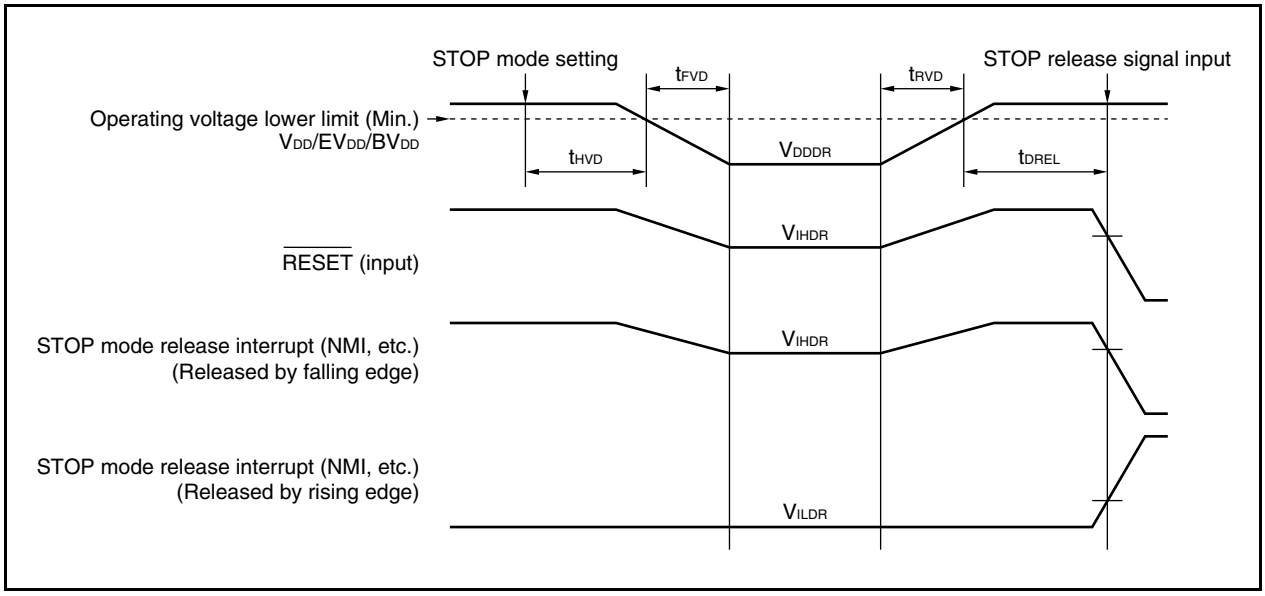
5. When the sub-OSC is not used.

1.1.9 Data Retention Characteristics

STOP Mode (T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 1.9 V to 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

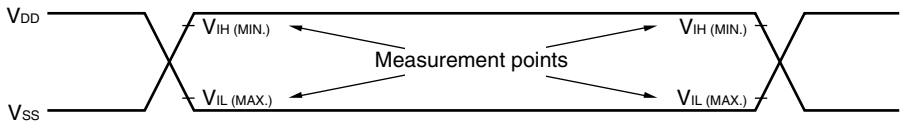
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	In STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.0 V		10	40	μA
Supply voltage rise time	t_{RVD}		1			μs
Supply voltage fall time	t_{FVD}		1			μs
Supply voltage retention time	t_{HVD}	After STOP mode release	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches MIN.: 3.5 V	0			μs
Data retention input voltage, high	V_{IHDR}	All input ports	0.9V_{DDDR}		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	All input ports	0		0.1V_{DDDR}	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

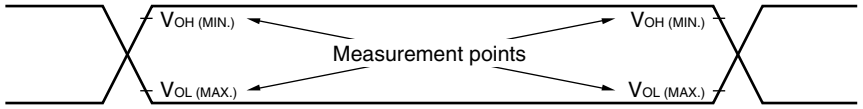


1.1.10 AC Characteristics

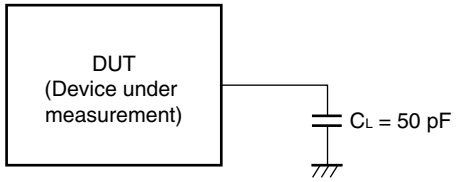
AC Test Input Measurement Points (V_{DD}, AV_{DD}, EV_{DD}, BV_{DD})



AC Test Output Measurement Points



Load Conditions



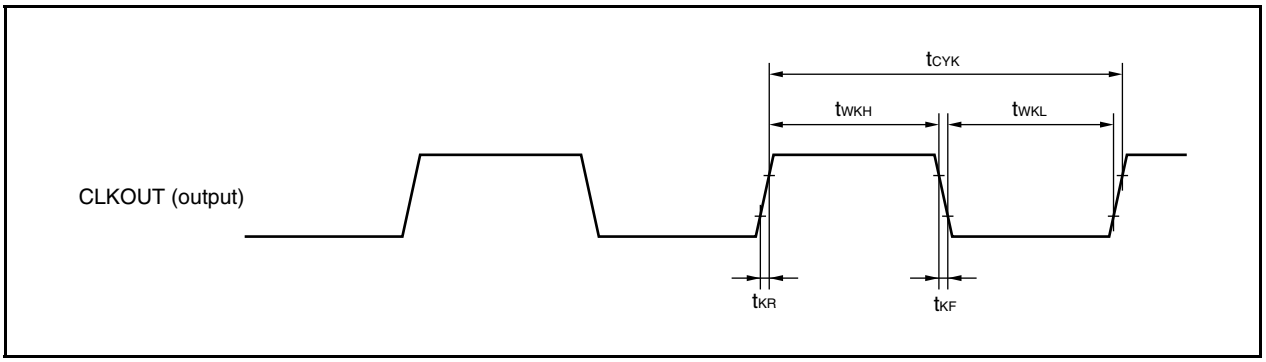
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

(1) CLKOUT output timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}		50 ns	80 μs	
High-level width	t_{WKH}		t_{CYK}/2 – 15		ns
Low-level width	t_{WKL}		t_{CYK}/2 – 15		ns
Rise time	t_{KR}			15	ns
Fall time	t_{KF}			15	ns

Clock Timing



(2) Bus timing

(a) CLKOUT asynchronous: In multiplex bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}		$(0.5 + t_{ASW})T - 20$		ns
Address hold time (from ASTB↓)	t_{HSTA}		$(0.5 + t_{AHW})T - 15$		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}			16	ns
Data input setup time from address	t_{SAID}			$(2 + n + t_{ASW} + t_{AHW})T - 40$	ns
Data input setup time from $\overline{RD}$↓	t_{SRDID}			$(1 + n)T - 30$	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{WRm}$↓	$t_{DSTRDWR}$		$(0.5 + t_{AHW})T - 15$		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}		0		ns
Address output time from $\overline{RD}$↑	t_{DRDA}		$(1 + i)T - 15$		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$		$0.5T - 15$		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}		$(1.5 + i + t_{ASW})T - 15$		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}		$(1 + n)T - 15$		ns
ASTB high-level width	t_{WSTH}		$(1 + i + t_{ASW})T - 15$		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}			15	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}		$(1 + n)T - 20$		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}		$T - 15$		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	$n \geq 1$		$(1.5 + t_{ASW} + t_{AHW})T - 45$	ns
	t_{SAWT2}			$(1.5 + n + t_{ASW} + t_{AHW})T - 45$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	$n \geq 1$	$(0.5 + n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}		$(1.5 + n + t_{ASW} + t_{AHW})T$		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	$n \geq 1$		$(1 + t_{AHW})T - 35$	ns
	t_{SSTWT2}			$(1 + n + t_{AHW})T - 35$	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	$n \geq 1$	$(n + t_{AHW})T$		ns
	t_{HSTWT2}		$(1 + n + t_{AHW})T$		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}		$T + 10$		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}		$T - 20$		ns
Delay time from $\overline{HLDAK}$↑ to bus output	t_{DHAC}		–3		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}			$(2n + 7.5)T + 25$	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}		$0.5T$	$1.5T + 35$	ns

Remarks 1. $T = 1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. m = 0, 1

4. i: Number of idle states inserted after a read cycle (0 or 1).

5. The values in the above specifications are values for when clocks with a 1: 1 duty ratio are input from X1.

6. t_{ASW}: Number of address setup wait clocks (0 or 1).
t_{AHW}: Number of address hold wait clocks (0 or 1).

Caution : When the operating frequency is high, it is not possible to access without a bus wait cycle. Please insert a wait clock ((data wait (n) / address setup wait (t_{ASW}) / address hold wait (t_{AHW}))

(b) CLKOUT synchronous: In multiplex bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

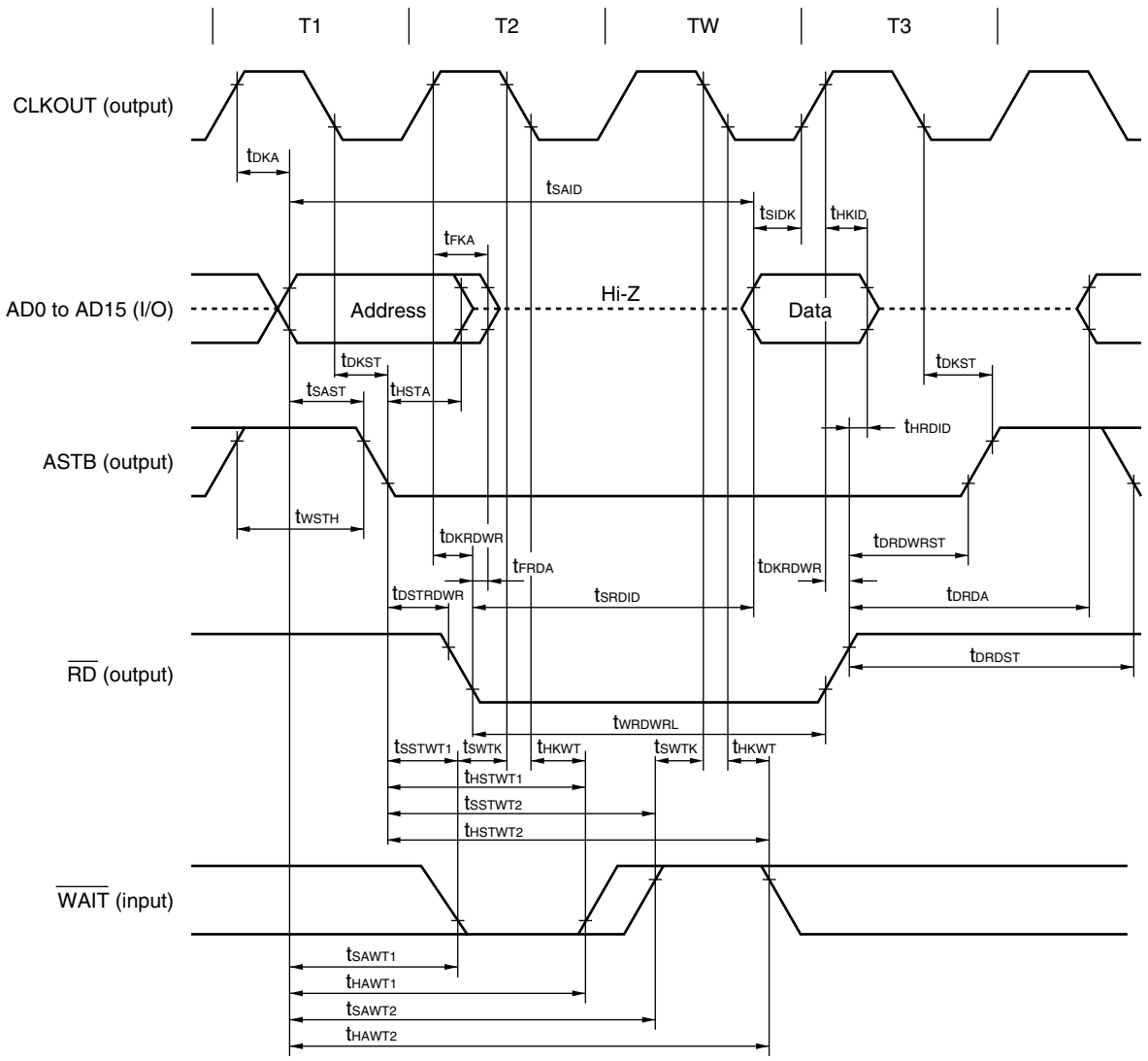
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}		0	24	ns
Delay time from CLKOUT↑ to address float	t_{FKA}		0	24	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}		–12	+12	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}		–5	+14	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	t_{HKID}		5		ns
Data output delay time from CLKOUT↑	t_{DKOD}			22	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}		30		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}		30		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}			24	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}			25	ns

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

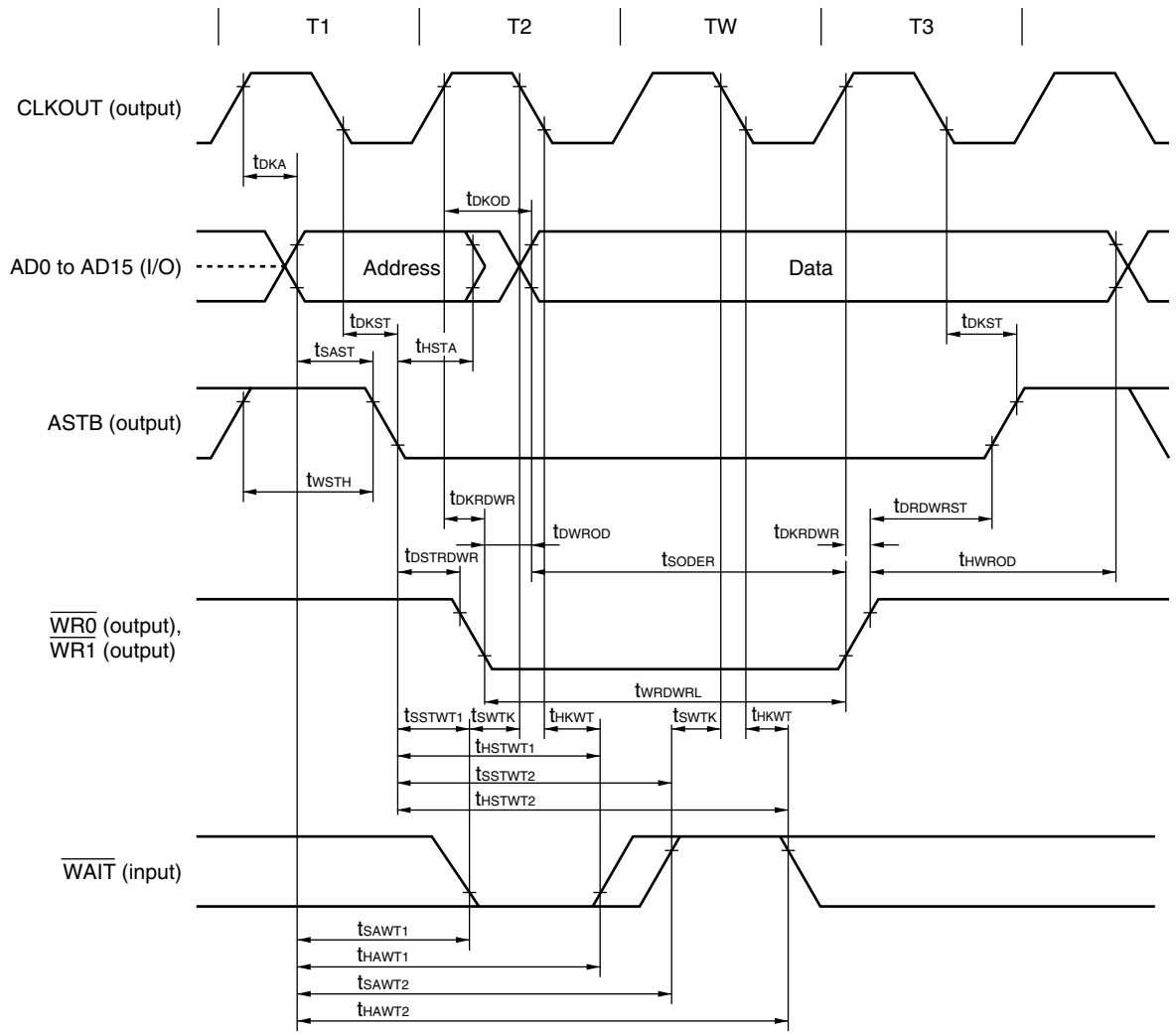
Caution : When the operating frequency is high, it is not possible to access without a bus wait cycle. Please insert a wait clock ((data wait (n) / address setup wait (t_{ASW}) / address hold wait (t_{AHW})).

Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



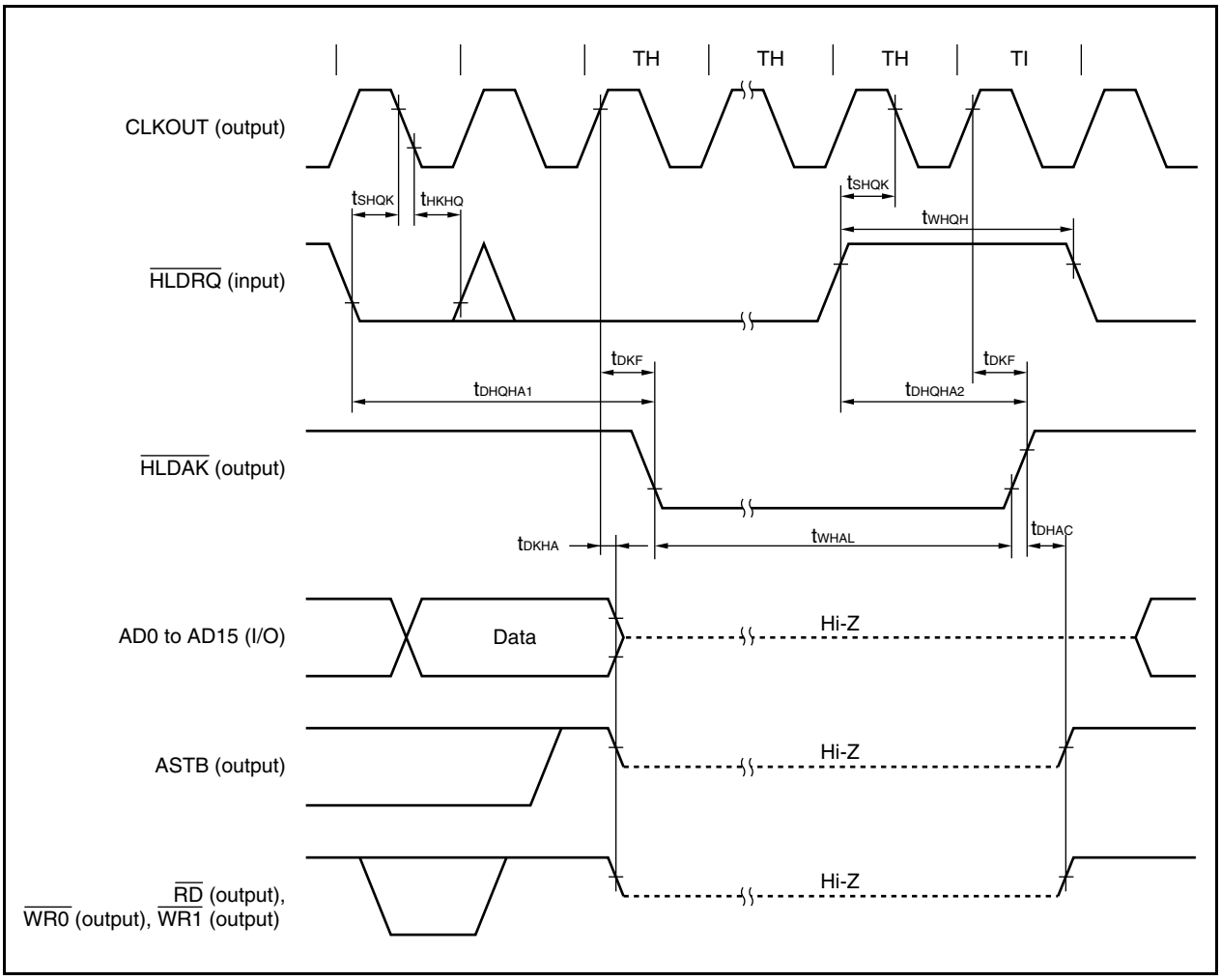
Remark $\overline{WR0}$ and $\overline{WR1}$ are high level.

Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



Remark $\overline{RD}$ is high level.

Bus Hold: In Multiplex Bus Mode



(3) Basic Operation

(a) Reset, Interrupt timing

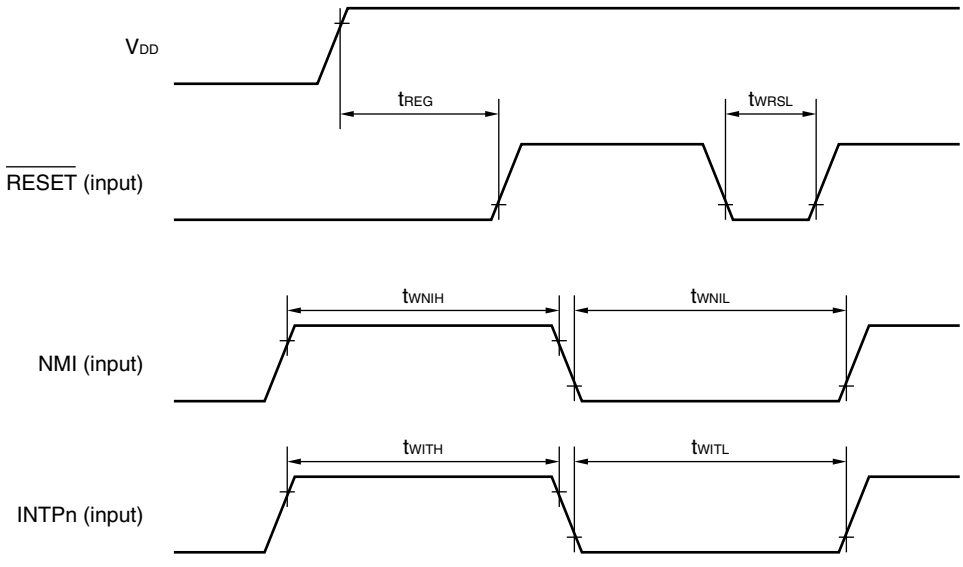
(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		500		ns
NMI high-level width	t_{WNIH}	Analog noise elimination	500		ns
NMI low-level width	t_{WNIL}	Analog noise elimination	500		ns
INTPn[Note 1] high-level width	t_{WITH}	Analog noise elimination (n = 0 to 14)	500		ns
		Digital noise elimination (n = 3)	**Note 2**		ns
INTPn[Note 1] low-level width	t_{WITL}	Analog noise elimination (n = 0 to 14)	1		ns
		Digital noise elimination (n = 3)	**Note 2**		ns

Notes 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/DRST).

2. 2Tsamp + 20 or 3Tsamp + 20
Tsamp: Sampling clock for noise elimination

Reset/Interrupt

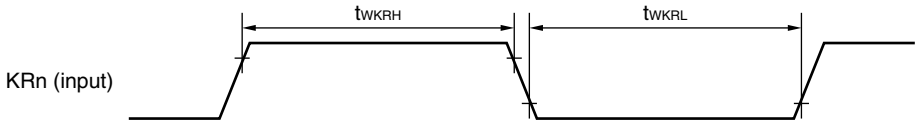


Remark n = 0 to 14

(b) Key return timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
KRn input high-level width	t_{WKRH}	Analog noise elimination (n = 0 to 14)	500		ns
KRn input low-level width	t_{WKRL}		500		ns



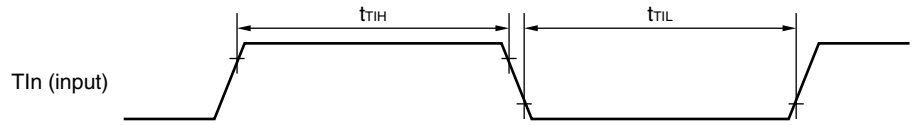
Remark n = 0 to 14

(c) Timer input timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TIn high-level width	t_{TIH}	TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03, TIQ10 to TIQ13, TIQ20 to TIQ23	**Note**		ns
TIn low-level width	t_{TIL}		**Note**		ns

Note 2Tsamp + 20 or 3Tsamp + 20
Tsamp: Sampling clock for noise elimination



Remark TIn: TIP00, TIP01, TIP10 TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03, TIQ10 to TIQ13, TIQ20 to TIQ23

(d) CSIB timing

(i) Master mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCYn}		125		ns
$\overline{SCKBn}$ high-level width	t_{KHn}		$t_{KCYn}/2 - 15$		ns
$\overline{SCKBn}$ low-level width	t_{KLn}		$t_{KCYn}/2 - 15$		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		30		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{KSIn}		25		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	t_{KSOn}			25	ns

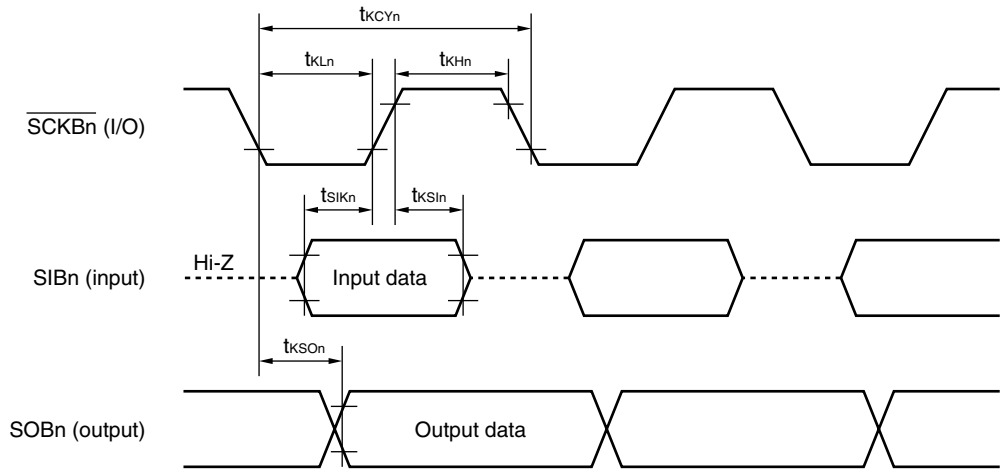
Remark n = 0 to 2

(ii) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCYn}		200		ns
$\overline{SCKBn}$ high-level width	t_{KHn}		90		ns
$\overline{SCKBn}$ low-level width	t_{KLn}		90		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		50		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{KSIn}		50		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	t_{KSOn}			50	ns

Remark n = 0 to 2



Remark n = 0 to 4

*CAN internal clock (fCAN): CAN baud rate clock

(e) UART timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

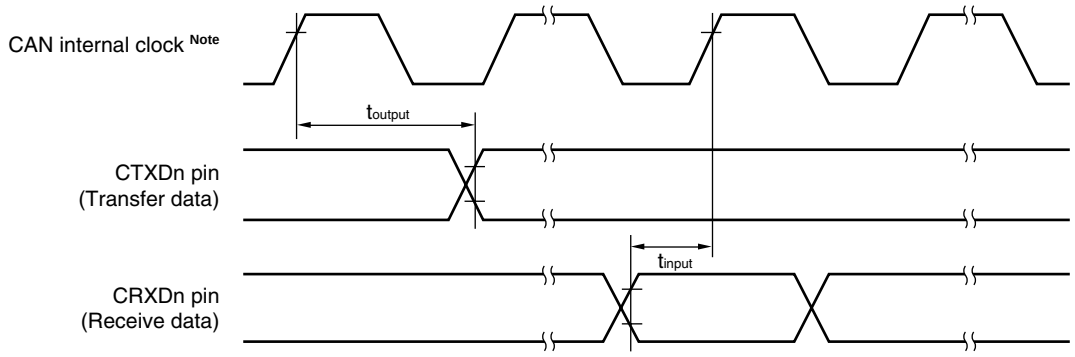
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Communication rate				312.5	kbps
ASCK0 cycle time				10	MHz

(f) CAN timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate				1	Mbps
Internal delay time[Note]				100	ns

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



Note *CAN internal clock (fCAN): CAN baud rate clock

Remark n = 0 to 3

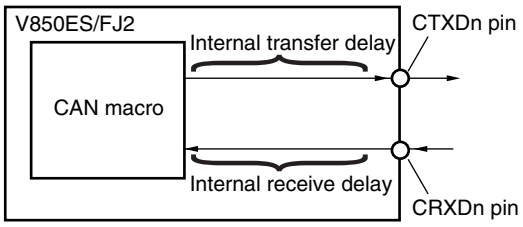


Image figure of internal delay

Remark n = 0 to 3

(g) A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		4.0 ≤ AV_{REF0} ≤ 5.5 V		±0.15	±0.3	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV_{REF0} current	I_{AREF0}	When using A/D converter		5	10	mA
		When not using A/D converter		1	10	μA

Note Excluding quantization error (±0.05%FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

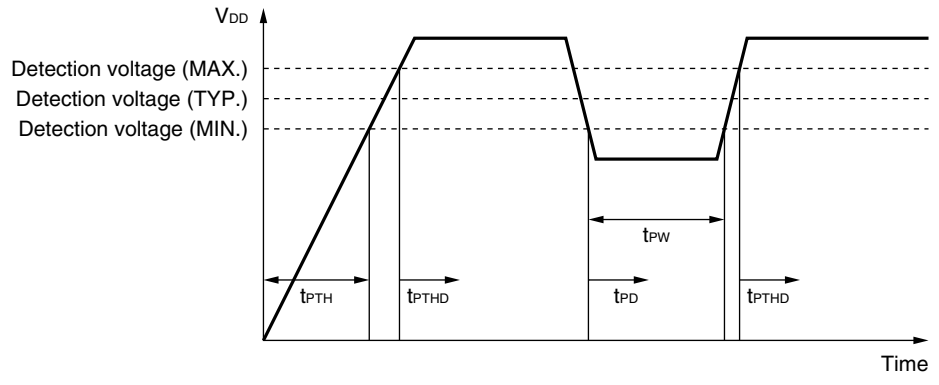
(h) POC circuit characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		3.5	3.7	3.9	V
Power supply startup time	t_{PTH}	V_{DD} = 0 V → 3.5 V	0.002			ms
Response delay time 1[Note 1]	t_{PTHD}	In case of power on. After V_{DD} reaches 3.9 V.			3.0	ms
Response delay time 2[Note 2]	t_{PD}	In case of power off. After V_{DD} drops 3.5 V.			1	ms
Minimum V_{DD} width	t_{PW}		0.2			ms

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.



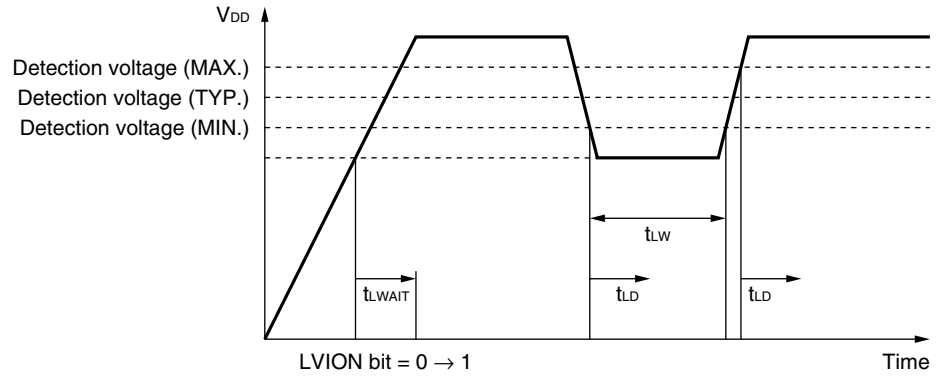
(i) LVI circuit characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.2	4.4	4.6	V
	V_{LVI1}		4.0	4.2	4.4	V
Response time Note 1	t_{LD}	After V_{DD} reaches V_{LVI0}/V_{LVI1} (Max.). After V_{DD} drops V_{LVI0}/V_{LVI1} (Min.).		0.2	2.0	ms
Minimum V_{DD} width	t_{LW}		0.2			ms
Reference voltage stabilization wait time Note 2	t_{LWAIT}	After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 →1		0.1	0.2	ms

Notes 1. The time required to output an interrupt/reset after the detection voltage is detected.

2. Unnecessary when the POC function is used.

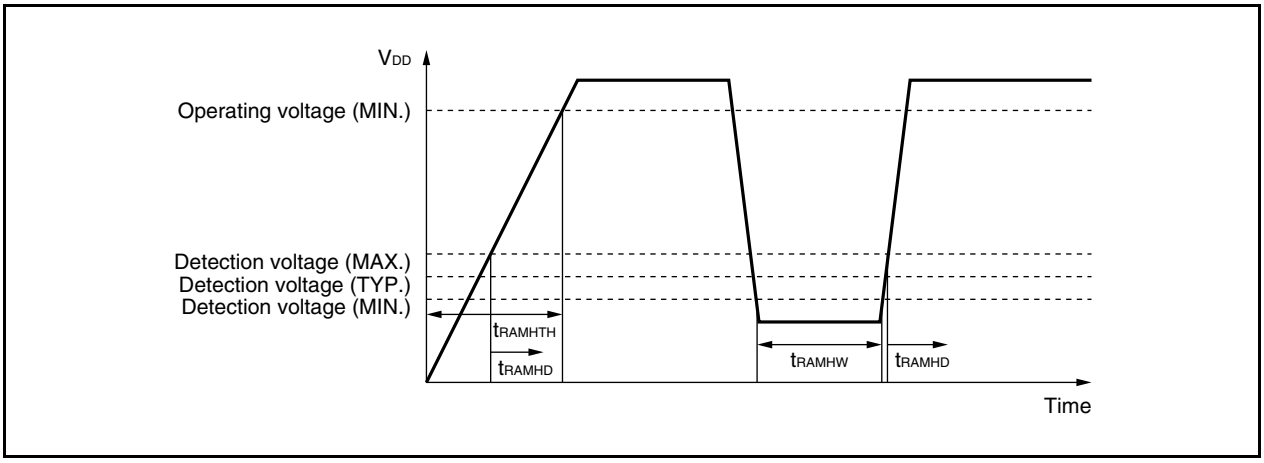


(j) RAM retention flag characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 1.9 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{RAMH}		1.9	2.0	2.1	V
Supply voltage rise time	t_{RAMHTH}	V_{DD} = 0 V → 3.5 V	0.002		1,800	ms
Response time[Note]	t_{RAMHD}	After the supply voltage reaches the detection voltage (MAX.)		0.2	2.0	ms
Minimum V_{DD} width	t_{RAMHW}		0.2			ms

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{CPU}		4		20	MHz
Supply voltage	V_{DD}		3.5		5.5	V
Number of writes	C_{WRT} Note				100	Times
Input voltage, high	V_{IH}	FLMD0	0.8EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL}	FLMD0	EV_{SS}		0.2EV_{DD}	V
Write time + erase time	t_{IWRT} + t_{ERASE}	Flash: 256 KB (μPD70F3237) 512 KB (μPD70F3239)			T.B.D	s
Programming temperature	t_{PRG}		–40		+85	°C

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

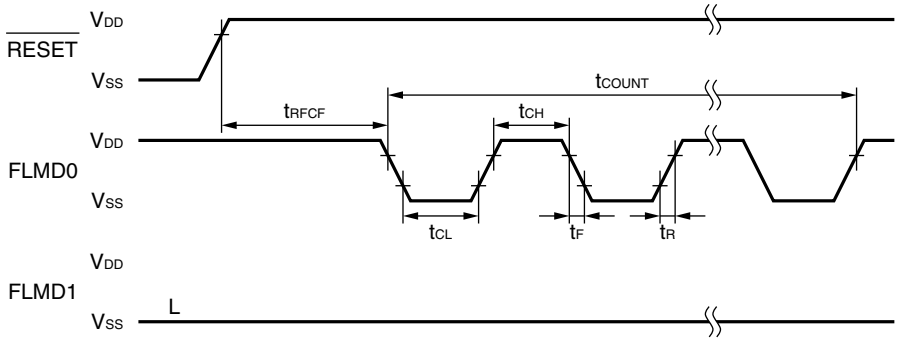
Example: P: Write, E: Erase
Shipped product → P → E → P → E → P: 3 rewrites
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time from $\overline{\text{RESET}}$↑	t_{RFCF}		5000/fx+ Note			s
Count execution time	t_{COUNT}				3	ms
FLMD0 high-level width	t_{CH}		10		100	μs
FLMD0 low-level width	t_{CL}		10		100	μs
FLMD rise time	t_R				50	ns
FLMD fall time	t_F				50	ns

Note " " represents the oscillation stabilization time.



1.2 Electrical Specifications of (A1)-Grade

1.2.1 Absolute maximum ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	BV_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	EV_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	AV_{REF0}		−0.5 to +6.5	V
	V_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	BV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	EV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 Note	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6		
	V_{I2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	−0.5 to BV_{DD} + 0.5 Note	V
	V_{I3}	X1, X2, XT1, XT2	−0.5 to V_{RO} + 0.5 Note	V
Analog input voltage	V_{IAN}	P70 to P715, P120 to P127	−0.5 to AV_{REF0} + 0.5 Note	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	Per pin	4	mA
			Total of all pins	50	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6			
		P70 to P715, P120 to P127	Per pin	4	mA
			Total of all pins	20	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	Per pin	4	mA
			Total of all pins	50	mA
Output current, high	I_{OH}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	Per pin	−4	mA
			Total of all pins	−50	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6			
		P70 to P715, P120 to P127	Per pin	−4	mA
			Total of all pins	−20	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	Per pin	−4	mA
			Total of all pins	−50	mA
Operating ambient temperature	T_A	Normal operating mode		−40 to +110	°C
		Flash programming mode		−40 to +85	
Storage temperature	T_{stg}			−40 to +125	°C

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.2.2 Capacitance

(T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	f_X = 1 MHz, Unmeasured pins returned to 0 V.			10	pF

1.2.3 Operating conditions

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

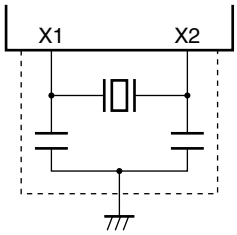
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC Capacity = 4.7 μF at operation with main clock	4		20	MHz
		REGC Capacity = 4.7 μF at operation with subclock (RC resonator)	12.5 **Note**		27.5 **Note**	kHz

Note The internal system clock frequency is half the oscillation frequency.

1.2.4 Oscillator Characteristics

Main clock oscillator characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1		4		5	MHz
		Oscillation stabilization time Note 2	After reset release		$2^{16}/f_X$		s
			After STOP mode release	0.5 Note 3	Note 4		ms
			After IDLE2 mode release	0.35	Note 4		ms
Crystal resonator		Oscillation frequency (f_X) Note 1		4		5	MHz
		Oscillation stabilization time Note 2	After reset release		$2^{16}/f_X$		s
			After STOP mode release	0.5 Note 3	Note 4		ms
			After IDLE2 mode release	350	Note 4		μs

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the crystal resonator after reset or STOP mode is released.

3. Time required to stabilize access to the internal flash memory.

4. The value differs depending on the OSTS register settings.

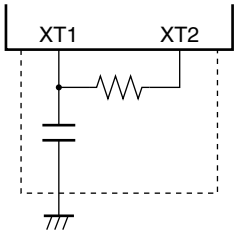
Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator		Oscillation frequency (f_{XT}) Notes 1, 4	R = 390 kΩ ±5% Note 3 C = 47 pF ±10% Note 3	25	40	55	kHz
		Oscillation stabilization time Note 2				100	μs

Notes 1. Indicates only oscillator characteristics. Refer to **28. 2. 10 AC Characteristics** for CPU operating clock.

2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.2.5 PLL Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		4		5	MHz
Output frequency	f_{xx}		16		20	MHz
Clock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			800	μs

1.2.6 Ring-OSC Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

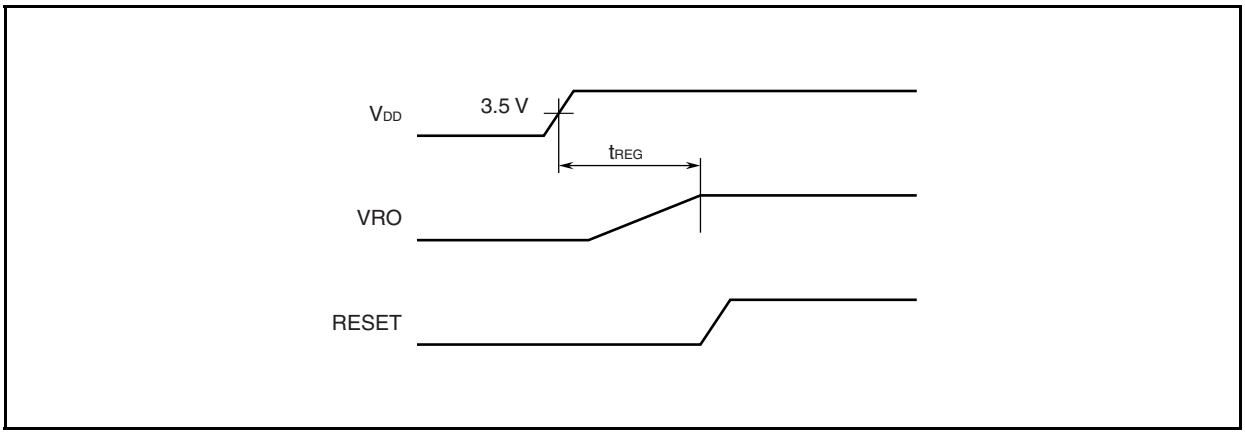
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_r		100	200	400	kHz

1.2.7 Voltage Regulator Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{DD}		3.5		5.5	V
Output voltage	V_{RO}			2.5		V
Lock time[Note 1]	t_{REG}	After V_{DD} reaches MIN.: 3.5 V Connect C = 4.7 μF ± 20% to REGC pin			1	ms

Note 1. The lock time does not have to be considered for devices that have POC.



1.2.8 DC Characteristics

(1) Input/Output level

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P30, P34, P36 to P38, P41, P63 to P69, P614, P615, P81, P98, P911 PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6	0.7EV_{DD}		EV_{DD}	V
	V_{IH2}	P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P60 to P62, P610 to P613, P80, P90 to P97, P99, P910, P912 to P915	0.8EV_{DD}		EV_{DD}	V
	V_{IH3}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	0.7BV_{DD}		BV_{DD}	V
	V_{IH4}	P70 to P715, P120 to P127	0.7AV_{REF0}		AV_{REF0}	V
	V_{IH5}	$\overline{RESET}$, FLMD0	0.8EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL1}	P30, P34, P36 to P38, P41, P63 to P69, P614, P615, P81, P98, P911 PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6	EV_{SS}		0.3EV_{DD}	V
	V_{IL2}	P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P60 to P62, P610 to P613, P80, P90 to P97, P99, P910, P912 to P915	EV_{SS}		0.2EV_{DD}	V
	V_{IL3}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	BV_{SS}		0.3BV_{DD}	V
	V_{IL4}	P70 to P715, P120 to P127	AV_{SS}		0.3AV_{REF0}	V
	V_{IL5}	$\overline{RESET}$, FLMD0	EV_{SS}		0.2EV_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high Note 1	V_{OH1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80 to P81, P90 to P915	I_{OH} = –1.0 mA	EV_{DD} – 1.0		EV_{DD}	V
			I_{OH} = –0.1 mA	EV_{DD} – 0.5		EV_{DD}	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6					
	V_{OH2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	I_{OH} = –1.0 mA	BV_{DD} – 1.0		BV_{DD}	V
			I_{OH} = –0.1 mA	BV_{DD} – 0.5		BV_{DD}	V
	V_{OH3}	P70 to P715, P120 to P127	I_{OH} = –1.0 mA	AV_{REF0} – 1.0		AV_{REF0}	V
			I_{OH} = –0.1 mA	AV_{REF0} – 0.5		AV_{REF0}	V
Output voltage, low Note 1	V_{OL1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	I_{OL} = 1.0 mA	0		0.4	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6					
	V_{OL2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	I_{OL} = 1.0 mA	0		0.4	V
	V_{OL3}	P70 to P715, P120 to P127	I_{OL} = 1.0 mA	0		0.4	V
Pull-up resistor	R_1	V_I = 0 V		10	30	100	kΩ
Pull-down resistor Note 2	R_2	V_I = V_{DD}		10	30	100	kΩ

Notes 1. Total IOH/IOL (Max.) is 20 mA/-20 mA each power supply terminal (EVDD, BVDD and AVREF0).

2. $\overline{\text{DRST}}$ pin only (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Analog pins			+0.3	μA
			Other pins[Note 1]			+2.0	
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Analog pins			−0.3	μA
			Other pins[Note 1]			−2.0	
Output leakage current, high	I_{LOH1}	V_O = V_{DD}	Analog pins			+0.3	μA
			Other pins			+2.0	
Output leakage current, low	I_{LOL1}	V_O = 0 V	Analog pins			−0.2	μA
			Other pins			−2.0	

Note 1. For flash memory product, specification of FLMD0 is as follows:

Input leakage current, high: 4 μA

Input leakage current, low: −4 μA

(3) Supply current

Supply current (V850ES/FJ2: μPD70F3239, μPD70F3238)

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current Note 1	I_{DD1}	Normal operation,	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		40	55	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		27		mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		25	37	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		14		mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.6	1.2	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.9	mA
	I_{DD5}	Subclock operation mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note 4		200	600	μA
	I_{DD6}	Sub-IDLE mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note 4		35	340	μA
	I_{DD7}	Stop mode Notes 2, 5	POC stopped, Ring-OSC stopped		7	250	μA
			POC operating, Ring-OSC stopped		10	255	μA
			POC stopped, Ring-OSC operating		15	265	μA
			POC operating, Ring-OSC operating		18	270	μA

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).
The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.

3. POC operating, Ring-OSC operating.

4. The RC oscillation frequency is 40 kHz (TYP.). This clock is internally divided by 2.

5. When the sub-OSC is not used.

Supply current (V850ES/FJ2: μPD70F3237)

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current Note 1	I_{DD1}	Normal operation	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		30	45	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		22		mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		18	30	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		11		mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.6	1.2	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.25	0.9	mA
	I_{DD5}	Subclock operation mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note		200	600	μA
	I_{DD6}	Sub-IDLE mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note 4		35	340	μA
	I_{DD7}	Stop mode Notes 2, 5	POC stopped, Ring-OSC stopped		7	250	μA
			POC operating, Ring-OSC stopped		10	255	μA
			POC stopped, Ring-OSC operating		15	265	μA
			POC operating, Ring-OSC operating		18	270	μA

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).
The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.

3. POC operating, Ring-OSC operating.

4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.

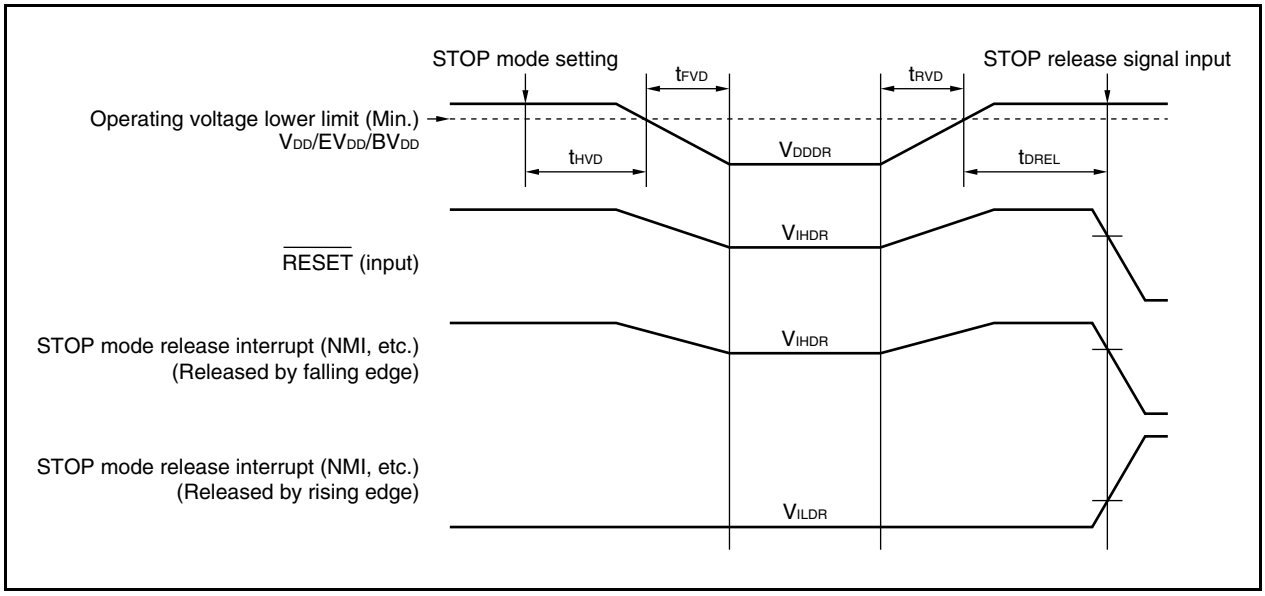
5. When the sub-OSC is not used.

1.2.9 Data Retention Characteristics

STOP Mode (T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 1.9 V to 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

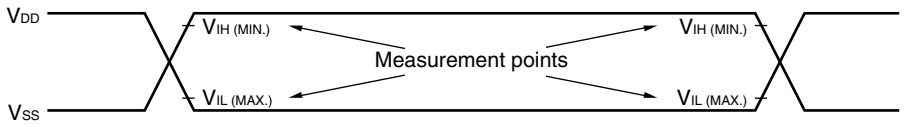
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	In STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.0 V		10	T.B.D	μA
Supply voltage rise time	t_{RVD}		1			μs
Supply voltage fall time	t_{FVD}		1			μs
Supply voltage retention time	t_{HVD}	After STOP mode release	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches MIN.: 3.5 V	0			μs
Data retention input voltage, high	V_{IHDR}	All input ports	0.9V_{DDDR}		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	All input ports	0		0.1V_{DDDR}	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

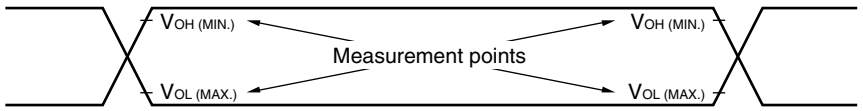


1.2.10 AC Characteristics

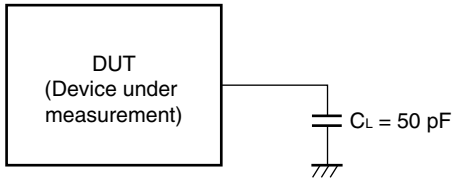
AC Test Input Measurement Points (V_{DD}, AV_{DD}, EV_{DD}, BV_{DD})



AC Test Output Measurement Points



Load Conditions



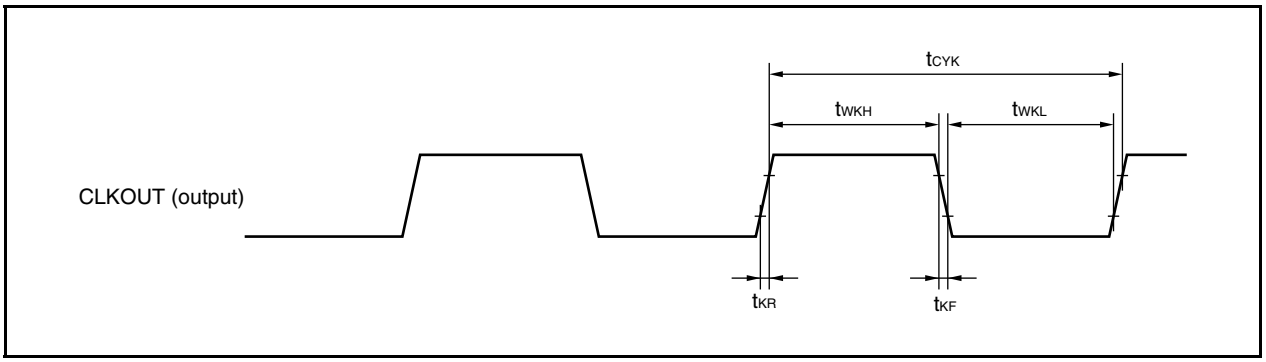
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

(1) CLKOUT output timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}		50 ns	80 μs	
High-level width	t_{WKH}		t_{CYK}/2 – 15		ns
Low-level width	t_{WKL}		t_{CYK}/2 – 15		ns
Rise time	t_{KR}			15	ns
Fall time	t_{KF}			15	ns

Clock Timing



(2) Bus timing

(a) CLKOUT asynchronous: In multiplex bus mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}		$(0.5 + t_{ASW})T - 20$		ns
Address hold time (from ASTB↓)	t_{HSTA}		$(0.5 + t_{AHW})T - 15$		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}			16	ns
Data input setup time from address	t_{SAID}			$(2 + n + t_{ASW} + t_{AHW})T - 40$	ns
Data input setup time from $\overline{RD}$↓	t_{SRDID}			$(1 + n)T - 30$	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{WRm}$↓	$t_{DSTRDWR}$		$(0.5 + t_{AHW})T - 15$		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}		0		ns
Address output time from $\overline{RD}$↑	t_{DRDA}		$(1 + i)T - 15$		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$		$0.5T - 15$		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}		$(1.5 + i + t_{ASW})T - 15$		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}		$(1 + n)T - 15$		ns
ASTB high-level width	t_{WSTH}		$(1 + i + t_{ASW})T - 15$		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}			15	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}		$(1 + n)T - 20$		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}		$T - 15$		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	n ≥ 1		$(1.5 + t_{ASW} + t_{AHW})T - 45$	ns
	t_{SAWT2}			$(1.5 + n + t_{ASW} + t_{AHW})T - 45$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	n ≥ 1	$(0.5 + n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}		$(1.5 + n + t_{ASW} + t_{AHW})T$		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	n ≥ 1		$(1 + t_{AHW})T - 35$	ns
	t_{SSTWT2}			$(1 + n + t_{AHW})T - 35$	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	n ≥ 1	$(n + t_{AHW})T$		ns
	t_{HSTWT2}		$(1 + n + t_{AHW})T$		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}		$T + 10$		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}		$T - 20$		ns
Delay time from $\overline{HLDAK}$↑ to bus output	t_{DHAC}		–3		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}			$(2n + 7.5)T + 25$	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}		$0.5T$	$1.5T + 35$	ns

Remarks 1. $T = 1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. m = 0, 1

4. i: Number of idle states inserted after a read cycle (0 or 1).

7. The values in the above specifications are values for when clocks with a 1: 1 duty ratio are input from X1.

8. t_{ASW}: Number of address setup wait clocks (0 or 1).
t_{AHW}: Number of address hold wait clocks (0 or 1).

Caution : When the operating frequency is high, it is not possible to access without a bus wait cycle. Please insert a wait clock ((data wait (n) / address setup wait (t_{ASW}) / address hold wait (t_{AHW}))

(b) CLKOUT synchronous: In multiplex bus mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

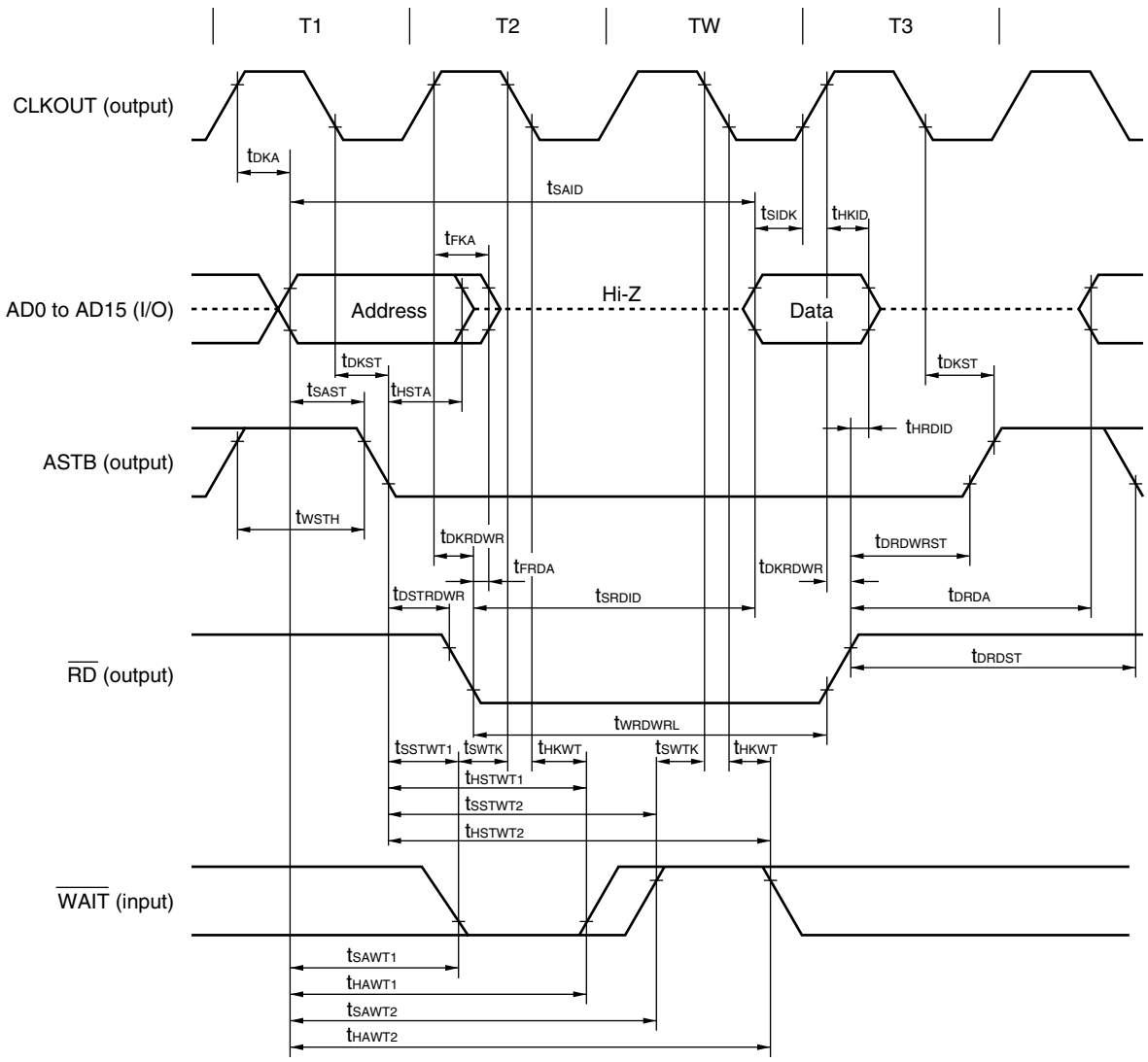
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}		0	24	ns
Delay time from CLKOUT↑ to address float	t_{FKA}		0	24	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}		–12	+12	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}		–5	+14	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	t_{HKID}		5		ns
Data output delay time from CLKOUT↑	t_{DKOD}			22	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}		30		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}		30		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}			24	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}			25	ns

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

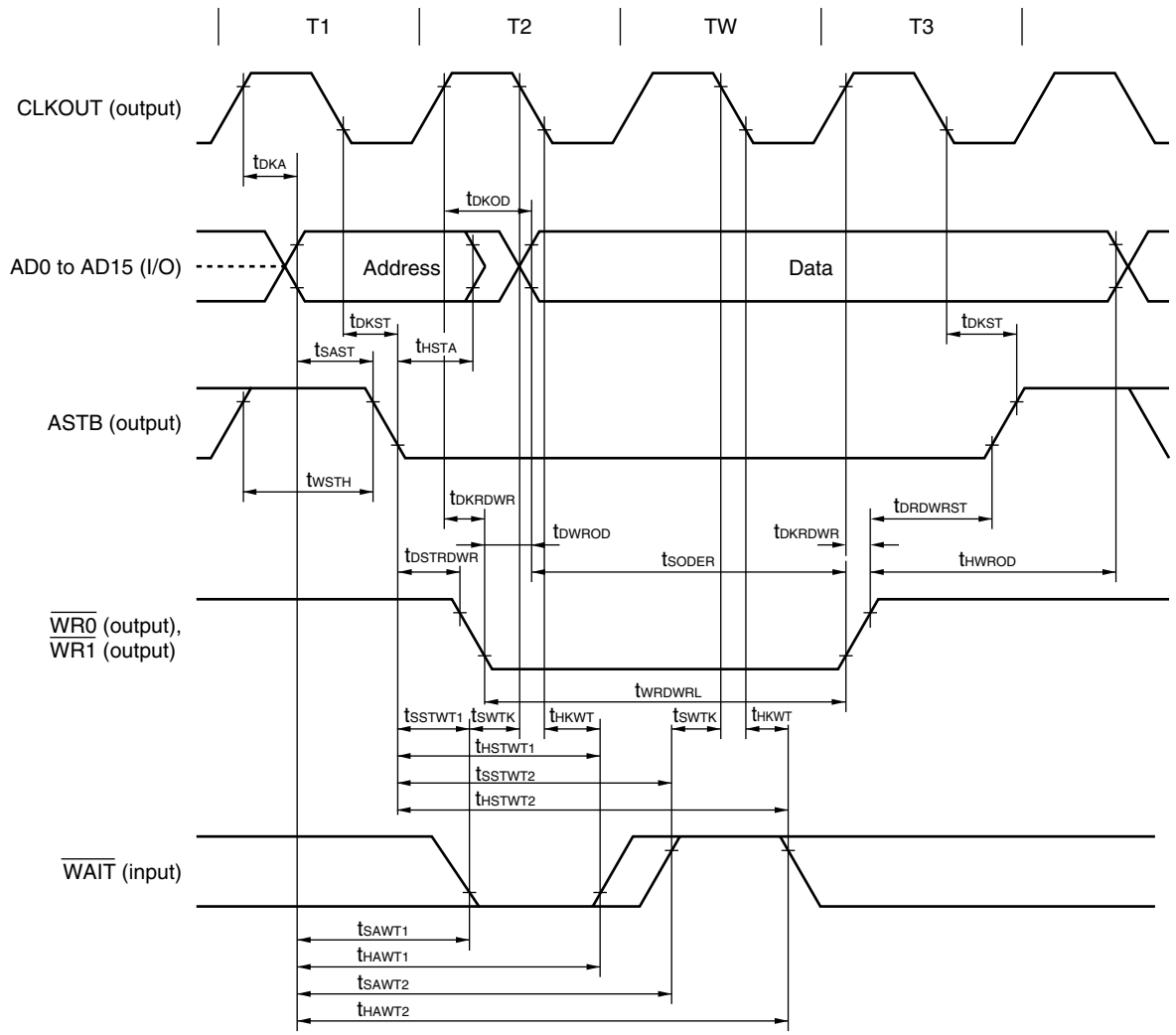
Caution : When the operating frequency is high, it is not possible to access without a bus wait cycle. Please insert a wait clock ((data wait (n) / address setup wait (t_{ASW}) / address hold wait (t_{AHW})).

Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



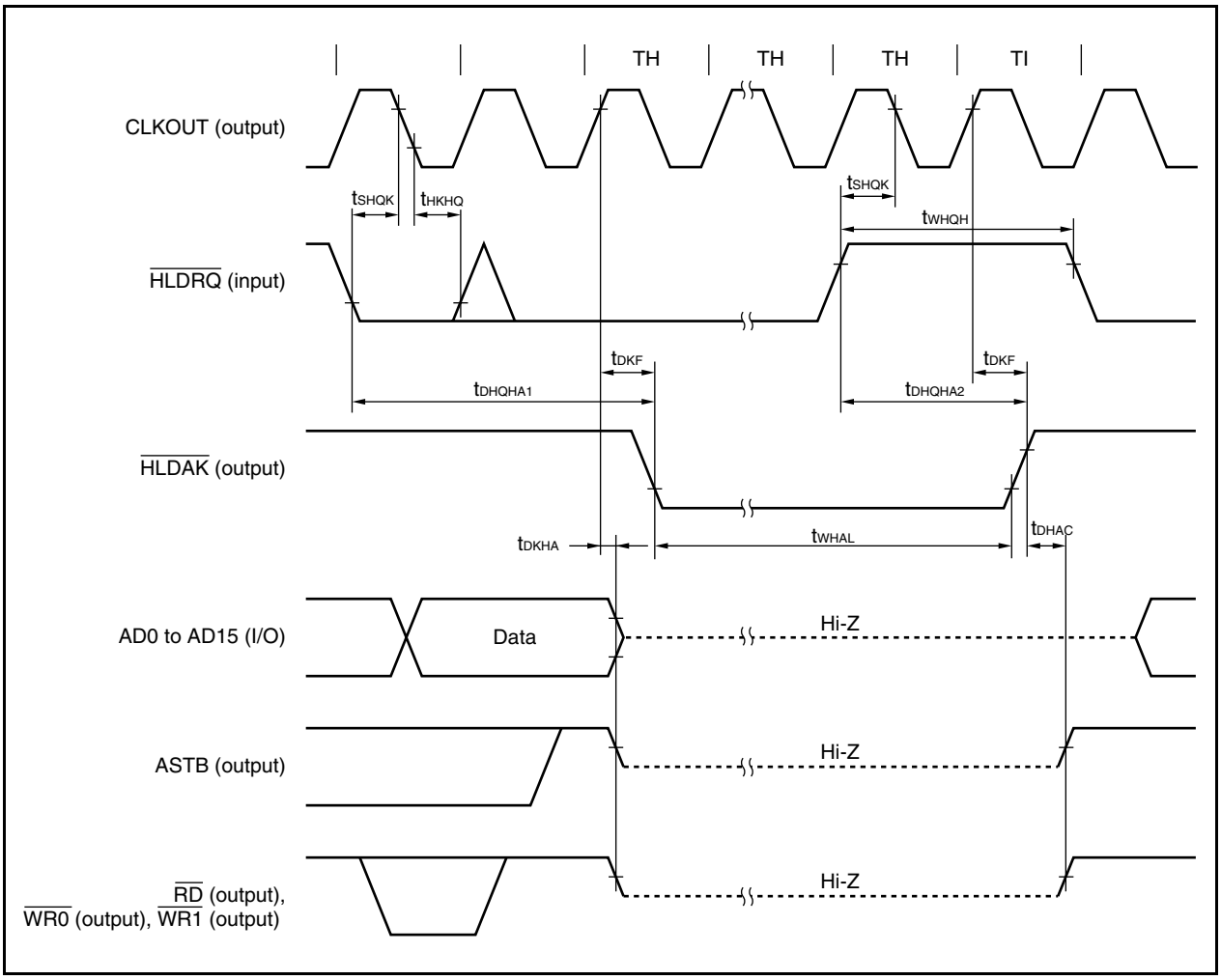
Remark $\overline{WR0}$ and $\overline{WR1}$ are high level.

Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



Remark $\overline{RD}$ is high level.

Bus Hold: In Multiplex Bus Mode



(3) Basic Operation

(a) Reset, Interrupt timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

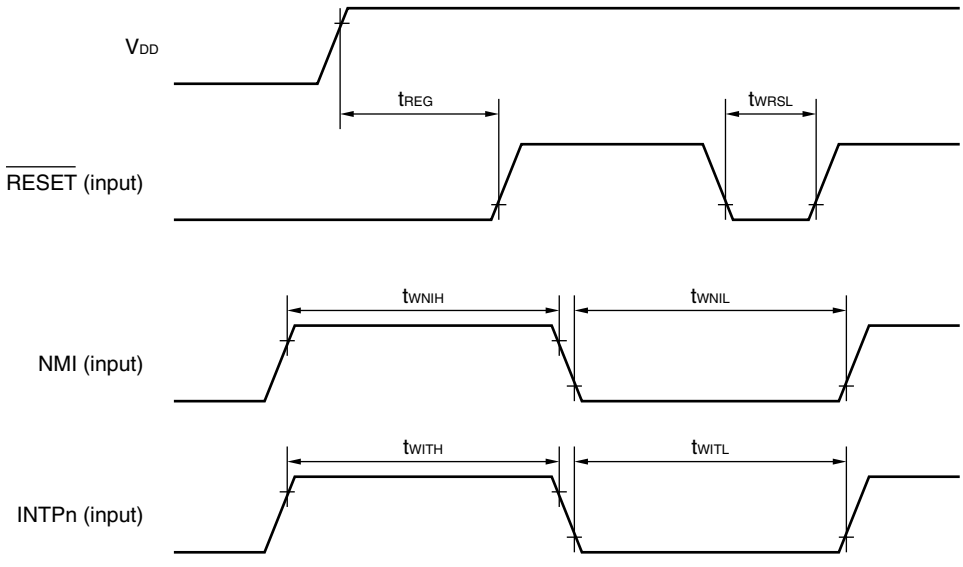
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		500		ns
NMI high-level width	t_{WNIH}	Analog noise elimination	500		ns
NMI low-level width	t_{WNIL}	Analog noise elimination	500		ns
INTPn[Note 1] high-level width	t_{WITH}	Analog noise elimination (n = 0 to 14)	500		ns
		Digital noise elimination (n = 3)	**Note 2**		ns
INTPn[Note 1] low-level width	t_{WITL}	Analog noise elimination (n = 0 to 14)	1		ns
		Digital noise elimination (n = 3)	**Note 2**		ns

Notes 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/DRST).

2. 2Tsamp + 20 or 3Tsamp + 20

Tsamp: Sampling clock for noise elimination

Reset/Interrupt

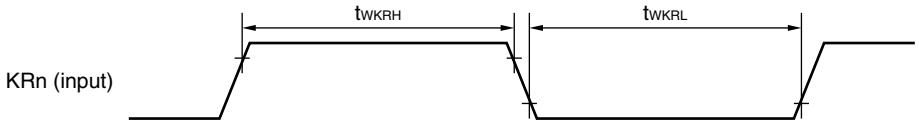


Remark n = 0 to 14

(b) Key return timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
KRn input high-level width	t_{WKRH}	Analog noise elimination (n = 0 to 14)	500		ns
KRn input low-level width	t_{WKRL}		500		ns



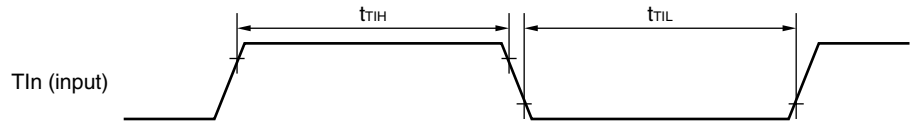
Remark n = 0 to 14

(c) Timer input timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TIn high-level width	t_{TIH}	TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03, TIQ10 to TIQ13, TIQ20 to TIQ23	**Note**		ns
TIn low-level width	t_{TIL}		**Note**		ns

Note 2Tsamp + 20 or 3Tsamp + 20
Tsamp: Sampling clock for noise elimination



Remark TIn: TIP00, TIP01, TIP10 TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03, TIQ10 to TIQ13, TIQ20 to TIQ23

(d) CSIB timing

(i) Master mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCYn}		125		ns
$\overline{SCKBn}$ high-level width	t_{KHn}		$t_{KCYn}/2 - 15$		ns
$\overline{SCKBn}$ low-level width	t_{KLn}		$t_{KCYn}/2 - 15$		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		30		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{KSIn}		25		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	t_{KSOn}			25	ns

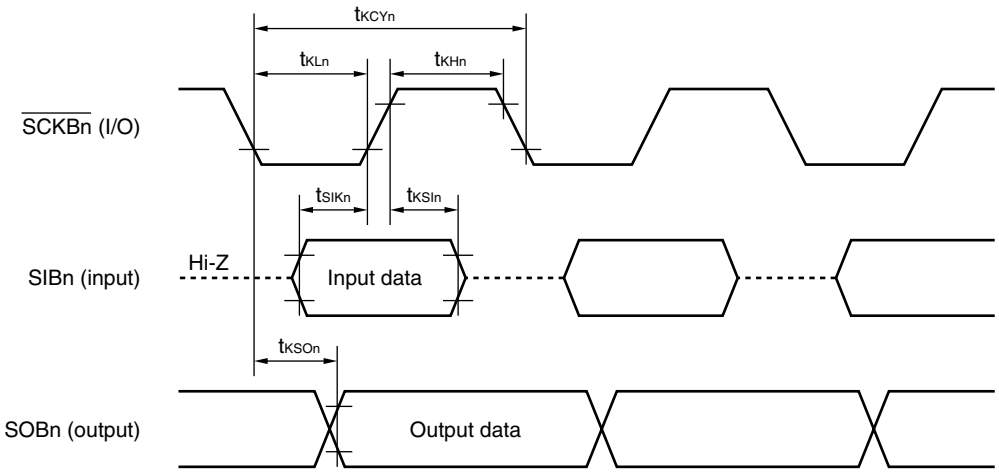
Remark n = 0 to 2

(ii) Slave mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCYn}		200		ns
$\overline{SCKBn}$ high-level width	t_{KHn}		90		ns
$\overline{SCKBn}$ low-level width	t_{KLn}		90		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		50		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{KSIn}		50		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	t_{KSOn}			50	ns

Remark n = 0 to 2



Remark n = 0 to 4

*CAN internal clock (fCAN): CAN baud rate clock

(e) UART timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

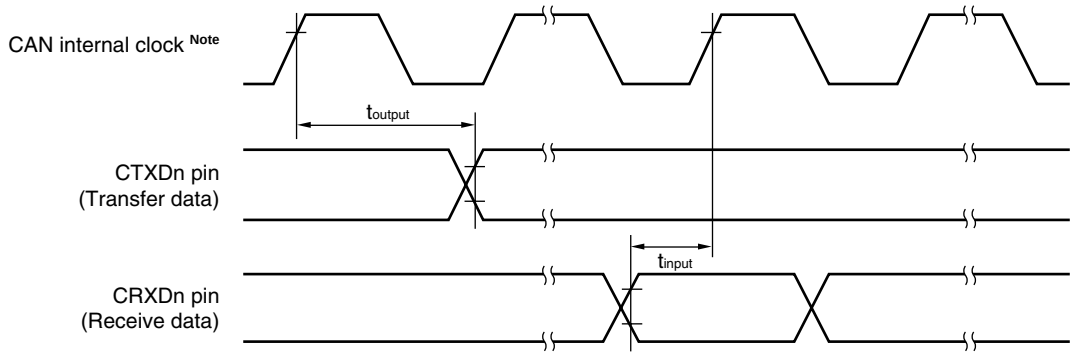
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Communication rate				312.5	kbps
ASCK0 cycle time				10	MHz

(f) CAN timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate				1	Mbps
Internal delay time[Note]				100	ns

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



Note *CAN internal clock (fCAN): CAN baud rate clock

Remark n = 0 to 3

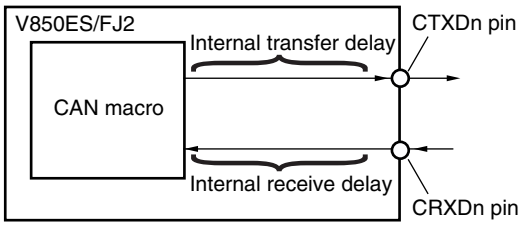


Image figure of internal delay

Remark n = 0 to 3

(g) A/D converter

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		4.0 ≤ AV_{REF0} ≤ 5.5 V		±0.15	±0.3	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV_{REF0} current	I_{AREF0}	When using A/D converter		5	10	mA
		When not using A/D converter		1	10	μA

Note Excluding quantization error (±0.05%FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

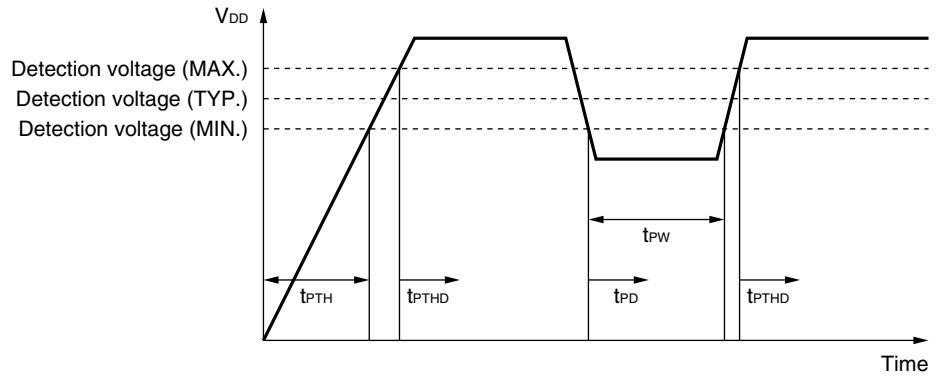
(h) POC circuit characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		3.5	3.7	3.9	V
Power supply startup time	t_{PTH}	V_{DD} = 0 V → 3.5 V	0.002			ms
Response delay time 1[Note 1]	t_{PTHD}	In case of power on. After V_{DD} reaches 3.9 V.			3.0	ms
Response delay time 2[Note 2]	t_{PD}	In case of power off. After V_{DD} drops 3.5 V.			1	ms
Minimum V_{DD} width	t_{PW}		0.2			ms

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.



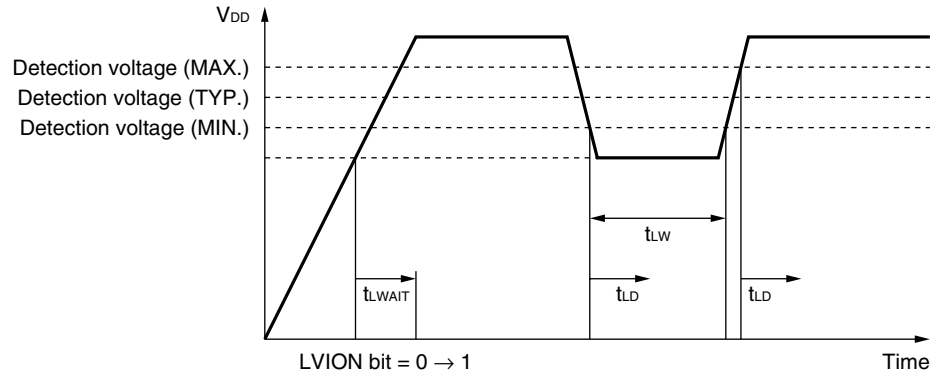
(i) LVI circuit characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.2	4.4	4.6	V
	V_{LVI1}		4.0	4.2	4.4	V
Response time[Note 1]	t_{LD}	After V_{DD} reaches V_{LVI0}/V_{LVI1} (Max.). After V_{DD} drops V_{LVI0}/V_{LVI1} (Min.).		0.2	2.0	ms
Minimum V_{DD} width	t_{LW}		0.2			ms
Reference voltage stabilization wait time[Note 2]	t_{LWAIT}	After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 →1		0.1	0.2	ms

Notes 1. The time required to output an interrupt/reset after the detection voltage is detected.

2. Unnecessary when the POC function is used.

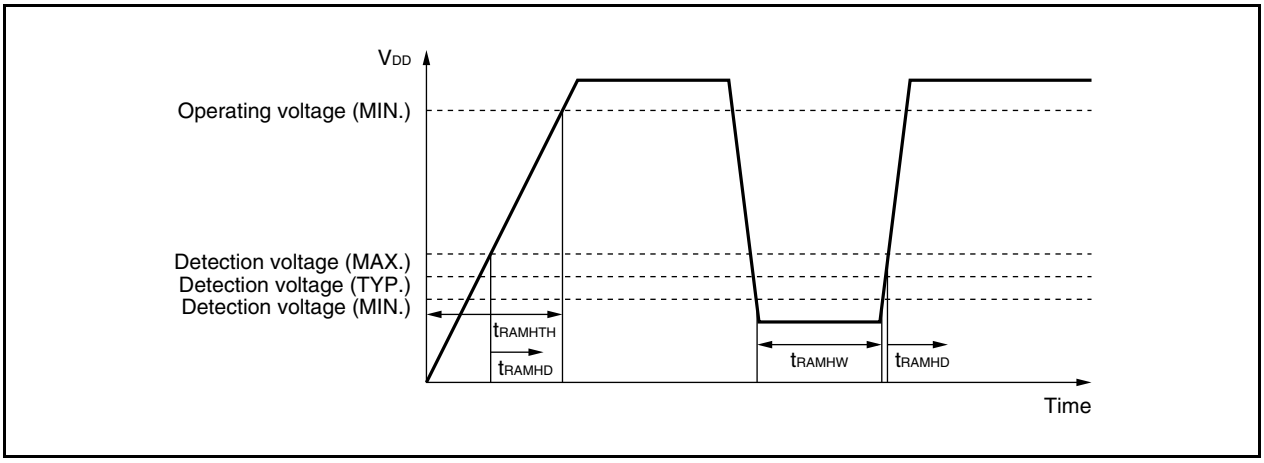


(j) RAM retention flag characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = BV_{DD} = 1.9 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{RAMH}		1.9	2.0	2.1	V
Supply voltage rise time	t_{RAMHTH}	V_{DD} = 0 V → 3.5 V	0.002		1,800	ms
Response time[Note]	t_{RAMHD}	After the supply voltage reaches the detection voltage (MAX.)		0.2	2.0	ms
Minimum V_{DD} width	t_{RAMHW}		0.2			ms

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{CPU}		4		20	MHz
Supply voltage	V_{DD}		3.5		5.5	V
Number of writes	C_{WRT} Note				100	Times
Input voltage, high	V_{IH}	FLMD0	0.8EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL}	FLMD0	EV_{SS}		0.2EV_{DD}	V
Write time + erase time	t_{IWRT} + t_{ERASE}	Flash: 256 KB (μPD70F3237) 512 KB (μPD70F3239)			T.B.D	s
Programming temperature	t_{PRG}		–40		+85	°C

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

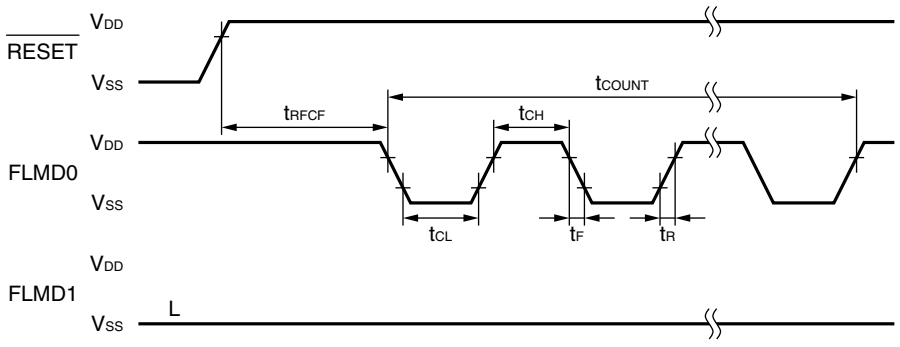
Example: P: Write, E: Erase
Shipped product → P → E → P → E → P: 3 rewrites
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time from $\overline{\text{RESET}}$↑	t_{RFCF}		5000/fx+ Note			s
Count execution time	t_{COUNT}				3	ms
FLMD0 high-level width	t_{CH}		10		100	μs
FLMD0 low-level width	t_{CL}		10		100	μs
FLMD rise time	t_R				50	ns
FLMD fall time	t_F				50	ns

Note " " represents the oscillation stabilization time.



1.3 Electrical Specifications of (A2)-Grade

1.3.1 Absolute maximum ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	BV_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	EV_{DD}	$V_{DD} = EV_{DD} = BV_{DD}$	−0.5 to +6.5	V
	AV_{REF0}		−0.5 to +6.5	V
	V_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	BV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	EV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 **Note**	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6		
	V_{I2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	−0.5 to BV_{DD} + 0.5 **Note**	V
	V_{I3}	X1, X2, XT1, XT2	−0.5 to V_{RO} + 0.5 **Note**	V
Analog input voltage	V_{IAN}	P70 to P715, P120 to P127	−0.5 to AV_{REF0} + 0.5 **Note**	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute maximum ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	Per pin	4	mA
			Total of all pins	50	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6			
		P70 to P715, P120 to P127	Per pin	4	mA
			Total of all pins	20	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	Per pin	4	mA
			Total of all pins	50	mA
Output current, high	I_{OH}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	Per pin	−4	mA
			Total of all pins	−50	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6			
		P70 to P715, P120 to P127	Per pin	−4	mA
			Total of all pins	−20	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	Per pin	−4	mA
			Total of all pins	−50	mA
Operating ambient temperature	T_A	Normal operating mode		−40 to +125	°C
		Flash programming mode		−40 to +85	
Storage temperature	T_{stg}			−40 to +125	°C

Cautions 1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

1.3.2 Capacitance

(T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	f_X = 1 MHz, Unmeasured pins returned to 0 V.			10	pF

1.3.3 Operating conditions

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

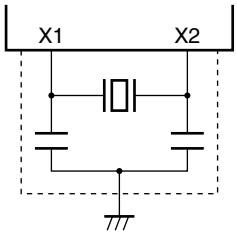
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC Capacity = 4.7 μF, at operation with main clock	4		20	MHz
		REGC Capacity = 4.7 μF, at operation with subclock (RC resonator)	12.5		27.5	kHz

Note The internal system clock frequency is half the oscillation frequency.

1.3.4 Oscillator Characteristics

Main clock oscillator characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1		4		5	MHz
		Oscillation stabilization time Note 2	After reset release		$2^{16}/f_X$		s
			After STOP mode release	0.5 Note 3	Note 4		ms
			After IDLE2 mode release	0.35	Note 4		ms
Crystal resonator		Oscillation frequency (f_X) Note 1		4		5	MHz
		Oscillation stabilization time Note 2	After reset release		$2^{16}/f_X$		s
			After STOP mode release	0.5 Note 3	Note 4		ms
			After IDLE2 mode release	350	Note 4		μs

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the crystal resonator after reset or STOP mode is released.

3. Time required to stabilize access to the internal flash memory.

4. The value differs depending on the OSTS register settings.

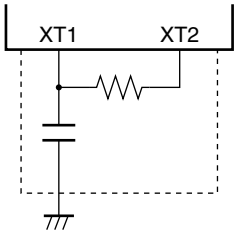
Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator		Oscillation frequency (f_{XT}) Notes 1, 4	R = 390 kΩ ±5% Note 3 C = 47 pF ±10% Note 3	25	40	55	kHz
		Oscillation stabilization time Note 2				100	μs

Notes 1. Indicates only oscillator characteristics. Refer to **28. 3. 10 AC Characteristics** for CPU operating clock.

2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC oscillation frequency is 40 kHz (Typ.). This clock is divided (1/2) internally. In case of RC oscillator, internal system clock frequency (f_{XT}) is 12.5 kHz (Min.), 20 kHz (Typ.), and 27.5 kHz (Max.).

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

1.3.5 PLL Characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		4		5	MHz
Output frequency	f_{xx}		16		20	MHz
Clock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			800	μs

1.3.6 Ring-OSC Characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

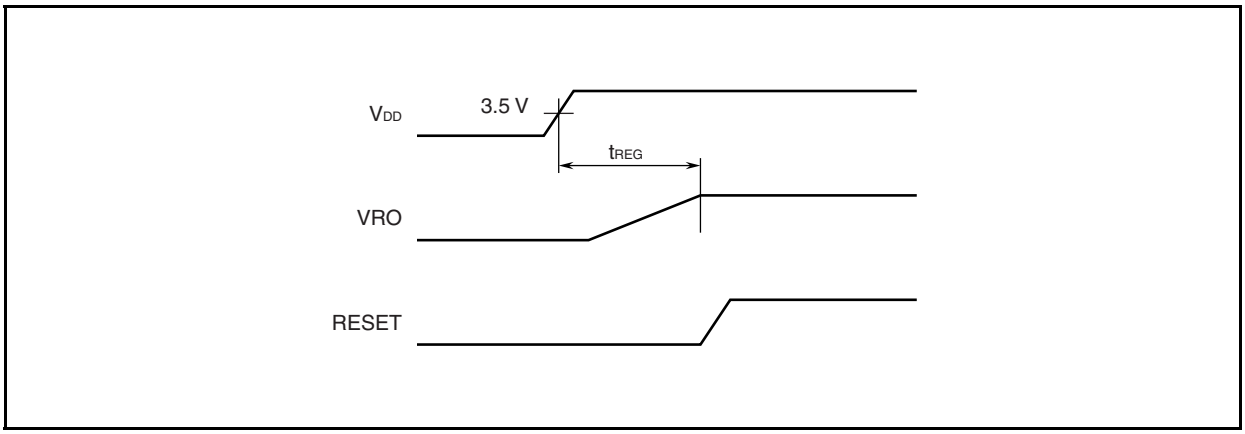
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_r		100	200	400	kHz

1.3.7 Voltage Regulator Characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{DD}		3.5		5.5	V
Output voltage	V_{RO}			2.5		V
Lock time[Note 1]	t_{REG}	After V_{DD} reaches MIN.: 3.5 V Connect C = 4.7 mF ± 20% to REGC pin			1	ms

Note 1. The lock time does not have to be considered for devices that have POC.



1.3.8 DC Characteristics

(1) Input/Output level

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P30, P34, P36 to P38, P41, P63 to P69, P614, P615, P81, P98, P911 PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6	0.7EV_{DD}		EV_{DD}	V
	V_{IH2}	P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P60 to P62, P610 to P613, P80, P90 to P97, P99, P910, P912 to P915	0.8EV_{DD}		EV_{DD}	V
	V_{IH3}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	0.7BV_{DD}		BV_{DD}	V
	V_{IH4}	P70 to P715, P120 to P127	0.7AV_{REF0}		AV_{REF0}	V
	V_{IH5}	$\overline{RESET}$, FLMD0	0.8EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL1}	P30, P34, P36 to P38, P41, P63 to P69, P614, P615, P81, P98, P911 PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6	EV_{SS}		0.3EV_{DD}	V
	V_{IL2}	P00 to P06, P10, P11, P31 to P33, P35, P39, P40, P42, P50 to P55, P60 to P62, P610 to P613, P80, P90 to P97, P99, P910, P912 to P915	EV_{SS}		0.2EV_{DD}	V
	V_{IL3}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	BV_{SS}		0.3BV_{DD}	V
	V_{IL4}	P70 to P715, P120 to P127	AV_{SS}		0.3AV_{REF0}	V
	V_{IL5}	$\overline{RESET}$, FLMD0	EV_{SS}		0.2EV_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high Note 1	V_{OH1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80 to P81, P90 to P915	I_{OH} = –1.0 mA	EV_{DD} – 1.0		EV_{DD}	V
			I_{OH} = –0.1 mA	EV_{DD} – 0.5		EV_{DD}	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6					
	V_{OH2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	I_{OH} = –1.0 mA	BV_{DD} – 1.0		BV_{DD}	V
			I_{OH} = –0.1 mA	BV_{DD} – 0.5		BV_{DD}	V
	V_{OH3}	P70 to P715, P120 to P127	I_{OH} = –1.0 mA	AV_{REF0} – 1.0		AV_{REF0}	V
			I_{OH} = –0.1 mA	AV_{REF0} – 0.5		AV_{REF0}	V
Output voltage, low Note 1	V_{OL1}	P00 to P06, P10, P11, P30 to P39, P40 to P42, P50 to P55, P60 to P615, P80, P81, P90 to P915	I_{OL} = 1.0 mA	0		0.4	V
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6					
	V_{OL2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15	I_{OL} = 1.0 mA	0		0.4	V
	V_{OL3}	P70 to P715, P120 to P127	I_{OL} = 1.0 mA	0		0.4	V
Pull-up resistor	R_1	V_I = 0 V		10	30	100	kΩ
Pull-down resistor Note 2	R_2	V_I = V_{DD}		10	30	100	kΩ

Notes 1. Total IOH/IOL (Max.) is 20 mA/-20 mA each power supply terminal (EVDD, BVDD and AVREF0).

2. $\overline{\text{DRST}}$ pin only (OCDM0 is the control register).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Pin leakage current

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Analog pins			+1.0	μA
			Other pins			+5.0	
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Analog pins			−1.0	μA
			Other pins			−5.0	
Output leakage current, high	I_{LOH1}	V_O = V_{DD}	Analog pins			+1.0	μA
			Other pins			+5.0	
Output leakage current, low	I_{LOL1}	V_O = 0 V	Analog pins			−1.0	μA
			Other pins			−5.0	

(3) Supply current

Supply current (V850ES/FJ2: μPD70F3239, μPD70F3238)

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current Note 1	I_{DD1}	Normal operation	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		40	55	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		27		mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		25	37	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		14		mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.6	1.5	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.25	1.15	mA
	I_{DD5}	Subclock operation mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note 4		200	850	μA
	I_{DD6}	Sub-IDLE mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note 4		35	590	μA
	I_{DD7}	Stop mode Notes 2, 5	POC stopped, Ring-OSC stopped		7	500	μA
			POC operating, Ring-OSC stopped		10	505	μA
			POC stopped, Ring-OSC operating		15	515	μA
			POC operating, Ring-OSC operating		18	520	μA

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).
The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.

3. POC operating, Ring-OSC operating.

4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.

5. When the sub-OSC is not used.

Supply current (256 KB version V850ES/FJ2: μPD70F3237)

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Flash memory products supply current Note 1	I_{DD1}	Normal operation	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		30	45	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		22		mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions operating		18	30	mA
			f_{XX} = 20 MHz (OSC = 5 MHz), all peripheral functions stopped		11		mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.6	1.5	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (OSC = 5 MHz), PLL off		0.25	1.15	mA
	I_{DD5}	Subclock operation mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note 4		200	850	μA
	I_{DD6}	Sub-IDLE mode Notes 2, 3	RC resonator f_{XT} = 40 kHz Note 4		35	590	μA
	I_{DD7}	Stop mode Notes 2, 5	POC stopped, Ring-OSC stopped		7	500	μA
			POC operating, Ring-OSC stopped		10	505	μA
			POC stopped, Ring-OSC operating		15	515	μA
			POC operating, Ring-OSC operating		18	520	μA

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped).
The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. When the main OSC is stopped.

3. POC operating, Ring-OSC operating.

4. The RC oscillation frequency is 40 kHz(TYP.). This clock is internally divided by 2.

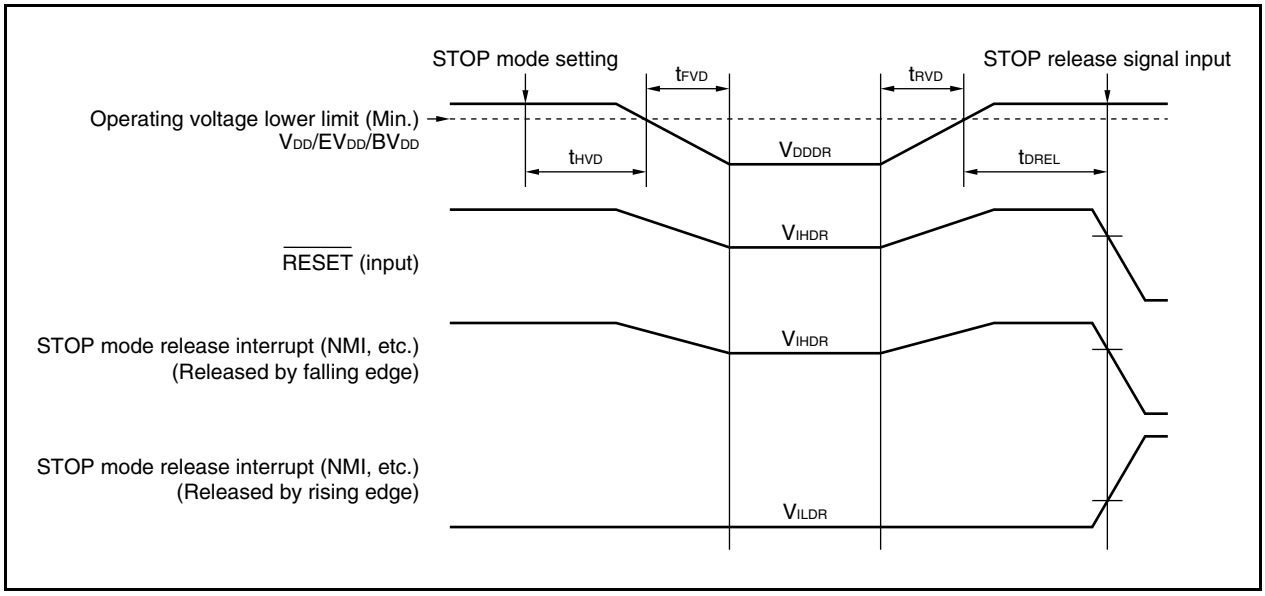
5. When the sub-OSC is not used.

1.3.9 Data Retention Characteristics

STOP Mode (T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 1.9 V to 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

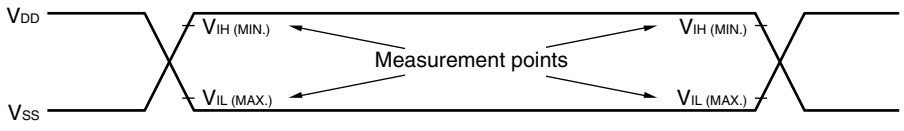
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	In STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.0 V		10	T.B.D	μA
Supply voltage rise time	t_{RVD}		1			μs
Supply voltage fall time	t_{FVD}		1			μs
Supply voltage retention time	t_{HVD}	After STOP mode release	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches MIN.: 3.5 V	0			μs
Data retention input voltage, high	V_{IHDR}	All input ports	0.9V_{DDDR}		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	All input ports	0		0.1V_{DDDR}	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

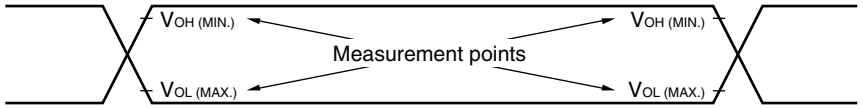


1.3.10 AC Characteristics

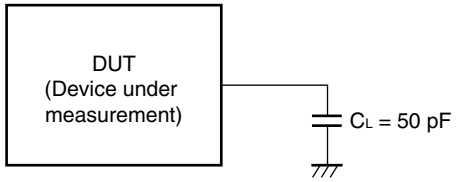
AC Test Input Measurement Points (V_{DD}, AV_{DD}, EV_{DD}, BV_{DD})



AC Test Output Measurement Points



Load Conditions



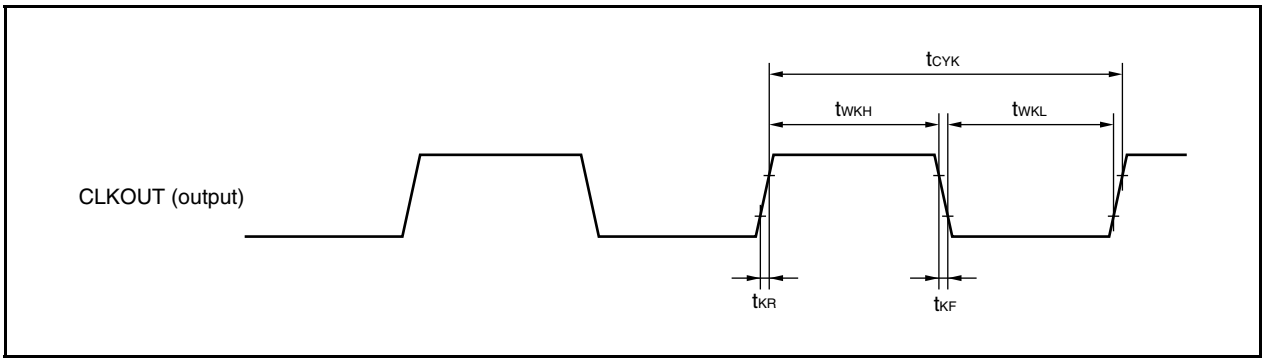
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

(1) CLKOUT output timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}		50 ns	80 μs	
High-level width	t_{WKH}		t_{CYK}/2 – 15		ns
Low-level width	t_{WKL}		t_{CYK}/2 – 15		ns
Rise time	t_{KR}			15	ns
Fall time	t_{KF}			15	ns

Clock Timing



(2) Bus timing

(a) CLKOUT asynchronous: In multiplex bus mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}		$(0.5 + t_{ASW})T - 20$		ns
Address hold time (from ASTB↓)	t_{HSTA}		$(0.5 + t_{AHW})T - 15$		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}			16	ns
Data input setup time from address	t_{SAID}			$(2 + n + t_{ASW} + t_{AHW})T - 40$	ns
Data input setup time from $\overline{RD}$↓	t_{SRDID}			$(1 + n)T - 30$	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{WRm}$↓	$t_{DSTRDWR}$		$(0.5 + t_{AHW})T - 15$		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}		0		ns
Address output time from $\overline{RD}$↑	t_{DRDA}		$(1 + i)T - 15$		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$		$0.5T - 15$		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}		$(1.5 + i + t_{ASW})T - 15$		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}		$(1 + n)T - 15$		ns
ASTB high-level width	t_{WSTH}		$(1 + i + t_{ASW})T - 15$		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}			15	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}		$(1 + n)T - 20$		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}		$T - 15$		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	n ≥ 1		$(1.5 + t_{ASW} + t_{AHW})T - 45$	ns
	t_{SAWT2}			$(1.5 + n + t_{ASW} + t_{AHW})T - 45$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	n ≥ 1	$(0.5 + n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}		$(1.5 + n + t_{ASW} + t_{AHW})T$		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	n ≥ 1		$(1 + t_{AHW})T - 35$	ns
	t_{SSTWT2}			$(1 + n + t_{AHW})T - 35$	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	n ≥ 1	$(n + t_{AHW})T$		ns
	t_{HSTWT2}		$(1 + n + t_{AHW})T$		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}		$T + 10$		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}		$T - 20$		ns
Delay time from $\overline{HLDAK}$↑ to bus output	t_{DHAC}		–3		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}			$(2n + 7.5)T + 25$	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}		$0.5T$	$1.5T + 35$	ns

Remarks 1. $T = 1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. m = 0, 1

4. i: Number of idle states inserted after a read cycle (0 or 1).

9. The values in the above specifications are values for when clocks with a 1: 1 duty ratio are input from X1.

10. t_{ASW}: Number of address setup wait clocks (0 or 1).
t_{AHW}: Number of address hold wait clocks (0 or 1).

Caution : When the operating frequency is high, it is not possible to access without a bus wait cycle. Please insert a wait clock ((data wait (n) / address setup wait (t_{ASW}) / address hold wait (t_{AHW}))

(b) CLKOUT synchronous: In multiplex bus mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

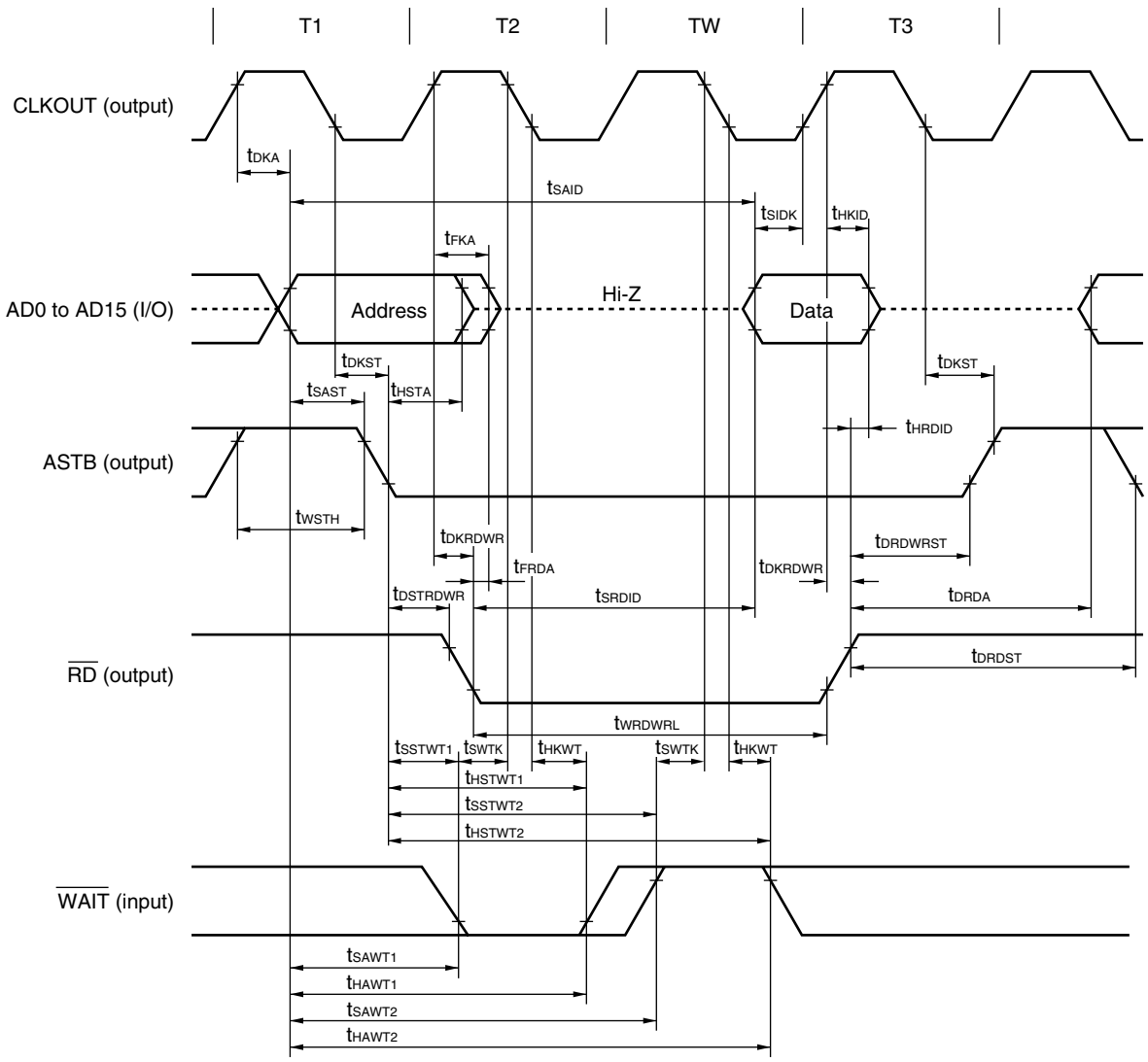
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}		0	24	ns
Delay time from CLKOUT↑ to address float	t_{FKA}		0	24	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}		–12	+12	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}		–5	+14	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	t_{HKID}		5		ns
Data output delay time from CLKOUT↑	t_{DKOD}			22	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}		30		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}		30		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}			24	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}			25	ns

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

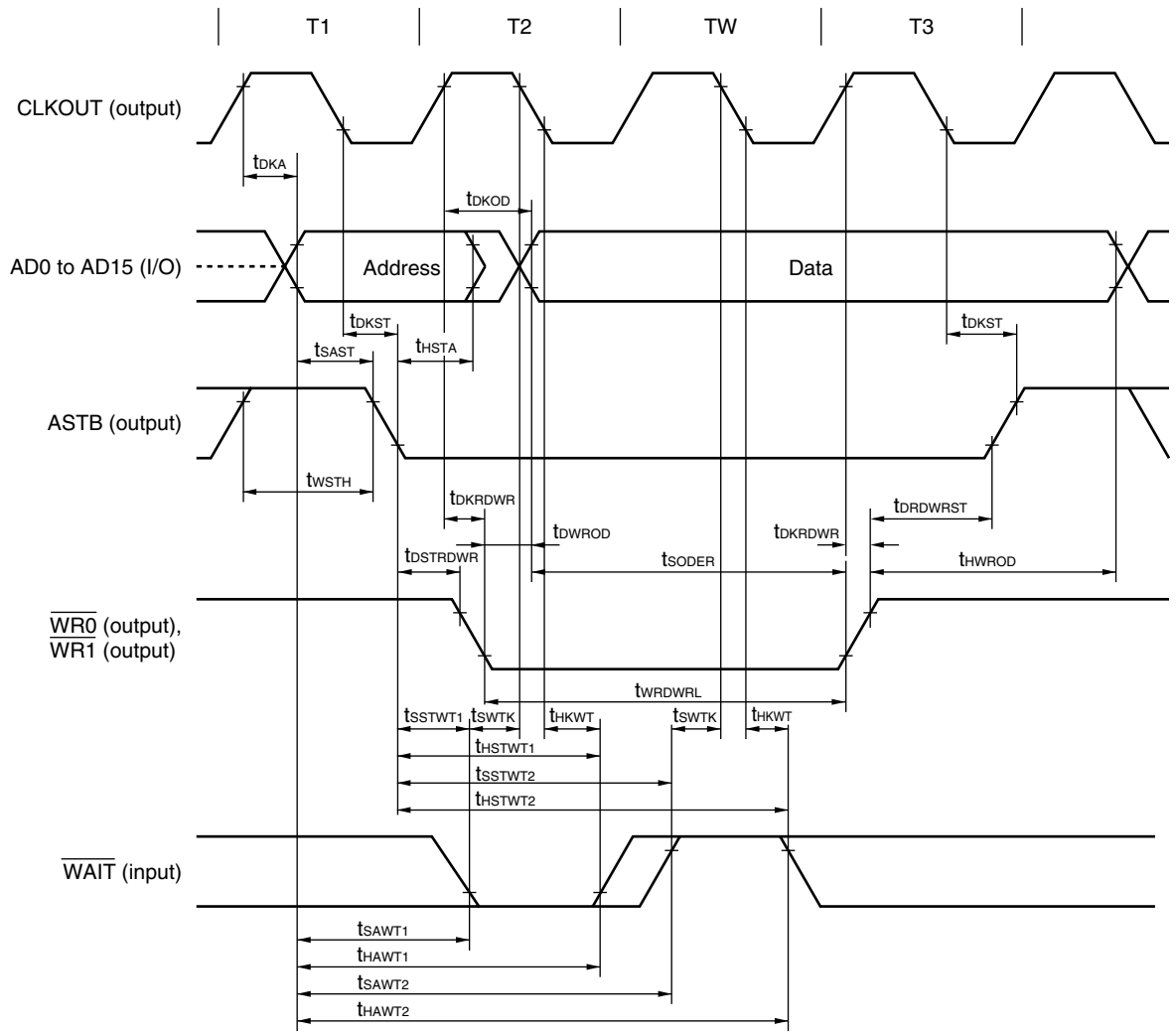
Caution : When the operating frequency is high, it is not possible to access without a bus wait cycle. Please insert a wait clock ((data wait (n) / address setup wait (t_{ASW}) / address hold wait (t_{AHW})).

Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



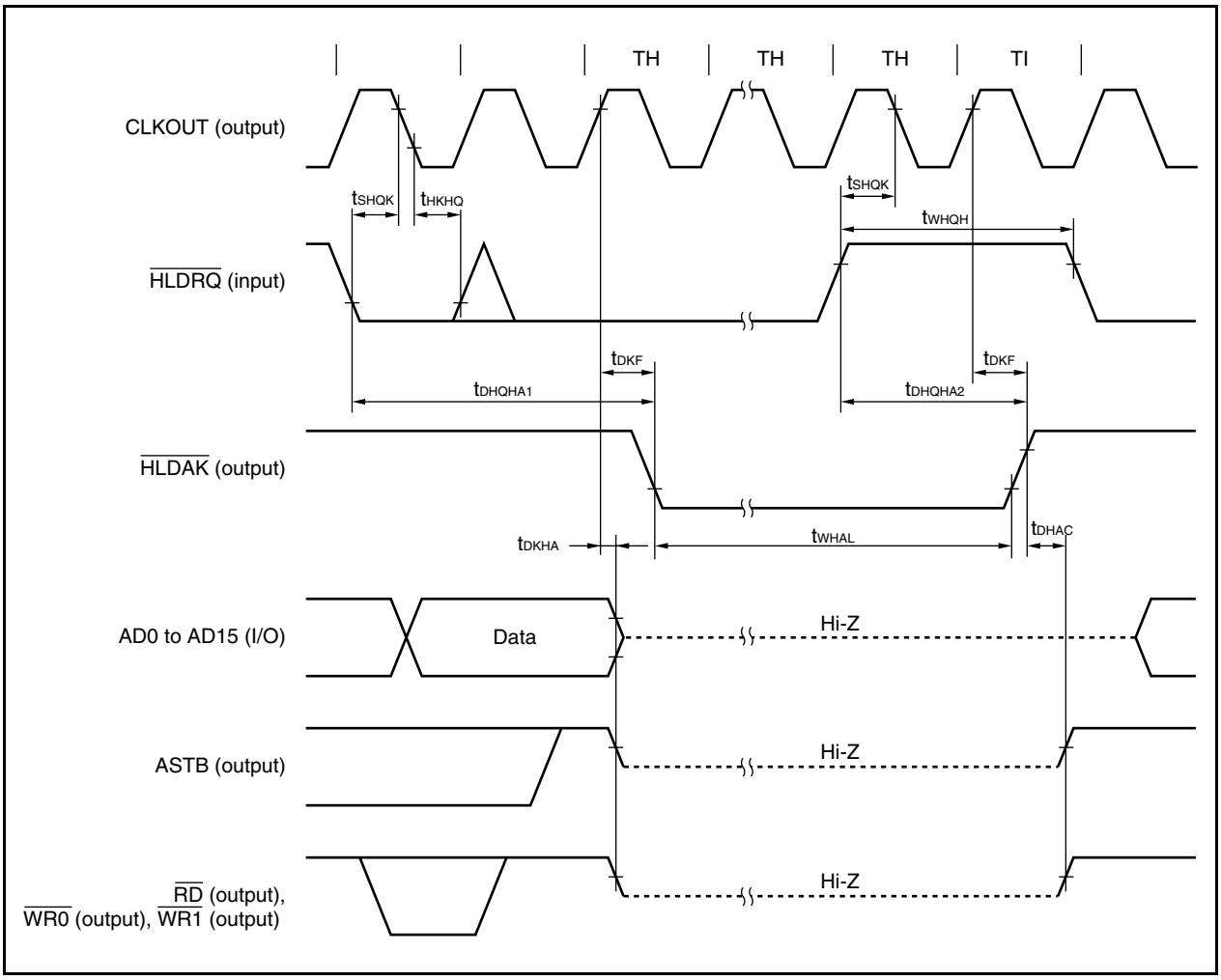
Remark $\overline{WR0}$ and $\overline{WR1}$ are high level.

Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



Remark $\overline{RD}$ is high level.

Bus Hold: In Multiplex Bus Mode



(3) Basic Operation

(a) Reset, Interrupt timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

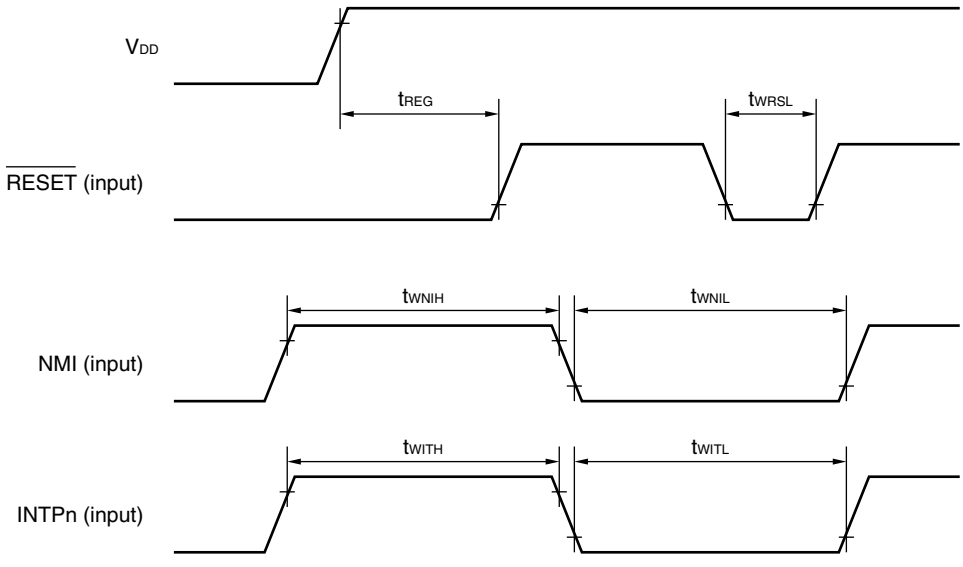
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		500		ns
NMI high-level width	t_{WNIH}	Analog noise elimination	500		ns
NMI low-level width	t_{WNIL}	Analog noise elimination	500		ns
INTPn[Note 1] high-level width	t_{WITH}	Analog noise elimination (n = 0 to 14)	500		ns
		Digital noise elimination (n = 3)	**Note 2**		ns
INTPn[Note 1] low-level width	t_{WITL}	Analog noise elimination (n = 0 to 14)	1		ns
		Digital noise elimination (n = 3)	**Note 2**		ns

Notes 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/DRST).

2. 2Tsamp + 20 or 3Tsamp + 20

Tsamp: Sampling clock for noise elimination

Reset/Interrupt

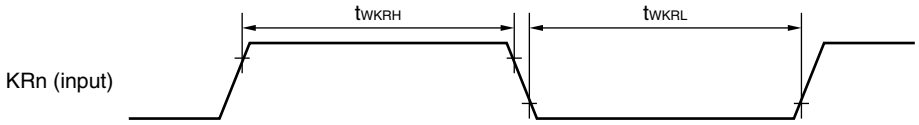


Remark n = 0 to 14

(b) Key return timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
KRn input high-level width	t_{WKRH}	Analog noise elimination (n = 0 to 14)	500		ns
KRn input low-level width	t_{WKRL}		500		ns



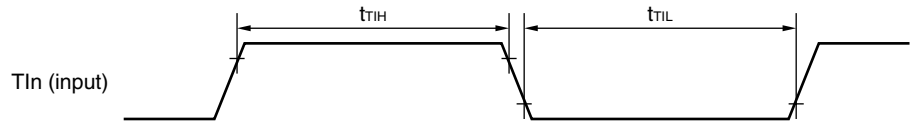
Remark n = 0 to 14

(c) Timer input timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TIn high-level width	t_{TIH}	TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03, TIQ10 to TIQ13, TIQ20 to TIQ23	**Note**		ns
TIn low-level width	t_{TIL}		**Note**		ns

Note 2Tsamp + 20 or 3Tsamp + 20
Tsamp: Sampling clock for noise elimination



Remark TIn: TIP00, TIP01, TIP10 TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03, TIQ10 to TIQ13, TIQ20 to TIQ23

(d) CSIB timing

(i) Master mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCYn}		125		ns
$\overline{SCKBn}$ high-level width	t_{KHn}		$t_{KCYn}/2 - 15$		ns
$\overline{SCKBn}$ low-level width	t_{KLn}		$t_{KCYn}/2 - 15$		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		30		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{KSIn}		25		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	t_{KSOn}			25	ns

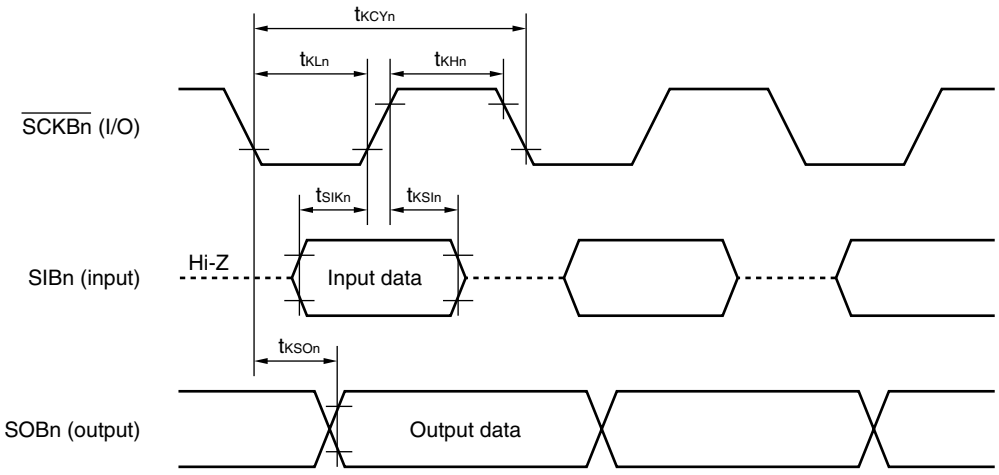
Remark n = 0 to 2

(ii) Slave mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCYn}		200		ns
$\overline{SCKBn}$ high-level width	t_{KHn}		90		ns
$\overline{SCKBn}$ low-level width	t_{KLn}		90		ns
SIBn setup time (to $\overline{SCKBn}\uparrow$)	t_{SIKn}		50		ns
SIBn hold time (from $\overline{SCKBn}\uparrow$)	t_{KSIn}		50		ns
Output delay time from $\overline{SCKBn}\downarrow$ to SOBn	t_{KSOn}			50	ns

Remark n = 0 to 2



Remark n = 0 to 4

*CAN internal clock (fCAN): CAN baud rate clock

(e) UART timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

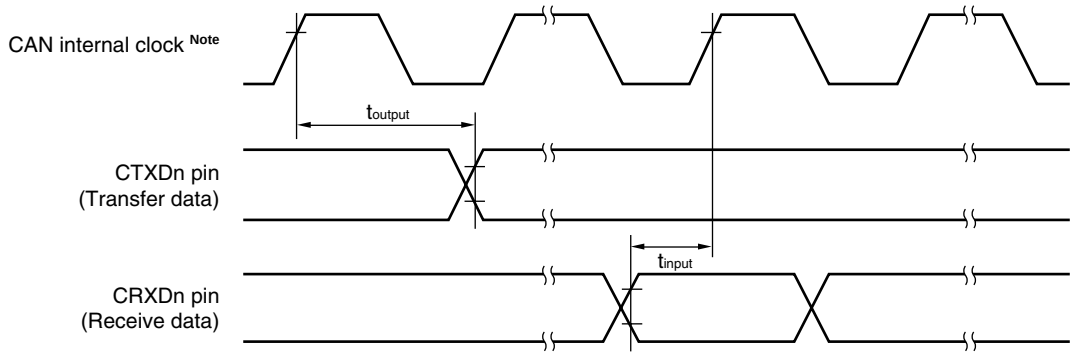
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Communication rate				312.5	kbps
ASCK0 cycle time				10	MHz

(f) CAN timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate				1	Mbps
Internal delay time[Note]				100	ns

Note Internal delay time (t_{NODE}) = Internal transfer delay time (t_{OUTPUT}) + Internal receive delay time (t_{INPUT})



Note *CAN internal clock (fCAN): CAN baud rate clock

Remark n = 0 to 3

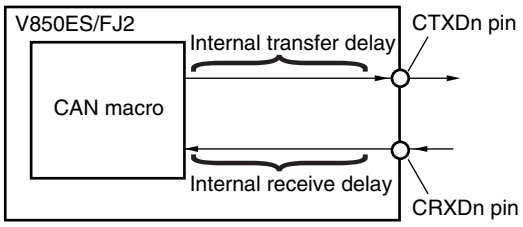


Image figure of internal delay

Remark n = 0 to 3

(g) A/D converter

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		4.0 ≤ AV_{REF0} ≤ 5.5 V		±0.15	±0.35	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV_{REF0} current	I_{AREF0}	When using A/D converter		5	10	mA
		When not using A/D converter		1	10	μA

Note Excluding quantization error (±0.05%FSR). Indicates the ratio to the full-scale value (%FSR).

Remark FSR: Full Scale Range

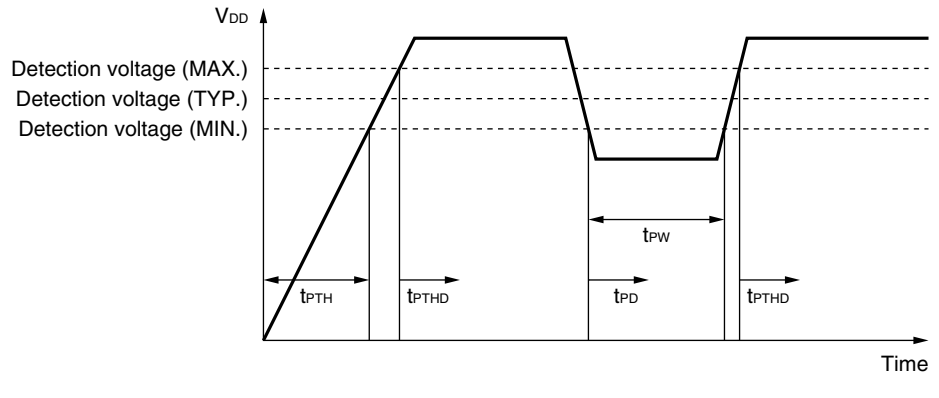
(h) POC circuit characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		3.5	3.7	3.9	V
Power supply startup time	t_{PTH}	V_{DD} = 0 V → 3.5 V	0.002			ms
Response delay time 1[Note 1]	t_{PTHD}	In case of power on. After V_{DD} reaches 3.9 V.			3.0	ms
Response delay time 2[Note 2]	t_{PD}	In case of power off. After V_{DD} drops 3.5 V.			1	ms
Minimum V_{DD} width	t_{PW}		0.2			ms

Notes 1. From detect voltage to release reset signal.

2. From detect voltage to output reset signal.



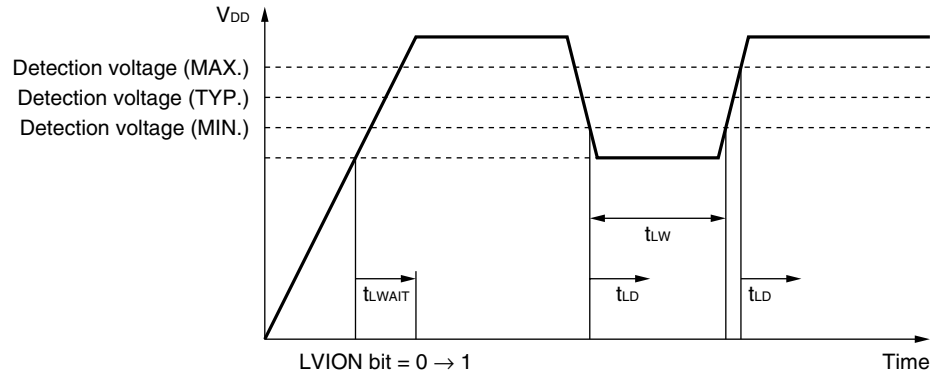
(i) LVI circuit characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.2	4.4	4.6	V
	V_{LVI1}		4.0	4.2	4.4	V
Response time Note 1	t_{LD}	After V_{DD} reaches V_{LVI0}/V_{LVI1} (Max.). After V_{DD} drops V_{LVI0}/V_{LVI1} (Min.).		0.2	2.0	ms
Minimum V_{DD} width	t_{LW}		0.2			ms
Reference voltage stabilization wait time Note 2	t_{LWAIT}	After V_{DD} reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 →1		0.1	0.2	ms

Notes 1. The time required to output an interrupt/reset after the detection voltage is detected.

2. Unnecessary when the POC function is used.

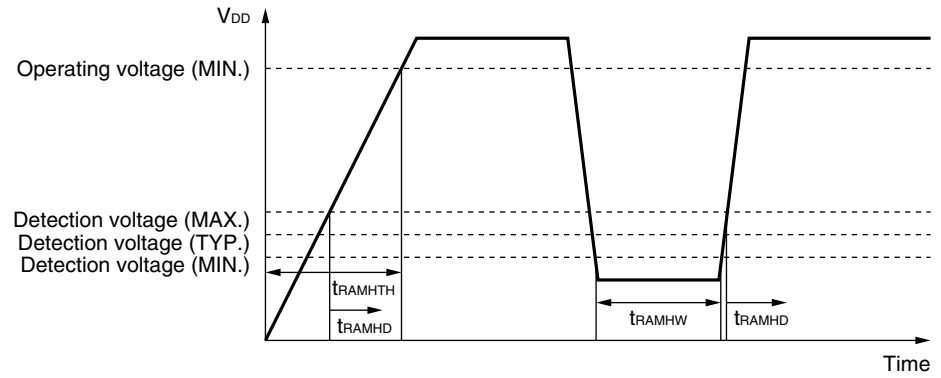


(j) RAM retention flag characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = BV_{DD} = 1.9 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{RAMH}		1.9	2.0	2.1	V
Supply voltage rise time	t_{RAMHTH}	V_{DD} = 0 V → 3.5 V	0.002		1,800	ms
Response time[Note]	t_{RAMHD}	After the supply voltage reaches the detection voltage (MAX.)		0.2	2.0	ms
Minimum V_{DD} width	t_{RAMHW}		0.2			ms

Note Time required to set the RAMF bit after the detection voltage is detected.



(k) Flash memory programming characteristics

(i) Basic characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{CPU}		4		20	MHz
Supply voltage	V_{DD}		3.5		5.5	V
Number of writes	C_{WRT} Note				100	Times
Input voltage, high	V_{IH}	FLMD0	0.8EV_{DD}		EV_{DD}	V
Input voltage, low	V_{IL}	FLMD0	EV_{SS}		0.2EV_{DD}	V
Write time + erase time	t_{IWRT} + t_{ERASE}	Flash: 256 KB (μPD70F3237) 512 KB (μPD70F3239)			T.B.D	s
Programming temperature	t_{PRG}		–40		+85	°C

Note The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

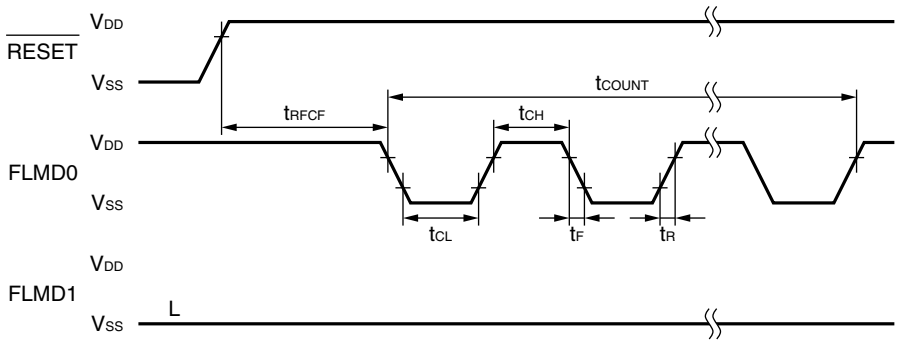
Example: P: Write, E: Erase
Shipped product → P → E → P → E → P: 3 rewrites
Shipped product → E → P → E → P → E → P: 3 rewrites

(ii) Serial Write Operation Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.5 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time from $\overline{\text{RESET}}$↑	t_{RFCF}		5000/fx+ Note			s
Count execution time	t_{COUNT}				3	ms
FLMD0 high-level width	t_{CH}		10		100	μs
FLMD0 low-level width	t_{CL}		10		100	μs
FLMD rise time	t_R				50	ns
FLMD fall time	t_F				50	ns

Note " " represents the oscillation stabilization time.



2. Injected Current Specification

2.1 Injected Current Specification of (A)-Grade

2.1.1 Absolute Maximum Ratings

(Ta = +25 °C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJPM}	Digital input pins	Per pin			4	mA
			Total			50	mA
		Analog input pins	Per pin			4	mA
			Total			20	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJNM}	Digital input pins	Per pin			-4	mA
			Total			-50	mA
		Analog input pins	Per pin			-4	mA
			Total			-20	mA

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.1.2 DC Characteristics for overload current

(**Ta = -40 to +85 °C**, $V_{DD}=EV_{DD}=BV_{DD}$= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}$=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJP}	Digital input pins	Per pin			2	mA
			Total			16	mA
		Analog input pins	Per pin			0.5	mA
			Total			2	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	Digital input pins Note1	Per pin			-0.3	mA
			Total			-2.4	mA
		Analog input pins	Per pin			-0.3	mA
			Total			-1.2	mA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	an adjacent pin of XT2 pin Note2	Per pin			-0.1	mA

Note(s):

2. An adjacent pin of XT2 pin is as follows:

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.1.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(**Ta = -40 to +85 °C**, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current High	I_{LIH}	$V_I = V_{DD}$	Digital input pins				
			I_{INJP} : 2mA(per pin), 4mA(total)		-	0.5	uA
			Analog input pins				
			I_{INJP} : 0.5mA(per pin), 1mA(total)		-	0.2	uA
Input leakage current Low	I_{LIL}	V_I = 0	Digital input pins				
			I_{INJN} : -0.3mA(per pin), -0.6mA(total)		5	40	uA
			I_{INJN} : -0.1mA(per pin), -0.2mA(total)		1	10	uA
			Analog input pins				
			I_{INJN} : -0.3mA(per pin), -0.6mA(total)		5	40	uA
			I_{INJN} : -0.1mA(per pin), -0.2mA(total)		1	10	uA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in Figure 1.
4. TYP. is the value of Ta=+25 °C.

2.1.4 A/D converter influenced by injected current on an adjacent pin

(**Ta = -40 to +85 °C**, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Degradation of Overall error Note1		I_{INJP} : 0.5mA(per pin), 1mA(total)			+/- 0.10	%FSR
		I_{INJN} : -0.3mA(per pin), -0.6mA(total)			+/- 0.25	%FSR

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in Figure 1.

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

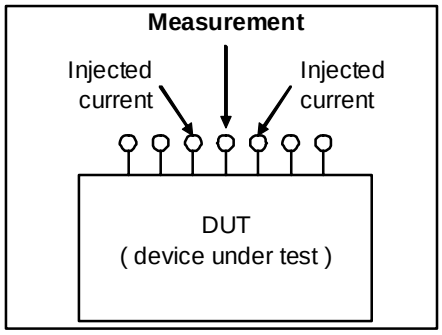
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

10(uA) x 10K(ohm) / 5(V) = 2 %FSR

Figure 1



2.2 Injected Current Specification of (A1)-Grade

2.2.1 Absolute Maximum Ratings

(Ta = +25 °C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJPM}	Digital input pins	Per pin			4	mA
			Total			50	mA
		Analog input pins	Per pin			4	mA
			Total			20	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJNM}	Digital input pins	Per pin			-4	mA
			Total			-50	mA
		Analog input pins	Per pin			-4	mA
			Total			-20	mA

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.2.2 DC Characteristics for overload current

(**Ta = -40 to +110 °C**, $V_{DD}=EV_{DD}=BV_{DD}$= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}$=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJP}	Digital input pins	Per pin			2	mA
			Total			16	mA
		Analog input pins	Per pin			0.5	mA
			Total			2	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	Digital input pins Note1	Per pin			-0.3	mA
			Total			-2.4	mA
		Analog input pins	Per pin			-0.3	mA
			Total			-1.2	mA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	an adjacent pin of XT2 pin Note2	Per pin			-0.1	mA

Note(s):

2. An adjacent pin of XT2 pin is as follows.

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.2.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(**Ta = -40 to +110 °C**, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current High	I_{LIH}	$V_I = V_{DD}$	Digital input pins				
			I_{INJP} : 2mA(per pin), 4mA(total)		-	2	uA
			Analog input pins				
			I_{INJP} : 0.5mA(per pin), 1mA(total)		-	2	uA
Input leakage current Low	I_{LIL}	$V_I = 0$	Digital input pins				
			I_{INJN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I_{INJN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA
			Analog input pins				
			I_{INJN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I_{INJN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in Figure 2.
4. TYP. is the value of Ta=+25 °C.

2.2.4 A/D converter influenced by injected current on an adjacent pin

(**Ta = -40 to +110 °C**, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Degradation of Overall error Note1		I_{INJP} : 0.5mA(per pin), 1mA(total)			+/- 0.10	%FSR
		I_{INJN} : -0.3mA(per pin), -0.6mA(total)			+/- 0.25	%FSR

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in Figure 2.

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

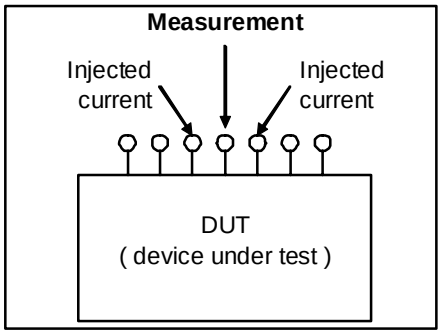
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

10(uA) x 10K(ohm) / 5(V) = 2 %FSR

Figure 2



2.3 Injected Current Specification of (A2)-Grade

2.3.1 Absolute Maximum Ratings

(Ta = +25 °C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJPM}	Digital input pins	Per pin			4	mA
			Total			50	mA
		Analog input pins	Per pin			4	mA
			Total			20	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJNM}	Digital input pins	Per pin			-4	mA
			Total			-50	mA
		Analog input pins	Per pin			-4	mA
			Total			-20	mA

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

Remark: Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.

2.3.2 DC Characteristics for overload current

(**Ta = -40 to +125 °C**, $V_{DD}=EV_{DD}=BV_{DD}$= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}$=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Pos. Overload Current $V_{IN} > V_{DD}$	I_{INJP}	Digital input pins	Per pin			2	mA
			Total			16	mA
		Analog input pins	Per pin			0.5	mA
			Total			2	mA
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	Digital input pins Note1	Per pin			-0.3	mA
			Total			-2.4	mA
		Analog input pins	Per pin			-0.3	mA
			Total			-1.2	mA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Refer to the next pages for Input leakage current and A/D characteristics.

Note(s):

1. In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Neg. Overload Current $V_{IN} < V_{SS}$	I_{INJN}	an adjacent pin of XT2 pin Note2	Per pin			-0.1	mA

Note(s):

2. An adjacent pin of XT2 pin is as follows.

V850ES/FE2: P00 pin, V850ES/FF2: P05 pin, V850ES/FG2: P02 pin, V850ES/FJ2: P02 pin

2.3.3 DC Characteristics for pins influenced by injected current on an adjacent pin

(**Ta = -40 to +125 °C**, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current High	I_{LIH}	$V_I = V_{DD}$	Digital input pins				
			I_{INJP} : 2mA(per pin), 4mA(total)		-	5	uA
			Analog input pins				
			I_{INJP} : 0.5mA(per pin), 1mA(total)		-	3	uA
Input leakage current Low	I_{LIL}	V_I = 0	Digital input pins				
			I_{INJN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I_{INJN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA
			Analog input pins				
			I_{INJN} : -0.3mA(per pin), -0.6mA(total)		5	60	uA
			I_{INJN} : -0.1mA(per pin), -0.2mA(total)		1	15	uA

Remark(s):

1. Analog input pins are pins of Port7 and Port12. Digital input pins are pins except analog input pins.
2. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
3. Measurement conditions are shown in Figure 3.
4. TYP. is the value of Ta=+25 °C.

2.3.4 A/D converter influenced by injected current on an adjacent pin

(**Ta = -40 to +125 °C**, V_{DD}=EV_{DD}=BV_{DD}= 3.5V to 5.5V, AV_{REF0}= 4.0V to 5.5V, V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Degradation of Overall error Note1		I_{INJP} : 0.5mA(per pin), 1mA(total)			+/- 0.10	%FSR
		I_{INJN} : -0.3mA(per pin), -0.6mA(total)			+/- 0.25	%FSR

Remark(s):

1. These specifications are not tested in outgoing inspection, but specified based on the device characterization.
2. Measurement conditions are shown in Figure 3.

Note(s):

This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Caution(s):

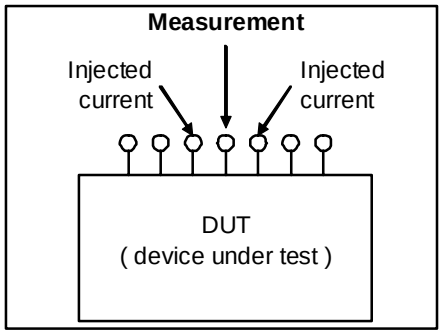
When there is a leakage current, the effect on the ADC accuracy depends on the external analog source impedance.

Example) Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm

If there is a leakage current of 10uA by injected current, the effect on the ADC accuracy is

10(uA) x 10K(ohm) / 5(V) = 2 %FSR

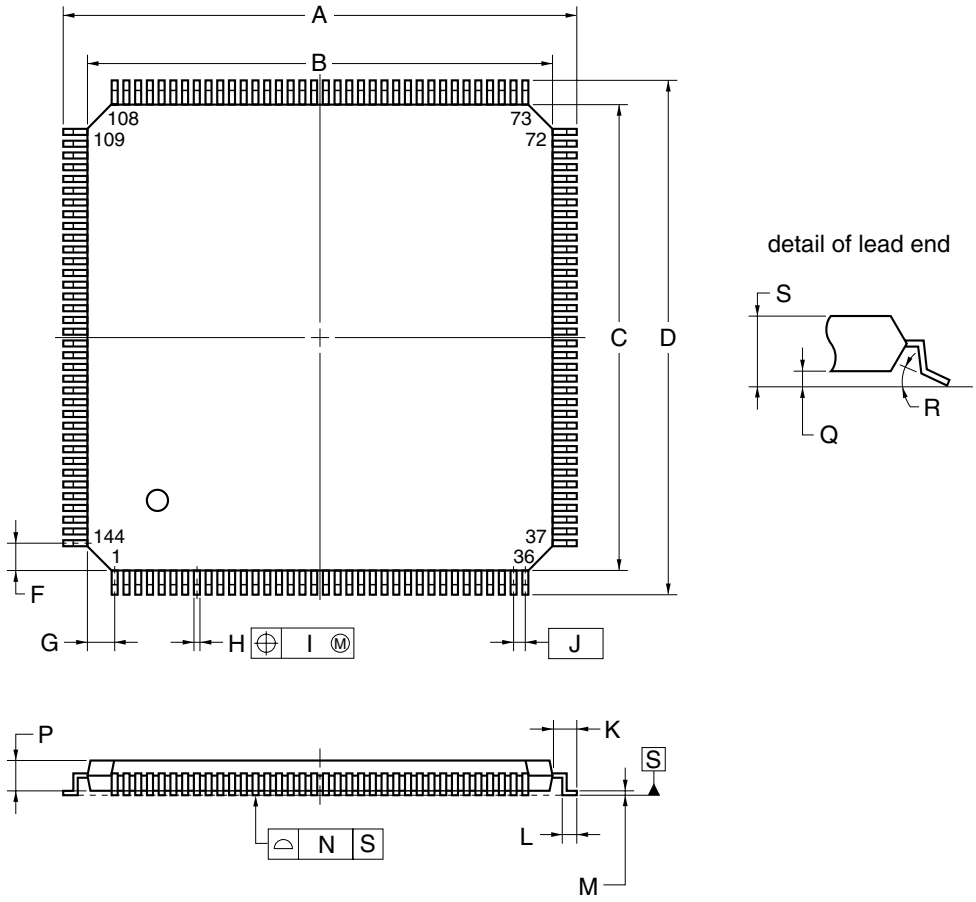
Figure 3



3. Package Drawing

Figure 3-1: Package Drawing

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

4. Recommended Soldering Conditions

Table 4-1: Soldering Conditions

(1) μPD70F3239MxGJ(Ax)-UEN, μPD70F3238MxGJ(Ax)-UEN, μPD70F3237MxGJ(Ax)-UEN

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared Reflow	Package Peak Temperature: 260°C Time: 30 seconds max. (210°C min.) Count: 3 max Exposure Limit: 7 days[Note]	IR60-207-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period. After that, prebaking is necessary at 125 °C for 20 to 72 hours.